國 立 交 通 大 學

工學院半導體材料與製程設備研究所

碩 士 論 文

探討化學氣相沉積在先進動態隨機存取記憶體淺溝槽絕緣的
填洞能力

**Study of Shallow Trench Isolation Gap Filling Capability
for Advanced DRAM by Chemical Vapor Deposition**

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指導教授：潘 扶 民 博士

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碩 士 論 文

A Thesis

Master Degree Program of Semiconductor Material and Processing Equipment

College of Engineering

National Chiao Tung University

in Partial fulfillment of the Requirement

for the Degree of Master of Science

in

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摘要

　　在於本碩士論文裡, 我們旨在利用 HARP-SACVD 以化學氣相沉積方式來探討如何以沒有摻質的玻璃來延伸先進動態隨機存取記憶體淺溝絕緣的填動能力。根據這次實驗結果，三步驟的沉積方式可以滿足，並沒有發現縫道在 60 奈米的槽寬度以及 AR 7:1 槽溝之填洞結果。第一步沉積是利用較高的 Ozone /TEOS 比例來得到極佳的階梯覆蓋，減少表面的選擇性，第二步沉積旨在不改變 Ozone/TEOS 之比例下，利用較少 TEOS 的流量來完成淺溝槽之填洞。而最後的沉積目的是增加晶片之生產量。

　　在本實驗中亦探討 TEOS 的初期流量以及完成 HARP 之玻璃沉積後回火處裡方式對淺溝槽填洞能力之影響。

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ABSTRACT

In this thesis, we explored the extendibility of shallow trench isolation (STI) gap filling capability of undoped silicate glass (USG) prepared by high aspect ratio process (HARP) in sub-atmosphere chemical vapor deposition (SACVD) systems for sub-70 nm technology nodes for the advanced dynamic random access memory (DRAM) applications. Based on the study, a 3-step deposition process, which is capable of achieving void free gap filling at 0.06μm trench width and > 7:1 aspect ratio with a smooth profile of trench sidewall, was developed. The first step is to deposit a homogeneous nucleation layer with trivial surface selectivity by using a gas source with a high $O_3/$ tetraethoxysilane (TEOS) ratio so that better film conformality can be

achieved. The second step is to deposit a sufficiently thick USG to fill trenches with a small to moderate width by using a gas feed of a relatively high O_3/TEOS ratio. The final step is targeted at throughput enhancement. The effect of initial TEOS composition and annealing treatment after the HARP USG deposition on the trench filling capability was also studied.

Key Words: O_3/TEOS, DRAM, shallow trench isolation, HARP, SACVD, USG, Gap filling, aspect Ratio, annealing.

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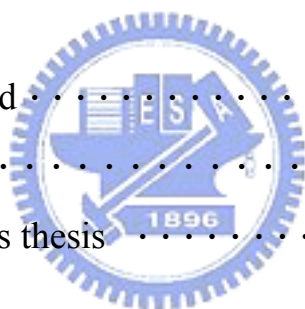
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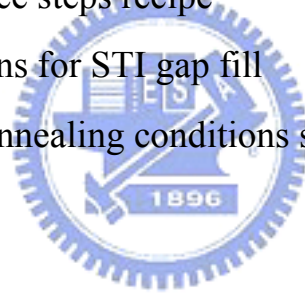
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Chapter 1
Introduction

1.1 General Background

Shallow trench isolation (STI) has rapidly become a vital electrical isolation scheme as CMOS technologies are scaled down below 0.25µm generation. This technique has the advantages of having no bird's beak and no encroachment. When two devices are separated by a trench, the electrical field lines have to travel a longer distance and change direction twice, so there are considerably weakened. Therefore, STI provides abrupt transition from active device to isolation regions and is adequate for preventing punch-through and latch-up phenomena [1]. In addition, this technology can concurrently achieve good planarity. One of the process steps involved in STI technique is trench-fill dielectrics for STI, which is where un-doped silicate glass (USG) is deposited.

Many challenges are encountered in the design of the STI process for electrical isolation. The greatest challenge lies on providing void-free, seamless gap filling by oxide deposition. Voids and seams formed during deposition can be enlarge during subsequent CMP and HF etching processes and filled with poly-silicon. This will cause gate-to-gate short failure, junction leakage and degrade overall parametric results and affect chip yields. Moreover, as device dimensions continue to shrink, the distance between

transistors active areas and STI side-wall also narrow, they become highly critical to obtain good gap filling to avoid deleterious device behavior.

In this study, we conducted screening tests based on different theories and empirical process approaches. A thermal process of HARP SACVD, based on O_3/TEOS chemical vapor deposition, to improve USG process significantly on two important fronts, improves gap filling capability of shallow trench isolation, and ensures no plasma damage to devices.

1.2 Motivation

Rapid progress in transistor scaling has made gap fill technology critical for all advanced devices, as the dimensions of ULSI circuits continue to shrink below nanometer technology. The requirements for shallow trench isolation (STI) include voids free gap filling, better conformal step coverage, low wet etch rate and metallic contamination. It is found that HDP is increasingly finding it difficult to provide a good gap-fill solution for the more aggressive STI structures at technology nodes of < 0.07μm. A viable alternative HARP SACVD based on O_3/TEOS ratio is on developing to achieve all requirements for the advanced dynamic random access memory (DRAM). A understanding of alternative techniques such as the methodology of furnace annealling for HARP USG is required for trench gapfill. Finally, A comprehensive understanding of the next generation of STI films and structure types is required to provide void free gap-fill

HDP-USG

Pad Nitride

Void

Aspect Ratio =7:1

space width is 80nm
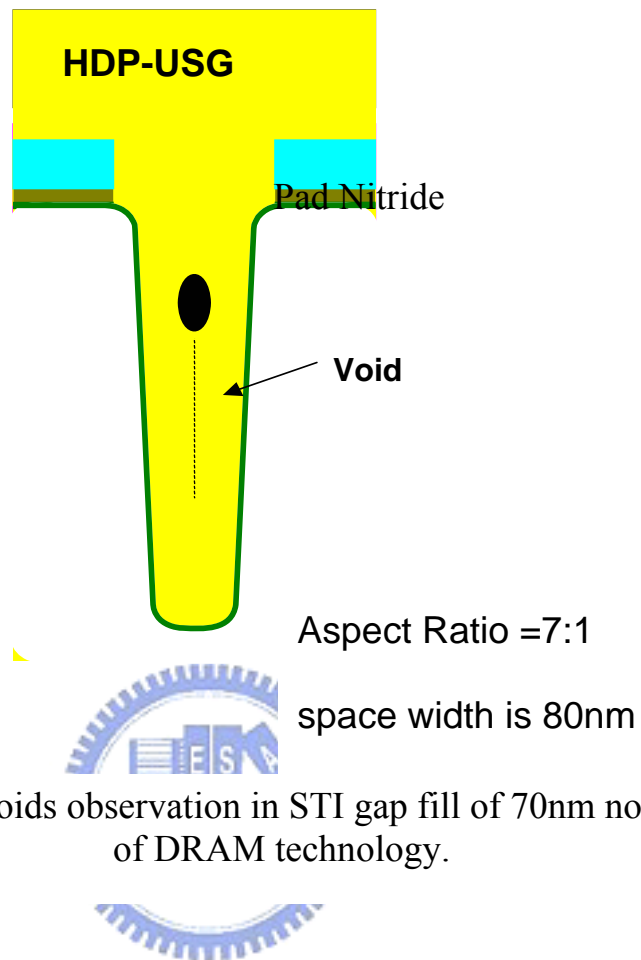
Figure 1.1   Voids observation in STI gap fill of 70nm node
of DRAM technology.

1.3 Organization of This Thesis

There will be five chapters in this thesis compositions.

Chapter 1 introduce to the general background of shallow trench isolation
and what challenge will be suffering if future .

Chapter 2 presents dielectric chemical vapor deposition basic theory and the process concepts of dielectric CVD likes SACVD, PECVD and HDPCVD.

Chapter 3 demonstrates the film properties of HARP USG films in SACVD as a function of deposition rate, wet etch rate and shrinkage rate   in variation of depsotion temperature, ozone concentration and process pressure. The effect of the trench filling with annealing and without annealing is also be explored.

Chapter 4 reveals the results of film properties and reliability in HARP SACVD and the shallow trench isolation gap fill capability through the experiement.

The final chapter makes conclusions for this thesis.

Chapter 2
Chemical vapor deposition

2.1 Overview of thin film deposition

Chemical vapor deposition (CVD) is a technique for synthesizing materials in which chemical components in vapor phase react to form a solid film at surfaces. The occurrence of a chemical reaction is essential to these means of film growth, as it is the requirement that reactants must start out in vapor phase. Ability to control the components of the gas phase, and the physical conditions of the gas phase, the solid surface, and the envelope surrounding them determines our capability to control the properties of thin films that to be produced.

CVD is a sequential process which starts from initial vapor phase, progress through a series of quasi steady states sub-process, and culminates in the formation of solid film in its final microstructure. This sequence is illustrated schematically in figure 2.1 **[2] [3]**.

  a. Diffusion of gaseous reactants to the surface.

  b. Adsorption of the reacting species on to surface sites, often after some migration on the surface.

  c. Surface chemical reaction between the reactants, usually catalyzed by the surface.

  d. Desorption of the by-products away from the surface.

  e. Diffusion of the by-products away from the surface.

f. Incorporation of the condensed solid product into the microstructure of the growth film.
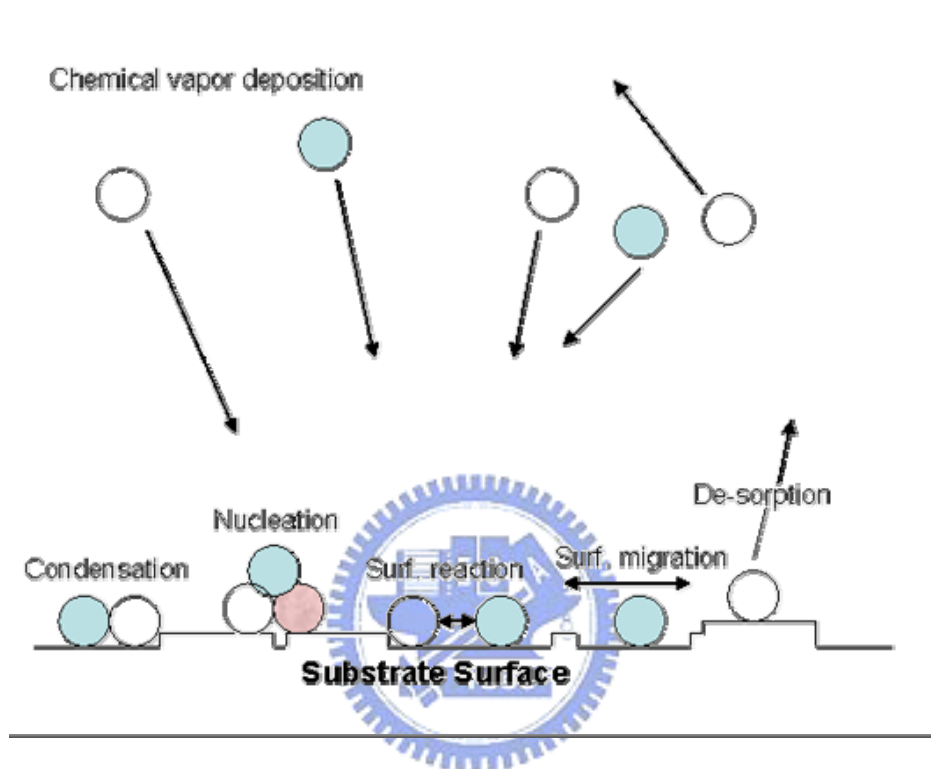
Figure 2.1   Schematic of events that occur around the substrate surface.
Summation of these events leads to deposition on the wafer.

In microelectronic applications, semiconductor films are patterned to form electronic devices. Conductive films act as a conduit through which electrical signals are transited to and away from these devices. Dielectric films are used to isolate devices to each other and to insulate the conductive wires. The application is enough to deduce many of the properties requirement by dielectric films used in microelectronics **[4].** For instance, a dielectric film should have a very low electrical conductance, high breakdown strength, and

should be physically void-free. Conversely, a conductive film should exhibit high electrical conductance and should has good long-term reliability under conditions of high current density **[5]**. Since many electrical devices are formed in mono-crystalline semi-conductive films, crystallographic perfection is essential, these are the generic requirements for the three kinds of films in microelectronic.

During the past several years, CVD has become an essential part of very large scale integrated circuit (VLSI) manufacturing. More and more film layers are attempted using CVD due to its often superior conformality. Newer CVD techniques are being developed for the deposition of more layers. It is importance to understand the fundamentals of chemical vapor deposition are therefore crucial to the development of an integrated process for manufacturing large-scale ICs.

In the early 1980s, low power consumption complementary MOS (COMS) circuits started to be dominant in IC design. Today, most ICs are CMOS based. Even though electrical conductivity is the main feature that separates conductors from dielectrics, the roles played by dielectrics in microelectronics are more varied when compared to the applications of conductors. Silicon based integrated circuit technology owes its popularity in no small measurement to the existence of a stable native dielectric silicon dioxide. SiO_2 is used as the gate oxide in most devices, where it dictates their performance. Dielectrics are used to isolate electrically active components, either semiconductors or conductors, and they are used as capacitors, they provide protection for the device from ambient impurities and moisture.
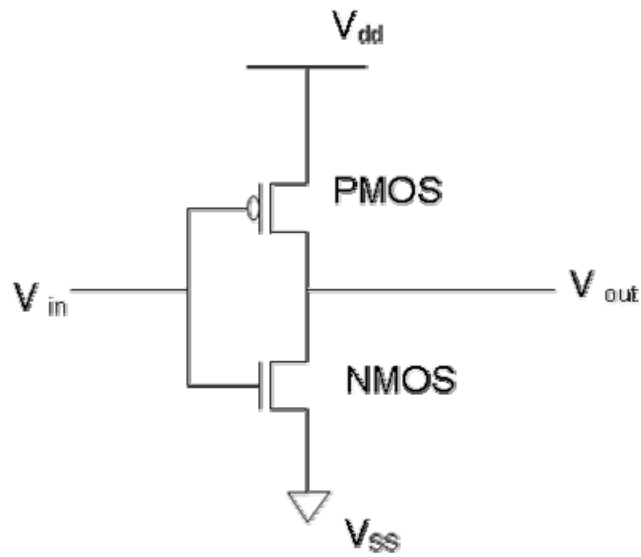
Figure 2.2   Complementary MOS (CMOS) Inverter.

(a)   (b)
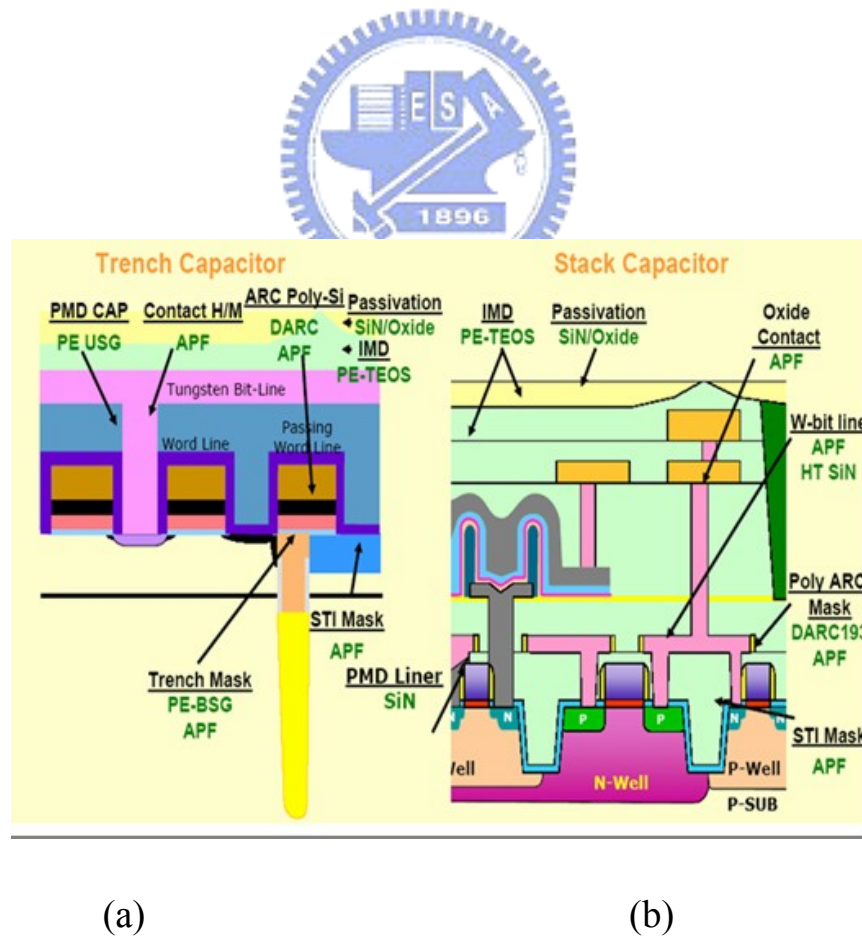
Figure 2.3   DRAM Structures: (a) Trench DRAM, (b) Stack DRAM.

2.2 CVD of dielectrics

There are two kinds of dielectrics in an IC chip, thermally grown dielectrics and chemical vapor deposition dielectrics. Gate oxide is a process of thermally grown oxide layers **[6] [7]**.

SiO2		SiO2
Silicon	Silicon	Silicon
Thermally grown oxide	Silicon Substrate	CVD dielectric film
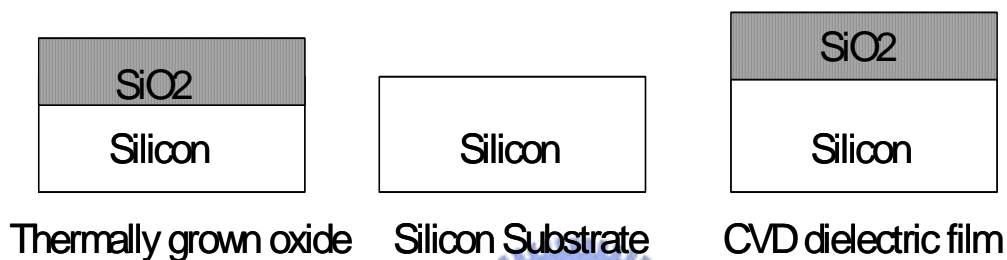
Figure 2.4 Show thermally grown oxide and CVD dielectric film.

Thermal oxidation offers the best quality for Si-SiO$_2$ interface and thus it has a low interface trap density. Therefore, it is almost used to form the gate oxide and field oxide. The following chemical reactions describe the thermal oxidation of silicon in oxygen or water vapor.

$$Si_{(solid)} + O_{2\ (gas)} \longrightarrow SiO_{2(solid)}$$

$$Si_{(Solid)} + 2H_2O_{(gas)} \longrightarrow SiO2_{(solid)} + 2H_{2(gas)}$$
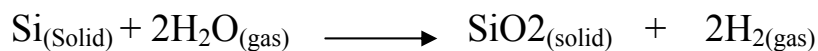
CVD dielectrics are mainly used for making interconnections and shallow trench isolation **[8]**. With device dimensions shrinking and the number of transistors increasing, one layer of metal is no longer enough to connect all transistors, thus, two or more metal layers are employed for making the interconnections.

For IC chips with two metal layers, three metal CVD dielectric layers are needed: pre-metal deposition (PMD), the dielectrics between the two metal layers, or inter-metal dielectrics (IMD), and passivation film deposition.

As device dimensions continue shrinking to sub-micron, more metal layers are needed for making the interconnections. The CMOS IC devices below, with seven layers of metal, needed eight CVD dielectric layers, one pre-metal deposition, six inter-metal depositions and one final passivation film. But for dynamic random access memory (DRAM), there is only three metal layers are employed for making interconnections in even technology goes to 70nm node generation and beyond.

2.3 Thin film phenomena

Having introduced the phenomena that occur during the growth of thin films, let us explore the properties of thin films, from a structural view-point, we will examine the way of physical, mechanical, and electrical properties, that which are affected by the film structure and microstructure. We will also examine deviations in material properties on going from bulk to thin film.

2.3.1 Physical properties of thin films.

Density or specific gravity of thin films can be determined through weight gain measurements using microbalances. We often observe an increasing in density in thin films with increasing thickness, with the bulk density as the upper limit. This phenomenon has been attributed to the smaller grain size and the increased grain boundary area, which is normally less dense than the grain itself [9]. More often, thinner films tend to contain microscopic voids that decrease as a percentage of the film volume as the film grows thicker. The tendencies that lead to crystallographic perfection generally lead to an increase in film density. Density of the film often correlates to resistivity and other film properties affected by the presence of voids.

Surface roughness arisen from the random nature of nucleation and coalescence [10]. Deviation from the average thickness Δt for films grown at relatively low temperature and at limited surface mobility can be modeled according to a poisson distribution.

$$\Delta t \propto \sqrt{t}$$

In characterizing roughness, both Δt and the periodicity of the peaks and valleys need to be accounted for. Various optical scattering and surface profile-metric techniques have been developed to characterize roughness. Another contributor to surface roughness is the presence of surface grooves. Since higher temperatures often results in large grooves, a direct relationship can be observed between roughness and temperature of growth. In this

situation, measurement of surface roughness yields a direct measuring of the film grain size distribution. Surface roughness acts as an excellent indicator of surface contamination. Often deviation in the film roughness can be directly attributed to leak in the deposition systems and the presence of gaseous impurities such as oxygen **[11]**.

2.3.2 Mechanical properties of thin films

2.3.2.1 Adhesion

The adhesion of grown and deposited films used in ULSI processing must be excellent. If the films lift from the substrate device failure can be result, and thus poor adhesion will represent a potential reliability problem.

Adhesion is also strongly affected by the cleanliness of the substrate. Contamination generally results in poor adhesion, as does an adsorbed gas layer. Cleaning the substrate prior to deposition is therefore important to insure film adhesion capability. Substrate surface roughness can also affect adhesion **[12]**, for example, increased roughness may promote adhesion because the substrate exhibits more to surface area than to flat surface, and mechanical interlocking between the film and the substrate may also occur. Excessive roughness, on the other hand, results in coating defects, which may promote adhesion failure.

It is highly advantageous to include a layer of a strong oxide-forming element between the oxide substrate and the metallization. This is particularly

true for gold-based metallization, where a chromium layer can be used to serve as an intermediate "adhesion layer" **[13] [14]**. **T**he intrinsic stress in thin film is generally not sufficient to result in de-lamination, unless the film is extremely thick. More often, high stress results in the cracking of films.

2.3.2.2 Stress in thin film.

Nearly all films are found to be in a state of internal stress, regardless of the means by which they have been produced. The stress may be compressive or tensile: Compressive stressed films would like to expand parallel to the substrate surface, and in the extreme, film in compressive stress will buckle up on the substrate. Films in tensile stress on the other hand, would like to contract parallel to the substrate, and may crack if their elastic limits are exceeded. In general, the stress in thin film is in the range of 10^8 to 5×10^{10} dynes/cm^2.

The total stress Q, in a film is the sum: a) any external stress Q_{ext}, on the film, perhaps from another film; b) the thermal stress $Q_{th:}$ and c) the intrinsic stress $Q_{int.}$ The total stress is written as:

$$Q = Q_{ext+}\ Q_{th+}\ Q_{int}$$

The thermal stress is easily to model, it arises from the difference in thermal expansion between the film and the substrate. During cooling from growth temperature, the film assumed to be tensile stress state if the film wants

to contract more than the substrate will allow. Conversely, the film assumes a compressive stress state if the substrate contracts more than the film wants to.

Intrinsic stress reflects the film structure in ways not yet completely understood **[15]**. It has been observed that the intrinsic stress in a film depends on thickness, deposition rate, deposition temperature, ambient pressure, method of film preparation, and type of substrate used, among other parameters.

Measurement of stress in the thin film can often be accomplished by measuring the curvature of the substrate, either as a disk or as a strip. Interference rings, laser holography, traveling microscopes, and optical curvature measurement techniques have been used to measure curvature of disks and deflection of the strip.
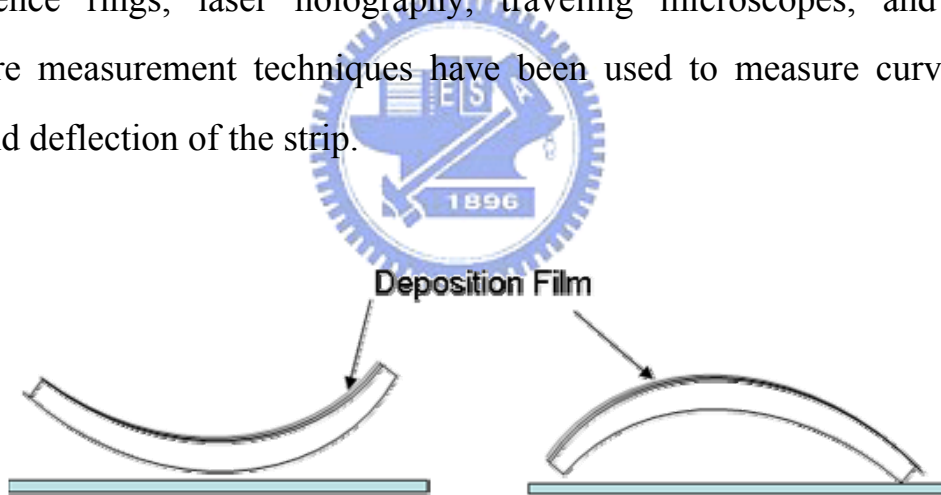
Figure 2.5   (a) Tensile stress causes concave bending, and

(b) Compressive stress causes convex bending of substrate.

2.3.3 Electrical properties of thin films.

The electrical conductivity of a material is due to the motion of charge carriers through the lattice under the influence of applied electric fields **[16]**. Here I will introduce the properties of dielectric film.

As a class of materials, dielectrics exhibit large energy gaps in their band structure, with few free electrons to participate in electrical conduction. Band gaps in dielectrics can be on the order of a few electron volts. The important characteristics of the dielectric constant that affect its usefulness in microelectronic application are the dielectric constant, the breakdown strength, and the dielectric loss. Dielectric constant or permittivity is a measure of the amount of electrical charge a material can withstand at a given electrical field strength, not to be confused with dielectric strength. For a nonmagnetic, non-absorbing material, the dielectric constant is the square of the index of refraction. A vacuum, the perfect dielectric, has a dielectric constant of unity.

The capacitance C in farads of a parallel-plate capacitor shown in figure 2.6 with surface area A and a dielectric of thickness t in centimeters is given by
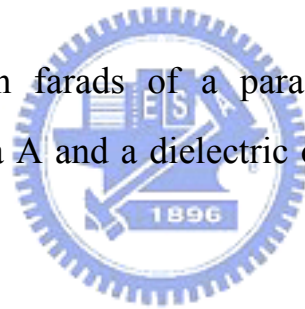
$$C = \varepsilon_o \varepsilon A / 4\, t = 8.85 \times 10^{-14} \varepsilon A / t$$

A high dielectric constant is required to obtain high values of capacitance for a storage capacitor in a DRAM. Interconnect applications require low capacitance between adjacent metal lines. Even though smaller thickness can result in a high value of the capacitance, dielectric strength or breakdown strength is a measurement of the resistance of the dielectric to electrical breakdown under the influence of strong fields [17]. The structural integrity of insulator, the presence of pinholes and metallic contaminants reduce the dielectric strength.

Dielectric loss is a measure of frictional loss, dissipated as heat, in the presence of a varying electric field. The loss occurs because electric polarization in a dielectric is unable to follow the electric field.
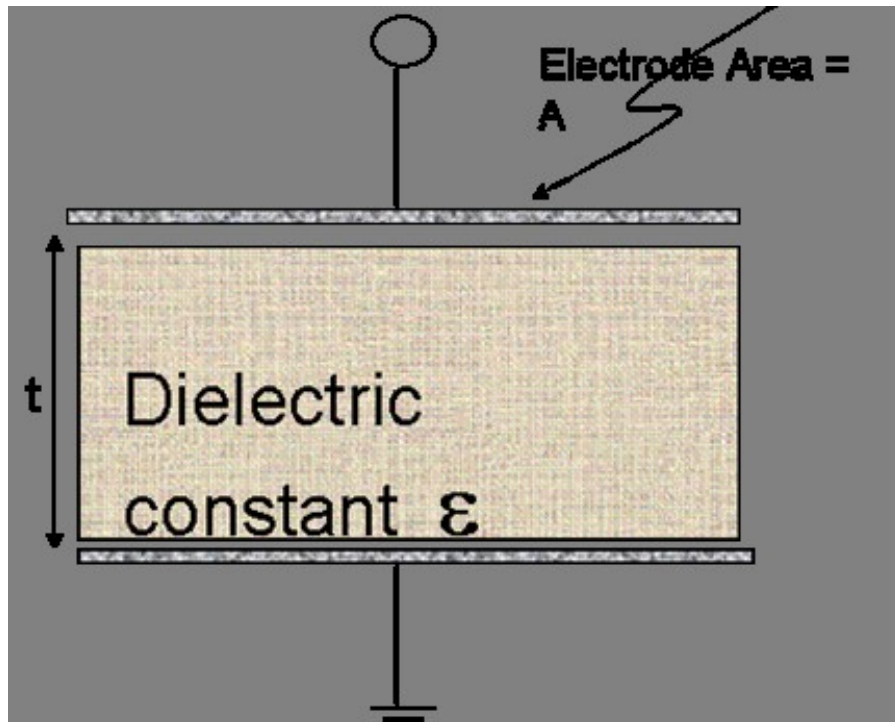
Figure 2.6   A parallel-plate capacitor.

2.3.4 Special properties requirements for microelectronics

Even though there are some introduction of general properties of thin films, such as mechanical characteristics and electron transport, there are certain unique requirements for thin films in microelectronics. These requirements are extensions of the properties discussed in the proceeding sections:

2.3.4.1 Conformability and step coverage

Conformability of a thin film refers to its capability to exactly reproduce surface topography of the under substrate. Conditions during growth and subsequent annealing, along with intrinsic properties of the materials determine conformality **[18]**. In some cases, geometrical constraints of the substrate topography preclude conformality. These concepts are illustrated in figure 2.7. The need for conformality arises because microelectronic processing proceeds by successively depositing and patterning features on thin films. If successive films do not follow the patterns created on the previous layers, voids in deposited layers begin to form. Etching these layers may result in stringers. These can lead to electrical shorts and opens, or to the failure caused by trapped material in the voids.

Sidewall step coverage = b/a   Conformality = b/c
Bottom step coverage = d/a   Overhang = (c-b)/a
Ration of Depth to width = h/w.
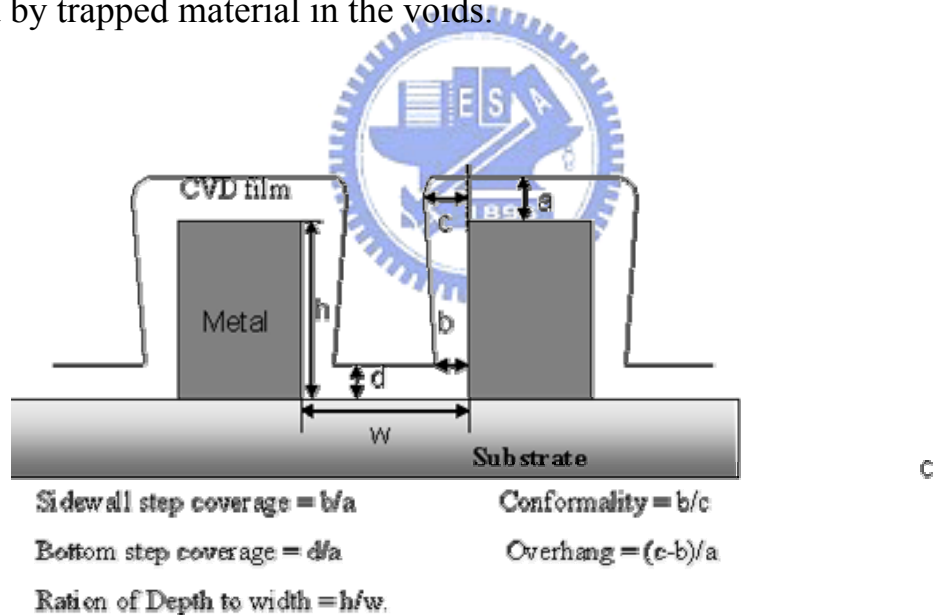
Figure 2.7   Step coverage and the related terms.

Arrival Angle and surface mobility can contribute significantly to conformality. However, even though surface mobility is a necessary condition for good step coverage, it is far from being sufficient. Conformality over a right-angled step is termed step coverage, the largest arriving angle it does at

the overhang of the step corner [19]. For the same step height, the narrower the gap, the smaller the arriving angle, and the harder it is to fill.

At lower pressure, the mean free path of the particle is longer, so it can affectively reduce the arriving angle at the step corner and improve sidewall step coverage.
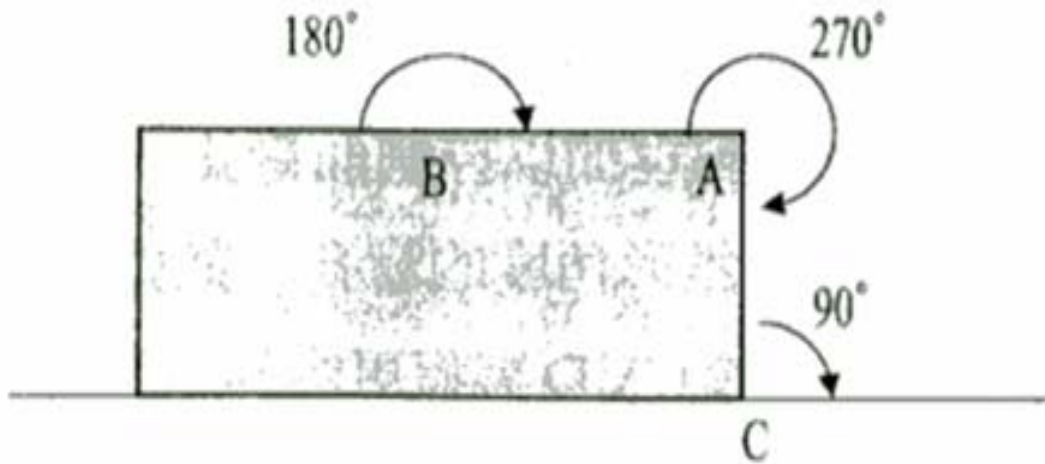
Figure 2.8   Arrival angle and surface mobility.

2.3.4.2 Planarity

A related film properties to conformality is palnarity. Lithographic imagers are used in microelectronic manufacturing to pattern very small features on the substrate, these image tools have limited depths of focus and hence require that each successive layer is sufficiently planar [20]. Planarity, can be achieved by many means, some of which are unrelated to CVD. However, one of the techniques used in planarization is the thermal flowing of doped oxide glasses deposited by CVD under elevated temperature. Figure 2.9 shown a cross-sectional electron micrograph of a thermally deposited

phosphosilicate glass deposited by CVD before and after reflow at a temperature of 800℃. Notice the improvement in the planarity.
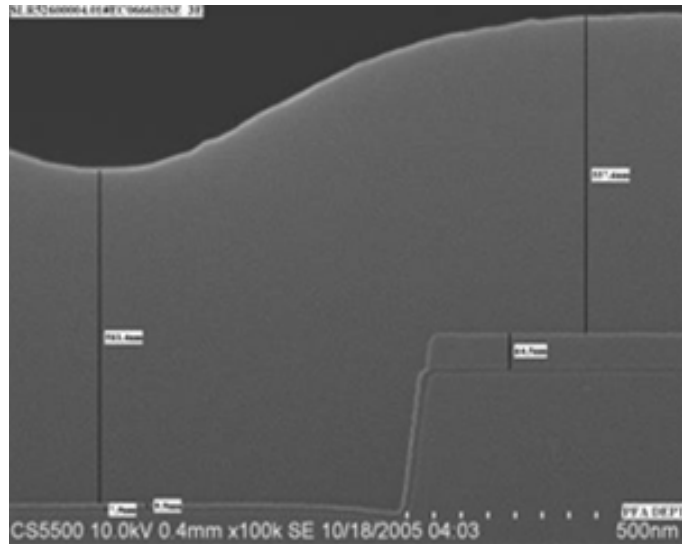
Figure 2.9   Reflow achieves planarity in doped oxide films.

2.3.5 Chemical reaction kinetics

Chemical kinetics is the study of the rate and the mechanism by which one chemical species is converted to another. The rate of a reaction is the mass in moles of a product species produced or reactant species consumed in unit time. It can be expressed as

R = Moles with component formed / Mass of solid x time

By the term mechanism it can be account for all the individual collision processes involving the reactant and product atoms that result in the overall rate.

2.3.5.1 Temperature dependence of rate

The rate constant k relates to overall rate of the reaction to the concentration dependent terms. It has been found to be a strong function of temperature and is well represented empirically by the Arrhenius Law [21].

$$k=A \exp (-Ea / kT)$$

A is the collision frequency term and Ea is the activation energy. The terms collision frequency and activation energy arise out of the concept of an activated complex.
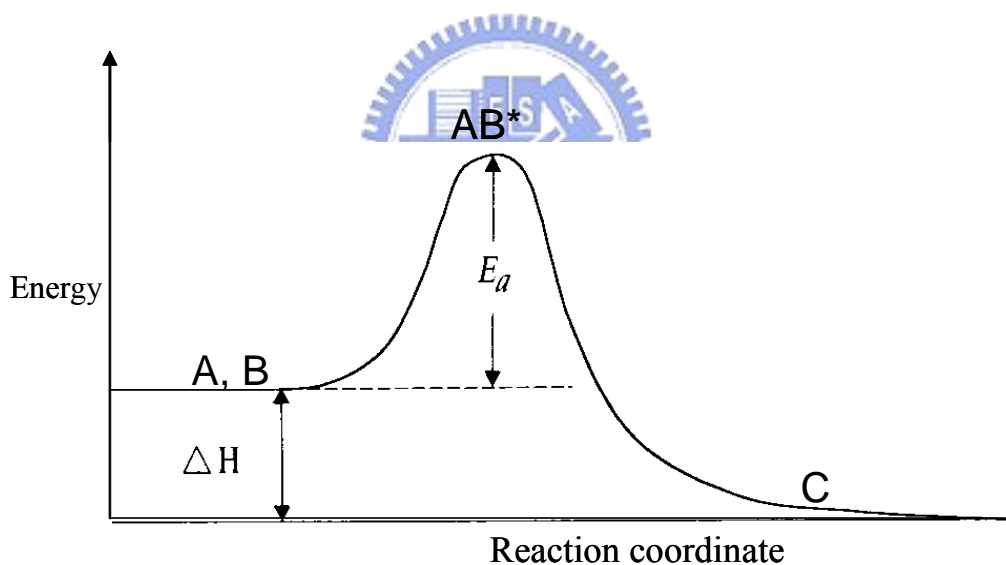
Figure 2.10   Activation energy of the: the change in energy of a reacting species as the reaction proceeds forward the energy needed for the reactants.

AB* is called the activated complex and is in equilibrium with A and B. The energetic of the reaction are shown in figure 2.10. The activated complex is formed by the collision of A and B molecules and is incapable energetically of existing itself. C is formed out of the decomposition of AB*. The rate of

formation of C is only dependent on thee concentration of AB* and its rate of decomposition.

2.3.5.2 Surface reaction and mass transfer controlled growths

Because the deposition process includes force convection, boundary-layer diffusion, surface absorption, decomposition, surface diffusion, and incorporation, there are several variables to be controlled. Temperature, pressure, flow rate, position, and reaction ratio all are important factors for high-quality films. The industry has optimized these conditions to improve the film properties.

Since the aforementioned steps for a CVD process are sequential, the one that occurs at the slowest rate will determine the deposition rate. The rate-determining steps can be grouped into gas-phase processes and surface processes [22]. For the gas-phase process, the concern is the rate at which gases impinge on the substrate. This model considers the rate at which gases cross the boundary layer that separates the bulk regions of flowing gas and substrate surface. Such transport processes occur by gas-phase diffusion, which is proportional to the diffusivity of the gas and the concentration gradient across the boundary layer. The rate of mass transport is only relatively weakly influenced by the deposition temperature.

On the other hand, at low temperature the surface reaction rate is reduced, and eventually the arrival rate of reactants exceeds the rate at which they are consumed by the surface reaction process. Under such conditions, the deposition rate is surface reaction rate limited. Thus, at high temperature, the deposition is usually mass transport limited, while at low temperature it is

surface reaction rate limited, as shown in figure 2.11. In actual processes the temperature at which the deposition condition moves from one of these growth regimes to the other depends on the activation energy of the reaction and the gas flow conditions in the reactor. In processes that are under surface-reaction-rate-limited conditions, the deposition temperature is an important parameter [23]. That is, uniform deposition rates throughout a reactor require conditions that maintain a constant reaction rate. This, in turn, implied that a constant temperature must also exist everywhere at all wafers. On the other hand, under such conditions the rate at which reactant arrive at the surface is not so important, because their concentrations do not limit the growth rate. Thus, it is not so critical that a reactor be designed to supply an equal flux of reactants to all locations of a wafer surface.
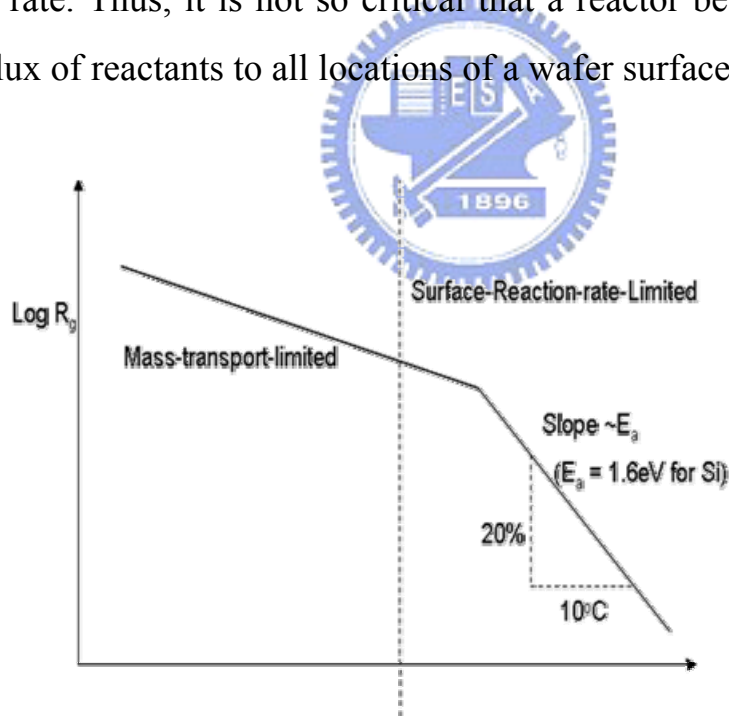
Figure 2.11   The deposition rate R_g is a rapid varying function of temp.(T) in the surface-reaction-limited regime of operation, whereas it changes only slowly with temperature in the mass-transport-limited regime (high temperature).

In deposition processes that are mass-transport-limited, the temperature control is not so critical. The mass transport process, which limits the growth rate, is only weakly dependent on the temperature [24]. On the other hand, it is very important that the same concentration of reactants be presented in the bulk gas regions adjacent to all locations of a wafer, because the arrival rates of the reactants are directly proportional to the concentration gradient in the bulk gas. Thus to ensure that films are uniform across a wafer, reactors operated in the mass-transport-limited regime must be designed so that all the locations of the wafer surface and all the wafers in a run are supplied with an equal flux of reactant species.

2.3.6 Plasma fundamental

Plasma processes are widely used in the semiconductor industry for etch, CVD, PVD, and photo-resist strip. Plasma is a quasi-neutral gas of charged and neutral particles which exhibits collective behavior.

2.3.6.1 Physical characteristics of plasma

Any body of gas typically contains three species: neutral atoms or molecules, ions and electrons. Their relative concentrations (for example, the degree of ionization) are considerably different in plasma. The concentration of ions in the atmosphere is negligibly small. In typical glow discharge plasma used in CVD processes, ionic concentrations are of the order of 10^{10} per cm^3. The electron concentration is the same as the ion concentration, so the overall plasma is electrically neutral.

From fundamental kinetic theory, the kinetic energy of a particle is given by

$$\varepsilon \;=\; \tfrac{1}{2}mv^2$$

An understanding of the interactions between the three types of species and the energetic involved in these processes is essential for us to make use of plasmas in producing thin films. Energy transfer into plasma and between the species, diffusion phenomena within the plasma and chemical reactions in the presence of charge species are some of the processes that depend on collisions between the three species.
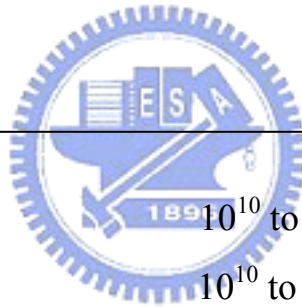
Electron concentration	10^{10} to 10^{11} per cm^3
Ion concentration	10^{10} to 10^{11} per cm^3
Electron temperature	3-5eV
Ion temperature	0.05eV
Electron velocity	10^7 cm /s
Ion velocity	10^4 cm /s

Table 2.1   Properties of a typical glow discharge.

2.3.6.2 Plasma chemistry

In a field-free space, charged particles behave the same way as neutrals, and their behavior can be treated similarly using the kinetic theory of gases

[25]. Collisions between particles can be written in terns of a mean free path λ given by

$$\lambda = 1 / \sqrt{2}\, n\sigma$$

n is the number density of the particles and σ is the collision cross section.

There are many kinds of inelastic collisions happening simultaneously in plasma. Three of them are the most important in CVD process, ionization, excitation-relation and dissociation.

Ionization in the plasma can occur through many mechanisms; the simplest is electron capture. For neutral species having high electron affinity, the following reaction occurs readily:

$$F + e^- \rightarrow F^-$$
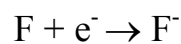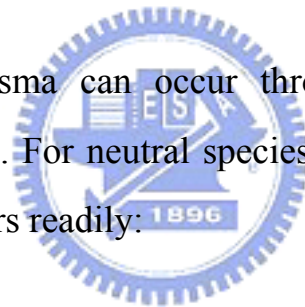
Electron capture contributes significantly to electron loss in halogen-containing plasma. An important mechanism for the maintenance of a glow discharge is the production of ions through electron impact. For instance, collision between an energetic electron and a xenon atom produces a xenon ion and another electron.

$$Xe + e^- \rightarrow Xe^+ + 2\, e^-$$
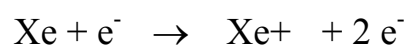
The two electrons are now accelerated by the potential gradient in a sheath to ionize more neutral, starting a chain reaction. The electrons have to posses a higher energy than the ionization potential of the neutral (~12eV for xenon) for this process to occur.

Excitation-Relaxation is an extreme case of the various excited states that an atom or a molecule can reach on electron impact, similar to ionization. There are electron energy thresholds equal to the energy of the first excited state, and they need to be exceeded for the excitation to occur.

$$e^- + A \quad \rightarrow \quad A^* + e^-$$

$$A^* \quad \rightarrow A + h\nu$$
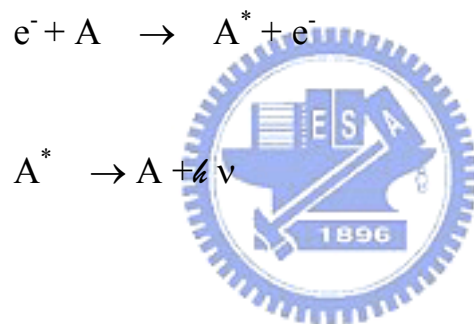
where h is plank constant, and ν is the frequency of the glow light. Different atoms or molecules have different frequencies, that which is why different gases have different glow colors. Oxygen glow is grayish blue, nitrogen glow is pink, and fluorine glow is red, etc.

When a molecule dissociates upon electron impact either its constituent atoms or further ionized products. Of more relevance to CVD is the formation of radicals in the plasma [26]. When an electron collides with a molecule, it can break the chemical bond and generate free radicals which are molecular fragments with unpaired electrons:

$$e^- \ + \ AB \ \rightarrow \ A \ + \ B \ + \ e^-$$
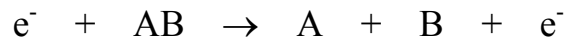
For example, in the Silane oxide process:

$$e^- \ + \ SiH_4 \ \rightarrow \ SiH_3 \ + \ H \ + e^-$$

$$e^- \ + \ N_2O \ \rightarrow \ N_2 \ + \ O \ + \ e$$
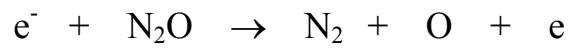
Collision	Byproducts	Energy of Formation
$e^- + SiH_4$	$SiH_2 + H_2 + e^-$	2.2eV
	$SiH_3 + H + e-$	4.0eV
	$Si + 2H_2 + e-$	4.2eV
	$SiH + H_2 + H + e-$	5.7eV
	$SiH^* + 2H + e-$	8.9eV
	$Si^* + 2H_2 + 2e-$	9.5eV
	$SiH_2^+ + H_2 + 2e-$	11.9eV
	$SiH_3^+ + H + 2e-$	12.32eV
	$Si^+ + 2H_2 + 2e-$	13.6eV
	$SiH+ + H_2 + H + 2e-$	15.3eV

Table 2.2   Possible collision processes in Silane Plasma.

2.3.6.3 Plasma parameters

There are some plasma parameters like thermal velocity, mean free path and Boltzman distribution [27].

Electron thermal velocity can be expressed as

$$u = (k\ T\ /\ m)^{1/2}$$

while k=1.38 x 10^{-23} ，T is temperature and m is the particle mass. For plasma in CVD chamber, ，$T_e \cong 2eV$，thus $V_e \cong 5.93\ x10^7$ cm/sec = 1.33x 10^7 mph. For Argon ion (Ar^+), $T_{Ar} \cong 0.05eV$, the thermal velocity is as:

$$V_i=3.46x10^4 \text{ cm/sec} = 774 \text{ mph}$$

In plasma, both electron and ion energy follow the Boltzman distribution. the average electron energy is about 2eV to 3eV, while ion energy in the bulk plasma is mainly determined by the chamber temperature , ~ 200℃ to 400℃, or 0.03eV to 0.05eV.
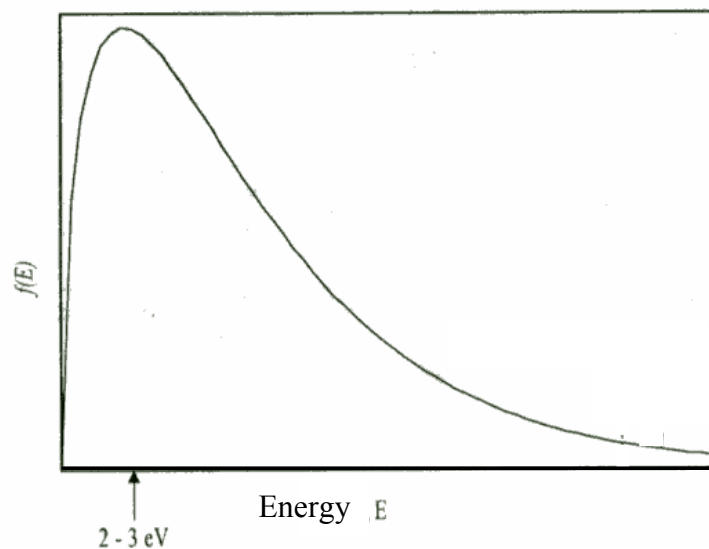
Figure 2.12　Boltzmann distribution.

2.3.6.4 Ion Bombardment

Since electrons move much faster than ions, the electrodes will be charged negative as soon as the plasma is initiated [28]. The negatively charged electrodes will repel negatively charged electrons and attract positive ions, therefore, in the vicinity of the electrodes. There are lesser electrons than ions.

The different between the negative and positive charge causes an electric field, called sheath potential, in that region. The light emission from that region is less intense than the bulk plasma due to fewer electrons and fewer electron collisions, thus a dark space can be observed near the electrodes.
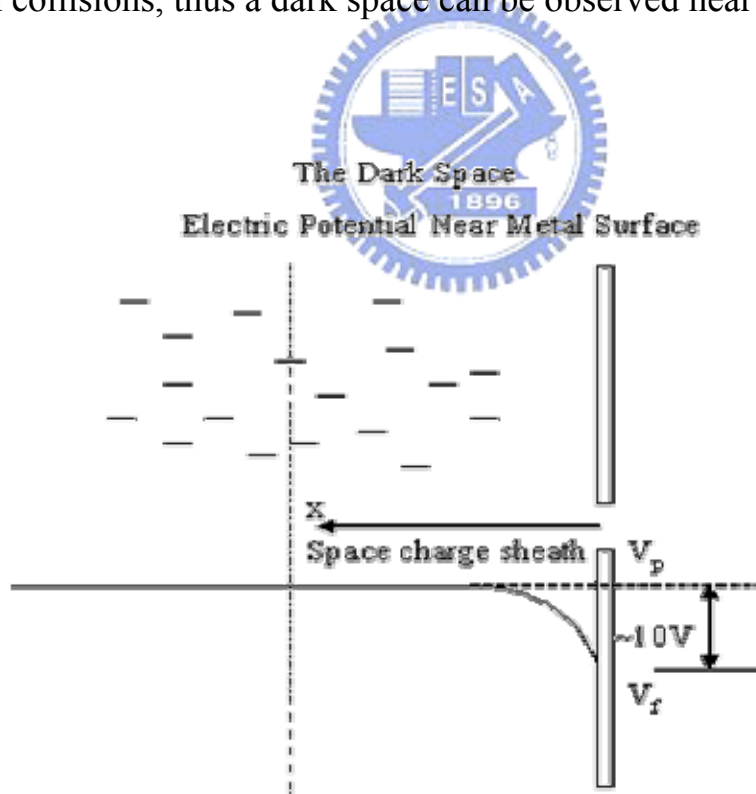
Figure 2.13   The sheath potential accelerates ions towards the electrode where the wafers sits and causes ion bombardment.

In an RF system, the potential on the RF hot electrode changes rapidly. The plasma potential also changes very quickly, because the electron moves fast and anything close to plasma charges negatively, plasma always has a higher potential than anything in contact with it. Therefore, in time average, there is a DC potential difference between the bulk plasma and the electrode. The energy of ion bombardment is determined by the DC bias, which is about 10 to 20 volts in CVD chambers.
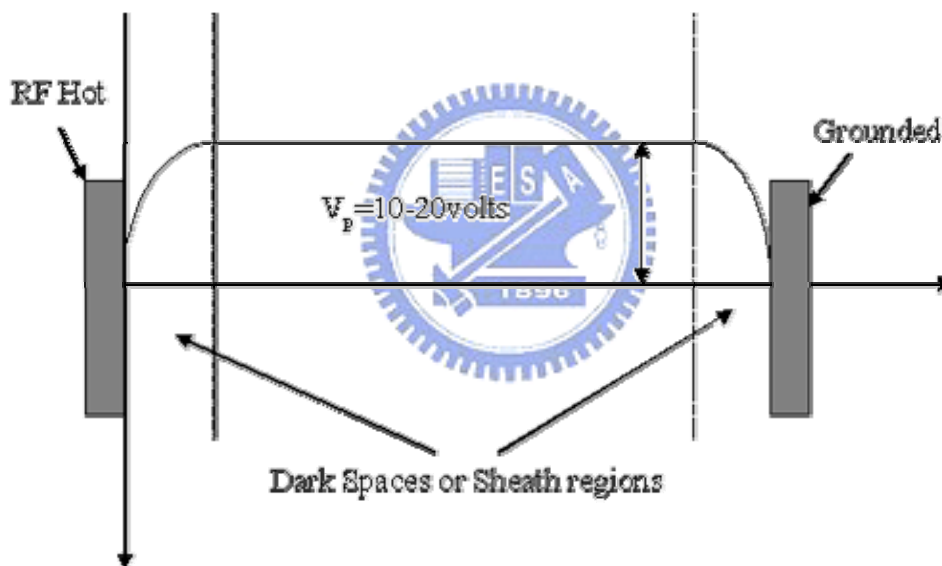
Figure 2.14   DC potential difference between the bulk plasma and
the electrode .

Plasma potential depends on RF power, pressure, and spacing between the electrodes, since RF power also affects the plasma density, the capacitance (parallel plate) coupled plasma sources can not independently change ion energy and ion flux [29].

Ions are much heavier than electrons, thus the ions move much more slowly in the RF plasma and have much less energy than the electrons, thus, at 13.56MHz the RF field coupled energy exclusively into the electrons and leaves the ions cold.

2.4 Chemical vapor deposition systems

CVD reactors are divided into two primary types: atmospheric pressure and low pressure CVD. There are a number of atmospheric pressure CVD and Sub-atmospheric pressure CVD. Most advanced device films are deposited in systems where the pressure has been lowered. These are called low pressure CVD or LPCVD.

CVD systems ate operated with two principal energy sources: thermal process and plasma process. Thermal sources are tube furnace, hot plates, and RF induction. Plasma enhanced chemical vapor deposition (PECVD) and high density plasma CVD in combination with lower pressure offers the unique advantage of lowered temperatures and good film composition and coverage.

2.4.1 Atmospheric pressure CVD systems

As the name implies, atmospheric CVD systems reactions and deposition take place at atmospheric pressure. There is an another thermal process CVD is called Sub-atmospheric pressure chemical vapor deposition (SAPCVD) which process range is from several torr to 600torr .
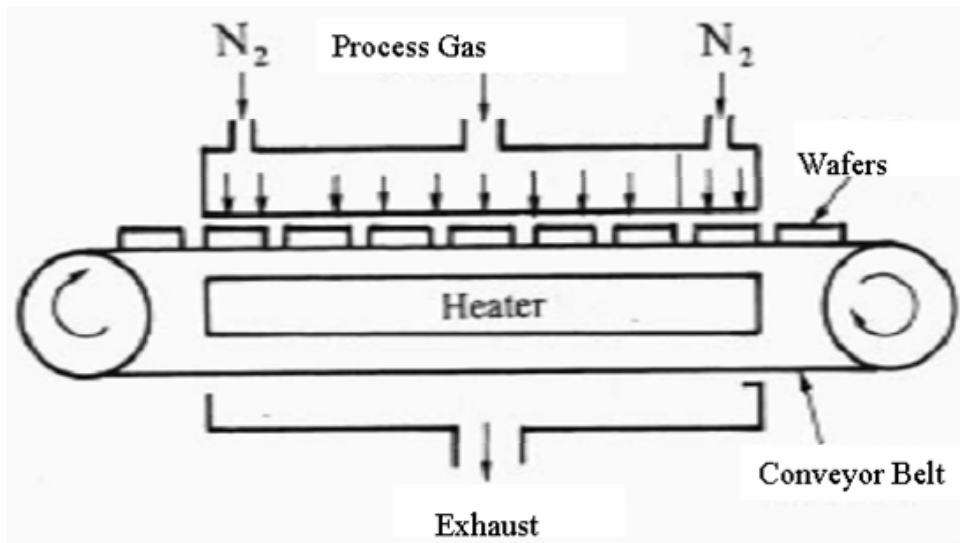
Figure 2.15　Schematic diagram of the APCVD.

2.4.1.1 Sub-atmospheric CVD (SAPCVD)

Atmospheric pressure CVD (APCVD) reactors were the first to be in the microelectronics industry. Operation at atmospheric pressures keeps reactor design simple and allow high film deposition rate. APCVD **[30] [31]**, however, is susceptible to gas-phase reactions, and the film typically exhibit poor step coverage. Since APCVD is generally conducted in the mass-transport- limited regime, the reactant flux to all parts of average substrate in the reactor must be precisely controlled.

Wafers are transported to three deposition areas in sequence by a load belt and conveyed out of the hot area by the unload belt. The belt is continuously cleaned of the SiO_2 deposited on its surface in a belt cleaner. Central to the deposition is the delivery of the reactant gases. This is accomplished by a

unique injector design. Oxidizers and hydrides, which react to form the film, are kept separate till the gases exit the injector onto the surface of the wafers.

The injector creates a chemical vapor curtain under which the wafers are transported by the belt. The curtain contains a tri-linear flow of oxygen in Nitrogen (N_2), and hydride in N_2. Deposition occurs in a small zone where the residence time of the reactants is minimized by the high gas flow volumes. The wafer is heated through a resistive heater block situated beneath the reaction surface.

APCVD benefits on high throughput, good uniformity, and the capability to process large -diameter wafers. However, they have the problems of high gas consumption and frequent need of reactor cleaning.
Films are produced by the following general reactions:

$$SiH_4 + 2O_2 \quad \rightarrow \quad SiO_2 + 2H_2O$$
$$2PH_3 + 4O_2 \quad \rightarrow \quad P_2O_5 + 3H_2O$$

and

$$B_2H_6 + 3O_2 \quad \rightarrow \quad B_2O_3 + 3H_2O$$
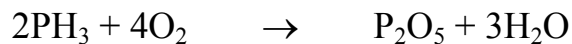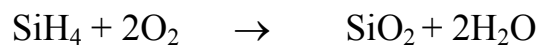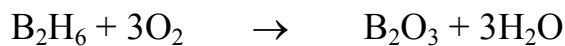
2.4.2 Sub-atmospheric chemical vapor deposition

2.4.2.1 SACVD Introduction

Recently, Sub-atmospheric pressure CVD is very common systems in 300mm manufacturing for dielectric bulk film deposition and gap filling process by using TEOS and ozone (O_3). This CVD technology enables the formation of oxide films with high conformality and low viscosity under low deposition temperatures. The step angle depends on the ozone concentration,

Borophosphosilicate glass (BPSG) [32] [33] has been widely used as a pre-metal dielectric in advanced very large scale integrated (VLSI) device fabrication. As device dimensions keep shrinking, BPSG has the advantages of filling high aspect ratio gaps and at the same time, achieving global planarization over the device surface due to its reflow capability at elevated temperature (> 800℃), without overstretching the thermal budget as compared to phosphosilicate glass (PSG) films. Using current chemical vapor deposition (CVD) technology, BPSG films can be deposited either by SILANE or O_3-TEOS (tetraethylorthosilicate) based BPSG processes, with TEOS/O_3 BPSG film shown much better step coverage than SILANE BPSG film. Among all the technologies, sub-atmospheric (SACVD) BPSG using triethylphosphate (TEPO) and triethylborate (TEB) as dopant sources have been studied extensively to yield superior film quality and improved reflowed capability [34]. However, due to the process complexity, very little is known about the reaction mechanism for TEOS/O_3 BPSG, even though some modeling has been done for the un-doped silicon glass (USG) using TEOS/O_3 chemistry. Comparing the two processes, BPSG has been proven to have enhanced deposition rate with no surface sensitivity. However, BPSG films

have worse step coverage as deposited, including changes in the reaction mechanism by the addition of doped precursors into the reaction chamber.

In addition, for the TEOS based processes, a certain type of carrier gas, for instant, helium or nitrogen, is utilized to deliver vaporized TEOS and liquid doped sources to the process chamber to reduce gas-phase nucleation for particle control. Due to their distinct physical properties, such as heat capacity and thermal and mass diffusivities, different carrier gases may result in different film characteristics.

The schematic shown in figure 2.16 is the SACVD chamber, which is described in detail elsewhere. Briefly, this is a single wafer process tool equipped with the precision-liquid-injection system (PLIS TM) for accurate and repeatable TEOS, TEB, and TEPO delivery. Liquid TEOS and dopants are vaporized and carried into the process chamber using a carrier gas (He or N_2) [35], then mixed with ozone (O_3) at the top of the reactor. Both liquid injection valves and liquid delivery lines are heated to prevent liquid condensation. after flow redistribution through the block and faceplate with optimized hole sizes and density, the gas mixture impinges onto the wafer, which is on a hot surface called heater (400℃ to 550℃), to form BPSG film. The heater temperature is controlled by heating module and the variation temperature is within less than 5℃. During deposition, the gas-phase temperature is controlled by both the heater as well as the chamber wall, which is maintaining at a constant temperature, to reduce gas nucleation. An in situ plasma chamber cleaning process was performed after each wafer deposition to ensure BPSG process repeatability and particle control over thousands of wafers. The controlling

variables for BPSG deposition include liquid flow of (TEOS, TEB, and TEPO), carrier gas type (N_2 or He) and flow, heater temperature (T), and spacing (Sp), as well as chamber pressure (Pr).
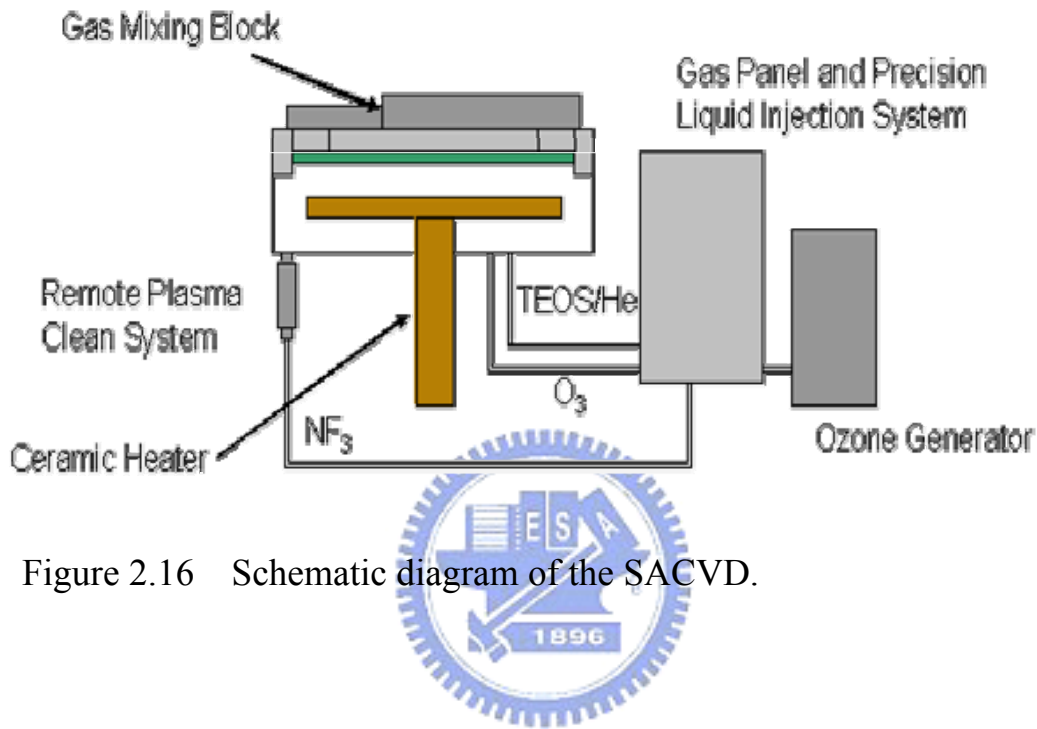
Figure 2.16   Schematic diagram of the SACVD.

2.4.2.3 Introduction to SACVD process

All film properties were evaluated on 300mm p-type silicon substrates. The film thickness and uniformity were monitoring by KLA Tencor and the doped concentrations were measure using both XRF(X-ray fluorescene spectroscopy) and FTIR, calibrated by inductively coupled plasma atomic emission spectroscopy (ICP-AES) for B_2O_3 and P_2O_5 weight percent (w/o).For gap fill evaluation, all the BPSG films were deposited at 5.0B w/o X 5.0 P w/o, and annealed at 800℃ in N2 ambient for 30 minutes.

For SACVD, reaction temperature are generally at 480℃. Earlier application of the TEOS reaction were in the formation of

borophosphosilicate glass (BPSG) films, with proper doped additives, this reaction is still one of the most popular sub- atmospheric pressure BPSG reaction **[36] [37]**.

Doping of the SiO_2 network by network modifiers and other glass-forming oxides serves the following purpose: (a) Dopant additives tend to lower the melting point of the glass, (b) they alter the viscosity of the glass at high temperatures, and (c) below certain concentrations they introduce the properties if the glass former without phase segregations from the SiO_2 matrix. For instance, boron oxides provide high temperature stability to the glass, whereas phosphorus oxides make the glass hygroscopic. Dopants also alter the glass transition temperature, for instance, ordinary window glass has sodium-based network properties, while the oven-to-table commercial glasses contain glass former such as B_2O_3.

The common additives to SiO_2 for semiconductor applications are boron and phosphorus oxides for poly-metal dielectrics, and arsenic for doping applications. Boron and phosphorus additions tend to lower the melting temperature, reduce the intrinsic stress in the glass, allow for better glass flow due to reduce viscosity, and phosphorus additions getter sodium ions. Phosphorus doped-glass (PSG) finds application as a passivation film to protect the device against sodium. Boron-doped glass (BSG) is used as a boron doped source.

Borophosphosilicate glass (BPSG) deposited by the Sub-Atmospheric CVD (SACVD) has been investigated for both gap-fill the Inter-layer Dielectric (ILD) trenches before etch back and the structural layer deposition

of the dopant activation to enable the fabrication process for the 90nm DT DRAM [38]. The result obtained suggest that the timing of incorporation of the Phosphorous dopant to the gas phase chemistry of the silicate glass plays an important roles in the reflow mobility and the nitric film consumption. The TEPO introduction should come later and gradually than the forming Borosilicate glass mixture (BSG).

It is important for BPSG applications in the semiconductor industry as an inter-metallic dielectric between the aluminum and the poly-silicon. BPSG deposition in SACVD is based on the pyroligneous decomposition of tetraethylorthosilicate (TEOS), triethylborate (TEB) and, triethylphosphate (TEPO) in an oxidizing atmosphere. The incorporation of Boron and Phosphorous in the BPSG effects the ability of the glass to reflow at temperature ranges compatible with the reduced thermal budget criteria employed in today's chip devices. The presence of Phosphorous enhances the ability of the glass to getter and trap alkali metal impurities thus, prevent the migration of these deleterious species into the active regions.

In advance ULSI processes, reduction of junction depths caused more restrictive thermal budgets and limit the time and temperature available for the flow anneal process [39]. PSG reflow at 1000-1100°C could result in excessive diffusion of shallow junction. Furthermore, impurity implanted MOS gate oxides cannot be exposed to high temperature (>900°C). However, to easing film coverage over the substrate topography, a flowing glass is still desirable prior to metal deposition. The glass flow temperature as low as 700 °C can be obtained by adding the boron dopant to the PSG gas flow mixture.

A ternary (three component) oxide system is formed; B_2O_3-P_2O_5-SiO_2. The boron (B) concentration is more dominant in determining the flow characteristics than the phosphorous (P) concentration.

The reflow ability of the glass to provide void free or seam free is critical for providing proper metal contact step coverage [40]. With the scaling down of device feature sizes, the manufacturing challenge presented by submicron devices is the ability to completely fill a narrow trench in a void-free manner. As the trench gets narrower and the aspect ratio (the ratio of the trench height to the trench width) increases, it becomes more likely that the opening of the trench will "pinch off." Pinching off a trench traps a void within the trench. Under certain conditions, the void will be filled during the reflow process; however, as the trench becomes narrower, it becomes more likely that the void will not be filled during the reflow process. Such voids are undesirable as they can reduce the yield of good chips per wafer and the reliability of the devices. Therefore, it is desirable to be able to fill narrow gaps with BPSG in a void-free manner. The difficulty to fill the gaps is observed when conducting in this study, the reduction in interconnect pitches of the 90nm devices and high aspect ratio of the trenches between interconnect lines.

USG process

$$O_3 \xrightarrow{\text{heat}} O_2 + O$$

$$O + Si(OC_2H_5)_4 \xrightarrow{\text{heat}} USG + \text{volatile organics}$$

PSG process

$$O + TEOS + TEPO \xrightarrow{\text{heat}} PSG + \text{volatile organics}$$

BPSG process
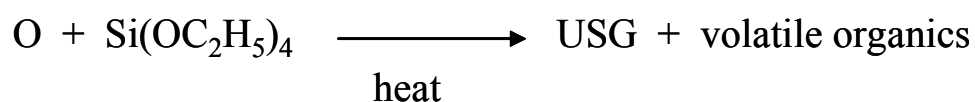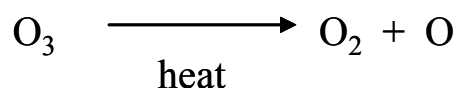
$$O + TEOS + TEPO + TEB \xrightarrow{\text{heat}} BPSG + \text{volatile organics}$$
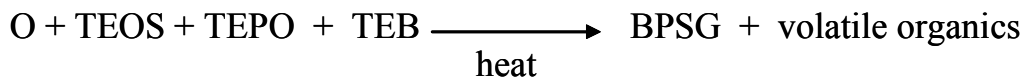
For SA BPSG film gap-fill, a significant improvement of PMD gap-fill has been achieved with changes in a main silicon precursor from TEOS to the mixture of TEOS and fluorinated TEOS, F-BPSG processes met the chosen target gap-fill parameters for "vertical" structure types defined as G_v<0.05 μm and AR_v>2, as can be seen in figure 2.17 as well as tapered structure types. It is known that fluorine contained compounds, being added to the gas-phase during chemical vapor deposition or plasma-enhanced deposition, improves film step coverage. Fluorinated SABPSG films hence provide much better gap-fill after rapid thermal anneal at 850°C for 30 seconds. This means that from a gap-fill point of view, this approach can be considered as an option for PMD with small device gaps at least at studied structure requirements if other approaches of structure tapering can not be used.
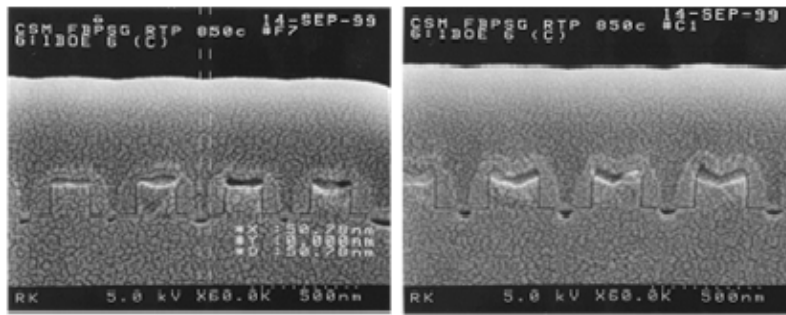
Figure 2.17   Vertical (left) and tapered (right) structure types show

gap fill with BPSG with RTP of 850°C for 30seconds.
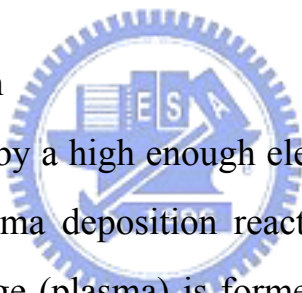
FTIR spectra of samples recorded immediately after film deposition did not reveal any moisture peaks in the area around 3000 cm^{-1} for both studied 4.5B-4P and 5.5B-4.5P dopant concentrations. The refractive index values have been found to be slightly higher for SA F-BPSG films. RTA of SA F-BPSG films at 850°C for 30secondss was found to decrease refractive index values, increase shrinkage values to twice that of SABPSG films, and increase surface charge values from about 5.8×E10 q/cm^2 to 6.5×E10 q/cm^2. After prolonged storage in clean-room conditions followed by RTA anneal, changes in the properties of SA -FBPSG films have been found to be more pronounced indicating that SA -FBPSG film properties need to be investigated in detail.

Gap-fill capability of SAPSG and SABPSG films deposited using 1-step and 2-step deposition processes at 480°C and 550°C and annealed at low thermal budget conditions in a dry gas ambient have been studied for film application as a void-free pre metal dielectric for 0.18 μm device technology and beyond **[41]**. Gap-fill capability was found to be strongly effected by using different structure types. "Tapered" structures with gaps 0.03 um and aspect ratios up to 6 have been successfully filled with all studied film options using

rapid thermal anneal at temperatures as low as 800-850°C for 30seconds in nitrogen ambient. Difficulties with film gap-fill capability have been found to arise with the use of "vertical", "partly vertical" and especially, with "re-entrant" structures. Films of fluorinated borophosphosilicate glass deposited at sub-atmospheric pressure conditions (SA F-BPSG) have been found to be able to improve gap-fill for "vertical" structures significantly at the same low thermal budget anneal condition.

2.4.3 Plasma enhanced chemical vapor deposition PECVD

2.4.3.1 PECVD introduction

When a gas is excited by a high enough electric field, for example, in the reaction chamber of a plasma deposition reactor such as the one shown in figure 2.18, a glow discharge (plasma) is formed. In the plasma, high energy electrons exist that can impart enough energy to reaction gases for reaction that normally take place only at high temperature to proceed near room temperature. The reactor looks superficially like the sputtering equipment, but there are some substantial differences. In plasma-enhanced CVD (PECVD) [42] [43], the inlet gas contains the reactants for deposition, and the anode instead of being sputtered away remains unaffected. The voltage applied to sputtering electrodes may be either RF or DC, depending on the specific mode of operation, but plasma deposition requires RF voltage.

The glowing (plasma) region will contain, in addition to the free electrons, normal neutral gas molecules, gas molecules that have become ionized,

ionized fragment of broken-up gas molecules, and free radicals. Deposition occurs when the molecules of incoming gases are broken-up in the plasma and then the appropriate ions are recombined at the surface to give the desired film.

Plasma enhanced CVD chambers can use Silane to deposit silicon oxide, nitride, and oxy-nitride, they also can use TEOS to deposit doped and un-doped oxide **[44] [45]**.
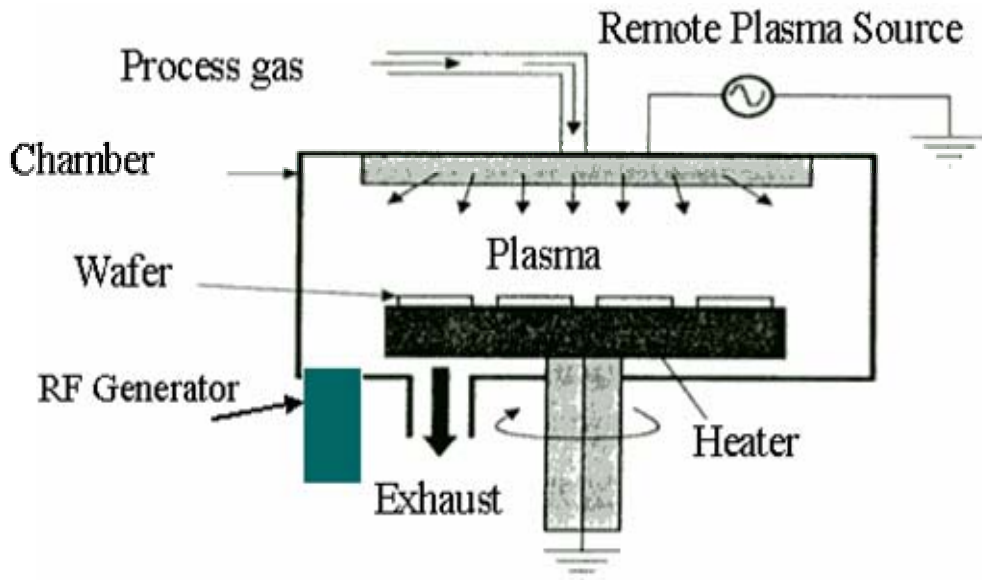
Figure 2.18   Schematic diagram of PECVD.

2.4.3.2 PECVD process introduction

The surface of both oxide and silicon exposed to the ambient are covered by hydrogen. Thus, the crystal lattice at the surface does not terminate with silicon and oxygen and dangling bond, but with OH in the case of oxide and SiH_4 in the case of silicon.

Thermal energy at 400℃ does not cause the chemisorbed precursors to leave the surface. However, in PECVD processes, ion bombardment has enough energy (10 to 20eV) to remove some chemisorbed precursors off the surface.

Silane is a molecule with a tetrahedron structure: A silicon atoms in the center and four hydrogen atoms, because there is a chemical bond, the chemisorbed molecules have very low surface mobility.
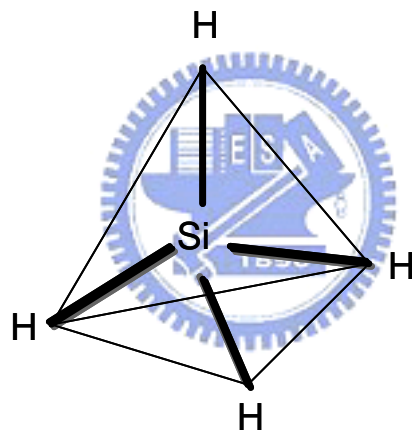
Figure 2.19   SILANE bonding.

Silane is pyrophobia, explosive, and toxic gas that which is widely used in the semiconductor industry as a silicon source to deposit silicon oxide or silicon nitride.

In the case of silane, the parent molecule will neither chemisorb nor physisorb to the oxide surface. The parent molecule is too symmetrical to react with the surface (i.e. chemisrb) and the hydrogen atoms are not capable of

hydrogen bonding to the surface (physisorption). However, the molecular fragments formed by pyrolysis or plasma dissociation, SiH_3, SiH_2, or SiH, are chemical radials that readily chemisorb on the oxide surface **[46]**.

SILANE USG reaction formula

$$SiH_4 + N_2O \xrightarrow{plasma/heat} SiO_x + N_2 + H_2 + H_2O + \text{other volatiles}$$

PSG reaction formula

$$SiH_4 + N_2O \xrightarrow{plasma/heat} SiO_2(P_2O_5)_xH_y \text{ other volatiles}$$
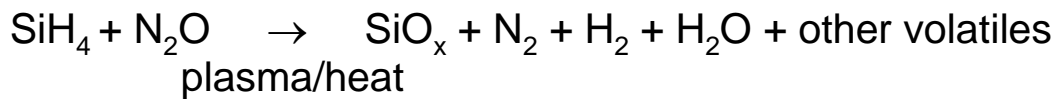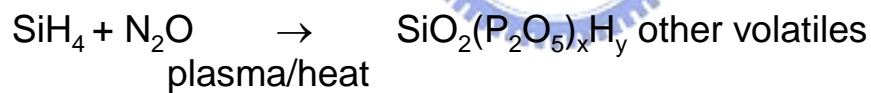
Nitride , UV nitride and high temperature (HT) nitride.

$$SiH_4 + N_2 + NH_3 \xrightarrow{RF \& heat} SiN_xH_y + \text{other volatiles}$$
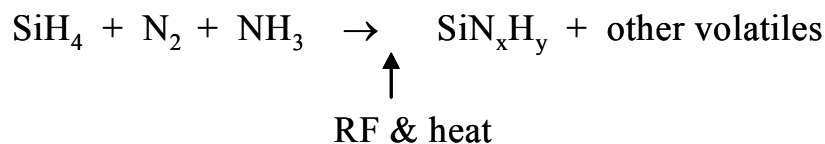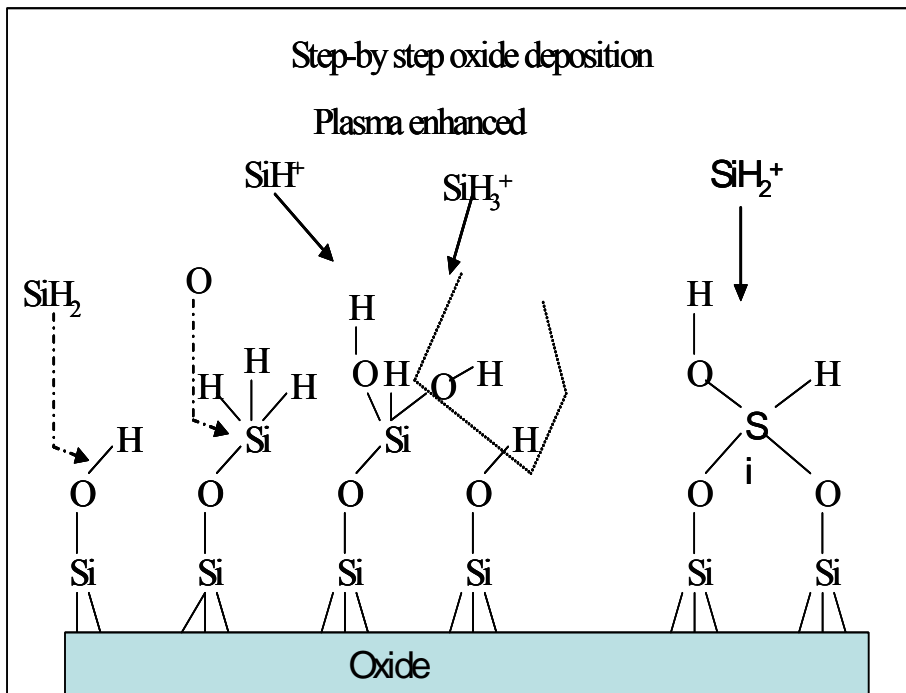
Figure 2.20   Silane mchanism of plasma CVD.

TEOS process

$$O_2 \; + \; Si(OC_2H_5)_4 \; \xrightarrow[\text{RF \& Heat}]{} \; USG \; + \; \text{volatile organics}$$

PSG process
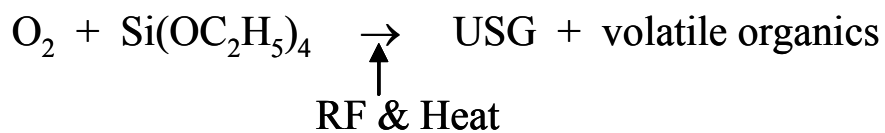
$$O_2 \; + \; TEOS \; + \; TMP \; \xrightarrow[\text{plasma \& heat}]{} \; PSG \; + \; \text{volatile organics}$$
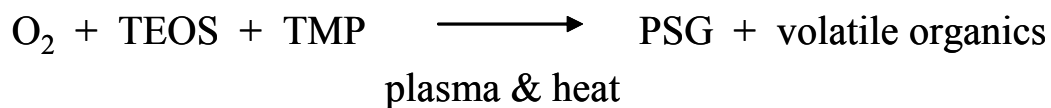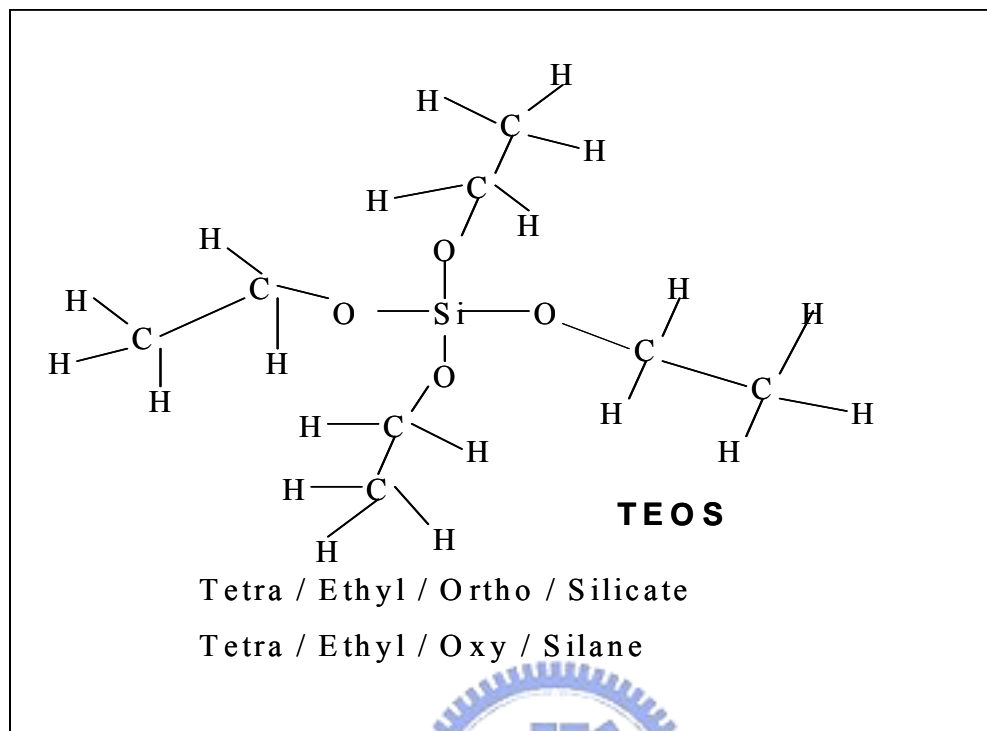
Figure 2.21   Physisorption on the oxide surface through hydrogen
            bonding.

In physisorbed, the adsorbed molecules are held to the surface with forces much weaker than for chemisorption. Physisorption involves energies usually leass than 0.5eV per molecule. the physisorbed molecules can move on the surface, so they have more surface mobility than chemisorbed molecules.

The oxygen atoms in the TEOS molecule each have two electron pairs and can act as the electronegative, proton acceptor atom necessary for formation of hydrogen bonding. Thus, the parent TEOS molecules readily physisorb on the oxide surface through hydrogn bonding.

2.4.3.2 Surface mobility

The surface mobility can strongly affect the step coverage and conformality of the deposited film. Higher surface mobility is usually associated with better step coverage and conformality. In silane process. SiH_4 disassociates to SiH_3, SiH_2, and SiH, sometimes just called SiHx. SiHx is chemisorbed on the surface and therefore has very low surface mobility, thus the step coverage for silane process is not very good.

TEOS can be physisorbed on the surface, therefore, the TEOS process has better step coverage and conformality that that of the silane.
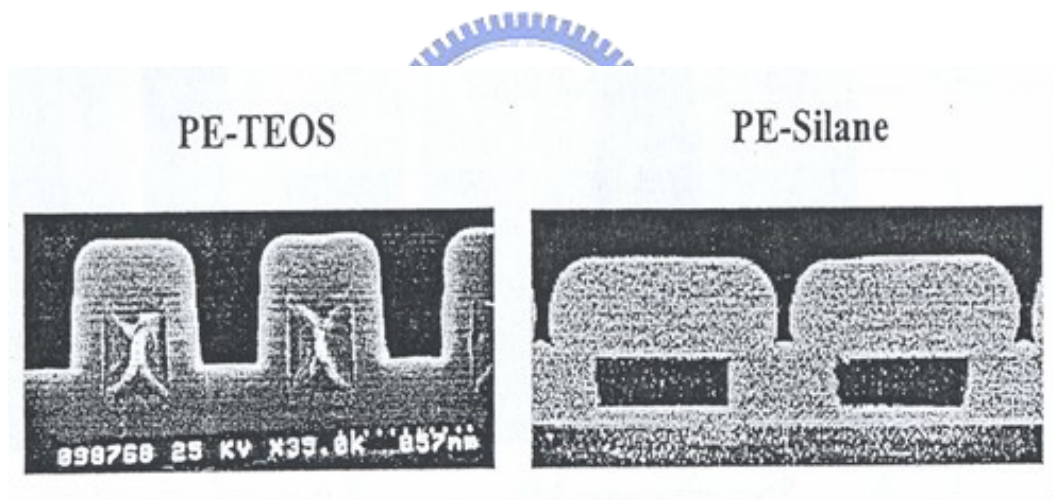
Figure 2.22   Step coverage and conformality of TEOS and silane USG.

In the PE-TEOS process, some TEOS molecules are dissociated in plasma. The dissociated TEOS molecular pieces are more likely to be chemisorbed than physisorbed [47]. That is at least part of the reason that the ozone-TEOS process, which does not use plasma, has better step coverage and conformality than the PE-TEOS process.
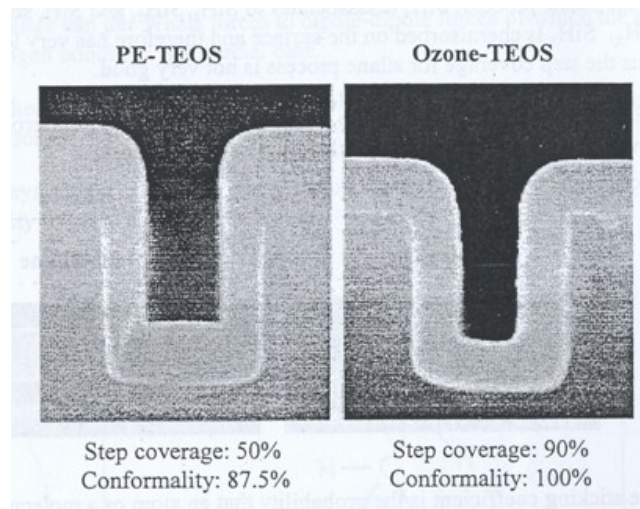
Figure 2.23   Step coverage and conformality of TEOS and silane USG

in trench.

2.4.4 High density plasma (HDP) processes

2.4.4.1 Introduction

A technique combines PECVD deposition with bias sputtering to obtain very good filling of narrow gaps. It is used primary for silicon oxide depositions. The high density plasma can be generated by a variety of sources, including electron cyclotron resonance (ECR) and inductively coupled plasma (ICP). This high density plasma results in a densely CVD silicon dioxide film at low temperature and a very low chamber pressure in the 1-10mtorr range. In fact, there is usually no intentional heating in these CVD systems. The ion bombardment supplies enough energy to raise the substrate temperature and cooling of the wafers is often required to keep the temperature below 400℃.

The HDPCVD chamber has three RF power sources. Both of top power and side power mainly generate the plasma and control the density via

inductive coupling. The other is called bias RF, which mainly controls bias and bombarding ion energy.

Heavy ion bombardment generates a large amount of heat. Therefore, an HDPCVD chamber needs a helium backside cooling system, the wafer is prevented from blowing off the chuck by using electrostatic attraction in the so-called E-chuck. With a separate RF bias applied on the substrate in HDPCVD systems, the angular dependence of ions sputtering is exploited **[48]**. puttering –the knocking off of atoms from a solid by incident ions when the solid is electrically biased that which occurs preferentially on sloped surfaces rather than on vertical or horizontal surface. This simultaneous sputtering of the film during its deposition can results in planarized and void-free films. The strong directed ion component of the HDPCVD deposition process also helps in the filling of holes, and the ion bombardment helps make the film denser.
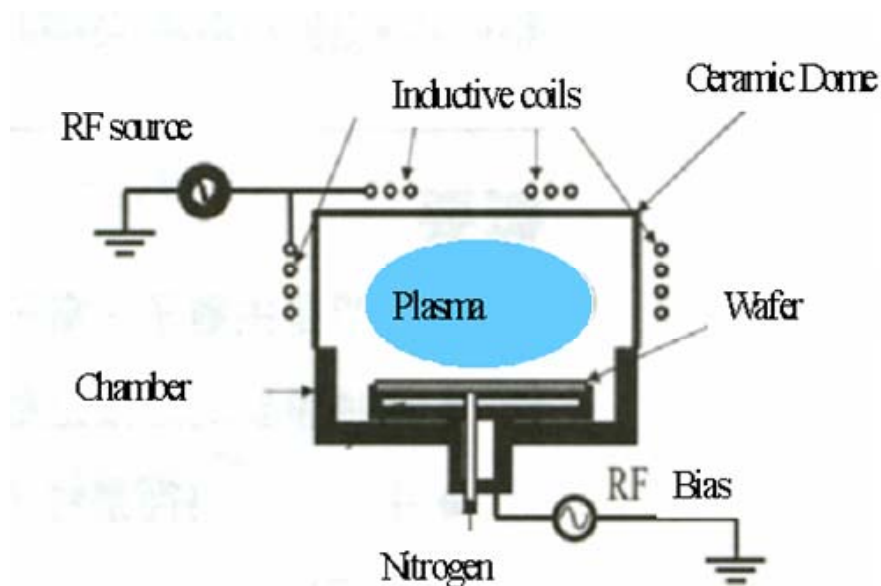
Figure 2.24   Schematic diagram of HDPCVD.

2.4.4.2 HDPCVD process

HDPCVD can display excellent filling and good planarizing film properties. It is widely be used for many gap fil layers like shallow trench isloation, gap filling of pre-metal deposition, inter-metal depsotion and final passivation deposition **[49]**. When the industry first encountered the gap fill issue, the first approach was to use deposition followed by etch back to open the gap, and complete the rest of the deposition. With more device shrinkage, repetitions of deposition and etch back were used. This has caused the cost and of processing a wafer to increase. To tackle this issue, a new concept of deposition technique has been developed which utilize the deposition and etch in the same reactor and called high density plasma chemical vapor deposition HDPCVD.
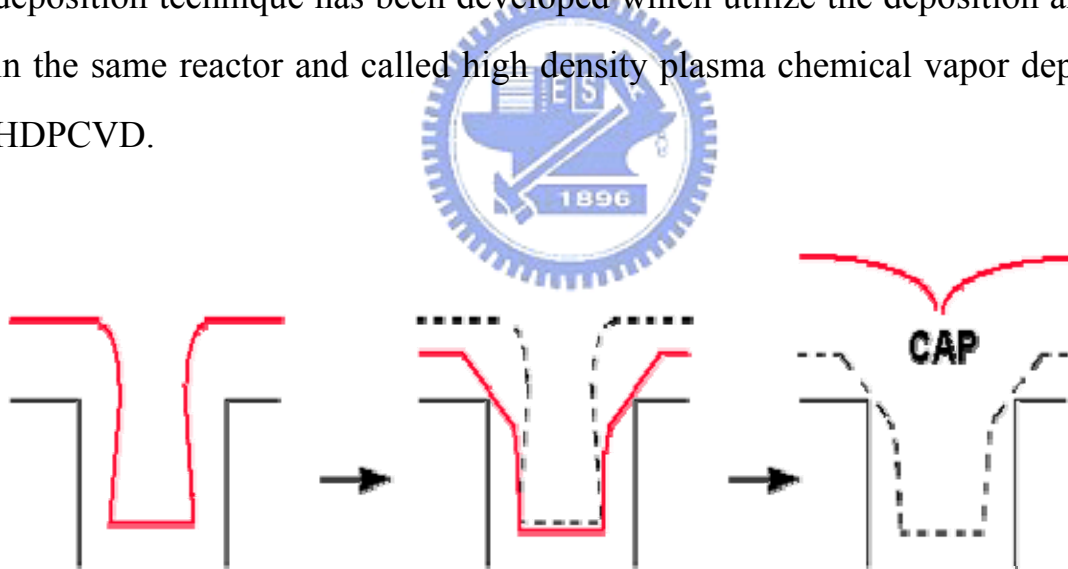
Figure 2.25   Schematic of deposition, etch and deposition process for gap
                fill.

The main components of HDP CVD are the deposition portion from the SiH_4 and O_2 chemistry and the etch portion from Ar and O_2 chemistry. The etch portion is the physically sputtering of the surface to open up the top of the trench.
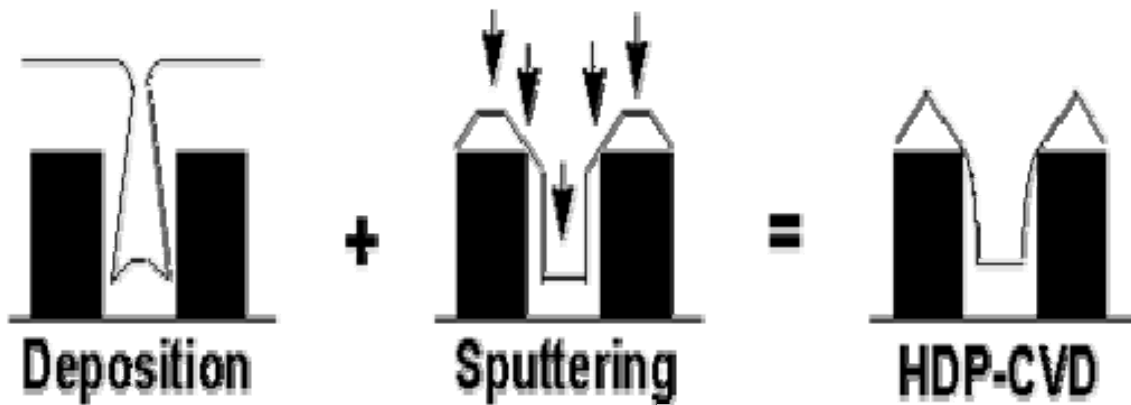
Figure 2.26   Main concept of HDP CVD is the combination of deposition
and sputter.

The processes running in HDPCVD chambers are

USG $SiH_4 + O_2 + Ar \longrightarrow$ USG   +   Volatiles

PSG $SiH_4 + PH_3 + O_2 + Ar \longrightarrow$ PSG   +   Volatiles

USG $SiH_4 + SiF_4 + O_2 + Ar \longrightarrow$ FSG   +   Volatiles

2.4.4.3 Sputtering

The key reason for the successful gap-fill of HDP CVD is the ion incident angle dependence on the sputter yield. As it is shown in figure 2.27, when the ion impacts on a solid, it transfers energy to the solid. The critical point is that the sputtering only occurs at the surface. Therefore, transferring the energy to a larger surface area will result in the higher sputter rate.

a) 0 degree

b) 45 degree

c) 90 degree
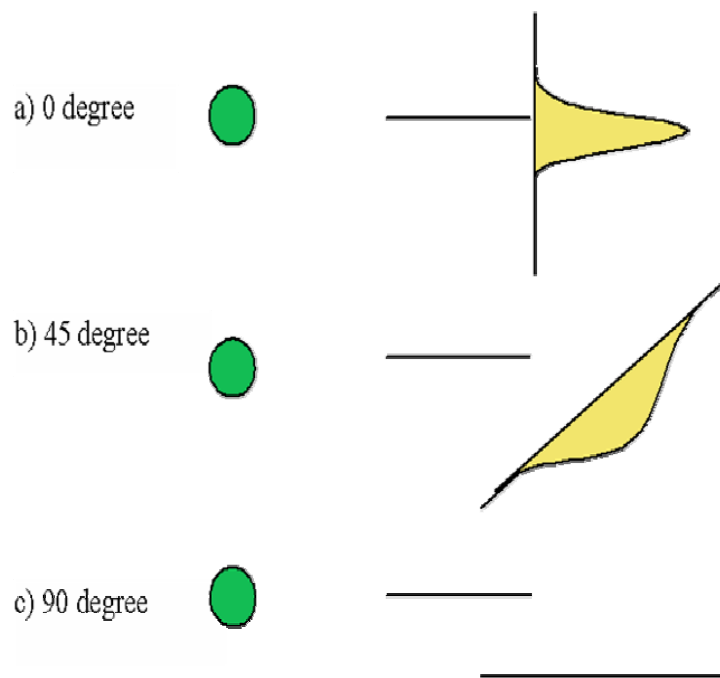
Figure 2.27   The relation between the incident angle and the transferred

energy distribution in bombarded material.

When an ion bombard on a solid, an ion can either bounce back (recoil) or travel through the solid and imbedded within the solid while it looses energy along the way by transferring the energy to nearby atoms in its path. The recoil usually takes place when an incident ion has high energy, ~ 1MeV. This effect is utilized for Rutherford Back Scattering (RBS) measurements, which can determine the thickness and the composition of a solid.

In HDP CVD, a typical ion energy, which are supplied by the bias RF, is around few hundreds eV. In this low energy region, most of the energy is transferred to solid and some of this energy will contribute to sputtering. When an ion bombard on a surface at a normal angle, figure 2.27a, it interacts with atoms in a small region of the surface. Since the sputtering takes place on the

surface layer, a small portion of the ion energy will contribute to sputtering and the rest of the energy will dissipate as a heat. On the other hand, if an ion impacts on the surface on a glancing angle, it may not have enough energy to penetrate the surface and just bounces off as shown in figure 2.28. In this case, almost no sputtering will take place. The most sputtering takes place if an incident ion can transfer most of its energy to the surface layer atoms as it is shown in figure 2.27b. A typical relationship between the incident angle and sputter yields is given in figure 2.28. The peak occurs usually between 45 degree to 70 degree depending on the incident ion energy and type. Because of this effect, sputter rate at the edge of the gap, the angled area, is higher than flat part, the bottom and top of the gap. This will keep the gap open during the deposition. The energy transfer to the surface is more effective when the ion incident on the surface at a slanting angle.
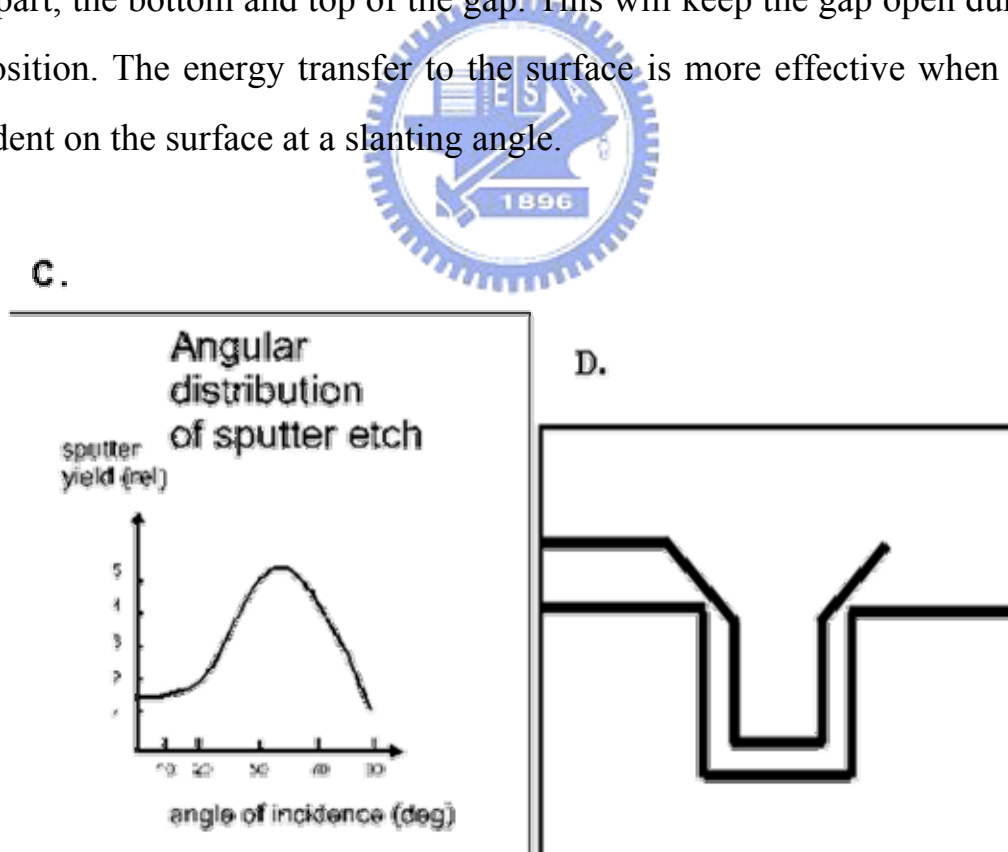
Figure 2.28   A relationship between angle of incidence and sputter
                        yield.

2.4.4.4 Deposition to sputter (DS) ratio

DS ratio is used as a reference to the HDP CVD deposited process, because the gap fill capability is depend on this factor. DS ratio is defined by

$$DS = GROSS\ DEPOSITION\ RATE/SPUTTER\ RATE$$
$$= (Net\ deposition\ rate + Sputter\ rate)/Sputter\ rate$$

Here, the gross deposition rate is the true deposition rate assuming there is no sputter component. The net deposition rate is the full HDP deposition under the simultaneous deposition and sputter. Note that DS is only a reference number. The way of measuring DS ratio is not perfectly accurate. When the sputter rate is measured, there is no SiH_4 chemistry. The sputter rate obtained without SiH_4 could be different from the actual sputter rate during the deposition. In any case, DS ratio provides good guideline of the HDP CVD process for gap fill and it is important to understand this concept. Also, in this industry other term called etch to deposition rate (ED ratio), which is the inversion of the DS ratio definition, is used. The measuring technique of the ED ratio is little different from the DS ratio. In general the inversion of the DS ratio is close to ED ratio, but not exactly the same.

In summary, the angle dependence of sputter yield is the mechanism for the triangular surface topology of HDP CVD. Also, due to this, HDP CVD has a bottom up gap fill mechanism that is different from other CVD deposition process where film grows from the side of the gap wall.
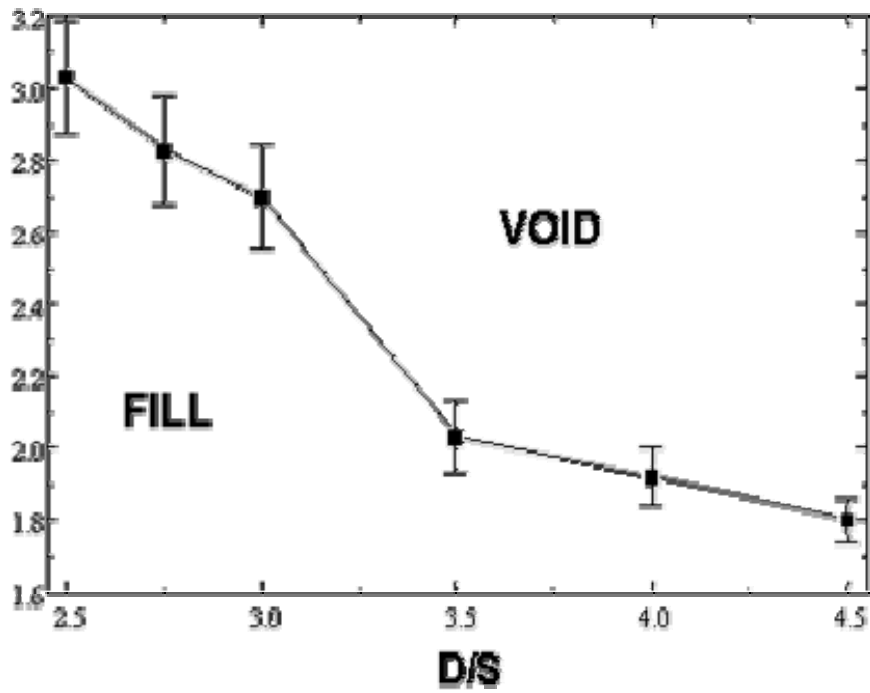
Figure 2.29   Relationship of sputtering rate against void capability.
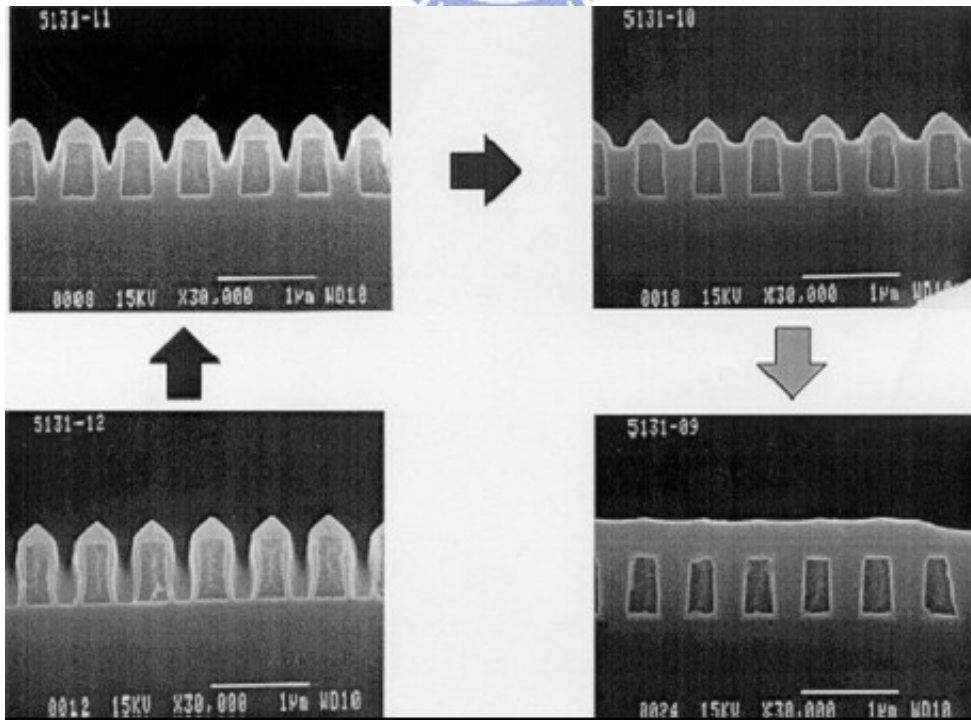
Figure 2.30   A illustration of gap fill evolution is HDP CVD.

2.5 Shallow trench isolation gap fill challenge

2.5.1 Introduction

The majority of manufacturers have used HDP-CVD for a variety of the reasons including the productivity, the thermal budget of annealing and CMP matching of film, while some customers have used O_3/TEOS technology for the STI oxide deposition. With the scaling down of devices and the stringent isolation requirements, shallow trench isolation gap filling is required beyond 100nm space with aspect ratio of 5-7:1. The HDP-CVD gap fill extension in 90nm-technology node requires definite model and its technique to show the route of void free in the next generation STI structures.

2.5.2 Challenge of shallow trench isolation by HDPCVD

In past gap fill characterization, its performances enhanced by (A) higher source RF power, (B) lower bias RF power, (C) lower process pressure and (D) higher deposition/sputtering (D/S) ratio as experience. (A) and (B) generally make smaller width of sheath in plasma. The way of (C) gives lower collision probability. These directions give the higher amount of ion species which has vertical directionality. Due to reduce the re-deposition inside the trench, which decreases the bottom up coverage and leads void formation, a process style of (D) is required. All these approaches are focusing on increasing the bottom up coverage, (shown in figure 2.31a, b) however these past approach faces that the real aspect ratio in partial fill gradually becomes bigger (shown in figure 2.32 a), and finally shows the limitation of gap filling beyond 90nm node. The impotence to achieve the void free beyond 90nm STI is the reducing the oxide growth on top of Silicon nitride (SiN) without

re-deposition amount though the all past learning (figure.32b). The effective improvement comes from the additional H_2 gas in deposition process. The sputtered component by light atom is known as prior coil model, which does not have re-deposition inside the trench, though the heavy atom is described by Cascade model. In addition to this, H_2 plasma provides small chemical etching of oxide. The partial fill profile at the open field after H_2 sputtering suggests our getting these effects. And the plasma density analysis leads the right H_2 doped process window.
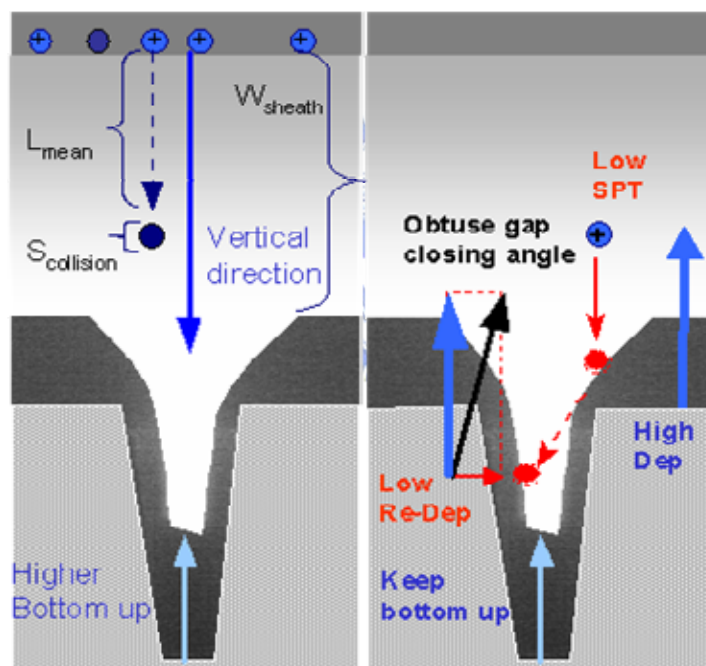
Figure 2.31   HDP-CVD past gap filling approach of
(a) less collision (left), and (b) geometry (right).

On the equal importance, the maxi H_2 sputtering rate has to be used **[50]**. H_2 flow dependence of sputtering has the max point. Due to emphasis the hydrogen effect, the suitable oxygen sputtering is required. Even the maximum H_2 sputtering, which is defined as above-mentioned for less top oxide growth

and higher gap opening, is not enough to keep the gap opening. On the other hand, excessive oxygen flow leads the void formation inside trench. Since the H_2 implantation is well known to happen the Silicon lattice damage, many manufacturers detest using hydrogen deposition in STI dielectric gap fill process in 65nm generation and beyond.
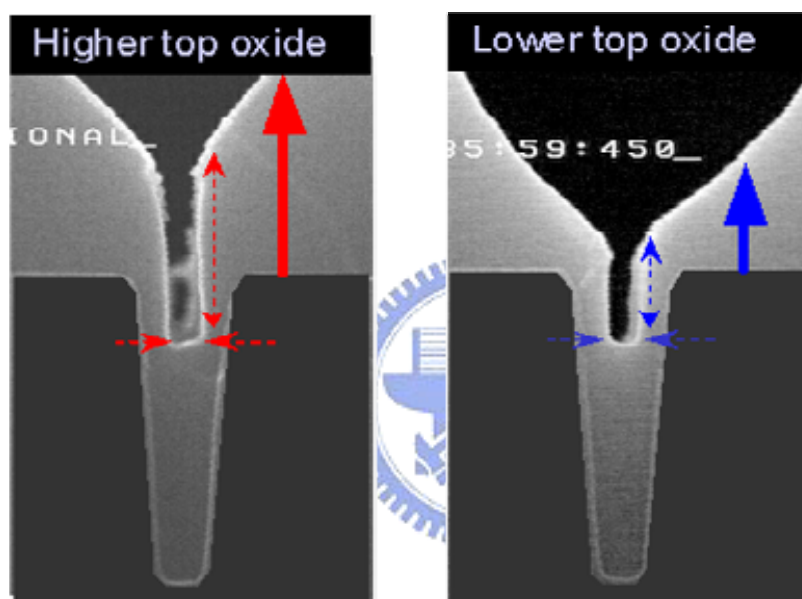
Figure 2.32   New geometrical gap filling model

(a) Conventional gap fill approach, and

(b) New model which has lower top oxide growth.

A viable alternative TEOS/Ozone based on TEOS/Ozone CVD is being developed to meet shallow trench isolation gap fill. High Aspect Ratio Process of SACVD development address two important problems, it is not only extendibility of gap fill technology, but also damage limitation of silicon lattice.

Chapter 3
Experimental procedure

3.1 Introduction

As the dimensions of ULSI circuits continue to shrink below the sub-quarter micron technology, shallow trench isolation (STI) is required as an active device technology. The requirements for STI include voids free gap filling, conformal step coverage, low wet etch rate, metallic contamination, and chemical mechanical polishing (CMP) compatibility. The available options for such trench filling includes Ozone/TEOS ratio based thermal processes performed either at APCVD (Atmospheric Pressure) or SACVD (Sub-Atmospheric), and silane based high density plasma CVD. Both chemistries have been proven to yield void free gap filling with different advantages and disadvantages relating to process integration in the technology of advanced DRAM.

However, HDPCVD is increasingly finding with difficulty to provide a good gap filling solution for the more aggressive STI structures at technology nodes of less than 70nm node dynamic access random memory DRAM. Rapid progress in transistor scaling has made gap filling technology critical for all advanced devices, but achieving void-free, high aspect ratio gap fill is becoming increasingly challenge. HARP (high aspect ratio process) will be the CVD gap filling technology to meet stringent 65nm node technology with high aspect ratio requirements (>7:1 aspect ratio) for STI (shallow trench isolation),

high temperature SACVD USG (HARP) does not require any pre-treatment process, and it does not allow any plasma attack to reduce the risk of devices damaged by high density plasma.

a: Actual spacing
b: Silicon trench depth
c: Nitride to Nitride
d: Si to Si
e: 1/2 trench depth
f : 1/3 trench depth
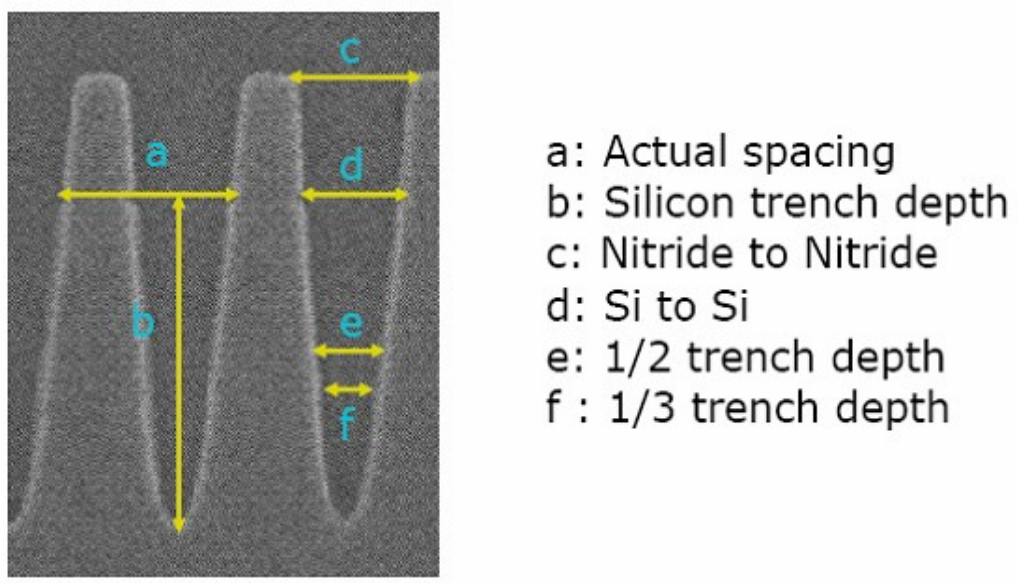
Figure 3.1   65nm node STI trench structure.

3.2 Evolution of HARP SACVD

3.2.1 HARP chamber configurations

The configurations of HARP chamber is much similarly to SACVD, but there is some different in both of block plates and showed heads. Because of the wafer bowling after thin film deposition by the low deposited rate, and vacuum chuck heater is the other characteristic hardware configuration for HARP SACVD chamber. Vacuum chuck heater is a heater flowing with Helium to attract wafer onto the heater surface by pressure servo during

process deposition. HARP systems mainly divide into process chamber body, liquid delivery controller and pump system.
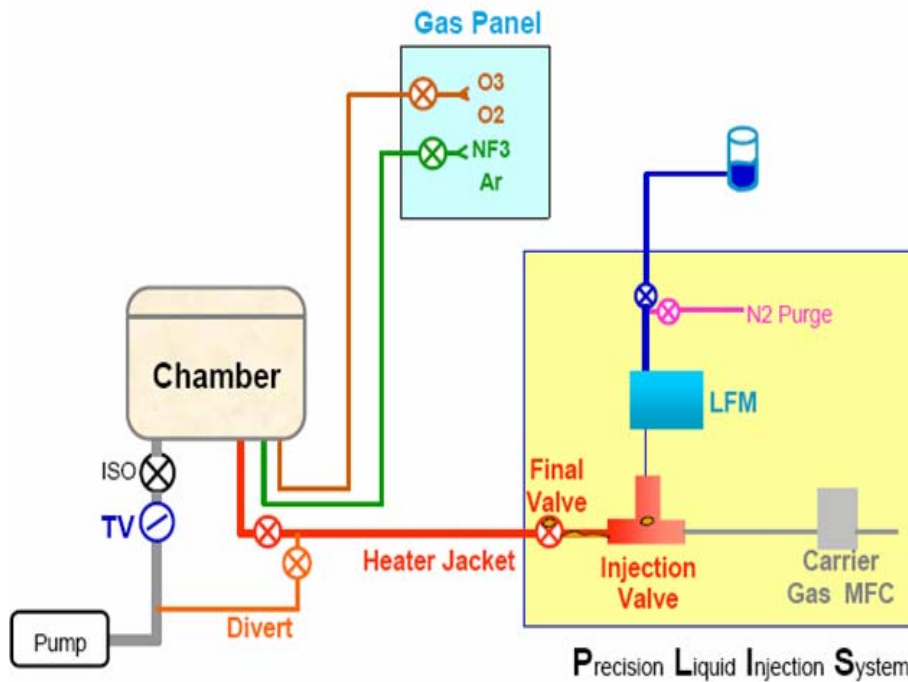
Figure 3.2   Chamber design of SACVD for high aspect ratio process.

HARP is the twin chamber designed by sharing the same pressure control, while temperature control is independently for each heater during processing. Due to HARP is the thermal process, there is no any RF or DC power to generate process gas or liquid into plasma, SACVD process is the decomposition process by using high concentration of ozone and high temperature to form dielectric film.

Remote plasma source RPS is used to clean chamber without any plasma damaged to chamber body and process kits. A larger unit of RPS provides a high efficiently power to break down high flowing clean gas of NF_3.
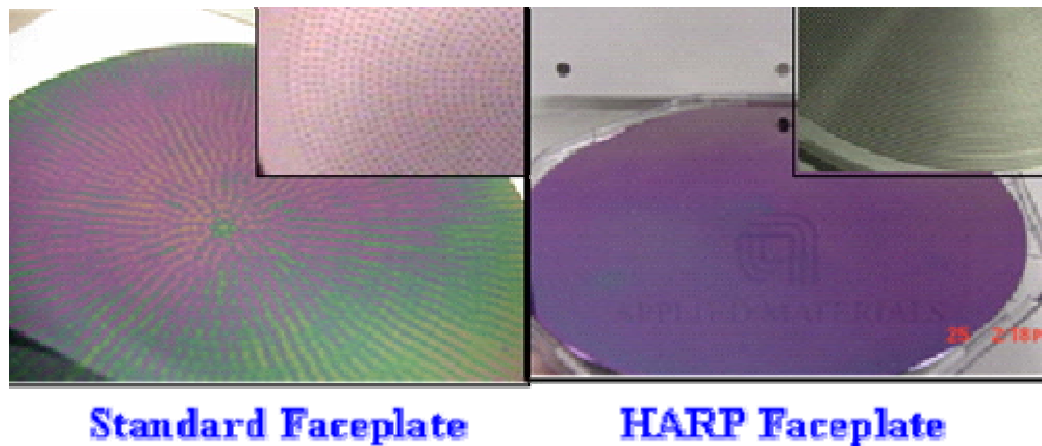
Figure 3.3　Face plates comparison between standard SACVD and

　　　　　HARP SACVD.

It is apparently that the HARP faceplate with the slots is quite effective in eliminating the spots and streaks. On a standard faceplate, the gases flow through a 62 mils holes and then through a 29 mils holes prior to exit from the showerhead. This "nozzle" designed increases the exit velocity of the gases. On the HARP faceplate, the gases initially flow through a 10mil hole, followed by a 25mils hole and then flow through an azimuth slot machined on the faceplate, the 25 mils hole and the 31 mils azimuth slot effectively reduce the downward vertical velocity of the gases. Reduction in downward velocity will reduce the intensity of the "spots". The alignment of the holes can also be eliminated by the design of azimuth slots **[51]**.

This model predicts that as the spacing reduces, the flow towards the edge of the wafer dramatically increases due to the large pressure drop from the center to edge of the blocker and faceplate. One method of addressing this problem is by increasing the pressure drop across the faceplate by reducing the diameter of the holes. A larger pressure drop across the faceplate will reduce

the effect of spacing overall uniformity by redistributing the flow between the blocker and faceplate.

3.2.2 Liquid delivery systems.

TEOS is the standard reactant for HARP process. Individual vapor line (IVL) high conductance GPLIS available on HARP chamber only, which supports high carrier gas flow (41slm) for high TEOS flow vaporization. A certain type of carrier gas, e.g., N_2 or He, is utilized to deliver vaporized TEOS and liquid dopant sources to the process chamber to reduce gas-phase nucleation for particle control. Due to their distinct physical properties, such as heat capacity and thermal and mass diffusivity, different carrier gases may result in different film characteristics. In this study, we report a complete analysis using N_2 as the carrier to develop a better understanding of the reaction mechanism and to achieve superior film quality. The N_2 carrier process satisfies the technical requirements for STI. The main drawback for this process is the high cost per wafer due to its low deposition rate and high He cost in the Asia Pacific.

TEOS flow is controlled by digital liquid flow meter T4. The T4 LFM has achieved the strict requirements necessary for the HARP process which include faster response, minimal ambient temperature effects, and accurate ramp rate. The T4 LFM also resolves the device leakage issue caused by the slow shut off of the do-pants on BPSG processes [52]. The T4 LFM dimensions and hardware requirement is identical to the existing liquid flow meters and thus is a drop in solution to our existing platform.
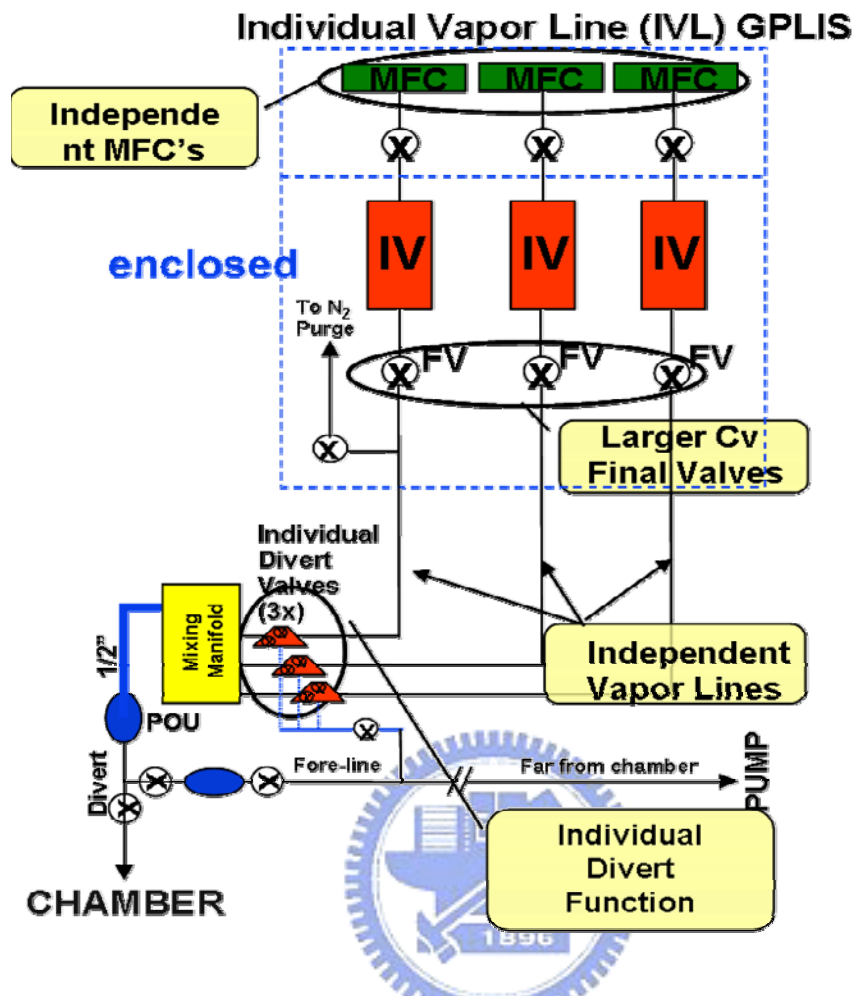
Figure 3.4 Individual liquid line modules.

The response time of T4 LFM is about 5-7 seconds. On entire range of LFM flow rate is unparalleled by other liquid flow device in the market. Further, the manufacturing factory will set PID values to allow the end user to install the hardware and without any changes or modifications to the hardware, making this LFM a truly a "plug and play" devices.

Vaporization test of liquid is for examining total amount of carrier gas flow during the new process development, exception of this, liquid line clogging can be used for troubleshooting by using vaporization test.

Figure 3.5   TEOS vaporization test.

3.2.3 Pump systems

There are a lot of by-products produced during high temperature process reaction. Most of the byproduct shall be pumped through gate valve and throttle valve to dry pump. Reliable pressure control likes high process pressure (600torr), and high gas/liquid flow rate (80slm) is well by using flapper-type throttle valve with D-Net control. The faster pressure servo and accurately pressure control are very important to HARP process. The slower pressure servo will induce particles and low throughput effect.
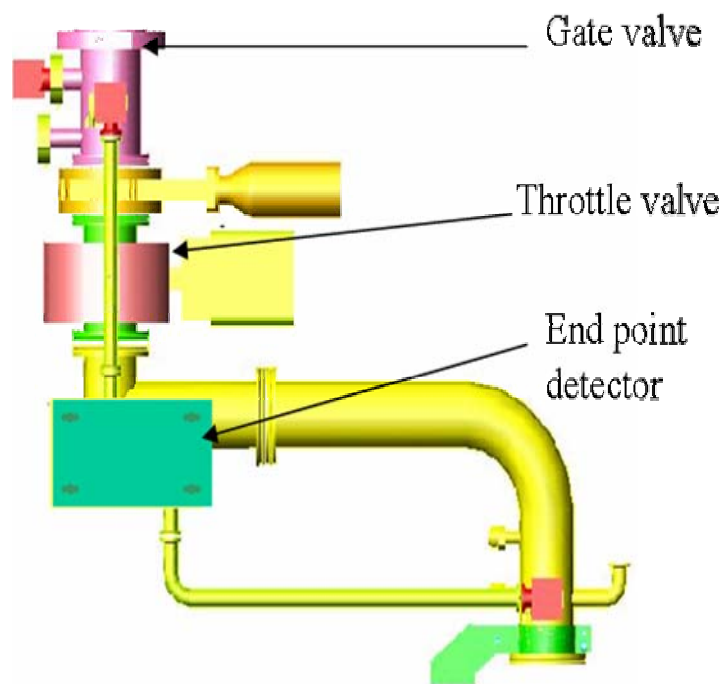
Figure 3.6   Pumping line systems.
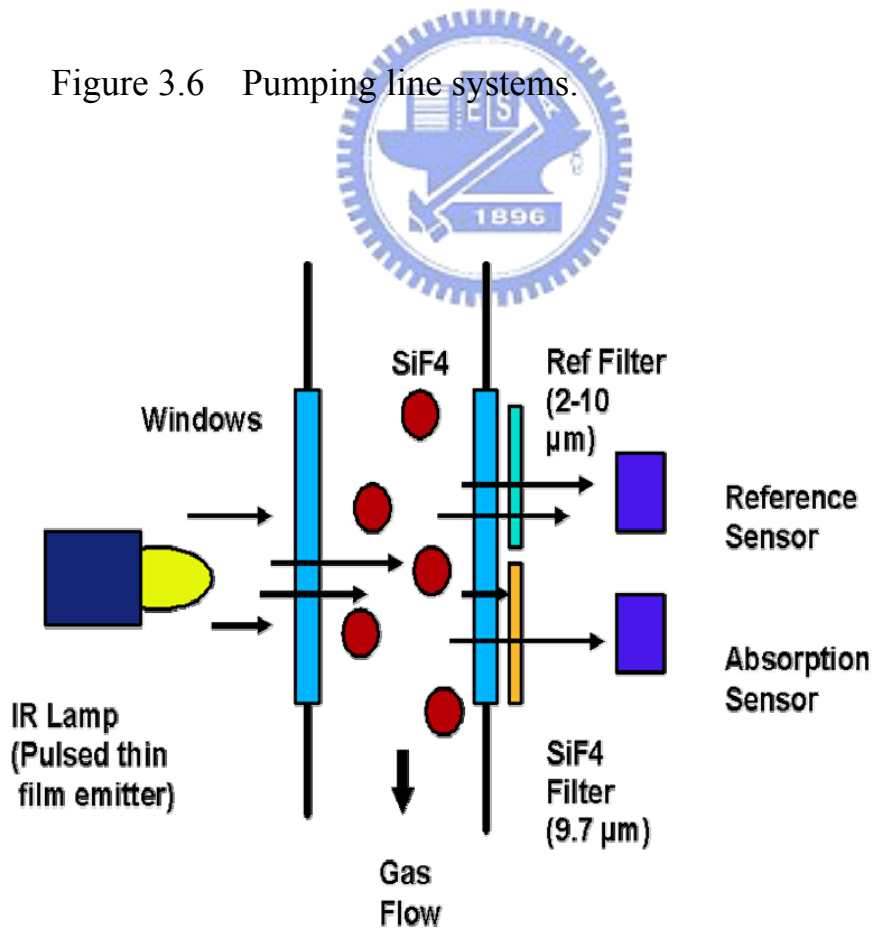
Figure 3.7   Basic concepts of NDIR endpoint detector.

3.2.4 NDIR end point detector

The NDIR endpoint unit is configured on the Producer 300mm chamber with a bypass valve to provide a consistent measurement of SiF_4 during the chamber clean process (fig-3.6). The endpoint times calculated is using slope of the endpoint signal, vary by approximately 10% and are very consistent within that range. Additionally, the endpoint times provided by the NDIR endpoint unit and slope algorithm result in a clean chamber over extended runs [53].

Optical methods that look at the effluent gas during the clean are the most used. Of the optical methods, there was a possibility of optical emission or optical absorption. Optical emission requires generating plasma in the gas stream and looking at that light through a "window". Optical absorption uses two windows and its own light source. It shines light through the gas stream and looks at what comes out. In either case, the window problem exists and by using optical absorption, the problem of generating a consistently plasma will be eliminated. In fairness, the problem of providing a consistent light source is not an easy task. Another difference between the two technologies is that the optical absorption unit looks for the presence of fluorine, while the optical absorption unit looks for SiF_4.

Currently, the NDIR endpoint unit is being developed to produce a signal to tell when the clean process is completed and it can perform this task well. This simple endpoint function is good and offers significant advantage over a "timed" chamber cleaning process. The real advantage of this product is its

potential to provide more data about the cleaning process. For example, there have been many questions about the "humps" in the SiF_4 trace.
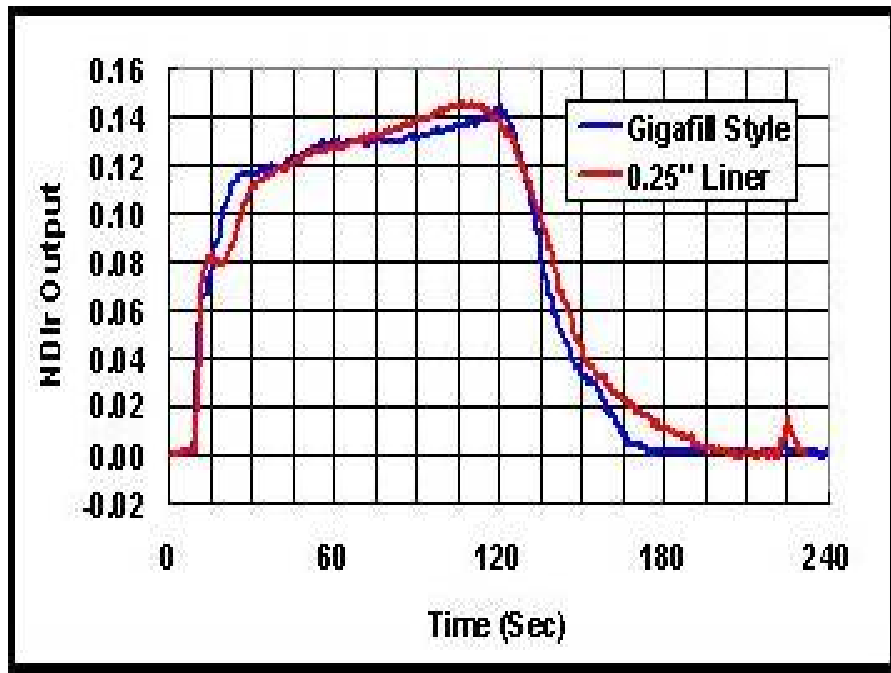
Figure 3.8   NDIR end point graphic monitoring.

What do they represent? Can anything be done to change these humps? What happens when the chamber hardware is changed? During the time the NDIR unit has been developed for endpoint, it has also offered information on things like alternative vendor faceplates and information on different process kit parts. In fact, the NDIR endpoint is being included as an analysis tool for the development of a new chamber pumping ring that which is attempting to minimize the deposition in "slow cleaning locations".

3.3 Methodology used:

3.3.1 Experimental preparation

HARP SA-USG was deposited by using Applied Materials producer chamber (fig-3.2), equipped with the precision liquid injection system (PLIS) for TEOS delivery and the high temperature ceramic heater. Remote microwave technology was used for cleaning to reduce metal contamination and to improve cleaning efficiency. All film properties were evaluated on 300mm p-type Silicon (100) substrates. The film thickness and uniformity were monitored by KLA Fx-100

KLA Fx-100 is very popular methodology tool for film property monitoring in semiconductor manufacturing, it is accurately in stability and repeatability for widely film applications include film thickness, reflected index and stress.
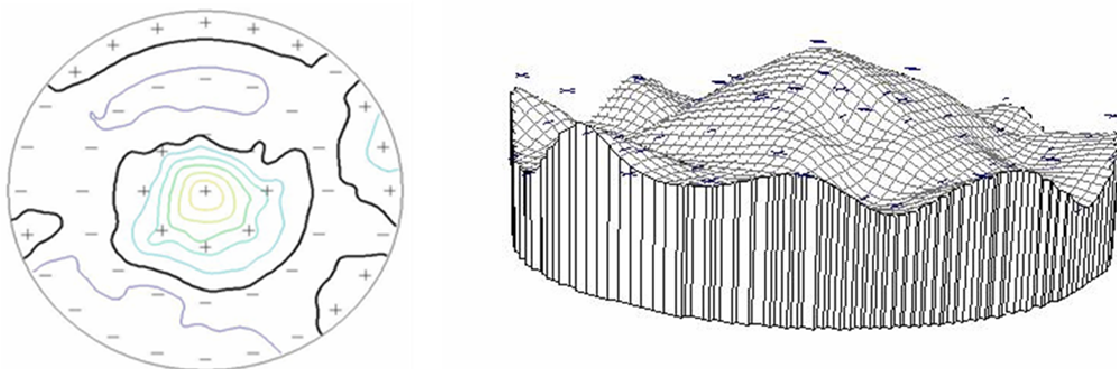
Figure 3.9　Contour map of HARP film by using KLA Fx-100.

The wet etch rate ratio (WERR) which is a good indicator for film integrity was performed in a BOE 300:1(300 NH_4F/ 1 HF/ 540 H_2O) referring thermally grown oxide film. We do not recommend dry etch rate (low process pressure, high RF>1000W with C_2H_2 gas) as a film monitoring because its faster plasma etch rate (>300nm/ min) results in unstable repeatability and reliability monitoring.

All SEM samples were decorated using 6:1 BOE for 10 seconds and a film coating, the pictures were taken on Hitachi 5200 SEM.

3.3.2 Experimental procedure

The effects of vary of temperature, pressure, spacing, and TEOS flowing on the deposition rate and wet etch rate ratio (WERR) have been compared for these two processes. The experiments were done with a nominal set points of 600Torr, 540 ℃, 1400mgm TEOS, 330 mils spacing, and 27slm ozone at 12.5 wt%. The carrier gas flows were optimized for best thickness uniformity with 8slm for Nitrogen.

Since both low shrinkage and WERR are the indicators of good gap filling, a set of experiment was created to explore and to optimize these film properties with higher deposition rate prior to gap fill testing, the detailed process experiments are outlined in Table-4.1.

Base on last experience, a well gap filling extendibility should composition of high process pressure, high O_3/TEOS ratio and low deposition rate. Thus we will approach a high O_3/TEOS ratio and a low deposition rate in

the initial deposition to achieve trench gap filling, throughput enhancement will be improved in bulk film by increasing of TEOS flow with low concentration of ozone. It is needed to explore basic film properties by the experiments. From the experiments, optimization of recipes was tested on production wafers to monitor gap filling performance.

Deposition rate improvement was clearly for all recipes. Increases in pressure, heater temperature, and Ozone concentration will prohibit its deposition rate, but it still need to provide significantly higher deposition rate to meet throughput. The results are shown in chapter 4.

3.3.3 Recipe optimization:

In order to retain the fastest deposit, ion rate while providing lowest WERR and shrinkage, a recipe with high O_3 concentration was chosen along with an additional recipe using O_2 to improve uniformity. Multiple steps recipe required to satisfy not only the void free of STI trench, but also does the throughput compatible as HDPCVD.

To achieve STI gap filling, we approach O_3/TEOS ratio variation in deposition steps. We found that high O_3/TEOS ratio during deposition is more favorable for gap filling in SA-BPSG. There were three-steps recipe was set up to meet throughput and gap filling capability. During the process, the initial step aims at having better nucleation of linear surface with very low TEOS flow rate and very high ozone concentration to achieve gap filling, TEOS ramps process that introduces very low amounts of TEOS in a Ozone rich environment to get a high quality initial oxide layer followed by a continuous

Recipe#	Chamber Pressure	Heater Temperature(C)	O$_3$ sccm	O$_3$ wt%	N2 sccm	TEOS mgm	O$_2$ sccm
1	700	550	27000	17.0	5000	1000	
1	600	550	27000	12.5	8000	1400	
2	600	530	27000	12.5	8000	1400	
3	600	540	27000	12.5	8000	1400	
4	700	540	27000	12.5	8000	1400	
5	500	540	27000	12.5	8000	1400	
6	600	540	27000	12.5	9000	1400	
7	600	540	27000	12.5	7000	1400	
8	600	540	27000	12.5	8000	1200	
9	600	540	27000	12.5	8000	1000	2000
10	600	540	27000	12.5	8000	1400	4000
11	600	540	27000	12.5	8000	1400	
12	600	540	27000	15	8000	1400	
13	600	540	27000	17.0	8000	1400	

Table 3.1   Experimental design table.

but slow increase in TEOS concentration, so that the subsequent layers are deposited faster without adversely affecting the gap filling. Bulk film, which is the major portion of the film stack, could be deposited at a much higher rate. In a typically requested 700nm thick film, only the first 200nm

is needed for completely trench filling, the rest of 500nm does not require filling any narrow trenches and this is where the attention is focused in order to improve throughput.

Deposition rate could be increased by simply increasing the totally amount of TEOS used in the final step of recipe. Decrease in process spacing between wafer and gas distribution plate (show-head) to minimize the mean free path is another dominant for faster deposition rate. Changing of TEOS flow rate and heater spacing versus time is as shown in figures 3.10.
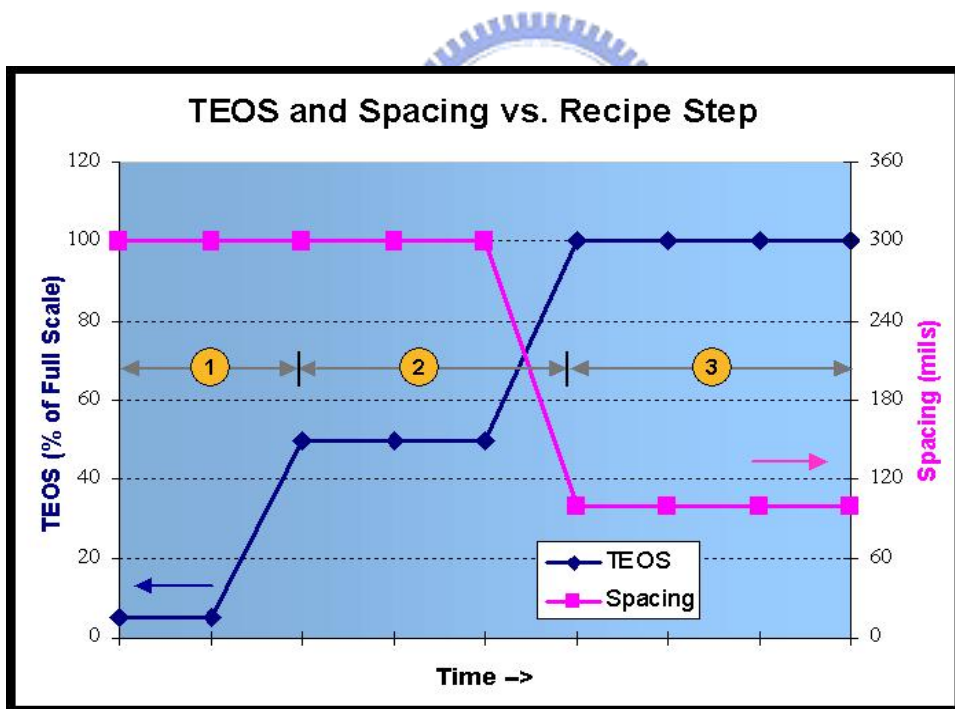

Figure 3.10   TEOS flow rate Vs time during 3-step HARP USG
for gap filling.

Three steps recipe is required to achieve STI trench without throughput suffering. The initial step deposition approach with a high O_3/TEOS ratio

results in a more homogeneous nucleation layer onto trench surface, while the second-step is to fix trench gap filling with TEOS ramp process that which introduces very low amounts of TEOS in a rich Ozone environment.

Step	Time (s)	Temp. (℃)	Pressure (Torr)	TEOS (mgm)	Carrier Gas (sccm)	O₃ flow (sccm)	O₃ conc (%)
Dep 1	168	540	600	1000	13500	27000	17
Dep 2	168	540	600	2700	13500	27000	17
Dep 3 (bulk film)	45	540	200	6000	13500	15000	12.5

Table 3.2   Optimized three steps recipe for gap fill.

In order to extend gap filling capability, the marginal windows monitoring is required to safe STI gap filling to prevent of some parameters drifting

DOE for gap fill	Dep 1				Dep 2	
	first step time (seconds)	transition step		ramp up rate (RR/s)	TEOS (mgm)	time (seconds)
		initial TEOS (mgm)	final TEOS (mgm)			
DOE_1	168	1000	2700	5	2700	142
DOE_2	336	1000	2700	15	2700	42
DOE_3	68	1000	2000	5	2000	330
DOE_4	68	1000	1500	15	1500	540
DOE_5	240	300	2700	10	2700	140

Table 3.3   Split conditions for STI gap fill.

3.3.4 HARP USG anneal by furnace

The annealing conditions are very important for the gap-fill. As reference to SA-BPSG for pre-metal gap filling, steam annealing is much helpfully to avoid seams or voids in the trench. Thus, two steps annealing will be approached in our experiment, The priority steam annealing at low temperature favors in gap filling , and then followed by 1000℃ dry annealing to densify the whole film.

Splits	Steam anneal		Dry anneal	
	temperature (℃)	time (seconds)	temperature (℃)	time (seconds)
Split_1	750	30	1000	30
Split_2	750	60	1000	60
Split_3	850	30	1000	30
Split_4	850	60	1000	60
Split_5			1000	60

Table 3.4　Post HARP film annealing condition splits.

Chapter 4
Results and discussion

4.1 Advancement in Gap-fill

A number of approaches were attempted to improve gap fill that included surface pre-treatment, a multi-step dep-etch-dep process, optimization of the existing process in the critical variables, and a high ozone process in which TEOS is introduced in a varying but controlled manner(TEOS ramp). From this work it became apparent that the first few oxide layers are critical in achieving a good gap-fill. The high quality oxide film essential for good gap-fill needs an extremely ozone rich environment coupled with low TEOS concentration in the gas phase. But this leads to deposition rates that are unacceptably low. At the time it was conjectured that the later layers may tolerate increasingly poorer ozone environment or conversely increasingly higher TEOS concentrations in the gas phase. Development of TEOS ramp process that introduces very low amounts of TEOS in ozone rich environment to get a high quality initial oxide layer, after that followed by a continuous but slow increasing in TEOS concentration so that the subsequent layer is deposited faster without adversely affecting the gap filling.

4.2 HARP film properties

We approach a very low TEOS flow to drive reaction into a starved state regime, resulting in a more homogeneous nucleation layer with less surface

selective film growth. Following nucleation layer step (TEOS ramp) with relatively high O_3/TEOS ratio layer of sufficient thickness is to fill small to moderately large trench widths.

4.2.1 Experiment results

Recipe#	Deposition Rate (A/min)	Uniformity Range%	Shrinkage %	Refractive Index	WERR	Stress (Dynes /cm2)
Recipe	590	3.70	2.87	1.465	3.32	< 1E9
1	900	5.31	4.15	1.4421	3.87	1.79
2	950	2.86	4.34	1.4419	3.93	1.8
3	920	4.13	4.90	1.4419	3.93	1.8
4	890	3.31	3.91	1.4417	3.87	1.8
5	930	5.63	4.56	1.4422	3.93	1.65
6	910	5.28	4.42	1.4418	3.85	1.81
7	900	3.82	4.13	1.4418	3.87	1.87
8	800	5.53	3.78	1.4423	3.6	1.7
9	650	7.1	3.09	1.4421	3.4	1.68
10	960	3.18	4.43	1.4423	3.79	1.6
11	980	2.88	4.49	1.4424	3.8	1.63
12	890	4.42	3.79	1.4416	3.7	NA
13	870	4.46	4.71	1.4416	3.68	NA

Table 4.1   Results of experiments.

Table 4.1 shows high O_3/TEOS ratio will have a low deposition rate and a low wet etch rate that which met the target we expected. Deposition rate improvement was clear for all recipes. Increases in pressure, heater

temperature, and O_3 concentration caused a decrease in deposition rate. Because deposition process includes force convection, boundary-layer diffusion, surface absorption, decomposition, there are several variables to be controlled. The heater temperature, pressure, flow rate and ozone concentration are very important factors in our experiment.

Deposition rate can be grouped into gas-phase processes and surfaces process. For the gas-phase process, the concern is the rate at which gases impinge on the substrate. This model considers the rate at which gases across the boundary layer that separates the bulk regions of the flowing gas and the substrate. On the other hand, the low temperature the surface reaction rate is reduced, and eventually the arrival rate of reactants can be exceeded. The rate at which they are consumed by the surface reaction process, thus, at a high temperature, the deposition is usually mass-transport-limited. Deposition rate no longer increases with temperature. Figures 4.1-3 show the effect of wafer temperature, chamber pressure and ozone concentration on film deposition rate of HARP USG processes. The high temperature USG shows a very strong surface temperature effect and ozone concentration, however weak dependence on pressure, this may indicate the USG process could be controlled by surface reaction steps, which explains the surface sensitivity of this process due to the participation of surface atoms.

Since the gas-phase temperature is controlled by thermo -conductivity of the gas molecules. It is not affected very much by any minor change in surface temperature while holding the chamber wall at a constant temperature. However, as the chamber pressure changes, an optimum deposition rate could

be achieved depending on other process conditions. In low pressure regime, the reaction rate is low due to insufficient gas-phase intermolecular collision. On the other hand, diffusion rate is faster due to the long mean free path of the gas-phase species. Therefore, at low pressure, the gas-phase reaction controls total deposition rate.

Furthermore, deposition rate is also determining by the ratio of O_3/TEOS, the lower ozone concentration the higher film deposition rate.
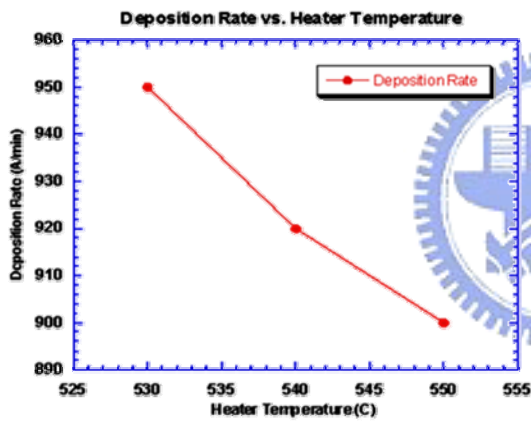

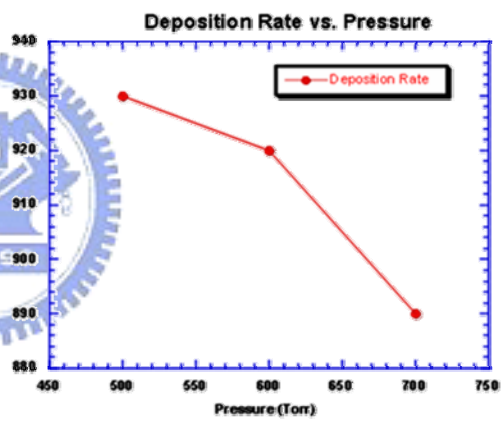Figure 4.1 deposition rate against heater temperature
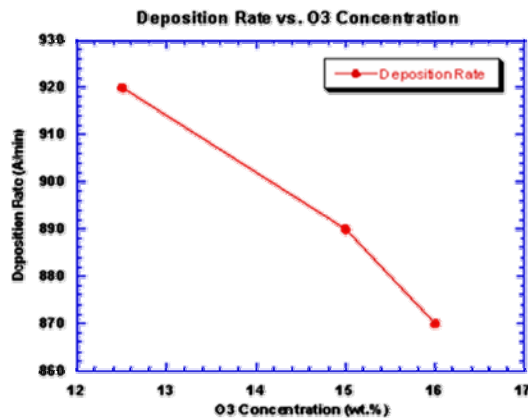
Figure 4.2 deposition rate against pressure

Figure 4.3 deposition rate against ozone concentration

Shallow trench isolation has emerged as the isolation scheme of choice for advanced technology of DRAM due to its high packing density, planar topography and low junction edge capacitance. Process flow of advanced DRAM is after STI trench gap filling, chemical mechanical polishing (CMP) is used to planarize and remove excess trench oxide over the patterned oxide-nitride stack. HDPCVD films are significantly more compressive that which can be beneficial because the compressive stress is associated with a lower wet-etch-rate (WER) and thus reduce wet-etch damage to the STI trench as well as better polish performance, thus , the experiments designed for HARP SACVD, wet-etch-rate is the criteria duplicating before gap filling process. The blanket wafers were used for WERR of DOE (design of experiments) testing with variation of chamber pressure, process temperature and ozone concentration before optimization of HARP recipe for gap filling.

The effects of temperature, pressure, ozone concentration, and TEOS flow on deposition rate and wet etch rate ratio (WERR) are studied in these experiments. The experiments were done with a nominal set points of 600torr, 540℃, 1400mgm TEOS, 330 mils spacing, and 27slm ozone at 12.5~17 wt%. The carrier gas was optimized for the best thickness uniformity (4slm for Nitrogen). Figures show WERR data of experiments as below: The effect of heater temperature, ozone concentration and process pressure on WERR. At higher deposition temperature, WERR is lower due to higher density of dielectric films.

It is found that at higher pressure environment, dielectric film becomes denser because the average distance a particle can travel before colliding with

another particle, wet-etch-rate shows lower with BOE 300:1. When process temperature increases, the film becomes more compressive and low WERR be found in BOE testing. Finally, it is also found ozone concentration increases from 12.5% up to 17%, WERR is low with ozone concentration increasing. The wet etch rate is very important to STI gap fill process, the following figures show WERR tendency for changing of some process parameters likes temperature, pressure, and O_3 concentration.
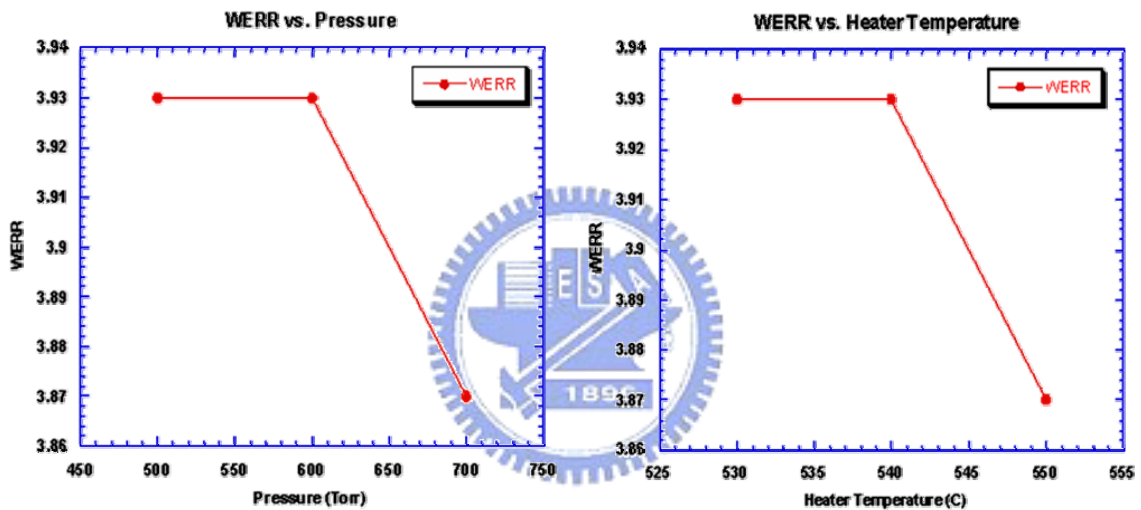

Figure 4.4 wet etch rate against process pressure

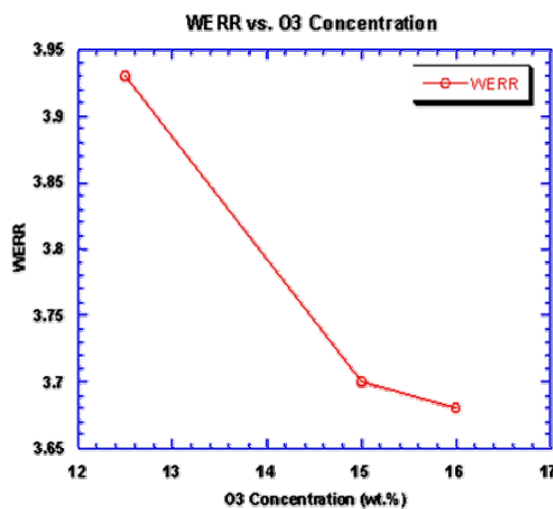Figure 4.5 wet etch rate against heater temperature

Figure 4.6 wet etch rate against ozone concentration

For HARP SACVD process approached to STI gap fill, after un-doped silicon oxide deposition, a subsequent heating is necessary until the dielectric film soften and reflow, the procedure is named annealing. The reflowing morphology of the un-doped silicon oxide will also be determined by the heating temperature, heating time, etc. In general, reflow process need a heating temperature as high as 950 to 1100℃ in 30 to 60minutes per a cycling. Furnace annealing time couple at high temperatures often result in significant diffusion, leads to remarkable junction movement, and out-diffusion. In addition, high-temperature reflow for a longer time also causes further oxidation of silicon substrate. These phenomena must be avoided in the fine geometry ULSI devices. In order to prevent these problems, a thin liner oxide is required to protect silicon side wall. On the other hand, two steps annealing are proposed for HARP USG gap fill in STI trenches, steam annealing with water vapor drain during processing results in seamless and void free without attacking of the underlying devices, and then a subsequent dry annealing with nitrogen flowing will be used to make the dielectric film denser and more stable. Obviously, the step -angles, reflected the smoothing topography, will increase with high thermal annealing temperature and time. Thus, in order to achieve seams for STI trench, steam annealing with water vapor source is required for gap fill and the subsequent dry annealing is used to densify the dielectric films with nitrogen flowing.

Shrinkage experiments were conducted by using 1000℃ furnace dry annealing with N_2 flow for 30minutes. The data shows increases in pressure shrinkage decreases, beside, it is also found that increases in TEOS flow, shrinkage increases. The shrinkage rate of dielectric films during annealing is

also a function of ozone concentration, as shown in figure 4.9. Because of their porosity, $O_{3/}$TEOS CVD films are often accompanied by plasma-assisted oxides to permit planarization in ULSI process. It also found to increase process temperature that which will leads shrinkage rate low.
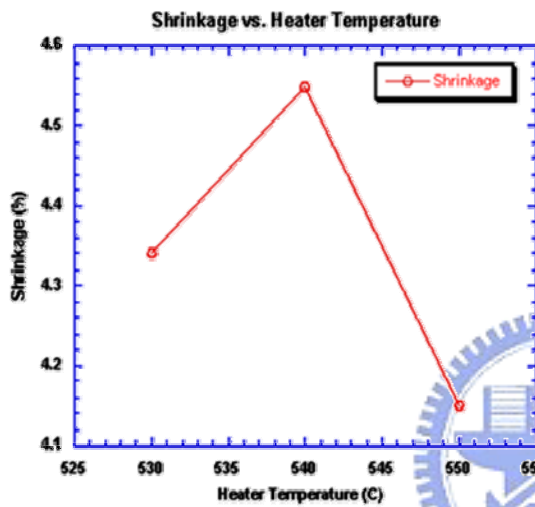

Figure 4.7 shrinkage rate against heater temperature
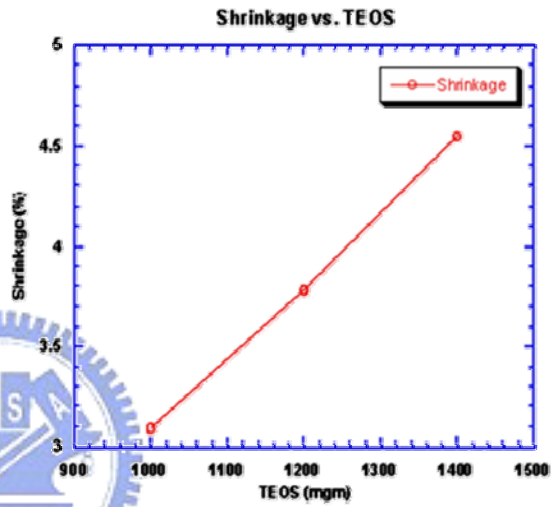

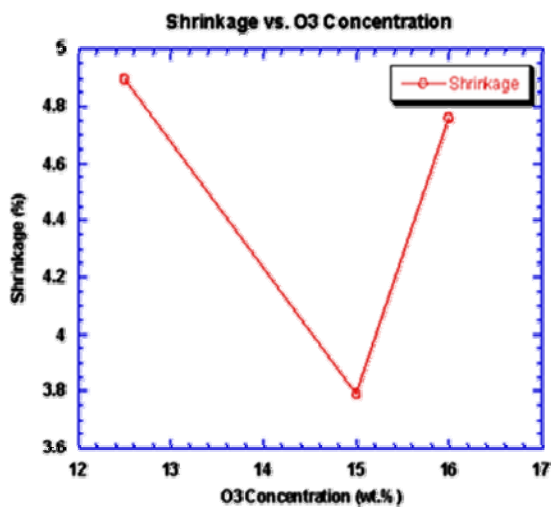Figure 4.8 shrinkage rate against TEOS flow

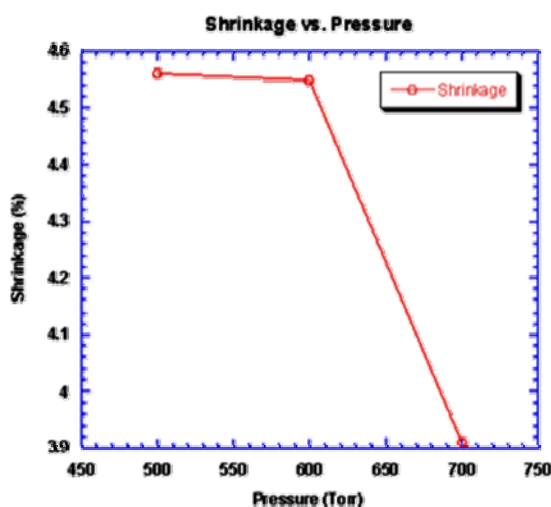Figure 4.9 shrinkage rate against ozone concentration

Figure 4.10 shrinkage rate against process pressure

4.2.2 Film properties study in three steps recipe

Step	Stress after deposition (Mpa)	Stress after anneal (Mpa)	Wet etch rate (refer Thox)
Dep 1	-228	-459	1.19
Dep 2	-149	-445	1.2
Dep 3	10	-217	1.35
Wet etch rate : BOE 300:1 for 180 seconds and refers to thermal oxide (TH$_{ox}$)= 10.2nm per minute			

Table 4.2   Film properties monitoring in each deposition step.

In order to identify film properties for each optimized recipe like wet - etch - rate, stress after deposition and stress after furnace reflowing, it found that the dielectric films are soften when high TEOS represents. Less compressive stress and faster wet etch rate be observed in high flow of TEOS. But a very interesting result was found that the dielectric films became more compressive in stress in high temperature annealing.

Dep-1				Dep 1+2			
DOE	THK (nm)	Uniformity (%)	Reflect index	DOE	THK (nm)	Uniformity (%)	Reflective index
DOE-1	684	3.49	1.4483	DOE-1	1937	2.03	1.4486
DOE-2	1612	2.98	1.4493	DOE-2	1983	4.44	1.4586
DOE-3	195	4.3	1.4466	DOE-3	2056	4.96	1.4652
DOE-4	130	5.22	1.4407	DOE-4	2068	5.02	1.4469
DOE-5	676	4.26	1.4463	DOE-5	2022	2.12	1.4456

Table 4.3   DOE film properties monitoring.

4.2.3 Film stability and repeatability bi-layer test

As a direct result of deposition rate, film thickness uniformity, and reflected index could be readily deduced. For HARP SA-USG process, the surface temperature uniformity of substrate controls deposition rate and thus the film uniformity. Displayed in the following figures 4.11-4.16 are the bi-layers repeatability tests. There were 50 bare-blanket silicon wafers used to monitor its stability and repeatability of the whole stack film, however, for HARP USG, uniformity pattern changes due to either the chamber pressure and/or the spacing, as gas flows play the major role in determining uniformity. Under the current optimum process conditions, for instant, pressure servo at 600torr, changing the spacing or TEOS flow will lead a drift in deposition rate and uniformity pattern. At very close spacing between gas distribution plate and wafer surface, the deposition rate becomes faster and uniformity is good. Another effect for uniformity we found, when the processing wafer is not sitting on the flat heater, uniformity pattern will drifts as a tilted plane due to mis-leveling between the heater and the gas distribution plate. This leveling effect becomes less sensitive at larger spacing, where the uniformity is solely controlled by the flow pattern and usually shows a symmetric bowl shape due to the chamber configuration and the flow dynamics of gases.

Whatever for initial deposition with low deposition rate or faster deposition rate with high TEOS representation, the thickness repeatability and stability is very consistently, and a high range uniformity was found at initial deposition due to low TEOS flow, when TEOS ramps up to 6000mgm, we

got a small range uniformity and the range uniformity was less than 1.7 per cent within wafers in repeatability test.

In the experiment, we got a very good uniformity, 2.0% for the whole bulk films through the repeatability test that which is beneficial on CMP process after HARP dielectric films deposition process.

4.2.3.1 Initial deposition repeatability test

Slot	1	5	10	15	20	25	30	35	40	45	50
Thickness (Å)	677	683	686	687	683	690	686	682	692	688	685
Uniformity (%)	3.5	3.3	3.4	3.25	3.63	3.5	3.29	3.33	3.19	3.17	3.2

Table 4.4   Initial layer repeatability test.
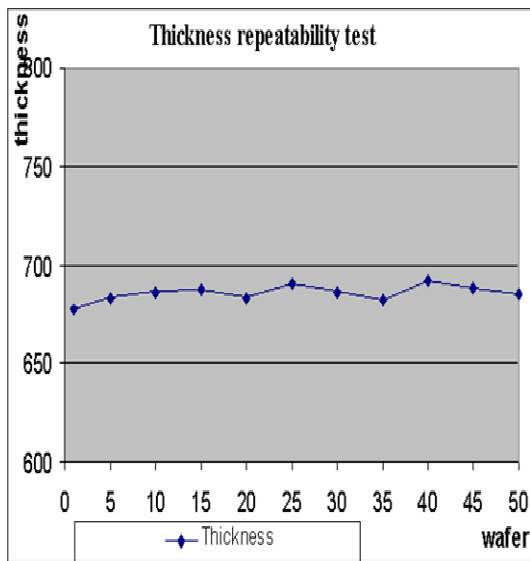
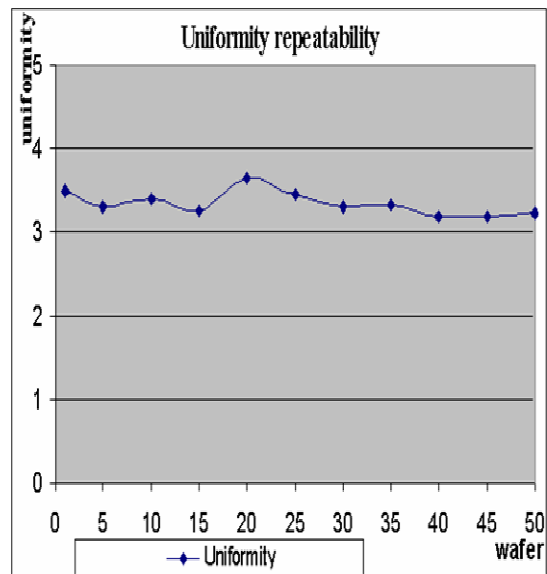Figure 4.11 initial layer thickness graphic chart   Figure 4.12 initial layer uniformity graphic chart
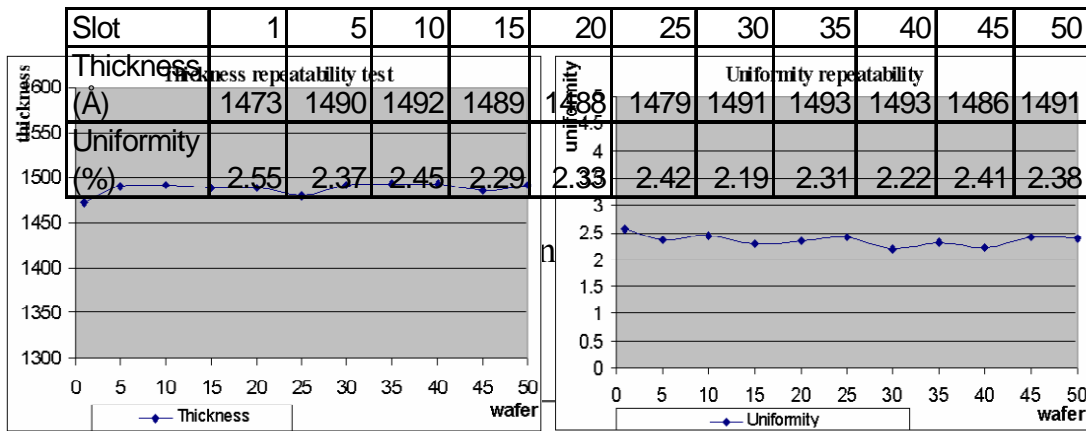
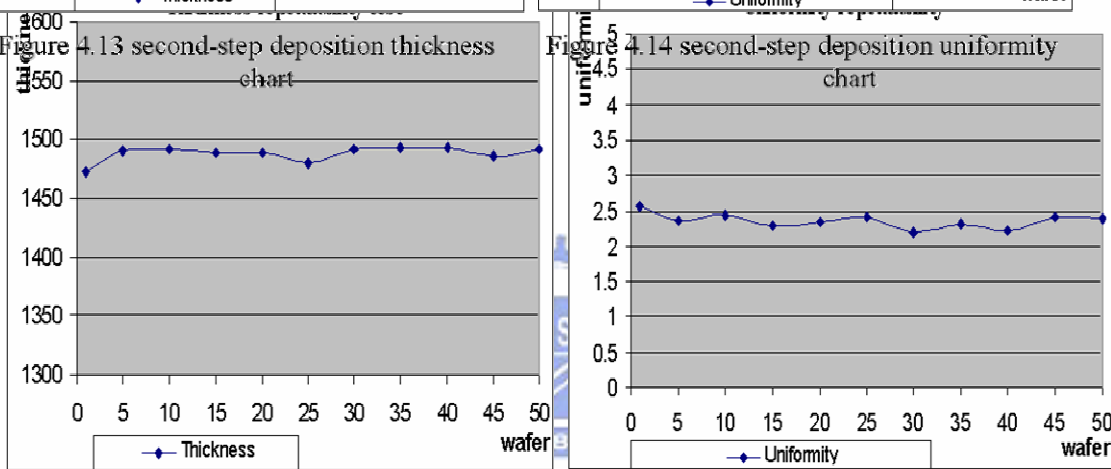| Slot	1	5	10	15	20	25	30	35	40	45	50
Thickness (Å)	1473	1490	1492	1489	1488	1479	1491	1493	1493	1486	1491
Uniformity (%)	2.55	2.37	2.45	2.29	2.33	2.42	2.19	2.31	2.22	2.41	2.38

Figure 4.13 second-step deposition thickness chart

Figure 4.14 second-step deposition uniformity chart

4.2.3.2 Third-step deposition (bulk layer) repeatability test

Slot	1	5	10	15	20	25	30	35	40	45	50
Thickness(Å)	4867	4888	4893	4876	4899	4883	4881	4933	4892	4880	4892
Uniformity (%)	1.67	1.55	1.39	1.43	1.51	1.37	1.42	1.33	1.45	1.29	1.36

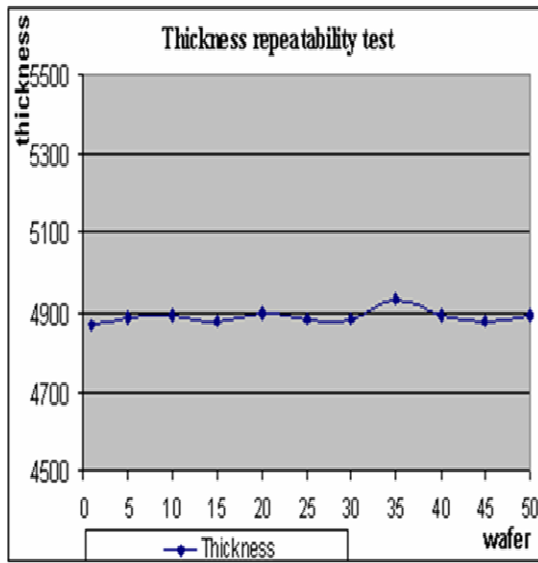Table 4.6   Bulk layer repeatability and stability test.

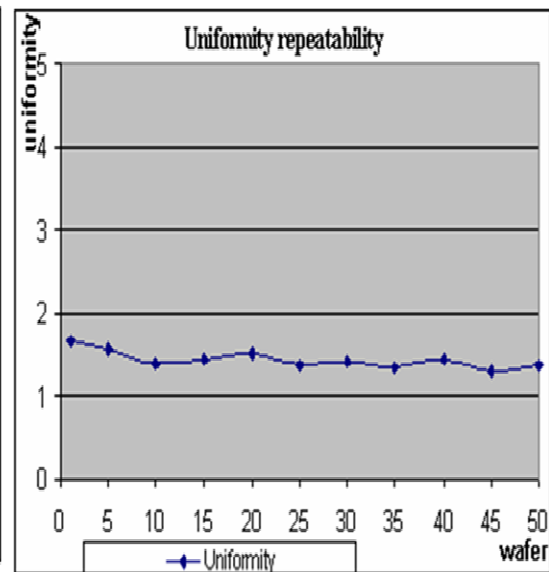Figure 4.15 bulk layer thickness chart   Figure 4.16 bulk layer uniformity chart

4.2.4   Whole-stack film stability and repeatability monitoring

For the whole film repeatability test, it found the dielectric film is also much consistently and repeatable, while the uniformity is good as we respect. The uniformity is less than 1.5% in range with wafer or wafer to wafer, beside, it is not the problem for chamber matching, if the process data is different in both stages of the chamber, there are a lot of tunable hardware parameter which can cover the chamber match issue. Heater temperature, needle valve and process spacing can compensate thickness of dielectric films drifting. TEOS flow to divert valve or flow to chamber at stable step is functional of liquid flow stability. All of these hardware and software function are beneficial to provide a better process of HARP SACVD.
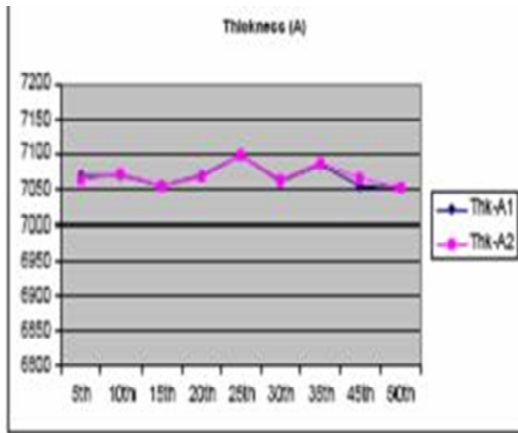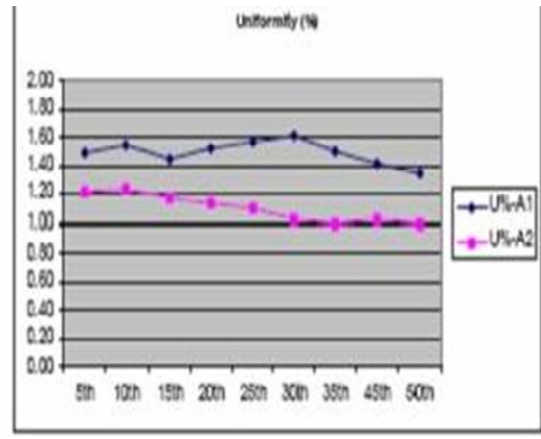
Figure 4.17 whole film thickness repeatability chart

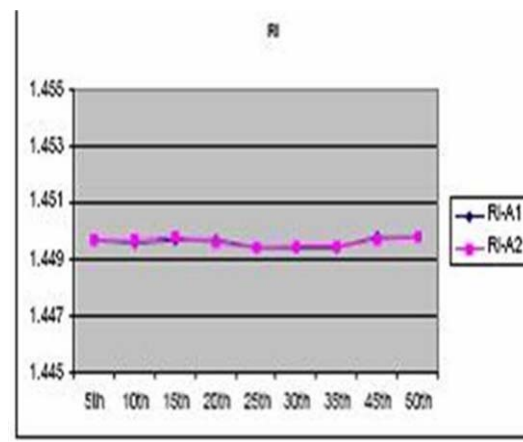

Figure 4.18 whole film uniformity repeatability chart

Figure 4.19 whole film reflected index repeatability chart

4.2.5 Wet etch rate monitoring

TEOS flow (mgm)	Etch rate (nm/min)
500	11.3
1000	14.8
1800	19.9
2700	25.7
3500	31.1
6000	46.6

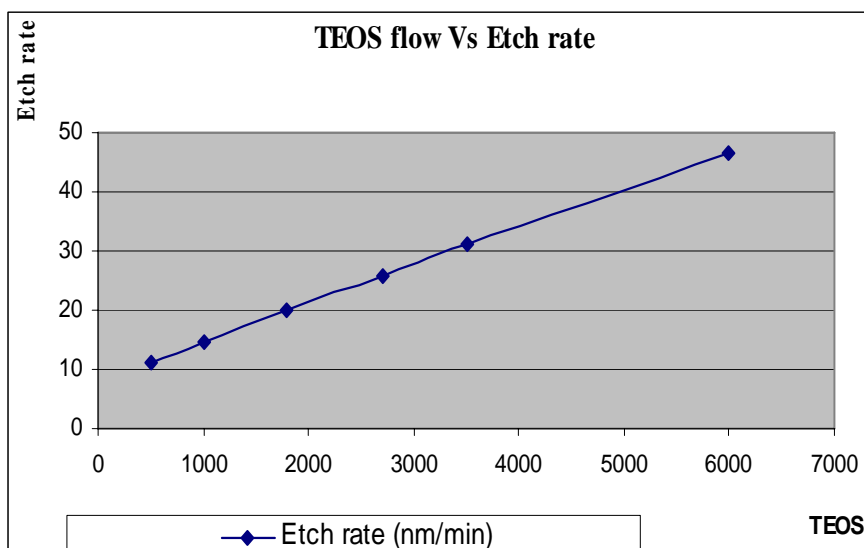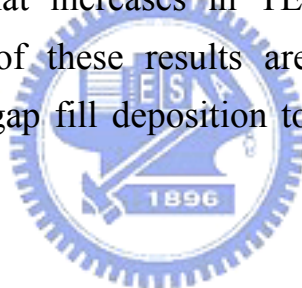Table 4.7   Wet etch rate vary TEOS flow, BOE 300:1 for 180seconds.

Figure 4.20　Wet etch rate vary TEOS trend chart

Figure 4.20 shows that increases in TEOS flow, wet etch rate also increases. The important of these results are beneficially to design both nucleation deposition and gap fill deposition to complete trench void free as well.

4.3　STI gap fill

4.3.1 Trench gap fill study by partial deposition

For STI gap filling, it is found that the void free of STI trench after steam and dry annealing, ramp up conditions of TEOS also show void-free, seamless in trenches for all splits. SEM shows that there is a very well bottom up process for high aspect ratio trench, the solution is to for the first step uses a method called "TEOS ramp" with an initial start of low TEOS on a fractional flow per seconds. The low TEOS flow starves deposition process with an O_3/TEOS ratio up to 1000mgm TEOS flow and results in a homogeneous nucleation layer and a less surface selective film growth (figures 4.21-22). The figures 4.23-24 show the gap filling after deposition 1 and 2 and it found there

is a very well STI gap fill without furnace annealing, no seam or void observed after trench gap filling process, so it can be define the initial homogeneous nucleation is extremely important for trench gap fill with bottom up deposition, TEOS ramps to 2700mgm with same ozone concentration maintaining also provides a very well trenches filling capability and no interfaces interruption.

After bi-layers gap fill monitoring, trenches filling with the whole stack film monitoring show there is seamless and voids free for the whole stack film deposition after steam annealing (figures 4.25-4.27).
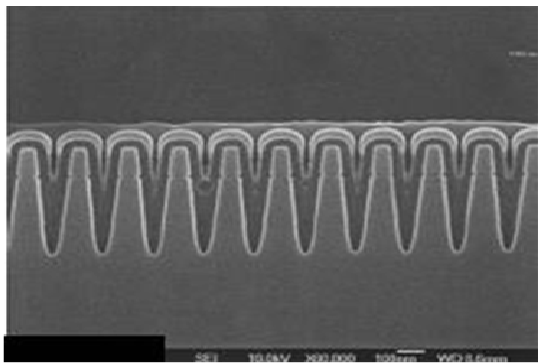

Figure 4.21 SEM shown Dep-1 for STI dense area without annealing. BOE 6:1, AR 7:1
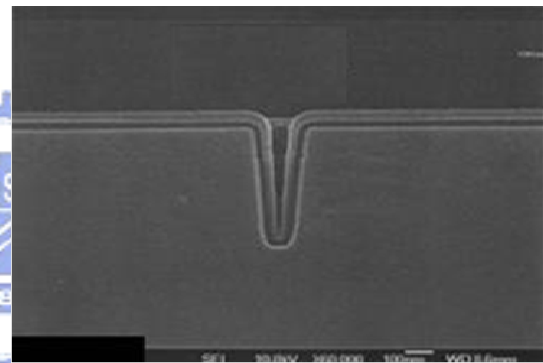
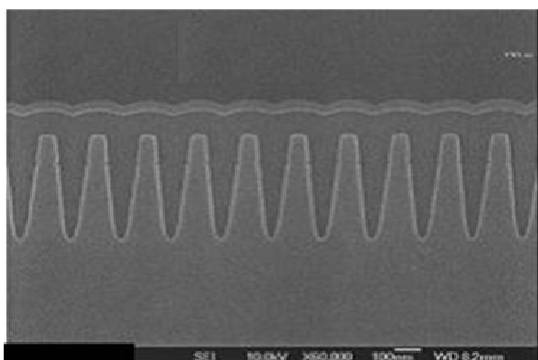Figure 4.22 SEM shown Dep-1 for STI trench area without annealing. BOE 6:1, AR 7:1

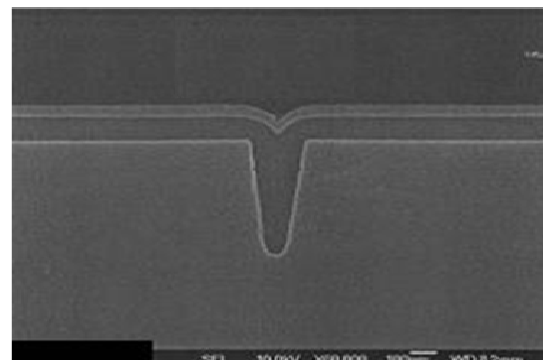Figure 4.23 SEM shown Dep1+2 for STI dense area without annealing. BOE 6:1, AR 7:1

Figure 4.24 SEM shown Dep1+2 for trench area without annealing. BOE 6:1, AR 7:1

4.3.2 STI gap fill check with three steps recipe

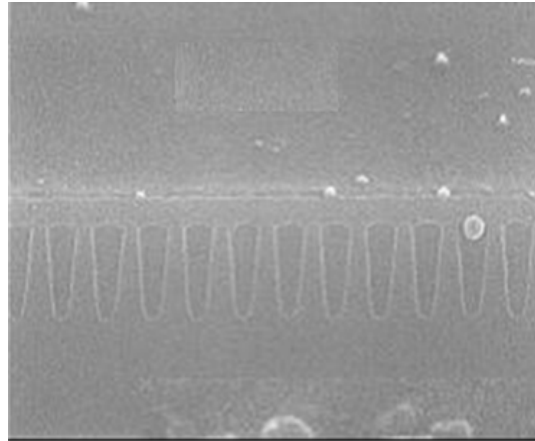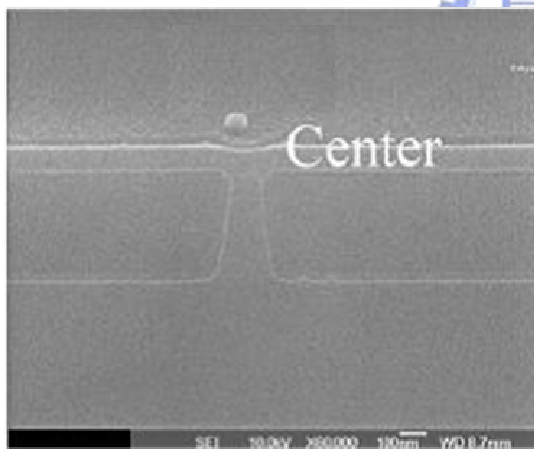Figure 4.27 SEM shown STI trench voids free in dense area after steam annealing. BOE 6:1, AR 7: 1.

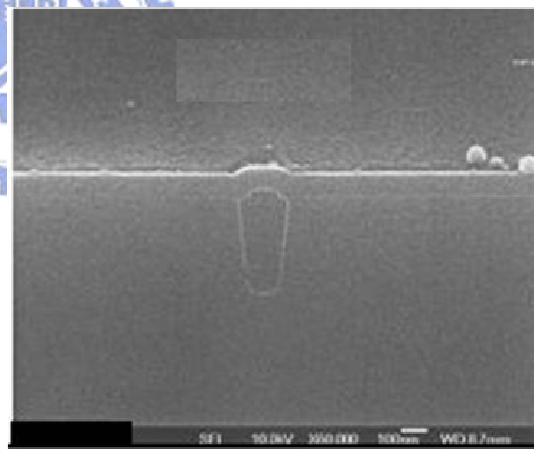Figure 4.28 SEM shown STI open area after steam annealing. BOE 6:1, AR 7: 1.

Figure 4.29 SEM shown STI voids free in trench area after steam annealing BOE 6:1, AR 7:1 .

The studies described here indicate a promising approach to improve HARP SA-USG for STI gap fill in technology of 70nm and beyond. Initial

experiments data also show that process with TEOS ramp-up during the first stage deposition can improve gap fill capability. The most important difficulty encountered during the first stage tests is how to obtain a more flexible and reliable TEOS ramp-up. Software and hardware work requests have been issued to meet the desired ramp situation.

Finally, we had some window splits for trenches filling effect on the initial TEOS flow and TEOS ramp up rate during transition process step, also, different anneal conditions will be tested to more efficiently heal the seams, of which we need to optimize annealing conditions for better understanding of the whole process and to set up the final process flow.

4.4 STI gap fill windows check

4.4.1 O_3/TEOS ratio adjustment

A number of approaches were attempted to improve gap filling (DOE_1~5), optimization of the existing process in the critical variables, and a high ozone process in which the TEOS is introduced in a varying but controlled manner (TEOS ramp). From this work, it became apparent that the initial oxide layer is very critical in achieving a good gap-fill. The high quality oxide film essential for good gap-fill needs an extremely Ozone rich environment coupled with low TEOS concentration in the gas phase. But this leads to deposition rates that are unacceptably low. At the time it was conjectured that the later layers may tolerate increasingly poorer ozone environment or conversely increasing higher TEOS concentrations in the gas phase. This leads to the development of TEOS ramp process that introduces very low amounts of TEOS in ozone rich environment to get a high quality

initial oxide layer followed by a continuous but slow increase in TEOS concentration, so that the subsequent layer is deposited faster without adversely affecting the trench filling.
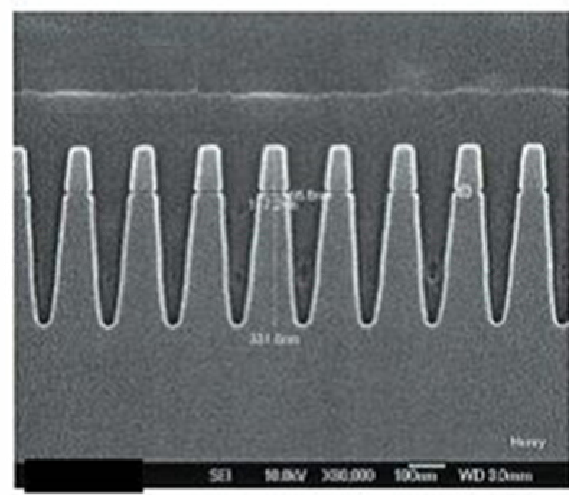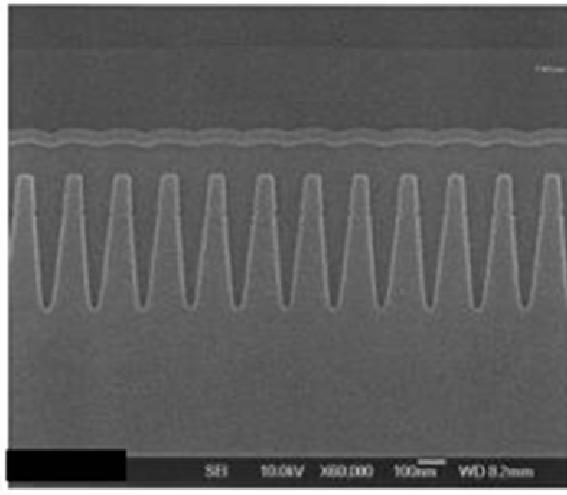

Figure 4.28 SEM shown voids free with initial low TEOS after furnace steam annealing (DOE_1-3,5)

Figure 4.29 SEM shown void initial low TEOS flow in DOE_4 after furnace steam annealing

There were some TEOS ramp rate tests with same O_3 concentration to monitor gap fill capability by using the same matrix wafers. TEOS ramp rate 5mgm/sec is the proper flow can achieve the gap filling with steam anneal, but, TEOS ramp rate at 15mgm/sec showed poor gap-fill result with thinner linear oxide of initial deposition.

For the critical structure, to achieve STI gap filling does not only need to use low TEOS ramp rate , but also to have enough liner oxide thickness to prevent bigger seam locating at the bottom of trench.

4.4.2 Anneal conditions

Steam annealing gives a very good gap fill in dense areas and very good conformality in opening area. The another challenge is reflow angle after furnace annealing, the less reflow angle means movable film is more sensitive to high temperature, the effect of steam annealing not only give a seamless and/or void free results, but also it provides a less reflow angle to beneficial on chemical mechanism polishing .
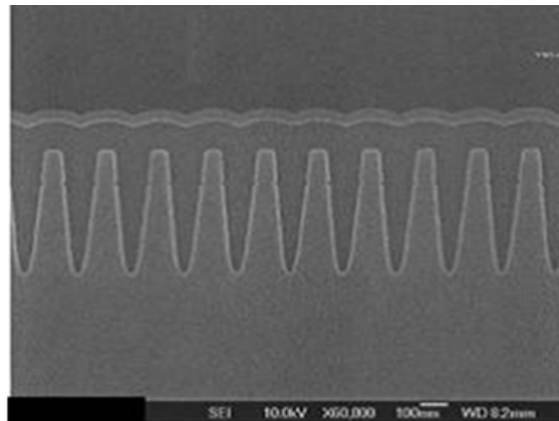

Figure 4.30 SEM shown voids free in STI dense area after steam furnace annealing. BOE 6:1, AR 7:1
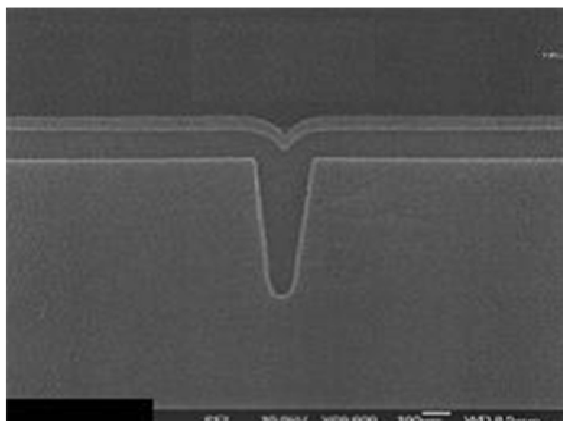

Figure 4.31 SEM shown voids free in trench after steam annealing by furnace. BOE 6:1, AR 7:1
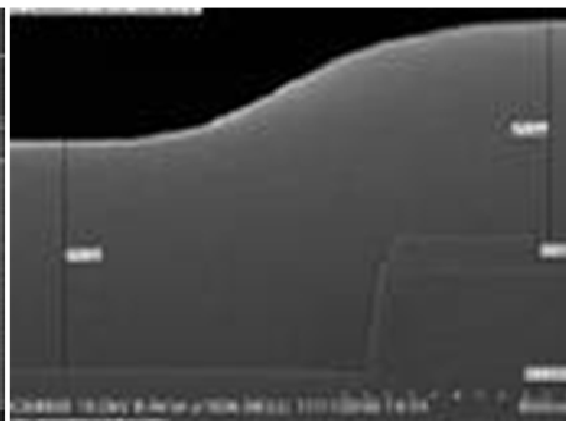
Figure 4.32 SEM shown reflow angle after HARP USG deposition after steam furnace annealing

Comparing to steam annealing, using dry furnace annealing can not get a better gap fill result as what we respected. It found that voids found in trenches whatever in dense areas or opening area, the reflow angle is also steep comparing with steam annealing. Thus, it can be concluded that dry furnace annealing is beneficial on film densification, but high temperature may prohibit significant diffusion of movable USG film.

Figure 4.33 SEM shown voids observation in STI dense area after dry furnace annealing. BOE 6:1, AR 7:1

Figure 4.34 SEM shown voids observation in trench by using dry furnace annealing only

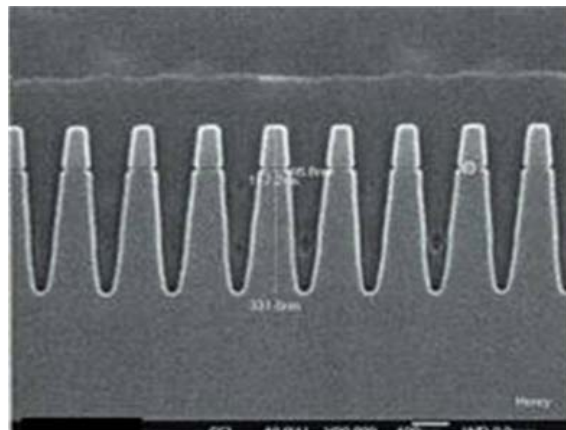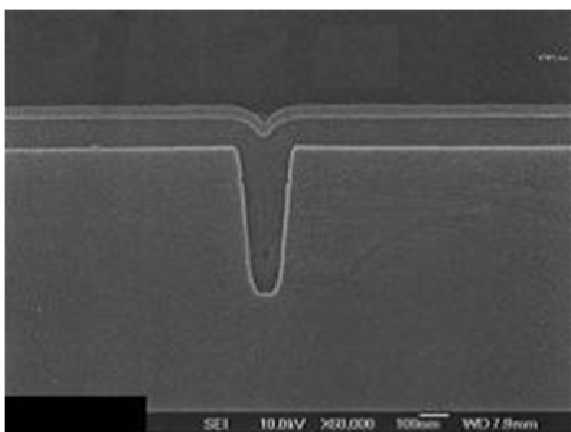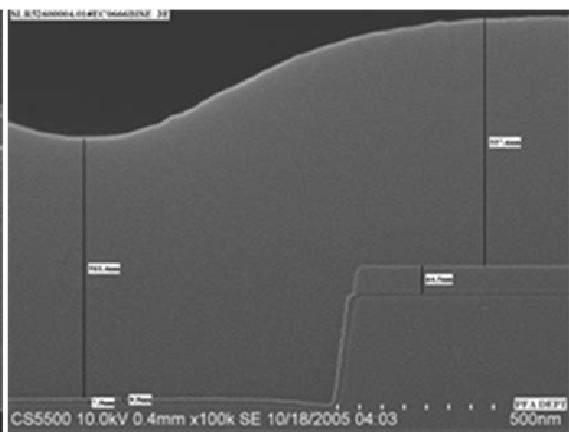Figure 4.35 SEM shown bigger reflow angle after HARP USG deposition by using dry annealing only

Furnace reflow is very important to HARP SA-USG, the experiments show that gap fill achieving is mainly by steam annealing, but dry anneal may densify the stack film to get the closely film properties likes HDPCVD film that which is beneficial on chemical mechanism polishing. For those STI structure wafers were with oxide liner, if just use high temperature of dry annealing that which causes silicon oxidation and gap filling can not be achieved as well as it could. The steam annealing by furnace results in a very well trench filling at 800^0C, there is also no measurable trench oxidation found. In order to have the compatible film density as well as HDPCVD, we approached two steps annealing to get the closely film density. The acceptably result of two steps annealing will be the finalized reflow in our test, steam reflow at 800^0C for 30 minutes and a sequent dry anneal at 1000^0C for 30minutes. The approach met the criteria of gap filling and film density as well as HDPCVD without any other side effects.

Chapter 5
CONCLUSION

From this study, we have found that the first few HARP USG layers are critical to achieve a good gap-fill. The high quality oxide film essential for good gap-fill needs an extremely ozone rich environment coupled with a low TEOS concentration in the gas phase. Even though this TEOS ramp method provides a void-free gap filling and improved seam performance, it still cannot completely eliminate this weak region for more aggressive structures, especially after the film is subjected to a mandatory high temperature anneal. A solution to this problem turns out to be in the modification of the annealing environment. Addition of the steam during anneal has shown a remarkable improvement in the healing of seams In order to meet the demand for void-free gap-fill for the 65nm generation STI using HARP process in the HARP SACVD tool, potential hardware concerns and optimization of process windows has to be properly addressed.

Finally, no plasma damage issue to the active areas and conformal films enable high aspect ratio trench is the biggest advantages of HARP SACVD process for the shallow trench isolation gap filling of advanced DRAM.

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