Chapter 1

Introduction

In recent years, wireless communications in the microwave and millimeter wave ranges play a very important role day by day in our daily life. There are many wireless system quickly involved in our life, such as GSM, CDMA, GPS and HDTV broadcast, etc. The deregulation of the communication services also results in the rapid development of many wireless communications systems for voice and data transmissions. For the increasing demand of wireless communication volume, multi-channel transmission with multiple operating frequencies to increase the transmission capacity become a common practice used for signal transmission in modern wireless communication.

But the neighboring frequencies are located closely to each other, the two signals with intermodulation distortion will be enhanced after the amplifier processed. A good linearity is a device which neighboring frequencies could locate closely to each other and produce less distortion. Therefore in the same bandwidth, a good linearity device will allow more frequencies processed and increase the communication volumes.

For noise applications at high frequencies, the devices require low noise, low distortion at low operation voltage. Compound semiconductor devices offer superior performance over Si-based counterparts especially in low noise and high power applications. Among them, GaAs high electron mobility transistors (HEMTs) offer best low noise performance over others. HEMT is a kind of field-effect transistor invented by the Japanese, Takashi Mimura [1], and has been successfully commercialized in many applications In the HEMT structure, the specific epitaxial

layers are designed to generate a band-gap discontinuity and produce two dimensional electron gas (2DEG) regions in the channel as shown in Figure.1-1. The electrons confined in the 2DEG regions result in less electron-impurity scattering and causes enhanced electron mobility, which enables HEMT to have a low noise figure meanwhile possesses high power density, high efficiency and good linearity. In the modern digital wireless communication systems, low noise HEMTs with high linearity are required.

The conventional HEMT is with AlGaAs/GaAs epitaxial structure. Because the AlGaAs layer is easy to be oxidized and has large surface recombination current, it is desired to use other materials to replace the AlGaAs layer for the Schottky layer. In this study, InGaP was used as the Schottky layer. The InGaP gated HEMT has several advantages over the AlGaAs gated HEMT, which make the InGaP gated structure more suitable for microwave applications. First, wider InGaP energy gap resulted in a higher device gate-to-drain breakdown voltage. Second, InGaP has higher valence band discontinuity, good thermal stability, low surface recombination current, and no deep-complex center (DX center). Third, there has excellent etching selectivity between InGaP and GaAs, which is beneficial to develop stable and high performance device processes [2].

In recent years, many works on HEMT device linearity improvement were reported. These include analysis of device linearity by nonlinearity circuit [3-4], and improvement of device linearity using double-heterojunction [5], doped-channel [6] and different device structure designs [7]. In this study, we investigate the device linearity improvement for the low noise GaAs HEMT using device layer structure and doping profile modifications.

Based on the fact that device gain compression is caused mainly by the cubic term of the Taylor expansion. The third-order intermodulation distortion (IM3) and

the third-order intercept point (IP3) are the important specifications for the device linearity. Drain-Source current model and a simple device equivalent circuit were used for device linearity analysis and the derivation of the relationships between IM3 and IP3 with the two current sources, Gm (V_{GS}) and Gds (V_{DS}) , are described in Chapter 2. To further investigate the linearity performance of the devices, polynomial curve fitting technique was applied to the transfer characteristic functions of these devices. According to the linearity analysis, two types of device structures were proposed with flat Gm distribution for device linearity improvement in this thesis. They are channel doped InGaP HEMT and Schottky layer doped InGaP HEMT.

The details of the pseudomorphic high electron mobility transistor (PHEMT) structure and processes are described in Chapter 3. After device fabricated, device measured method was describe in chapter 4. And we will show the result in DC & RF in chapter 5. Finally, the work on device linearity improvements in this thesis is summarized in Chapter 6 as the conclusions.
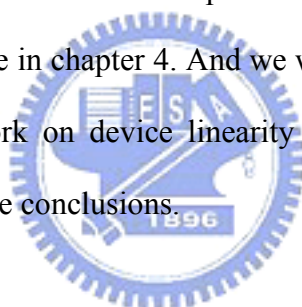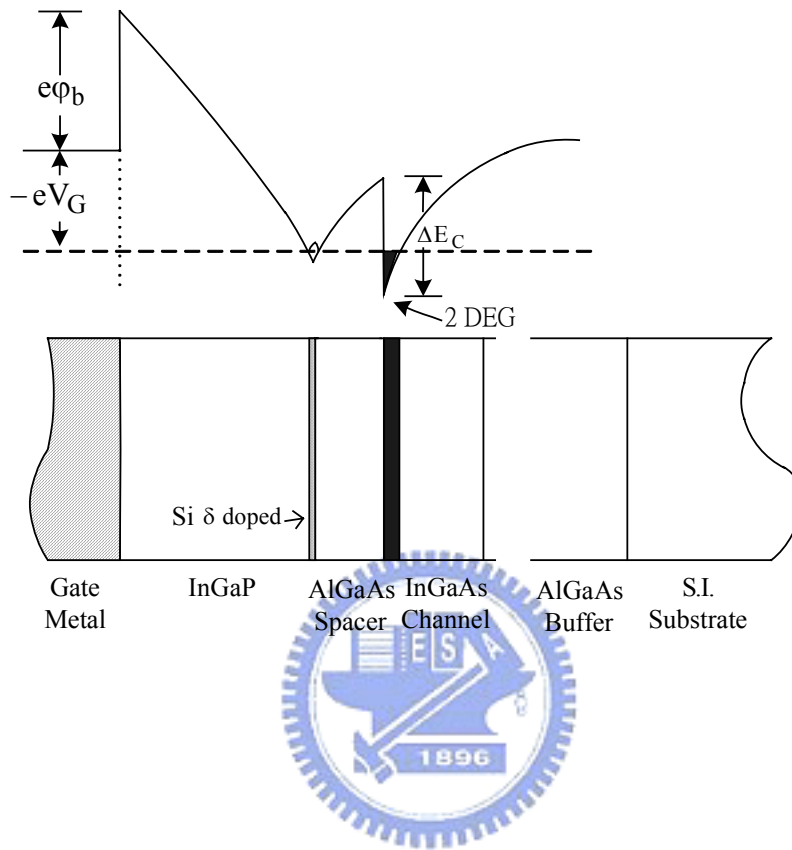
Figure 1-1 The band diagram of the InGaP PHEMT.

Chapter 2

Device Linearity Analysis for improvement

2.1 Introduction

For wireless communication system, the signal was transmitted and received by the transceiver. In ideal linear and noiseless situation, transmitted signal can be recovered at the receiver. However, in real transceivers, nonlinear devices generate nonlinear distortion.

In this chapter we will show the linearity key index IM3 &IP3 & its relationship with device transconductance Gm. After we deviate their relationships, we can find the ways to improve the device linearity.
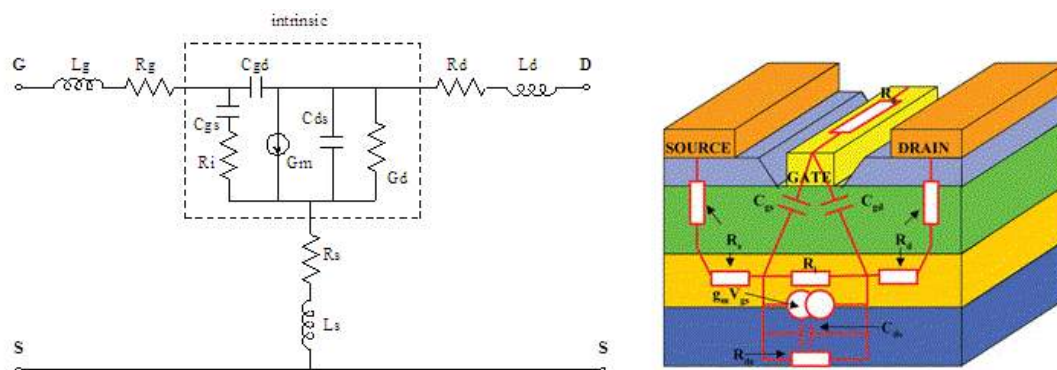
2.2 Device model

Figure 2-1 HEMTs structure and its equivalent circuit model

Figure 2-1 shows a schematic cross-section of a typical HEMT structure (right side) and its simple device equivalent circuit model (left side). The non-linearity circuit elements in this model are Schottky barrier junction capacitance at the gate (C_{gs}), the gate to drain capacitance (C_{gd}), the intrinsic transcnductance (G_m), and the drain conductance (G_d). Among them, C_{gs} and G_m are dependence on the input voltage (Vi), while Gd is dependence on the output voltage (Vo)[8].

PHEMT developed is characterized using on-wafer probing and the bias-dependent S-parameters are measured and followed by equivalent circuit parameter extraction. The small-signal equivalent circuit used for parameter extraction also requires "cold measurement" (V_{ds}=0). As shown in Figure 2-1, the symbols for the device parameters could be explained as following.

(a) C_{gs} : the capacitance between gate and source has the expression.

$$C_{gs} = C_{gsi} + C_{gsf}$$

where C_{gsi} is an intrinsic component, which for a given L_g (the inductance of the gate metal) is proportional to $1/D_g$ (gate-to-channel distance), and C_{gsf} is a fringing capacitance, which is an additional parasitic capacitance. C_{gs} is expected to be proportional to $1/D_g$ and increases with recess depth. The magnitude of C_{gsf} is relatively small compared to the intrinsic C_{gsi} value [9].

(b) C_{gd} : the capacitance between gate and drain is given as :

$$C_{gd} = C_{gd,dep} + C_{gd,met} = C_{gdi} + C_{gdair} + C_{gdsc}$$

$C_{gd,met}$ is the feedback capacitance due to the gate-drain metallization depending on the gate-to-drain distance. $C_{gd,dep}$ is the feedback capacitance due to the gate-drain depletion [10].

In another expression, C_{gd} is a parasitic capacitance between gate and drain, and it consists of three terms: C_{gdi} (the capacitance of the gate-drain surface depletion

region), C_{gdair} (a weak contribution through the air), and C_{gdsc} (an intrinsic component due to the short channel effect). By a deeper recess, C_{gdi} and C_{gdair} decrease due to lateral extension of the recess notch. C_{gdsc}, on the other hand, increases due to the reduced short channel effect. Since the later effect is important for shallow recess, the overall C_{gd} characteristics show first a slow rate of decrease in capacitance with recess and later on a much faster rate of decrease, and the ratio of C_{gs} and C_{gd} increases with deeper recess [9].

(c) R_i：the series resistance between gate and drain

(d) G_d：the conductance between drain and source

(e) C_{ds}：the capacitance between source and drain

(f) L_g：the inductance of the gate metal

(g) R_g：the resistance of the gate

(h) G_m：transconductance

(i) R_s：the resistance of the sum of gate-source intervening material and the ohmic contact of the source electrode.

(j) L_s：the inductance of the sum of gate-source intervening material and the ohmic contact of the source electrode.

(k) R_d：the resistance of the sum of gate-drain intervening material and the ohmic contact of the drain electrode.

(l)L_d：the inductance of the sum of gate-drain intervening material and the ohmic contact of the drain electrode.

2.3 The nonlinear effects of device

2.3.1 Gain compression

We observed device nonlinear phenomena with a single frequency input as shown in equation (2.1):

$$v_i = A\cos\omega t \tag{2.1}$$

The nonlinear voltage gain of devices may be approximated by the polynomial expansion as equation (2.2):

$$v_o = k_1 v_i + k_2 v_i^2 + k_3 v_i^3 \tag{2.2}$$

To substitute equation (2.1) into (2.2), many of the nonlinearities may be observed.

$$v_o = 0.5A^2 k_2 + \left(k_1 A + 0.75 k_3 A^3\right)\cos\omega_1 t + 0.5 k_2 A^2 \cos 2\omega_1 t \\ + 0.25 k_3 \cos 3\omega_1 t + .. \tag{2.3}$$

Equation (2.3) shows one collects the terms of the series expansion, the nonlinear phenomena of output include a shift in the DC level ($0.5A^2 k_2$), gain compression ($k_1 A + 0.75 k_3 A^3$) and harmonics. The gain compression with increasing signal level is due to the cubic term which has to be negative to account for gain compression, and not gain expansion. The second harmonic is caused by the square term, k_2 and the third harmonics are caused by the cubic term, k_3.

2.3.2 Analysis of IM3 and IP3

In modern wireless communication system, multi-channel transmission is a common practice used for signal transmission. The transmission bandwidth of communication system was divided into multiple information bandwidths and used multiple operating frequencies for data transmission to increase the transmission capacity. Nevertheless, when the operating frequencies of the system are more than two and the neighboring frequencies are located closely to each other, the device used in such system will generate intermodulation distortion.

For the intermodulation distortion analysis, two-tone signal which consists of two signals with the same amplitude *A* at two different but closely located frequencies is applied as the input. Substitution of the two-tone input signal as shown in equation

(2.4) into equation (2.2), the output voltage is as shown in equation (2.5).

$$v_i = A\cos\omega_1 t + A\cos\omega_2 t \tag{2.4}$$

$$\begin{aligned}
v_o &= k_1 A^2 \cos(\omega_1 - \omega_2)t + \left(k_1 A + 2.25 k_3 A^3\right)\cos\omega_1 t + \left(k_1 A + 2.25 k_3 A^3\right)\cos\omega_2 t \\
&+ 0.75 k_3 A^3 \cos(2\omega_1 - \omega_2)t + 0.75 k_3 A^3 \cos(2\omega_2 - \omega_1)t \\
&+ k_2 A^2 \cos(\omega_1 + \omega_2) + 0.5 k_2 A^2 \cos 2\omega_1 t + 0.5 k_2 A^2 \cos 2\omega_2 t \\
&+ 0.75 k_3 A^3 \cos(2\omega_1 + \omega_2)t + 0.75 k_3 A^3 \cos(2\omega_2 + \omega_1)t \\
&+ 0.25 k_3 \cos 3\omega_1 t + 0.25 k_3 A^3 \cos 3\omega_2 t + ..
\end{aligned} \tag{2.5}$$

Among all the intermodulation distortions incurred by the devices, because of gain compression is caused mainly by the cubic tear, third-order intermodulation distortion (IM3) and the third-order intercept point (IP3) will dominant and determine the device linearity. Therefore, IM3 and IP3 have become the important figure of merit for the devices used for modern wireless communication applications. In this chapter, IM3 and IP3 were as the device linearity specification and derivative the relationships between IM3 and IP3 with two current source parameter Gm (V_{GS}) and Gds (V_{DS}).

The IM3 level at frequencies $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ are as equation (2.6) [12]:

$$v_{o(IM3)} = 0.75 k_3 A^3 \cos(2\omega_1 - \omega_2)t + 0.75 k_3 A^3 \cos(2\omega_2 - \omega_1)t \tag{2.6}$$

An illustration of the output power spectrum is shown in Figure.2-2.

For device linearity improvement, a simple device equivalent circuit as shown in Figure. 2-1 was used to derivate the relationship between IM3, IP3 and Gm. The nonlinear circuit elements involved in this model are the Schottky-barrier junction capacitance at the gate (C_{gs}), the gate to drain capacitance (C_{gd}), the intrinsic transconductance (g_m) and the drain conductance (G_d). Among them, C_{gs} and g_m are dependent on the input voltage (V_i), and Gd is dependent on the output voltage (V_o) [13]. Analysis and estimation of the IM3 level and IP3 incurred by the device itself begin with the derivation of the nonlinear transfer function of the two-port network

using classical theory [12]. In such case, the device may be classified as near-linear two-port system with a relatively small amount of nonlinearity. The two-port's voltage gain may then be approximated by the polynomial expansion as: (2.2):

Applying Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL) at specific nodes of the network, the nonlinear voltage transfer function can be derived:

$$v_o = \left[\frac{j\omega C_{gd}}{G_d} - \frac{g_m}{G_d}\right] \cdot \left[1 + \frac{j\omega C_{gd}}{G_d}\right]^{-1} v_i \tag{2.7}$$

Considering the first order significant terms for simplicity of analysis, the coefficients in equation (2.7) can be expressed explicitly as $k_1 = -g_m/G_d$, $k_2 = -g_m'/G_d$ and $k_3 = -(1/2)g_m''/G_d$ where g_m' and g_m'' are the first and second derivatives of the intrinsic transconductance, respectively.

$$IM3 = \frac{\left(\frac{3}{4}k_3 A^3\right)^2}{2R_L} = \left(\frac{3}{4\sqrt{2}}\right)^2 \cdot \frac{k_3^2 A^6}{R_L} = \left(\frac{3}{8\sqrt{2}}\right)^2 \frac{\left(g_m''\right)^2}{G_{ds}^2 \cdot R_L} \cdot A^6 \tag{2.8}$$

Using IP3 definition (linear part is equal to the third-order intermodulation distortion) to obtain A as shown in equation (2.9), the device IP3 can be obtained as equation (2.10).

$$k_1 A = \frac{3}{4}k_3 A^3 \tag{2.9}$$

$$IP3 = \frac{k_1^2 A^2}{2R_L} = \frac{4}{3}\frac{g_m^3}{g_m'' \cdot G_{ds}^2 \cdot R_L} \tag{2.10}$$

In the linear equivalent circuit, a drain-source current model can be used for IM3 and IP3 estimated as equation (2.11) [14, 15].

$$i_{ds}\left(v_{gs}, v_{ds}\right) = \frac{\partial I_{DS}}{\partial V_{GS}} \cdot v_{gs} + \frac{\partial I_{DS}}{\partial V_{DS}} \cdot v_{ds} \tag{2.11}$$

Where v_{gs} and v_{ds} are the incremental gate and drain voltages, respectively. i_{ds} is linear terms of drain to source current. The nonlinear drain to source current is controlled by

two voltages as shown in equation (2.12).

$$I_{DS}(V_{GS},V_{DS}) = a_0 + a_1V_{GS} + a_2V_{GS}^2 + a_3V_{GS}^3 + a_4V_{GS}^4 + a_5V_{GS}^5 + ...$$
$$+ b_0 + b_1V_{DS} + b_2V_{DS}^2 + b_3V_{DS}^3 + b_4V_{DS}^4 + b_5V_{DS}^5 \qquad (2.12)$$

The small-signal drain to source current can be modeled by means of a pair of separate elements Gm and conductance (Gds) shown in equation (2.13) and (2.14).

$$G_m(V_{GS}) = \frac{\partial I_{DS}(V_{GS},V_{DS})}{\partial V_{GS}} = a_1 + 2a_2V_{GS} + 3a_3V_{GS}^2 + 4a_4V_{GS}^3 + 5a_5V_{GS}^4 + .. \quad (2.13)$$

$$G_{ds}(V_{DS}) = \frac{\partial I_{DS}(V_{GS},V_{DS})}{\partial V_{DS}} = b_1 + 2b_2V_{DS} + 3b_3V_{DS}^2 + 4b_4V_{DS}^3 + 5b_5V_{DS}^4 + .. \quad (2.14)$$

Hence, the relationship between IM3, IP3 and Gm, Gds are shown in equation (2.15) and (2.16).

$$IM3 \propto \frac{\left(G_m''\right)^2}{G_{ds}^2 \cdot R_L} \cdot A^6 \qquad (2.15)$$

$$IP3 \propto \frac{\left(G_m\right)^3}{G_m'' \cdot G_{ds}^2 \cdot R_L} \qquad (2.16)$$

As a result, the IM3 is direct proportion to the second derivatives of the extrinsic transconductance (Gm″). The IP3 is an inverse proportion to Gm″ and direct proportion to third power of Gm. For this reason, the lower IM3 can be achieved by improving the Gm distribution flatness across the gate bias region. Meanwhile, higher Gm with flat Gm distribution also will result in higher IP3. In this paper, the extra doping either in the Schottky layer or in the channel layer was used to modify the drain-source current (I$_{DS}$) profile and to improve the Gm distribution flatness to improve device linearity.

2.4 Transconductance (Gm)

The transconductance of the HEMTs indicates the ability of the gate voltage on the control of the drain current. It can be defined as：

$$G_m = \frac{dI_D}{dV_G} = \frac{\varepsilon_2}{d_2}Z_G v_{sat}$$

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where the v_{sat} is the electron velocity of the "two dimensional electron gas" (2-DEG).

The measurement requires specification of the initial gate voltage, the gate voltage step, and the drain voltage at which the measurement is made. Because of the nonlinear behavior of source-drain current as a function of gate voltage, g_m typically will become less as the bias approaches pinch-off approaches. This also means that a smaller voltage step will yield a higher transconductance. The extrinsic transconductance is a function of the total gate width of the device, so the width must also be given. Besides, g_m may also be normalized to a unit gate width, usually mmho/mm.

2.5 Polynomial curve fitting technique

To further investigate the linearity performance of the three devices, polynomial curve fitting technique was applied to the transfer characteristic functions of these devices. The equation (2.12) was changed to I_{DS}-V_{GS} curves that were expressed in terms of a high order polynomial as equation (2.17):

$$I_{DS}(V_{GS}) = A_0 + a_1 V_{GS} + a_2 V_{GS}{}^2 + a_3 V_{GS}{}^3 + a_4 V_{GS}{}^4 + a_5 V_{GS}{}^5 + ... \qquad (2.17)$$

Moreover, the IM3 levels incurred by the device can then be readily derived as [16, 17]:

$$IM3 = \frac{3}{8} a_3 A^3 + \frac{50}{32} a_5 A^5 \qquad (2.18)$$

For a device with good linearity, I_{DS} should increase linearly with V_{GS}, therefore, a_1 should be larger and the higher order constants a_3 and a_5 should be minimized [17].
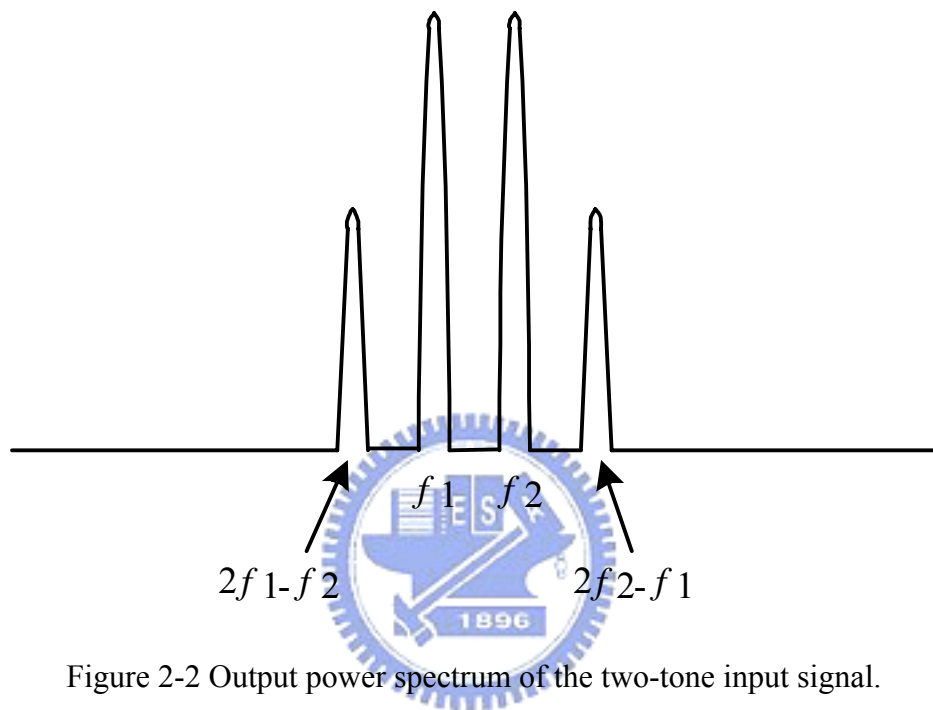
Figure 2-2 Output power spectrum of the two-tone input signal.

Chapter 3

Device structure & PMEMT Experimental

The fabrication process flow of the InGaP PHEMT is shown in Figure 3-1. The standard process includes wafer cleaning, device isolation, ohmic contact formation, gate formation, device passivation, contact via formation, air-bridge plating, wafer lapping, backside via-hole etching, backside grounded metallization, and die sawing. In this study, we use InGaP/InGaAs/GaAs epitaxial structure to fabricate the low noise PHEMTs. The DC and RF measurements are also performed to characterize the device performance. In the following section, the detailed fabrication process of the InGaP PHEMT devices will be described.
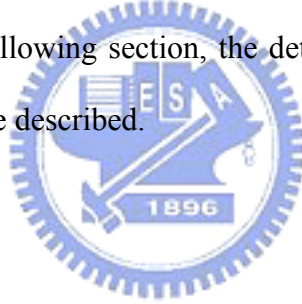
3-1 Device structure

In this study, we use molecular beam epitaxy (MBE) to grow the epitaxial structure on the GaAs substrate. Because of the MBE can precisely control the epitaxy thickness and quality, better heterojunction interface can be obtained. The reference conventional delta doped device structure in this study is shown in Figure 3-2(a).

As Figure 3-2(a) shows, the first layer is n^+-GaAs layer with a high doping concentration. Its main purpose is to form good ohmic contact with drain and source electrodes. The second layer is the InGaP Schottky layer. This layer is used to control the device current by changing the recess depth, and gate metal is also grown above it. Because InGaP has wider band-gap, the devices will have higher breakdown voltage. The third layer is the Si δ-doped layer. This layer is the electron-providing layer. In this study we use double δ-doped structure to create two electron-conducting

channels. This can increase power density and output power by the increase of the number of conducting electrons. The fourth layer is the undoped InGaP layer. It is used as a "spacer" layer to prevent the electrons in the channel region to be scattered by the dopant ions in the electron-providing layer. The fifth layer is the InGaAs channel layer. InGaAs has higher electron mobility than GaAs, and the devices with InGaAs channel layer will have higher electron speed and higher operation frequency. Besides, there is a band-gap difference between InGaP and InGaAs, which will form the heterojunction interface with a quantum-well structure. The band diagram of the InGaP HEMT is shown in Figure 1-1, "2-DEG" will form at the InGaP/InGaAs junction interface. This can decrease electron scattering phenomenon and increase the electron mobility. Then the AlGaAs/GaAs "superlattice" layer is used to reduce the leakage current from the substrate. Finally, there is the undoped "buffer" layer. This layer is used to increase the isolation between channel layer and substrate. It can prevent the impurity atoms in the substrate from diffusing to the channel and affecting the electron movement in the conduction layer.

For linearity improvement to occurred, light doping in Schottkey layer and in the channel layer were used to improved the flatness of Gm as a function of gate-bias condition. The other compared device is in Figure 3-1 (b) with channel doped with Si concentration of 5×10^{17} cm^{-3} & 1×10^{18} cm^{-3}. And another 2 are no δ-doped structure in Schottky layer but instead of Schottky layer with uniform Si concentration of 2×10^{18} cm^{-3} (top)2×10^{18} (bottom)cm^{-3} (Figure3-1 (c)) & 3×10^{18} cm^{-3} (top)2×10^{18} (bottom)cm^{-3} (Figure 3-1 (d)) .

The device layout we used is finger-type style, which can effectively reduce the device area and largely increase the device density on the wafer. This enables us to fabricate more than ten thousand HEMT devices in a three-inch wafer. The device gate length is 0.5 μm, gate width is from 160 μm to 500 μm, and the source-to-drain

spacings is either 3 μ m or 4 μ m in this wafer. Totally there are ten different types of device layout with different gate width and source-to-drain spacing.

3.2 Introduction of PHEMT process

The PHEMT process includes five major steps. They are: device active region definition, Ohmic metal deposition and annealing, gate formation by wet chemical recess and electron beam (EB) lithography, device passivation and air-bridge formation.

3.2.1 Device active region definition (mesa)

Device active region definition is the area which to restrict the electrically conductive part of the wafer to specific parts of its surface area so that electrical current is restricted from flowing to other active areas. GaAs has a major advantage over silicon with respect to device isolation: GaAs substrates can be made semi-insulation, and which are, generally speaking, insulation. The electrically conductive portion is also called the "active region" of the wafer. The purposes of the active region definition include the active region formation, device isolation, reduction of parasitic capacitance, parasitic resistance, leakage current, and back-gating effect. It provides sufficient insulating area for device.

The mesa etch defines the source-drain area. Without mesa area, some portion of the current were to flow without passing under the gate control, the current would represent a parasitic resistance, which would degrade the RF performance of the device.

Further, after the mesa etching, the active region forms a stage above non-active region, and then gate pad region will deplet on non-active region. This structure also reduces the parasitic capacitance below gate pad area.

We defined the device active region by photolithography. In the CSD lab, we use ABM (Figure 3-3) for the mesa photo definition. Then the wafer was mesa etched by using HCl/H$_2$O (1:1) solution for the InGaP layer [11] and HF/H$_2$O$_2$/H$_2$O (2:3:10) solution for other layers. After mesa etching ,we checked the mesa pattern under microscope as in Figure 3-4 and measured etch step high under α-step .

3.2.2 Ohmic metal deposition and annealing

An ohmic contact means to form the contact between a metal and a semiconductor to allow carriers to flow in and out of the semiconductor, and an ideal ohmic contact must have no effect on device performance, i.e., it must be capable of delivering the required current and without voltage drop between the semiconductor and the metal.

In real condition, therefore, an ohmic contact must have a contact resistance that is as small as possible, to make the resistance negligible in comparison to the bulk or spreading resistance of the semiconductor.

The device Ohmic contact was formed by Ohmic metal deposition and annealing. Lower contact resistance results in lower device noise and lower power consumption for the device. Therefore, a heavily doped region was used near the metal-semiconductor interface to obtain a low resistance Ohmic contact.

We used Au/Ge/Ni/Au as the ohmic metal with total thickness of 4100Å in the ohmic contact formation of our MHEMT process. The Au/Ge alloy is the most commonly used because it forms low contact resistance and has good reliability. For the ohmic metal layer, the germanium (Ge) was used for doping the GaAs and the nickel (Ni) was act as a wetting agent and prevented the AuGe metal from "balling up" during alloy.

For the ohmic contact formation, first, the ohmic contact was defined by deep

UV photolithography with undercut profile. Then O_2 plasma descum was used to remove the residual photo-resist on the open windows. We also dip samples in 10% HCl solution for 1 minute to remove oxide from the surface before depositing the ohmic metal. Finally, e-gun evaporation system was used to deposit Au/Ge/Ni/Au metal. The ACE was used for device lift-off procedure, then the wafer was thermally alloyed by using rapid thermal anneal system (RTA) at 310℃ for 30 seconds. Final check the ohmic contact pattern with microscope image as show in Figure 3-5.

3.2.3 Recess and gate formation

Because dry etching generates ion-bombardment damage on the surface and affect the device performance, in here, the wet chemical etching process was used for the device gate recess. In order to further increase gate-to-drain breakdown voltage, the double gate recess also was processed. The 1st recess slot was defined by e-beam photolithography to form the photo-resist layer. The gate process include wet chemical recess and electron beam (EB) lithography. The size and position of the gate is critical to HEMT performance for high frequency operation. Therefore, most power HEMTs use a recessed gate geometry in which the gate stripe is placed in an etched slot for the device performance improvement. The gate recess process has two advantages. One is that the gate is placed below the surface depletion layer of the surrounding material, preventing surface depletion from restricting current under forward gate bias, and the other one is the gate recess will reduce channel thickness and source-to-drain saturation current. Consequently, it can be used to increase device breakdown voltage, and decreased source-to-gate and gate-to-drain parasitic resistances. Because GaAs HEMTs are very sensitive to surface states in the gate area, therefore, after device gate metal deposition and lift-off process, a PECVD silicon

nitride film was deposited to protect the devices from environmental contamination and mechanical damages.

The gate recess was performed using a highly selective citric acid/H_2O_2/H_2O solution to selectively remove the GaAs cap material and HCl/H_2O solution was used for the etching of the InGaP Schottky layer until it reachd the target current. The target current is a critical parameter in HEMTs performance. So we measure the drain-to-source current during the recess process to control the target current by curve tracer.

After removing the 1st recess photo-resist, the gate openings were defined by e-beam lithography to form the dual photo-resist layers with T-shaped profile. The succinic acid/H_2O_2/H_2O solution was also used to execute the 2nd recess. The 2nd recess can further increase the breakdown voltage.

Before the gate metal deposition, the sample was dipped in the 20% HCl solution for 15 seconds to remove the native oxide from the surface. And that gate metal was deposited by e-gun evaporation system. The gate metal used is Ti/Pt/Au=1000/1000/3000Å. Titanium provides good adhesion to substrate, platinum provides a barrier to prevent Au diffusing into GaAs, and Au provides high electrical conductivity. Finally the wafer was immersed into ACE to lift-off the undesired metal.

As a result, T-shaped gate has a large cross-section area at the top of the gate, and a short gate length in contact with the wafer. T-shaped gate (Figure.3-6) can reduce the gate resistance and capacitance. As the gate length is reduced, the gate resistance will obviously increase because of the reduction of gate cross-section area.

To fabricate the T-shaped gate, the dual photo-resist layers had was used. They consists of poly methyl methacrylate (PMMA) as the bottom layer, and copolymer P(MMA-MAA) as the top layer. Because of the sensitivity of copolymer is higher than that of PMMA, we can get a T-shaped profile.

3.3.4 Device passivation

For device passovation, the silicon nitride film was formed by PECVD. Silicon nitride is less permeable to ions than silicon dioxide, and therefore makes it the superior encapsulant. The wafer was first dipped in the solution of $NH_4OH:H_2O=1:50$ for 10 seconds to clean the surface and decrease the surface dangling bonds. The silicon nitride film was grown at 250℃. RF power was 35W, and the precursors were SiH_4/Ar, NH_3, and N_2. The film thickness was about 1000Å and its refractive index was about 2.0, which were measured by ellipsometer.

The thickness of the silicon nitride film represents a trade-off between conflicting requirements. If the nitride film is too thin, the number of pinholes will be large and has less mechanical strength. If the nitride film is too thick, the parasitic capacitance will increase.

After the passivation process, the contact via was defined for interconnections. Then the silicon nitride film was etched by reactive ion etching (RIE) system. The reactive plasmas are CF_4 and O_2, the RF power is 80W, and the pressure is 60 mtorr.

3.3.5 Air-bridge plating

Finally, plated air-bridges were used for the GaAs device interconnects. The air-bridge structure provides several advantages:lower parasitic capacitance, immunity to edge profile problems and the ability to carry substantial current. The fabrication process flow of the HEMT is shown in Figure.3-1.The major steps of air-bridge formation are shown in Figure.3-7. The plated metal on the GaAs devices is usually Au. Au has many superior properties as compared to other metals. Au plated interconnect, which has high electrical conductivity, is easily soldered or welded, and is resistant to oxidation and most acids, and is ductile. But gold has poor adhesion on

the wafer surface, we have to deposit thin titanium layer firstly to improve the adhesion. The detailed air-bridge process flow is described as following.

First, a layer of photo-resist was spun and patterned to open areas over metal pads. Then, a thin coating of Ti/Au/Ti=300/500/300Å was applied to the entire wafer. The thin metal layer can conduct the plating current to the whole wafer. Next, a second coating of photo-resist was applied and patterned. Then the wafer was electroplated with Au for $2\,\mu$m thickness. After plating, the top resist layer, thin Ti/Au/Ti metal, and lower resist layer were removed individually, leaving only the plated airbridge.

After the air-bridge plating, the front-side process of MHEMT is completed, and the RF characteristics of the devices can be measured. The image of the finished 0.25x160-μm^2 device is shown in Figure. 3-8. It use multi-finger type and has a drain to source spacing of $2\,\mu$m.

(a)

GaAs		GaAs
InGP	Schottky	
AlGaAs	Spacer	
InGaAs	Channel	
AlGaAs	Spacer	

(b)
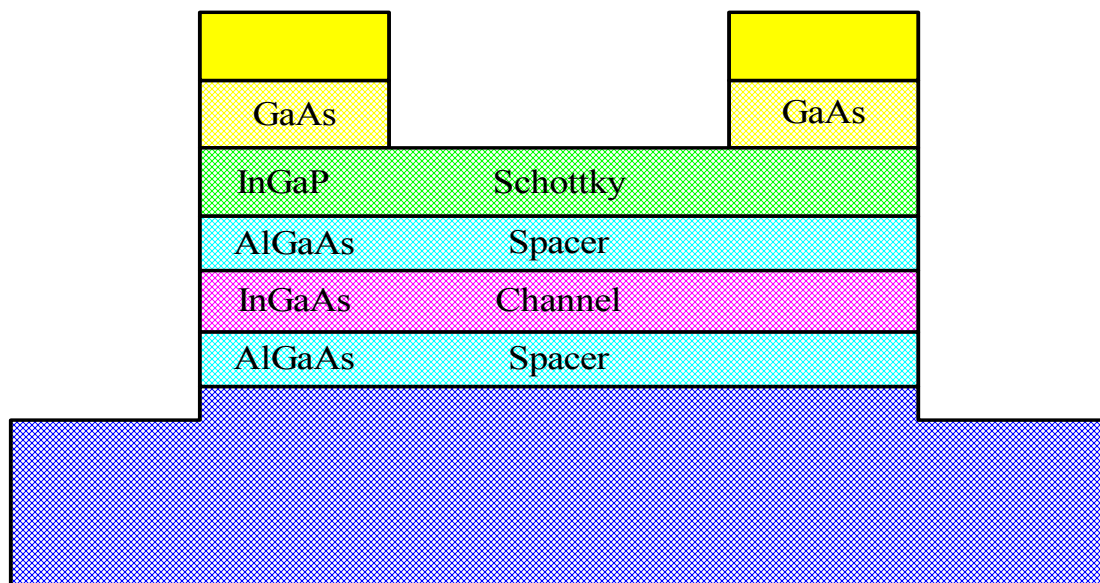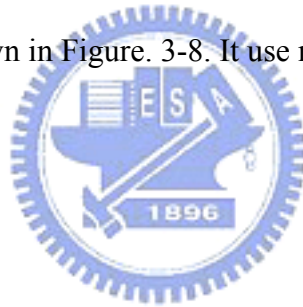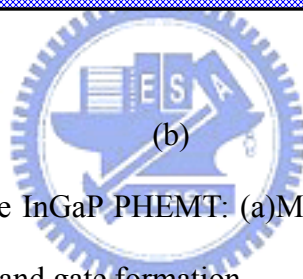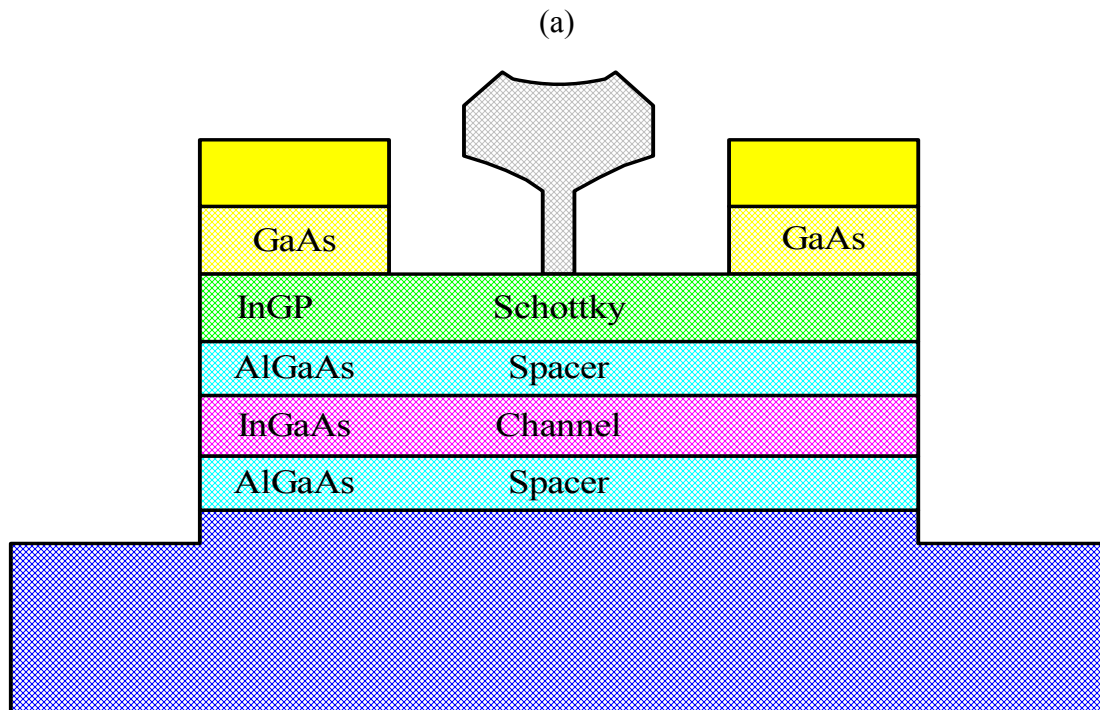
Figure 3-1 Process flow of the InGaP PHEMT: (a)Mesa isolation and ohmic contact

formation, and (b) gate recess and gate formation.

GaAs		GaAs
InGaP	Schottky	
AlGaAs	Spacer	
InGaAs	Channel	
AlGaAs	Spacer	
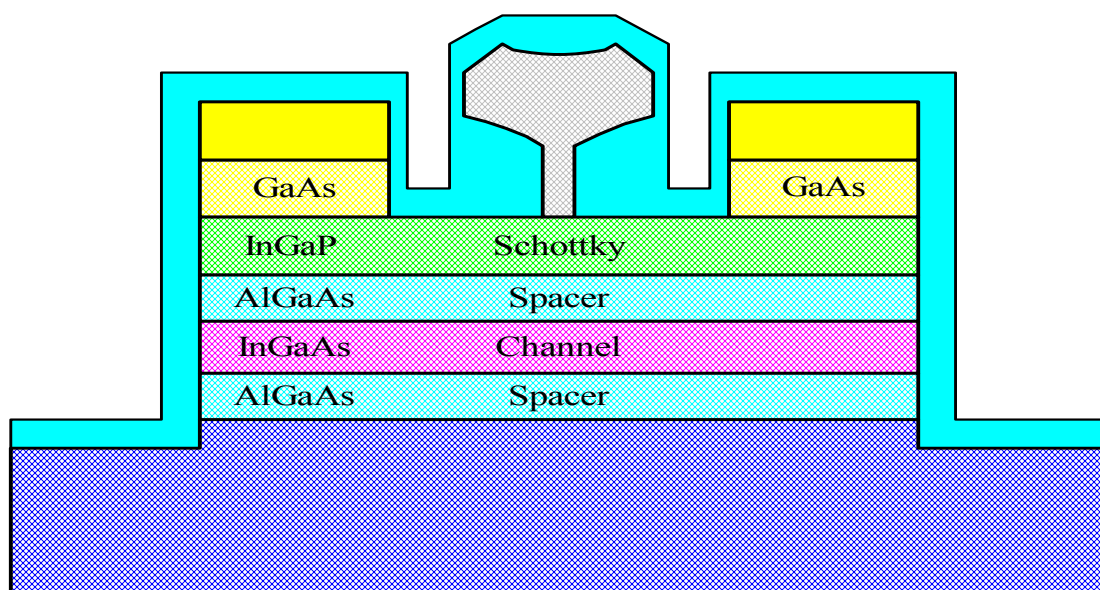
(c)
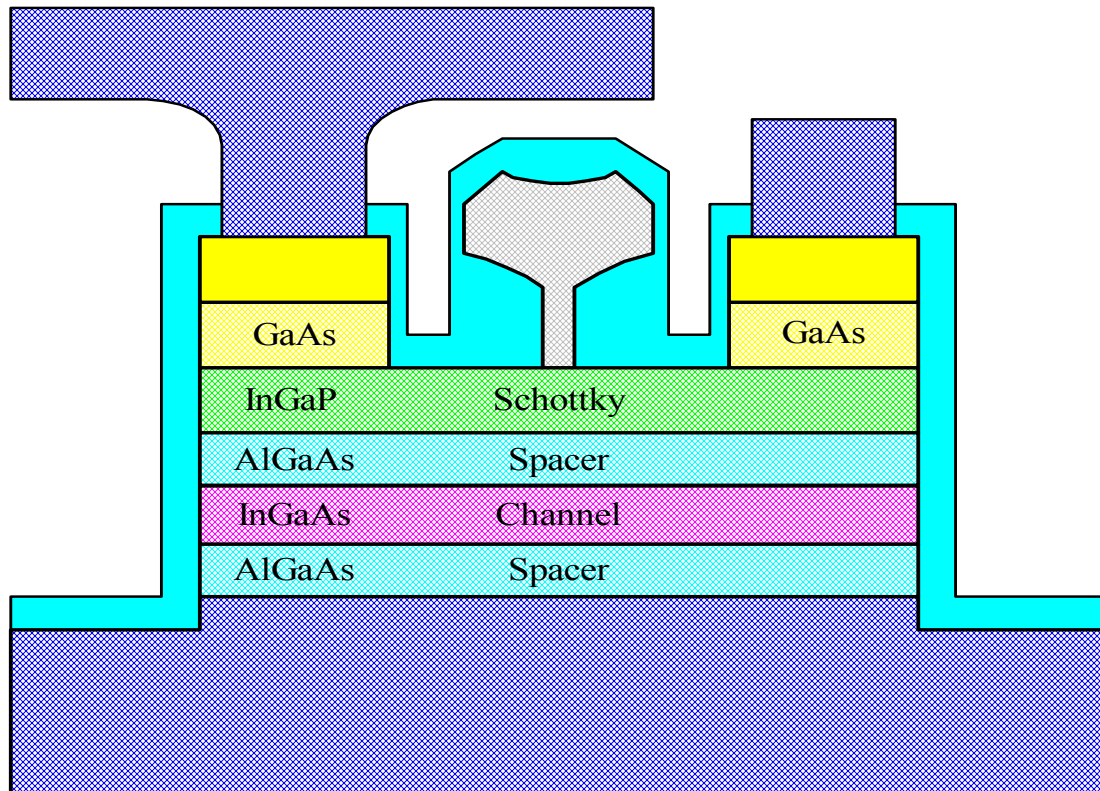
(d)

Figure3-1 Process flow of the HEMT. (c) Device passivation and contact via formation, and (d) air-bridge plating.

Au/Ge/Ni/Au	Ti/Pt/Au	Au/Ge/Ni/Au
n+-GaAs		20 nm
i-In$_{0.49}$GaP		20 nm
i-In$_{0.4}$GaP		4 nm
i-In$_{0.22}$GaAs	Si δ-doping	12 nm
i-Al$_{0.24}$GaAs		4 nm
i-Al$_{0.24}$GaAs		30 nm
i-Al$_{0.28}$GaAs		150 nm
AlGaAs/GaAs supperlattice		
GaAs buffer		
SI GaAs		

Figure 3-2(a) structure of conventional delta doped PHEMT
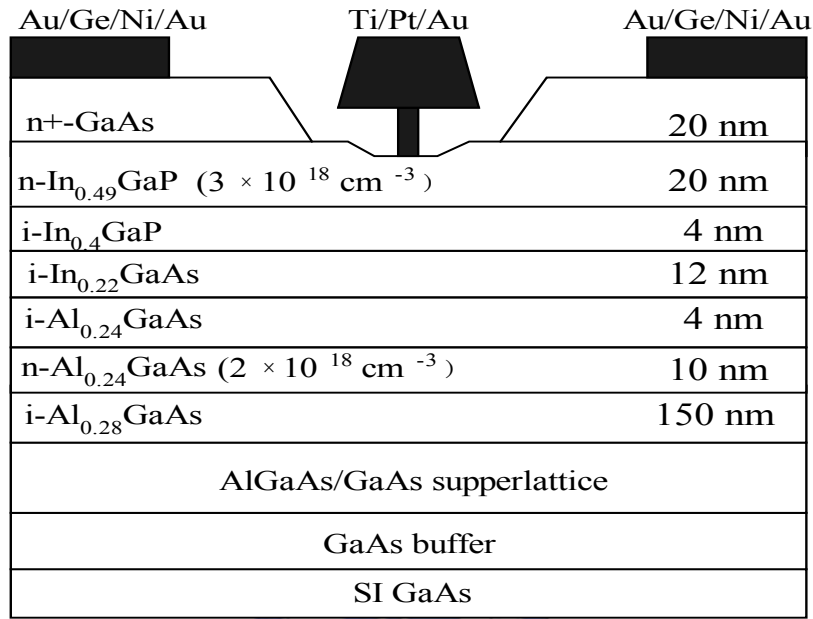
Au/Ge/Ni/Au	Ti/Pt/Au	Au/Ge/Ni/Au

n+-GaAs	20 nm
i-In$_{0.49}$GaP	20 nm
i-In$_{0.4}$GaP	4 nm
n-In$_{0.22}$GaAs (5×10^{17} cm^{-3}) Si δ -doping	12 nm
i-Al$_{0.24}$GaAs	4 nm
i-Al$_{0.24}$GaAs	30 nm
i-Al$_{0.28}$GaAs	150 nm
AlGaAs/GaAs supperlattice	
GaAs buffer	
SI GaAs	

Figure 3-2(b) structure of channel doped PHEMT

Au/Ge/Ni/Au	Ti/Pt/Au	Au/Ge/Ni/Au

n+-GaAs	20 nm
n-In$_{0.49}$GaP (2×10^{18} cm^{-3})	20 nm
i-In$_{0.4}$GaP	4 nm
i-In$_{0.22}$GaAs	12 nm
i-Al$_{0.24}$GaAs	4 nm
n-Al$_{0.24}$GaAs (2×10^{18} cm^{-3})	10 nm
i-Al$_{0.28}$GaAs	150 nm
AlGaAs/GaAs supperlattice	
GaAs buffer	
SI GaAs	

Figure 3-2(c) structure of Schottky layer with uniform Si 2×10^{18} cm^{-3} (top)/ 2×10^{18} (bottom)cm^{-3} .PHEMT

Au/Ge/Ni/Au	Ti/Pt/Au	Au/Ge/Ni/Au	
n+-GaAs			20 nm
n-In$_{0.49}$GaP (3×10^{18} cm^{-3})			20 nm
i-In$_{0.4}$GaP			4 nm
i-In$_{0.22}$GaAs			12 nm
i-Al$_{0.24}$GaAs			4 nm
n-Al$_{0.24}$GaAs (2×10^{18} cm^{-3})			10 nm
i-Al$_{0.28}$GaAs			150 nm
AlGaAs/GaAs supperlattice			
GaAs buffer			
SI GaAs			

Figure 3-2(d) structure of Schottky layer with uniform Si 3×10^{18} cm^{-3} (top)/2×10^{18} (bottom)cm^{-3} PHEMT
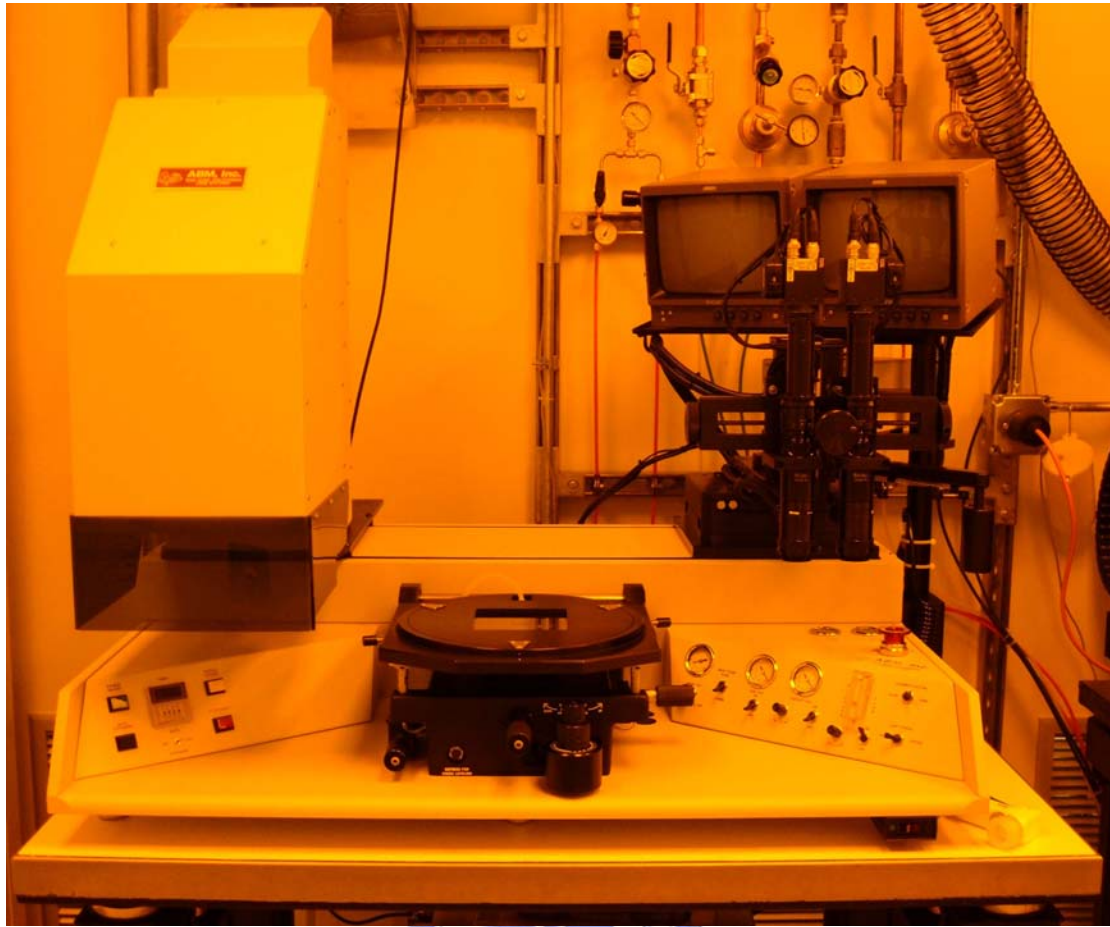
Figure 3-3 Lithography exposure ABM
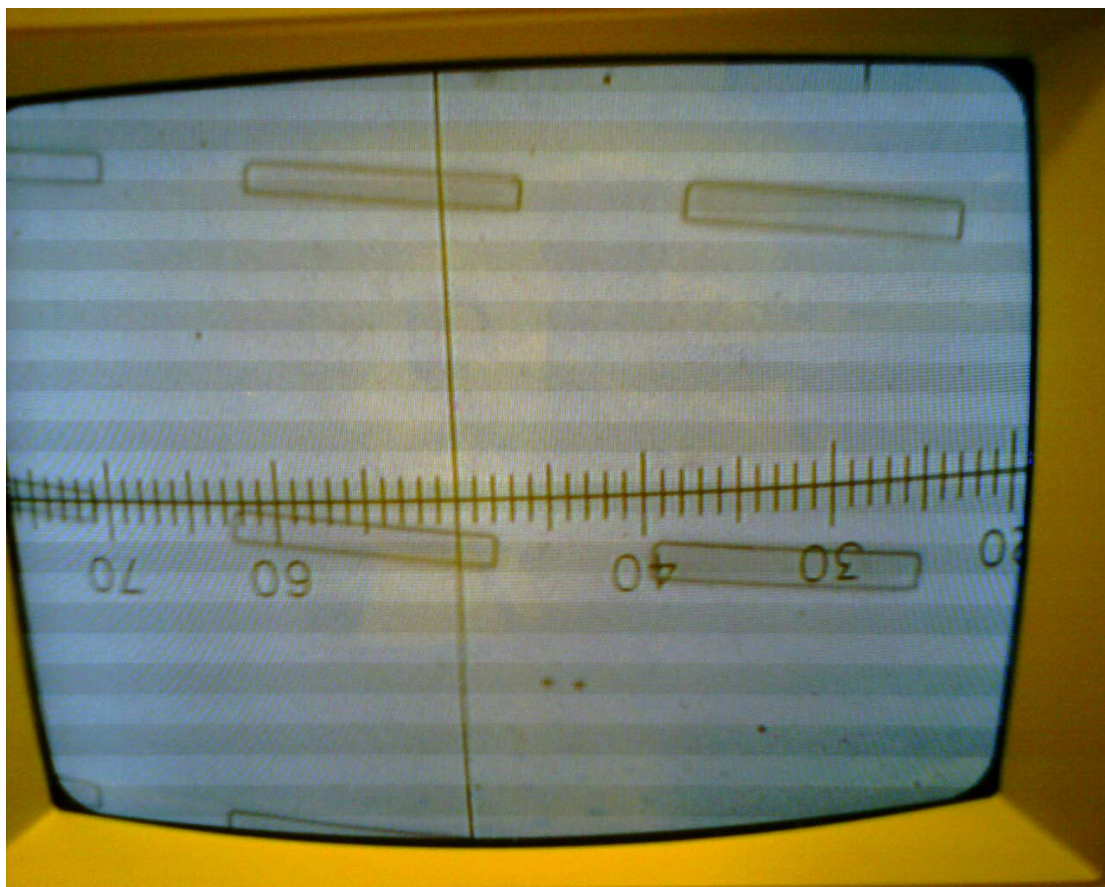
Figure 3-4 mesa pattern image from microscope
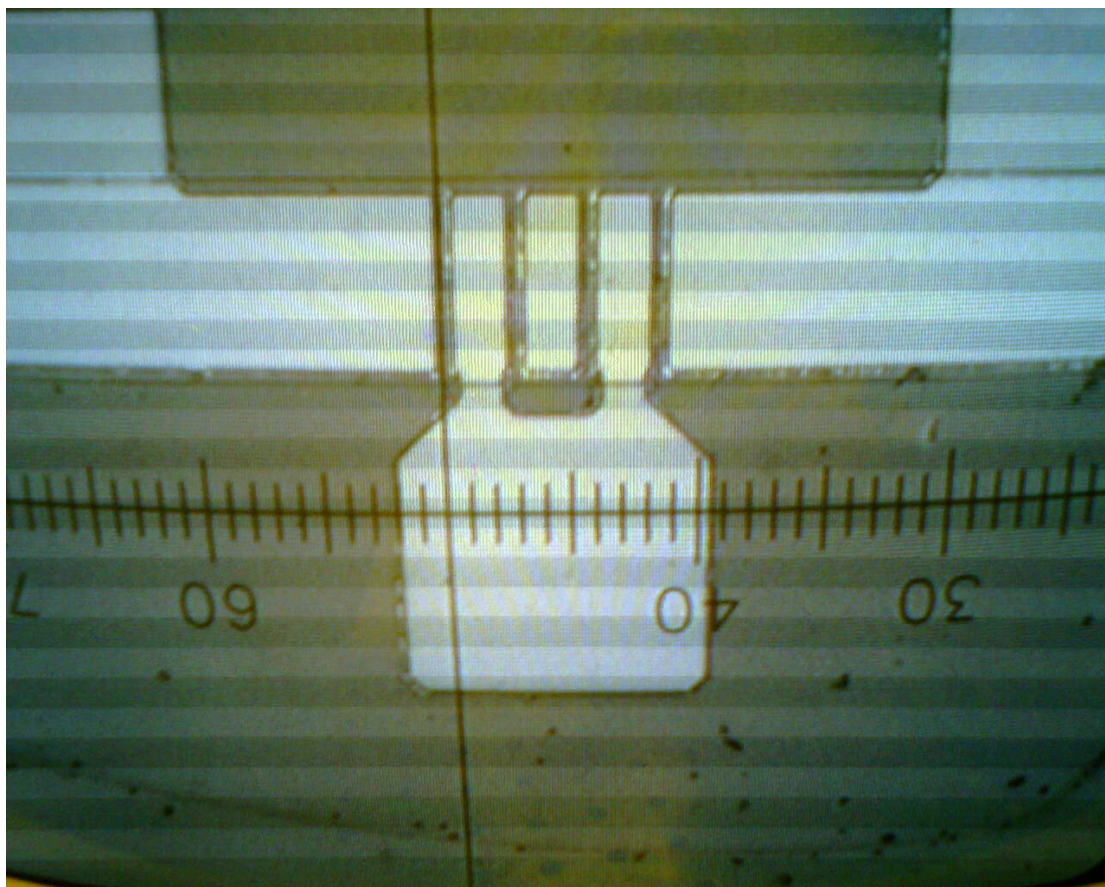
Figure 3-5 The ohmic contact pattern from microscope image

L41411 25.0kV X20.0K 900nm

Figure 3-6 The SEM image of the T-shaped gate.

AB1 RESIST　　　　　THIN METAL LAYER

METAL PADS

(a)

AB2 RESIST　　THIN METAL LAYER

(b)

PLATED GOLD

(c)

COMPLETED BRIDGE

GaAs

(d)
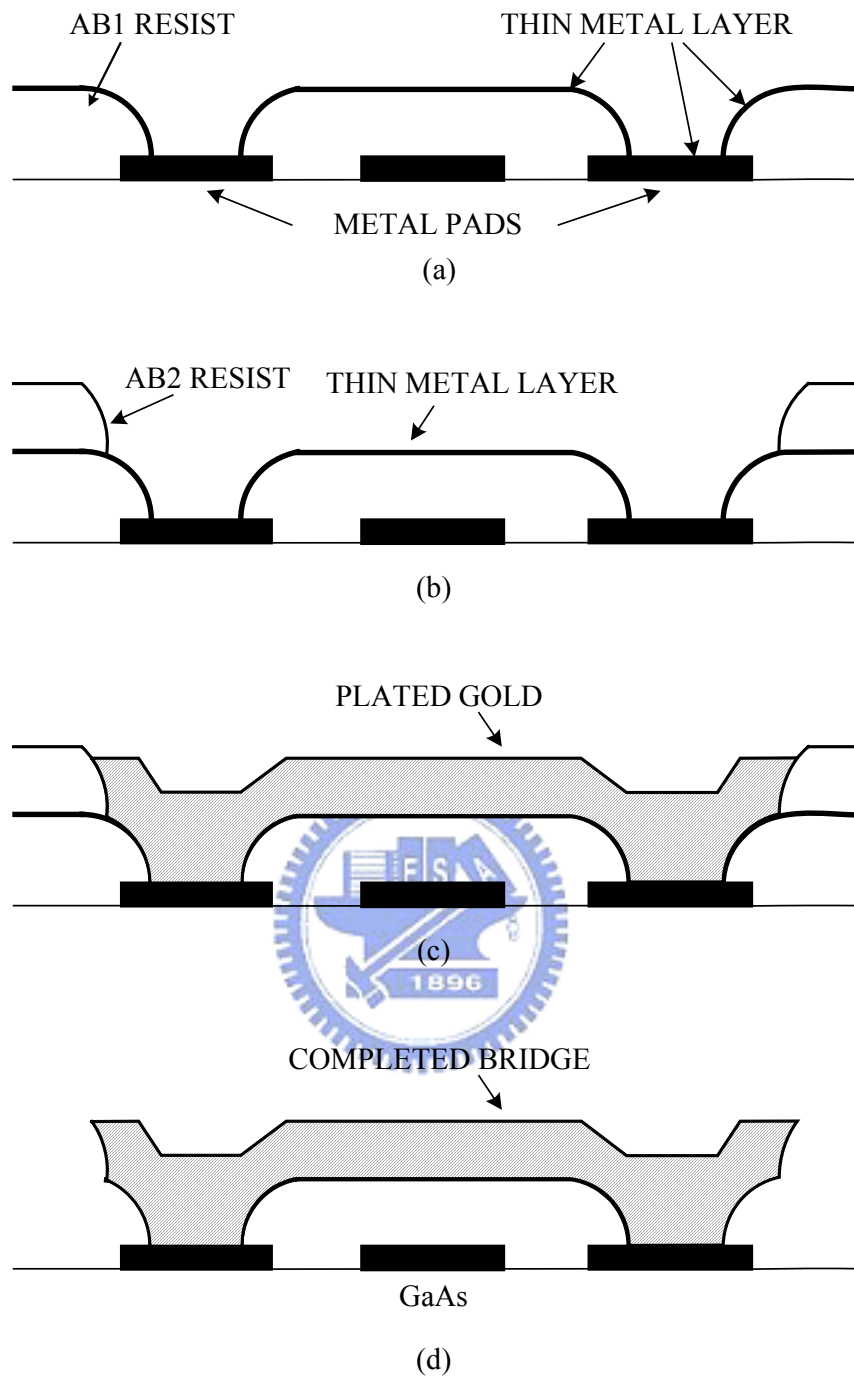
Figure 3-7 The major steps of air-bridge formation.
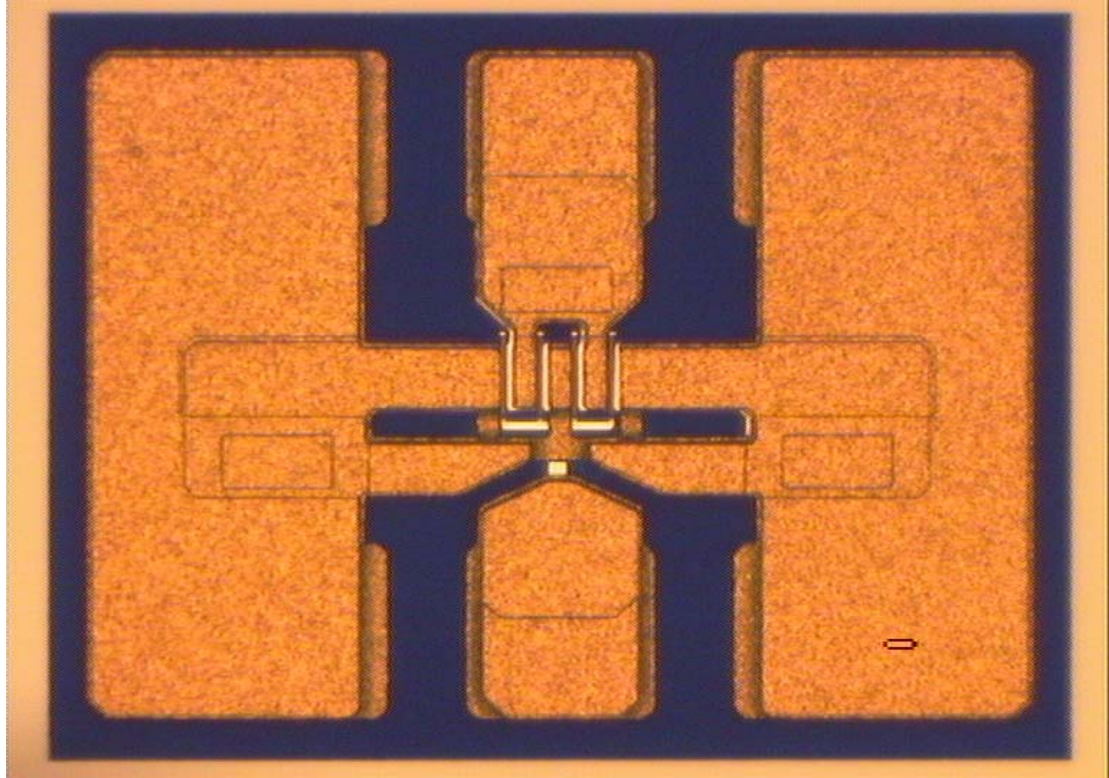
Figure 3-8 The Image of the finished 0.5x160 μ m^2 HEMT device

Chapter 4
Instruments & Measurements

After the devices fabrication, the electrical characteristics of the devices were evaluated. Because any change in the process condition can influence the electrical properties of the finished devices, the process development or modification must be optimized to achieve the best electrical performance. In this chapter, we will describe the electrical measurement instruments and the methods of measurement including DC and RF measurement. The DC characteristics measurements include contact properties, current-voltage curves (I-V curves), pinch-off voltage, breakdown voltage, and extrinsic transconductance. The RF characteristics measurements include scattering parameter (S-parameter), third-order intercept point (IP3), and noise figure. We can use S-parameter to calculate f_T and f_{max}, and obtain the device linearity performance from the IP3 measurement.

4-1 Instruments

In this section, the measurement methods of the HEMT devices are be described. The DC characteristics were measured by Keithley2400 source meter, HP4142B modular DC source, and Karl Suss semi-automatic probe system. The RF characteristics were measured by HP8510 network analyzer, noise figure analyzer, and vector network analyzer (VNA).

4-2 DC characteristics measurement

4-2-1 Contact properties

In order to measure the ohmic contact resistance to identify the contact property, the transmission line method (TLM) is commonly used. The patterns and measurement method of TLM are shown in Figure 4-1. The resistance between two adjacent electrodes can be expressed by

$$R = 2R_c + \frac{R_s L}{W} \qquad (1)$$

where R is measured resistance, R_c is contact resistance, R_s is sheet resistance of channel region, W is electrode width, and L is the space between electrodes.

As Figure 4-1 shows, from the measured R values with different electrode intervals, we can calculate the R_c and R_s values. The R_c value can be calculated by the y-axis intersect, and the R_s value is given by the slope of the function.

Another important parameter related to the contact property is the specific contact resistivity ρ_c, which is defined by

$$\rho_c = \frac{W^2 R_c^2}{R_s} \qquad (2)$$

In this work, the specific contact resistivity was measured by Keithley2400 and Karl Suss semi-automatic probe system. The distances between TLM electrodes were 3 μm, 5 μm, 10 μm, 20 μm, and 36 μm, respectively.

4-2-2 Current-voltage curves (I-V curves)

The I-V curves were measured by HP4142B and Karl Suss semi-automatic probe system. During measuring the I-V curves, three probes were used to contact the pads of drain, source, and gate. The source electrode was grounded, the gate electrode was biased with negative voltage, and the drain electrode was biased with positive voltage.

In this work, the applied drain-to-source voltage was from 0 to 1.5V, and the

applied gate voltage was from 0 to –0.8V. From the I-V curves, we could get the information of saturation current, pinch-off voltage, and knee voltage.

4-2-3 Pinch-off voltage (V$_{PO}$) & Breakdown voltage (V$_B$)

The pinch-off voltage and breakdown voltage were measured by HP4142B and Karl Suss semi-automatic probe system. To measure the pinch-off voltage, the source-to-drain bias keeps constantly, and gradually increases the gate bias to decrease the source-to-drain current. In this work, the pinch-off voltage of the InGaP HEMT was about –0.8V. When measuring the breakdown voltage, the source pad was not contacted to the probe, and the drain was grounded. The drain-to-gate bias was gradually applied to find out the breakdown voltage which was defined as the drain-to gate current reaches 1mA/mm.
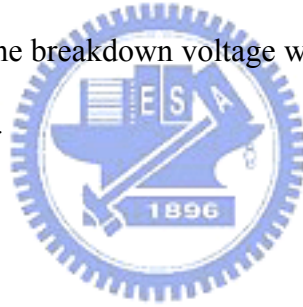
4-2-4 Extrinsic transconductance (g$_m$)

The g$_m$ was measured by HP4142B and Karl Suss semi-automatic probe system. To measure the g$_m$, the source-to-drain bias is applied, and the gate bias is varied to obtain the peak g$_m$ value. Different source-to-drain bias or gate bias will lead to different g$_m$ value. In this work, the source-to-drain voltage was at 1.4V, and the gate voltage was ranging from –1 to 1V. The value of g$_m$ was calculated by differentiating I$_d$ vs. V$_{gs}$.
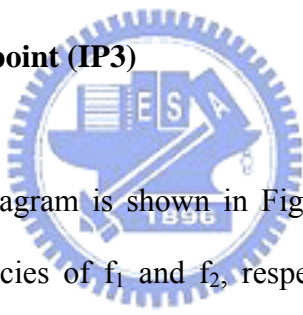
$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{3}$$

4-3 RF characteristics measurement

4-3-1 Scattering parameters (S-parameters)

The S-parameters are usually measured by VNA. The S-parameters of two ports consists of four terms. They are input reflection coefficient (S_{11}), forward transmission coefficient (S_{21}), reverse transmission coefficient (S_{12}), and output reflection coefficient (S_{22}). Before measuring the S-parameters, the instruments must be calibrated first to ensure the result of the measurement is correct. The S-parameters can be used to calculate f_T and f_{max}.

4-3-2 Third-order intercept point (IP3)

The IP3 measurement diagram is shown in Figure 4-3. Two signal generators generate signals with frequencies of f_1 and f_2, respectively. Then the signals were mixed and amplified by the mixer and the amplifier. The output spectrum is shown in Figure 4-4. The desired fundamental signals and the undesired harmonic signals are mixed togather, and the greater the ratio between the fundamental and the harmonic signals is, the greater the linearity is. From Figure 4-4, the value of G is the gain of the amplifier, and Δ is the power difference between output fundamental signal and third-order product signal. IP3 can be expressed as following.

$$IP3(dBm)=P_{in}(dBm)+ \Delta/2 \ (dB) \hspace{3cm} (4)$$

(a)

Active Region   Contact Pad

L_1 L_2 L_3 L_4 L_5

W

(b)

R

$2R_C$

L_5 L_4 L_3 L_2 L_1

L
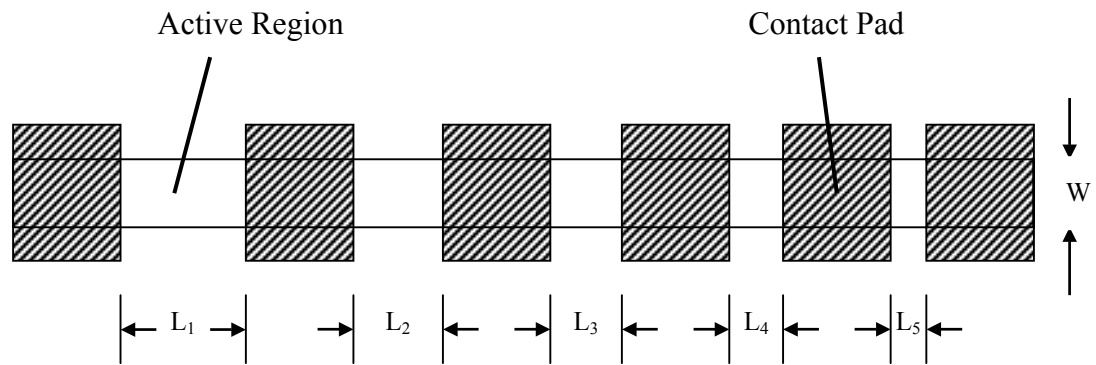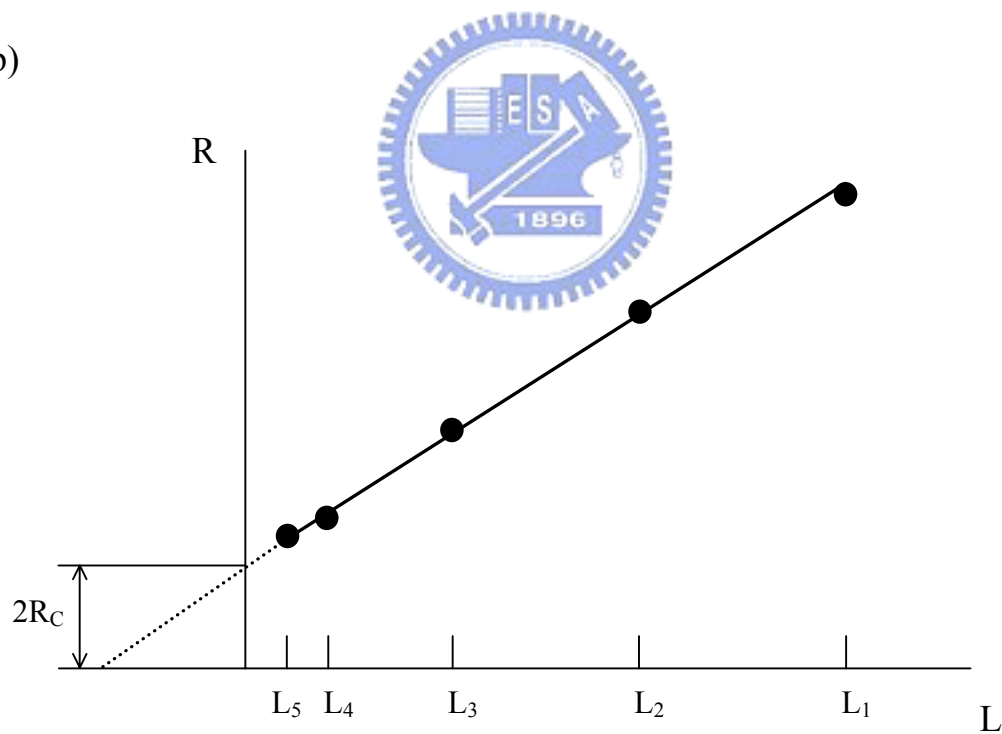
Figure 4-1   The transmission line method (TLM).
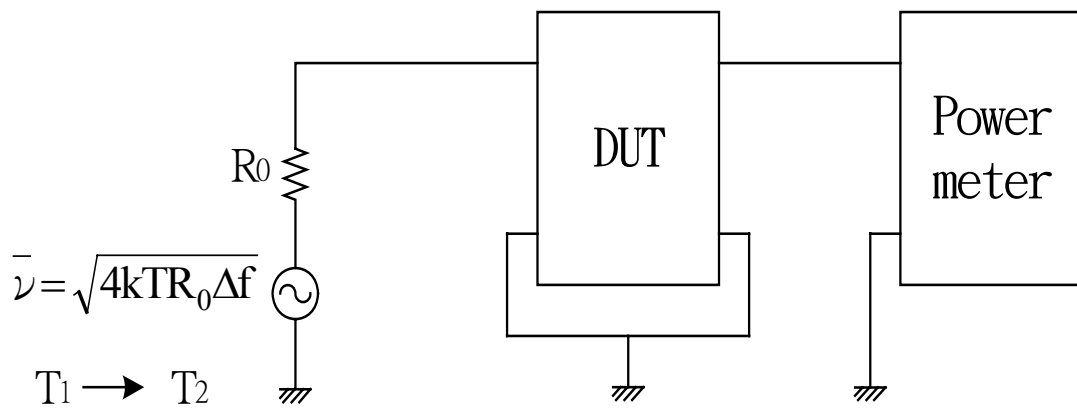(a) TLM patterns. (b) TLM measurement method.
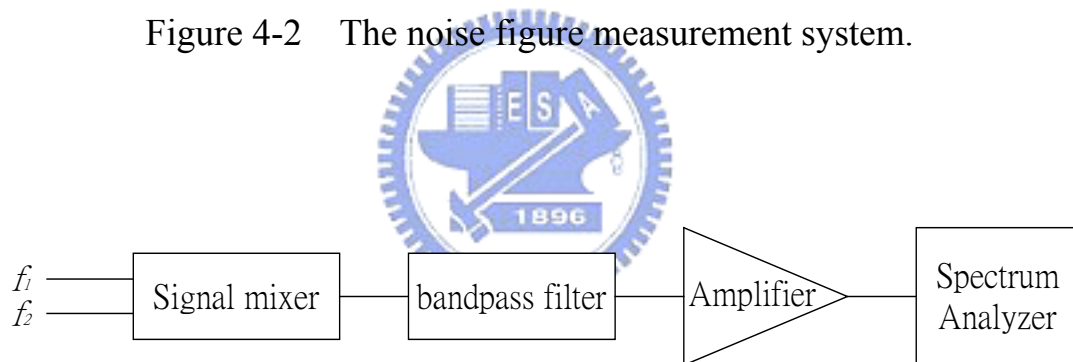
Figure 4-2   The noise figure measurement system.

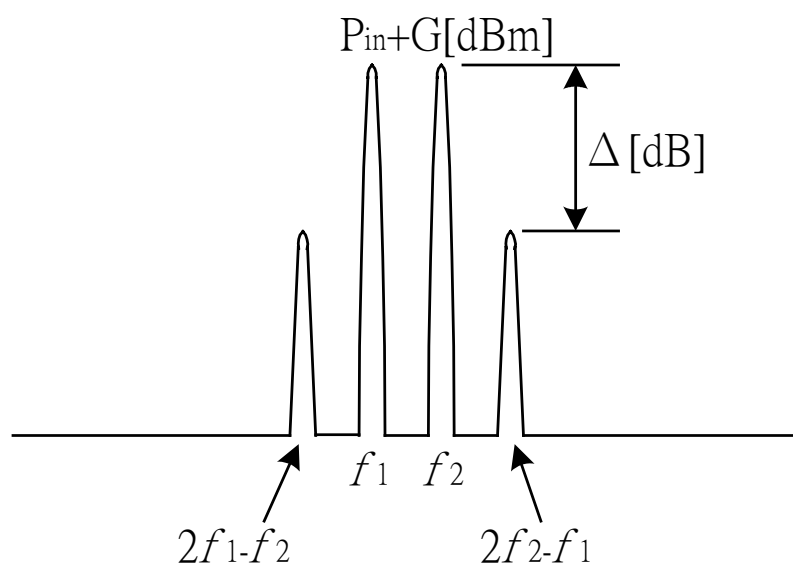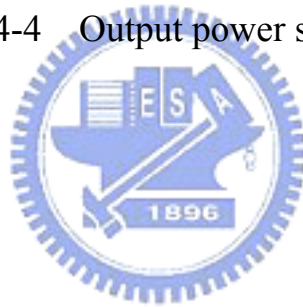Figure 4-3   IP3 measurement system diagram.

$P_{in}+G[dBm]$

$\Delta[dB]$

$2f_1\text{-}f_2$

f_1 f_2

$2f_2\text{-}f_1$

Figure 4-4   Output power spectrum.

Chapter 5

Results and Discussion

In this chapter, the electrical performances of the InGaP/InGaAs PHEMTs are described. The three type of $0.5 \times 160 - \mu m$ InGaP/InGaAs HEMTs, as show in Figure 3-2, were fabricated ,tested, and compared.

The DC and RF performances are also described in this chapter. The DC characteristics include I-V curve, g_m. The RF characteristics are IP3, and ACPR(adjacent-channel power ratio).

Figure 5-1 shows the I_{DS} versus V_{DS} curves of the three different types of devices. From a comparison of these devices, it can be seen that the channel layer-doped device has a higher I_{DSS} (I_{DS} @ $V_{GS} = 0V$) of 561.1mA/mm and has a higher pinch-off voltage of –2.2V. The characteristics of the Gm dependence on the gate-bias are shown in Figure 5-2. It can be observed that extra doping either in the channel or in the Schottky layer of a conventional δ-doped InGaP/InGaAs PHEMT result in a flatter Gm distribution, but both have a lower maximum Gm value as compared to that of a conventional δ doped device. The comparative I_{DS}-V_{GS} curve for these devices is shown in Figure 5-3. The channel-doped device has the maximum I_{DS} value of 625.1 mA/mm which is the hightest of the three structures. The addition of doping typically indicates that the extra doping can improve the device linearity and can be used for handset applications. However, it is not preferred in high-voltage operations

of base stations. A comparison of the DC characteristics of these three 0.5 um $\times$ 160 um devices is presented in Table I &II.

To further investigate the linearity performance of the three devices, the polynomial curve fitting technique using equation (2-18) was applied to the transfer characteristic functions of these devices.

Moreover, the IM3 levels incurred by the device can then be readily derived as

$$IM3 = \frac{3}{8}a_3A^3 + \frac{50}{32}a_5A^5 \qquad\qquad (2\text{-}18)$$

For a device with good linearity, I_{DS} should increase linearly with V_{GS}, therefore, a_1 should be larger and the higher order constants a_3 and a_5 should be minimized . The coefficients of these devices extracted from the measurement data when V_{DS} = 1.5V are listed in Table 5-1.
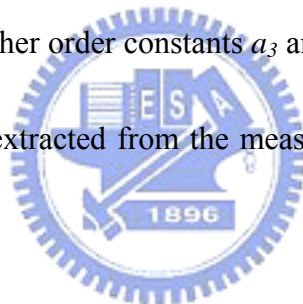
To evaluate the device linearity, the IM3 level and IP3 of these devices were measured. The IM3 and IP3 measurements were carried out by injecting two signals with the same amplitude but at two different frequencies: 5.8 GHz and 5.801GHz, setting the devices biased at V_{DS} = 1.5 V, and adjusting the I_{DS} to get the IP3 versus I_{DS} curves. The channel-doped device shows a more uniform electron distribution in the 2DEG when the V_{DS} bias increases. But for the Schottky layer-doped device, the electrons concentration is higher at the top of the channel where the electron distribution is sharp on one side. A load pull measurement was performed on these devices using a W-CDMA modulation signal as the input to evaluate the device linearity at different DC biases. The P_{1dB}, gain of these devices were measured by using a single tone input power at 2GHz and by tuning the maximum power with different V_{DS} at the best

biases for IM3 level. A W-CDMA modulation signal was used as the input signal to meet the adjacent-channel power ratio (ACPR) with P_{1dB} at +/- 5 MHz offset and at +/- 10 MHz offset from the center frequency. Table 5-2 shows a comparison of the ACPR measurements for both the Schottky layer-doped device and the channel-doped device under different V_{DS} biases at the best I_{DS} bias for the IM3. However, for the Schottky layer-doped device, the distribution of Gm is compressed with an increase V_{DS} bias. The ACPR tests performed on these two devices using 2GHz W-CDMA modulation signals and a V_{DS} bias at 1.5V are shown in Figure 5-4. When devices bias at class AB, the channel doped device performs better power performance with ACPR of -28 dBc at +/- 5 MHz offset and –41.5 dBc at +/- 10 MHz offset from the center frequency Figure 5-4 (a). The performance of the Schottky layer-doped device is ACPR of -28 dBc at +/- 5 MHz offset and -42 dBc at +/- 10 MHz offset [Figure5-4 (c)]. When device bias at class A, the performance of the Schottky layer-doped device is inferior to that of the channel-doped device as it only obtained ACPR of -26 dBc at +/- 5 MHz offset and -42 dBc at +/- 10 MHz offset [Figure. 5-4 (d)]]. By contrast, the channel-doped device demonstrates a much better linearity under CDMA modulation than does the uniformly-doped device, especially if there is a high I_{DS} bias
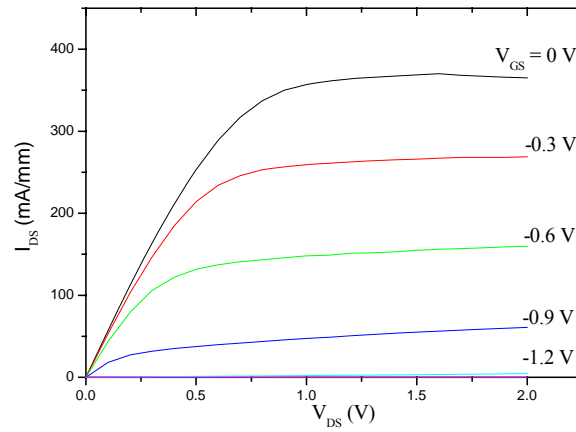
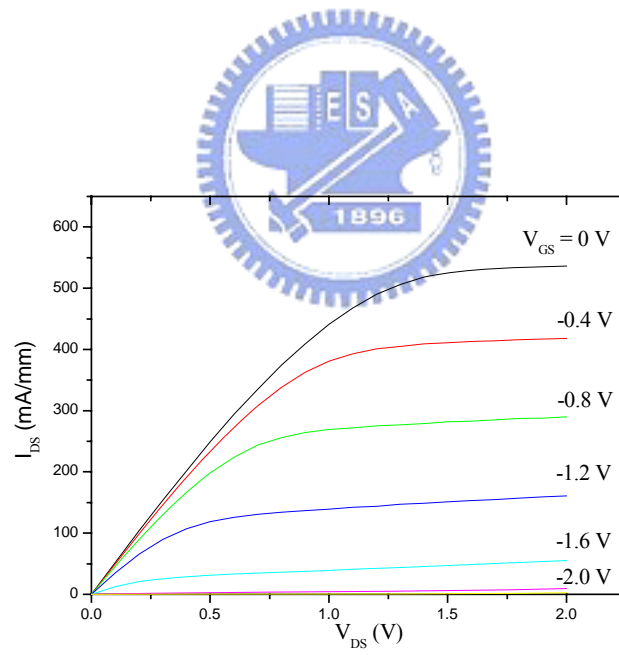Figure 5-1 (a)I_{DS} versus V_{DS} curve for the conventional δ-doped
InGaP PHEMT.

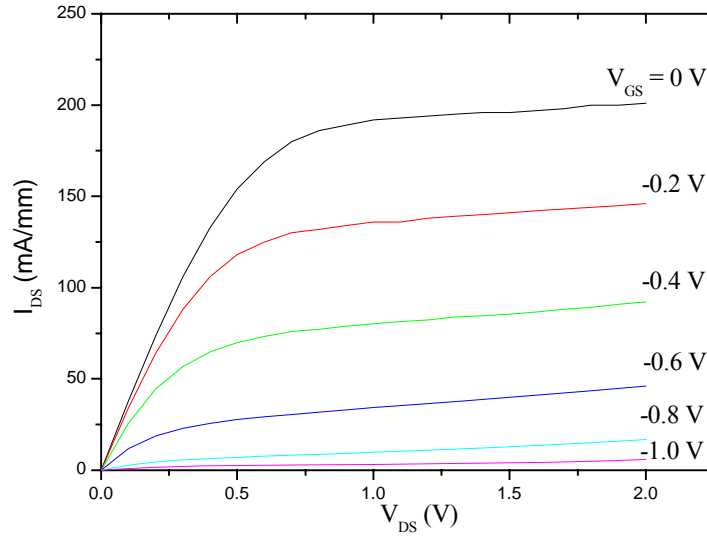Figure 5-1 (b)I_{DS} versus V_{DS} curve for the channel-doped
InGaP PHEMT.

Figure 5-1 (c)I_{DS} versus V_{DS} curve for the schotty uniformity-doped
(2×10^{18} cm^{-3} (top), 2×10^{18} (bottom)cm^{-3})

InGaP PHEMT.

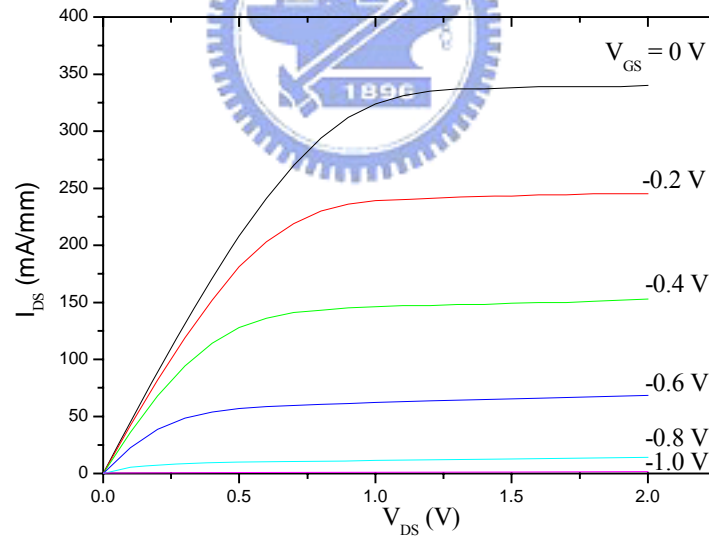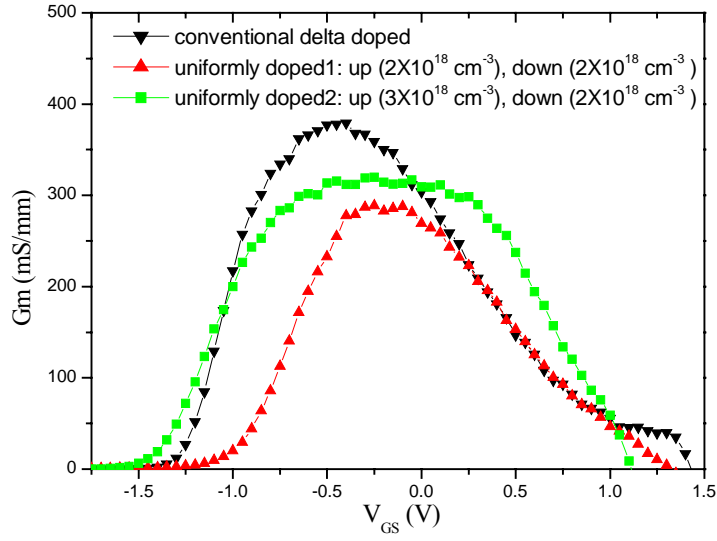Figure 5-1 (d)I_{DS} versus V_{DS} curve for the schotty uniformity-doped
(3×10^{18} cm^{-3} (top), 2×10^{18} (bottom)cm^{-3})

InGaP PHEMT.

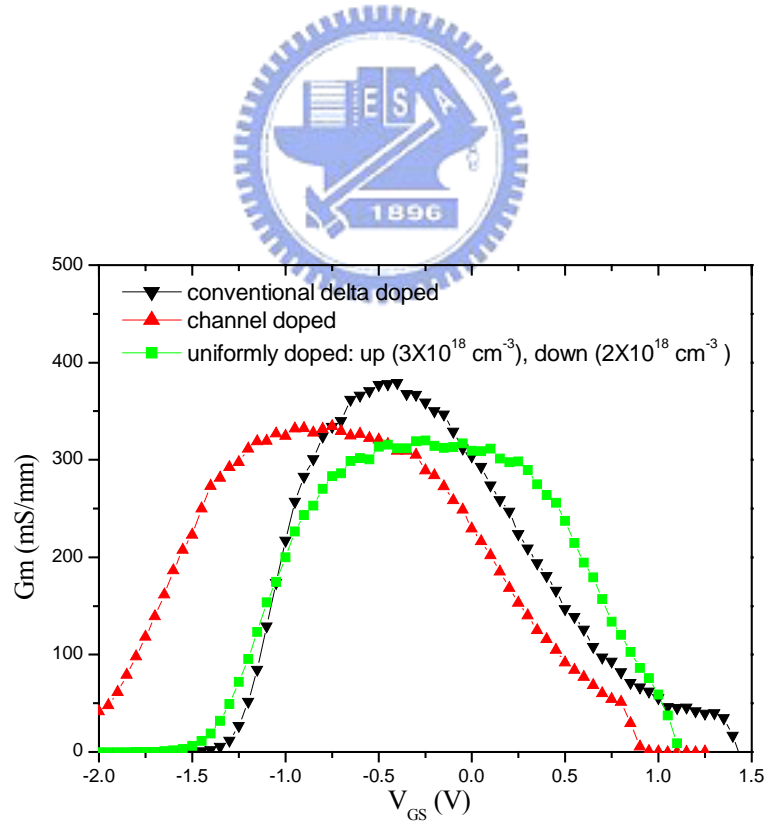Figure 5-2 (a)Gm versus V_{GS} curve for the Schotty-doped
InGaP PHEMT.

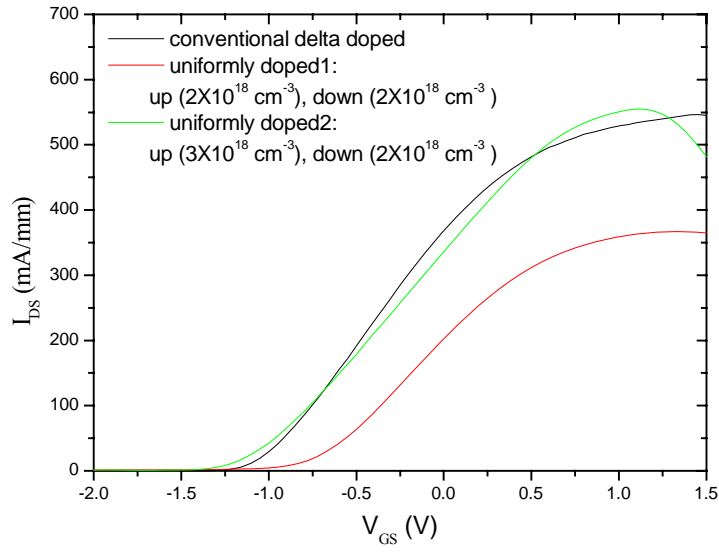Figure 5-2 (b)Gm versus V_{GS} curve for the Schotty & channel doped
InGaP PHEMT.

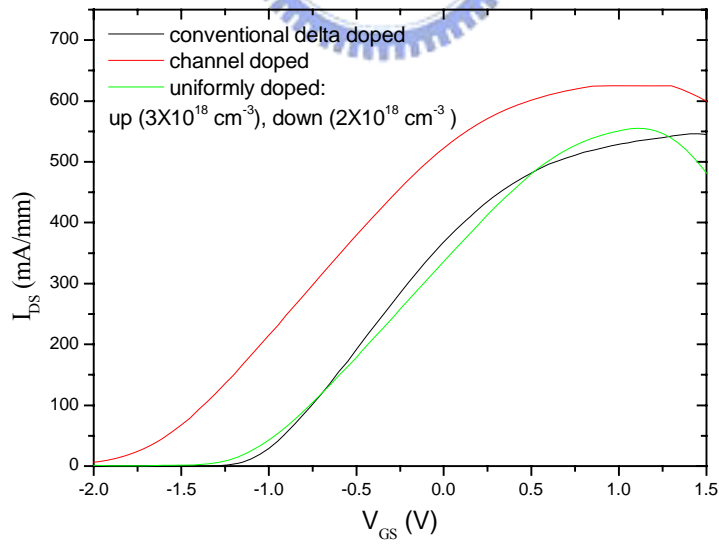Figure 5-3 (a)Ids versus V_{GS} curve for the uniform-doped
InGaP PHEMT.

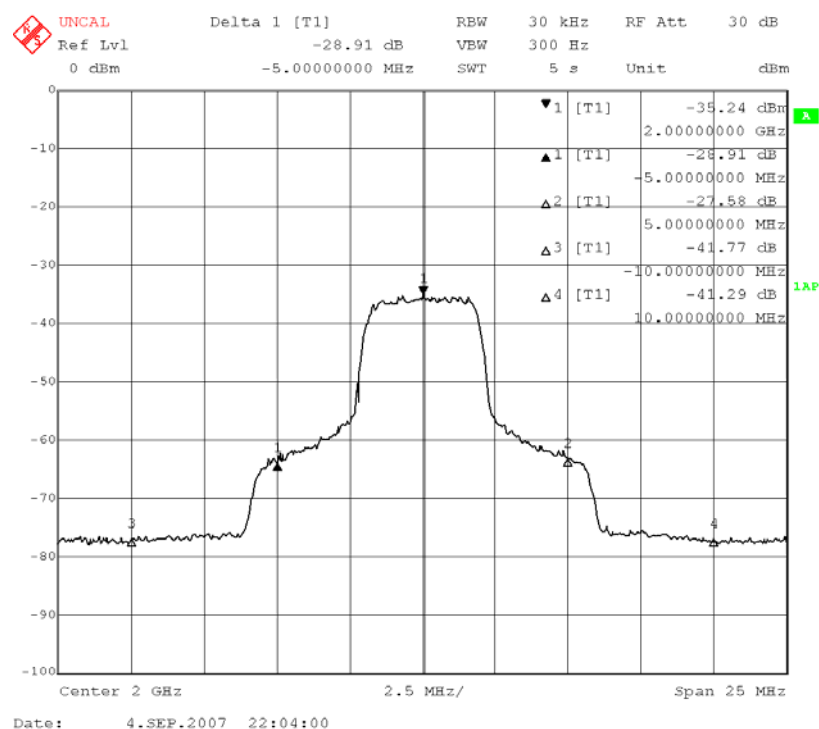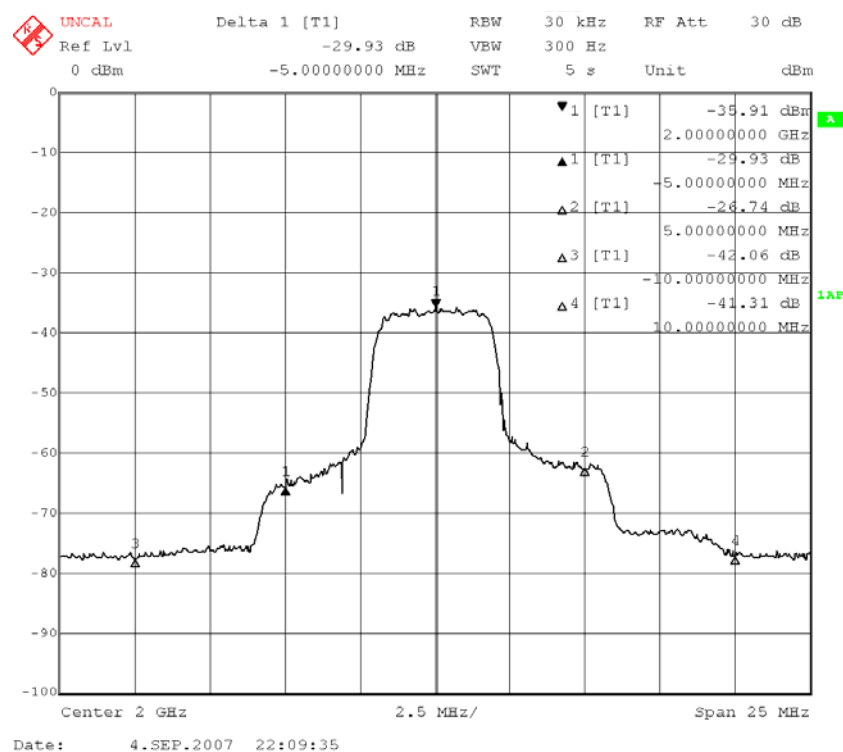Figure 5-3 (b)Idsversus V_{GS} curve for the Schotty & channel doped
InGaP PHEMT.

(a)
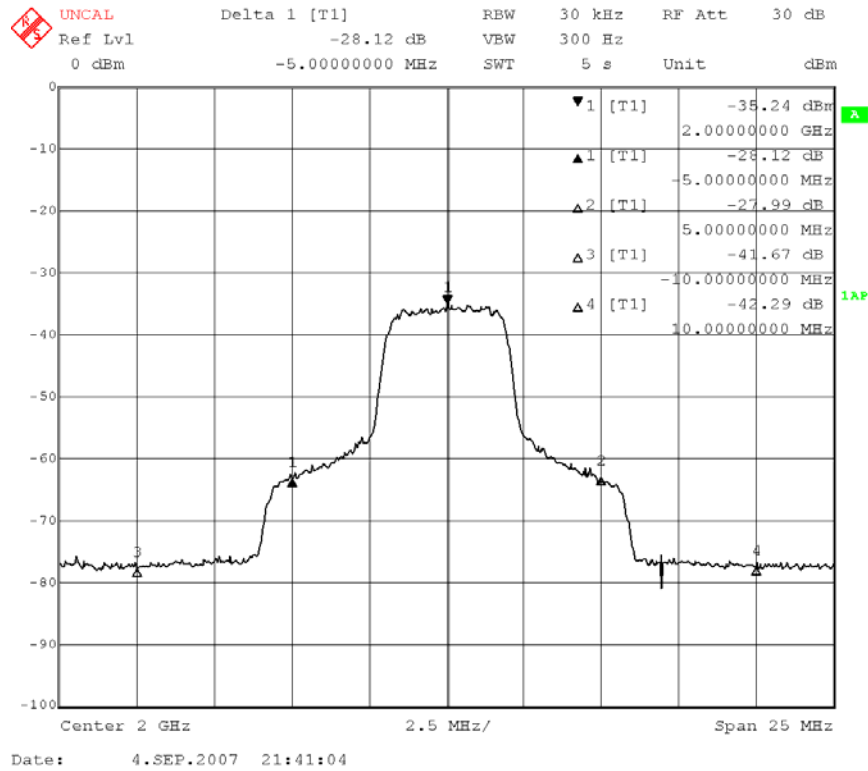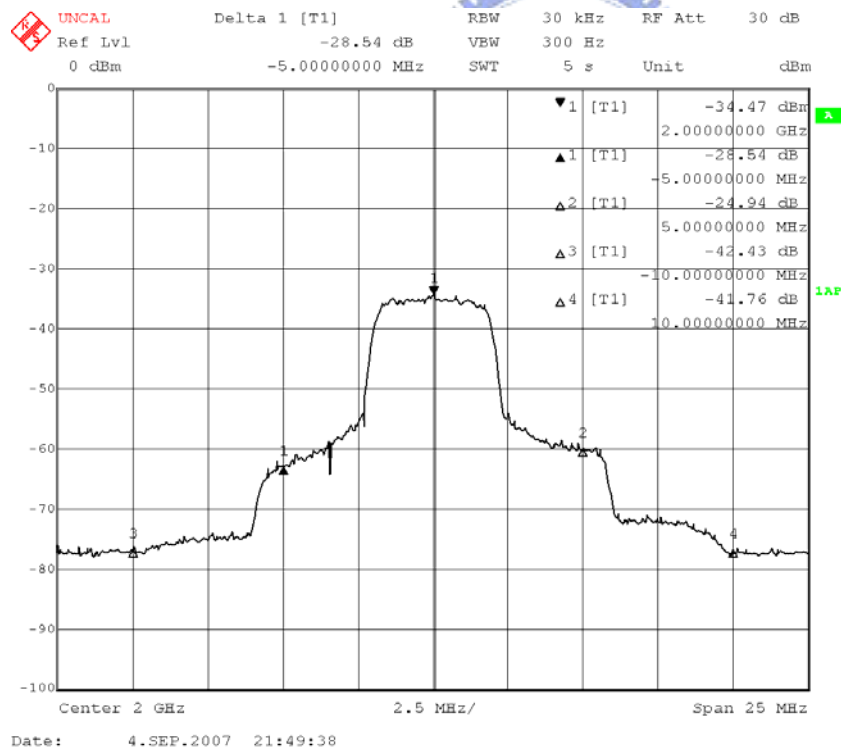

(b)

Figure5-4 (a)(b) ACPR spectrum of the channel doped InGaP/InGaAs PHEMTs (device size: 0.5 x 160 μm^2) (a) bias condition: Vds=1.5V, class AB and the input signal frequency is 2 GHz (b) bias condition: Vds=1.5V, class A and the input signal frequency is 2 GHz.

(c)

(d)

Figure5-4 (c) (d) ACPR spectrum of the uniform doped InGaP/InGaAs PHEMTs (device size: 0.5 x 160 μm^2) (c) bias condition: Vds=1.5V, class AB and the input signal frequency is 2 GHz (d) bias condition: Vds=1.5V, class A and the input signal frequency is 2 GHz.

(e)

(f)

Figure5-4 (e) (f) ACPR spectrum of the conventional σ doped InGaP/InGaAs PHEMTs (device size: 0.5 x 160 μm^2) (e) bias condition: Vds=1.5V, class AB and the input signal frequency is 2 GHz (f) bias condition: Vds=1.5V, class A and the input signal frequency is 2 GHz.

Table 5-1

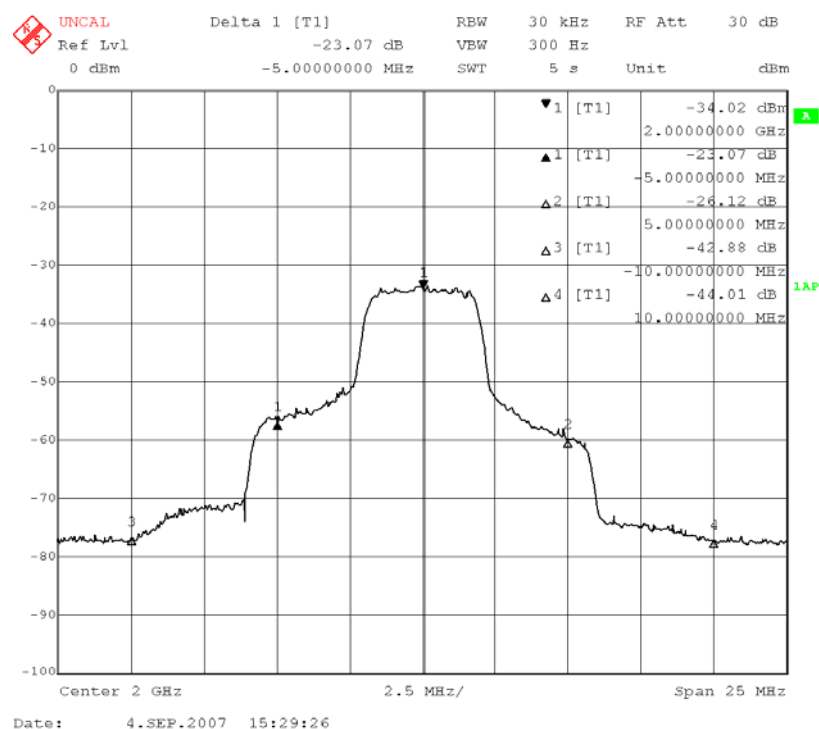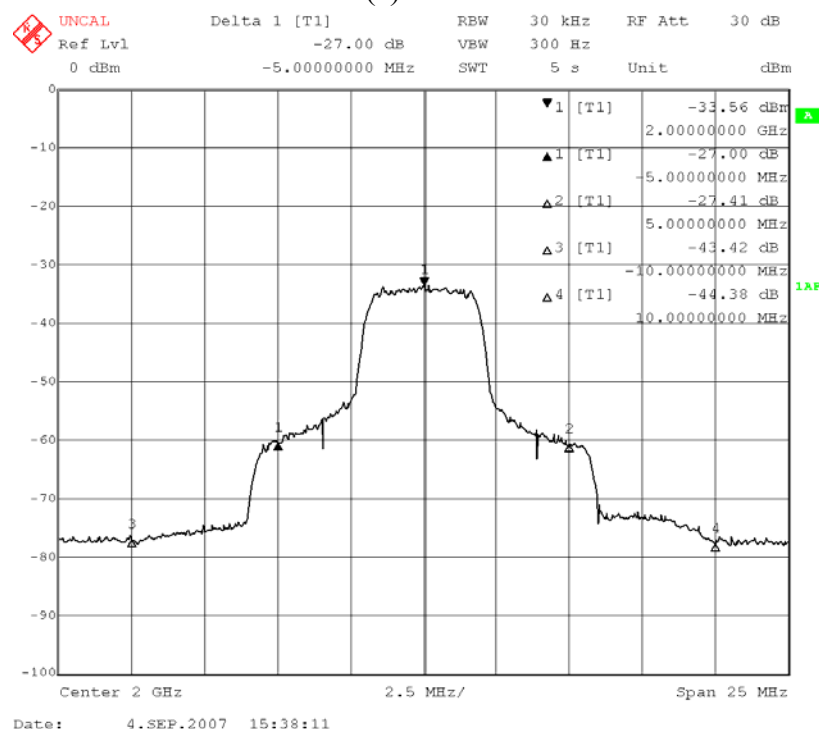The comparison of the electron DC properties of InGaP PHEMT with different doping.

Device Type			Conventional δ doped InGaP/InGaAs PHEMT	Channel doped InGaP/InGaAs PHEMT	Uniformly doped InGaP/InGaAs PHEMT
Doping density	Delta doping (cm^{-2})	above	4.0×10^{12}	4.0×10^{12}	undoped
		below	2.0×10^{12}	2.0×10^{12}	
	Channel doped (cm^{-3})		undoped	5.0×10^{17}	undoped
	Uniformly doped carrier layers (cm^{-3})	above	undoped	undoped	3.0×10^{18}
		below			2.0×10^{18}
I_{DSS} (I_{DS} @ V_{GS}=0, mA/mm)			403.1	522.9	336.5
I_{DS}-max (mA/mm)			609	625.1	554.7
Gm_{max} (mS/mm)			450.0	332.5	320.0
Pinch-off voltage			-1.30	-2.25	-1.40
I_{DS}-V_{GS} polynomial 1st order coefficient a_1			0.05417	0.03716	0.04980
I_{DS}-V_{GS} polynomial 3rd order coefficient a_3			-0.01126	-0.00730	-0.00573
a_3/a_1			-0.20786	-0.19645	-0.11506
I_{DS}-V_{GS} polynomial 5th order coefficient a_5			9.43333E-4	0.00464	-0.00571
a_5/a_1			0.01741	0.124865	-0.11466

Table5-2 P_{1dB}, Gain, PAE and ACPR of the three different devices under different V_{DS} at class AB bias.

Device	RF Performance		Class AB	Class A
Schottky layer doped InGaP/InGaAs PHEMT	P1dB(dBm)		9.04	9.41
	Gain(dB)		21.4	22.3
	ACPR (dBc)	+5MHz offset	-27.99	-24.94
		-5MHz offset	-28.12	-28.54
		+10MHz offset	-42.29	-41.76
		-10MHz offset	-41.67	-42.43
Channel doped InGaP/InGaAs PHEMT	P1dB(dBm)		8.77	8.31
	Gain(dB)		20.98	20.4
	ACPR (dBc)	+5MHz offset	-27.58	-26.74
		-5MHz offset	-28.91	-29.93
		+10MHz offset	-41.29	-41.31
		-10MHz offset	-41.77	-42.06

Chapter 6

Conclusions

Theoretical base for achieving high linearity device is first discussed. The relationships between IM3 and IP3 with two current source Gm (V_{GS}) and Gds (V_{DS}) were derived. According to the linearity analysis in this study, the device linearity can be improved either by layer structure design or electron doping profile modification. Four different types of InGaP/InGaAs PHEMT devices are studied based on the theoretical analysis in this study.

In the InGaP/InGaAs PHEMT linearity improved, even though the δ doped device has higher peak transconductance, the uniformly-doped and channel doped PHEMT shows much better device linearity. This is because the devices has more uniform electron distribution in the quantum well region which enables the device to possess straight I_{DS} versus V_{GS} curve and more flat G_m versus I_{DS} curve Thus, the uniformly-doped and channel doped PHEMT are more suitable than δ doped device for the modern digital wireless communication system application which impose very stringent linearity requirement for the devices. However, when the device current bias point increase, the performance of the uniformly-doped device is inferior to that of the channel-doped device. By contrast, the channel-doped device demonstrates a much better linearity under CDMA modulation than does the uniformly-doped device, especially if there is a high I_{DS} bias.

The channel doped device with light doping $5\times10^{17}/cm^3$ in the channel region demonstrated highest maximum I_{DS} and flattest G_m versus V_{GS} curve. These DC characteristics lead to the best ACPR under CDMA modulation for the channel doped device as compared to the other two types of devices studied even though it has

lowest electron mobility among these three devices.

Overall, in this study, the experimental results in this work are consistent with the theoretical analysis. Layer structure design and doping modification either in channel region or in Schottky layer are proven to be effective in improving the device linearity for the PHEMT devices in this study, this approach can be practically used for the development for high linearity devices for wireless communication application in the future.

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