國立交通大學

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博士論文

先進互補式金氧半電晶體及氮化矽快閃式記憶元件之可靠度分析和蒙地卡羅模擬

Reliability and Monte Carlo Analysis in Advanced CMOS and SONOS Flash Memory

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摘 要

本篇論文主要著重在蒙地卡羅模擬(Monte Carlo simulation)於先進互補式金氧半電晶體(advanced CMOS)及氮化矽快閃式記憶元件(SONOS flash memory)之應用。此外，高介電閘極氧化層(high-*k*)之可靠性議題，如電壓溫度引致不穩定(BTI)之研究，亦有所探討。

第一章首先描述本論文中蒙地卡羅模擬之三項應用研究成果。前兩項探討NOR 型氮化矽記憶陣列中，寫入干擾(program disturb)以及電子非平衡傳輸(non-equilibrium transport)之物理機制。元件基本結構及寫入方法亦有清楚描述。最後一項應用是研究對於鍺通道(Ge-channel)雙閘極(double gate)電晶體，量子效應對電洞遷移率(hole mobility)之影響。此外，吾人於此篇論文最後，強調高介電閘極氧化層中負電壓溫度引致不穩定之重要性。

第二章探討在潛擴散式(buried diffusion)位元線 SONOS 陣列中，當位元線寬度變窄時所衍生之寫入干擾現象。實驗結果顯示，寫入干擾造成鄰近元件之臨界電壓有 1 伏特的增加，使得寫入干擾已成為 50 奈米 NOR 型 SONOS 技術開發之主要問題之一。吾人採用多階式蒙地卡羅模擬來探討寫入干擾之物理機制。研究結果顯示，在熱電子寫入的過程中，鄰近元件臨界電壓會漂移的原因，是由於撞擊游離所產生之二次電子，注入至鄰近元件。此種效應對於窄位元線、淺潛擴散接面以及高摻雜環形佈值濃度之元件，將愈益明顯。此外，吾人發現透過熱電子寫入電壓以及元件結構之最佳化，可將減低寫入干擾。

第三章提出一種在潛擴散式位元線 SONOS 陣列中新的熱電子寫入方法。此方法是利用在奈米尺度電子呈現之非平衡傳輸現象。與傳統熱電子寫入方法不同，電子加速是在兩個相鄰元件內完成。因此，汲極至源極電壓(V_{ds})可降低至 2.5 伏特，以解決閘極長度微縮時所遭遇之貫穿(punch-through)問題。吾人亦利用蒙地卡羅模擬來探討電子非平衡傳輸行為。研究結果顯示，新的熱電子寫法方式比傳統熱電子寫入方法具有更高之寫入效率，這是因為電子經過潛擴散區域後，在寫入單元之源極端具有殘存的能量。此外，當位元線微縮時，新的熱電子寫入方法將更有效率。

第四章探討對於鍺通道雙閘極電晶體，量子效應對電洞遷移率之影響。低電場之電洞遷移率是透過蒙地卡羅方法求得。模擬結果得知，對於 (100) /[110]「矽」通道，電洞遷移率隨著通道厚度變薄而減少。此模擬結果與實驗相符合。然而對於(100)/[100]「鍺」通道，電洞遷移率在某個通道厚度下具有最大值。此現象乃因「次能帶內」散射與「次能帶間」散射交互作用下所產生。在(110)/[-110]「鍺」通道方向上，亦可發現相同情形。此外，吾人發現當單軸壓縮應力施於(100)/[110]或(110)/[-110]鍺通道上時，電洞遷移率將可進一步提昇。

在第五章，吾人利用電腦自動化量測電路系統，研究 HfSiON pMOSFETs 中負電壓溫度所引致之不穩定性。實驗結果顯示，在某特定加壓條件下，負電壓溫度加壓所引致之汲極電流，將從增益模式逐漸演變成退化模式，隨著加壓時間或加壓電壓之呈現奇特的「轉彎現象」(turn around)。此外，對於 pMOSFET 元件加壓後，汲極電流呈現退化行為。然而，對於 nMOSFET 元件加壓後，汲極電流呈現恢復行為。吾人提出一「雙極電荷捕捉模型」成功解釋奇特的「轉彎現象」，並以單電荷散逸量測、電荷幫浦法以及載子分離量測，驗證所提出之物理模型。

最後於第六章，吾人將對本論文做個總結。

關鍵字：蒙地卡羅模擬，先進互補式金氧半電晶體，氮化矽快閃式記憶元件，潛擴散式，熱電子寫入，寫入干擾，低汲極至源極電壓，貫穿，雙閘極，鍺通道，電洞遷移率，單軸壓縮應力，高介電閘極氧化層，負電壓溫度引致不穩定，雙極電荷捕捉模型，單電荷散逸，電荷幫浦量測

Reliability and Monte Carlo Analysis in Advanced CMOS and SONOS Flash Memory

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ABSTRACT

This thesis will focus on the Monte Caro simulation and its applications to advanced CMOS and SONOS flash memory. The reliability issue, negative bias temperature instability (NBTI) in advanced gate dielectric (high-*k*), is studied as well.

In Chapter 1, three applications of Monte Carlo simulation are firstly addressed. The first two are the investigations of program disturb and electron non-equilibrium transport in a NOR-type SONOS array. The device configuration and program methods of the cell are described. The third application is the study of quantum confinement effects on hole mobility in Ge-channel double gate pMOSFETs. The role of NBTI in high-*k* gate dielectric is also emphasized.

In Chapter 2, the new program disturb in a buried diffusion bit-line SONOS array is investigated. Our characterization shows that the program disturb is 1V, which has been a major issue for the 50nm technology node and beyond. We utilize a multi-step Monte Carlo simulation to explore the disturb mechanism. We find that the threshold voltage shift of a disturbed cell is attributed to impact ionization-generated secondary

electrons in a neighboring cell when it is in programming. The disturb is more serious for the small bit-line width, shallow bit-line junction, and high pocket implant dosage. In addition, we find that optimization of program bias conditions and device structure can alleviate the program disturb.

Proposed in Chapter 3 is a novel hot-electron programming method by means of electron non-equilibrium transport in a buried-diffusion bit-line SONOS memory array. In this method, electron acceleration is achieved in two adjacent cells rather than in a single cell. In this way, the drain-to-source voltage (V_{ds}) in each cell can be reduced to 2.5V, which is immune to channel punch-through. The Monte Carlo simulation similar to that described in Chapter 2 is employed to explore the non-equilibrium transport behavior. Our study shows that the higher programming efficiency in this method than in the conventional method is attributed to the residual energy at the source of the program cell. Furthermore, this method is more effective as bit-line width reduces.

The quantum confinement effects on hole mobility in Ge-channel double gate MOSFETs are studied in Chapter 4. The low-field hole mobility is calculated by a Monte Carlo simulation. Our simulation result shows that the hole mobility in a (100)/[110] silicon well decreases with a decreasing well thickness, which is in agreement with the experimental result. The hole mobility in a Ge-channel pMOSFET, however, exhibits a peak in a sub-20 nm well because of the interplay between intrasubband and intersubband scatterings. The peak mobility in (110)/[-110] channel direction can be also achieved. Moreover, we find that the hole mobility can be further improved when the uniaxial compressive stress is applied to (100)/[110] or (110)/[-110] channel direction.

The characteristic of bipolar charge trapping induced anomalous NBTI in HfSiON gate dielectric pMOSFETs is demonstrated in Chapter 5 by using a fast transient

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Conclusions are finally made in Chapter 6.

Keyword: Monte Carlo simulation, Advanced CMOS, SONOS, NOR, Buried diffusion, Hot-electron programming, Program disturb, Low V_{ds}, Punch-through, Double gate, Ge-channel, Hole mobility, Uniaxial compressive stress, High-*k*, NBTI, Bipolar charge trapping model, Single charge emission, Charge pumping technique

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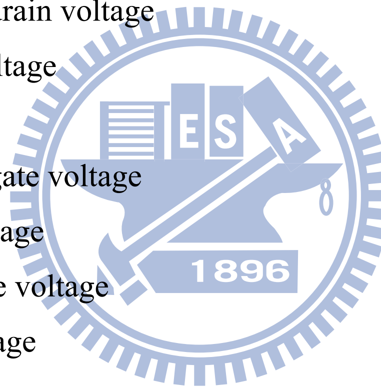
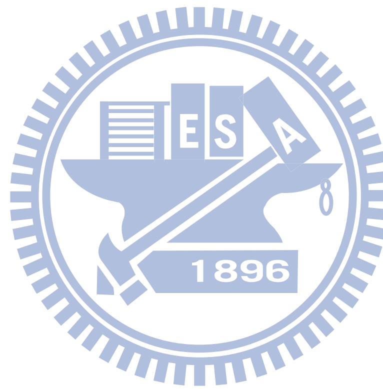
LIST OF SYMBOLS

a_v	Bir-Pikus deformation potential
b	Bir-Pikus deformation potential
C	Elastic stiffness constant matrix
D_{it}	Interace trap density
D_n	Two-dimensional density of hole states in n-th subband
D_tK	Average optical deformation potential
d	Bir-Pikus deformation potential
E_F	Fermi level
E_n	n-th subband energy
E_t	Trap energy (from the conduction band)
E_{ox}	Perpendicular oxide field
f_0	Fermi-Dirac distribution
H	6×6 Hamiltonian
H_k	Luttinger Hamiltonian
H_{mn}	Overlap factor
H_ε	Bir-Pikus Hamiltonian
h_i	Mesh size between adjacent grid points x_i and x_{i+1}
k_B	Boltzmann constant
k_x, k_y, k_z	Wave-vector in x, y, z-direction
I	Identity matrix
I_{cp}	Charge pumping current
I_d	Drain current
$I_{d,lin}$	Linear drain current
$I_{S/D}$	Source/Drain current
I_{sub}	Substrate current
L	Channel length
m_0	Free electron mass
n_{op}	Bose-Einstein distribution
N_{HK}	High-k trap density
N_{inj}	Number of injected hot electrons
p_{inv}	Inversion hole density

q	Elementary charge
x_i	Mesh point at *i*-th grid
S	Elastic compliance constant matrix
S_{ac}^{m}	Acoustic phonon scattering rate in *m*-th subband
S_{op}^{m}	Optical phonon scattering rate in *m*-th subband
T	Lattice temperature
T_{Ge}	Body thickness of a Ge-channel
t_{meas}	Measurement time
t_{stress}	Stress time
u_l	Longitudinal sound veloctiy
W	Channel width
V	Potential energy
V_d	Drain voltage
$V_{d,meas}$	Measurement drain voltage
$V_{d,stress}$	Stress drain voltage
V_g	Gate voltage
$V_{g,meas}$	Measurement gate voltage
$V_{g,stress}$	Stress gate voltage
V_{ds}	Drain-to-source voltage
V_t	Threshold voltage
V_T	Thermal voltage
V_{BL}	Bit-line voltage
V_{WL}	Word-line voltage
$\hbar$	Reduced Planck constant
$\Delta I_{d,lin}$	Change in linear drain current
ΔE_t	Energy range for available dielectric traps
ΔV_t	Change in threshold voltage
α	Coefficient of effective oxide barrier height
β	Coefficient of effective oxide barrier height
ε	Strain tensor
ϕ_B	Effective oxide barrier height
ϕ_{SiO2}	SiO_2/Si conduction band offset
φ	6×1 wave-vector



λ	Split-off energy
ρ	Material density
σ	Stress tensor
$\gamma_1,\gamma_2,\gamma_2$	Luttinger parameter
ω_{op}	Optical phonon frequency
Δ	Average step height
Φ	Wave-function
Λ	Correlation length
Ξ	Effective acoustic deformation potential
$\lvert J, m_J \rangle$	Basis function
$^+$	Operation of complex conjugate



Chapter 1

Introduction

1.1 Backgrounds

Flash memories play an important role in our VLSI industry with their wide applications (see Fig. 1.1). NOR-type flash memory is suitable for code storage applications, such as personal computers, mobile phones. On the other hand, NAND-type flash memory is suitable for data storage applications, such as digital camera. In terms of charge storage devices, two state-of-the-art structures attract great attention. One is floating gate (FG) flash and the other is charge trapping (CT) flash. The major difference in charge loss mechanisms between FG and CT flash devices is that the charge storage media is conductive in FG flash and is non-conductive in CT flash, as illustrated in Fig. 1.2. Recently, considerable research efforts have been made to study the nitride-based, localized charge trapping storage flash memories for its smaller cell size ($2.5F^2$ per bit, where F is the feature size of the process), simpler fabrication process [1.1]-[1.2], the absence of drain turn-on and over-erase [1.3] in comparison with conventional floating gate flash. In a NOR-type SONOS (silicon-oxide-nitride-oxide-silicon) memory, a virtual ground array with n^+ buried diffusion bit-lines is usually implemented to achieve a higher packing density [1.4]. Much attention is particularly paid to its two bits storage capability. The two bits operation can be achieved by placing the programmed charges in the nitride layer locally above the source or drain junction by channel hot electron (CHE) program and band to band hot hole (BTB HH) erase. The reverse-read scheme is used to monitor the threshold voltage window [1.1].

With respect to the advanced CMOS devices, Fig. 1.3 shows the cross sectional images of Intel's state-of-the-art transistors for 65 nm [1.5] and 45 nm technology nodes [1.6],[1.7]. In order to maintain the scaling roadmap, Intel has made a significant breakthrough in solving the gate leakage problem. They replace the SiO_2 with the high permittivity (high-*k*) material, hafnium-based, and replace the polysilicon gate electrode with new metals for the 45 nm technology node (see Fig. 1.3 (b)). The implementation of the high-*k* material is to reduce the gate leakage, and metal gate electrode is to eliminate the poly depletion effect, resolve the threshold voltage pinning effect, and screen soft phonons for improved mobility [1.7]. In Fig. 1.3 (b), advanced strained silicon technologies, such as dual-stress liner [1.8] and embedded SiGe source or drain [1.9], are also incorporated to boost the device performance. Fig. 1.4 shows the roadmap for the future options from Intel's predictions. For the 22 nm technology node and beyond, double-gate metal-oxide-semiconductor field-effect-transistors (MOSFETs) and fin field-effect-transistor have been considered as promising alternatives to bulk MOSFETs [1.0-1.12] due to their immunity to short channel effects. In addition, advanced channel materials with higher carrier mobility than bulk Si, such as Ge [1.13], and III-V materials [1.14], offer potential long term options. The nanowire is under research as well.

1.2 Description of the Problem

As the technology node is scaled down, three major reliability issues in a NOR-type SONOS memory are identified, which may impose new constraints in cell scaling. The first issue is random telegraph signal (RTS). As bit size aggressively shrinks, the number of programmed charges reduces. A single charge

trapping/detrapping will induce a large fluctuation in read current [1.15]. This current fluctuation, referred to as RTS, has become a serious concern in advanced CMOS technologies [1.16] and will cause retention loss tail bits in a SONOS array. Note that this issue is not studied in this dissertation. The second issue is the program disturb. As the technology node advances, the buried diffusion bit-line width is reduced. Previous works have shown that, in channel hot electron program, channel initiated secondary electrons (CHISEL) play an important role in charge injection [1.17]-[1.19]. As a result, impact ionization-generated secondary electrons may flow to a neighboring cell and cause a program disturb, which results in a threshold voltage shift of a neighboring cell. This program disturb will be a bottleneck in cell scaling. The third issue is the channel punch-through leakage. For hot electron program in a NOR-type SONOS memory, a large drain-to-source voltage is usually required for channel electrons to overcome the tunnel dielectric barrier height. In a SiO_2/Si system, the barrier height is 3.1 eV for electron. When the memory cell's gate length is shrunk, the punch-through leakage contributed from the un-selected cells sharing the same bit-line voltage will be significant and limit the cell performance. .

For the 22 nm technology node and beyond, the multiple gate structures and novel channel materials are appreciated due to their immunity to short channel effect and high carrier mobility than Si, respectively. It is also demonstrated that the carrier mobility can be further improved in quantum structure MOSFETs by a subband modulation [1.20],[1.21]. As a consequence, it is of much importance to investigate the transport properties in a quantum structure MOSFET with an advanced channel material.

The program disturb and channel punch-through in a NOR-type SONOS memory are characterized and evaluated by a Monte Carlo simulation. We use a

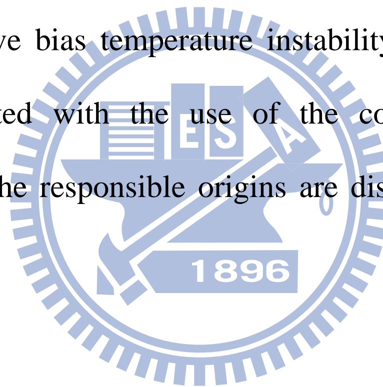
Monte Carlo method to solve the Boltzmann transport equation (BTE) [1.22], which is a very difficult equation to solve numerically or analytically. The Monte Carlo method has the following attributes. It is a stochastic determination. It can be implemented with band structures and scattering processes. Thus, the quantities of physical interest, such as drift velocity, mean free path, and average carrier energy, can be evaluated. Furthermore, the Monte Carlo method is commonly employed to solve BTE in high-field transport conditions, which is suitable for the simulation of impact ionization, substrate current and hot carrier phenomena [1.23],[1.24]. Furthermore, the applications of Monte Carlo simulation are also widely used to solve BTE for the study of inversion carrier mobility in high-*k* [1.25] and strained-Si devices [1.26].

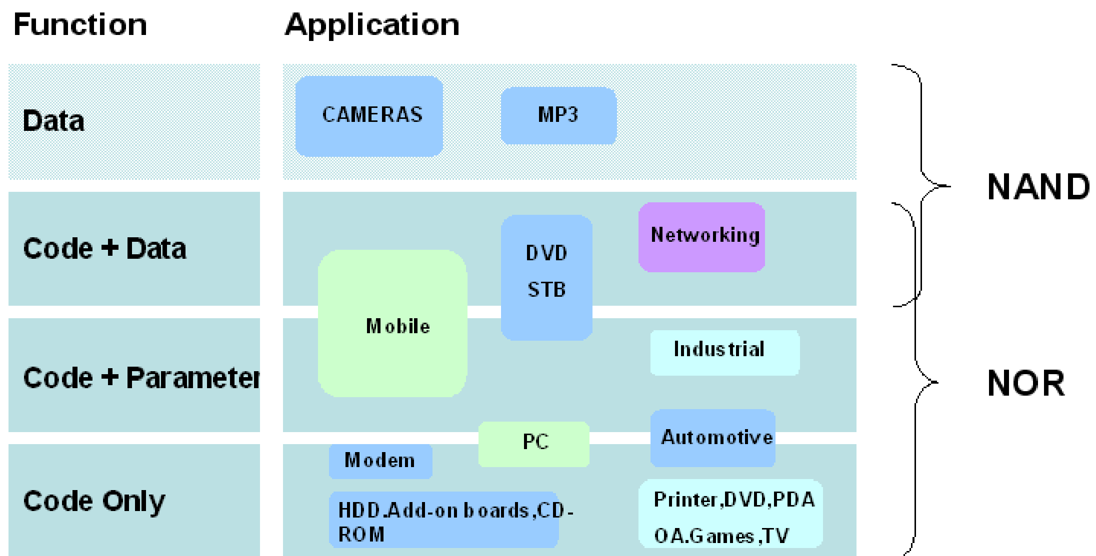
Finally, we will focus on the negative bias temperature instability (NBTI) in high-*k* devices. NBTI has been recognized as a major reliability concern in ultra-thin gate dielectric pMOSFETs [1.27], which is attributed to the interface generation and hole trapping. Compared to a SiO_2 gate dielectric, however, the NBT instability in high-*k* gate dielectric pMOSFETs has been less explored. As a consequence, we employ the fast transient measurement technique [1.28] to minimize a switching delay between "stress and sense" down to μs, and thus reduce the post-stress transient effect due to charge trapping/detrapping in high-*k* gate dielectric.

1.3 Organization of this dissertation

This dissertation consists of six chapters. The scope of the dissertation mainly focuses on the applications of Monte Carlo simulation in advanced CMOS and SONOS flash memory. Following the introduction, the characterization and physical mechanisms of the program disturb in a NOR-type SONOS memory are described in

Chapter 2. The multi-step Monte Carlo simulation is employed to explore this disturb mechanism. Proposed in Chapter 3 is a novel hot electron programming method with a low drain-to-source voltage in a NOR-type SONOS memory. This method has the merit of immunity to channel punch-through. The concept of this method is verified by means of a Monte Carlo simulation. In Chapter 4, we have developed a Monte Carlo simulation including realistic subband structures to simulate the properties of two-dimensional hole transport in Ge-channel double-gate pMOSFETs. The low field hole mobility is calculated by a Monte Carlo simulation. The effects of substrate/channel orientation effects and uniaxial compressive stress on hole mobility are particularly evaluated. In Chapter 5, the characteristic of bipolar charge trapping induced anomalous negative bias temperature instability in HfSiON gate dielectric pMOSFETs is demonstrated with the use of the computer-automated transient measurement system and the responsible origins are discussed. Finally, conclusions are drawn in Chapter 6.





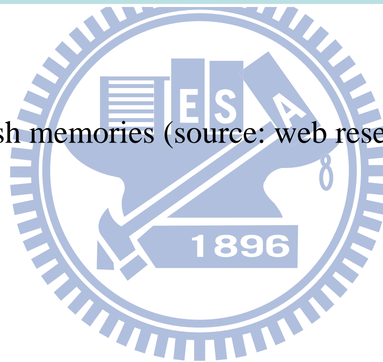

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Fig. 1.1 Applications of flash memories (source: web research feet inc. 2003).

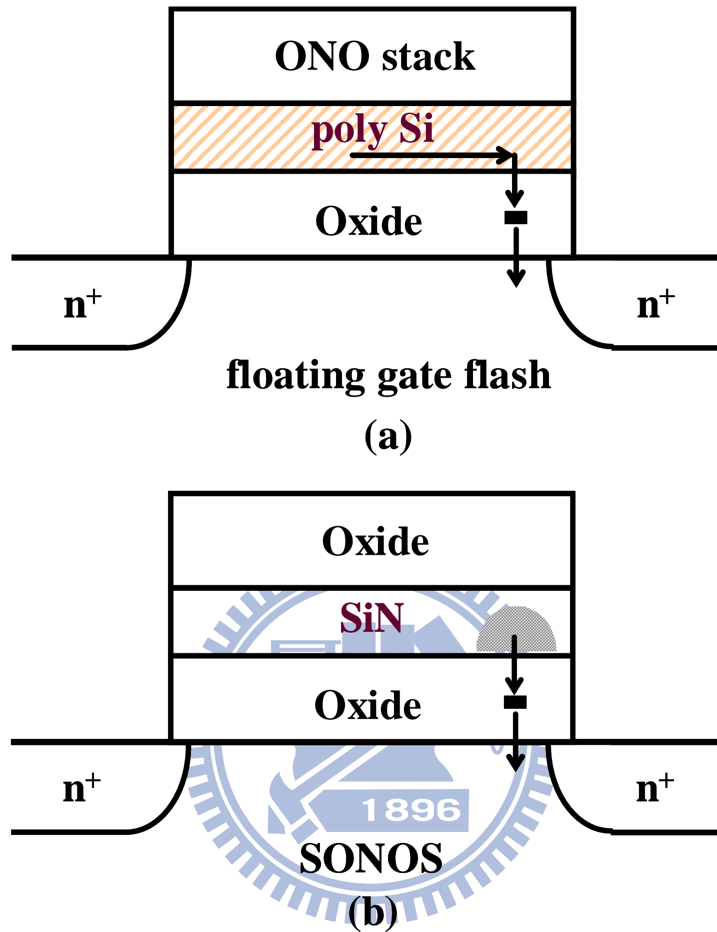


Fig. 1.2 Charge loss via the oxide trap (a) in a floating gate memory and (b) in a SONOS memory.

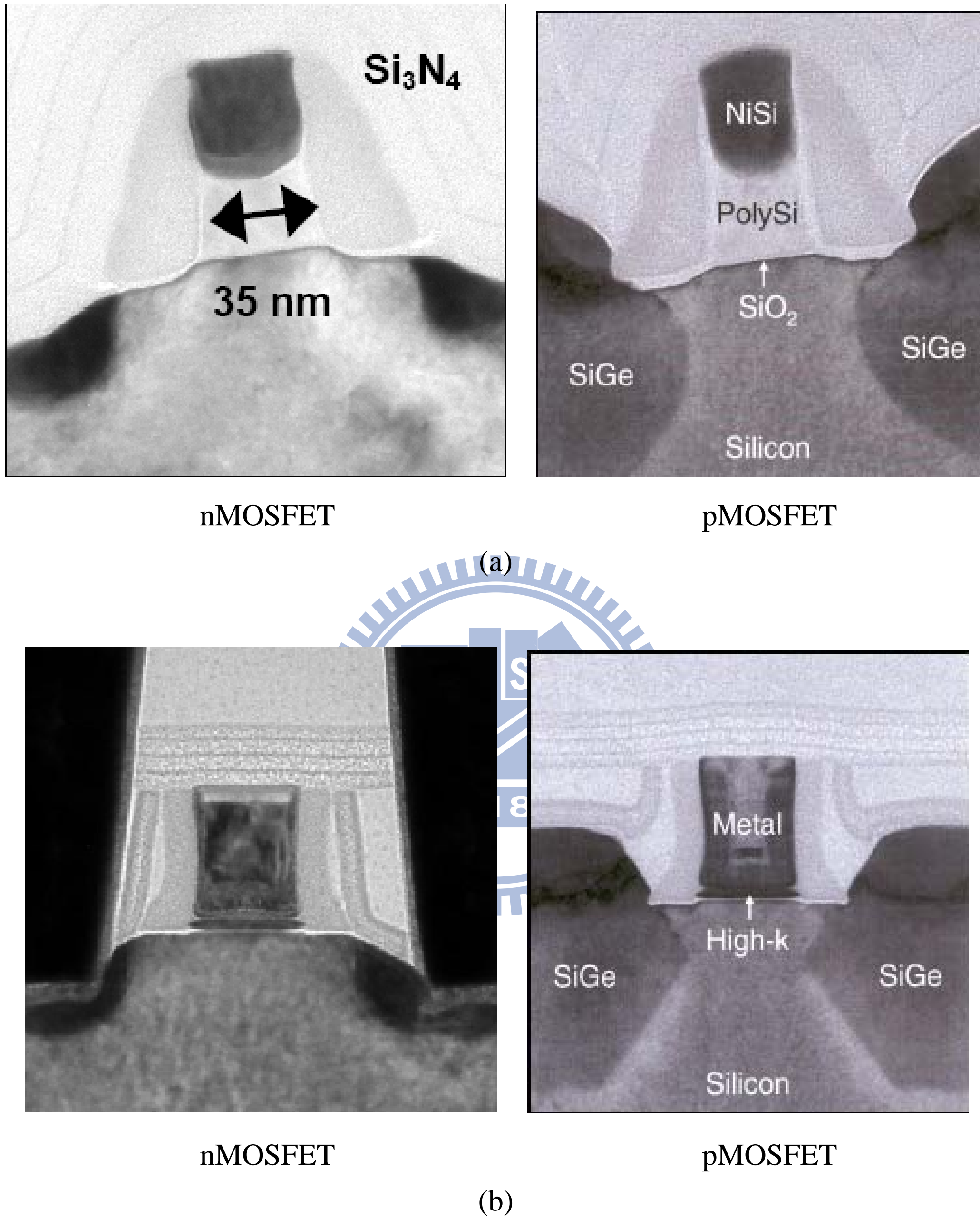


Fig. 1.3 Cross sectional TEM images of the state-of-the-art transistors for (a) 65 nm and (b) 45 nm technology nodes [1.5]-[1.7].

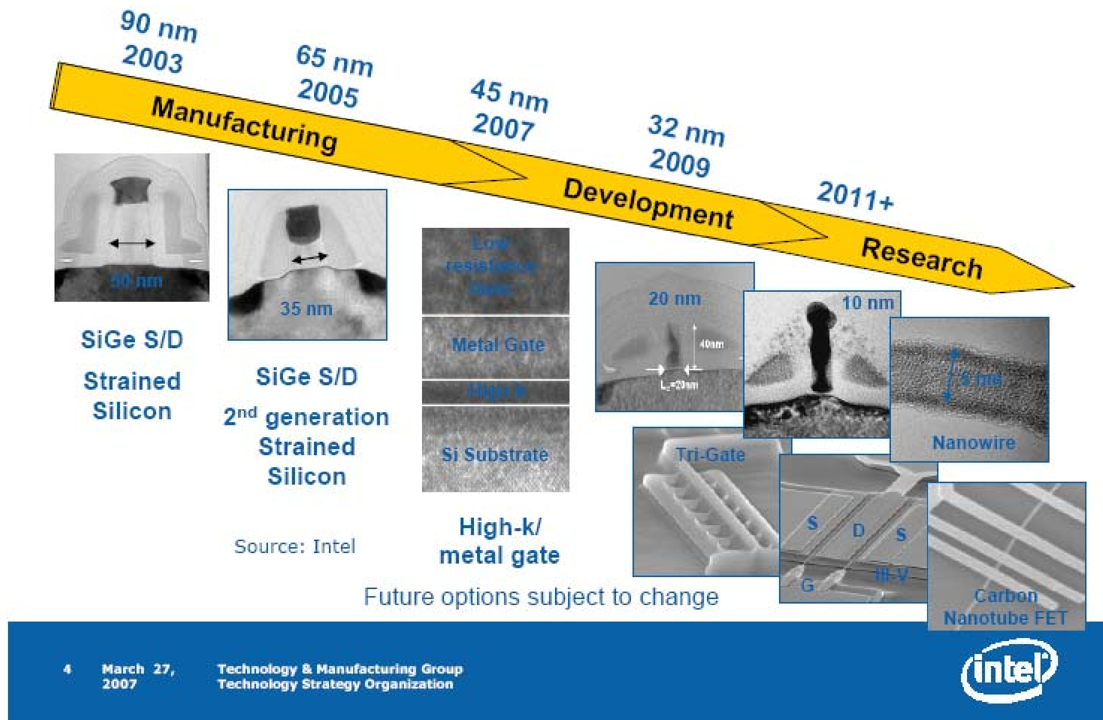


Fig. 1.4 The roadmap for the future options (source: Intel).

Chapter 2

Characterization and Monte Carlo Analysis of Secondary Electrons Induced Program Disturb in a Buried Diffusion Bit-line SONOS Flash Memory

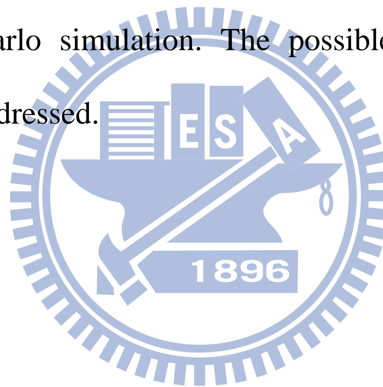
2.1 Preface

Nitride based, localized charge trapping storage flash memory devices have received great interest due to superior performance than conventional floating gate memory devices. Recently, two bits per cell SONOS flash memories by utilizing channel hot electron program and band-to-band tunneling hot hole erase have been demonstrated with good performance and reliability, small die size and low fabrication cost [1.1][1.2]. A virtual ground array with n^+ buried diffusion (BD) bit-lines is implemented to achieve a higher packing density [1.4]. The reliability issues of these memories and their physical mechanisms such as program-state charge loss, erase-state threshold voltage (V_t) drift and read disturb have been addressed in [1.2][2.1]. As the technology node is scaled beyond 50 nm, two new reliability issues due to number fluctuation of stored charges [1.15][2.2] and bit-line scaling are identified, which may impose a new constraint in cell scaling.

First, as bit size aggressively shrinks, the number of programmed charges reduces. A single charge trapping/detrapping will induce a large fluctuation in read current. This current fluctuation, referred to as random telegraph noise, has become a major concern in advanced CMOS technologies [1.16] and will cause retention loss tail bits in a SONOS flash [2.2]. Second, previous studies have shown that, in channel

hot electron program, channel initiated secondary electrons (CHISEL) play an important role in charge injection [1.17]-[1.19]. As a buried diffusion bit-line width is reduced, we find that impact ionization-generated secondary electrons may flow to a neighboring cell and cause a program disturb, as illustrated in Fig. 2.1.

In this work, we first measure the programming characteristics of the programmed cell, i.e. cell (N-1), and the disturbed cell, i.e. cell (N). Then, a multi-step Monte Carlo (MC) simulation is performed to explore the disturb mechanism. The effect of substrate bias on the program disturb is characterized and evaluated by a Monte Carlo simulation to verify the proposed physical mechanism. Furthermore, the effects of bit-line dimension and pocket implant on the program disturb are also discussed by a Monte Carlo simulation. The possible solutions to alleviate the program disturb are also addressed.



2.2 Experimental

2.2.1 Devices

To explore this new failure mode and its impact on bit-line scaling, we fabricate a SONOS mini-array. The SONOS memory cell is fabricated by a standard CMOS process and the gate dielectric is replaced with a nitride trapping layer, sandwiched between two SiO_2 layers. The SONOS cells are processed in a virtual ground array, where bit-lines are n^+ buried diffusions and word-lines are poly stripes. Bit charges are stored in the two sides of a channel to realize two-bit per cell operation. Since there is no field isolation, buried diffusion bit-line array is desirable for a higher packing density. Fig. 2.2 (a) and (b) show the cross section and top view of a buried diffusion bit-line SONOS array, respectively. The BD width in this work is 0.12 μm.

2.2.2 Program Disturb in a NOR-type SONOS Memory

Bit B in cell (N-1) is a programmed bit. Bits C and bit D in cell (N) sharing the same word-line are disturbed bits (see Fig. 2.2 (a)). The program bias voltages are given in Table 2.1, where V_{BL} is the bit-line voltage and V_{WL} is the word-line voltage. During channel hot electron programming, the V_{WL} is 9V, the $V_{BL(N-1)}$ and $V_{BL(N)}$ are 0V and 4.2V respectively while $V_{BL(N+1)}$ is kept floating. Fig. 2.3 measures the V_t evolutions of two neighboring cells during programming for two different BD width splits. A reverse-read scheme with a bit-line voltage of 1.6V is employed [1.1]. It is obvious that for a larger bit-line width, i.e. 0.25 μm, no program disturb is observed. However, for a 0.12 μm bit-line width, a significant program disturb (ΔV_t of bits C and D) is observed. As a consequence, this program disturb will become a new constraint in bit-line scaling. In addition, it is found that the program disturb is apparently more serious for a larger program window.

2.2.3 Mechanisms for the Program Disturb

Two possible mechanisms for the program disturb are illustrated in Fig. 2.4. One is secondary electron generation by impact ionization. In channel hot electron programming, channel electrons gain energy from a large electric field. These high energy electrons induce a first impact ionization near the drain junction and then the generated holes are accelerated by the large drain-to-substrate voltage. The hot holes induce a second impact ionization and generated secondary electrons may flow to a neighboring cell, i.e. disturbed cell, and cause a program disturb. The other possible mechanism is substrate electron generation via re-absorption of channel hot electron emitted light. The main cause of the program disturb will be identified later.

2.3 Monte Carlo Model

A multi-step Monte Carlo simulation similar to that described in [2.3][2.4] is used to explore the program disturb mechanism, as illustrated in Fig. 2.5. The Monte Carlo simulation is performed in the frozen-field approximation [1.23]. The electric field is never updated to reflect the dynamics of the carriers. In other words, the electric field obtained from the two-dimensional device simulator is not calculated self-consistently with the Monte Carlo solution of Boltzmann transport equation. The validity of this nonself-consistent approach has been performed in [2.5], which can be used for hot carrier simulation. This is because the substrate current contributes little to the total current in the channel. It should be noted that the nonself-consistent approach reduces the CPU time without sacrificing too much accuracy.

Then, the electric field distribution in cell (N-1) and cell (N) is firstly obtained from a two-dimensional device simulator, Medici [2.6]. The hydrodynamic model, which takes into account the average carrier energy, should be used. The Monte Carlo simulation includes a full band structure for the high energy simulation. A pseudo-potential model [2.7] and a bond-orbital model [2.8] are used to calculate the conduction band-structure and the valence band-structure, respectively. The energy dispersions are drawn in Fig. 2.6 (a). The scattering mechanisms in the simulation include acoustic phonon scattering, optical phonon scattering and impact ionization. The impact ionization rate is calculated by Keldysh's empirical model [2.9]. The band structure and carrier scattering parameters were calibrated in our earlier papers [2.10][2.11]. In a Monte Carlo window, as marked in Fig. 2.6 (b), both electron and hole Monte Carlo simulations are performed. The Monte Carlo window consists of two neighboring cells that both programmed bit and disturbed bits are included. Then, electrons are launched at the source of a programmed cell. The launched electrons

have a room temperature and a Maxwell-Boltzmann distribution in energy. The lower and upper surfaces of the Monte Carlo window are treated as reflective boundaries. Each electron or hole is simulated until it either produces an impact ionization event or passes out of the Monte Carlo window. When an impact ionization event takes place, the energy of each electron or hole minus the band-gap energy is shared by the three created secondaries. Moreover, the hot electron injection is simulated by counting the electrons hitting the Si and SiO_2 interface with energy larger than the effective barrier height.

2.4 Results and Discussions

2.4.1 Spatial Distribution of Secondary Hot Electrons

A multi-step Monte Carlo simulation is performed at a program condition of V_{WL}=9V and $V_{BL(N)}$=4.2V. First, electrons are launched at the source in cell (N-1) and primary impact ionization events are simulated (Fig. 2.7 (a)). It is obvious that most of primary impact ionization events take place near the drain junction where the lateral electric field is the largest. In the second step, holes are launched at primary impact ionization sites and secondary impact ionization events are simulated (Fig. 2.7 (b)). It is found that the secondary impact ionization region extends into the substrate. In the third step, electrons are launched at the secondary impact ionization sites and hot electron injection into both cell (N-1) and cell (N) is simulated (Fig. 2.7 (c)). A random sample of 50 impact ionization events is chosen in Fig. 2.7 (a) and (b). A random sample of 500 secondary hot electrons with energy above 2.6 eV is displayed in Fig. 2.7 (c). It is found that Fig. 2.7 (c) confirms the flowing of some secondary electrons into cell (N), which is the cause of the program disturb.

To gain insight into the program disturb path, the Monte Carlo simulated

trajectories of secondary electron injection are shown in Fig. 2.8. For path 1, a generated secondary electron injects into the nitride of cell (N-1), resulting in the increase of V_t (bit B) in Fig. 2.3 (b). For path 2, a generated secondary electron goes around the n^+ buried diffusion junction and injects into cell (N), resulting in the increase of V_t (bit C) or V_t (bit D) in Fig. 2.3 (b).

2.4.2 Energy Distribution of Secondary Hot Electrons

Fig. 2.9 shows the simulated electron energy distributions in a programmed cell and a disturbed cell. In a programmed cell, electrons near the drain side (bit B) and near the source side (bit A) are collected separately. As shown in the figure, the bit A follows approximately a Boltzmann distribution. However, the bit B has an apparent high energy tail due to non-equilibrium transport in the high field region. The high energy tail includes both primary hot electrons and secondary hot electrons (see Fig. 2..4). It should be pointed out that the secondary hot electrons (CHISEL) become dominant for energy above 2.6 eV. On the other hand, in a disturbed cell, only secondary hot electrons in the entire channel are accumulated.

A flow chart for the simulation of hot electron injection is shown in Fig. 2.10. According to [2.12], the effective barrier height, ϕ_B, is expressed as

$$\phi_B = \phi_{SiO_2} - \alpha E_{ox}^{2/3} - \beta E_{ox}^{1/2}$$

The effective barrier height is lowered after taking into account tunneling (α=1.0x10^{-5}(Vcm^2)$^{1/3}$) and image force (β=2.59x10^{-4}(Vcm)$^{1/2}$). E_{ox} is the perpendicular oxide field and ϕ_{SiO2} is set to be 3.1 eV. Then, the number of injected hot electrons, N_{inj}, can be calculated by counting electrons hitting the SiO_2 and Si

interface with energy above the effective barrier height. Fig. 2.11 shows the effective barrier height as a function of programmed bit ΔV_t for two programming word-line voltages. Two points are worth noting. First, as programmed bit ΔV_t raises, the effective barrier height increases due to the build-up of program charges in the nitride layer. As a result, in the initial stage of programming, CHE injection is dominant. Then, due to the decrease of CHE significantly during programming, CHISEL injection then becomes dominant. Second, for a larger programming word-line voltage, i.e. V_{WL}=10.5V, CHE is more dominant in the programming transient and the role of CHISEL is played down, which implies that the program disturb can be alleviated by an appropriate program bias optimization.

We re-plot Fig. 2.3 (b) to Fig. 2.12 (a). Two-stage behavior is observed. In the initial stage of programming, the program disturb is negligible. The charge injection rate in the programmed cell is larger than that in the disturbed cell. The reason is that CHE is dominant in this stage. However, the disturbed bit ΔV_t increases drastically for a program bit ΔV_t above 3.0V. The reason is that CHISEL becomes dominant in this stage. Fig. 2.12 (b) shows the normalized N_{inj} in the disturbed cell during programming from a Monte Carlo simulation. A similar trend from the measurement and simulation is obtained.

After taking into account an electron energy distribution from the Monte Carlo simulation and the effective barrier height, the spatial distribution of N_{inj} in the programmed cell and in the disturbed cell is shown in Fig. 2.13 and Fig. 2.15, respectively, at a program level of 3.0V, i.e. ΔV_t(bit B)=3.0V. In the programmed cell, the injected charges have a tight distribution near the drain, as shown in Fig. 2.13. The injected charge also affects the threshold voltage of bit A, which is referred to as second bit effect [2.13]. It is found that CHISEL broadens the injected charge

distribution, and thus has an adverse effect on the second bit effect. In other words, the ΔV_t(bit A) increases in the programming transient, as shown in Fig. 2.14. Unlike in a programmed cell, however, Fig. 2.15 shows that the injected charges in the disturbed cell spread over the entire channel, that both bits C and D are affected, which is consistent with the experimental result in Fig. 2.12 (a). Furthermore, a larger threshold voltage shift in bit C than in bit D can be realized due to an asymmetrical injected charge distribution towards bit C.

2.4.3 Substrate Bias Effect

The substrate bias effect on the program disturb is characterized in Fig. 2.16 (a). A negative substrate bias in programming enhances the program disturb. The reason is that a negative substrate bias increases the drain-to-substrate voltage drop, which results in an increase of impact ionization events. The trend is also verified by a Monte Carlo simulation in Fig. 2.16 (b). In addition to impact ionization, Fig. 2.17 demonstrates that the substrate bias has a negligible effect on hot electron radiation [2.14], which implies that substrate electron generation via re-absorption of hot electron emitted light should not be a dominant mechanism in the program disturb.

Furthermore, the Monte Carlo simulation shows a broader injected charge distribution in the programmed cell when a negative substrate bias is applied, as shown in Fig. 2.18, which would result in a worsened second bit effect.

2.4.4 Bit-line Depth and Width Effects

The cell or bit-line scaling effects on the program disturb are also evaluated by a Monte Carlo simulation. For cell scaling, a shallower junction depth is required to reduce the short channel effect. A random sample of 500 secondary electrons with

energy above 2.6eV is drawn in Fig. 2.19 (a) to represent the spatial distributions for two bit-line depth splits. It is found that a shallower BD junction aggravates the program disturb because the secondary electrons have a larger chance to go around the BD bit-line. The simulated N_{inj} versus bit-line junction depth is also shown in Fig. 2.19 (b). Nevertheless, it is possible that the program disturb can be reduced in a recessed buried source/drain SONOS memory.

On the other hand, the Monte Carlo simulation shows a strong dependence on a BD bit-line width in Fig. 2.20. The program disturb is more serious in a narrow BD bit-line because secondary electrons have a larger chance to go around the BD bit-line. The N_{inj} in the disturbed cell increases by two orders as a bit-line width reduces from 0.25μm to 0.1μm. As a consequence, the program disturb becomes a new constraint as the cell/ bit-line scaling advances.

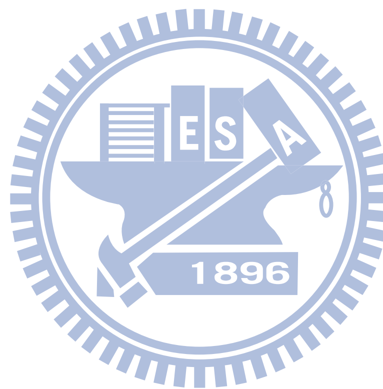
2.4.5 Pocket Implant Effect

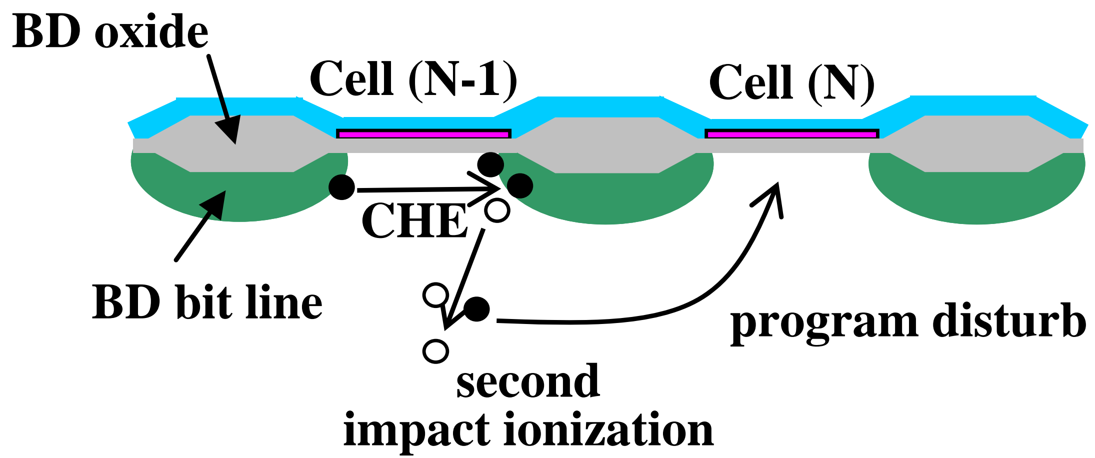
In Fig. 2.21, we evaluate the effect of pocket implant on the program disturb. The dosages of two pocket implant splits differ by two times. It is found that, for a higher pocket dose, the secondary impact ionization events increase (i.e. CHISEL increase) due to a larger substrate field, which leads to a larger program disturb. Therefore, it appears that there is a trade-off between the bulk punch-through and the program disturb.

2.5 Summary

In this work, a new program disturb in a scaled BD bit-line SONOS array is demonstrated. Our Monte Carlo simulation confirms that the program disturb is attributed to the impact ionization-generated secondary electrons flowing to a

neighboring cell. This program disturb becomes more serious as cell or bit-line scaling advances. The factors affecting the program disturb are summarized in Table 2.2. The characteristics of the program disturb can be well simulated by a Monte Carlo code. Optimization of pocket implant, bit-line geometry and program bias conditions can alleviate this program disturb. The program disturb is one of the main bottlenecks for the scaling of NOR-type flash memory.





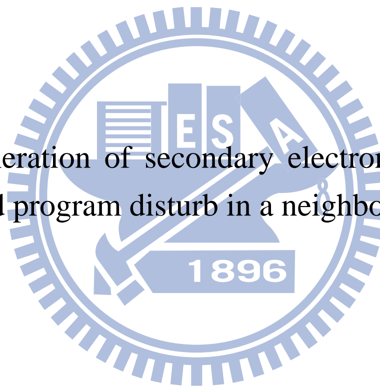
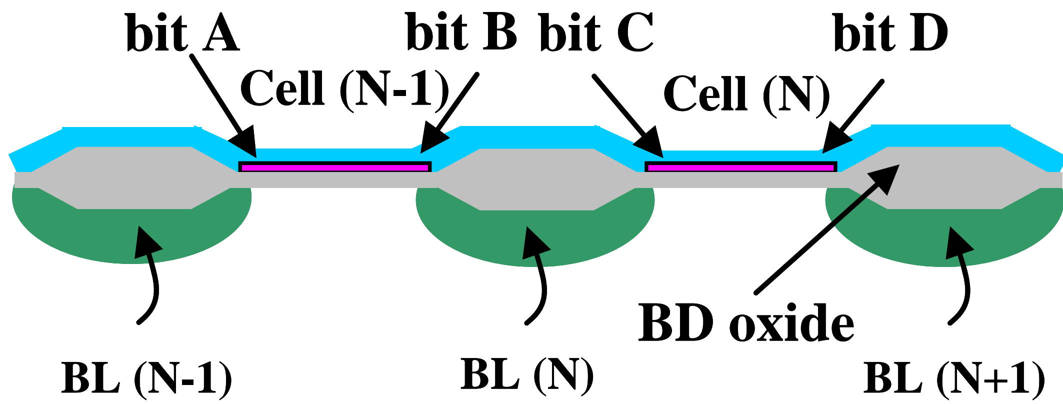


Fig. 2.1 Illustration of generation of secondary electrons by impact ionization and secondary electrons induced program disturb in a neighboring cell.



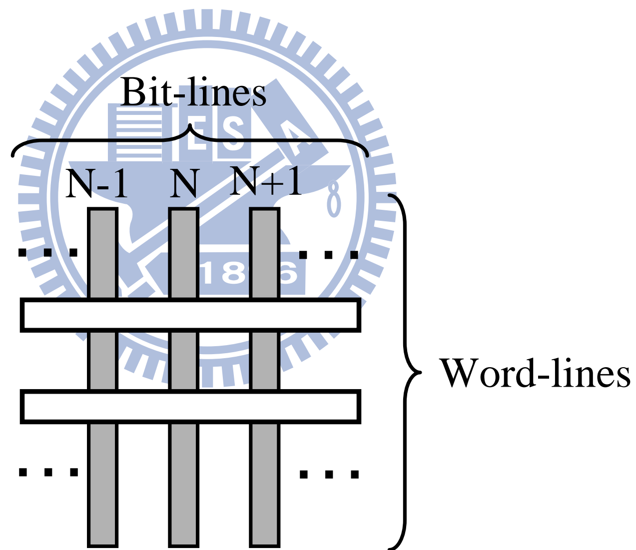
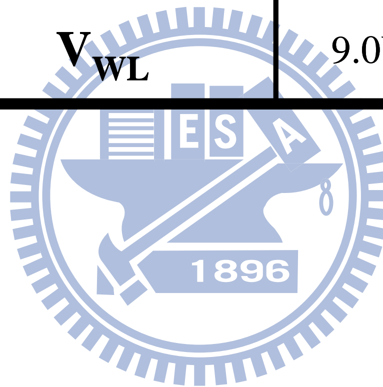
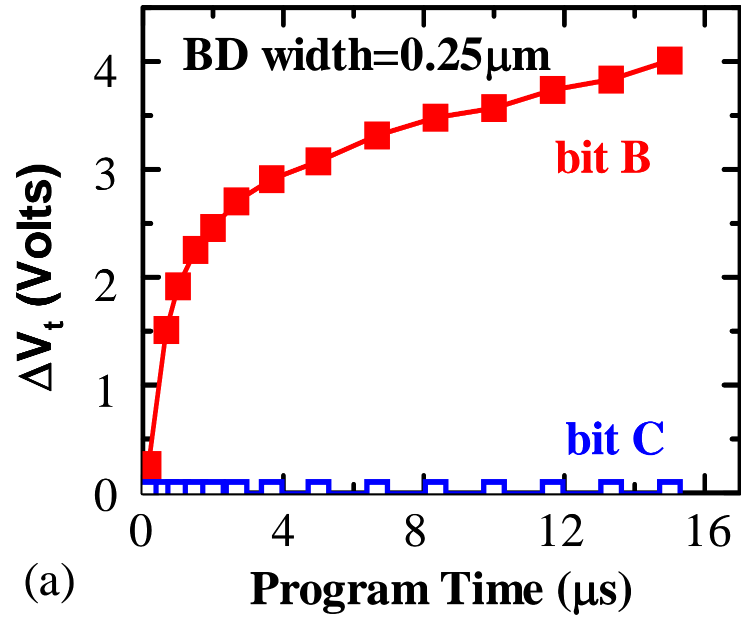


Fig. 2.2 (a) Top view and (b) cross-section of a buried diffusion bit-line SONOS array. The BD width is 0.12 μm in this work.

Table 2.1 Program bias voltages. V_{BL} is the bit-line voltage and V_{WL} is the word-line voltage.

$V_{BL(N-1)}$	0V
$V_{BL(N)}$	4.2V
$V_{BL(N+1)}$	Floating
V_{WL}	9.0V





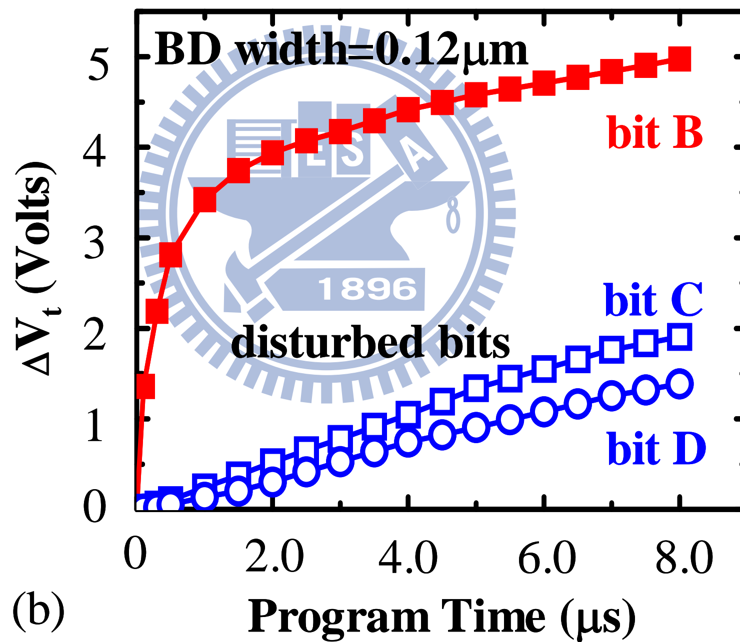


Fig. 2.3 Threshold voltage shifts versus programming time. Bit B in cell (N-1) is a programmed bit, and bits C and bit D in cell (N) are disturbed bits. A reverse read with a bit-line voltage of 1.6V is employed. The bit-line width splits used in this work are (a) 0.25μm and (b) 0.12μm, respectively.

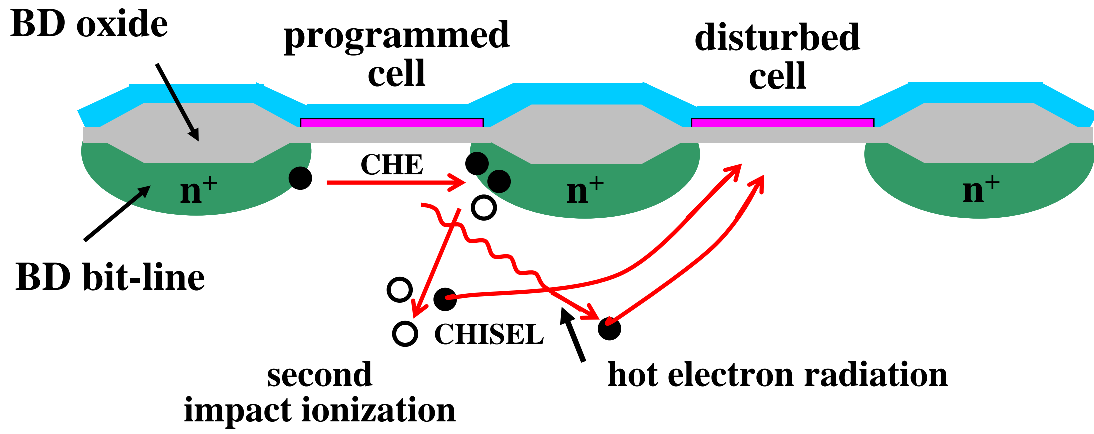


Fig. 2.4 Two possible mechanisms for the new program disturb.

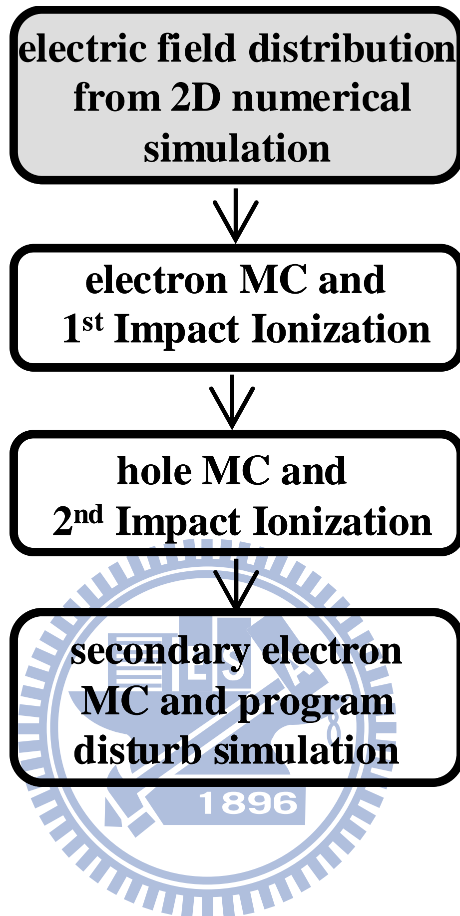


Fig. 2.5 Three-step Monte Carlo simulation flow using both electron and hole Monte Carlo codes to simulate secondary hot electrons.

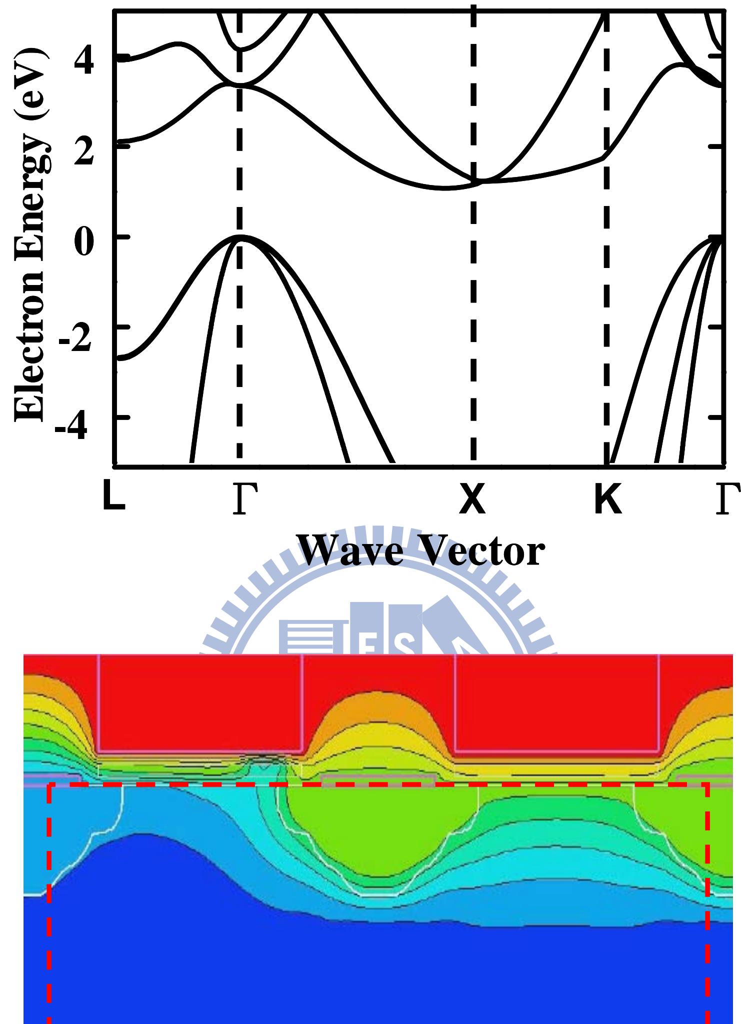


Fig. 2.6 (a) E-*k* relation used in the Monte Carlo simulation. A pseudo-potential model and a bond-orbital model are used to calculate the conduction band and the valence band structure, respectively. (b) Monte Carlo window includes both a programmed cell and a disturbed cell. The electric field distribution during programming is shown.

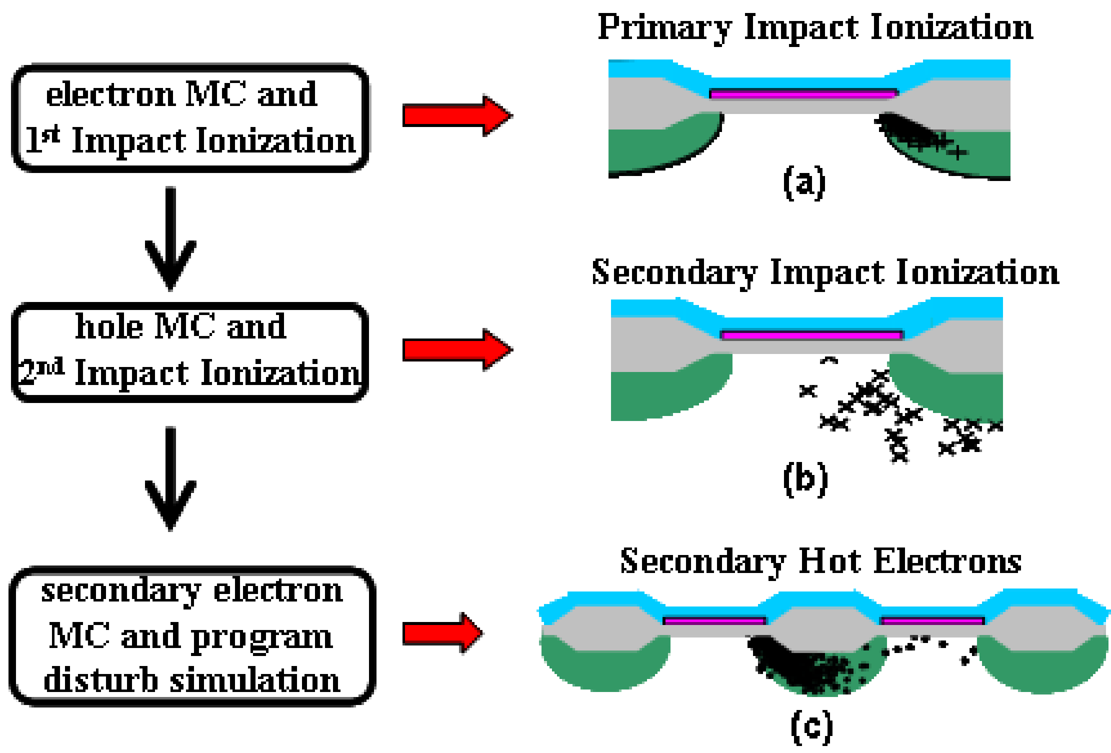


Fig. 2.7 (a) A random sample of 50 primary impact ionization events (denoted by ＋) from the first step MC simulation. (b) A random sample of 50 secondary impact ionization events (denoted by ⨯) from the second step MC simulation (c) A random sample of 500 secondary electrons (denoted by •) with energy above 2.6eV from the third step MC simulation.

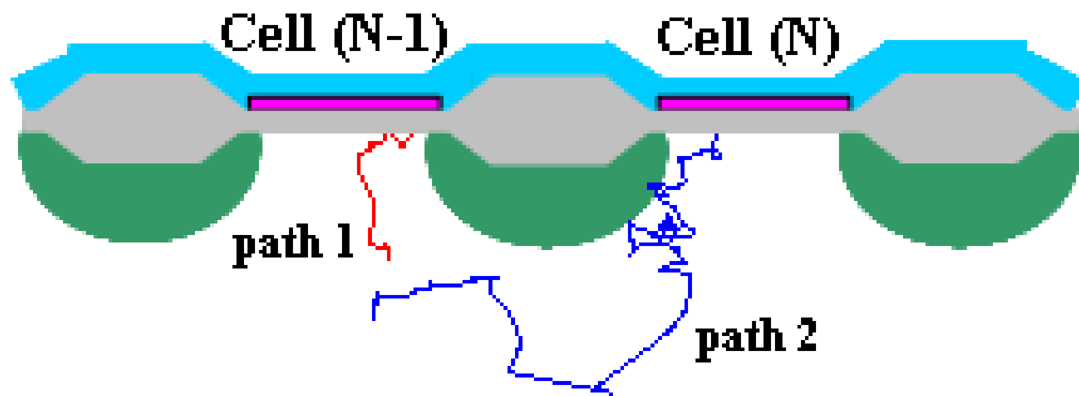


Fig. 2.8 Monte-Carlo simulated trajectory of secondary hot electron injection.

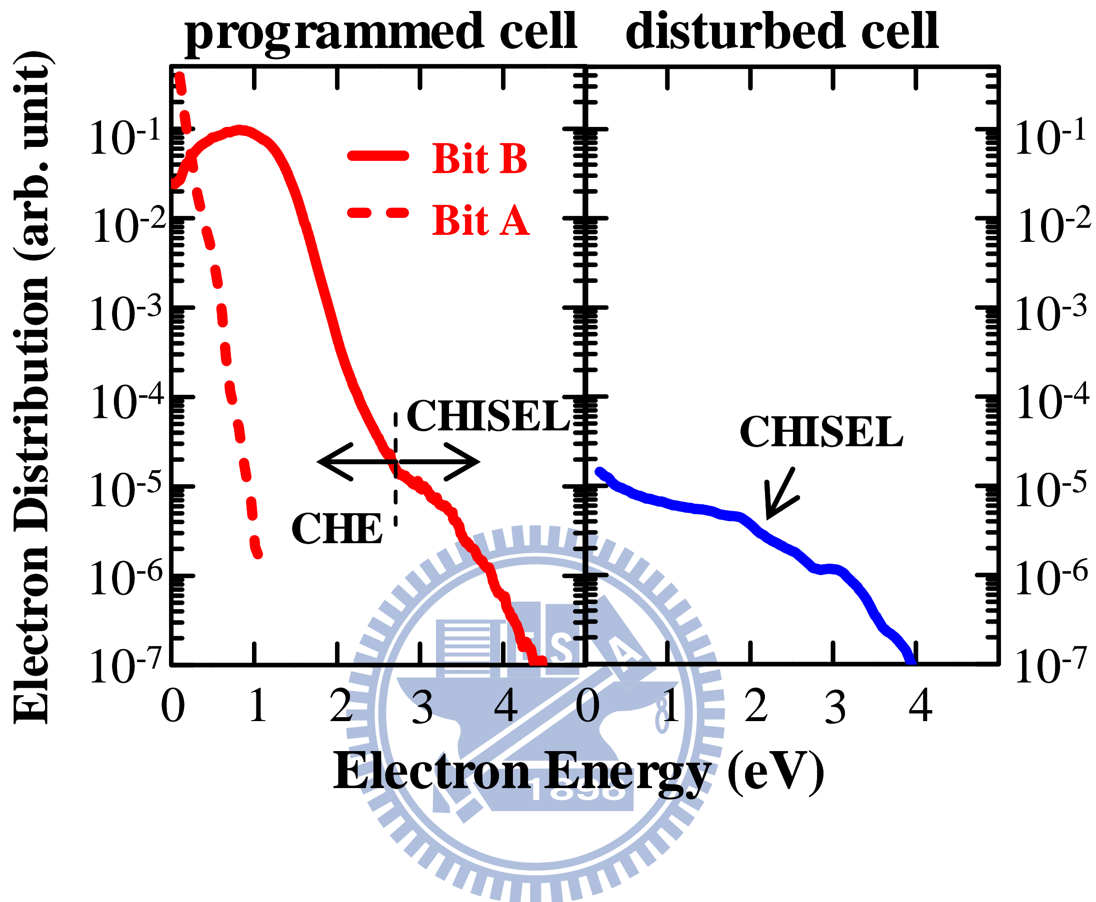


Fig. 2.9 Electron energy distributions in a programmed cell (a) and in a disturbed cell (b). In a programmed cell, electrons near the drain (bit B) and near the source (bit A) are collected separately. Both primary and secondary electrons are counted. In a disturbed cell, secondary electrons in the entire channel are accumulated.

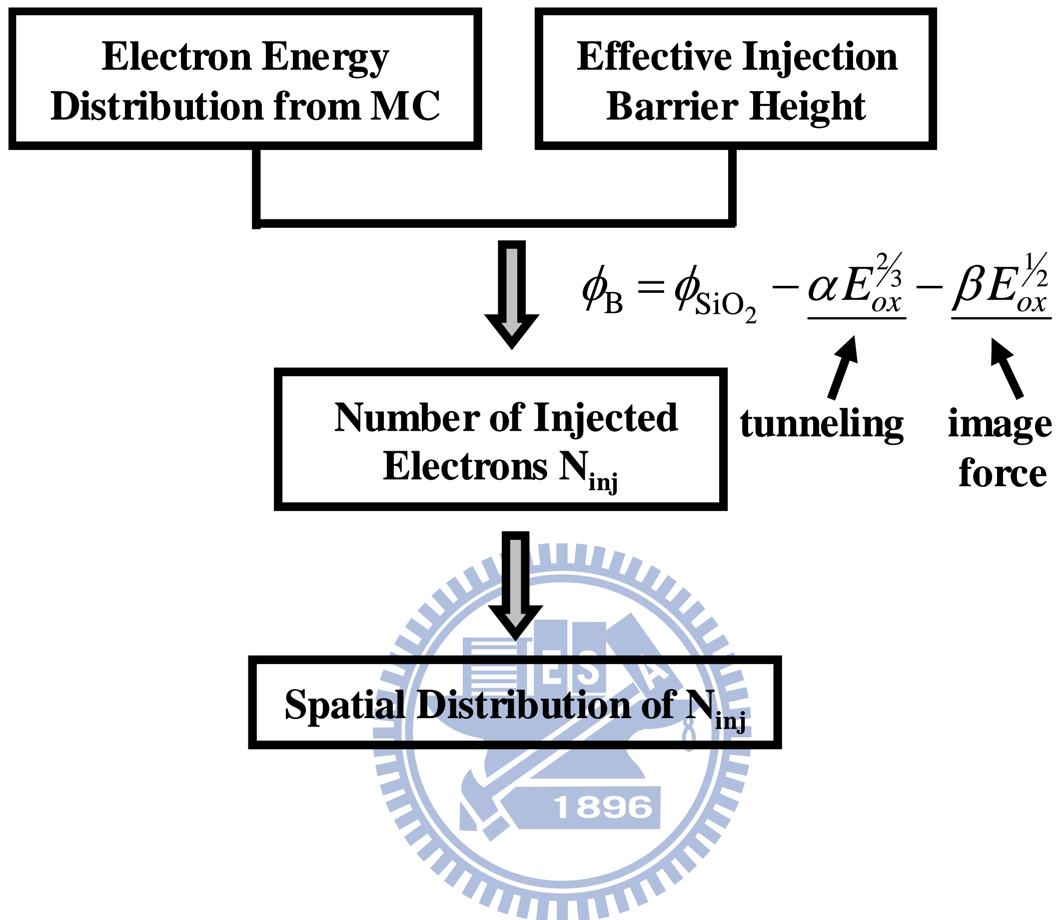


Fig. 2.10 Simulation flow of hot electron injection.

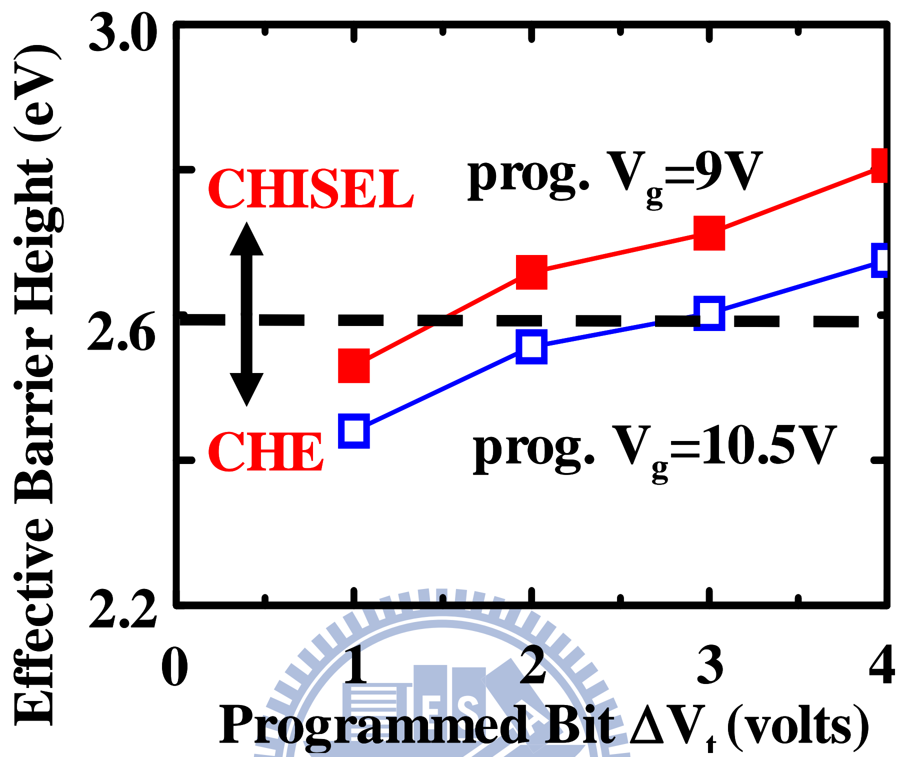


Fig. 2.11 Programmed bit ΔV_t dependence on the effective barrier height. The two program word-line voltages are compared. CHISEL is dominant for energy above 2.6eV.

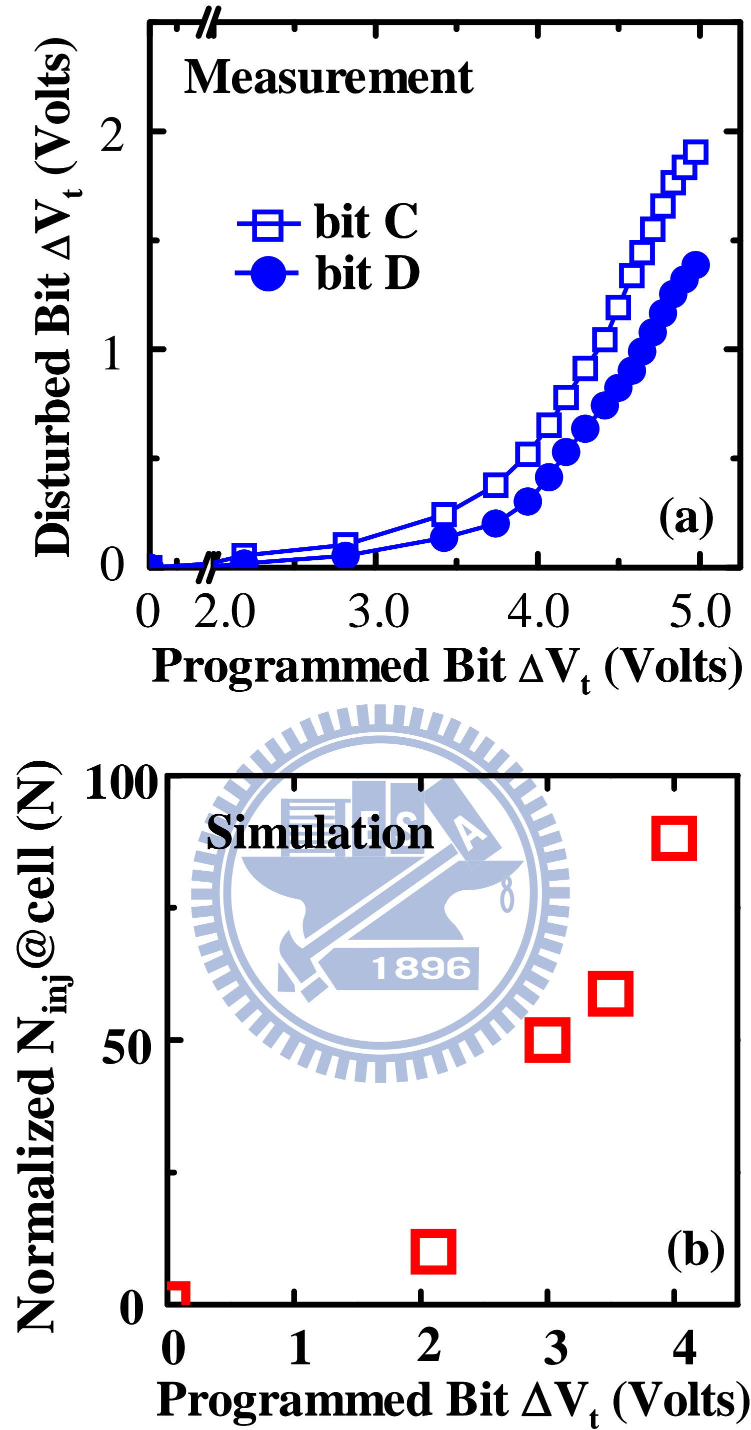


Fig. 2.12 (a) Disturbed bit ΔV_t versus programmed bit ΔV_t from measurement. (b) Normalized charge injection in cell (N) versus programmed bit ΔV_t from Monte Carlo simulation. Two-stage behavior is observed.

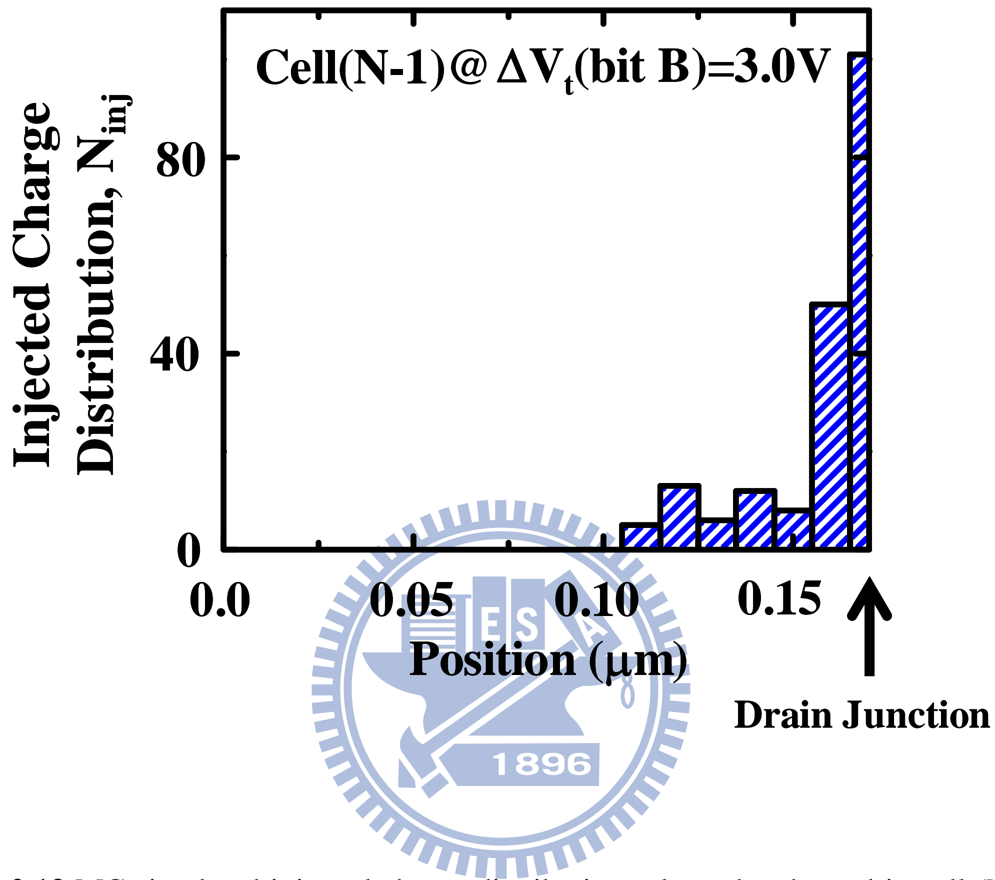


Fig. 2.13 MC-simulated injected charge distributions along the channel in cell (N-1). The effective oxide barrier height in cell (N-1) is calculated for ΔV_t(bit B)=3.0V.

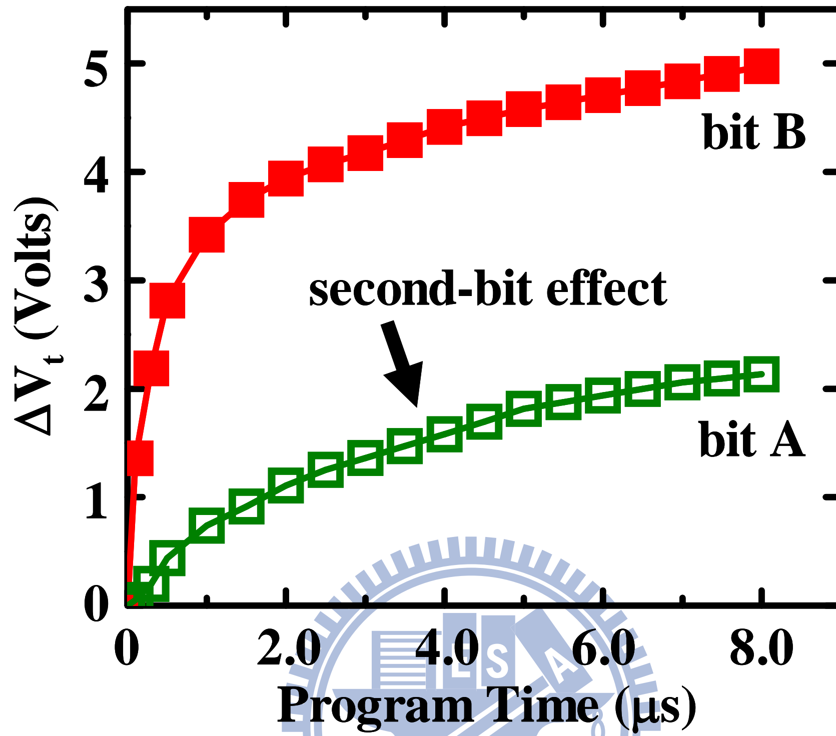


Fig. 2.14 ΔV_t of bit B and bit A during programming.

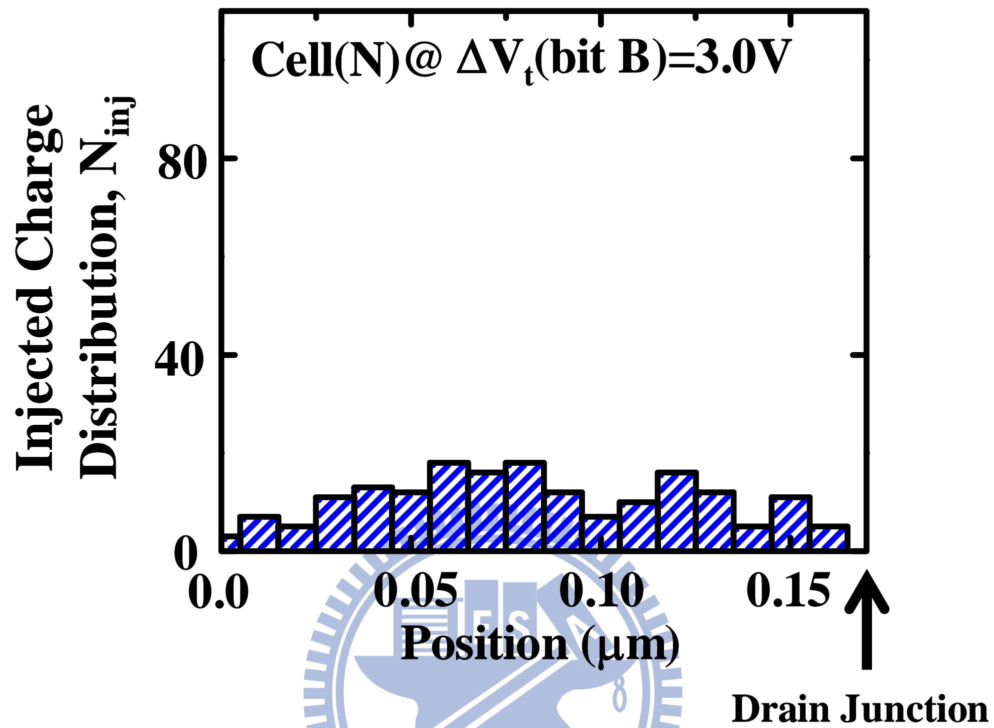


Fig. 2.15 MC-simulated injected charge distributions along the channel in cell (N). The effective oxide barrier height in cell (N) is calculated for ΔV_t(bit B)=3.0V.

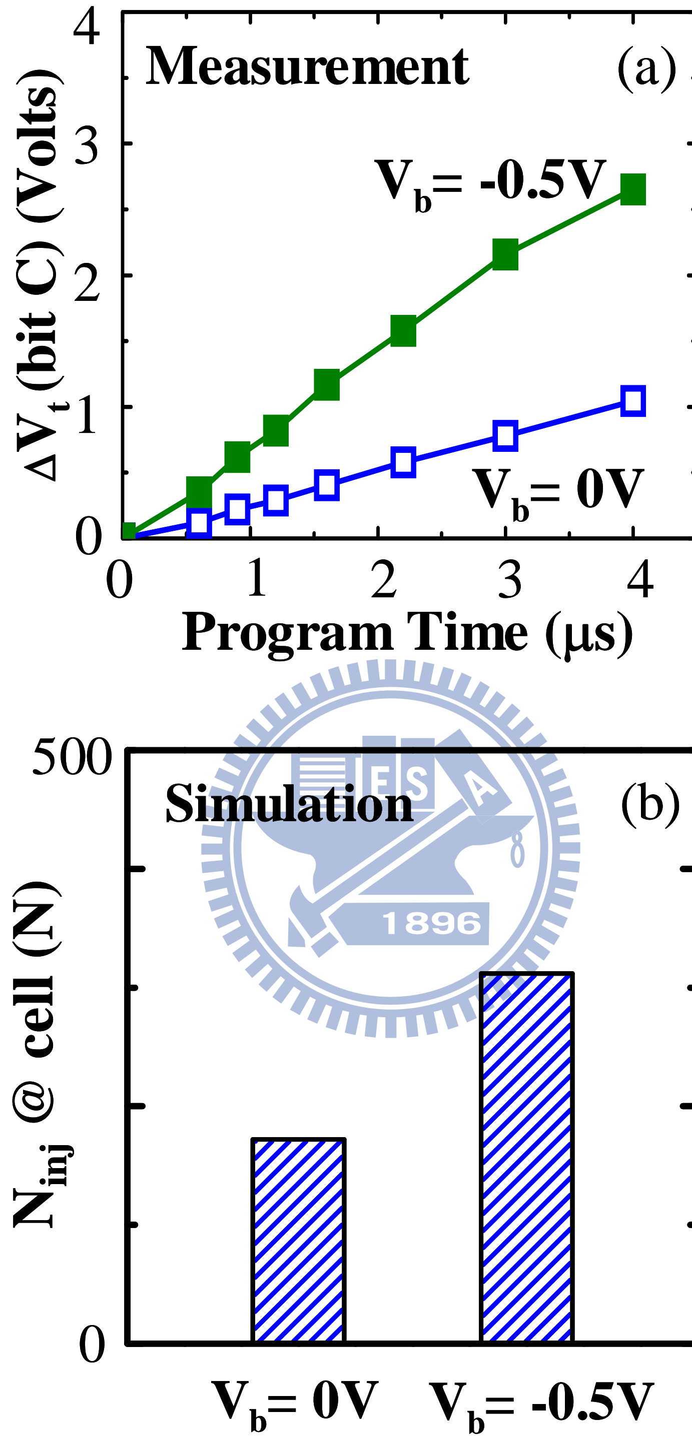


Fig. 2.16 (a) Measured substrate bias (V_b) effect on the program disturb, ΔV_t(bit C) versus program time, and (b) simulated N_{inj} in cell (N), for V_b=0V and -0.5V.

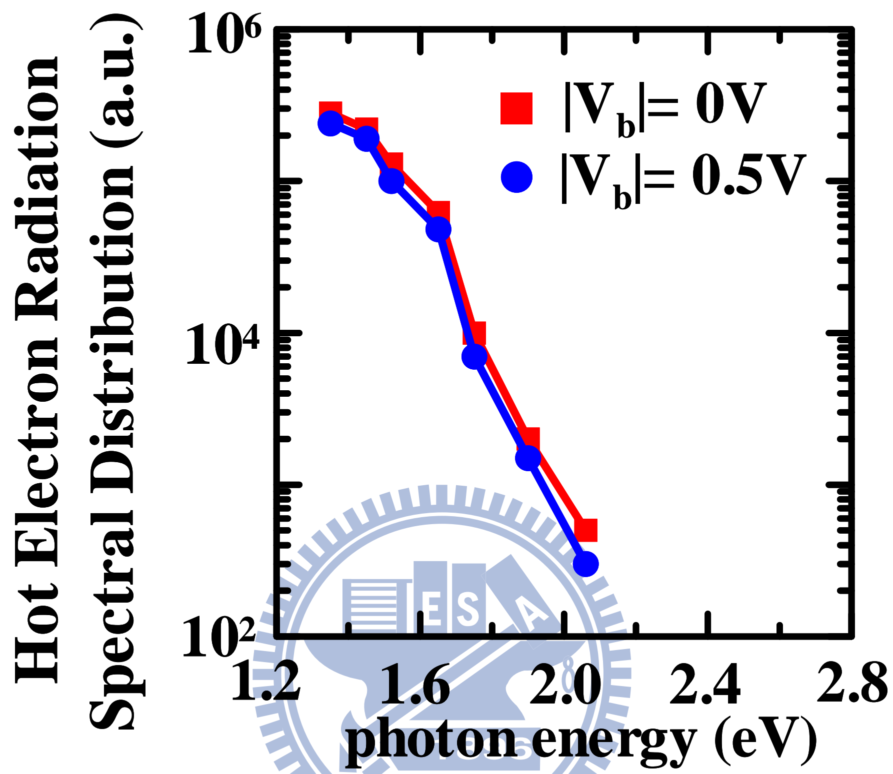


Fig. 2.17 Dependence of hot electron light emission spectrum on substrate bias in a nMOSFET [2.14].

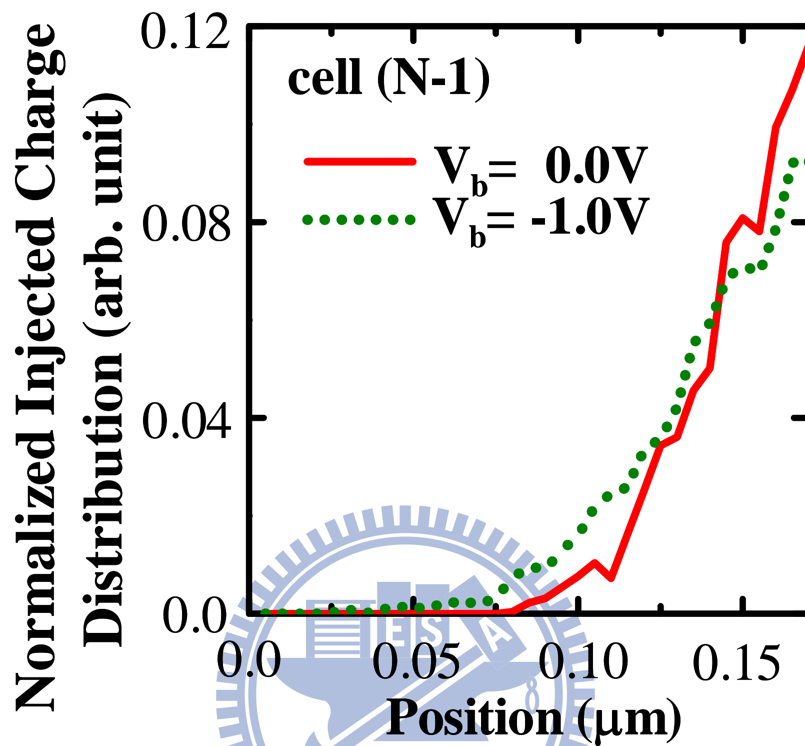
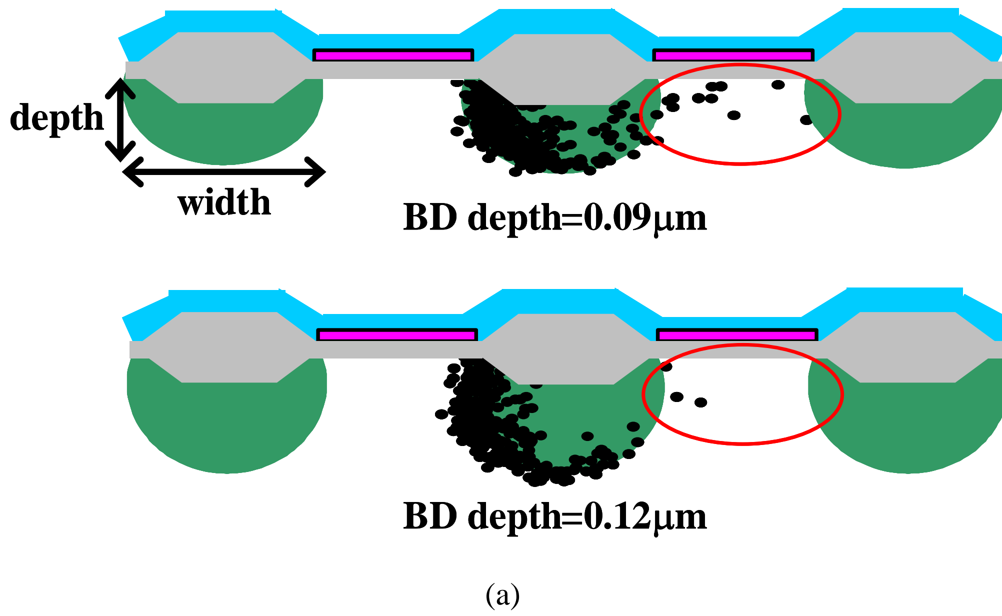
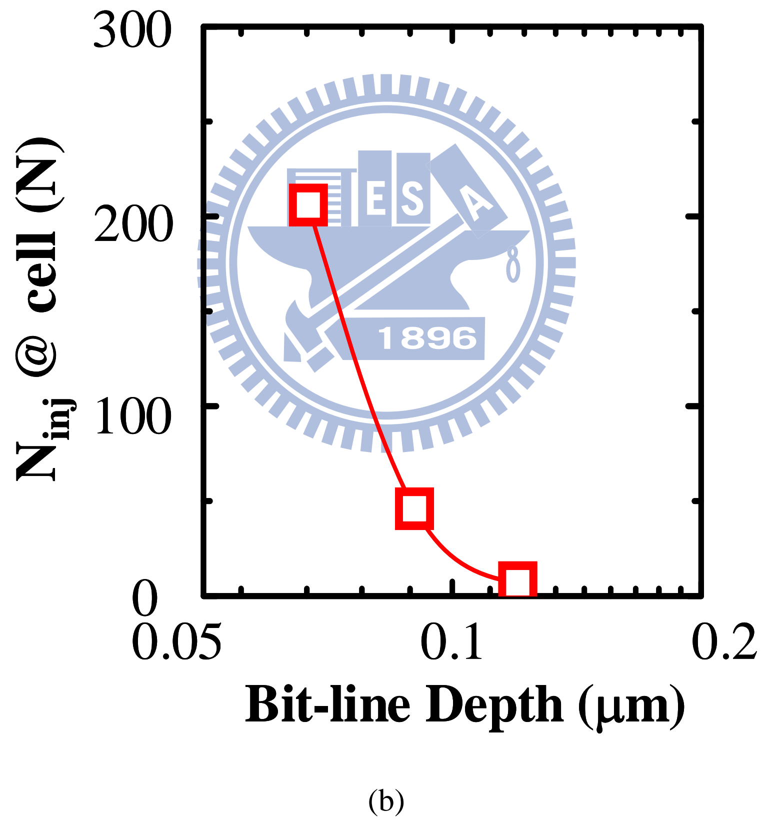


Fig. 2.18 Normalized injected charge distributions along the channel for V_b=0V and -1.0V. The V_b= -1.0V has a broader distribution due to secondary electron injection.



(a)



(b)

Fig. 2.19 (a) Simulated spatial distribution. A random sample of 500 secondary electrons with energy above 2.6eV is drawn. (b) Dependence of the program disturb on BD bit-line junction depth, N_{inj}(cell (N)) versus bit-line depth.

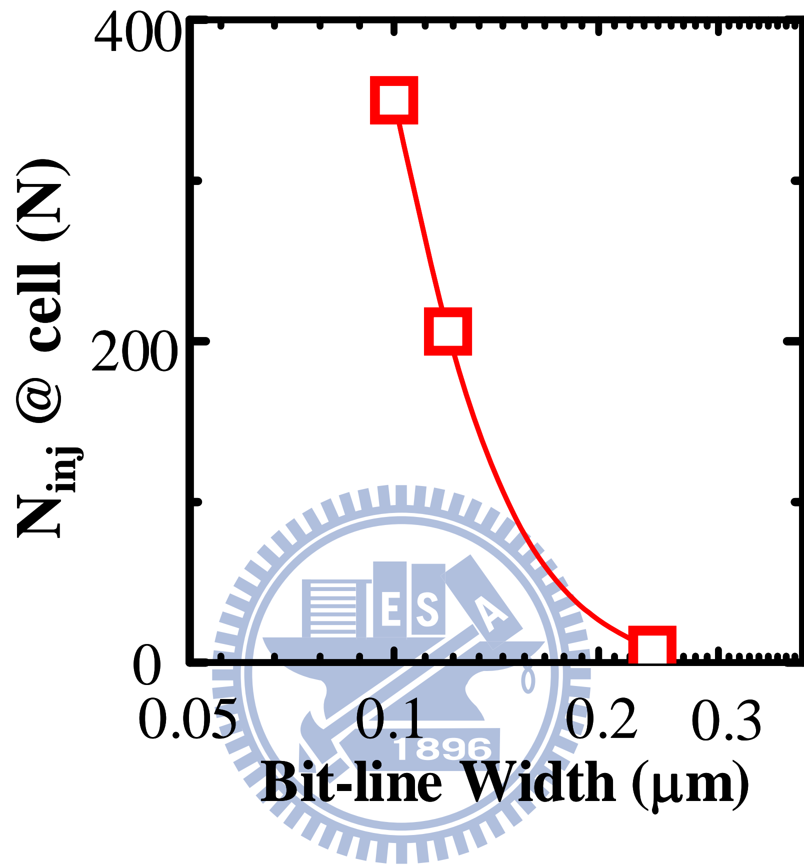


Fig. 2.20 Dependence of the program disturb on BD bit-line width, N_{inj}(cell (N)) versus bit-line width.

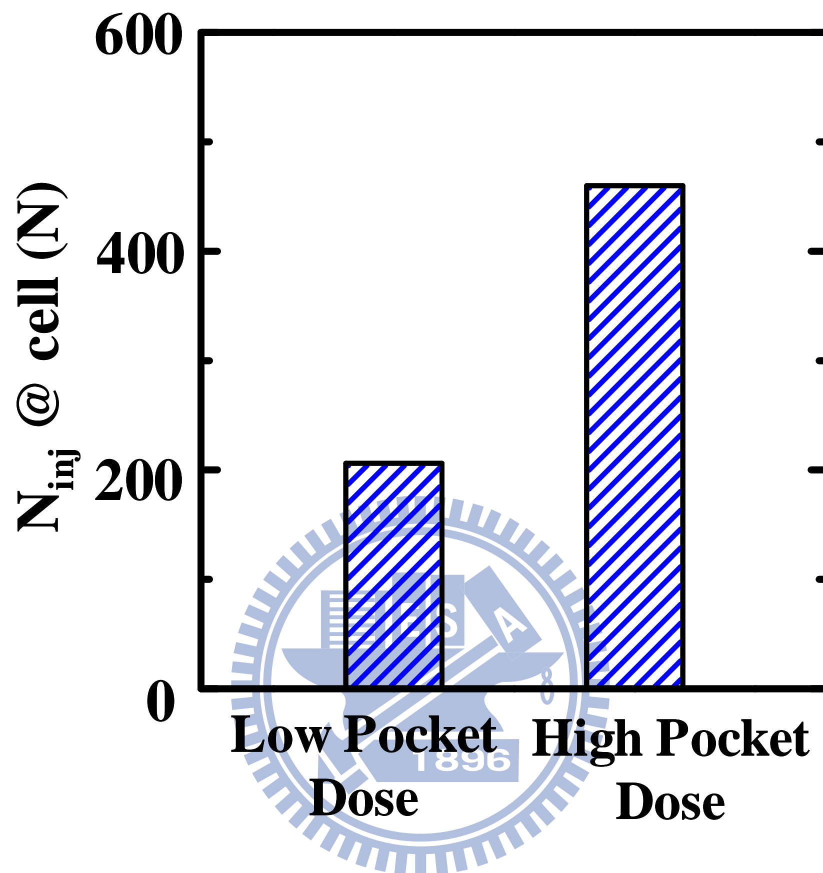
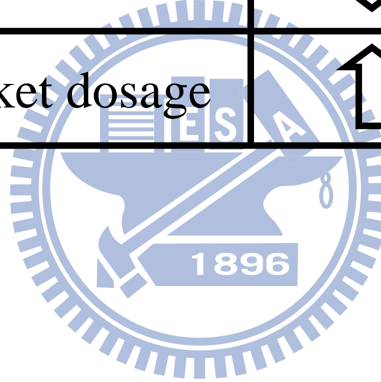


Fig. 2.21 Pocket implant dosage effect on the program disturb. The dosages of the two pocket implant splits differ by two times.

Table 2.2 Key factors affecting program disturb.

Factor	Effect
substrate bias	⇧
bit-line width	⇩
bit-line depth	⇩
Pocket dosage	⇧



Chapter 3

A Novel Hot Electron Programming Method in a Buried Diffusion Bit-line SONOS Memory by Utilizing Non-Equilibrium Charge Transport

3.1 Preface

NOR-type SONOS flash memories by utilizing channel hot electron (CHE) program and band-to-band tunneling hot hole (BTBT HH) erase have been demonstrated with good performance and reliability, small die size and low fabrication cost [1.1][1.2], [3.1-3.3]. A virtual ground array with n^+ buried diffusion (BD) bit-lines is usually implemented to achieve a higher packing density. For hot electron programming in a NOR-type flash memory, a large drain-to-source voltage V_{ds} (~4V) is usually required for channel electrons to surmount the tunnel barrier. For SiO_2/Si system, the tunnel barrier height for electrons is 3.1 eV. As gate length is scaled down, the tunnel barrier height remains unchanged. As a consequence, the leakage current contributed by the un-selected cells sharing the same bit-line voltage will be significant due to channel punch-through caused by a large V_{ds} and limit the cell performance. The illustration is drawn in Fig. 3.1.

Various techniques to boost electron injection energy, such as Schottky barrier source [3.4], have been proposed to enhance hot electron programming efficiency. In this work, we propose a new concept of hot electron programming in a buried diffusion bit-line array with a low V_{ds}. In our method, channel electrons gain energy in two stages, as shown in Fig. 3.2. Electrons are pre-accelerated in a preceding cell,

i.e. cell (N-1). Some energetic electrons may traverse the n^+ BD region and reach a program cell, i.e. cell (N), with residual energy. This residual energy is significant when the BD region is narrow and is attributed to the non-equilibrium transport across the BD region where the electric field is almost zero. With the electron energy boosting at the source, channel electrons in a program cell exhibit higher programming efficiency.

In this work, we first compare the programming speeds of our method and two conventional hot electron program methods. The program disturb and electron pre-acceleration effect are characterized. Furthermore, the concept of our method is verified through a Monte Carlo simulation. The impact of a bit-line width is also characterized and evaluated.

3.2 A Novel Hot Electron Programming Method

A virtual-ground SONOS array was fabricated. The gate length is 0.1 μm and the BD width is 0.1 μm. Fig. 3.2 (a) and (b) show the cross section and top view of a buried diffusion bit-line SONOS array, respectively. The program bias voltages are given in Table 3.1. The bias conditions of two conventional hot electron program methods (methods B and C) are also shown in Table 3.1 for a comparative study. Method B has CHISEL injection [1.17] while method C does not have CHISEL.

3.2.1 Programming Speed

The programming speeds of this method and two conventional methods are compared in Fig. 3.3. The V_{ds} in a program cell is fixed at 2.5V in all the methods. A reverse-read scheme with a bit-line voltage of 1.6V is employed [1.1]. Obviously, our method has a faster programming speed, as compared to the conventional methods

with or without CHISEL. Our method shows that a program threshold voltage (V_t) window of 4V is achieved in 2.5μs programming time. In addition, our method exhibits a larger program V_t window than the method B by ~0.9V. It should be pointed out that the program current (i.e., the channel current of cell N) in our method and in method B is about the same. The reason is that the voltages applied to the program cell in our method and in method B are exactly the same except that the source of the channel current is different. The programming electrons in our method are from a preceding cell, which experience pre-acceleration, while they are from a bit-line in method B.

3.2.2 Program Disturb

In addition, we measure the threshold voltage of a preceding cell, cell (N-1), in programming. No V_t shift (program disturb) is observed in a program period of 2.5μs, as shown in Fig. 3.4. The reason is that the drain-to-source voltage in a preceding cell is only 2V.

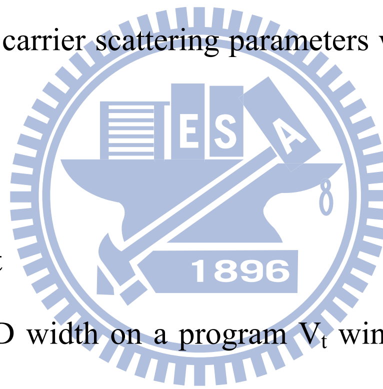
3.2.3 Electron Pre-acceleration Effect

In order to examine the electron pre-acceleration effect on V_t window, we vary the pre-acceleration voltage $V_{BL(N)}$ in programming while the V_{ds} of a program cell, i.e. $V_{BL(N+1)}$-$V_{BL(N)}$, is fixed at 2.5V. The programming time is 2.5μs and a V_t window enlargement is defined as ΔV_t(this method)- ΔV_t(method B). In Fig. 3.5, a program V_t window shows a positive dependence on the pre-acceleration voltage $V_{BL(N)}$. This trend suggests that, as $V_{BL(N)}$ increases, program cell electrons have higher energy and thus higher injection efficiency.

3.3 Monte Carlo Analysis

3.3.1 Monte Carlo Model

To simulate non-equilibrium transport in the n^+ BD region and an electron residual energy distribution, a multi-step Monte Carlo simulation similar to [2.3] is performed. In the simulation, the electric field distributions in cells (N-1) and (N) are obtained from a two-dimensional device simulator. Fig. 3.6 shows the potential distribution along the channel in the bias condition of our method. The Monte Carlo simulation includes a full band structure, consisting of a conduction band structure [2.7] and a valence band structure [2.8]. The relevant scattering mechanisms in the simulation include acoustic phonon scattering, intervalley optical phonon scattering and impact ionization. The carrier scattering parameters were calibrated in our earlier paper [2.10][2.11].



3.3.2 Bit-line Width Effect

The dependence of BD width on a program V_t window is characterized in Fig. 3.7. Two different BD width splits, 0.1 μm and 0.12 μm, were fabricated. The smaller BD width apparently has higher injection energy and thus a larger program V_t window.

We further utilize a Monte Carlo simulation to evaluate the BD width effect. Electrons are launched at the source of cell (N-1) with a Boltzmann distribution. The electron energy distributions in cell (N-1) and cell (N) are shown in Fig. 3.8 (a) and (b), respectively. The dot symbol represents the energy distribution in the source side while the line represents the energy distribution in the drain side. The energy distribution in the source side of cell (N) apparently deviates from a Boltzmann distribution and exhibits a high-energy tail. This is due to the non-equilibrium

transport across the n^+ BD region. Moreover, the hump in the drain side of cell (N) is due to CHISEL.

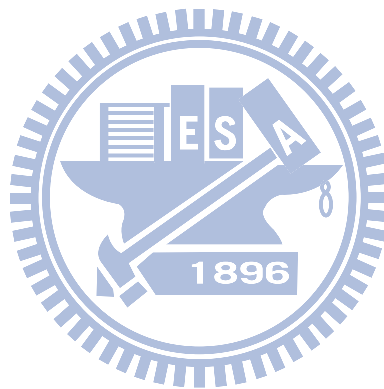
We find that the high-energy tail becomes more pronounced as a BD width is reduced, as shown in Fig. 3.9. The reason is that electrons acquiring energy in cell (N-1) cannot release their energy completely by means of phonon scatterings when passing through a narrow BD region. As a consequence, a smaller BD width has a stronger non-equilibrium transport and thus a larger program V_t window, which is in agreement with the experimental result in Fig. 3.7.

The number of hot electrons in a program cell is simulated in Fig. 3.10. The conventional method with CHISEL is also shown for a comparison study. The same number of electrons is used. Then, the number of hot electrons is calculated by counting electrons hitting the SiO_2 and Si interface of a program cell with energy above the effective oxide barrier height. In Fig. 3.10, the effective oxide barrier height varies during programming due to the build-up of program charges in the nitride. The initial effective barrier height is near 2.5 eV after taking into account tunneling and image force. Obviously, our Monte Carlo analysis confirms that our method has a larger charge injection rate due to the presence of a high-energy tail at the source of a program cell.

3.4 Summary

A novel hot electron programming concept in a buried diffusion bit-line SONOS array is demonstrated. In our method, electron acceleration is achieved in two adjacent cells rather than in a single cell. In this way, the V_{ds} in each cell can be reduced to avoid channel punch-through. Our study shows that this method is more efficient than conventional hot electron program methods. This method is more

effective as a bit-line width reduces and is suitable for further scaling in a NOR-type SONOS flash memory.



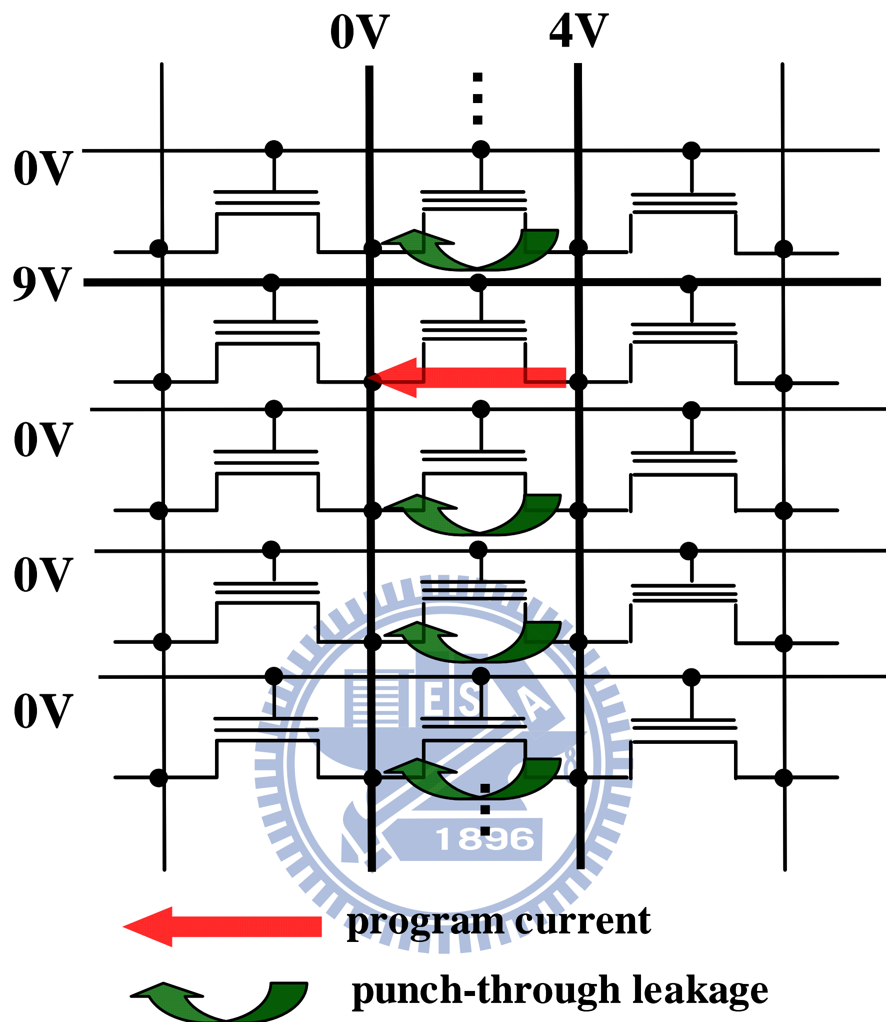
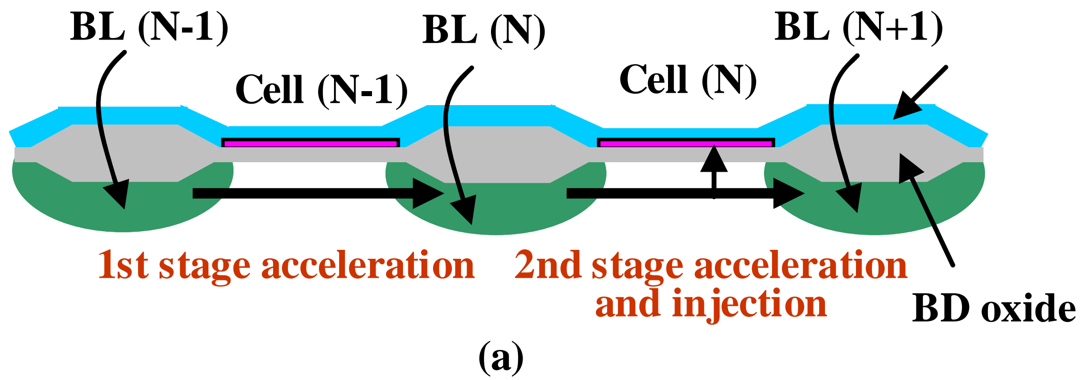


Fig. 3.1 Illustration of punch-through leakages during conventional hot electron programming in a NOR-type SONOS memory array.



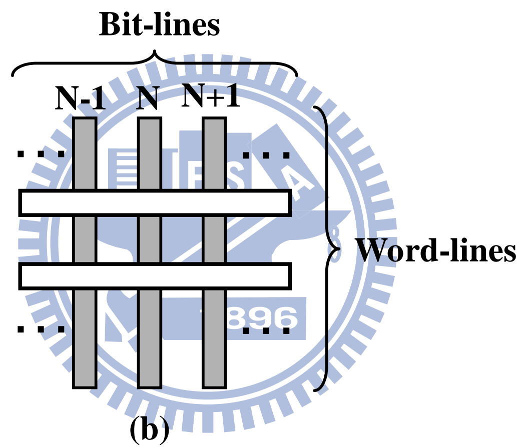


Fig. 3.2 (a) Illustration of a new hot electron programming method and two-stage electron acceleration in a buried diffusion bit-line SONOS memory array. (b) Top view of the array. The gate length and the BD width are 0.1μm.

Table 3.1 Program bias voltages used in this method (A) and two conventional hot electrons methods (B and C). Method B has CHISEL injection while method C dose not have CHISEL.

voltages / methods	$V_{BL(N-1)}$	$V_{BL(N)}$	$V_{BL(N+1)}$	V_{WL}
A (this method)	0.0V	2.0V	4.5V	9.5V
B (w/ CHISEL)	floating	2.0V	4.5V	9.5V
C (w/o CHISEL)	floating	0.0V	2.5V	9.5V

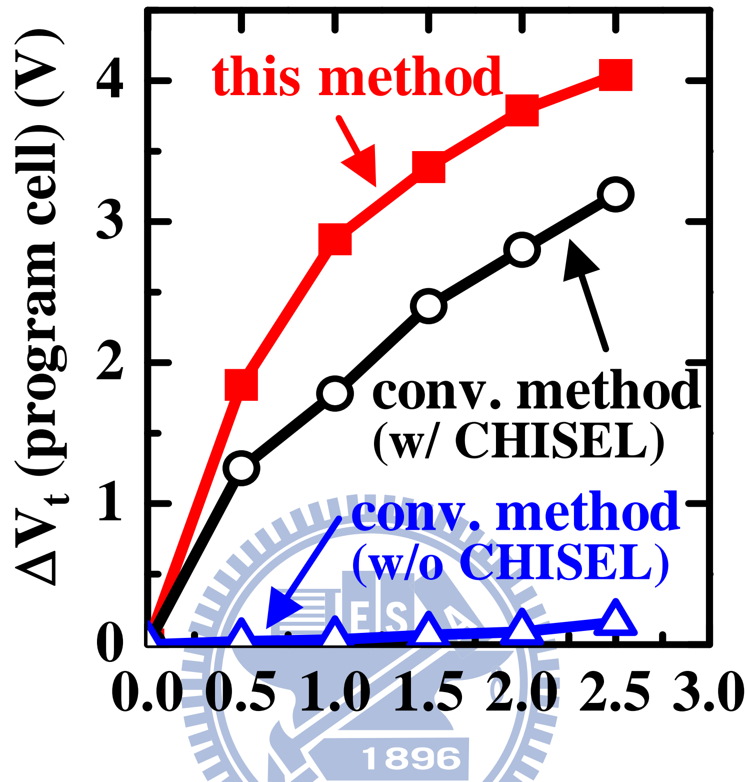


Fig. 3.3 Threshold voltage shift versus programming time of the three hot electron program methods in Table 3.1. The V_{ds} of a program cell is fixed at 2.5V.

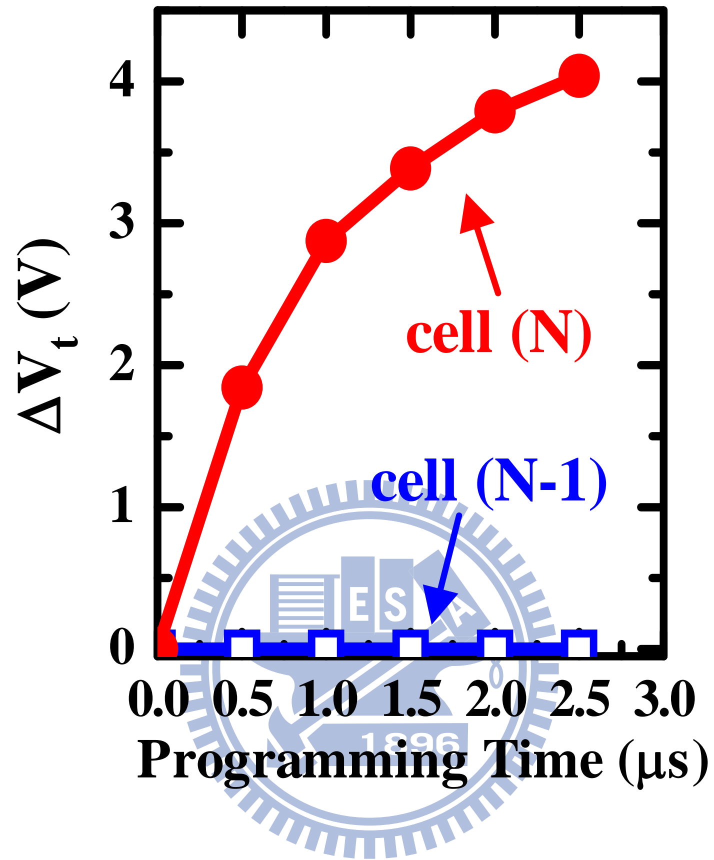


Fig. 3.4 Threshold voltage shift versus programming time in cell (N) and cell (N-1). The read voltage is 1.6V.

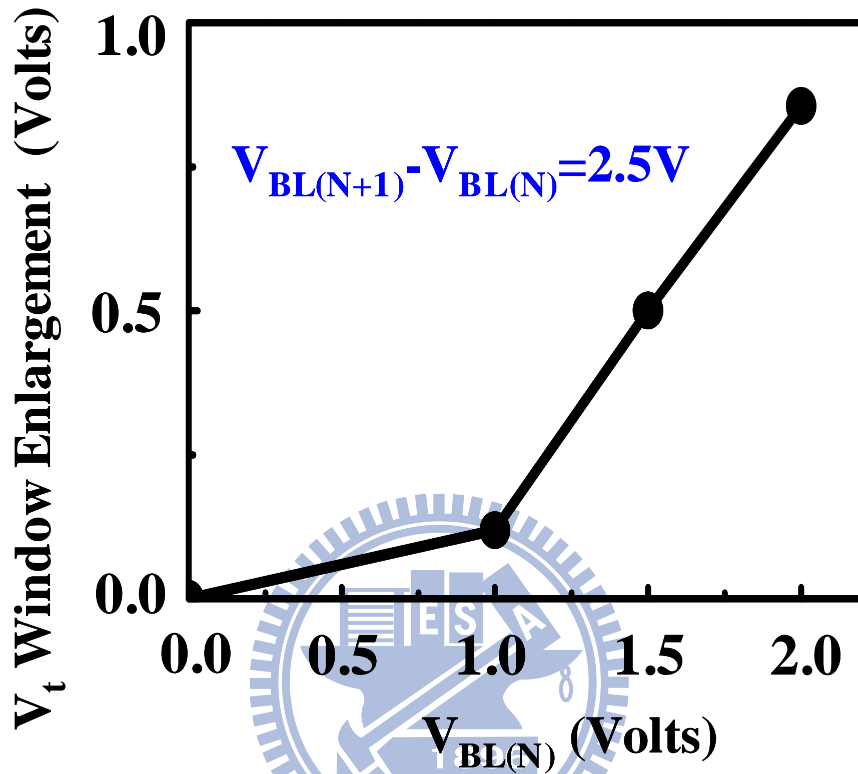


Fig. 3.5 The dependence of V_t window enlargement on the pre-acceleration voltage $V_{BL(N)}$ in this method. The V_t window enlargement is defined as V_t(this method)-V_t(method B). The V_{ds} of a program cell, i.e. $V_{BL(N+1)}$-$V_{BL(N)}$, is fixed at 2.5V. The programming time is 2.5μs.

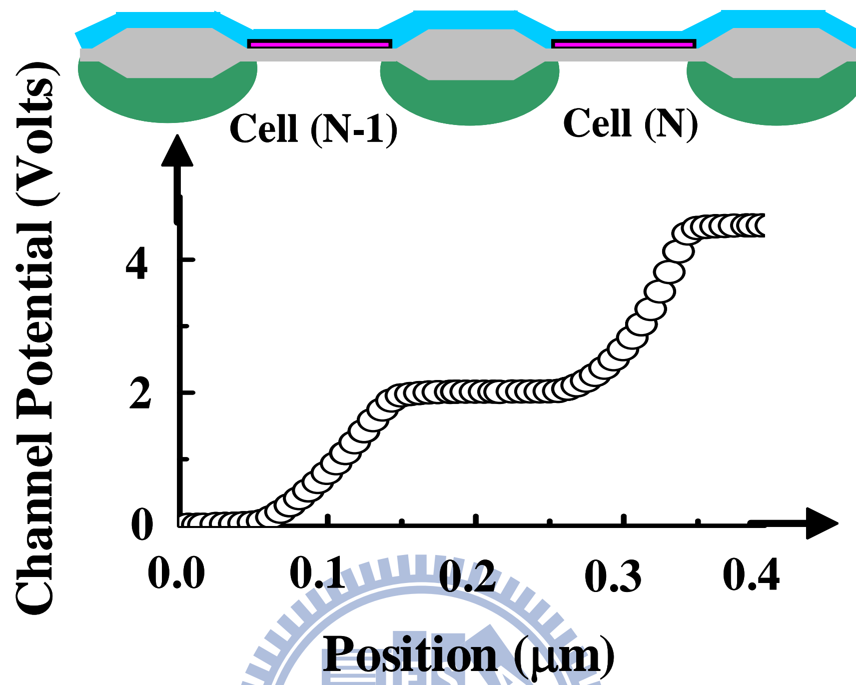


Fig. 3.6 Potential distribution along the channel direction obtained from a two-dimensional device simulator.

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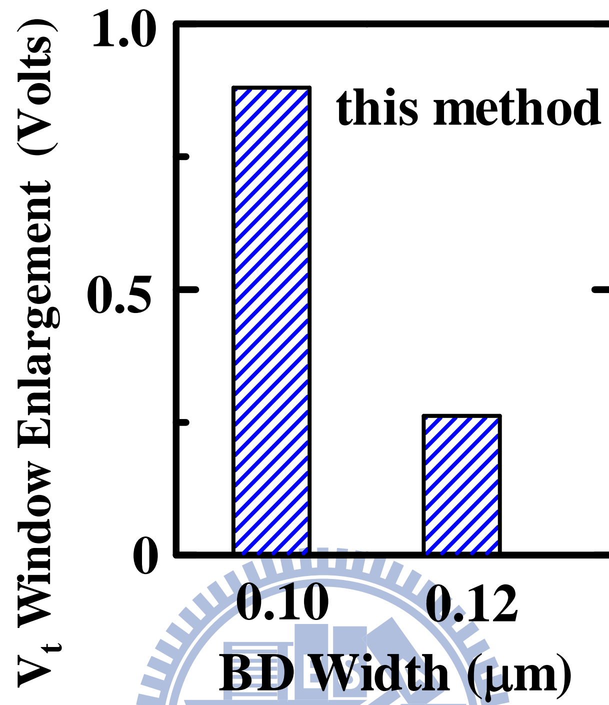


Fig. 3.7 Comparison of a V_t window enlargement in two different BD width splits. The V_{ds} of a program cell is fixed at 2.5V. The programming time is 2.5μs.

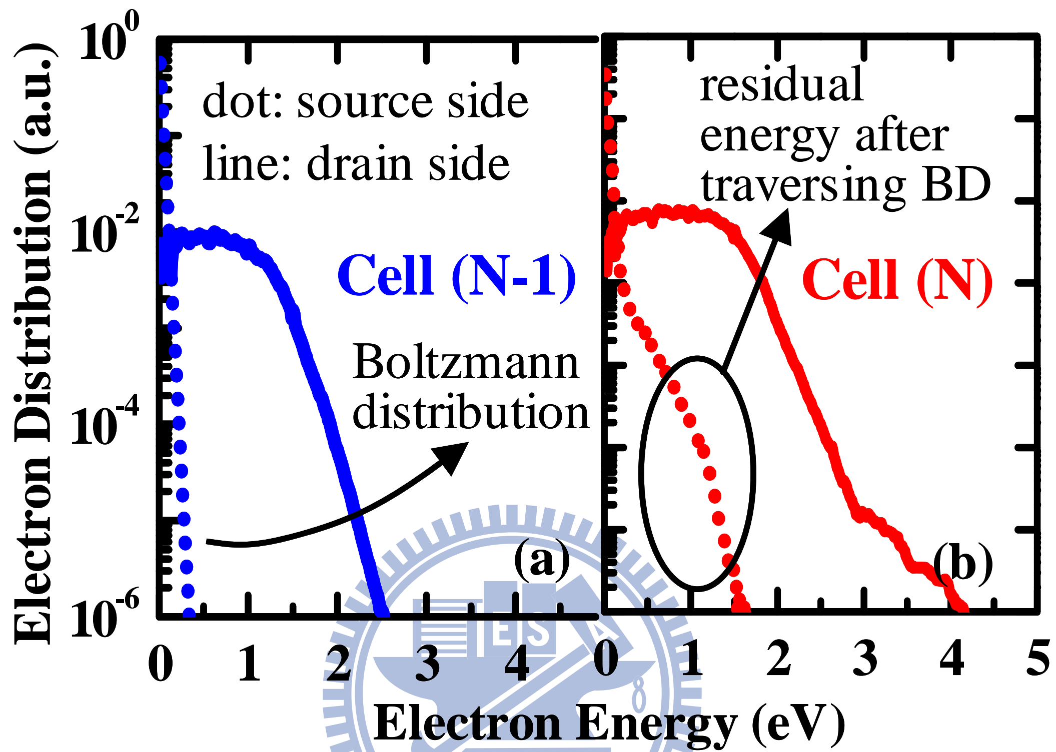


Fig. 3.8 (a) Electron energy distributions in the source side and in the drain side, respectively, in cell (N-1). (b) Electron energy distributions in cell (N). A high-energy tail near the source is highlighted, which results from electron non-equilibrium transport across the n^+ BD region.

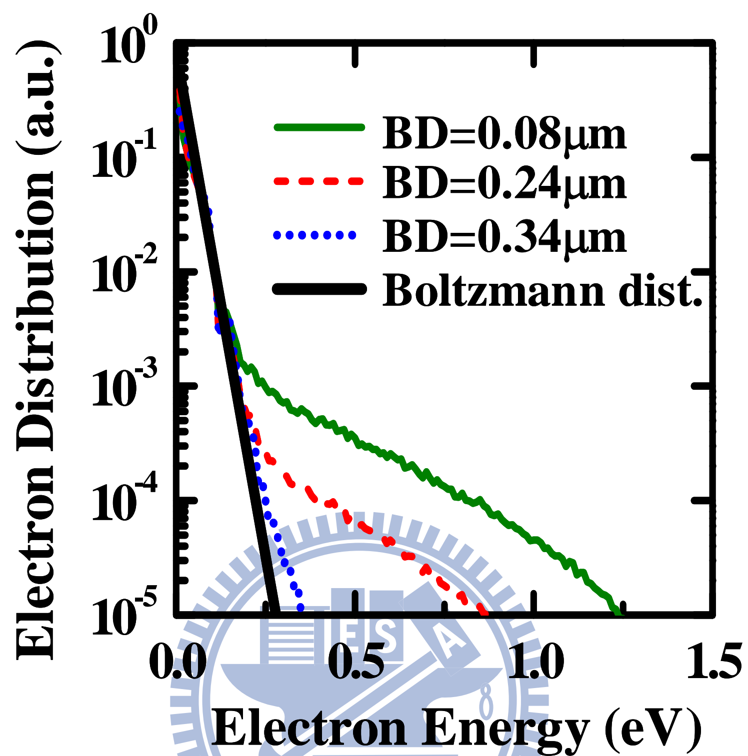


Fig. 3.9 Monte Carlo simulated electron energy distribution at the source of cell (N) for different BD widths. The bias voltages are given in Table 3.1. The thick solid line represents a Boltzmann distribution.

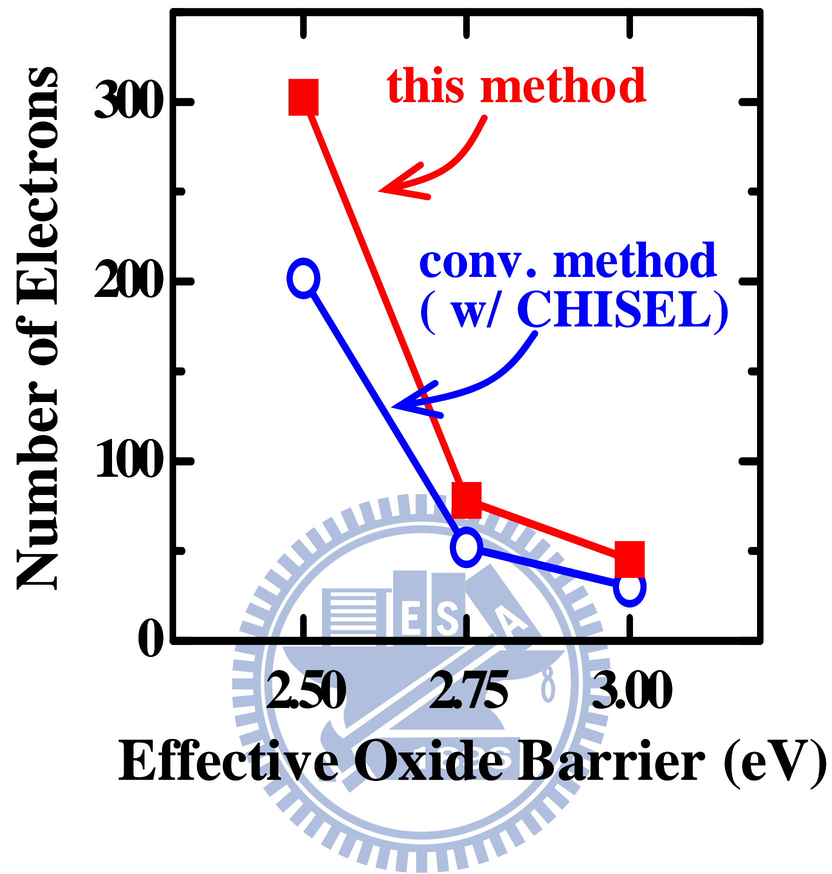


Fig. 3.10 Total number of simulated electrons with energy above a certain effective oxide barrier in this method and in method B.

Chapter 4

Study of Quantum Confinement Effects on Hole Mobility in Silicon and Germanium Double Gate MOSFETs

4.1 Preface

Double-gate (DG) metal-oxide-semiconductor field-effect-transistors (MOSFETs) and fin field-effect-transistor have been considered as promising alternatives to bulk MOSFETs in 22nm technology node and beyond due to their immunity to short channel effects. Recently, advanced channel materials with higher carrier mobility than bulk Si, such as Ge, and III-V materials, have attracted much attention. Experimental works have shown the possibility that the inversion carrier mobility can be further improved in quantum structure MOSFETs by a subband modulation [1.20][1.21]. However, there has been little work on Ge-channel DG-pMOSFETs addressing valence subband and substrate/channel orientation effects on hole mobility.

In this work, we analyze quantum confinement effects on hole mobility as a function of a body thickness in Si- and Ge-channel DG-pMOSFETs. The low-field hole mobility is calculated by a Monte Carlo method [1.22]. The role of quantum confinement effects in a Ge-channel is compared with a Si-channel with a valence subband calculation. The impact of substrate orientation on hole mobility is also evaluated. Furthermore, the effect of uniaxial compressive stress is discussed.

4.2 Valence Band Structure in Strained Bulk Materials

Various methods have been developed to calculate a band structure in

semiconductors, including the pseudo-potential method [2.7], the k · p method [4.1], the tight binding method [4.2], and the bond orbital model method [2.8]. In this work, the Luttinger-Kohn model [4.3] under the framework of k · p method is employed to calculate the valence band structure. This method has the following merits. First, the Luttinger-Kohn model is suitable for diamond and zinc blende structure semiconductors, whose band gap is much larger than the split-off energy [4.4]. Second, due to the warping of valence bands, the Luttiner-Kohn model rather than the effective-mass approximation is commonly used to obtain an accurate valence band structure. Third, the strain effects can be easily taken into account when the Bir-Pikus Hamiltonian [4.5] is incorporated into the Luttinger Hamiltonian. For the k · p method in the Luttinger-Kohn model, the heavy-hole, the light-hole and split-off bands in double degeneracy are considered and are called class A. The rest of the bands are defined as class B. The effects of bands in class B on those in class A are also considered.

Based on the theory of Luttinger-Kohn and Bir-Pikus, the valence band structure of a strained bulk material can be expressed in Equation (4.1) [4.6],

$$H = H_k + H_\varepsilon \tag{4.1}$$

where H_k is the unstrained Hamiltonian (Luttinger Hamiltonian) and H_ε is the strained Hamiltonian (Bir-Pikus Hamiltonian). Thus, the total Hamiltonian H can be expressed as the 6×6 Hamiltonian in the envelope function space (Equation (4.2)).

$$H=-\begin{bmatrix} P+Q & -S & R & 0 & -\frac{1}{\sqrt{2}}S & \sqrt{2}R \\ -S^{+} & P-Q & 0 & R & -\sqrt{2}Q & \sqrt{\frac{3}{2}}S \\ R^{+} & 0 & P-Q & S & \sqrt{\frac{3}{2}}S^{+} & \sqrt{2}Q \\ 0 & R^{+} & S^{+} & P+Q & -\sqrt{2}R^{+} & -\frac{1}{\sqrt{2}}S^{+} \\ -\frac{1}{\sqrt{2}}S^{+} & -\sqrt{2}Q^{+} & \sqrt{\frac{3}{2}}S & -\sqrt{2}R & P+\lambda & 0 \\ \sqrt{2}R^{+} & \sqrt{\frac{3}{2}}S^{+} & \sqrt{2}Q^{+} & -\frac{1}{\sqrt{2}}S & 0 & P+\lambda \end{bmatrix} \begin{matrix} \left|\frac{3}{2},\frac{3}{2}\right\rangle \\ \left|\frac{3}{2},\frac{1}{2}\right\rangle \\ \left|\frac{3}{2},-\frac{1}{2}\right\rangle \\ \left|\frac{3}{2},-\frac{3}{2}\right\rangle \\ \left|\frac{1}{2},\frac{1}{2}\right\rangle \\ \left|\frac{1}{2},-\frac{1}{2}\right\rangle \end{matrix} \tag{4.2}$$

where $P=P_k+P_\varepsilon$, $Q=Q_k+Q_\varepsilon$, $R=R_k+R_\varepsilon$, $S=S_k+S_\varepsilon$. The symbol λ represents the split-off energy. The symbol $^+$ represents the operation of the complex conjugate. The basis function $\left|J,m_J\right\rangle$ represents the Bloch wave function at the zone center, consisting of heavy hole states $\left|\frac{3}{2},\pm\frac{3}{2}\right\rangle$, light hole states $\left|\frac{3}{2},\pm\frac{1}{2}\right\rangle$, and split-off states $\left|\frac{1}{2},\pm\frac{1}{2}\right\rangle$, which takes into account two spin states..

$$P_k=\left(\frac{\hbar^2}{2m_0}\right)\gamma_1(k_x{}^2+k_y{}^2+k_z{}^2) \tag{4.3a}$$

$$Q_k=\left(\frac{\hbar^2}{2m_0}\right)\gamma_2(k_x{}^2+k_y{}^2-2k_z{}^2) \tag{4.3b}$$

$$R_k=\left(\frac{\hbar^2}{2m_0}\right)\sqrt{3}[-\gamma_2\ (k_x{}^2-k_y{}^2)+2i\gamma_3k_xk_y] \tag{4.3c}$$

$$S_k=\left(\frac{\hbar^2}{2m_0}\right)2\sqrt{3}\gamma_3(k_x-ik_y)k_z \tag{4.3d}$$

$$P_\varepsilon=-a_v(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) \tag{4.4a}$$

$$Q_\varepsilon=-\frac{b}{2}(\varepsilon_{xx}+\varepsilon_{yy}-2\varepsilon_{zz}) \tag{4.4b}$$

$$R_\varepsilon=-\frac{\sqrt{3}}{2}b(\varepsilon_{xx}-\varepsilon_{yy})-id\varepsilon_{xy} \tag{4.4c}$$

$$S_\varepsilon = -d(\varepsilon_{zx} - i\varepsilon_{yz}) \tag{4.4d}$$

γ_1, γ_2, and γ_3 are the Luttinger parameters. m_0 is the mass of free electron. k_x, k_y, and k_z are the wave vector in x, y and z direction, respectively. a_v, b and d are the Bir-Pikus deformation potentials for the valence bands. According to [4.7], the strain tensor (ε) is related to the stress tensor (σ) by the elastic compliance matrix or elastic stiffness matrix.

$$\varepsilon = S \bullet \sigma \tag{4.5}$$

$$\sigma = C \bullet \varepsilon \tag{4.6}$$

The elastic compliance or elastic stiffness matrix relates the six strain components to the six stress components. As a result, the matrix, S or C, has 36 coefficients. However, due to the cubic symmetry in Si or Ge, only the three independent coefficients are needed. Thus, the strain-stress relation can be expressed as Equations (4.7) and (4.8) [4.7].

$$\begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{xz} \\ 2\varepsilon_{xy} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{bmatrix} \tag{4.7}$$

$$
\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{44} \end{bmatrix} \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{xz} \\ 2\varepsilon_{xy} \end{bmatrix} \tag{4.8}
$$

where the elastic compliance constant and elastic stiffness constant can be related by

$$
C_{11} - C_{12} = (S_{11} - S_{12})^{-1} \tag{4.9a}
$$

$$
C_{11} + C_{12} = (S_{11} + 2S_{12})^{-1} \tag{4.9b}
$$

$$
C_{44} = 1/S_{44} \tag{4.9c}
$$

Moreover, we can express Equation (4.7) into Equation (4.10).

$$
\begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{xz} \\ 2\varepsilon_{xy} \end{bmatrix} = \begin{bmatrix} S_{11}\sigma_{xx} + S_{12}\sigma_{yy} + S_{12}\sigma_{zz} \\ S_{12}\sigma_{xx} + S_{11}\sigma_{yy} + S_{12}\sigma_{zz} \\ S_{12}\sigma_{xx} + S_{12}\sigma_{yy} + S_{11}\sigma_{zz} \\ S_{44}\sigma_{yz} \\ S_{44}\sigma_{xz} \\ S_{44}\sigma_{xy} \end{bmatrix} \tag{4.10}
$$

For instance, it is believed that the [110] channel direction is the primarily used channel direction in strained-Si technologies because of its largest hole piezoresistance coefficient for longitudinal compressive stress on both (100) and (110) substrates [4.8]. The [ ] and ( ) are the notations of channel direction and substrate orientation, respectively. As an uniaxial stress is applied to the (100)/[110] direction,

the unit vector along the [110] direction is $[\frac{1}{\sqrt{2}},\frac{1}{\sqrt{2}},0]$. Thus, we have $\sigma_{xx}=\frac{1}{2}\sigma$, $\sigma_{yy}=\frac{1}{2}\sigma$, $\sigma_{zz}=0$, $\sigma_{yz}=0$, $\sigma_{xz}=0$, and $\sigma_{xy}=\frac{1}{2}\sigma$, where σ is positive for a tensile stress and is negative for a compressive stress. As a consequence, according to Equation (4.10), $\varepsilon_{xx}=\frac{1}{2}(S_{11}+S_{12})\cdot\sigma$, $\varepsilon_{yy}=\frac{1}{2}(S_{11}+S_{12})\cdot\sigma$, $\varepsilon_{zz}=S_{12}\cdot\sigma$, $\varepsilon_{yz}=0$, $\varepsilon_{xz}=0$, $\varepsilon_{xy}=\frac{1}{4}S_{44}\cdot\sigma$. Then, these strain components are introduced into Equation (4.2) to consider the stress effect.

When dealing with the substrate orientation other than the (100) direction, an appropriate rotation matrix is employed [4.9]. We must transform the crystallographic coordinate system (x,y,z) into the new coordinate system (x',y',z'), where z' is also the new growth direction. For example, when the (110) substrate is considered, the new coordinate system (x',y',z') is thus given by Equation (4.11). The corresponding Luttinger Hamiltonian components are written as Equation (4.12).

$$k_x' = -k_z \tag{4.11a}$$

$$k_y' = \frac{1}{\sqrt{2}}(-k_x + k_y) \tag{4.11b}$$

$$k_z' = \frac{1}{\sqrt{2}}(k_x + k_y) \tag{4.11c}$$

$$P_k = (\frac{\hbar^2}{2m_0})\gamma_1(k_x'^2 + k_y'^2 + k_z'^2) \tag{4.12a}$$

$$Q_k = (\frac{\hbar^2}{2m_0})\gamma_2(-2k_x'^2 + k_y'^2 + k_z'^2) \tag{4.12b}$$

$$R_k = (\frac{\hbar^2}{2m_0})\sqrt{3}[2\gamma_2 k_y' k_z' + i\gamma_3(-k_y'^2 + k_z'^2)] \tag{4.12c}$$

$$S_k = (\frac{\hbar^2}{2m_0})\sqrt{6}\gamma_3(k_x' k_y' - k_x' k_z' + ik_x' k_y' + ik_x' k_z') \tag{4.12d}$$

4.3 Valence Subband Structure in pMOSFETs

4.3.1 Schrodinger Equation with a Six-band Luttinger Hamiltonian

The valence subbands in an inversion layer can be solved by obtaining the self-consistent solution to the Poisson and Schrödinger equations under the framework of a six-band Luttinger Hamiltonian. The effective mass approximation is not appropriate because the valence band structure (see Fig. 4.1) is warped due to the valence band mixing effect. In the simulation, we take the coordinate z to be the direction perpendicular to the semiconductor and gate dielectric interface. The Schrödinger equation can be expressed as Equation (4.13).

$$\left[H(k_x,k_y,k_z)+V(z)I_{6\times 6}\right]\varphi_{n,k_x,k_y}(z)=E_n\cdot\varphi_{n,k_x,k_y}(z) \tag{4.13}$$

where H is the 6×6 Hamiltonian with or without strain Hamiltonian. $\varphi_{n,kx,ky}(z)$ is a 6×1 vector containing the components of the basis function $\left|J,m_J\right\rangle$, I_{6x6} is the identity matrix of order 6, $V(z)$ is the potential energy, and E_n is the n-th subband energy. From Equations (4.3)-(4.4), we know that H is a second-order polynomial in k_z. Thus H can be expressed in Equation (4.14) [4.10].

$$H=H^{(2)}\cdot k_z^2+H^{(1)}\cdot k_z+H^{(0)} \tag{4.14}$$

Since the z direction is the confinement direction, the quantum number k_z is then represented by $-i\frac{d}{dz}$.

$$\left[-H^{(2)}\frac{d^2}{dz^2}-iH^{(1)}\frac{d}{dz}+H^{(0)}+V(z)I_{6\times6}\right]\cdot\varphi_{n,k_x,k_y}(z)=E_n\cdot\varphi_{n,k_x,k_y}(z) \tag{4.15}$$

When the three-point finite-difference method is employed, Equation (4.15) becomes

$$H_{i,i}=H^{(2)}(\frac{1}{h_{i-1}}+\frac{1}{h_i})\cdot(\frac{2}{h_{i-1}+h_i})+H^{(0)}+V(z) \tag{4.16a}$$

$$H_{i,i-1}=-H^{(2)}(\frac{1}{h_{i-1}})\cdot(\frac{2}{h_{i-1}+h_i})+\frac{iH^{(1)}}{2}\cdot(\frac{2}{h_{i-1}+h_i}) \tag{4.16b}$$

$$H_{i,i+1}=-H^{(2)}(\frac{1}{h_i})\cdot(\frac{2}{h_{i-1}+h_i})-\frac{iH^{(1)}}{2}\cdot(\frac{2}{h_{i-1}+h_i}) \tag{4.16c}$$

where the index i represents each mesh point and h_i stands for the mesh size between adjacent mesh points x_i and x_{i+1}. Equation (4.16) produces an asymmetric tri-diagonal matrix if mesh spacing is non-uniform, which will result in a complex eigenvalue. In order to obtain a real-valued eigenvalue, a diagonal matrix, L, is used, as reported in literature [4.11].

$$L_i^2=\left.(h_{i-1}+h_i)\right/2 \tag{4.17}$$

When we set $B=L^2\bullet H$, then B is a Hermitian matrix because of $B_{i,i+1}=B_{i+1,i}$. By using the relation $B=L^2\bullet H$, we can show that

$$(L^{-1}BL^{-1})L\varphi=L^{-1}LLH\varphi=(E_n)L\varphi \tag{4.18}$$

Thus, instead of solving Equation (4.16) directly, one can solve Equation (4.18) to obtain the eigenvalue E_n corresponding to the eigen-function Φ, which ensures the

real-valued eigenvalues.

$$(L^{-1}BL^{-1})\Phi = (E_n)\Phi \qquad \text{where} \quad \varphi = L^{-1}\Phi \tag{4.19}$$

4.3.2 Poisson Equation

The one dimensional Poisson equation taking position dependence of dielectric constant into consideration is given by

$$\nabla \cdot (\varepsilon(z) \cdot \nabla \phi(z)) = -q \cdot (p(z) - n(z) - N_A^-(z) + N_D^+(z)) \tag{4.20}$$

where q represents elementary charge, $\varepsilon(z)$ is the position-dependent dielectric constant, and $\phi(z)$ is the electrostatic potential. Complete ionization at 300K is assumed in the simulation. The finite difference method is employed for the discretization of the Poisson equation. In a gate dielectric region, we have

$$\nabla^2 \phi(z) = 0 \tag{4.21a}$$

$$\phi_i = \frac{1}{c_1}\left(\frac{1}{x_i}\phi_{i+1} - \frac{1}{x_{i-1}}\phi_{i-1}\right) \tag{4.21b}$$

where $c_1 = \left(\frac{1}{x_i} + \frac{1}{x_{i-1}}\right)$.

In the gate dielectric and semiconductor interface, discretization of Equation (4.20) can be achieved by using the linearization scheme. The simplest way is to let $\phi^{k+1} = \phi^k + \delta$, where δ is small. As a result, we have

$$\varepsilon\nabla\cdot\nabla\delta-\frac{q}{V_T}(n+p)\cdot\delta=q(n-p+N_A^- -N_D^+)-\varepsilon\nabla\cdot\nabla\phi^k \tag{4.22}$$

where $V_T = kT/q$. After applying the finite-difference method, we have

$$\frac{\varepsilon_1\frac{\delta_{i+1}-\delta_i}{x_i}-\varepsilon_2\frac{\delta_i-\delta_{i-1}}{x_{i-1}}}{\frac{1}{2}(x_i+x_{i-1})}-\frac{q}{V_T}(n+p)\delta_i=q(n-p+N_A^- -N_D^+)-\frac{\varepsilon_1\frac{\phi_{i+1}-\phi_i}{x_i}-\varepsilon_2\frac{\phi_i-\phi_{i-1}}{x_{i-1}}}{\frac{1}{2}(x_i+x_{i-1})} \tag{4.23}$$

Equation (4.23) can be written in a simple form, that is

$$b_{i-1}\delta_{i-1}-\delta_i+a_{i+1}\delta_{i+1}=-c_i \tag{4.24}$$

$$a_{i+1}=\frac{1}{x_i(\frac{1}{x_i}+\frac{\Gamma}{x_{i-1}}+\frac{q}{\varepsilon_1}\frac{1}{V_T}(n+p)e_i)} \tag{4.25a}$$

$$b_{i-1}=\frac{\Gamma}{x_{i-1}(\frac{1}{x_i}+\frac{\Gamma}{x_{i-1}}+\frac{q}{\varepsilon_1}\frac{1}{V_T}(n+p)e_i)} \tag{4.25b}$$

$$c_i=\frac{\frac{1}{x_i}(\phi_{i+1}-\phi_i)+\frac{\Gamma}{x_{i-1}}(\phi_{i-1}-\phi_i)+\frac{q}{\varepsilon_1}(p-n+N_D^+-N_A^-)e_i}{\frac{1}{x_i}+\frac{\Gamma}{x_{i-1}}+\frac{q}{\varepsilon_1}\frac{1}{V_T}(n+p)e_i} \tag{4.25c}$$

$$e_i=\tfrac{1}{2}(x_i+x_{i-1}) \tag{4.25d}$$

$$\Gamma=\frac{\varepsilon_2}{\varepsilon_1} \tag{4.25e}$$

In a semiconductor region, the discretization scheme is similar to Equation (4.23), but the value Γ is equal to 1.

4.3.3 Self-consistent Solution to Poisson and Schrödinger Equations

The simulation flow of the coupled self-consistent Poisson and Schrödinger equations is described in Fig. 4.2, which is similar to [4.12]. The "classical" potential is first obtained by solving the Poisson equation where the "classical" carrier concentrations are computed by a Fermi integral. Then, the potential energy takes into account the potential due to the free charges and ionized impurities. We assume that the image force cancels many-body corrections (exchange and correlation effects) in a bulk inversion layer, as reported in literature [4.13]. Then, with the subband energies and wave-functions obtained from the 6x6 Schrödinger equation, the two-dimensional carrier concentrations, n_s, can be computed. Once the free charge is replaced by n_s, we solve the Poisson equation to obtain the new potential. The subsequent iteration (see Fig. 4.2) will yield the final self-consistent solution when the potential difference between two successive iterations is lower than 10^{-6} V. Note that we assume the wave-function penetration into the gate dielectric is zero.

4.4 Monte Carlo Model

Material parameters of Si and Ge, including Luttinger parameters, deformation potentials, and elastic constants used in the simulation, are given in Table 4.1 [4.14]-[4.16]. Relevant scattering mechanisms, including acoustic phonon scattering and optical phonon scattering, and surface roughness scattering, are considered in the simulation [4.17]-[4.20]. The scattering-matrix elements are approximated, such that phonon scattering can be considered as velocity randomizing. For an acoustic phonon, the scattering rate can be expressed as

$$S_{ac}^{m} = \frac{2\pi k_B T \Xi^2}{\hbar \rho u_l^2} \sum_n D_n(E) \cdot H_{mn} \tag{4.26}$$

where Ξ is the effective acoustic deformation potential, k_B is a Boltzmann constant, T is lattice temperature, $\hbar$ is a reduced Planck constant, ρ is the material density, u_l is the longitudinal sound velocity, $D_n(E)$ is the two-dimensional density of hole states in n-th subband, and H_{mn} is the overlap factor. We ignore the k-dependence of the wave-functions because of relatively small errors [4.17]. Thus,

$$H_{mn} = \int_0^w dz \left| \varphi_{m,0}(z) \cdot \varphi_{n,0}^{\dagger}(z) \right|^2 \tag{4.27}$$

On the other hand, the optical phonon scattering rate can be expressed as

$$S_{op}^{m} = \frac{\pi (D_t K)_{op}^2}{\rho \omega_{op}} \sum_n H_{mn} \cdot D_n(E \mp \hbar\omega_{op}) \cdot \frac{1 - f_0(E \mp \hbar\omega_{op})}{1 - f_0(E)} \cdot (n_{op} + \frac{1}{2} \pm \frac{1}{2}) \tag{4.28}$$

where D_tK is the average optical deformation potential, ω_{op} is the optical phonon frequency, n_{op} is the Bose-Einstein distribution, and f_0 is the Fermi-Dirac distribution. The + and – represents the absorption and emission rates. Furthermore, the formulation of the surface roughness scattering rate can be found in [4.17][4.20] and is briefly describe in Equation (4.29).

$$S_{sr} = \frac{q^2 E_{\text{eff}}^2 m_{\text{DOS}}^{\text{2D}}}{2\pi\hbar^3} \int_0^{2\pi} S(Q)(1 - \cos(\theta)) d\theta \tag{4.29a}$$

$$S(Q) = \pi \cdot \Lambda^2 \Delta^2 \Big/ \left[1 + (Q^2 \Lambda^2 / 2) \right]^3 \tag{4.29b}$$

$$Q = \left| k_i - k_f \right| \tag{4.29c}$$

where E_{eff} is the transverse effective electric field, $m_{\text{DOS}}^{\text{2D}}$ is the density-of-state

effective mass, *S(Q)* is the power spectrum of the roughness at the interface, *Q* is the magnitude of wave-vector change. Λ is the correlation length and Δ is the average step height. Table 4.1 shows the scattering parameters of Si and Ge, which are calibrated from a conventional Si MOSFET and from a SiGe-on-insulator device, respectively [4.19].

In the numerical implementation of the valence subband structure in a Monte Carlo simulation, a tabular form of the *E-k* relationship is established. Only eigenvalues for $k_{||} < 0.6\pi/a$, which significantly contribute to the low-field channel mobility, are evaluated [4.21]. A flowchart of the Monte Carlo simulation can be referred to [1.22]. In the simulation, a single hole is simulated under an external electric field. It travels freely between two successive scatterings. The free-flight time is determined by using a fixed time technique. During the free flight, the hole is accelerated by the field and its momentum and energy are updated according to the tabular form of the *E-k* relationship. If a scattering happens, a random number, 0~1, is then generated to decide the responsible scattering mechanism and subband index. Then, the new hole state is chosen according to the sorted *E-k* relationship. This procedure is continued until the mobility fluctuation due to the statistical error is less than 0.5%.

4.5 Hole Mobility in silicon and germanium double-gate MOSFETs

4.5.1 Subband Structures in (100) Si- and Ge-channels

Fig 4.3 shows the simulated device configuration. The inversion hole density, p_{inv}, is set to be 4×10^{12}cm^{-2}. The 2D hole density of a 15nm Ge-channel is drawn. The wave-functions of a 10nm Si-channel and a 15nm Ge-channel are also depicted in Fig. 4.4. In Fig. 4.4, the first subband of Si-channel is the heavy hole subband, which is

defined from the characteristics of the six basis functions $\left|J,m_J\right\rangle$ at the zone center (i.e. $k=0$). For example, HH1 denotes the first heavy-hole subband, in which the two heavy hole states, $\left|\frac{3}{2},\frac{3}{2}\right\rangle$ or $\left|\frac{3}{2},-\frac{3}{2}\right\rangle$, are dominant (see Fig. 4.4). Likewise, LH1 is the first light-hole subband. The lowest two subbands in a (100) Si-channel are HH1 and LH1, respectively, due to the high degree of degeneracy of heavy and light holes in Si [1.21]. On the other hand, the lowest two subbands in a (100) Ge-channel are HH1 and HH2 because the LH mass ($0.04m_0$) is relatively smaller than HH mass ($0.43m_0$). The calculated 2D hole density of state (DOS) in a Ge-channel is shown in Fig. 4.5. It is obvious that the 2D DOS is not stair-like owing to the valence band-mixing effect.

4.5.2 Hole Mobility in Si- and Ge-channels

Fig. 4.6 compares the hole mobility as a function of a body thickness in (100)/[110] Si- and Ge-channel DG-pMOSFETs. The choice of the [110] channel in Si is because it has a larger stress effect [4.20]. The experimental result for Si-channels is also shown for comparison [1.20]. The p_{inv} is set to be $4\times10^{12}cm^{-2}$. The simulated hole mobility in a Si-channel decreases monotonically with a body thickness, which is consistent with the experimental data. Unlike a Si-channel, the hole mobility in a Ge-channel shows a turn-around characteristic with a body thickness. When a body thickness reduces, the hole mobility increases gradually to a maximum around T_{Ge}=16nm, and then decreases drastically. Note that in the window of inversion hole density and body thickness considered in this work, where the transverse effective electric field is about 0.12 MV/cm in a Ge-channel, the surface roughness scattering has a minor effect on the hole mobility in a Ge-channel. The

same conclusion can be found in [4.22]. Therefore, surface roughness scattering should not affect the existence of a mobility peak in a Ge-channel. Moreover, the calculated hole mobility at T_{Ge}=28nm is about 617 cm^2/Vs, which deviates from the bulk value of Ge. This is due to larger phonon deformation potentials in a MOSFET than in a bulk material, resulting from stress at gate dielectric and semiconductor interface [4.23].

The turn-around behavior of the hole mobility in a Ge-channel can be explained in the two following aspects: overlap integral and energy separation between subbands. As a body thickness decreases, the energy difference, ΔE, between the first subband and the second subband increases owing to quantum confinement effects, as shown in Fig. 4.4 and Fig. 4.7. Because of less chance to be scattered to the second subband, inversion holes have a larger mobility owing to a smaller inter-subband scattering rate. On the other side, the intra-subband scattering rate increases due to an increase of an overlap integral. The confinement effect on the overlap integral can be understood from the illustration in Fig. 4.8. When a smaller body thickness is considered, the wave-function has a wider distribution in momentum space due to the uncertainty principle. For a fixed phonon momentum in the quantized direction q_z, only the shaded region in Fig. 4.8 contributes to the overlap integral. A broader distribution in momentum space results in a larger overlap factor (Fig. 4.7) and thus a larger intra-subband scattering rate. The interplay between inter-subband and intra-subband scatterings opens a window of a body thickness where the scattering rates can be minimized, giving rise to a peak in hole mobility, as shown in Fig. 4.6. Unlike a Si-channel, because Ge has a stronger quantum confinement effect than Si, the larger energy difference for Ge-channel has a larger chance to give rise to the interplay between inter-subband and intra-subband scatterings. As a result, a mobility

peak is observed for Ge-channel.

4.5.3 Substrate Orientation Effect

Moreover, the substrate orientation effect in Ge-channels is evaluated. The same scattering parameters of surface roughness scattering for (100) and (110) substrates are assumed. The hole mobility in (100)/[110] and (110)/[-110] directions versus body thickness is shown in Fig. 4.9. Three points are worth noting. First, quantum confinement induced mobility enhancement is again observed in (110) substrate. Second, the (110) substrate shows an anisotropy of energy dispersion, such that the (110)/[-110] channel direction exhibits a highest mobility, and then the (110)/[00-1] (result not shown in Fig. 4.9). The higher mobility in (110)/[-110] than in (100)/[110] is attributed to a lower conductivity effective mass. Third, the peak mobility in (110)/[-110] occurs at a smaller body thickness. This reason is that a smaller energy difference between the lowest two subbands is obtained in Ge (110) substrate (see the inset in Fig. 4.9).

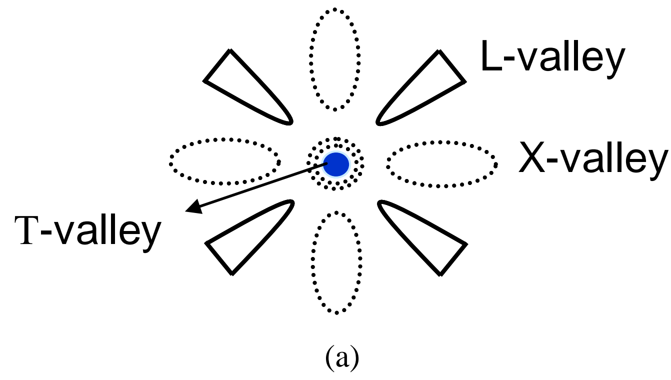
4.5.4 Uniaxial Compressive Stress Effect

Finally, the effect of uniaxial compressive stress on Ge hole mobility is shown in Fig. 4.10 (a). Note that the channel direction is also the uniaxial stress direction. The normalized hole mobility in both (100)/[110] and (110)/[-110] channel directions is evaluated in 0.3GPa uniaxial compressive stress. Generally, the uniaxial compressive stress removes the heavy hole and light hole degeneracy and alters the warping of the valence bands. As a result, the effective mass becomes anisotropic with applied stress. The constant energy contours of the first subband in (100) substrate with or without stress are depicted in Fig. 4.10 (b). In Fig. 4.10 (a), at a large body thickness, the

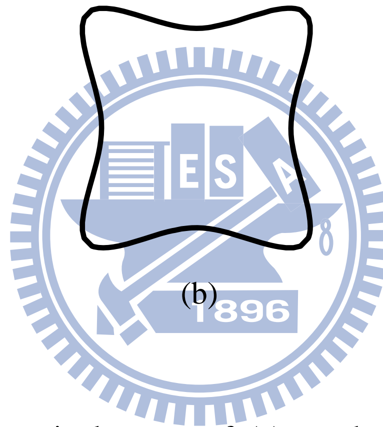
stress induced hole mobility enhancement in (100)/[110] and (110)/[-110] channel directions is comparable due to the same bulk piezoresistance coefficients [4.24]. For a smaller body thickness, the quantum confinement effect plays a role and the energy difference from the uniaxial compressive stress and surface field is additive, which is responsible for the slight shift of the peak mobility.

4.6 Summary

The effects of channel/substrate orientation and uniaxial compressive stress on hole mobility versus body thickness in Ge-channel DG-pMOSFETs are investigated. The peak mobility in both (100)/[110] and (110)/[-110] channel directions can be achieved at a certain body thickness due to the interplay between inter-subband and intra-subband scatterings. Furthermore, it is found that the hole mobility can be further improved when the uniaxial compressive stress is applied to (100)/[110] or (110)/[-110] channel direction. These findings would play a significant role for the design of the Ge-channel DG-pMOSFETs.



(a)



(b)

Fig. 4.1 Equi-energy contour in k-space of (a) conduction-band structure and (b) valence band structure (heavy-hole) of bulk Ge (100) substrate.

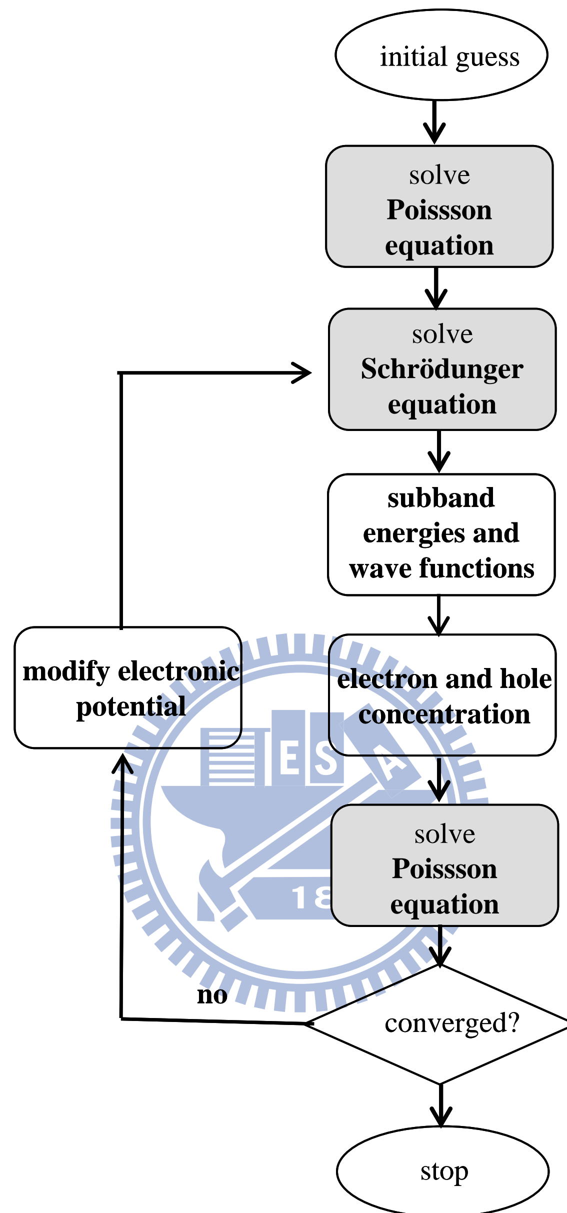


Fig. 4.2 The simulation flow for the self-consistent solution to Poisson and Schrödinger equations.

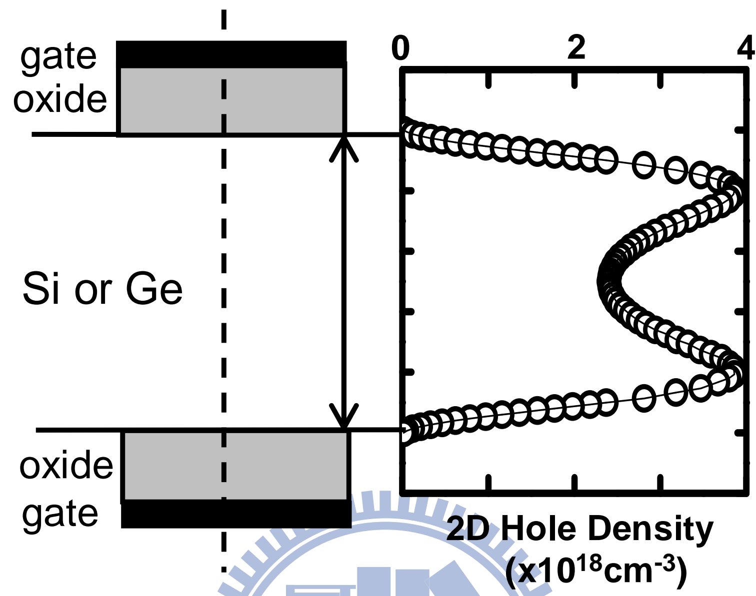


Fig. 4.3 The device configuration and 2D hole density in a (100) Ge-channel.

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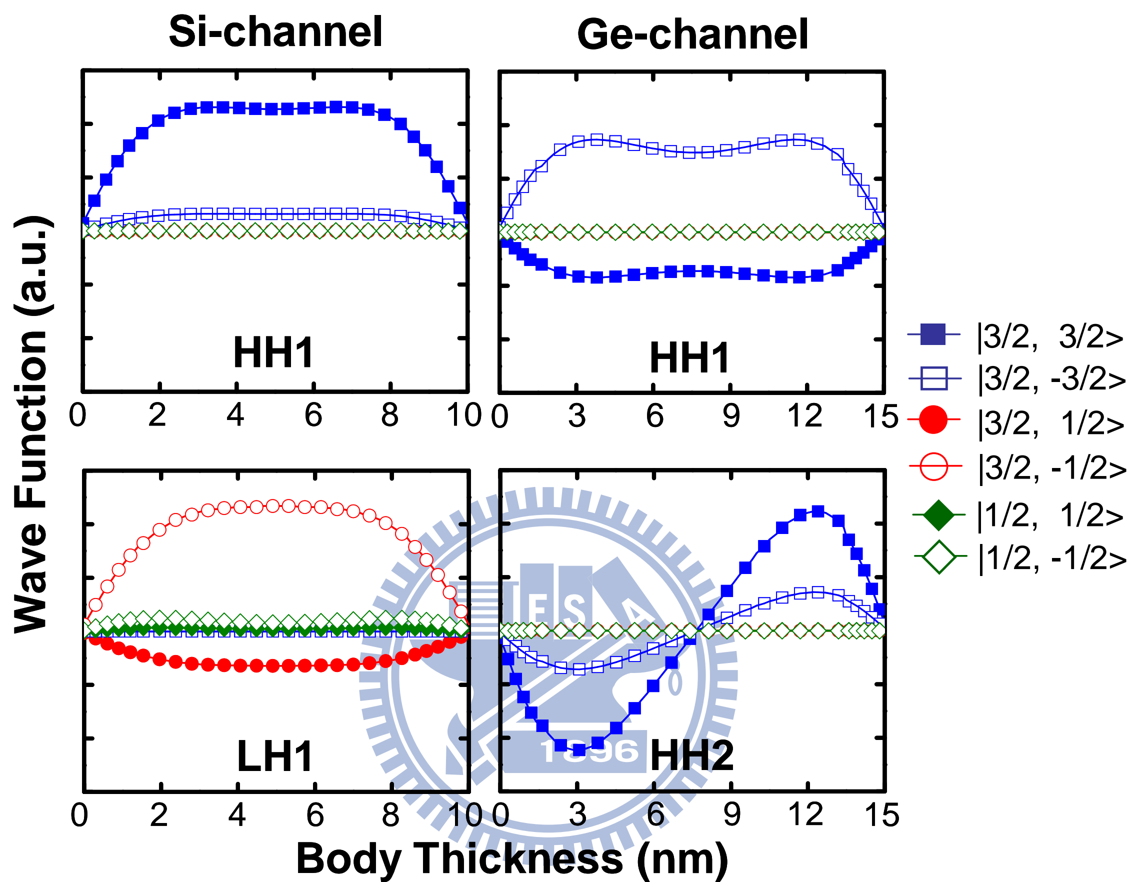


Fig. 4.4 The wave-functions at the zone center of the lowest two subbands in a Si-channel and Ge-channel

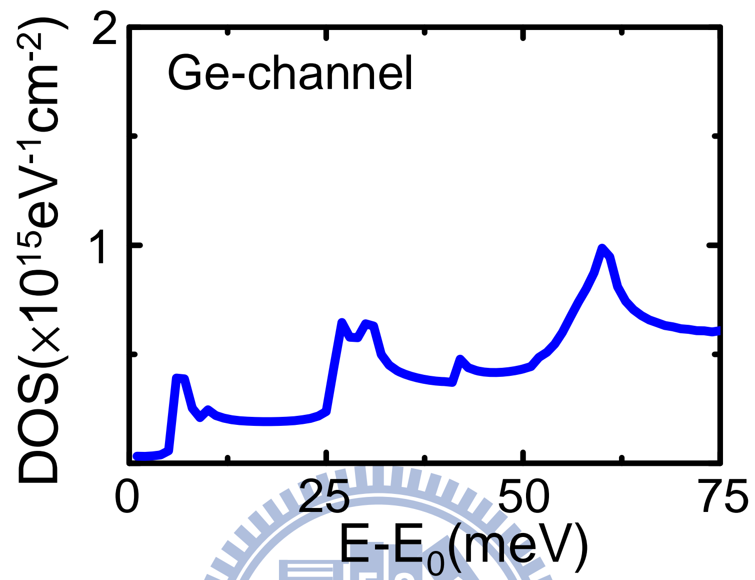


Fig. 4.5 The 2D hole density of state in a Ge-channel.

Table 4.1. The relevant material parameters and scattering parameters used in the Monte Carlo simulation for both Si and Ge. The γ_1, γ_2 and γ_3 are Luttinger parameters. The a_v, b, and d are the Bir-Pikus deformation potentials. The C_{11} and C_{12} are elastic constants. The Ξ and D_tK are the average acoustic and optical deformation potential, respectively. The $\hbar\omega$ is the phonon energy. The Δ is the average step height and the Λ is the correlation length.

Material paramters

	γ_1	γ_2	γ_3	a_v (eV)	b (eV)	d (eV)	C_{11} (dyn/cm^2)	C_{12} (dyn/cm^2)
Si	4.285	0.339	1.446					
Ge	13.38	4.24	5.69	2.0	-2.2	-4.4	1.2853×10^{12}	4.826×10^{11}

Scattering paramters

	Ξ (eV)	D_tK (10^8eV/cm)	$\hbar\omega$ (meV)	Δ (nm)	Λ (nm)
Si	9.2	13	62	0.32	3.0
Ge	11	6	38	0.368	3.0

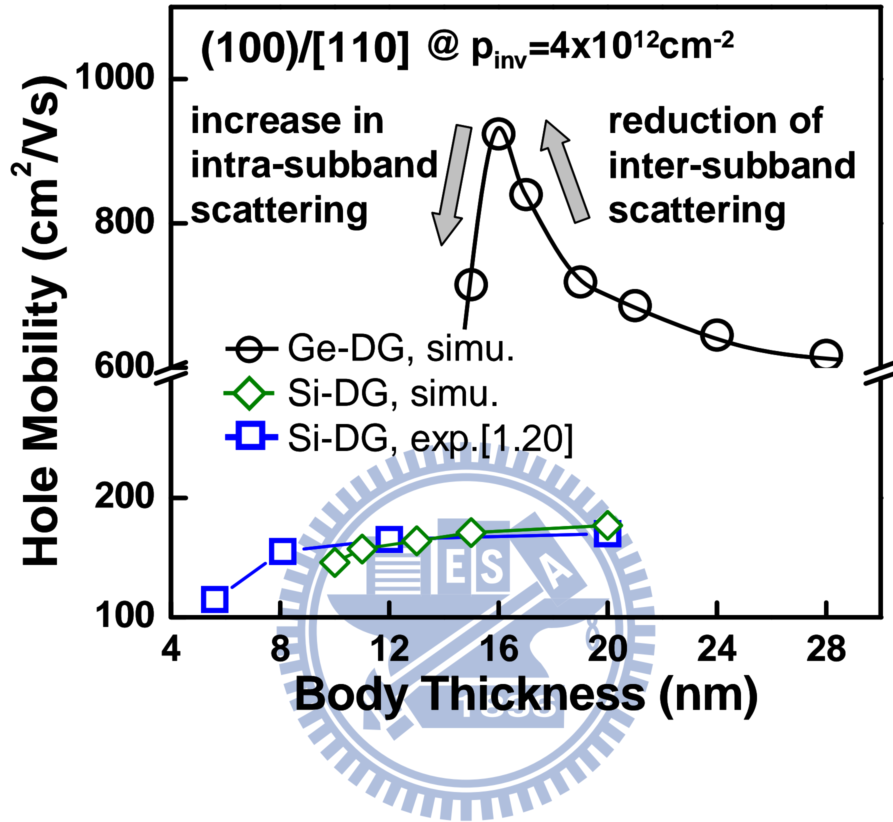


Fig. 4.6 Simulated hole mobility as a function of a body thickness in (100)/[110] Si- and Ge-channel DG-pMOSFETs. The experimental result for Si-channels is plotted for comparison.

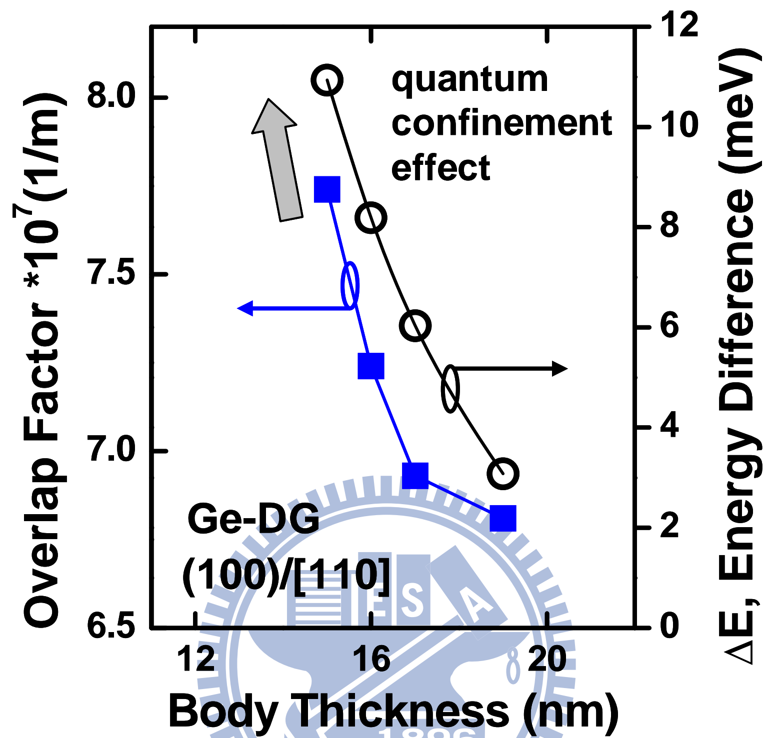


Fig. 4.7 The body thickness dependence of an overlap factor and an energy difference between the lowest two subbands in (100)/[110] Ge-channel DG-pMOSFETs.

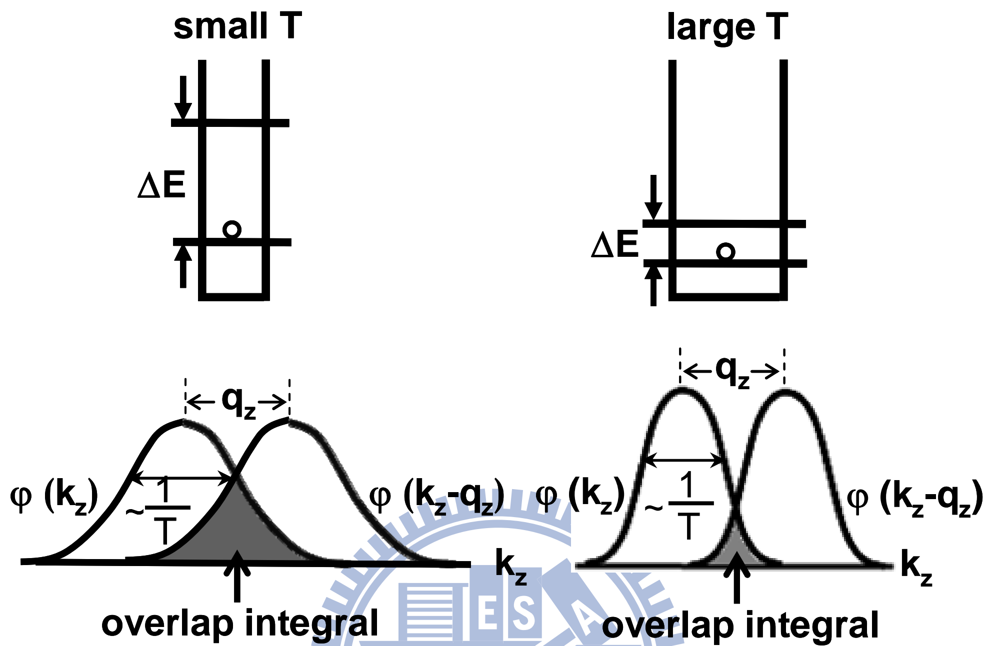


Fig. 4.8 Illustration of the body thickness dependence of valence subband energy and overlap factor. The shaded region corresponds to an overlap integral. A narrower quantum well has a larger energy separation between subbands and a larger overlap factor.

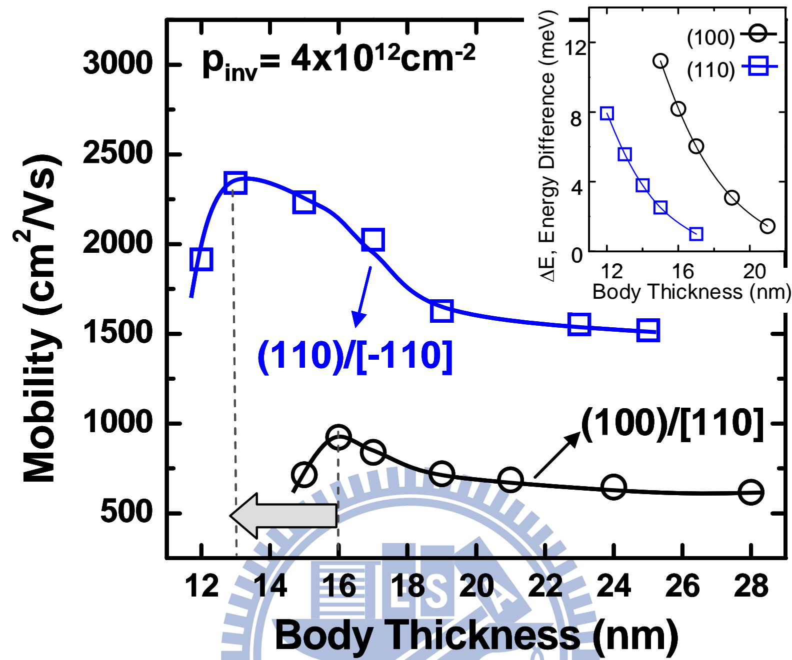
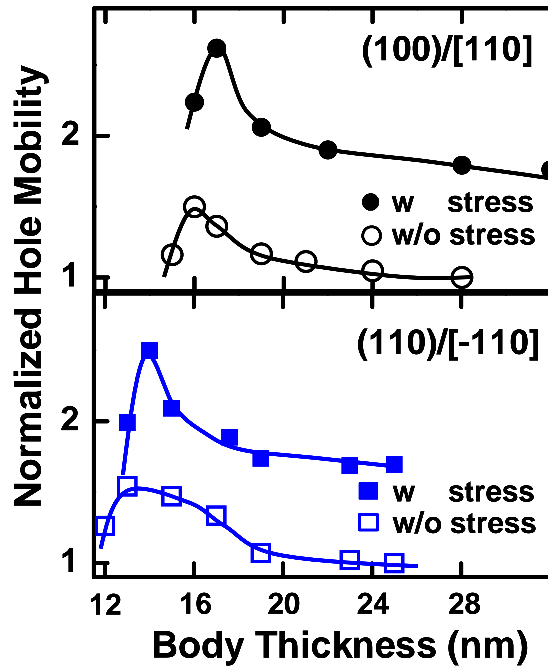
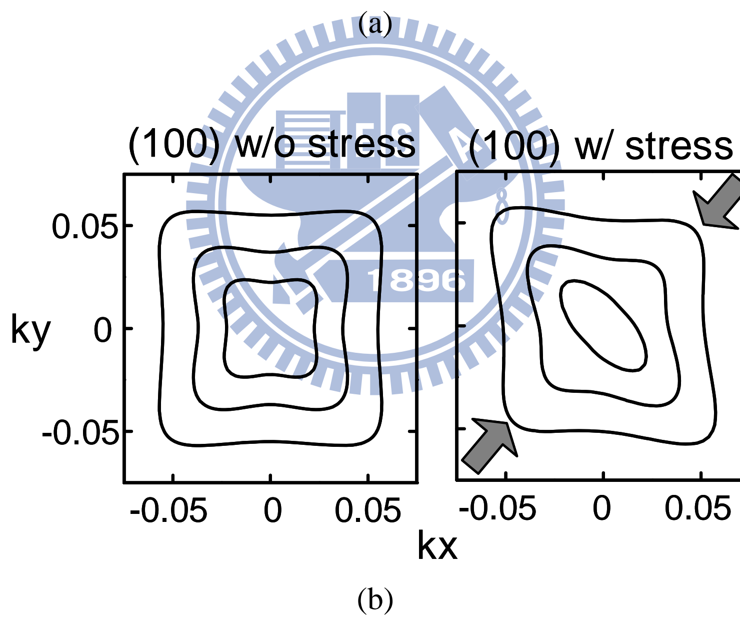


Fig. 4.9 Comparisons of the hole mobility and subband energy difference in (100)/[110] and (110)/[-110] Ge-channels.



(a)



(b)

Fig. 4.10 (a) Ge hole mobility as a function of a body thickness in (100)/[110] and (110)/[-110] channel directions with and without an uniaxial compressive stress of 0.3GPa. The mobility is normalized to the one without stress effect. (b) The constant energy contours in (100) substrate are plotted. The constant energies are 10, 25 and 50 meV.

Chapter 5

Bipolar Charge Trapping Induced Anomalous Negative Bias-Temperature Instability in HfSiON Gate Dielectric pMOSFETs

5.1 Preface

Negative bias temperature (NBT) instability has been recognized as a major reliability concern in ultra-thin gate dielectric MOSFETs. It occurs in p-type devices and manifests itself as negative shifts of threshold voltage due to positive oxide charge trapping and interface generation under a negative gate voltage stress. Compared to a SiO_2 gate dielectric, the NBT instability (NBTI) in high permittivity (high-*k*) gate dielectric pMOSFETs has been less explored.

In previous NBTI studies [5.1]-[5.3], a conventional "stress-and-sense" method was used, which introduces a switching delay between stress and sense of up to a few seconds. For high-*k* gate dielectrics such as HfSiON, a significant post-stress transient effect was reported due to high-*k* dielectric charge trapping/detrapping. The ignorance of high-*k* charge trapping/detrapping in a switching delay may lead to an erroneous interpretation of measurement data and underlying physical mechanisms. Thus, to retrieve the important information between stress and sense, a fast transient measurement technique [1.28][1.29] with a resolution of microseconds is employed. By using this technique, the mode of the NBT-induced drain current instability is characterized. Both current enhancement and degradation modes are observed in a HfSiON pMOSFET [5.4]. A physical model based on bipolar charge trapping and trap

generation in a high-*k* gate dielectric is proposed to explain the instability modes.

The devices used here are p-type MOSFETs with a polysilicon electrode and a HfSiON-SiO_2 gate stack. The gate length ranges from 0.08μm to 1.2μm, and the gate width ranges from 0.16μm to 10μm. The physical thickness of the high-*k* layer and the interfacial SiO_2 layer (IL) is 2.5nm and 1.4nm, respectively. The equivalent oxide thickness is 1.8nm. Detailed fabrication process and device characteristics were reported in [5.5][5.6]. To reduce the switching delay in characterization, our measurement system is computer-automated, including high-speed switches, an operational amplifier, and a digital oscilloscope, as shown in Fig. 5.1. The high speed switches minimize a switching delay down to microseconds between stress and drain current measurement. The detailed measurement procedures were described in [1.28][1.29]. Other measurement techniques, such as charge pumping (CP) technique, single charge emission measurement and carrier separation measurement are utilized to monitor charge trapping/detrapping and trap generation.

In this work, the negative bias temperature induced drain current instability is first characterized in control SiO_2 pMOSFETs. The BTI in HfSiON nMOSFETs and pMOSFETs are also shown for a comparative study. Then, the dependence of stress time, gate voltage and temperature on drain current instability in HfSiON pMOSFETs is investigated. We propose a bipolar charge trapping model along with trap generation to explain the observed phenomena. Finally, three characterization methods, single charge emission, charge pumping and carrier separation measurement are utilized to justify the model.

5.2 Anomalous Turn-around in Linear Drain Current Evolutions

The V_g/V_d waveforms in the transient measurement are depicted in Fig. 5.2

during stress phase and measurement phase. Fig. 5.3 shows the evolutions of NBT stress-induced linear drain current change ($\Delta I_{d,lin}$) in control SiO_2 and HfSiON pMOSFETs. The device dimension is W/L=10μm/0.2μm. The stress V_g is -2.8V, and the linear drain current ($I_{d,lin}$) is measured at V_g/V_d= -1.2V/-0.2V. As shown in the figure, $\Delta I_{d,lin}$ decreases monotonically with stress time in a SiO_2 control device, while a turn-around characteristic of $\Delta I_{d,lin}$ versus stress time is obtained in a HfSiON pMOSFET. Note that one may fail to observe this anomalous turn-around behavior by using a conventional measurement setup such as Agilent 4156 due to a switching delay of up to a few seconds. Furthermore, the NBTI and its counterpart PBTI in a nMOSFET are compared in Fig. 5.4. The stress V_g is -2.8V for the pMOSFET and 2.2V for the nMOSFET. As shown in the figure, the $\Delta I_{d,lin}$ in a nMOSFET (PBTI) is negative in the entire stress period and no turn-around feature like the NBTI is observed. More interestingly, the NBTI and the PBTI in HfSiON MOSFETs exhibit distinctly different post-stress drain current evolutions in Fig. 5.5. The PBTI exhibits a drain current recovery, as reported in literature [1.28]. However, the NBTI shows persistent drain current degradation after stress. The post-stress $I_{d,lin}$ degradation in a high-*k* pMOSFET implies trapped electron emission from a high-*k* gate dielectric after stressing V_g is removed.

In Fig. 5.6 and Fig. 5.7, NBT induced $\Delta I_{d,lin}$ at various stress V_g and temperatures are shown, respectively. The stress V_g ranges from -1.6V (result not shown in Fig.5.6) to -2.8V with all other terminals grounded and the temperature is from 25°C to 125°C. For a stress V_g weaker than -2V (selectively shown for clarity), $\Delta I_{d,lin}$ is negative (degradation mode) and decreases monotonically with stress time. The degradation aggravates with a larger stress $|V_g|$ (more negative). For a stress V_g stronger than -2V or a higher stress temperature, the drain current instability shows a different feature.

The $I_{d,lin}$ initially increases with stress time (enhancement mode) and shortly evolves into degradation mode ($\Delta I_{d,lin}<0$), featuring a turn-around characteristic. The drain current enhancement has a positive dependence on stress $|V_g|$ and temperature. The transition time for the $I_{d,lin}$ evolving from enhancement mode to degradation mode is mostly within seconds in the bias range of interest. Fig. 5.8 demonstrates the dependence of $\Delta I_{d,lin}$ on stress V_g at different stress times. For t=0.1s, a lower stress $|V_g|$ (-1.4V~ -2V) induces a $I_{d,lin}$ degradation while a larger stress $|V_g|$ results in an enhancement. This trend remains for t=10s, but the turn-around $|V_g|$ is slightly increased. For a longer stress time (e.g., t=1000s), the dependence of $\Delta I_{d,lin}$ on V_g returns to a normal degradation mode as in SiO_2 gate dielectric transistors, and a larger stress $|V_g|$ results in a larger degradation [5.7][5.8]. The stress temperature dependence of $\Delta I_{d,lin}$ is shown in Fig. 5.9. For a short stress time (e.g., t=10s), $\Delta I_{d,lin}$ changes from negative at low temperatures to positive at high temperatures. But for a longer stress time (e.g., t=1000s), the $I_{d,lin}$ degradation increases monotonically with stress temperature. The positive temperature dependence of the $I_{d,lin}$ degradation in a high-*k* MOSFET can be realized due to temperature accelerated high-*k*/IL trap generation because of thermo-chemical reaction [5.9].

5.3 Bipolar Charge Trapping Model

In a negative V_g stress, two carrier injection processes affect I_d instability, (i) valence band electron injection from the p^+ poly-gate into high-*k* traps (I_d enhancement mode) and (ii) hole injection from the inverted channel into high-*k*/IL traps (I_d degradation mode). Therefore, available trap states in a high-*k* dielectric, either pre-existing traps or stress generated traps, and injected carrier fluence should be considered in a NBT instability model. Fig. 5.10 illustrates the energy band

diagrams in equilibrium (Fig. 5.10(a)) and in various NBT stress conditions, for example, low V_g and low temperature stress (Fig. 5.10(b)), low V_g and high temperature stress (Fig. 5.10(c)), and high V_g and low temperature stress (Fig. 5.10(d)). In thermal equilibrium, trap states with energy (E_t) below the Fermi level (E_F) are occupied by electrons while those above E_F are empty. The shaded area in Fig. 5.10 represents the occupied states in the high-*k* layer. When a low stress $|V_g|$/ temperature is applied (Fig. 5.10(b)), the empty high-*k* traps available for poly-gate valence electron injection are very limited due to a small band-bending (ΔE_t) in a high-*k* gate dielectric. In this case, electron trapping into the high-*k* layer is negligible, and $\Delta I_{d,lin}$ is dominated by hole injection from the inverted channel, leading to a $I_{d,lin}$ degradation. In this regime, a larger $|V_g|$ aggravates $\Delta I_{d,lin}$ due to a larger hole injection current, which is in agreement with our measured result in Fig. 5.8. As stress temperature or $|V_g|$ increases, more poly-gate electrons can inject into pre-existing high-*k* traps either because of thermally assisted tunneling (Fig. 5.10(c)) or because of more available empty states due to a larger band-bending (Fig. 5.10(d)). In these stress conditions, both electron trapping and hole trapping into the high-k layer are possible. The measurement result in Fig. 5.6 and Fig. 5.7 implies that electron trapping is dominant in the initial stress period and hole trapping gradually supersedes electron trapping due to new hole trap creation in the high-*k* and IL layers, thus resulting in a turn-around feature of the $I_{d,lin}$ evolution.

5.4 Single Charge Emission and Charge Pumping

To confirm our bipolar charge trapping model for NBT instability, post-stress trapped charge emissions are characterized. The purpose of this characterization is to identify injected charge species during stress. The detail of this method was described

in our previous papers for trapped electron emission from HfSiON in a nMOSFET [1.28] and trapped hole emission from SiO_2 in a pMOSFET [5.10]. Fig. 5.11 shows our measured post-stress I_d evolution patterns in small area devices after low (-1.5V) and high (-2.2V) V_g stress, respectively. The transistors have W/L=0.16μm/0.08μm. The waveforms are shown in Fig. 5.12. The stress time (or exactly the charge filling time) for both cases is 0.2s, and the post-stress measurement condition is V_g~V_t to magnify the effect of single charge on drain current and V_d= -0.2V. In Fig. 5.11, trapped charge emission is manifested by a staircase-like jump in the drain current. For a pMOSFET, an upward shift (increase in $|I_d|$) corresponds to a single hole emission, and a downward shift corresponds to a single electron emission. Notably, only trapped hole emissions are found for the low V_g stress (Fig. 5.11(a)) while both electron and hole emissions are obtained for the high V_g stress (Fig. 5.11(b)). This single charge emission result provides direct evidence of bipolar charge trapping in a high V_g stress condition. Fig. 5.13 shows the single charge emission induced current jumps in a post-PBT stress nMOSFET. Only three trapped electrons are observed and the post-stress drain current exhibits full recovery. It should be remarked that we did not observe any random telegraph signal at the post-stress measurement biases, indicating that the observed current jumps in Fig. 5.11 are attributed to injected charge emissions.

We also characterize high-*k*/IL trap generation for low and high V_g stress by using a charge pumping method. A two-frequency (5kHz and 1MHz) technique is used to separate IL/Si interface traps (D_{it}) from bulk high-*k* traps (N_{HK}) [5.11]. The characterization procedure is described in Fig. 5.14. The high frequency CP current is contributed by D_{it} and the difference between the CP currents of the two frequencies reflects high-*k* trap density N_{HK}.

$$N_{HK} = \frac{1}{WLq}\left[\frac{(I_{CP}@5kHz)}{5kHz} - \frac{(I_{CP}@1MHz)}{1MHz}\right]$$

Fig. 5.15 shows the extracted D_{it} and N_{HK} versus stress time for stress V_g=-1.5V and -2.2V. No new traps are created in a low V_g (-1.5V) stress even for a stress time of t=1000s, indicating that the $I_{d,lin}$ degradation at a low stress V_g is mainly attributed to hole trapping into pre-existing high-*k* traps. On the other side, both interface trap and bulk high-*k* trap generation is observed in a high V_g (-2.2V) stress.

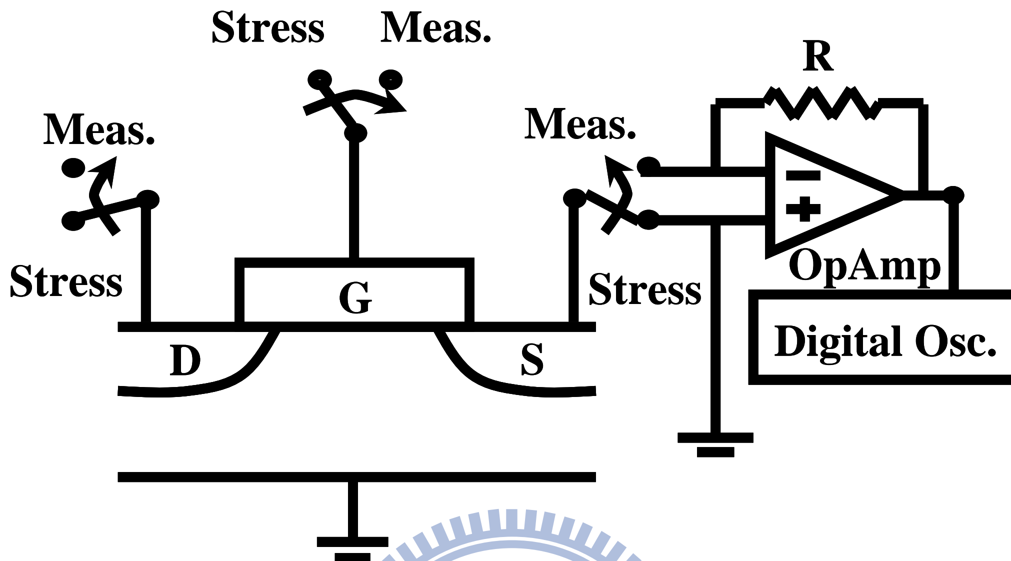
5.5 Carrier Separation Measurement

In addition to available traps for electron and hole injection, another factor affecting NBT instability mode is the fluence of injected carriers during stress. A carrier separation measurement was performed to explore the effect of injected carrier fluence on I_d instability. Fig. 5.16 illustrates the carrier separation measurement and the carrier flow in a high-*k* pMOSFET under $-V_g$ stressing. The hole injection current from the inverted channel constitutes the source/drain current (i.e., $I_{S/D}$) and the electron injection current from the p^+ poly-gate flows to the substrate (i.e., I_{sub}). Both can be measured separately through the connected source and drain measurement configuration. Fig. 5.17(a) shows the measured hole and electron currents versus stress gate voltage at T=25°C. One point is worth noting. Holes are the dominant conduction carrier at a low stress $|V_g|$. As a stress $|V_g|$ increases, an electron current becomes dominant. Thus, electron filling effect is more significant than hole filling at a higher stress $|V_g|$. This trend is consistent with the measured result in Fig. 5.8, i.e, $I_{d,lin}$ degradation in a low V_g region and $I_{d,lin}$ enhancement in a high V_g region in the initial stress period.

As stress temperature increases to 100°C (Fig. 5.17 (b)), the electron current is enhanced to a larger extent, compared to the hole current and thus it supersedes the hole current at a smaller stress V_g. This result is in agreement with our thermally-assisted electron tunneling model in Fig. 5.10(c) and can well explain the increased $I_{d,lin}$ enhancement at a higher temperature in a low stress V_g region (Fig. 5.7).

5.6 Summary

Various NBT induced drain current instability modes in a pMOSFET with a HfSiON-SiO_2 gate stack are investigated by using a fast transient measurement method. The drain current enhancement is observed in the initial stress period in a high stress V_g or at a high temperature. Electron trapping, hole trapping and new trap generation are found to be responsible for the drain current instability modes. The impact of stress V_g, temperature and stress time on NBT instability is characterized. The drain current instability modes are summarized in Table 5.1. In high $|V_g|$ and/or high temperature stress, electron trapping into pre-existing high-*k* traps is dominant in the initial stress period, thus causing an I_d enhancement. As stress continues, hole injection and new hole trap creation in HK/IL layers eventually become dominant, giving rise to a turn-around characteristic of the drain current evolution with time. For low V_g stress, the I_d instability is dictated by hole injection throughout the entire stress period, and thus $\Delta I_{d,lin}$ decreases monotonically with stress time. In order to extrapolate a reliable NBTI lifetime, the above mechanisms should be carefully considered in a voltage-accelerated stress.



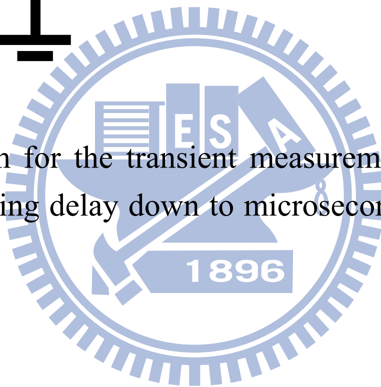


Fig. 5.1 Schematic diagram for the transient measurement system. The high speed switches minimize a switching delay down to microseconds between stress and drain current measurement.

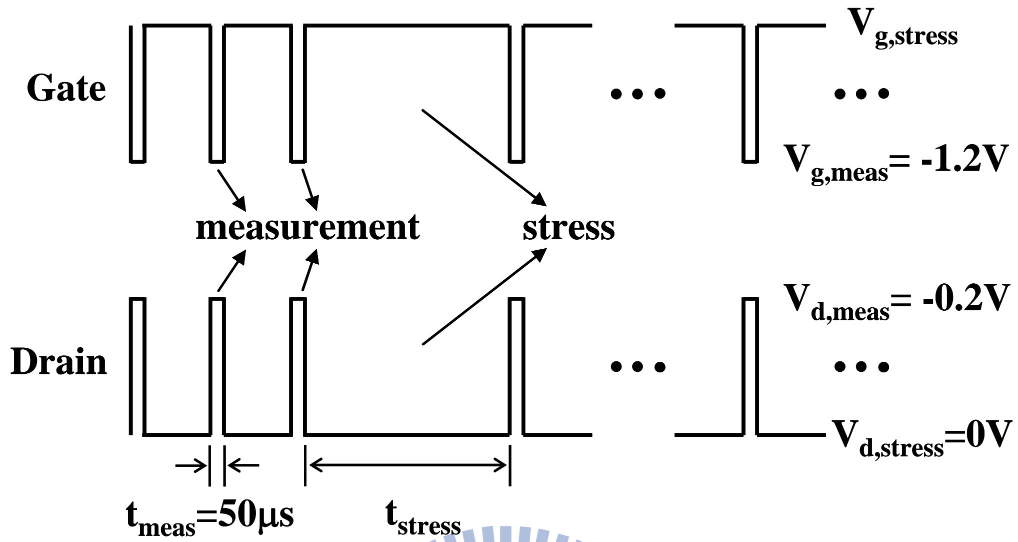


Fig. 5.2 The waveforms applied to the gate and drain in the transient measurement.

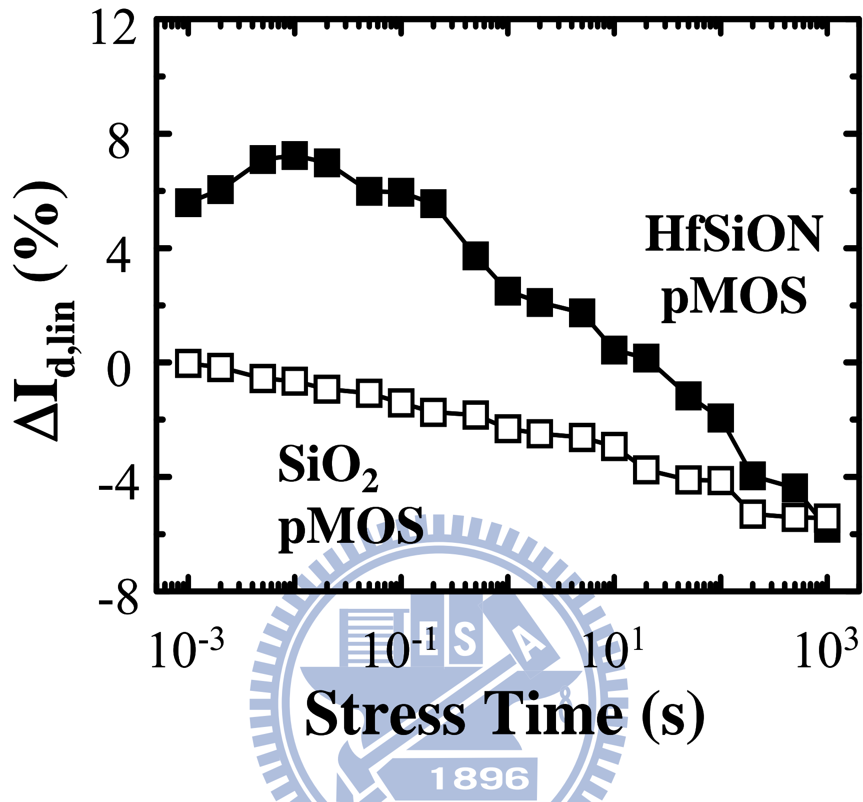


Fig. 5.3 NBT stress induced linear drain current change ($\Delta I_{d,lin}$) in SiO_2 and HfSiON pMOSFETs. The stress V_g is -2.8V and the linear drain current ($I_{d,lin}$) is measured at V_g/V_d=-1.2V/-0.2V.

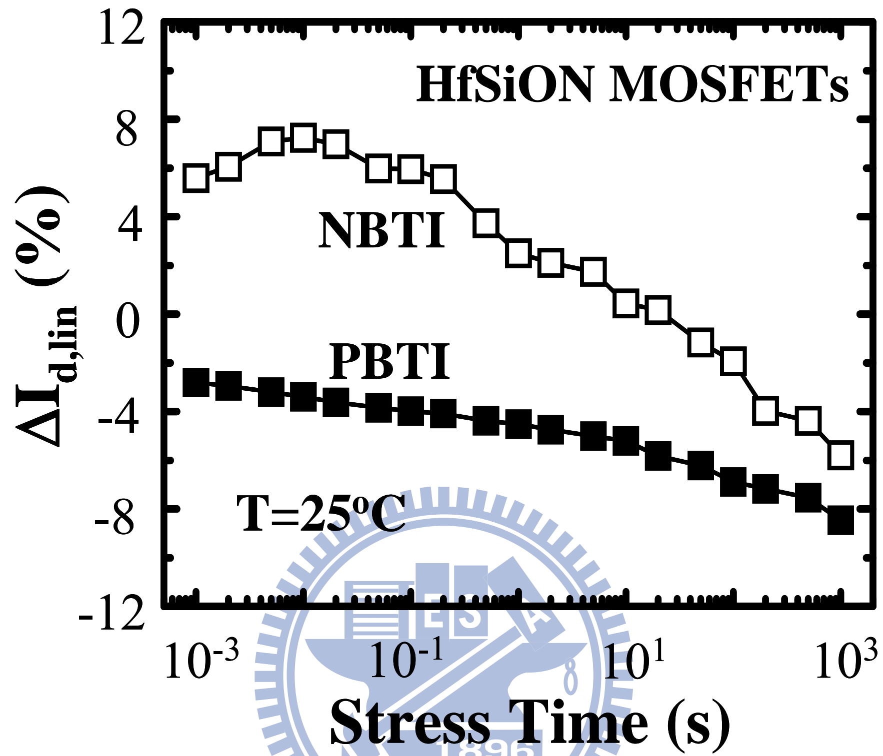


Fig. 5.4 Linear drain current change ($\Delta I_{d,lin}$) in a pMOSFET (NBTI) and in a nMOSFET (PBTI). The stress V_g is -2.8V for the pMOSFET and 2.2V for the nMOSFET.

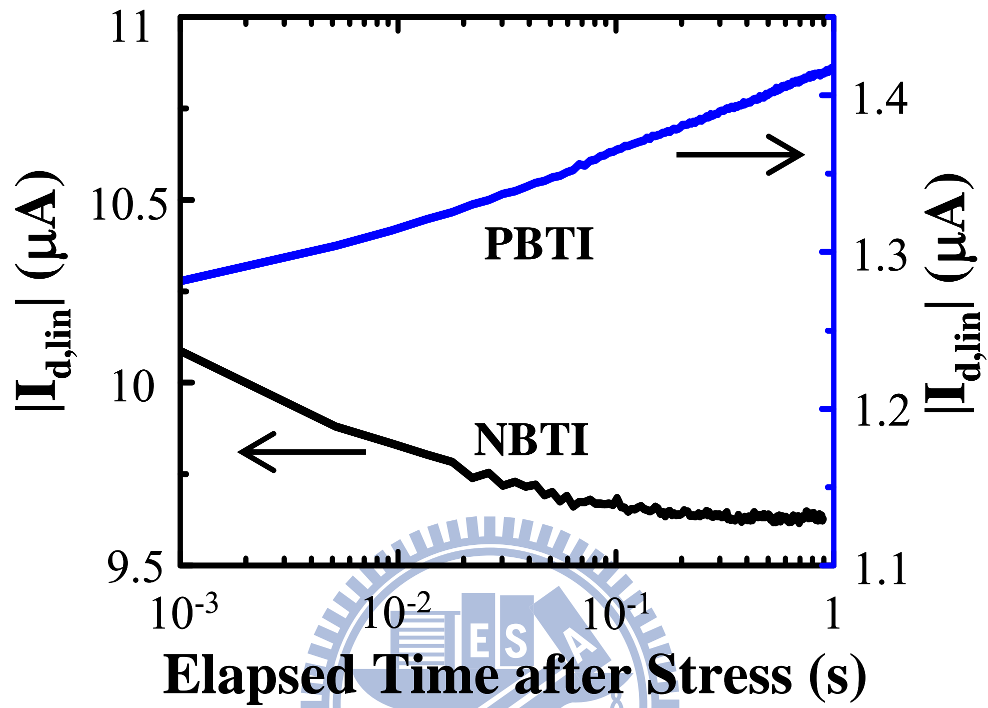


Fig. 5.5 $|I_{d,lin}|$ as a function of elapsed time after stress. The drain current recovery is observed in a nMOSFET, while the NBTI shows persistent post-stress current degradation.

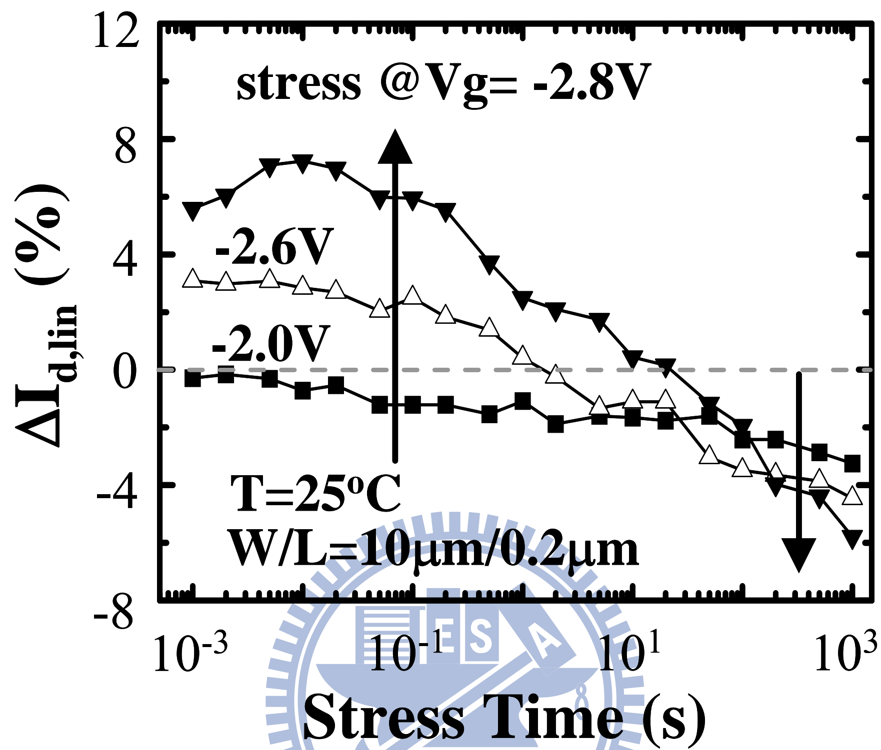


Fig. 5.6 NBT stress induced drain current evolution for different stress V_g. Drain current enhancement in an initial stage of stressing is observed for high stress V_g (-2.6V and -2.8V).

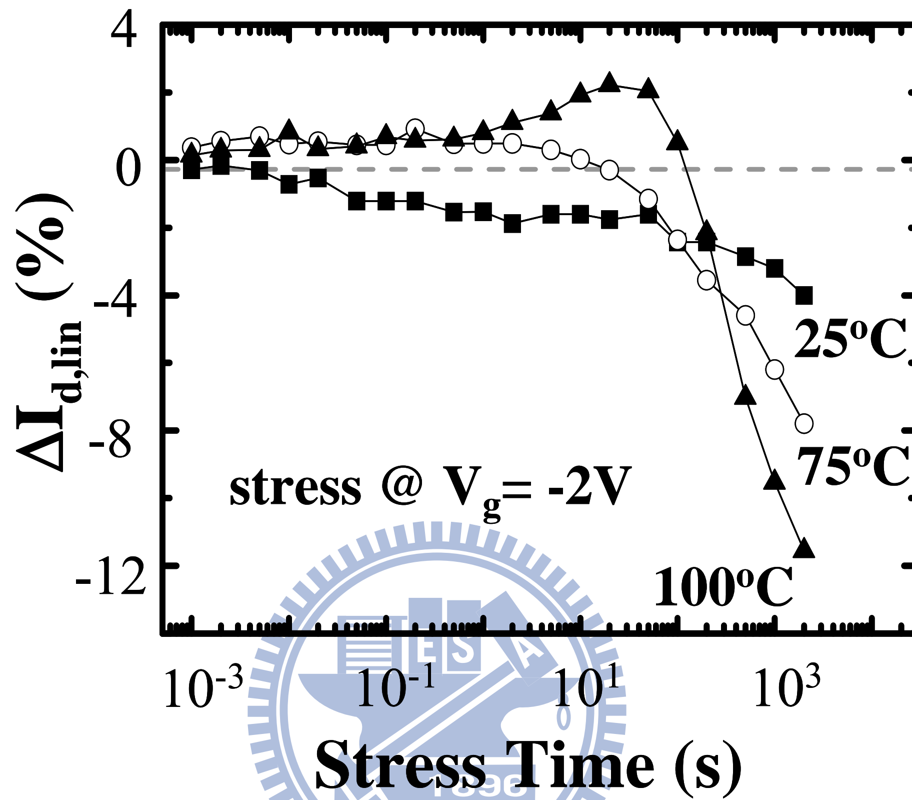


Fig. 5.7 NBT stress induced drain current evolution for different stress temperatures. Drain current enhancement in an initial stage of stressing is observed for high stress temperatures.

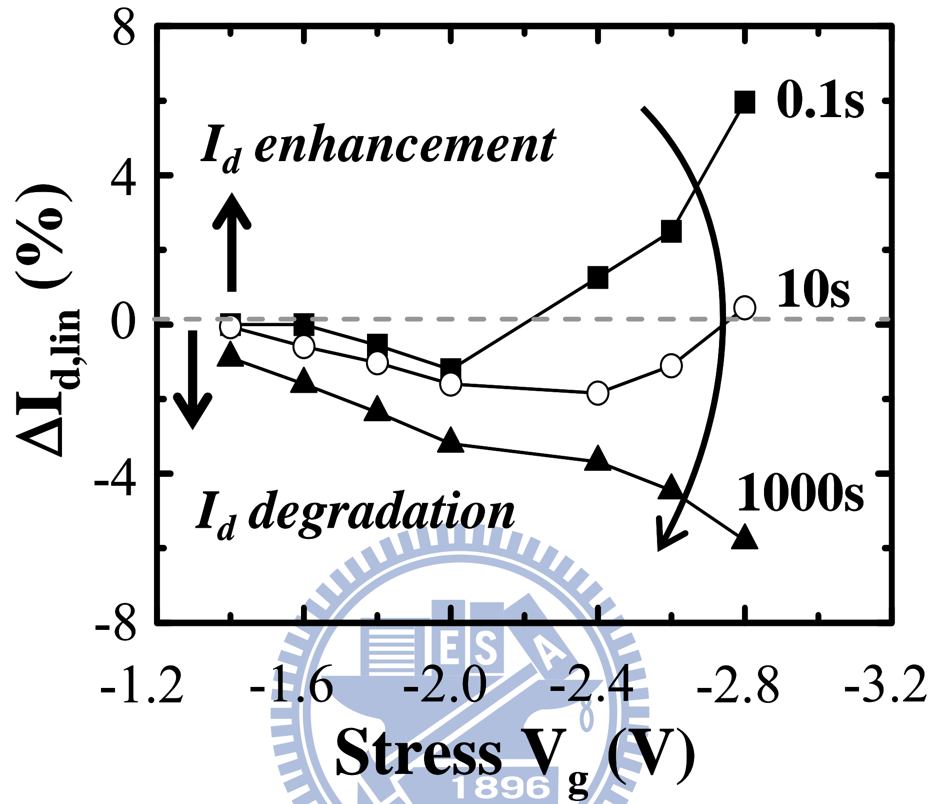


Fig. 5.8 Stress V_g dependence of $\Delta I_{d,lin}$ at different stress times. For a short stress time (t=0.1s and 10s), $\Delta I_{d,lin}$ can be positive or negative, depending on stress V_g. For a longer stress time (t=1000s), the dependence returns to a normal degradation mode as in SiO_2 gate dielectric transistors.

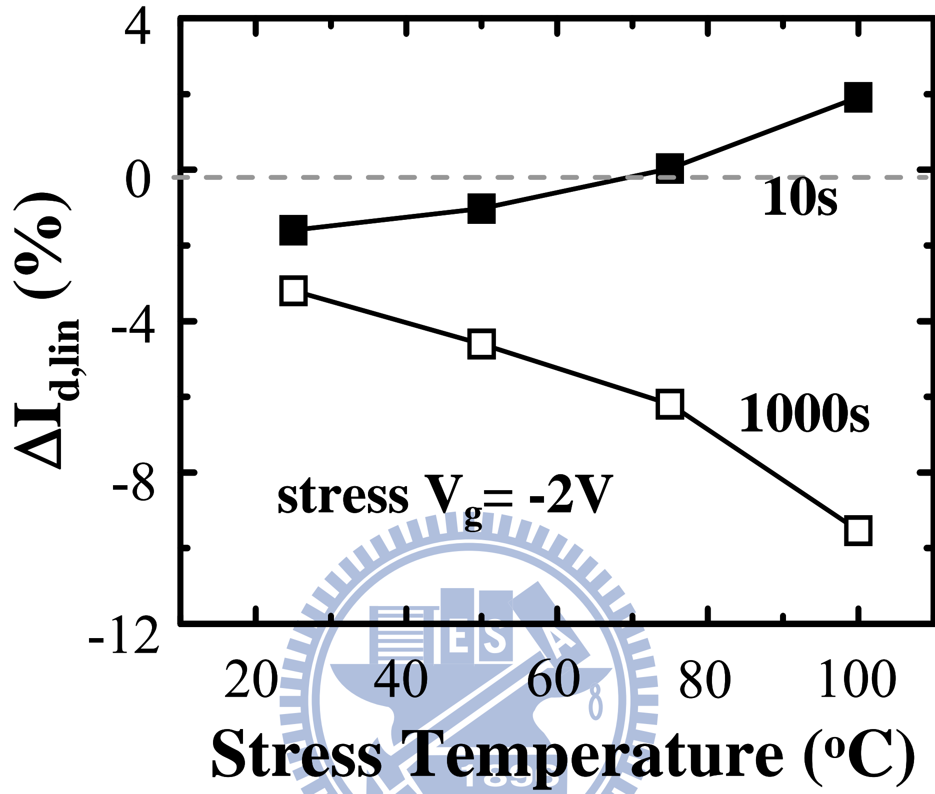


Fig. 5.9 Stress temperature dependence of $\Delta I_{d,lin}$.

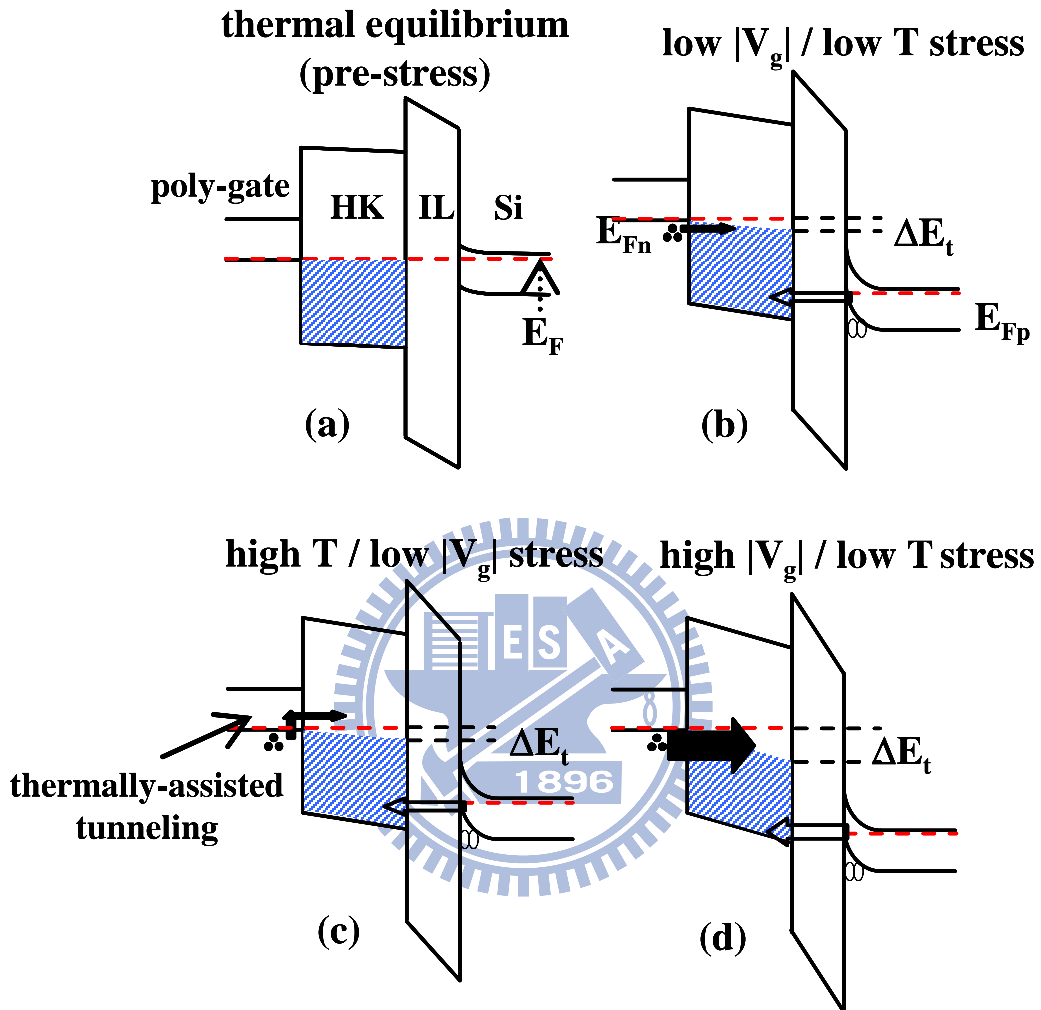
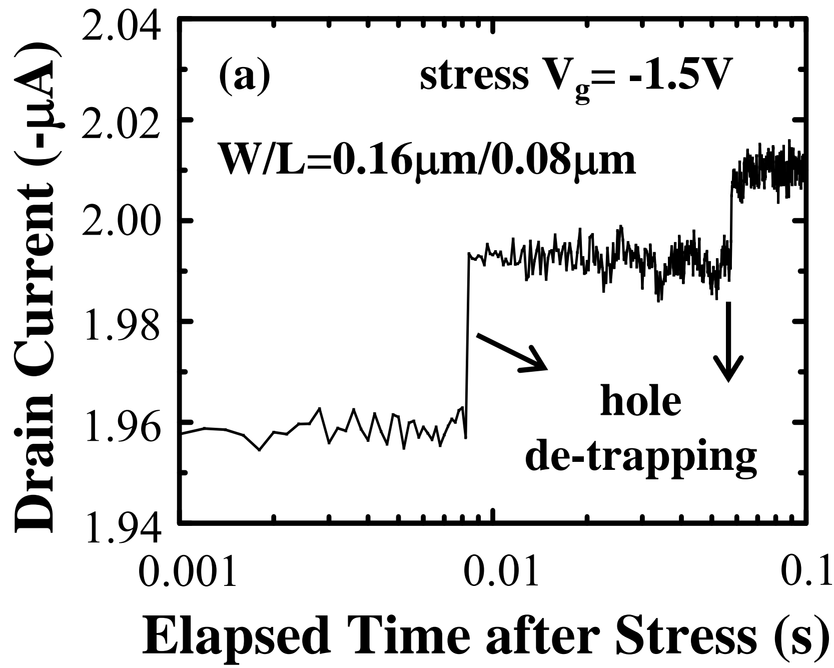


Fig. 5.10 Schematic representation of an energy band diagram and charge injection processes in (a) thermal equilibrium, (b) low $|V_g|$/ low T stress, (c) high T/ low $|V_g|$ stress, and (d) high $|V_g|$/ low T stress. The shaded area represents the occupied trap states in the high-*k* layer. Electron injection from the poly gate and hole injection from the channel are illustrated.



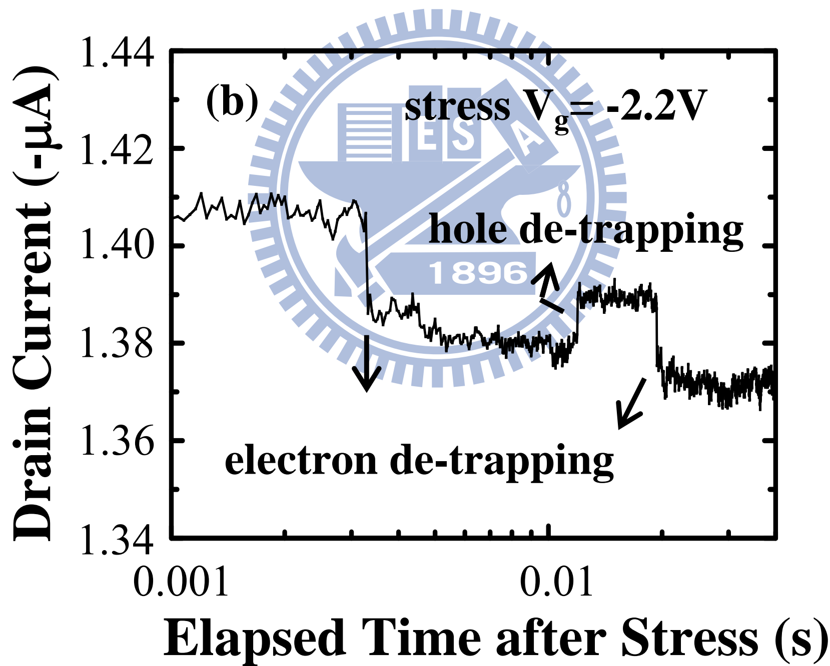
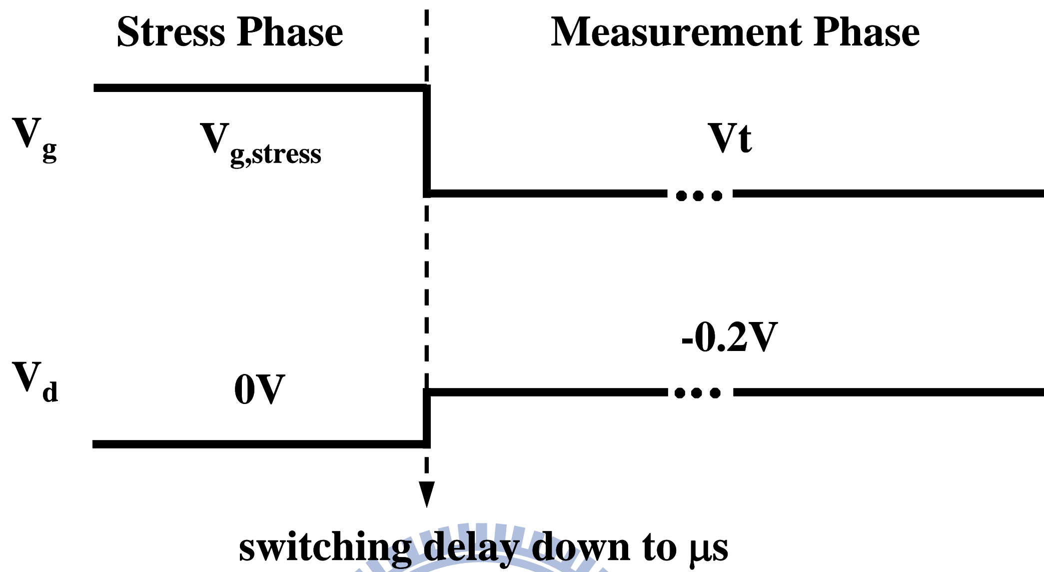


Fig. 5.11 Post-stress I_d evolution patterns in small-area devices after (a) a low $|V_g|$ (-1.5V) stress and (b) a high $|V_g|$ (-2.2V) stress. The post-stress measurement condition is V_g~V_t and V_d=-0.2V.



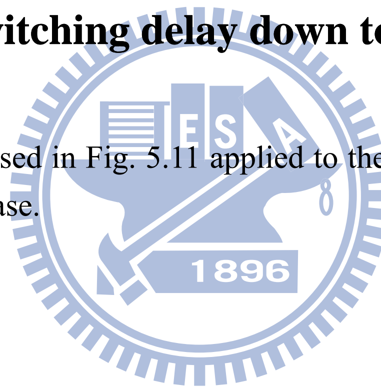


Fig. 5.12 The waveforms used in Fig. 5.11 applied to the gate and drain during stress phase and measurement phase.

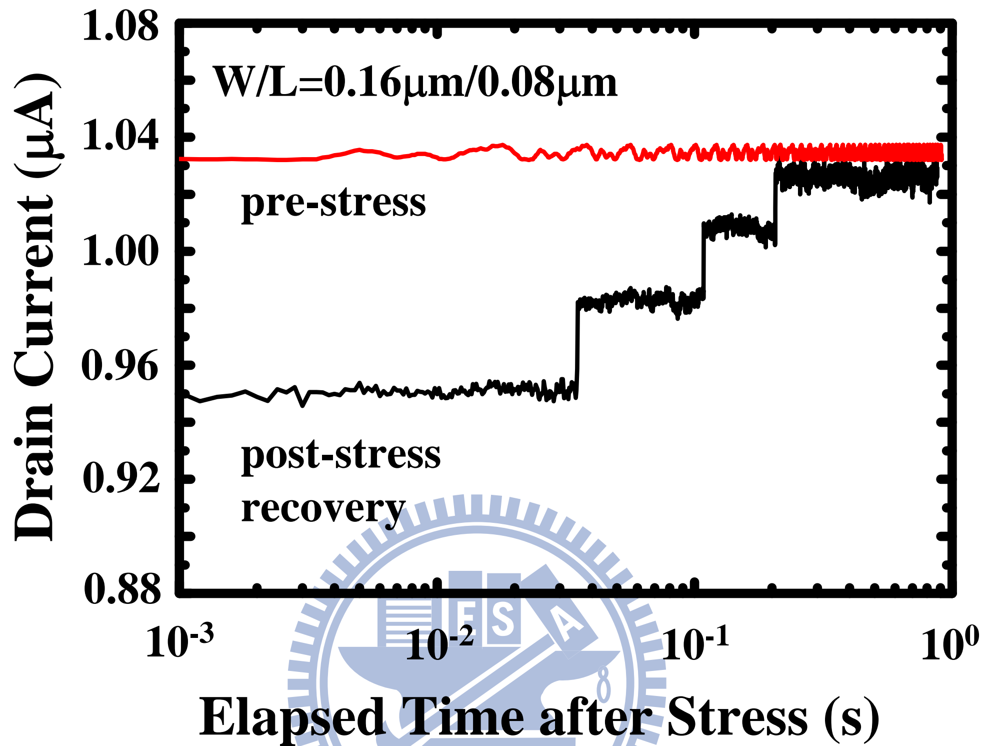


Fig. 5.13 Post-stress I_d evolution patterns after stress at V_g=0.7V for 0.2s in a nMOSFET. The post-stress measurement condition is V_g/V_d=0.3V/0.2V.

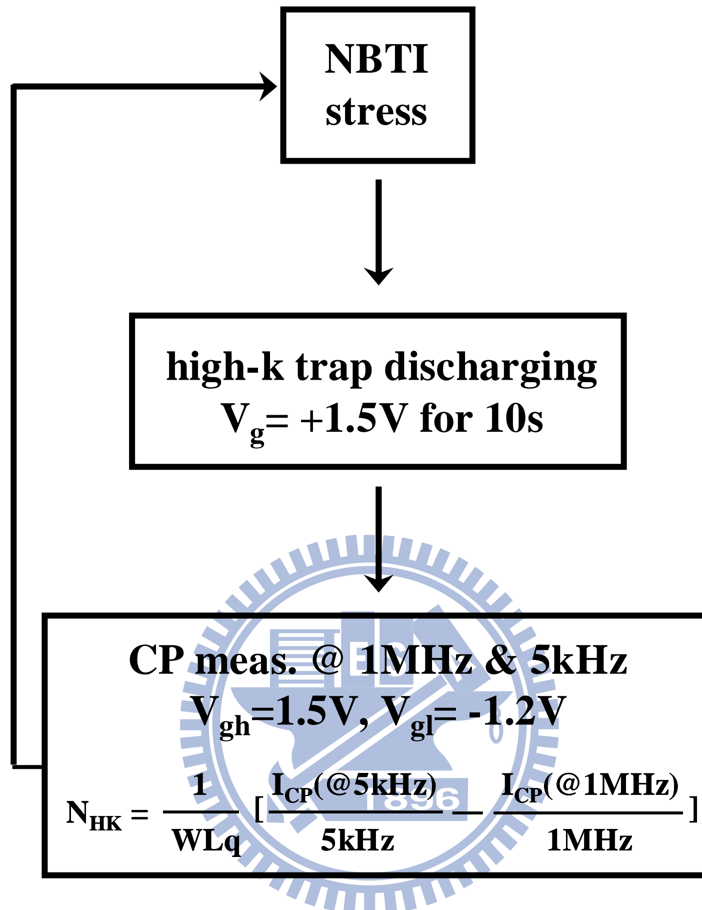


Fig. 5.14 The characterization procedures of two-frequency charge pumping technique for high-*k* trap density extraction.

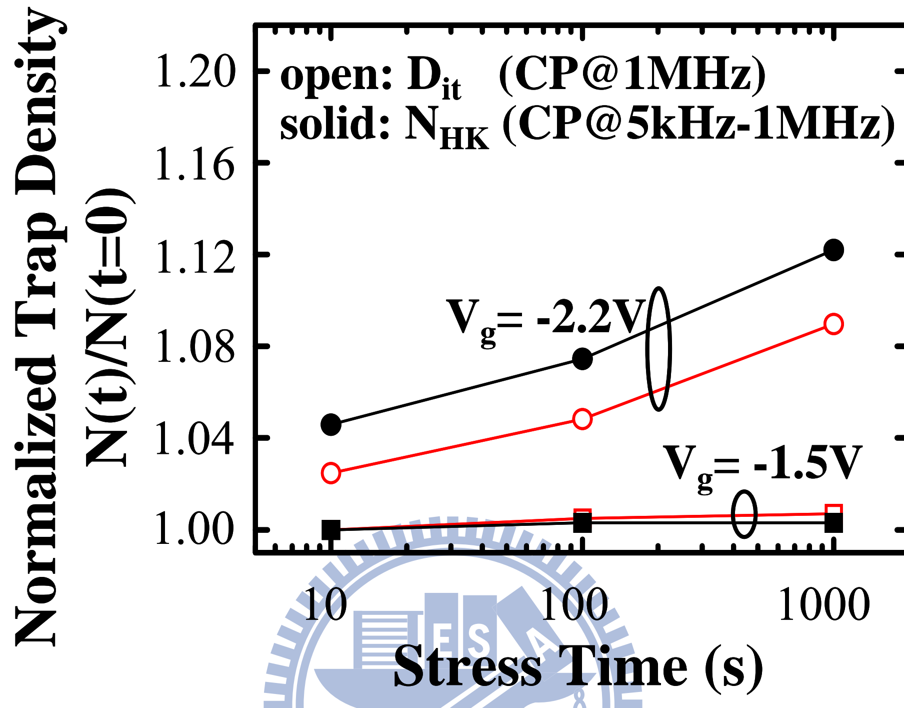


Fig. 5.15 Interface traps (D_{it}) and bulk high-*k* traps (N_{HK}) growth rates in NBT stress at Vg=-1.5V and Vg=-2.2V.

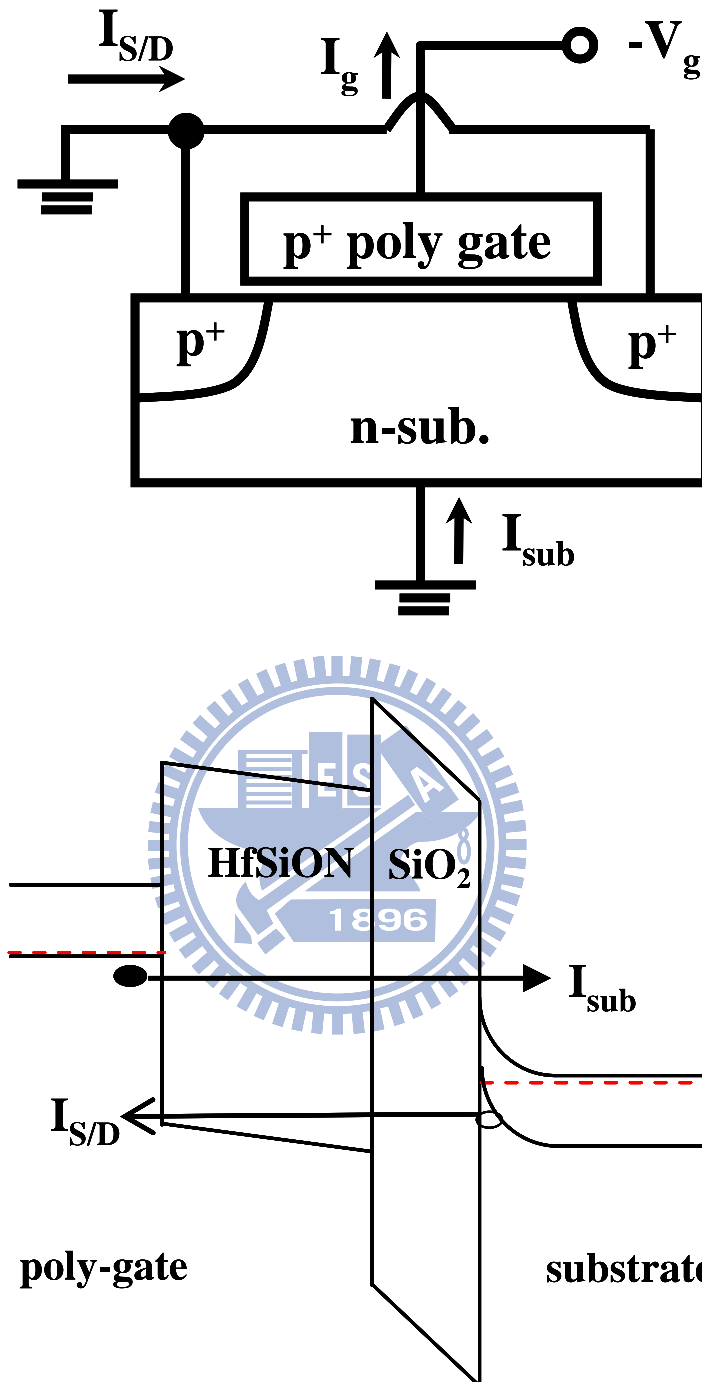
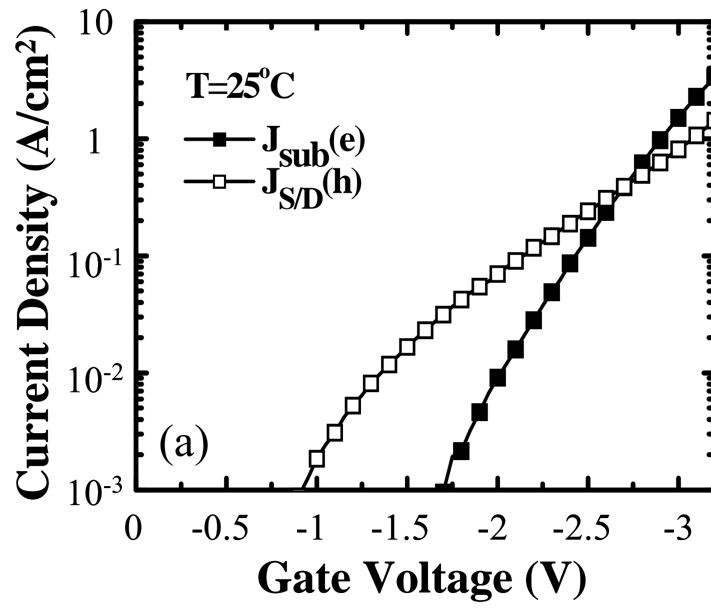


Fig. 5.16 Illustration of charge separation measurement and carrier flow in a high-*k* pMOSFET under $-V_g$ stressing. I_{sub} denotes the electron injection current from the p^+ poly-gate to substrate, and $I_{S/D}$ stands for hole injection current from the inverted channel. Both can be measured separately through the connected source and drain measurement configuration.



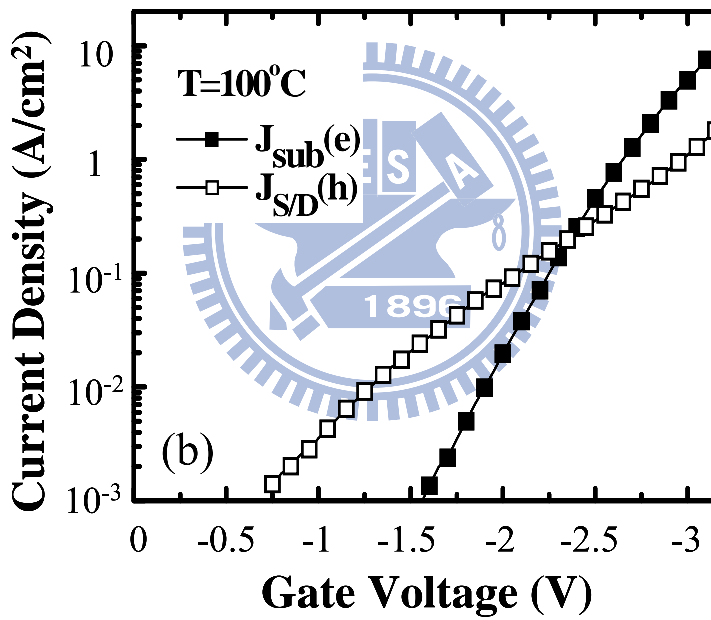


Fig. 5.17 Gate voltage dependence of hole injection current ($I_{S/D}$) and electron injection current (I_{sub}) in a high-*k* pMOSFET, measured at (a) T=25°C and (b) T=100°C.

Table 5.1 Summary of NBT stress caused drain current instability and responsible mechanisms.

Stress Time \ Stress $\|V_g\|$ and T	low $\|V_g\|$	high $\|V_g\|$	high temperature
short	1.Hole trapping into HK traps 2.I_D degradation	1.Electron trapping into HK traps 2.Hole trapping into HK traps 3.I_D enhancement	1.Electron trapping into HK traps via thermally assisted tunneling 2.Hole trapping into HK 3.I_D enhancement
long	1.Hole trapping 2.HK/IL degradation 3.I_D degradation	1.Electron/ hole trapping 2.HK/IL degradation 3.I_D degradation	1.Electron/ hole trapping 2.Accelerated HK/IL degradation 3.I_D degradation

Chapter 6

Conclusions

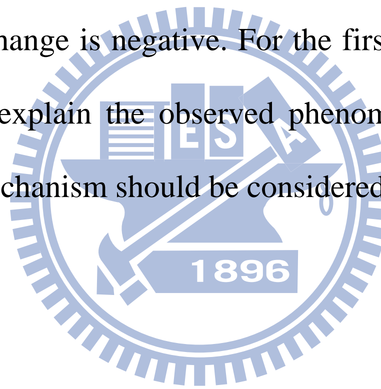
In short, this dissertation has involved major reliability issues in a NOR-type SONOS memory array, among them program disturb and punch-through. A Monte Carlo code is successfully developed to simulate the carrier transport behaviors in both NOR-type SONOS flash memory and quantum MOSFETs. The NBTI in HfSiON gate dielectric pMOSFETs is also studied. Contributions of each subject in this work are summarized as follows.

First, we investigate the new failure mode called program disturb in a NOR-type SONOS memory array when it is in programming. The Monte Carlo simulation shows that the cause of the program disturb is due to impact ionization-generated secondary electrons flowing into the neighboring cell. The effect of substrate bias effect on the program disturb is characterized and evaluated by a Monte Carlo simulation, which confirms the proposed physical mechanism. The program disturb will impose a new constraint for the technology node beyond 50nm.

Next, we propose a novel hot electron programming method in a NOR-type SONOS memory array. The electron acceleration is achieved in adjacent two cells rather than in a single cell. The Monte Carlo simulation shows that some energetic electrons may transverse the n^+ buried diffusion region and reach a program cell with residual energy, which results from the electron non-equilibrium transport. This residual energy enhances the programming efficiency and is significant as the bit-line width is further reduced. In our method, the V_{ds} in each cell can be reduced to 2.5V for the immunity to channel punch-through.

Then, we study the quantum confinement effects on hole mobility in Ge-channel double gate pMOSFETs by a Monte Carlo simulation. We find that in (100)/[110] and (110)/[-110] channel directions, the mobility peak can be achieved due to the interplay between intrasubband and intersubband scatterings. Furthermore, the hole mobility can be further improved when an uniaxial compressive stress is applied to these two channel directions.

Finally, an anomalous turn-around drain current instability is measured in HfSiON pMOSFETs. The initial increase in drain current results from valence band electron trapping into pre-existing high-*k* traps. When the stress time evolves, hole trapping and new hole trap creation in high-*k*/IL layers eventually take over. In this regime, the drain current change is negative. For the first time, we propose a bipolar charge trapping model to explain the observed phenomena. For a reliable lifetime extrapolation, the above mechanism should be considered carefully.



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Reliability and Monte Carlo Analysis in Advanced CMOS and SONOS Flash Memory

Publication List

(a) Journal Papers

3. A類國際性期刊短文

(1) Chun-Jung Tang, Tahui Wang, and Chih-Sheng Chang, "Study of quantum confinement effects on hole mobility in silicon and germanium double gate metal-oxide-semiconductor field-effect transistors", *Appl. Phys. Lett.*, vol. 95, 142103, 2009

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(3) Chun-Jung Tang, H. C. Ma, Tahui Wang, C. T. Chan, and Chih-Sheng Chang, "Bipolar Charge Trapping Induced Anomalous Negative Bias-Temperature Instability in HfSiON Gate Dielectric pMOSFETs," **Invited Paper**, *IEEE Trans. on Device and Materials Reliability*, vol. 7, pp. 518 - 523, 2007

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(b) Conference Papers

(6) H.C. Ma, J.P. Chiu, C.J. Tang and Tahui Wang, "Investigation of Post-NBT Stress Current Instability Modes in HfSiON Gate Dielectric pMOSFETs by Measurement of Individual Trapped Charge Emissions," *Int. Reliability Phys. Symp. (IRPS)*, Montreal, Canada, pp.51-54, 2009

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2. A類國際會議論文

Chang, T.C. Lu, W.P. Lu, K.C. Chen, and Chih-Yuan Lu, "Characterization and Monte Carlo Analysis of Secondary Electrons Induced Program Disturb in a Buried Diffusion Bit-line SONOS Flash Memory," *IEEE International Electron Devices Meeting*, pp.173-176, 2007

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