國立交通大學

電子工程學系　　電子研究所

碩士論文

利用準分子及連續波雷射退火製作高效能低溫複晶矽薄膜電晶體之研究

Study on High-Performance Low-Temperature Poly-Silicon Thin Film Transistors with Excimer and Continuous-Wave Laser Annealings

研 究 生：陳旭信　　**Hsu-Hsin Chen**

指導教授：鄭晃忠 博士　　**Dr. Huang-Chung Cheng**

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摘要

近年來，低溫複晶矽薄膜電晶體是在顯示技術應用中的關鍵元件。雖然透過準分子雷射可有效的提升頂閘極低溫複晶矽薄膜電晶體複晶矽層的結晶性，但此方法仍有此許缺點，如它可能在主動層和介電層之間造成大的粗糙界面，也可能形成隨機的晶界分佈等等。在這篇論文裡，我們將提出三種方法來增進低溫複晶矽薄膜電晶體的特性。

在第一個部分，我們稱為位置控制單垂直晶界低溫複晶矽薄膜電晶體方法將被提出而加以探討。我們將介紹單晶界低溫複晶矽薄膜電晶體機制。因為底閘極結構邊緣台階區提供了較厚非晶矽層，在準分子雷射退火時表示出晶種的特性。當雷射能量密度控制使得較薄的元件通道區域全熔，且接近角落較厚的區域半熔，如此一來，由通道二邊側

向成長的晶粒沿著相反的方向向通道中間成長，進而在通道的中心只形成一條垂直的晶界。因此，我們可以得到大型的晶粒，進而提升元件的效能。各種各樣的分析方法也將用來探討單垂直晶界低溫複晶矽薄膜層，由掃描式電子顯微鏡，穿透式電子顯微鏡和原子力顯微鏡的分析中可知，我們觀察到大約 0.75μm長的人工控制晶粒。

我們也加以研究了單垂直晶界低溫複晶矽薄膜電晶體的電特性，可完全與傳統底閘極低溫複晶矽薄膜電晶體製作流程相容的單垂直晶界低溫複晶矽薄膜電晶體將被製作出來，在沒有任何氫化的處理之下，其載子移動率更超過 250cm^2 / V-s。我們也觀察到閘極引起的汲極漏電和紐結效應也減少了，同樣的元件的均勻性也被提升，在量測二十個元件之下，載子移動率的標準差小於30cm^2/V*s ，臨界電壓的標準差小於0.5 V。而且在沒有任何可靠度衰退之下（如在傳統的頂閘級元件中較低的崩潰電場），單垂直晶界低溫複晶矽薄膜電晶體更適用於較薄的閘極氧化層。因此，高性能單垂直晶界低溫複晶矽薄膜電晶體可在無任何特殊結構和材料的條件下單純利用較薄的閘極氧化層得到更佳的元件驅動能力與更陡直的的次臨界擺幅。

雖然單垂直晶界低溫複晶矽薄膜電晶體表現出良好的電特性，由於偏離的離子佈植使得不對稱的電特性成為其一大問題。因此在第二個部分中，我們將結合單垂直晶界低溫複晶矽薄膜電晶體方法與背後曝光法製作出新穎自我對準的單垂直晶界低溫複晶矽薄膜電晶體。非晶矽閘極層形成了如同光罩的效果，在微影製程下阻擋了來自於汞燈的紫外光，從光學顯微鏡和掃描式電子顯微鏡的分析中可看出，光阻可完美自我對準於非晶矽閘極層。除了單垂直晶界低溫複晶矽薄膜電晶體原本具有的良好特性外，自我對準的單垂直晶界低溫複晶矽薄膜電晶體也表現出對稱性良好的電特性。自我對準單垂直晶界低溫複晶矽薄膜電晶體載子遷移率可大約192 cm^2 / V-s而在同樣的製程條件下的非自我對準元件卻大約只有 17.76 cm^2 / V-s。閘極引起的汲極漏電和紐結效應也減少了。如此一來我們更能將自我對準的單垂直晶界低溫複晶矽薄膜電晶體應用於畫素電路中的開關元件。

可惜的是，在自我對準的單垂直晶界低溫複晶矽薄膜電晶體的通道中仍然有一垂直晶界。因此，新穎連續波雷射結晶法在本論文的第三部分被提出。首先，我們先探討了

連續波雷射在摻雜活化的特性，我們發現以連續波雷射活化是一個低熱預算和高效率方法。其活化能力可使片電阻低於 47 Ω/□。接下來，我們也用連續波雷射結晶法製作出高效能 n 型和 p 型的低溫複晶矽薄膜電晶體。根據以前的研究中指出，利用連續波結晶法晶界將和雷射掃描的方法平行。如此一來，使用連續波雷射結晶法可製作出無高角度晶界的低溫複晶矽薄膜電晶體，而載子移動率在 n 型和 p 型中分別為 192 cm^2/V-s 和 92 cm^2/V-s。另一方面，由於可完全與傳統頂閘極低溫複晶矽薄膜電晶體製作流程相容，因此製作流程十分簡單。加上由於連續波雷射結晶法掃描的速度很快，使得連續波結晶法低溫複晶矽薄膜電晶體的產出率上升，因此十分適合將來系統面板的應用 。

Study on High-Performance Low-Temperature Poly-Silicon Thin Film Transistors with Excimer and Continuous-Wave Laser Annealings

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ABSTRACT

In recent years, low temperature polycrystalline thin film transistors (LTPS-TFTs) were the key devices in display applications. Although conventional top-gate LTPS-TFTs by excimer laser crystallization was an effective technology in improving the crystallinity of polycrystalline silicon thin films, there were still some drawbacks in conventional top-gate LTPS-TFTs such as high roughness interface between active layer and gate insulator, random grain boundaries and etc. In this thesis, we introduced three methods to improve the performance of LTPS-TFTs.

In the first part, the methods called location-controlled vertical single grain-boundary (VSGB) low temperature poly silicon (LTPS) thin films transistors with bottom gate (BG) structures fabricated by excimer laser annealing were investigated. The mechanisms of VSGB-LTPS thin film were studied. A thick amorphous silicon region was formed in the

corner due to the step structures of bottom gate which they served as the seeds for lateral grain growth during excimer laser irradiation. The laser energy density must be controlled to completely melt the thin region in the channel and partially melt the thick region near the corner. In addition, the lateral grain growth starting from channel edge could progress along the opposite direction toward the center of channel region. There was only one longitudinal boundary in the center of the channel. Thus, a large-grain polycrystalline silicon film was obtained which would lead to improved device performance. Various analyses were performed to investigate VSGB-LTPS thin films. From the analyses of scanning electron microscope (SEM), transmission electron microscope (TEM) and atomic force microscope (AFM), large longitudinal grains artificially grown measuring about 0.75μm were observed.

Electrical characteristics of VSGB LTPS-TFTs were also studied. High-performance VSGB-LTPS-TFTs, which were fully compatible with the process flow of conventional bottom gate LTPS-TFTs, with field-effect mobility exceeding 250cm^2/V-s have been fabricated without any hydrogenation treatment. Low GIDL effect and kink effect were also observed. The uniformity were also improved by this method. If twenty VSGB LTPS-TFTs devices were taken into discussion, the standard deviation of mobility was smaller than 30cm^2/V*s and the standard deviation of Vth was smaller than 0.5V. Moreover, the VSGB-LTPS-TFTs could be fabricated with thinner gate oxide without any reliability issue such as lower breakdown field of gate oxide which was serious in conventional top-gate ones. Therefore, higher performance VSGB-LTPS-TFTs with larger driving current and better subthreshold swing could be easily produced by thinner gate oxide without additional structures or materials.

Although VSGB-LTPS-TFTs exhibited high performance characteristics, asymmetrical electrical characteristics were also observed in VSGB-LTPS-TFTs due to the mis-aligned ion implantation. In the second part, we introduced the novel method called self-aligned location-controlled vertical single grain-boundary (VSGB) low temperature poly silicon

(LTPS) thin films transistors with backside UV exposure. The simple process flows were also fully compatible with conventional bottom gate process. The amorphous gates could act as the masks of the lithography to stop the ultra violate light from the Hg light. From the OM and SEM images, the P.R. was self-aligned perfectly with the amorphous gate regions. Besides the advantages of VSGB-LTPS-TFTs, symmetrical electrical characteristics were also observed in SA-VSGB-LTPS-TFTs. The SA-VSGB-LTPS-TFTs exhibited better electrical characteristics than mis-aligned ones. SA-VSGB-LTPS-TFT with field effect mobility of about 192 cm^2/V-s could be achieved while the mobility the counterpart was about only 17.76 cm^2/V-s. The GIDL and kink effect were also reduced. Alghough VSGB-LTPS-TFTs shown high performance, SA-VSGB-LTPS-TFTs fabricated by this method were more suitable to the elements of the pixel switch devices.

Unfortunatelly, there was still one high angle grain boundary in the channel of SA-VSGB-LTPS-TFTs. Therefore, a new continuous wave (CW) laser crystallization (CLC) to form directional lateral grain was proposed in the third part of the thesis. First, dopant activation by CW laser annealing was studied. It was found that dopant activation by CW laser annealing was a low-thermal budget and high-efficiency method. Low sheet resistance of 47 Ω/□ was observed. Second, we demonstrated the high performance n-type and p-type LTPS-TFTs fabricated by CLC method. According to previous reports, the grain boundaries were generally parallel to one another and to the scan direction of the laser beam by CLC methods. Therefore, high performance LTPS-TFTs without any high angle grain boundary could be fabricated and the mobilities were 192 cm^2/V-s for n-type CLC-LTPS-TFTs and 92 cm^2/V-s for p-type CLC-LTPS-TFTs, respectively. Moreover, the process flow was simple because the process flows were compatible with conventional top-gate LTPS-TFTs process. Additionally, due to the high scanning rate of CLC method, the throughput of CLC-LTPS-TFTs was improved. Hence, the CLC method was quite promising for the system on panel (SOP) application in the future.

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Fig. 5-17 The output characteristics of p-type CLC-LTPS-TFTs with channel lengths of 2μm.

Chapter 1

Introduction

1-1 Overview of Low Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

Recently, polycrystalline silicon thin film transistors (polysilicon TFTs) were key devices in large area electronics applications, including active-matrix liquid crystal displays (AMLCDs). and active matrix organic light emitting displays (AMOLEDs) [1.1]-[1.5]. In large size active matrix liquid crystal displays (AMLCDs), the pixel switching elements were TFTs fabricated in amorphous silicon (amorphous silicon) while the peripheral driving circuitry, for which the very low amorphous silicon TFT mobility was inadequate, was fabricated on single crystal silicon. The effective carrier mobility in polycrystalline silicon was significantly higher (by two orders of magnitude) than those in amorphous silicon, so that both n- and p-channel devices with reasonably high drive currents could be achieved in polycrystalline silicon [1.6]. Therefore, the capability to realize complementary metal-oxide-semiconductor (CMOS) circuits allows low-power driving circuitry to be integrated with the active matrix [1.7]. This fact allows the integration of both the active matrix pixel switching elements and the peripheral driving circuitry onto a single glass substrate, thus substantially reducing manufacturing complexity and cost, and therefore enables the possibility of a complete system on panel (SOP) which could generate a number of innovative new products and markets. Besides, since system-on-panel mounts a screen and

its peripheral circuits on the same substrate, the successful implementation of this technology would lead to substantial savings in costs by shortening the display manufacturing and inspection processes while maintaining a level of high reliability.

One of the advantages of LTPS TFTs compared to high temperature polycrystalline silicon (HTPS) TFTs was that it could be processed at temperature low enough to utilize low cost, large area glass substrates rather than expensive quartz substrates which required process temperatures of 900°C. High-mobility polycrystalline silicon (poly-Si) thin film transistors (TFTs) fabricated in a low temperature process below 600°C were required for giant-microelectronic application. In particular, high mobility polycrystalline silicon films produced from a low temperature fabrication technique capable of utilizing an inexpensive glass substrates were thought to be fundamental to this technology. In recent years, dozens of researches have been made to develop various technologies for improving the performance and reliability of LTPS TFTs. Although polycrystalline silicon thin films could be directly deposited on glass substrate by low-pressure chemical vapor deposition (LPCVD) and electron cyclotron resonance chemical vapor deposition (ECRCVD). However, due to the high deposition temperature (approximately 625°C) and the poor crystallinity of the as-deposited polycrystalline silicon thin film, the direct deposition method has been excluded in the fabrication of LTPS TFTs. Therefore, Crystallization of amorphous silicon thin films has been considered the most important process for fabricating high-performance LTPS TFTs.

1-2 Overview for Crystallization of Amorphous Silicon Thin Films

The crystallized polycrystalline silicon thin films always acted as channel regions in the polycrystalline silicon TFTs. Therefore, a robust crystallization process was required for LTPS

TFTs to become a mainstream technology. In order to obtain high-mobility polycrystalline silicon films, it was widely accepted that enlarging the grain size and reducing the defect density were the most important key technologies. Enlarging the grain size and reducing the defect density in polycrystalline material would make it approach the quality of single-crystalline material, which would lead to better performance of polycrystalline devices. Therefore, it was important to control the size of the grains, the number of the grains, and the location of the grains to fabricate high quality polycrystalline silicon thin films. Recently various technologies have been proposed for amorphous silicon crystallization on glass material. In several low-temperature polycrystalline silicon fabrication techniques, we could classify them into three groups: solid phase crystallization, metal induced crystallization and laser crystallization. In the following three kinds of low temperature crystallization methods were roughly reviewed.

1-2-1 Solid Phase Crystallization of Amorphous Silicon Thin Films

Crystallized the as deposited amorphous silicon thin film into polycrystalline silicon have been shown to have higher carrier mobilities [1.8]. Depositing the amorphous silicon thin film at temperatures below 600°C, then thermal crystallized into polycrystalline silicon for several hours (~ 24 h) at 600°C was required to convert them into final polycrystalline form [1.9]. Unfortunately, it requires annealing for a long time(over 20 h) at high temperature (over 600°C) and therefore limits its application on large scale glass substrate for mass production requirement.

1-2-2 Metal Induced Crystallization of Amorphous Silicon Thin Films

The SPC's temperature of amorphous silicon could be lowered by introducing certain

metals. It was well known that such method was called “metal induced crystallization (MIC)”. The reaction between the metal and amorphous silicon occurred at an interlayer by diffusion and lowered the crystallization temperature. Such enhancement of crystallization was due to an interaction of the free electrons from the metal with covalent Si bonds near the growing interface. Among various metals, Ni has been shown to be the best candidate of inducing lateral crystallization at low temperature for fabricating good-performance polycrystalline silicon TFTs. For instance, when nickel was deposited on amorphous silicon, followed by thermal annealing, octahedral precipitates $NiSi_2$ would be formed on amorphous silicon films [1.10]-[1.13]. The $NiSi_2$ precipitates act as nucleation sites for crystallization. Needlelike crystallites were formed as a result of migration of the $NiSi_2$ precipitates through the amorphous silicon network. Unfortunately, the metal contamination would degrade the electrical properties such as leakage current of LTPS TFTs.

1-2-3 Laser Crystallization of Amorphous Silicon Thin Films

The laser crystallization seems to be the most promising for giant-microelectronics application. Because of its extremely short duration and shallow melt-regrowth process, this method avoids thermal damage to the glass substrate even the flexible substrate. Moreover, the polycrystalline silicon films were obtained better crystallinity by laser crystallization. The basic principle of laser crystallization was the transformation from amorphous to crystalline silicon by melting the silicon for a very short time. Laser crystallization of amorphous silicon could be performed using a variety of lasers and different techniques. Excimer laser crystallization (ELC) was by far the most widely used method at the moment [1.14][1.15]. The most important advantage of excimer lasers was the strong absorption of UV light in silicon. In consequence, most of the laser energy was absorbed close to the surface of the thin film and the thermal strain on the substrate was much lower than in case of lasers with longer wavelength. ELC of polycrystalline silicon TFTs has been studied for a number of years and

several important aspects of this process have been well established. The technique yielded high-performance polycrystalline silicon TFTs with high throughput thanked to the large beam size of the high energy laser beam. In the recent years, substituting of the laser system was an effective way to fabricate higher mobility polycrystalline silicon channel layer. At present, the most possible laser system was continuous wave laser [1.16]. The power instability of DPSS CW laser was less than 1%, which was superior to that of KrF and XeCl excimer laser. In this technique, high scanning speed was used to achieve high throughput. The crystallized polycrystalline silicon thin film was made up of very large grains (about 3 x 20μm^2). The grain boundaries were generally parallel to one another and to the scan direction of the laser beam. However, this technique was not well-developed and the crystallization mechanisms and large-area laser annealing equipment were still under investigated.

1-3 Motivation

In order to fabricate high performance and uniform LTPS-TFTs, we introduced three methods to improve the performance and uniformity of LTPS-TFTs. In the first part, we introduced the bottom gate structure and modify the bottom gate device in various process methods. The methods were location-controlled vertical single grain-boundary (VSGB) low temperature poly silicon (LTPS) thin films transistors with bottom gate (BG) structures fabricated by excimer laser annealing and backside exposure self-aligned technology. In the grain boundary control method, we investigated a simple process to control grain growth in the channel region of TFTs. In the second part, we use novel backside exposure technology to form self-aligned VSGB-LTPS-TFTs. In the third part, we substituted the laser system by continuous wave (CW) laser to obtain LTPS-TFTs with better electrical characteristic. A novel crystallization technology of polycrystalline silicon thin film would be fabricated by

continuous wave laser.

1-3-1 Low Temperature Polycrystalline silicon (LTPS) Thin Films Transistors with Bottom Gate (BG) Structures Fabricated by Excimer Laser Annealing

Although conventional top-gate structure was widely used to fabricated TFTs, the high roughness between active layer and gate insulator, random grain boundary position and small process window (SLG) were noteworthy issues. Besides, there were additional process steps between active layer and gate insulator deposition which would introduce contamination in the interface between active layer and gate insulator. Therefore, we choose bottom gate structure to fabricate the high performance LTPS TFTs in the following methods.

1-3-1-1 Location-Controlled Vertical single grain-boundary (VSGB) method

Although pulsed excimer laser crystallization (ELC) had the potential to improve the crystallinity of polycrystalline silicon films, narrow ELC process window and the uniformity of the crystallized polycrystalline silicon films were important issues. According to many prior studies, the grain size of the ELC polycrystalline silicon film was significantly dependent on energy density of laser irradiation so that the energy for producing super-lateral growth was too critical to hit it right. Fluctuation of energy profile, pulse-to-pulse energy variation and unevenness of initial silicon thin films would crucially affect grain growth after solidification. As a result, many methods have been proposed to solve the above problems, such as sequential lateral solidification (SLS), phase-modulated ELC using an optical phase-shift mask, dual beam ELC, pre-pattern ELC, μ-Czochralski (so called grain filter) methods, selectively enlarging laser crystallization (SELAX) technology and etc.. However, most of them were not compatible with the existing excimer laser annealing system or needed complex processes. In this thesis, we investigate a novel ELC technique called

“Location-Controlled Vertical single grain-boundary (VSGB) method”. The objective of VSGB-LTPS-TFTs design was to fabricate thermal gradient in the selected regions. We found by experience that there was a thicker region at the corner of the bottom gate structure, i.e. the thin film containing different thicknesses at the corner region. If the laser energy density was controlled to completely melt the thin region in the channel and partially melted the thick region near the corner, a lateral temperature gradient would exist between the complete melting liquid-phase region and un-melting solid-phase seeds, and grains would grow laterally towards the center of the melting region from the un-melting solid seeds. In the first part of this thesis, the device uniformity and performance were investigated using this structure.

1-3-1-2 Self-Aligned VSGB-LTPS-TFTs Fabricated by Backside Exposure Lithography Method

Although VSGB-LTPS-TFTs exhibited superior device electrical performance and uniformity than conventional top-gate ones, one major drawback in VSGB-LTPS-TFTs was the misaligned source/drain implantation lithography owing to the non-ideal of lithography stepper system or manual alignment equipment. The mis-aligned problem would make a significant difference in turn-on characteristic of VSGB-LTPS-TFTs. Such difference would not be observed in the self-aligned case. It indicated the importance of conventional top gate device and bottom gate alignment in giving a symmetrical device as well as reducing performance variations. Therefore, many methods have been proposed to solve the above problems [1.17]-[1.19]. Among all the methods, backside exposure method seemed to be the best one to fabricate self-aligned (SA) VSGB-LTPS-TFTs on glass substrates or quartz substrates. In the second part of this thesis, we use the bottom polycrystalline silicon gate as the backside exposure mask to stop the UV lights from Hg lamp and we combined the

VSGB-LTPS-TFTs method with backside exposure technology to fabricate high performance SA-VSGB-LTPS-TFTs. The device uniformity and performance were investigated using the SA-VSGB-LTPS-TFTs configurations in ELC polycrystalline silicon TFTs.

1-3-2 Application of Continuous Wave Laser Crystallization for Low Temperature Polycrystalline Thin Films Transistors

Substituting the laser system was an effective method to fabricate higher mobility polycrystalline silicon active layer. At present, the most potential laser system was the continuous wave (CW) laser. The power instability of DPSS CW laser was less than 1%, which was superior to that of KrF and XeCl excimer laser. In this technique, high scanning speed was used to achieve high throughput. The crystallized polycrystalline silicon thin film was made up of very large grains (about 3 x 20μm^2). The grain boundaries were generally parallel to one another and to the scan direction of the laser beam. Surface orientation of many grains was nearly (100) direction. Surface of the crystallized polycrystalline silicon was smooth and grain boundary didn't form ridge. CW lateral crystallization made it easy to form large grains with high scan speed and wide energy range because of continuous energy supply, directional solidification caused by laser scanning and slow cooling rate of the molten silicon thin film. In the third part of the thesis, a novel crystallization technology of polycrystalline silicon thin film would be fabricated by continuous wave laser. ELA and CW laser activation technology for phosphorus and boron dopants in amorphous silicon thin films were also performed, and taken into comparison.

1-4 Thesis Outline

In chapter 2, experimental procedures of VSGB-LTPS thin films would be introduced. The mechanisms of lateral growth of VSGB-LTPS thin films was proposed by material

analysis. The material properties of VSGB-LTPS thin films were analyzed by scanning electron microscope (SEM), atomic force microscopy (AFM) and transmission electron microscope (TEM).

In chapter 3, experimental procedures of VSGB-LTPS-TFTs would be introduced. The electrical properties of VSGB-LTPS-TFTs, including the field effect mobility, the subthreshold swing, the threshold voltage, the uniformity and bidirectional electrical properties were also investigated.

In chapter 4, VSGB-LTPS-TFTs were modified by using a novel method, so called backside exposure method. The misaligned lithography problem was observed using optical microscope (OM) and SEM. Experimental process flows would be introduced and the electrical properties of self-aligned VSGB-LTPS-TFTs, including the field effect mobility, the subthreshold swing and the threshold voltage were investigated. The bidirectional electrical properties of SA-VSGB-LTPS-TFTs was also discussed.

In chapter 5, a novel crystallization technology of polycrystalline silicon thin film was fabricated by continuous wave (CW) laser. ELA and CW laser activation technology for phosphorus and boron dopants in amorphous silicon thin films were also performed, and taken into comparison. Electrical properties of CW laser TFTs, including the field effect mobility, the subthreshold swing and the threshold voltage were also investigated.

Finally, conclusions were given in chapter 6.

Chapter 2

Material Analyses of Location-Controlled Vertical Single Grain-Boundary (VSGB) Low Temperature Poly Silicon (LTPS) Thin Films with Bottom Gate (BG) Structures Fabricated by Excimer Laser Annealing (ELA)

2-1 Introduction

Currently, high driving-current capacity, low leakage-current and good uniformity of TFT characteristics over a large area of glass substrate were imperative for devices aiming at AMLCD/AMOLED drivers and matrix. Low-temperature polycrystalline silicon (LTPS) technology has been the most promising method to manufacture high performance thin film transistors (TFTs) for the past decades. As comparison to amorphous silicon (amorphous silicon), The mobility of polycrystalline silicon TFTs was generally much higher than that of amorphous silicon TFTs. The high drive current allows smaller TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio. In addition, the capability to realize complementary metal-oxide-semiconductor (CMOS) circuits allowed low-power

driver circuitry to be integrated with the active matrix, for reduced display-module cost and improved reliability. As comparison to high temperature poly silicon (HTPS), the thermal budget was much lower for LTPS TFTs. The LTPS technology was compatible with glass substrate even plastic substrate. Therefore, the cost of LTPS technology was much lower than HTPS technology, especially in large panel application.

Among many techniques reported to date, excimer-laser crystallization (ELC) method seemed the most promising method for preparing high quality polycrystalline silicon thin films. The major advantage was that the polycrystalline silicon film obtained by this technology possesses good crystallinity with very few intragrain defects, due to the melt-regrowth process. But the conventional top-gate ELC LTPS TFTs have some drawbacks . First, there was higher surface roughness between active layer and insulator due to the ridge formation of grain boundaries. Second, the location of grain boundaries cannot be controlled due to the random position of nucleation during excimer laser crystallization. Third, although large grains could be obtained in the super lateral growth (SLG) regime, many small grains still spread between these large grains. According to SLG model [2.1], the lateral grain growth distance was determined by the quenching rate of liquid silicon and the retain-solid Si seed distance. Thus, a little deviation in spatial and/or pulse-to-pulse energy density and amorphous silicon thin film thickness could easily result in partial or full melting of amorphous silicon thin film at local region. Fourth, after the deposition of active layers, there were many process steps such as the pattern of active region and laser crystallization before the deposition of gate insulators. Therefore, there was possible contamination between the deposition of active layers and gate insulators.

Polycrystalline silicon thin films with large grain always resulted in high-performance polycrystalline silicon thin film devices due to the reduction of defect traps of the grain boundaries. Hence, enlarging grain size was the most effective manner for improving the

performance of the polycrystalline silicon devices. A variety of crystallization methods have been proposed to produce large grains with superior grain size distribution uniformity. They include sequential lateral solidification (SLS) [2.2]-[2.4], grain-filters (or substrate-embedded seeds) method [2.5][2.6], phase-modulated ELC using an optical phase-shift mask [2.7], ELC of selectively floating amorphous silicon thin film [2.8], ELC of pre-patterned amorphous silicon thin film [2.9]-[2.11], dual beam ELA [2.12], dual pluses ELA [2.13], slicing channel [2.14] and so on. Although all of them provided alternatives to produce large-grain polycrystalline silicon thin films, these methods could not be compatible with conventional LTPS process equipments.

It was desired that the growth of high-quality large grain could be controlled in the device channel region from the viewpoint of device performance and uniformity. In this chapter, a novel process for producing high-mobility polycrystalline silicon was described. In order to induce lateral grain growth, a lateral temperature gradient must be created between the adjacent areas and there must be retained solid Si to act as the seeds for lateral crystallization. By completely melting the amorphous Si thin film in a certain region and partially melting the one at adjacent area, a large lateral temperature gradient would exist between these two regions, and grains would grow laterally towards the complete melting region from the retained solid Si. In this method, bottom gate structures were adopted. A thick amorphous silicon region was formed in the corner due to the step structures of bottom gate which they served as the seeds for lateral grain growth during excimer laser irradiation. The laser energy density must be controlled to completely melt the thin region in the channel and partially melt the thick region near the corner. Thus, a large-grain polycrystalline silicon film was obtained which would lead to improved device performance. In addition, the lateral grain growth starting from channel edge could progress along the opposite direction toward the center of channel region. There was only one longitudinal boundary in the center of the channel. So we call this novel method, location-controlled Vertical single grain-boundary

(VSGB) Low Temperature Poly Silicon (LTPS) Thin Films. Due to the artificial controlling of the lateral growth in the channel region, the uniformity of device characteristic could be further improved.

Besides, another advantage of VSGB-LTPS method was that it could be used to fabricate thinner gate insulator TFTs. Due to the smoother interface between the gate insulator and active region of TFTs, thinner gate insulator could be used. Therefore, VSGB-LTPS-TFTs would exhibit higher drivability and better subthreshold swing. The performance of the VSGB-LTPS-TFTs could be easily improved at the some condition of crystallization of polycrystalline silicon.

In this chapter, experimental procedures of VSGB-LTPS thin films would be introduced. We studied the mechanisms of lateral growth of VSGB-LTPS method by many material analysis equipments. The material properties of VSGB-LTPS thin films were analyzed by scanning electron microscope (SEM), transmission electron microscope (TEM) and atomic force microscope (AFM). Besides, the electrical properties of VSGB-LTPS TFTs, including the field effect mobility, the subthreshold swing and the threshold voltage, the uniformity and bidirectional electrical properties were also investigated.

2-2 Process Flows for Material Analyses of Vertical Single Grain Boundary Low Temperature Polycrystalline Thin Films

More detailed flow of preparing samples was shown in Fig. 2-1. At first, in-situ doping phosphorus polycrystalline silicon thin films with thickness of 1000Å/2000Å/3000Å were deposited by pyrolysis of pure SiH4 and PH3 with low-pressure chemical vapor deposition (LPCVD) at 550℃ on oxidized silicon substrates with oxide thickness of 1 μm. Then, the

doping polycrystalline silicon layer was defined to form polycrystalline silicon gate by TCP-RIE. Next, a 1000Å/500Å TEOS oxide layer was deposited as gate insulator by PECVD at 385°C. After the deposition of gate insulator, the 1000Å amorphous silicon layer was deposition as the active layer by LPCVD at 550℃ with SiH4 as gas source. Laser crystallization was performed by KrF excimer laser (λ=248nm). The excimer laser system was shown in Fig. 2-2. During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and substrate was maintained at room temperature. The number of laser shots per area was 20 (i.e., 95% overlapping) and laser energy density was varied. The grain structure of the crystallized polycrystalline silicon thin film was analyzed using scanning electron microscope (SEM), atomic force microscopy (AFM) and transmission electron microscope (TEM). In order to facilitate the SEM observation, all the samples were processed by secco-etch before SEM analysis.

2-3 Material Analyses of Vertical Single Grain Boundary Low Temperature Polycrystalline Thin Film

2-3-1 Scanning Electron Microscope (SEM) Analysis

Fig. 2-3 show SEM graphs of excimer laser crystallized polycrystalline silicon with bottom gate structure. The channel length was 1.2μm (a) and 1.5μm(b). The laser energy was 420 mJ/cm^2 and the poly gate thickness was 1000Å. As expected, longitudinal grains with 0.75 μm in length were formed in the laser crystallized polycrystalline silicon thin film of channel region. It has been reported that lateral thermal gradient could arise as a result of the heat generated at moving solid-melting interface [2.15]. When a proper laser energy density irradiates the silicon thin film containing different thicknesses, the thin region in the channel region was completely melted while the thick region in the corner due to the step structures of

bottom gate was only partially melted, leaving behind islands of solid material. As a result, grains would grow laterally towards the complete melting region from the retained solid seeds. The lateral growth would start from the still solid amorphous silicon spacer seed, and stretch toward the completely melted region until the solid-melt interface from opposite direction impinge. Because the channel region was in-situ designed at the thin region, the grain boundaries perpendicular to the current flow in the channel region could be reduced. Thus the field-effect mobility of polycrystalline silicon TFTs could be greatly improved with this crystallization technique.

In order to investigate the maximum distance of lateral grain growth, the length of channel was broadened. Fig. 2-4(a)~Fig. 2-4(b) show the SEM graphs of the crystallized polycrystalline silicon thin film with gate oxide thickness of 1000Å. Evidently, the laser fluence determined the extension of lateral grain growth. When a longer channel length was adopted for crystallization, the laser fluence has to increase high enough to make the longitudinal grains collide with those grown from the other side; otherwise, small grains caused by spontaneous homogeneous nucleation would form in the center of the channel region. But when we increased the laser density from 420 to 480 mJ/cm^2. The longitudinal grains was still not long enough to collide with those grown from the other side. As expect, when the laser energy was further increased, the amorphous silicon films was ablated as show in Fig. 2-4(c). If spontaneous nucleation could be suppressed or delayed by substrate heating or any other methods, the lateral growth would continuous to a longer distance, hence producing longer lateral growth. As a result, by adopting a suitable length of adjacent channel length, location control lateral grain growth could be acquired in the polycrystalline silicon thin film. Fig. 2-6 shows the SEM graphs with gate oxide thickness of 500Å. The same phenomenon was also observed by thicker gate oxide.

The influence of the poly gate height on the eventual grain structure in the crystallized polycrystalline silicon thin film was also studied. We used the thicker poly-gate to increase

the thickness of the corner region. Fig. 2-5(a)~Fig. 2-5(b) show the SEM graphs of excimer laser crystallized polycrystalline silicon with bottom gate structure. The channel length was 2 μm. The laser energy density was 420 mJ/cm^2. In this case, the poly gate thickness was 2000Å(a) 3000Å(b). Unfortunately, the polycrystalline silicon films in the corner was ablated due to the thinning effect of laser irradiation. The higher poly-gate made larger step height and the thinning effect became more serious. Therefore, in order to prevent the thinning effect due to the step height, we must use poly gate thickness of 1000Å.

2-3-2 Atomic Force Microscopy (AFM) Analysis

By using AFM analysis the grains could be distinguished apparently due to the huge hillock formation at the grain boundaries. The hillock was resulted from the freezing of capillary waves excited in the melting silicon during laser crystallization [2.16]. Grain boundaries and vertices, which typically were the last to freeze during lateral grain growth, have accumulated silicon due to the action of the expanded solid material on the remaining (denser) liquid material. When the laser crystallization begins, nucleated grains advance laterally through the denser liquid at first. As the solid regions grow, they fill a larger volume than the melt they consume. Eventually, the remaining liquid extends above the surrounding film. Where two grains meet to form a grain boundary, a ridge develops. Where three or more grains meet to form a vertex, a hillock may develop. As shown in Fig. 2-8, longitudinal grains with 0.75 μm in length were formed in the laser crystallized polycrystalline silicon thin film of channel region. We formed a vertical single grain boundary in the center of the channel between the location controlled grains.

2-3-3 Transmission Electron Microscope (TEM) Analysis

Fig. 2-9 shows the cross-section TEM graphs of polycrystalline silicon thin film in the channel region of bottom gate structure. From the figure, it could be found that vertical single grain boundary was controlled artificially in the center of the channel region. Only two large grain with fewer intra defect were observed. For polycrystalline silicon thin film used as active laywer in thin film transistor, polycrystalline silicon thin film with fewer defects was the desired one. Meanwhile, cross-section TEM images also fit that the interface between active region and gate insulator was vary smooth. No hillock in conventional top-gate LTPS was observed. Therefore, we could use thinner gate insulator than conventional top-gate LTPS TFTs without sacrificing the gate insulator reliability due the smoother interface between the active region and the gate insulator.

Fig. 2-10 shows the cross-section TEM graphs of polycrystalline silicon thin film in the corner region of bottom gate structure. Thinning effect was observed in the corner region. The thickness of the corner region was thinner than the channel region. Therefore, we couldn't use higher poly-gate or the polycrystalline silicon thin film of the corner region would be broken due to the thinning effect. From the correlated diffraction pattern of polycrystalline silicon thin film, the crystallinity of the polycrystalline silicon could be observed. It could be found that as the channel region was selected, the diffraction spots become more obvious, which means that the crystallinity was good. When the corner region was selected, the ring was more obvious, which means that the vertical growth in the corner region of the grains exhibit poor crystallinity. But the corner regions would be heavily doped and act as the source/drain region of TFTs. Therefore, the poor crystallinity would not degrade the performance of LTPS-TFTs.

2-4 Summary

In this chapter, we carry out the material analyses of VSGB-LTPS thin films. First, we introduce the mechanisms of VSGB-LTPS thin film. After that, various analyses were performed to investigate VSGB-LTPS thin films. From the analysis of SEM, AFM and TEM, large longitudinal grains were artificially grown measuring about 0.75 μm was observed. Furthermore, the lateral growth starting from the seeds of corner region could progress along the opposite direction and vertical single grain boundary were controlled in the center of the channel region artificially. Therefore, the channel region in-situ designed to arrange at the region of longitudinal grains, the grain boundaries perpendicular to the current flow in the channel region could be reduced. In addition to the enhancement of quality of crystallization of polycrystalline silicon, the interface between the active region and gate insulator was much smoother than conventional top-gate LTPS thin film. This crystallization technique could be applied to short channel bottom gate LTPS-TFTs and we would carried the new VSGB-LTPS TFTs in the next chapter.

Chapter 3

Characteristics of Location-Controlled Vertical Single Grain-Boundary (VSGB) Low Temperature Poly Silicon Thin Films Transistors (LTPS-TFTs) with Bottom Gate (BG) Structures Fabricated by Excimer Laser Annealing (ELA)

3-1 Introduction

High current-driving capacity, low leakage-current and good uniformity of TFT characteristics over a large area of glass substrate [3.1]-[3.5] were imperative for devices aiming at AMLCD and AMOLED drivers and matrix. Furthermore, they should be produced with low cost and high throughput. It was desired that the growth of high-quality large grain could be controlled in the device channel region from the viewpoint of device performance and uniformity. In this chapter, a novel process for high quality LTPS thin films in chapter 2 for producing high-mobility polycrystalline silicon TFTs was described. We call this novel method, location-controlled Vertical single grain-boundary (VSGB) Low Temperature Poly

Silicon Thin Films Transistors (LTPS-TFTs). In this method, VSGB-LTPS-TFTs with bottom gate structures were formed. Thus, a large-grain polycrystalline silicon film was obtained which would lead to improved device performance. There was only one longitudinal boundary in the center of the channel. Besides, another advantage of VSGB-LTPS TFTs method was that it could be used to fabricate thinner gate insulator TFTs. Due to the smoother interface between the gate insulator and active region of TFTs, thinner gate insulator could be used. Therefore, VSGB-LTPS-TFTs would exhibit higher drivability and better subthreshold swing. The performance of the VSGB-LTPS-TFTs could be easily improved at the some condition of crystallization of polycrystalline silicon. Moreover, due to the artificial controlling of the lateral growth in the channel region the uniformity of device characteristic could be further improved. In the last part of the chapter, the mis-alinged problem of bottom gate structure would be introduced. That would degrade the performance of VSGB-LTPS-TFTs, especially in small dimension device [3.6]-[3.8]. There must be a novel self-aligned source/drain ion implantation process to solve the mis-aligned problem.

3-2 Process Flows of Vertical Single Grain Boundary Low Temperature Polycrystalline Thin Film Transistors

More detailed flow of preparing samples was shown in Fig. 3-1. At first, in-situ doping phosphorus polycrystalline silicon thin films with thickness of 1000Å were deposited by pyrolysis of pure SiH4 and PH3 with low-pressure chemical vapor deposition (LPCVD) at 550℃ on oxidized silicon substrates with oxide thickness of 1μm. Then, the doping polycrystalline silicon layer was defined to form polycrystalline silicon gate by TCP-RIE. Next, a 1000Å/500Å TEOS oxide layer was deposited as gate insulator by PECVD at 385˚C. After the deposition of gate insulator, the 1000Å amorphous silicon layer was deposition as

the active layer by LPCVD at 550℃ with SiH4 as gas source. Laser crystallization was performed by KrF excimer laser (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and substrate was maintained at room temperature. The number of laser shots per area was 10/20 (i.e., 90/95% overlapping) and laser energy density was varied. Next, a phosphorus ion implantation with a dosage of $5X10^{15}$ cm^{-2} was performed to form source and drain regions following by the definition of active region by TCP-RIE. A 3000Å TEOS oxide layer was deposition as passivation layer at 385℃ and the implanted dopants were activated by thermal annealing in furnace at 600°C for 12 hours. Then, contact opening by TEL5000-RIE and and metallization with Aluminum were carried out. Finally, Aluminum sintering was carried out at 400 ℃ to reduce the serious resistance. No hydrogenation plasma treatment was performed during the device fabrication process. For comparison, conventional top-gate ELC polycrystalline silicon TFTs were also fabricated.

3-3 Electrical Characteristics of Vertical Single Grain Boundary Low Temperature Polycrystalline Thin Film Transistors

3-3-1 Electrical Characteristics of VSGB-LTPS-TFTs with Gate Oxide Thickness of 1000Å

In the previous chapter, it has been demonstrated that large and longitudinal grains could be produced in the channel by adopting bottom gate structure. The grain structure would have a profound influence on the electrical characteristics of the fabricated TFTs. Fig. 3-2~Fig. 3-8 show the typical transfer characteristics of polycrystalline silicon TFTs crystallized using VSGB-LTPS-TFTs structure with channel lengths of 1.2 μm ~ 40 μm, in which the thickness

of gate oxide was 1000Å and the number of laser shots per area was 10 (i.e., 90% overlapping). Fig. 3-9~Fig. 3-15 show the typical transfer characteristics of polycrystalline silicon TFTs crystallized using VSGB-LTPS-TFTs structure with channel lengths of 1.2 μm ~ 40 μm, in which the thickness of gate oxide was 1000Å and the number of laser shots per area was 20 (i.e., 90% overlapping).The laser process conditions were optimized. The conventional TFTs were also shown for comparison. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of I_d = (W/L) x 10^{-8} A at $|V_{ds}|$ = 0.1V. The field effect mobility was extracted from the maximum transconductance in the linear region of I_d-V_g characteristics at $|V_d|$ = 0.1V. Several important electrical characteristics of the TFTs were summarized in Table 3. 1 and Table 3. 2 for laser shots of 10 and 20, respectively.

According to these figures, the polycrystalline silicon TFTs with VSGB-LTPS-TFTs structure exhibit better electrical characteristics than those of conventional top-gate ones, especially in short channel devices. This could be attributed to the longitudinal grain in the device channel region. Take the dimension of W = L = 1.2 μm and lasr shots of 10 for example, VSGB-LTPS-TFTs with field effect mobility of about 250 cm^2/V-s could be achieved by using this VSGB-LTPS method while the mobility of the conventional counterpart was about 79 cm^2/V-s. In addition, although the maximum achievable length of lateral grain growth was limited between 0.75 μm as described in the previous chapter, the electrical characteristics of the TFTs with device dimension up to W = L = 5 μm were still superior to those of conventional ones. This could also ascribed to the long longitudinal grain growth at the channel edge even though many small grains resulted from spontaneous nucleation exist in the channel center as well.

Fig. 3-16~Fig. 3-22 and Fig. 3-23~Fig. 3-29 display the output characteristics polycrystalline silicon TFTs crystallized using VSGB-LTPS-TFTs structure with laser shots 10 and 20 respectively. It was demonstrated that polycrystalline silicon TFTs with

VSGB-LTPS structure provide higher driving current than conventional ELC polycrystalline silicon TFTs under the same bias condition, especially in short channel devices. It was reported that the trap center due to grain boundaries enhance kink effect [3.9]-[3.11]. The good crystallinity at the drain edge due to the artificial controlled grain also reduced the kink effect, especially in short channel devices.

In addition to the enhancement of LTPS TFTs performance, LTPS TFTs crystallized with VSGB-LTPS TFTs structure also exhibited better uniformity. Fig. 3-30~Fig. 3-31 and Fig. 3-33~Fig. 3-34 show the dependences of field-effect mobility and threshold voltage on different channel lengths for the number of laser shots 10 and 20 respectively. Twenty TFTs were measured for each laser irradiation condition to investigate the device-to-device variation. The vertical bars in the figures indicate the minimum and maximum characteristic values found at the optimized laser energy density, and the solid symbols were the average calculated characteristic values. Fig. 3-32 and Fig. 3-35 show the standard deviation of the field-effect mobility and threshold voltage for the number of laser shots 10 and 20, respectively. Compared to the conventional top-gate LTPS TFT, it could be found that for the LTPS TFTs with VSGB-LTPS-TFTs structure, the field-effect mobility and threshold voltage show better uniformity than conventional top-gate ones in short channel devices. High performance VSGB-LTPS-TFTs with good uniformity could be fabricated easily using bottom gate structure with the number of laser shots 10. Therefore, the number of laser shots was reduced and the throughput and the yield could be increased. This fact facilitates the industry application with the VSGB-LTPS method due to the cost reduction of LTPS-TFTs.

3-3-2 Electrical Characteristics of VSGB-LTPS-TFTs with Gate Oxide Thickness of 500Å

Fig. 3-36~Fig. 3-42 show the typical transfer characteristics of polycrystalline silicon TFTs crystallized using VSGB-LTPS-TFTs structure with channel lengths of 1.2 μm ~ 40 μm,

in which the thickness of gate oxide was 500Å and the number of laser shots per area was 10 (i.e., 90% overlapping). Fig. 3-43~Fig. 3-49 show the typical transfer characteristics of polycrystalline silicon TFTs crystallized using VSGB-LTPS-TFTs structure with channel lengths of 1.2 μm ~ 40 μm, in which the thickness of gate oxide was 500Å and the number of laser shots per area was 20 (i.e., 90% overlapping).The laser process conditions were optimized. The conventional TFTs were also shown for comparison. Several important electrical characteristics of the TFTs were summarized in Table 3. 2 for laser shots 10 and 20, respectively. According to these figures, the polycrystalline silicon TFTs with VSGB-LTPS-TFTs structure exhibited better electrical characteristics than conventional top-gate ones, especially in short channel devices. This could be attributed to the longitudinal grain in the device channel region. Take the dimension of W = L = 1.2 μm and laser shots of 10 for example, VSGB-LTPS-TFTs with field effect mobility of about 201 cm^2/V-s could be achieved by using this VSGB-LTPS method while the mobility of the conventional counterpart was about 76 cm^2/V-s. The electrical characteristics of the TFTs with device dimension up to W = L = 5 μm were still superior to those of conventional ones. This could also ascribed to the long longitudinal grain growth at the channel edge even though many small grains resulted from spontaneous nucleation exist in the channel center as well. In addition to the high performance characteristics, VSGB-LTPS-TFTs exhibit low grate induced drain leakage (GIDL) effect, especially in thin gate oxide devices. Fig. 3-50 shows the mechanism of the higher GIDL in conventional top-gate device. The thinning effect of thin gate oxide was poor. Therefore, we must use thicker gate oxide in conventional top-gate device to prevent the local high electrical field from gate electrode due to the high surface roughness after ELA. Moreover, the VSGB-LTPS-TFTs have smooth interface between gate oxide and active region. We could use thin gate oxide in VSGB-LTPS-TFTs without scarifying the reliability.

Fig. 3-51~Fig. 3-57and Fig. 3-58~Fig. 3-64 display the output characteristics

polycrystalline silicon TFTs crystallized using VSGB-LTPS-TFTs structure with laser shots 10 and 20 respectively. It was demonstrated that polycrystalline silicon TFTs with VSGB-LTPS structure provide higher driving current than conventional ELC polycrystalline silicon TFTs under the same bias condition, especially in short channel devices. The good crystallinity at the drain edge due to the artificial controlled grain also reduced the kink effect, especially in short channel devices.

Fig. 3-65~Fig. 3-66 and Fig. 3-68~Fig. 3-69 show the dependence of field-effect mobility and threshold voltage on different channel lengths for the number of laser shots 10 and 20 respectively. Twenty TFTs were measured for each laser irradiation condition to investigate the device-to-device variation. The vertical bars in the figures indicate the minimum and maximum characteristic values found at the optimized laser energy density, and the solid symbols were the average calculated characteristic values. Fig. 3-67 and Fig. 3-70 show the standard deviation of the field-effect mobility and threshold voltage for the number of laser shots 10 and 20 respectively. Compared to the conventional top-gate LTPS TFT, it could be found that for the LTPS TFTs with VSGB-LTPS-TFTs structure, the field-effect mobility and threshold voltage show better uniformity than conventional top-gate ones in short channel devices. The same as the previous section, high performance VSGB-LTPS-TFTs could be fabricated easily using bottom gate structure with the number of laser shots 10. Therefore, the number of laser shots was reduced and the throughput and the yield could be increased. This fact facilitates the industry application with the VSGB-LTPS method due to the cost reduction of LTPS-TFTs.

3-3-3 The Comparisons of Electrical Characteristics Between Gate Oxide Thickness of 500Å and 1000Å with VSGB-LTPS-TFTs Structure

Fig. 3-71~Fig. 3-74 show the typical transfer characteristics of polycrystalline silicon

TFTs crystallized using VSGB-LTPS-TFTs structure with channel lengths of 1.2 μm ~ 2 μm in which the thickness of gate oxide was 500Å and 1000Å and the number of laser shots were 10 and 20. Fig. 3-75~Fig. 3-78 display the output characteristics polycrystalline silicon TFTs crystallized using VSGB-LTPS-TFTs structure using different gate oxide thickness with laser shots 10 and 20, respectively. According to these figures, the VSGB-LTPS-TFTs with thinner gate oxide exhibit better electrical characteristics than thicker ones, especially in short channel devices. This could be attributed to the better gate control ability. Thinner gate oxide could make the gate electrode control the channel more easily. Therefore, higher performance VSGB-LTPS-TFTs could be easily produced by thinner gate oxide without additional structures.

If thin gate oxide was used, there would be some reliability issue on breakdown field. Fig. 3-79 and Fig. 3-80 show the breakdown field with gate oxide 500Å and 1000Å. We made the source and drain ground and increase the gate voltage until the gate oxide breakdown. According to these figures, the breakdown field of the conventional top-gate devices was the same as VSGB-LTPS-TFTs due to the smoothing effect of thick gate oxide of 1000Å. But the breakdown field of conventional top-gate devices was much lower than VSGB-LTPS-TFTs due to the surface roughness of active region with gate oxide thickness of 500 Å. VSGB-LTPS-TFTs exhibited higher reliability than conventional top-gate ones. We could use thin gate oxide to get higher performance of TFTs without scarifying reliability of gate oxide.

3-4 The Mis-Alignment Effect of Source/Drain Ion Implantation on VSGB-LTPS-TFTs

Although VSGB-LTPS-TFTs exhibited high performance characteristic with filed effect mobility exceeding 250 cm^2/V-s, the structure of VSGB-LTPS-TFTs had an essential

drawback. The disadvantage was the mis-alignment of source/drain ion implantation. Because of the no perfection of lithography system such as steppers or aligners, the lithography of source/drain ion implantation would exhibit mis-aligned problem. Because the percentage of the mis-alignment variation increased more dramatically in short channel device than in long channel devices, the mis-alignment of source/drain ion implantation would degrade the performance of VSGB-LTPS-TFTs more seriously in short channel devices. Fig. 3-81~Fig. 3-84 show the typical transfer characteristics of VSGB-LTPS-TFTs with forward and reverse bias in channel length of 1.2μm and 1.5μm and the number of laser shots was 10 and 20. We changed the roles of source and drain electrode for the measurement of forward and reverse. Asymmetrical electrical characteristics were observed. Beside the shift of the subthreshold swing, the GIDL effect became more seriously and the drivability was degraded. Fig. 3-85~Fig. 3-88 display the output characteristics of VSGB-LTPS-TFTs with forward and reverse bias in channel length of 1.2 μm and 1.5μm and the the number of laser shots were 10 and 20. We changed the roles of source and drain electrode. Asymmetrical electrical characteristics were also observed. The kink effect became more seriously. The degradation of the performance of VSGB-LTPS TFTs might be due to the vertical small grains in the corner region near the drain edge as shown in Fig. 3-89. According to Fig. 3-89, there were many small vertical grains in the corner region of the step. If the ion implantation didn't make the region heavy doped, the region would become parts of the channel region. The undoped region would become a serious resistance in the channel region which degrade the output current. The small grains with a lot of trap densities would degrade the performance of VSGB-LTPS-TFTs and the GIDL and the kink effect would become more serious. Therefore, a novel self-aligned ion implantation process must be introduced to solve the mis-aligned problem. The mis-alignment problem of the lithography of ion implantation could be solved and a novel backside exposure lithography would be used in next chapter.

3-5 Summary

High-performance VSGB-LTPS-TFTs with field-effect mobility exceeding 250 cm^2/V-s have been fabricated with bottom gate structure which was fully compatible with the process flow of conventional bottom gate LTPS-TFTs . Low GIDL effect and kink effect were also be observed. The VSGB-LTPS-TFTs with bottom gate structure exhibited better electrical characteristics than the conventional top-gate ones, especially in short channel devices owing to the artificially controlled lateral grain growth. Furthermore, the lateral growth starting from the seed in the corner region could progress along the opposite direction. Hence, the channel region was in-situ designed at the large grain regions, the grain boundaries perpendicular to the current flow in the channel region could be reduced.

In addition to the enhancement of TFT performance, TFTs crystallized with VSGB-LTPS structure also demonstrated excellent uniformity. Due to the artificial controlled grains, the excellent uniformity of VSGB-LTPS-TFTs was also demonstrated. The standard deviation of mobility was smaller than 30 cm^2/V*s and the standard deviation of Vth was smaller than 0.5V. Therefore, we could reduce the number of shots as less as possible. High performance VSGB-LTPS-TFTs could be fabricated easily using bottom gate structure with the number of laser shots 10. Therefore, the number of laser shots was reduced and the throughput and the yield could be increased. This fact facilitates the industry application with the VSGB-LTPS method due to the cost reduction of fabricating LTPS-TFTs.

Moreover, the VSGB-LTPS-TFTs could be fabricated with thinner gate oxide without any reliability issue such as lower breakdown field of gate oxide which was serious in conventional top-gate ones. The VSGB-LTPS-TFTs with thinner gate oxide of 500 Å exhibit better electrical characteristics than thicker ones of 1000Å, especially in short channel devices. This could be attributed to Thinner gate oxide made the gate electrode control the channel

more easily. Therefore, higher performance VSGB-LTPS-TFTs with larger driving current and better subthreshold swing could be easily produced by thinner gate oxide without additional structures or materials.

Because of the no perfection of lithography system such as steppers or aligners, the lithography of source/drain ion implantation would exhibit mis-aligned problem. Asymmetrical electrical characteristics was observed and the performance of VSGB-LTPS-TFTs was degraded. The GIDL effect and the kink effect also became more serious due to the small grains in the corner. Therefore, a novel self-aligned ion implantation process must be introduced to dismiss the mis-aligned problem. The mis-alignment problem of the lithography of ion implantation could be solved and a novel backside exposure lithography would be used in next chapter.

Chapter 4

Novel Self - Aligned VSGB - LTPS- TFTs with Bottom Gates Using Backside Exposure Method

4-1 Introduction

Although VSGB-LTPS-TFTs exhibit high performance characteristic with filed effect mobility, the structure of VSGB-LTPS-TFTs had an essential drawback. The disadvantage was the mis-alignment of source/drain ion implantation. Because of the no perfection of lithography system such as steppers or aligners, the lithography of source/drain ion implantation would exhibit mis-aligned problem. Because the percentage of the mis-alignment variation increased more dramatically in short channel device than in long channel devices, the mis-alignment of source/drain ion implantation would degrade the performance of VSGB-LTPS-TFTs more seriously in short channel devices. Asymmetrical electrical characteristic was also observed in VSGB-LTPS-TFTs. Beside the shift of the threshold voltage, the GIDL effect became more seriously and the drivability was degraded.

Recently, self-aligned process has been widely used in conventional top-gate polycrystalline silicon TFTs [4.1]~[4.4]. The top poly gate acts as a mask of ion implantation. Therefore, the dopant can't be implanted into the channel region. But VSGB-LTPS TFTs were fabricated with bottom gate structure. The poly gate can't act as a mask of ion implantation. We must introduce additional lithography step to implant the dopant into the source and drain

regions.

In this chapter, in order to solve the mis-alignment of the source and drain ion implantation, a novel method of self-aligned ion implantation lithography was used by backside exposure [4.5],[4.6]. We call this novel method, self-aligned (SA) location-controlled Vertical single grain-boundary (VSGB) Low Temperature Poly Silicon Thin Films Transistors (LTPS-TFTs). Detail process procedures would be described and the self-aligned lithography would be observed by Optical Microscope (OM) and SEM analyses. In this method, VSGB-LTPS-TFTs with self-aligned ion implantation were formed. Meanwhile, the electrical characteristics of SA-VSGB-LTPS-TFTs with thickness of poly gate from 1000Å to 1500Å were take in into comparison. The symmetrical and asymmetrical electrical characteristics of SA-VSGB-LTPS TFTs and mis-aligned VSGB-LTPS-TFTs were also discussed. At last, several important electrical characteristics of the SA-VSGB-LTPS-TFTs and mis-aligned VSGB-LTPS-TFTs were summarized.

4-2 Process Flows of Self-Aligned Vertical Single Grain Boundary Low Temperature Polycrystalline Thin Film Transistors (SA-VSGB-LTPS-TFTs)

For high performance LTPS-TFTs, we combined VSGB-LTPS structure with the novel backside exposure lithography. More detailed flow of devices preparation was shown in Fig. 4-1. At first, amorphous silicon thin films with thickness of 1000Å and 1500Å were deposited by pyrolysis of pure SiH4 with low-pressure chemical vapor deposition (LPCVD) at 550℃ on quartz substrates. Next, a phosphorus ion implantation with a dosage of $5X10^{15}$ cm^{-2} was performed. Then, the doping amorphous silicon layer was defined to form amorphous silicon gate by TCP-RIE. Next, a 1000Å TEOS oxide layer was deposited as gate insulator by

PECVD at 385°C. After the deposition of gate insulator, a 1000Å amorphous silicon layer was deposited as the active layer by LPCVD at 550℃ with SiH4 as gas source. Laser crystallization was performed by KrF excimer laser (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and substrate was maintained at 400℃. The number of laser shots per area was 20 (i.e., 95% overlapping) and laser energy density was varied. Next, a self-aligned lithography by backside exposure method was carried out for source and drain ion implantation. Then, a phosphorus ion implantation with a dosage of $5X10^{15}$ cm^{-2} was performed to form source and drain regions following by the definition of active region by TCP-RIE. A 3000Å TEOS oxide layer was deposition as passivation layer at 385℃ and the implanted dopants were activated by thermal annealing in furnace at 600°C for 12 hours. Then, contact opening by TEL5000-RIE and and metallization with Aluminum were carried out. Finally, Aluminum sintering was carried out at 400 ℃ to reduce the contact resistance. No hydrogenation plasma treatment was performed during the device fabrication process. For comparison, non self-aligned VSGB-LTPS-TFTs were also fabricated.

4-3 Results and Discussion

4-3-1 Material Analyses of Photo Resist with Backside Exposure Method

Fig. 4-2~Fig. 4-3 show the Optical Microscope (OM) images of the samples with bottom gate structure from transparent light source. The thickness of the amorphous gate was 1000Å and the channel length was 2 μm and 5 μm. According to those pictures, regardless the channel length, the regions above the amorphous gate were dark but the other regions

were bright. It was attributed to that the light couldn't pass the region covered by the amorphous gate but could pass the active region covered by polycrystalline silicon. We could only see the light which was not reflected or absorbed by the amorphous gate. Hence, if the thickness of amorphous gate was thicker enough, the light can't pass the region of amorphous gate either. Therefore, the amorphous gates with thickness of 1000Å and 1500Å could act as the masks of the lithography to stop the ultra violate light from the Hg light. Fig. 4-4~Fig. 4-5 show OM images of mis-aligned and self-aligned implantation devices after lithography from reflected light source. The channel length was 2μm. Fig. 4-4 shows the mis-aligned lithography. Due to the problem of mis-alignment of aligner, there were vertical and horizontal shifts of Photo Resist (P.R.) on the region of amorphous gate. The vertical horizontal shift was about 1μm which would degrade process of the ion implantation. Fig. 4-5 show self-aligned lithography by backside exposure method. Due to perfect self-aligned ultra violate light form the backside exposure, the P.R. on the amorphous gate wouldn't absorb UV light. Therefore the P.R. wouldn't be developed out. The P.R. was perfectly aligned to amorphous gate due to the self-aligned process. No shift was observed after lithography. Therefore, the ion implantation of source and drain would perfectly be carried out without any shifts.

Fig. 4-6 show the SEM graph of the P.R. after lithography. The SEM graph reveal the microstructure of P.R.. According to the graph, the P.R. with thickness of 1.2μm was observed and the P.R. was perfectly aligned with the amorphous silicon gate which was similar to the results given by OM graph. To sum up, for self-aligned LTPS-TFTs application the amorphous silicon gate could act as the mask of lithography to stop the UV light from Hg light source. Therefore, the P.R. which was aligned with the amorphous silicon gate would benefit the ion implantation of source and drain.

4-3-2 Electrical Characteristics of SA-VSGB-LTPS-TFTs

It's well known that the thicker the amorphous gate the less light passing through the amorphous gate. But in chapter 2, it has been investigated that if the amorphous gate was thicker than 2000Å, the thinning effect was too serious to fabricate VSGB-LTPS-TFTs. Therefore, SA-VSGB-LTPS-TFTs with amorphous gate thickness of 1000Å and 1500Å were fabricated for comparison. Fig. 4-7 shows the typical transfer characteristics of SA-VSGB-LTPS structure with amorphous gate thickness of 1000Å and 1500Å. The laser process conditions were optimized. According to the figure, the SA-VSGB-LTPS-TFTs with amorphous gate thickness of 1000Å exhibit better electrical characteristics than 1500Å one. Take the dimension of W = L = 1μm for example, SA-VSGB-LTPS-TFT with field effect mobility of about 192 cm^2/V-s could be achieved by using amorphous gate thickness of 1000Å while the mobility the counterpart was about 129 cm^2/V-s. This could be attributed to the shorter longitudinal grain in the channel region by using amorphous gate thickness of 1500Å. The thicker the amorphous gate, the more heat was conducted to the amorphous gate. Therefore, during laser irradiation, the cooling rate of SA-VSGB-LTPS-TFTs with amorphous gate thickness of 1500Å was higher than the that of SA-VSGB-LTPS-TFTs with amorphous gate thickness of 1000Å. The thicker the gate thickness the shorter the longitudinal grain in the channel region. Fig. 4-8 shows the output characteristics of SA-VSGB-LTPS structure with amorphous gate thickness of 1000Å and 1500Å. It was demonstrated that SA-VSGB-LTPS-TFTs with amorphous gate thickness of 1000Å provide higher driving current than 1500Å under the same bias condition. The improved driving current could be attributed to the high field effect mobility due to longer longitudinal grain in the channel region. Therefore, amorphous gate thickness of 1000Å was the optimized condition to fabricate SA-VSGB-LTPS-TFTs. We would discus SA-VSGB-LTPS TFTs with amorphous gate thickness of 1000Å in the following section.

In the previous section, it has been demonstrated that SA-VSGB-LTPS TFTs could be

produced by adopting bottom gate structure. Fig. 4-9 and Fig. 4-10 show the typical transfer characteristics of SA-VSGB-LTPS TFTs with channel lengths of 1μm and 5 μm, in which the thickness of amorphous gate was 1000Å. The laser process conditions were optimized. The mis-aligned VSGB-LTPS TFTs were also shown for comparison. Several important electrical characteristics of the TFTs were summarized in Table 4. 1. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of Id = (W/L) x 10-8 A at |Vds| = 0.1V. The field effect mobility was extracted from the maximum transconductance in the linear region of Id-Vg characteristics at |Vd| = 0.1V. According to the figures, the SA-VSGB-LTPS-TFTs exhibit better electrical characteristics than mis-aligned ones. Take the dimension of W = L = 1μm for example, SA-VSGB-LTPS-TFT with field effect mobility of about 192 cm2/V-s could be achieved while the mobility of the counterpart was about only 17.76 cm2/V-s. This could be due to the self-aligned ion implantation. Hence, no serious resistance was formed near the source and drain region after self-aligned ion implantation. It should be noted that the shorter the channel length the more serious the degradation of the performance of the mis-aligned VSGB-LTPS-TFTs. Because the percentage of the variation of the mis-alignment increase more dramatically in short channel device than in long channel devices, the mis-alignment of source/drain ion implantation would degrade the performance of VSGB-LTPS-TFTs more seriously in short channel devices. Fig. 4-11 and Fig. 4-12 show the output characteristics of SA-VSGB-LTPS TFTs. It was demonstrated that SA-VSGB-LTPS-TFTs provide higher driving current than mis-aligned VSGB-LTPS-TFTs under the same bias condition. The improved driving current could be attributed to less series resistance near the source and drain regions due to self-aligned ion implantation.

According to these figures from Fig. 4-9~Fig. 4-12, the GIDL and kink effect were also reduced. It was attributed that the small vertical grains in the corner region of the step were heavily doped. The self-aligned ion implantation made the region heavy doped, the region would become parts of source and drain regions. The trap density of the small grains near the

source and drain regions wouldn't induce the GIDL and kink effect.

Fig. 4-13 and Fig. 4-14 show the typical transfer characteristics of VSGB-LTPS-TFTs with forward and reverse bias in channel length of 1μm and 5μm. We changed the roles of source and drain electrode for the measurement of forward and reverse. Asymmetrical and symmetrical electrical characteristics were observed in mis-aligned VSGB-LTPS-TFTs and self-aligned ones, respectively. The mis-aligned VSGB-LTPS-TFTs showed not only the shift of the threshold voltage but also the serious GIDL effect. These problems were all solved in SA-VSGB-LTPS-TFTs. Fig. 4-15 and Fig. 4-16 show the output characteristics of VSGB-LTPS-TFTs with forward and reverse bias in channel length of 1μm and 5μm. Asymmetrical and symmetrical electrical characteristics were also observed in mis-aligned VSGB-LTPS-TFTs and self-aligned ones, respectively. Due to the symmetrical electrical characteristics, we could fabricate the VSGB-LTPS-TFTs more suitable to the elements of the pixel switch devices.

4-4 Summary

In this chapter, we carry out the novel self-aligned vertical single grain boundary low temperature thin film transistors (SA-VSGB-LTPS-TFTs) by combining backside exposure method and VSGB-LTPS-TFTs. In the first section of the chapter, process flows of SA-VSGB-LTPS-TFTs were introduced. The simple process flows were fully compatible with conventional bottom gate process. After that, material analyses of SA-VSGB-LTPS TFTs were demonstrated by using OM and SEM. From the OM image, the P.R. was self-aligned perfectly with the amorphous gate regions. The amorphous gates could act as the masks of the lithography to stop the ultra violate light from the Hg light. Due to the perfect self-aligned ultra violate light from the backside exposure, the P.R. on the amorphous gate wouldn't

absorb UV light. Therefore the P.R. wouldn't be developed out. No shift was observed after lithography. From the SEM graph of the P.R. after lithography, the SEM graph revealed the microstructure of P.R.. The P.R. with thickness of 1.2μm was observed and the P.R. was perfectly aligned with the amorphous silicon gate which was similar to the results given by OM graphs. Therefore, the ion implantation of source and drain would perfectly be carried out without any shifts.

In the second section of the chapter, electrical characteristics of SA-VSGB-LTPS-TFTs were discussed. First, SA-VSGB-LTPS-TFTs with amorphous gate thickness of 1000Å and 1500Å were fabricated for comparison. The SA-VSGB-LTPS-TFTs with amorphous gate thickness of 1000Å exhibit better electrical characteristics than 1500Å one. SA-VSGB-LTPS-TFT with field effect mobility of about 192 cm^2/V-s could be achieved by using amorphous gate thickness of 1000Å while the mobility of 1500Å gate was about 129 cm^2/V-s. This could be attributed to the shorter longitudinal grain in the channel region by using amorphous gate thickness of 1500Å because amorphous gate thickness of 1500Å has a larger cooling rate during laser irradiation.

Second, the mis-aligned and self-aligned VSGB-LTPS TFTs were also taken into comparison. The SA-VSGB-LTPS-TFTs exhibit better electrical characteristics than mis-aligned ones. The GIDL and kink effect were also reduced. SA-VSGB-LTPS-TFT with field effect mobility of about 192 cm^2/V-s could be achieved while the mobility the counterpart was about only 17.76 cm^2/V-s. This could be due to the self-aligned ion implantation. No serious resistance was formed near the source and drain region after self-aligned ion implantation.

Third, symmetrical electrical characteristics were also observed in SA-VSGB-LTPS-TFTs due to the self-aligned ion implantation. Due to the symmetrical electrical characteristics, we could fabricate the VSGB-LTPS-TFTs more suitable to the elements of the pixel switch devices.

Chapter 5

High-Performance LTPS-TFTs Fabricated by Continuous Wave (CW) Laser Annealing

5-1 Introduction

In recent, low temperature polycrystalline siliconlicon TFTs fabricated by excimer laser annealing (ELA) had been applied to high performance AMLCDs and AMOLEDs. However, higher quality displays with the better peripheral integrated circuits were needed. Since the device driving capability would crucially influence the performance of the integrated circuits, the mobility of the device became a significant problem. According to the previous report, the mobility would be limited to a saturation value due to other effects, such as grain boundary in the channel region. Moreover, conventional excimer laser crystallization has some essential drawbacks such as complex optical system, high facility cost, troublesome maintenance, poor output energy stability (±5 ~10 %) and narrow process window (<10 mJ). These problems would lead to the non-uniform electrical characteristics of LTPS-TFTs. Therefore, novel crystallization methods were demanded to enhance both the device performance and uniformity for next generation LTPS TFT.

Recently, a stable diode pumped solid state (DPSS) continuous wave (CW) laser crystallization was also applied to the fabrication of high-performance polycrystalline silicon TFTs on non-alkali glass substrate[5.1]-[5.5]. The power instability of DPSS CW laser was less than 1%, which was superior to that of KrF excimer laser and Ar laser. In this technique, large scanning speed was used to achieve high throughput. The crystallized polycrystalline

silicon thin film was made up of very large grains (about 3 x 20μm^2). The grain boundaries were generally parallel to one another and to the scan direction of the laser beam. Surface orientation of many grains was nearly (100) direction. Surface of the crystallized polycrystalline silicon was smooth and grain boundary does not form ridge. CW lateral crystallization makes it easy to form large grains with high scan speed and wide energy range because of continuous energy supply, directional solidification caused by laser scanning and slow cooling rate of the molten Si. In the previous chapter, we had demonstrated that SA-VSGB-LTPS-TFTs fabricated by ELC of amorphous silicon thin film. However, there was still a high angle grain boundary in the center of the channel region. The grain boundary would limit the mobility of the SA-VSGB-LTPS-TFTs. In order to fabricate higher performance LTPS-TFTs without any grain boundary in the channel region, the CW laser crystallization was investigated in the chapter.

Moreover, for a transistor to work effectively, the source and drain contacts must have relatively low resistance which requires low sheet resistance in the source and drain regions. In order to achieve low sheet resistance, the source and drain implants must be activated to a high degree. In semiconductor processing, activation was performed by either a furnace anneal or rapid thermal processing (RTP). However, both these steps require temperatures well beyond the strain point of glass. In laser activation, the silicon was heated, melted and reformed without heating the glass, resulting in a very high efficiency approach. Laser activation technology seems to be the most promising method to active the dopant with low thermal budget. But the activation technology of CW laser was rarely studied. We would investigate the activation by CW laser annealing in this chapter.

In this chapter, a novel activation and crystallization technology of poly silicon thin film would be fabricated by continuous wave laser. In the first section, CW laser activation technology would be investigated. The material properties of doped LTPS thin films after activation by CW laser were analyzed by four point probe measurement system and secondary

ion mass spectrometer (SIMS). Low-thermal-budget and high-efficiency dopant activation by CW laser would be introduced and discussed. In the second section, CW laser crystallization technology would also be studied. High performance p-type and n-type CW laser crystallization (CLC) TFTs would be fabricated with conventional top-gate structure. Conventional top-gate LTPS-TFTs by ELC would be fabricated for comparison.

5-2 Phosphorus and Boron Dopant Activation by CW Laser Annealing

5-2-1 Process Flows of Phosphorus and Boron Dopant Activation by CW Laser Annealing

Detail process flow for sample prepatation was shown in Fig. 5-1. First, 1000Å thick amorphous silicon thin films were formed on fused quartz wafers by LPCVD with SiH4 as gas source.. After that, ion implantations of phosphorus and boron were performed. The dosages were varied from $5X10^{15}$ to $5X10^{14}$ cm^{-2}. Dopant activation was performed by CW laser (λ=532nm) and KrF excimer laser (λ=248nm). The CW laser system was show in Fig. 5-2. During the CW laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and substrate was maintained at room temperature. The values of power of CW laser were 10W and 15W and the scanning rate was varied. During the excimer laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and substrate was maintained at room temperature, too. The number of laser shots per area was 20 (i.e., 95% overlapping) and laser energy density was varied. The doped polycrystalline silicon thin films were analyzed using four point probe measurement system and secondary ion mass spectrometer (SIMS).

5-2-2 Material Analyses of Phosphorus and Boron Dopant Activation by CW Laser Annealing

Fig. 5-3 and Fig. 5-4 show the sheet resistance of samples after excimer laser activation by four-point probe system. The energy density of excimer laser was varied from 190mJ/cm^2 to 390mJ/cm^2. As expected, if the energy density was higher, the sheet resistance was lower. It was attributed that there was more heat on the dopant amorphous silicon thin films with higher energy density. Therefore, the cooling rate of the laser irradiation was slow. The activation time of high energy density would be longer than low energy density. Hence, more implanted dopants were aligned into the correct lattice sites and the sheet resistance would be lower.

Fig. 5-5 and Fig. 5-6 show the sheet resistance of samples after CW laser activation by four-point probe system. The laser power was 10W. the scanning rate was varied. According to these figures, if the scanning rate was slower, lower sheet resistance was observed, especially in low ion implantation density. It was attributed that the annealing time would be longer if the scanning rate was lower. Therefore, more implanted dopants were aligned into the correct lattice sites and the sheet resistance would be lower.

Fig. 5-7 and Fig. 5-8 show the sheet resistance of samples after CW laser activation with laser power of 15W. Polycrystalline silicon of low sheet resistance of 47 Ω/□ was fabricated by CW laser annealing. The phenomenon of turn around was also observed. The phenomenon was explained as following. When the scanning velocity was larger than 100mm/sec, The size of polycrystalline silicon grain dominated the sheet resistance. If the size of polycrystalline silicon was larger, the sheet resistance would be lower. When the scanning velocity was smaller than 100mm/sec, the ablation of polycrystalline silicon thin film and the segregation effect dominated the sheet resistance. Due to the destruction effect of ablation, the sheet resistance of the doped polycrystalline silicon thin film was increased. The segregation of the

dopant also degraded the sheet resistance of the polycrystalline silicon thin film. The sheet resistances of samples after CW laser and excimer laser activation were summarized in Table 5. 1.

Fig. 5-9 shows the redistribution profiles of P_{31} after excimer and continuous wave laser annealings. The power of CW laser was 15W. The scanning rate was 100mm/sec. The energy density of excimer laser was 390 mJ/cm^2. The number of laser shots was 20(ie. 95% overlapping). The ion implantation dose was 5X10^{15}cm^{-2}. Fig. 5-10 shows the redistribution profiles of B_{11} after excimer and continuous wave laser annealings. The power of CW laser was 15W. The scanning rate was 90mm/sec. The energy density of excimer laser was 390 mJ/cm^2. The number of laser shots was 20(ie. 95% overlapping). The ion implantation dose was 5X10^{15}cm^{-2}. From the redistribution profiles, we found that the redistribution profiles of CW laser were as uniformly as excimer laser ones in the polycrystalline silicon thin films.

To sum up, laser activation by CW laser annealing was a low-thermal budget and high-efficiency method. Due to the high scanning rate of the CW laser, the throughput of the activation was higher than conventional excimer laser activation. Therefore, the CW laser activation technology could reduce the activation time than any other methods. The high throughput would reduce the cost of activation and facility the industry application.

5-3 High-Performance LTPS-TFTs Fabricated by CW Laser Annealing

5-3-1 Process Flows of High-Performance LTPS-TFTs Fabricated by CW Laser Annealing

In the previous chapter, we had demonstrated that SA-VSGB-LTPS-TFTs fabricated by ELC of amorphous silicon thin film. However, there was still a high angle grain boundary in

the center of the channel region. The grain boundary would limit the mobility of the SA-VSGB-LTPS-TFTs. In CW laser crystallization, the grain boundaries were generally parallel to one another and to the scan direction of the laser beam. Therefore, we could fabricate high performance LTPS-TFTs without any high angle grain boundary in the channel region by CW laser crystallization. More detailed flow of preparing samples was shown in Fig. 5-11. At first, amorphous silicon thin films with thickness of 500Å were deposited by pure SiH4 with low-pressure chemical vapor deposition (LPCVD) at 550℃ on quartz substrates. Then, laser crystallization was performed by CW laser (λ=532nm). During the laser irradiation, the samples were located on a substrate in air and substrate was maintained at room temperature. The output power of CW laser was 4W and scanning rate of the laser irradiation was 60 mm/sec. The scanning direction was parallel to the current flow of the TFT. After that, active region were defined by RIE. Then, a 1000Å TEOS oxide layer was deposited as gate insulator by PECVD at 385°C. After the deposition of gate insulator, the 2000Å amorphous silicon layer was deposition as gate electrode by LPCVD at 550°C with SiH4 as gas source. Next, the amorphous silicon thin films were etched by TCP-RIE and the gate insulator were removed by RIE and buffer oxide etch (BOE) chemical solution. A self-aligned phosphorous implantation with a dosage of 5×10^{15} cm^{-2} was performed to form source and drain regions. 3000 Å-thick TEOS passivation oxide layers were deposited by PECVD at 385℃ and the implanted dopants were activated by thermal annealing at 600°C for 12 hours. After contact opening by RIE, aluminum thin film with a thickness of 5000Å was deposited by thermal evaporation and patterned to complete the fabrication of CW laser crystallization (CLC) LTPS-TFTs. A 20-min sintering process was performed at 400°C to reduce the contact series resistance of the source and drain electrodes. No post plasma treatment was carried out on these devices. For comparison, conventional top-gate ELC LTPS-TFTs with laser energy in SLG region and laser shots of 100 were also fabricated.

5-3-2 Electrical Characteristics of High-Performance LTPS-TFTs Fabricated by CW Laser Annealing

Fig. 5-12 and Fig. 5-13show the typical transfer characteristics of n-type CLC-LTPS-TFTs with channel lengths of 2μm and 5 μm. Conventional top-gate n-type ELC LTPS-TFTs were also shown for comparison. Several important electrical characteristics of the n-type CLC-LTPS-TFTs were summarized in The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of I_d = (W/L) x 10^{-8} A at $|V_{ds}|$ = 0.1V. The field effect mobility was extracted from the maximum transconductance in the linear region of I_d-V_g characteristics at $|V_d|$ = 0.1V. According to the figures, the CLC-LTPS-TFTs exhibit better electrical characteristics than ELC ones. Take the dimension of W = L = 2 μm for example, CLC-LTPS-TFT with field effect mobility of about 164 cm^2/V-s could be achieved while the mobility of ELC-LTPS-TFT was about 105 cm^2/V-s. This could be attributed to the good crystallillity in the device channel region by CLC. High field effect mobility result from the super-giant grains and fewer intragrain defects. In addition, the grain boundaries were generally parallel to one another and to the scan direction of the laser beam. If the scanning direction was parallel to the current flow of the TFT, there would be no grain boundary in the channel region. Fig. 5-14 and Fig. 5-15 display the output characteristics polycrystalline silicon TFTs crystallized using CLC. It was demonstrated that polycrystalline silicon TFTs by CLC provided higher driving current than conventional ELC polycrystalline silicon TFTs under the same bias condition. The good crystallinity at the drain edge by CLC also reduced the kink effect.

Fig. 5-16 and Fig. 5-17 show the typical transfer characteristics and output characteristics of p-type CLC-LTPS-TFTs with channel lengths of 2μm. As expected, high performance p-type LTPS-TFTs were fabricated by CLC. For example, p-type CLC-LTPS-TFTs with field effect mobility of about 92 cm^2/V-s could be achieved. Several

important electrical characteristics of the p-type CLC-LTPS-TFTs were also summarized in Table 5. 2.

5-4 Summary

In the first section of this chapter, we carried out the laser dopant activation by CW laser and excimer laser. It was found that laser activation by CW laser annealing was a low-thermal budget and high-efficiency method. Low sheet resistance of 47 Ω/□ was observed by CW laser annealing. Due to the high scanning rate of the CW laser, the throughput of the activation was higher than conventional excimer laser activation. Therefore, the CW laser activation technology could reduce the activation time than any other methods.

In the second section of this chapter, we demonstrated that high performance LTPS-TFTs fabricated by CLC method. The CLC-LTPS-TFTs exhibit better electrical characteristics than ELC ones. This could be attributed to the better crystallillity in the device channel region by CLC. High field effect mobility result from the super-giant grains and fewer intragrain defects. In addition, the grain boundaries were generally parallel to one another and to the scan direction of the laser beam. If the scanning direction was parallel to the current flow of the TFT, there would be no grain boundary in the channel region. Therefore, the mobility could be 164 cm^2/V-s for n-type CLC LTPS-TFTs and 92 cm^2/V-s for p-type CLC LTPS-TFTs. Moreover, the process flow was simple because the process flows were compatible with conventional top-gate LTPS-TFTs process. Additionally, due to the high scanning rate of CLC method, the throughput of CLC-LTPS-TFTs was improved. Hence, the CLC method was quite promising for the system on panel (SOP) application in the future.

Chapter 6

Conclusions

In order to fabricate high performance LTPS-TFTs by laser annealing, three technologies were investigated in the thesis. Location-controlled vertical single grain-boundary (VSGB) low temperature poly silicon (LTPS) thin films transistors with bottom gate (BG) structures fabricated by excimer laser annealing have been studied in chapter 2 and chapter 3. For solving the mis-aligned problem, novel self - aligned VSGB - LTPS- TFTs with bottom gates using backside exposure method have been studied in chapter 4. To eliminate the high angle grain boundary, continuous wave (CW) laser crystallization were proposed in chapter 5. The proposed LTPS-TFTs by CW laser crystallization (CLC) exhibited excellent carrier mobility.

In chapter 2, material analyses of VSGB-LTPS thin films with BG structures fabricated by ELA were investigated. We introduced the mechanisms of VSGB-LTPS thin film. After that, various analyses were performed to investigate VSGB-LTPS thin films. From the analysis of scanning electron microscope (SEM), transmission electron microscope (TEM) and atomic force microscope (AFM), large longitudinal grains were artificially grown measuring about 0.75μm was observed. Furthermore, the lateral growth starting from the seeds of corner region could progress along the opposite direction and vertical single grain boundary was controlled in the center of the channel region artificially. The grain boundaries perpendicular to the current flow in the channel region could be reduced. In addition to the enhancement of quality of crystallization of polycrystalline silicon, the interface between the active region and gate insulator was much smoother than conventional top-gate LTPS thin film. This crystallization technique could be applied to short channel bottom gate LTPS-TFTs and we would carry out the new VSGB-LTPS TFTs in the next chapter.

In chapter 3, characteristics of VSGB LTPS-TFTs with BG structures fabricated by ELA were studied. High-performance VSGB-LTPS-TFTs with field-effect mobility exceeding 249 cm^2/V-s have been fabricated with bottom gate structure which was fully compatible with the process flow of conventional bottom gate LTPS-TFTs . Low GIDL effect and kink effect were also observed. The VSGB-LTPS-TFTs with bottom gate structure exhibited better electrical characteristics than the conventional top-gate ones, especially in short channel devices owing to the artificially controlled lateral grain growth. Because the channel region was in-situ designed at the large grain regions, the grain boundaries perpendicular to the current flow in the channel region could be reduced. In addition to the enhancement of TFT performance, TFTs crystallized with VSGB-LTPS structure also demonstrated excellent uniformity. The standard deviation of mobility was smaller than 30 cm^2/V*s and the standard deviation of threshold voltage was smaller than 0.1V. Therefore, we could reduce the number of shots as less as possible. High performance VSGB-LTPS-TFTs could be fabricated easily using bottom gate structure with 10 laser shots. Therefore, the number of laser shots was reduced and the throughput and the yield could be increased. This fact facilitated the industry application with the VSGB-LTPS method due to the cost reduction of fabricating LTPS-TFTs. Moreover, the VSGB-LTPS-TFTs could be fabricated with thinner gate oxide with high reliability. The VSGB-LTPS-TFTs with thinner gate oxide of 500 Å exhibited better electrical characteristics than those of oxide thickness of 1000Å, especially in short channel devices. This could be attributed to the better gate control ability. Thinner gate oxide could make the gate electrode control the channel more easily. The VSGB-LTPS-TFTs with thinner gate oxide also exhibited higher reliability than top-gate ones due to the low roughness interface between active layer and gate insulator. Therefore, higher performance VSGB-LTPS-TFTs with larger driving current and better subthreshold swing could be easily produced by thinner gate oxide without additional structures or materials.

Although VSGB-LTPS-TFTs exhibited high performance characteristic, the structure of

VSGB-LTPS-TFTs had an essential drawback. The disadvantage was the mis-alignment of source/drain ion implantation. In chapter 4, we carried out the novel SA-VSGB-LTPS-TFTs by combining backside exposure method and VSGB-LTPS-TFTs. Material analyses of SA-VSGB-LTPS TFTs were demonstrated by using Optical Microscope (OM) and SEM. From the OM and SEM images, the P.R. was self-aligned perfectly with the amorphous gate regions. The amorphous gates could act as the masks of the lithography to stop the ultra violate light from the Hg light. No shift of P.R. was observed after lithography. SA-VSGB-LTPS-TFT with field effect mobility of about 192 cm^2/V-s could be achieved by using amorphous gate thickness of 1000Å while the mobility the mis-aligned VSGB-LTPS-TFT was about only 17.76 cm^2/V-s. The improved driving current could be attributed to smaller series resistance near the source and drain regions due to self-aligned ion implantation. The GIDL and kink effect were also reduced. The trap density of the small grains near the source and drain regions wouldn't induce the GIDL and kink effect. Symmetrical electrical characteristics were also observed in SA-VSGB-LTPS-TFTs due to the self-aligned ion implantation. Due to the symmetrical electrical characteristics, we could fabricate the VSGB-LTPS-TFTs more suitable to the elements of the pixel switch devices.

To eliminate the single high angle grain boundary, continuous wave (CW) laser crystallization were proposed in chapter 5. In the first section of this chapter, laser activation by CW laser annealing was studied. It was found that laser activation by CW laser annealing was a low-thermal budget and high-efficiency method. Low sheet resistance of 47 Ω/□ was observed by four point probe measurement system. The redistribution profile was also observed by secondary ion mass spectrometer (SIMS). Due to the high scanning rate of the CW laser, the throughput of the activation was higher than conventional excimer laser activation. Therefore, the CW laser activation technology could reduce the activation time than any other methods. In the second section of this chapter, we demonstrated that high performance LTPS-TFTs could be fabricated by CLC method. The CLC-LTPS-TFTs exhibited

better electrical characteristics than ELC ones. High field effect mobilities result from the super-giant grains and fewer intragrain defects. In addition, the grain boundaries were generally parallel to one another and to the scan direction of the laser beam. If the scanning direction was parallel to the current flow of the TFT, there would be no grain boundary in the channel region. Therefore, the mobilities were 164 cm^2/V-s for n-type CLC-LTPS-TFTs and 92 cm^2/V-s for p-type CLC-LTPS-TFTs. Moreover, the process flow was simple because the process flows were compatible with conventional top-gate LTPS-TFTs process. Additionally, due to the high scanning rate of CLC method, the throughput of CLC-LTPS-TFTs was improved. Hence, the CLC method was quite promising for the system on panel (SOP) application in the future.

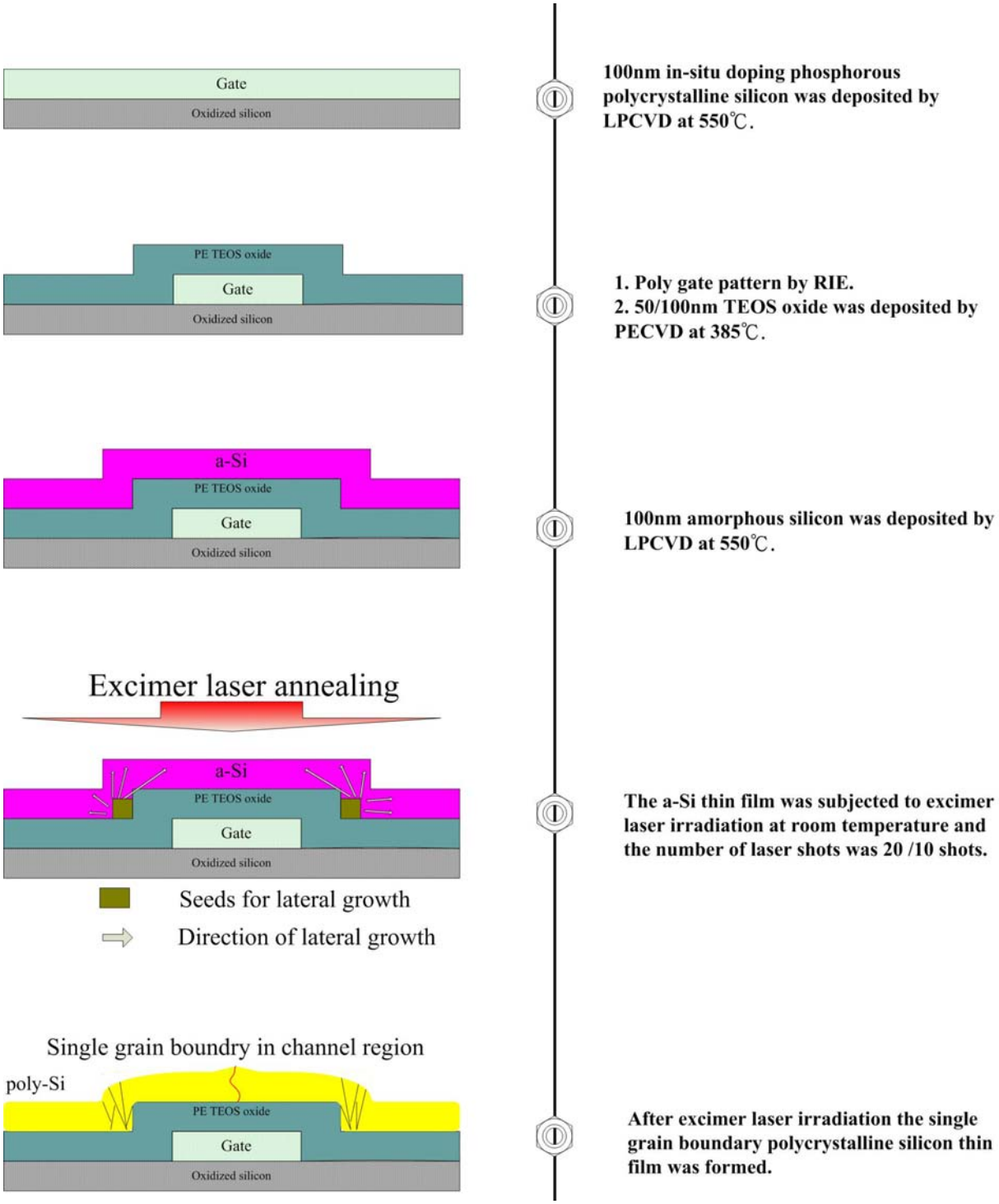


Fig. 2-1 Process flow of preparing samples for material characteristics of vertical single grain boundary low temperature polycrystalline silicon thin films.

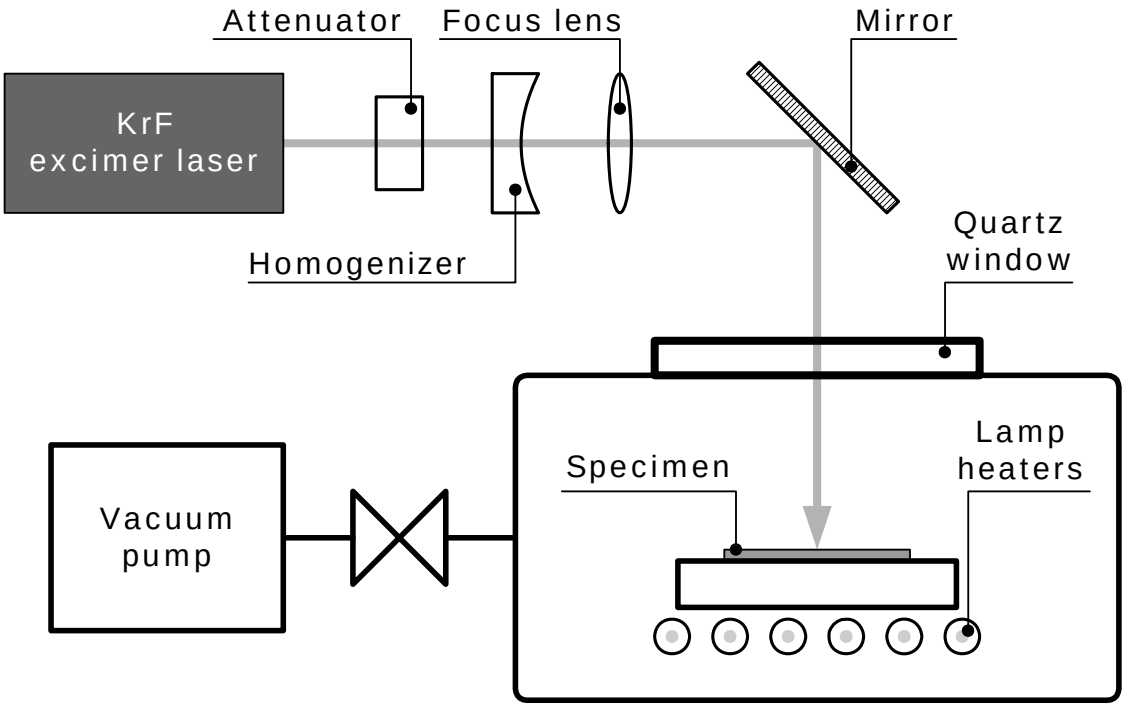
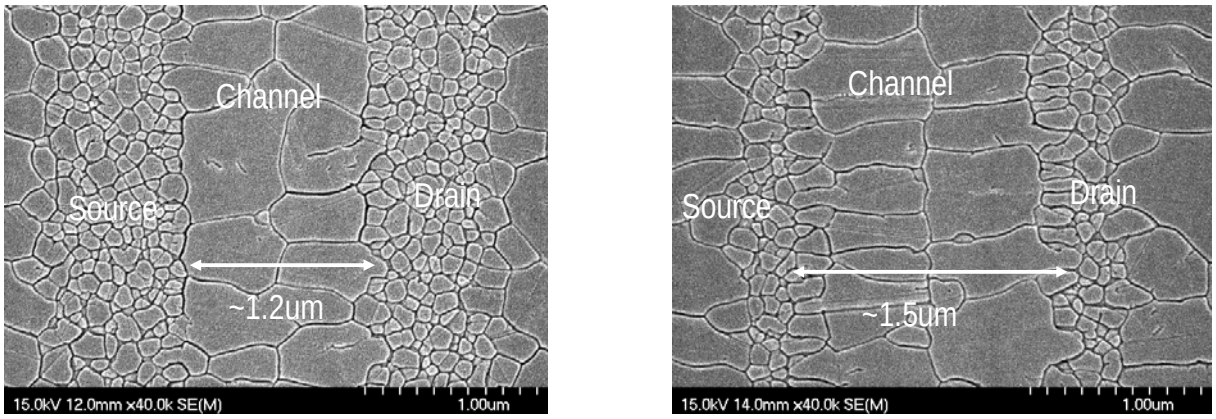
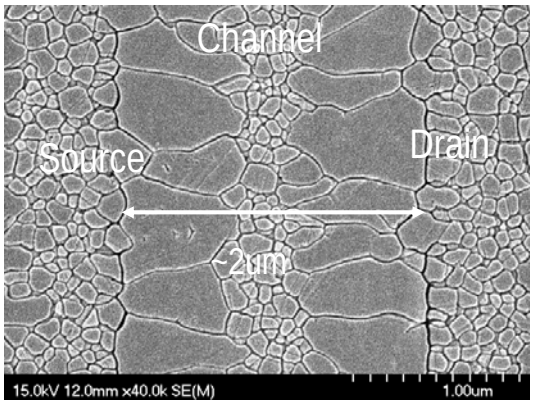


Fig. 2-2 A brief schematic of the excimer laser system.

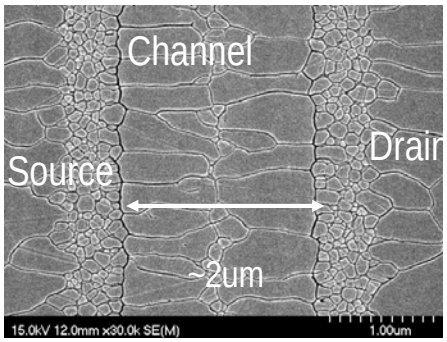


(a) (b)

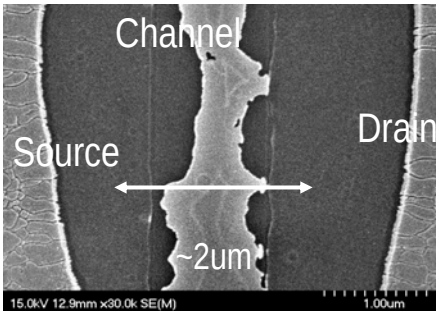
Fig. 2-3 SEM graphs of excimer laser crystallized polycrystalline silicon thin films with bottom gate structure. The channel length was 1μm (a) and 1.5μm (b). The laser energy density was 420 mJ/cm^2 and the gate oxide thickness was 1000Å.



(a)

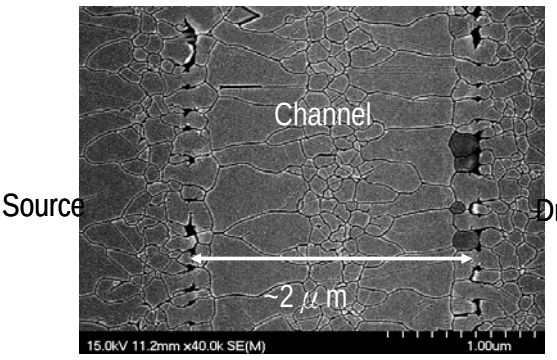


(b)

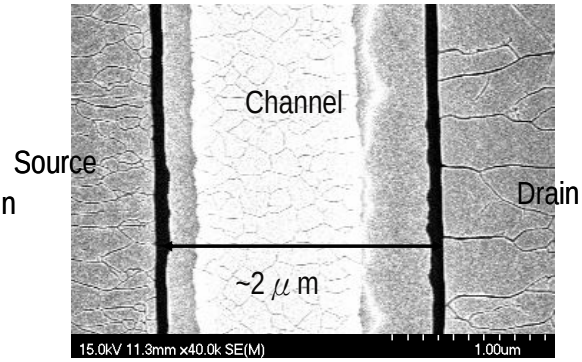


(c)

Fig. 2-4 SEM graphs of excimer laser crystallized polycrystalline silicon thin films with bottom gate structure. The channel length was 2 μm. The poly gate thickness was 1000Å and the gate oxide thickness was 1000Å. The laser energy density was 420 (a) 450 (b) 480 (c) mJ/cm2.

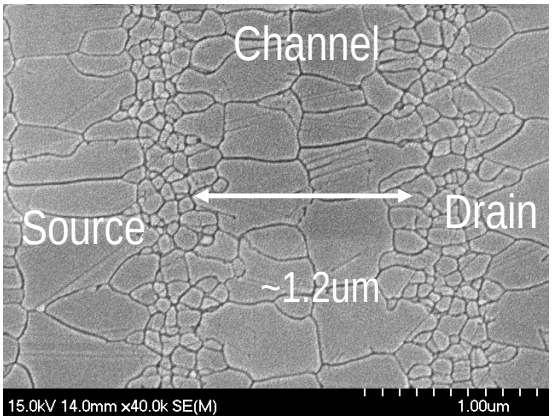


(a)

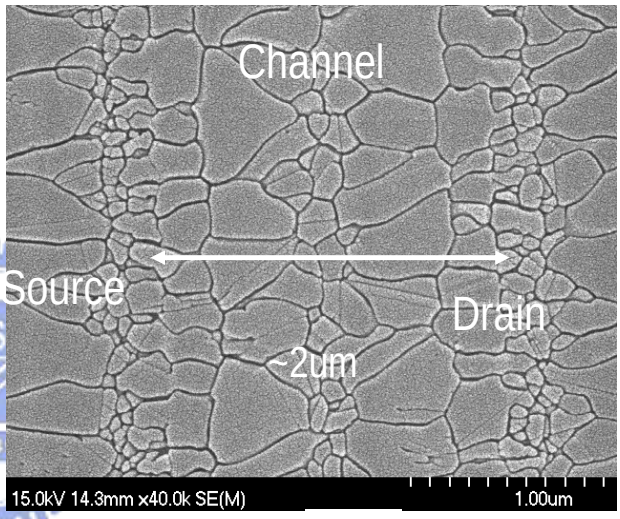


(b)

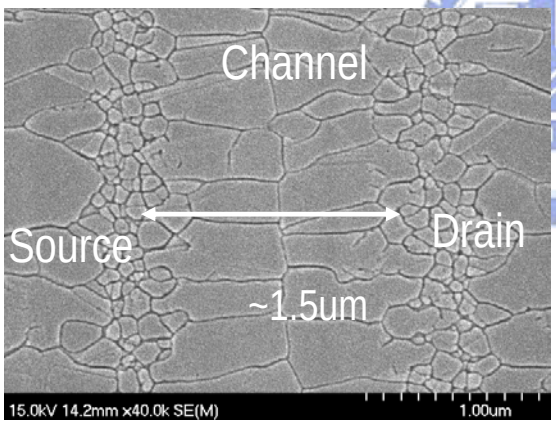
Fig. 2-5 SEM graph of excimer laser crystallized polycrystalline silicon thin films with bottom gate structure. The channel length was 2 μm. The laser energy density was 420 mJ/cm^2 and the gate oxide thickness was 1000Å. The poly gate thickness was 2000Å(a) 3000Å(b).



(a)



(c)



(b)

Fig. 2-6 SEM graphs of excimer laser crystallized polycrystalline silicon with bottom gate structure. The channel length was varied from 1.2μm to 2 μm. The poly gate thickness was 1000Å and the gate oxide thickness was 1000Å. The laser energy density was 420 mJ/cm^2

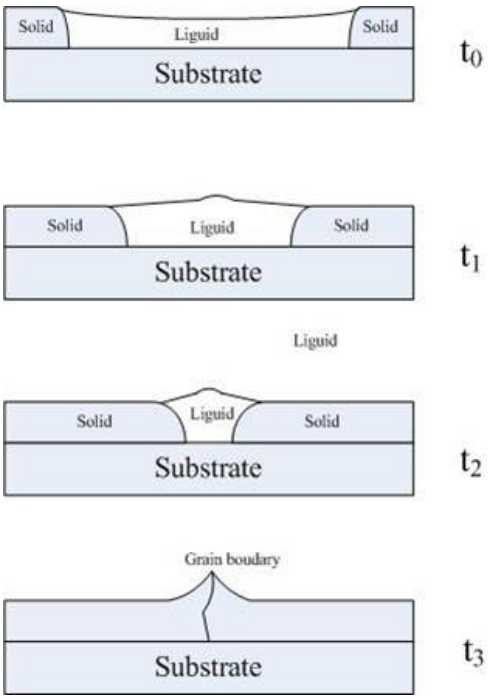
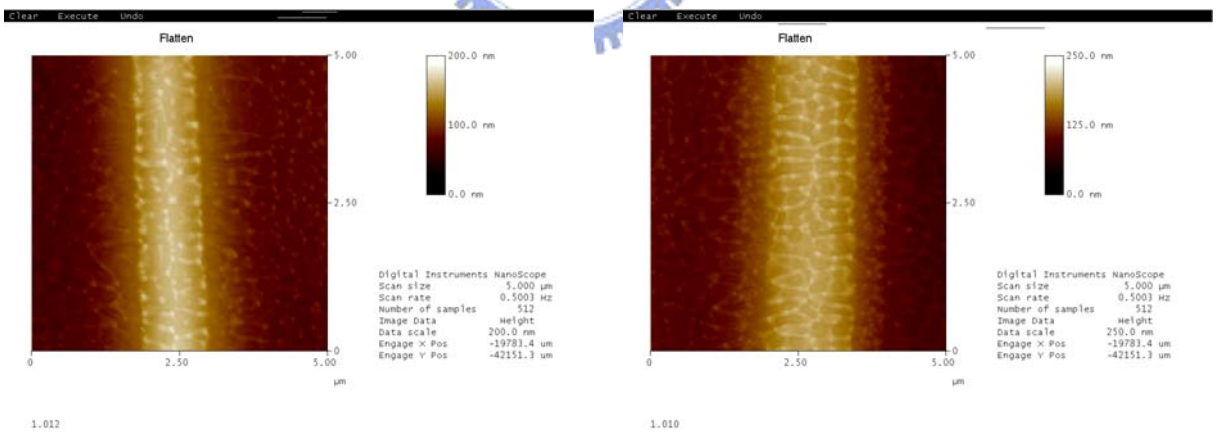


Fig. 2-7 Hillock formation at the grain boundaries. Driving force: density change between liquid and solid silicon. 2.53 g/cm^3 for liquid silicon. 2.30 g/cm^3 for solid silicon.



(a) (b)

Fig. 2-8 AFM graphs of excimer laser crystallized polycrystalline silicon thin films with bottom gate structure. The channel length was 1.2 µm(a) 1.5µm(b). The laser energy density was 420 mJ/cm^2. The poly gate thickness was 1000Å.

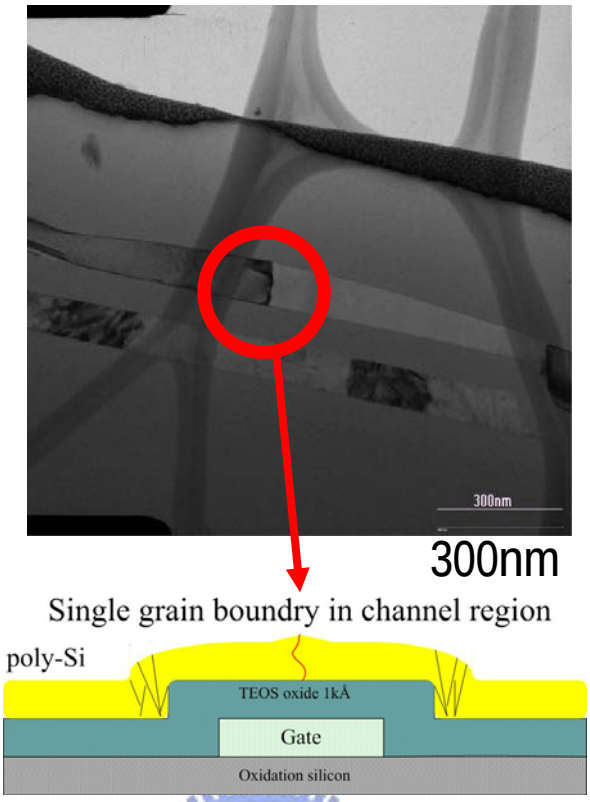


Fig. 2-9 Cross-section TEM graph of excimer laser crystallized polycrystalline silicon thin films with bottom gate structure. The channel length was 1.5μm. The laser energy density was 420 mJ/cm^2. The poly gate thickness was 1000Å.

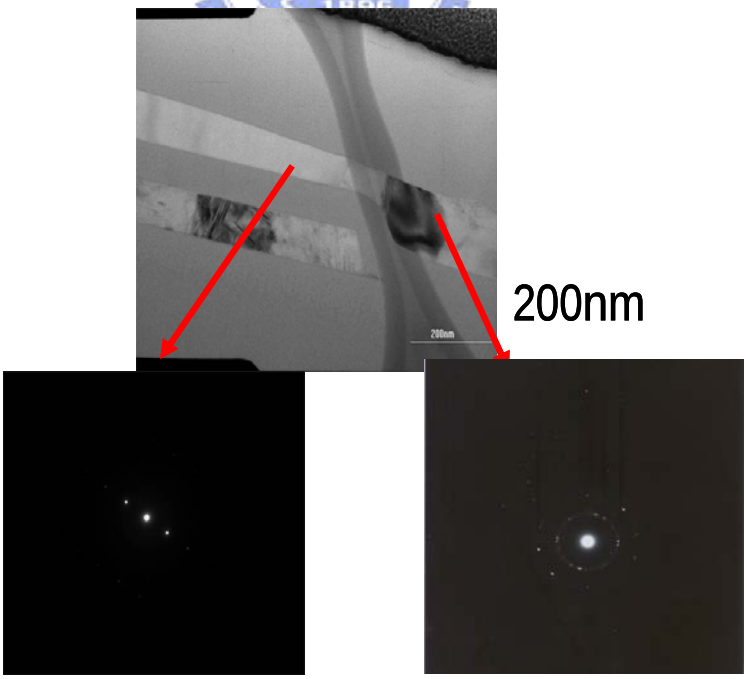


Fig. 2-10 Cross section TEM graph and correlated diffraction pattern of excimer laser crystallized polycrystalline silicon thin films with bottom gate structure. The channel length was 1.5μm. The laser energy density was 420 mJ/cm^2. The poly gate thickness was 1000Å.

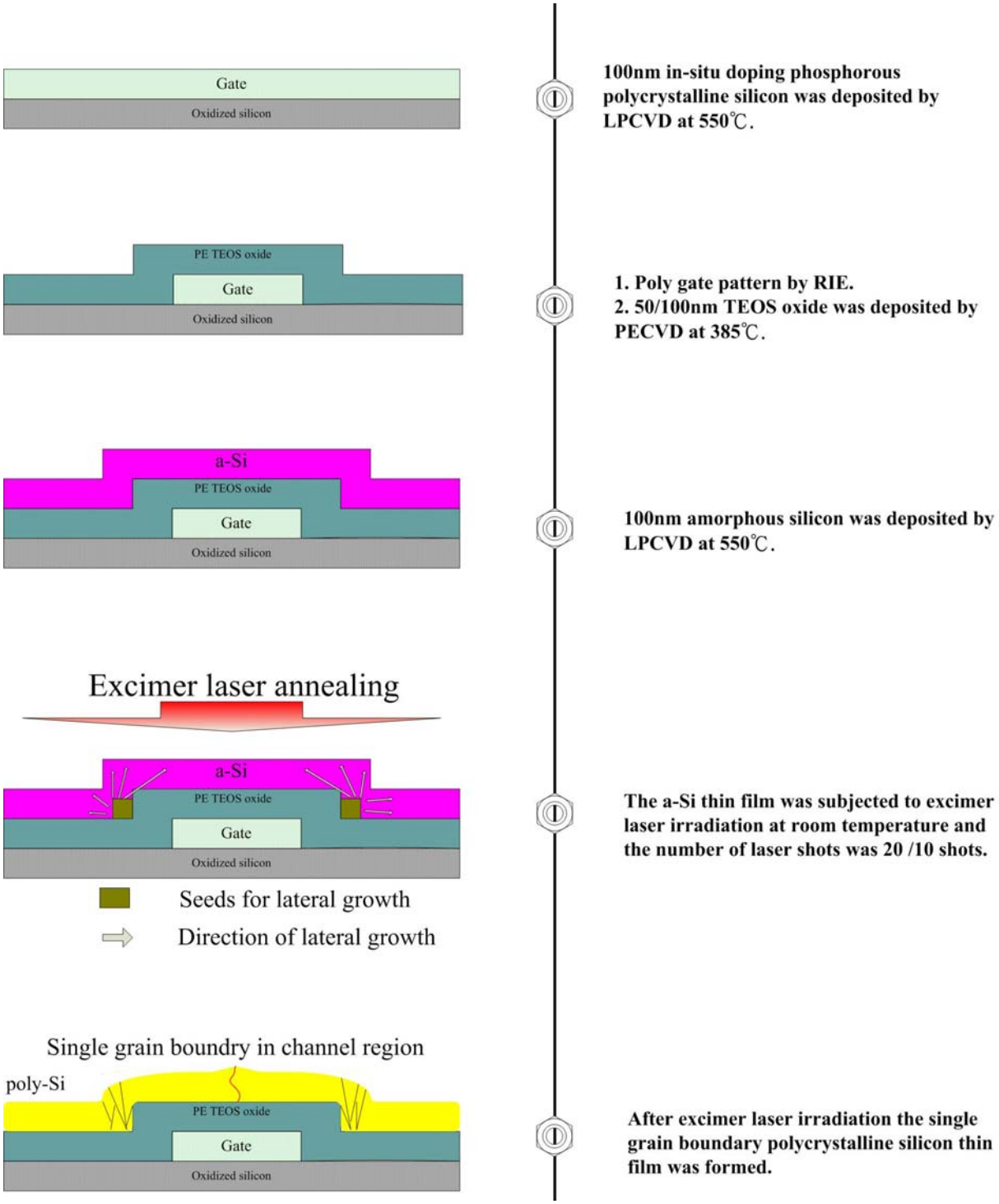


Fig. 3-1 The key processes for fabrication of VSGB-LTPS-TFTs (I)

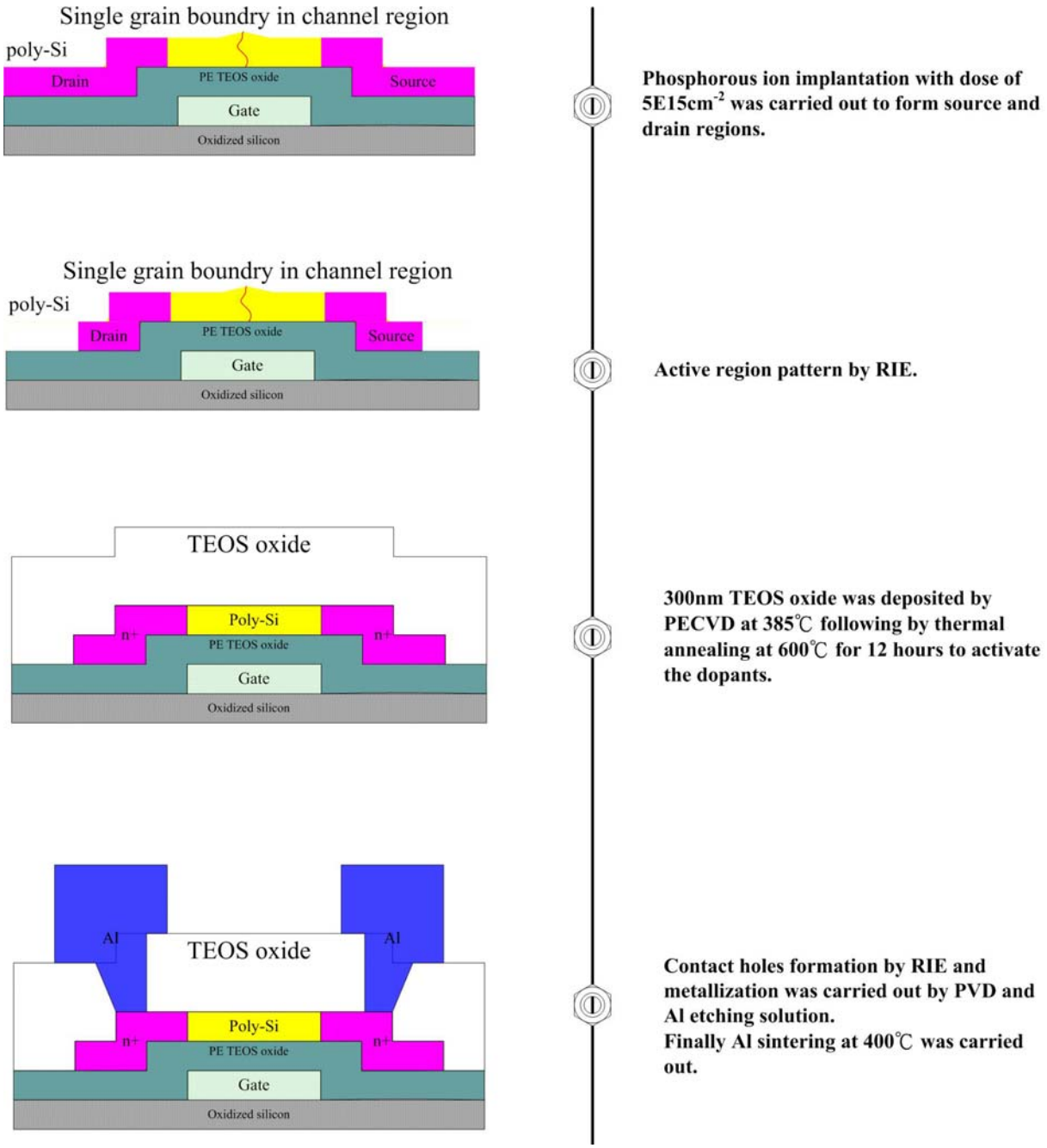


Fig. 3-1 The key processes for fabrication of VSGB-LTPS-TFTs (II)

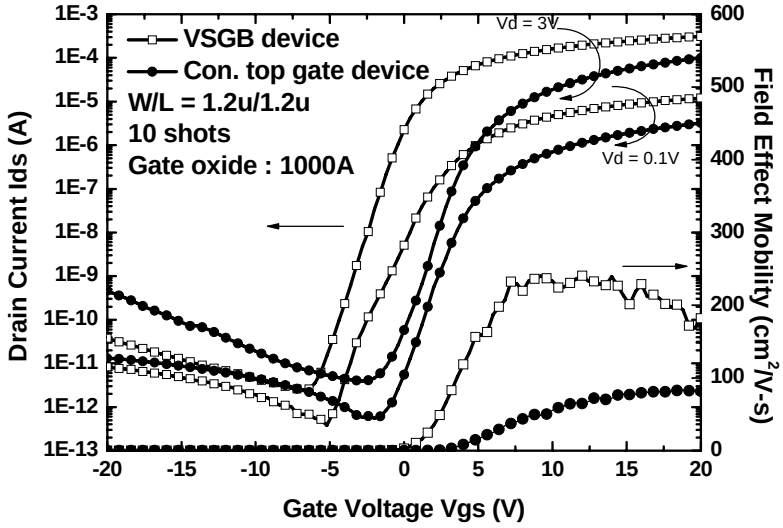


Fig. 3-2 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

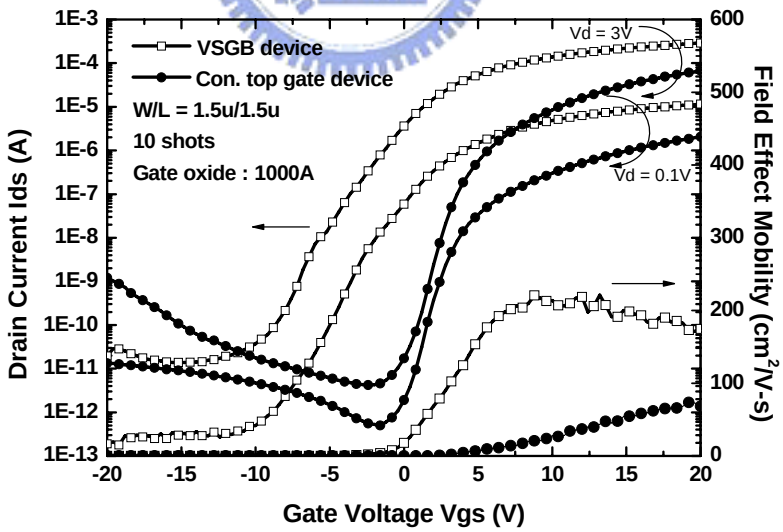


Fig. 3-3 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

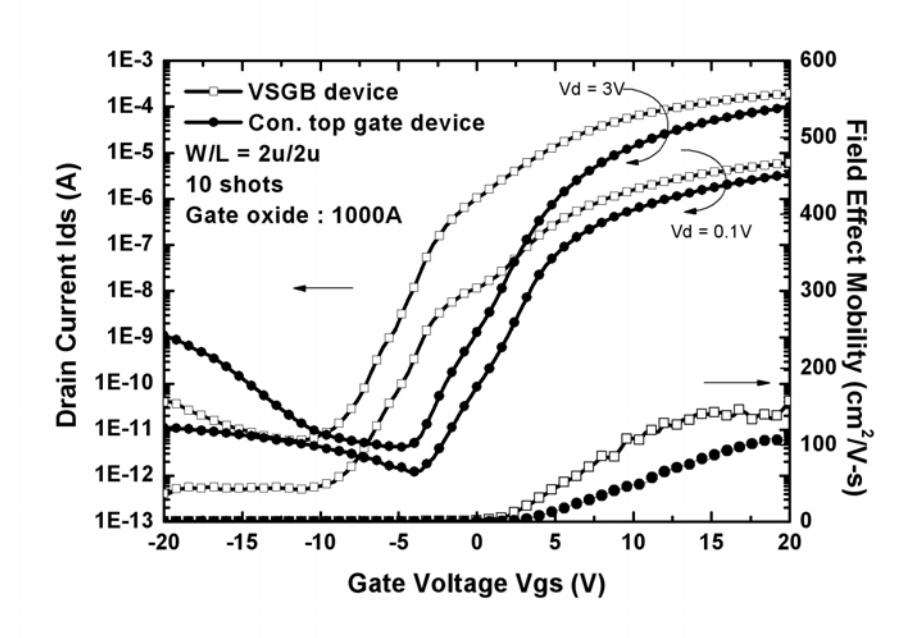


Fig. 3-4 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

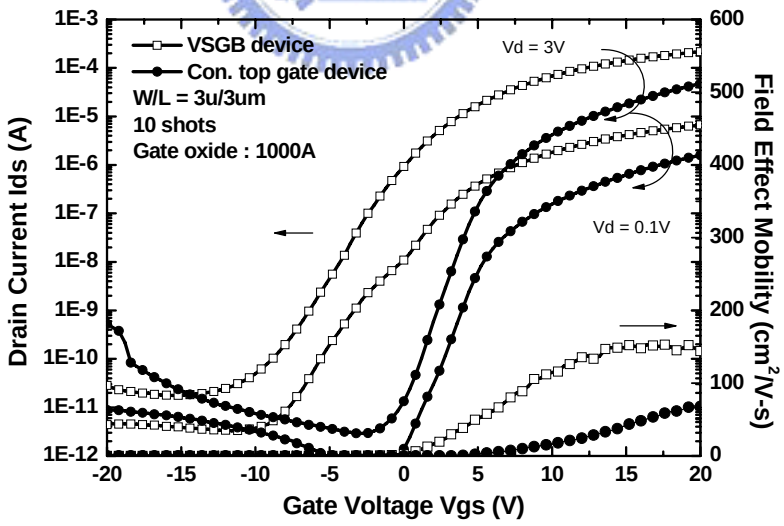


Fig. 3-5 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 3 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

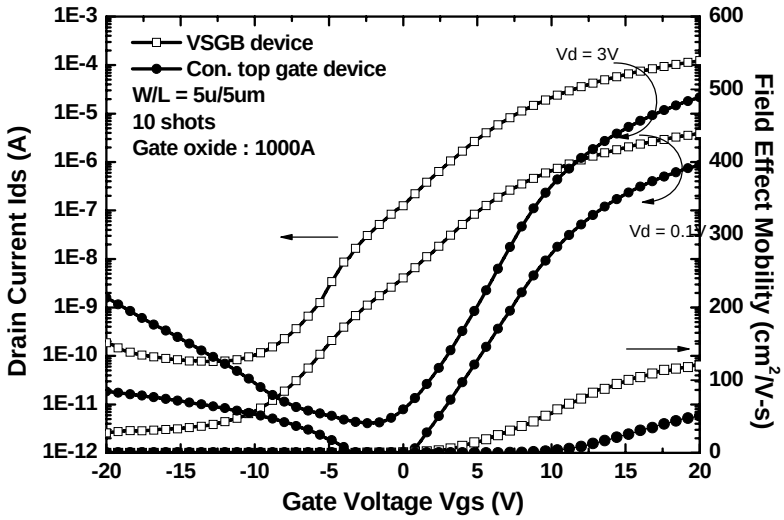


Fig. 3-6 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

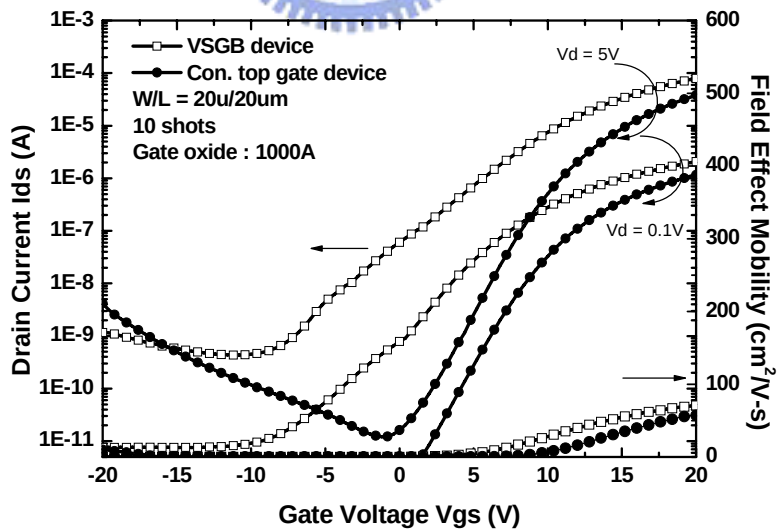


Fig. 3-7 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 20 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

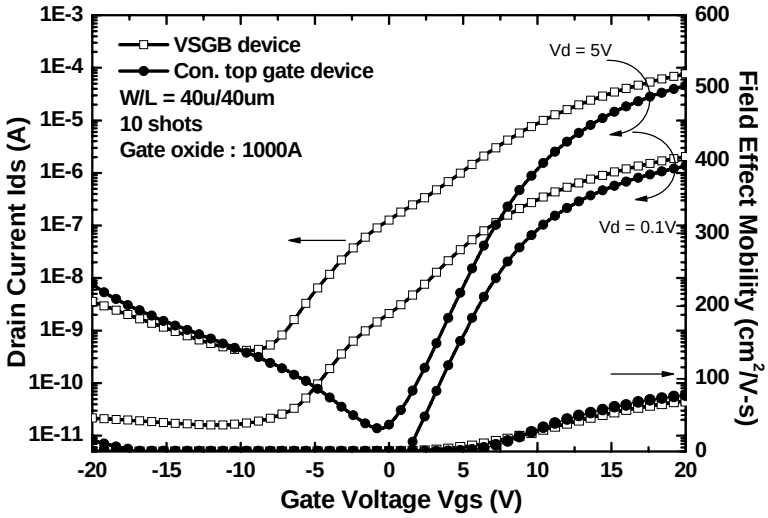


Fig. 3-8 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 40 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

10 shots Gate oxide: 1000 Å	Mobility (cm^2/V-s)	Sub-threshold swing (V/dec)	Vth (V)	on/off current ratio at Vds = 3 V
conventional top gate LTPS-TFT (W/L= 1.2/1.2um)	79.388	1.128	3.515	1.52E+07
VSGB-LTPS-TFT (W/L= 1.2/1.2um)	224.343	1.021	-0.803	1.24E+08
conventional top gate LTPS-TFT (W/L= 1.5/1.5um)	87.815	1.275	3.907	9.59E+06
VSGB-LTPS-TFT (W/L= 1.5/1.5um)	211.504	1.313	-0.893	5.10E+07
conventional top gate LTPS-TFT (W/L= 2/2um)	78.933	1.291	5.812	2.39E+07
VSGB-LTPS-TFT (W/L= 2/2um)	150.272	1.795	-0.086	3.28E+07

Table 3. 1 Measured optimal electrical characteristics of TFTs crystallized with VSGB-LTPS structure and conventional structure in short channel devices. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

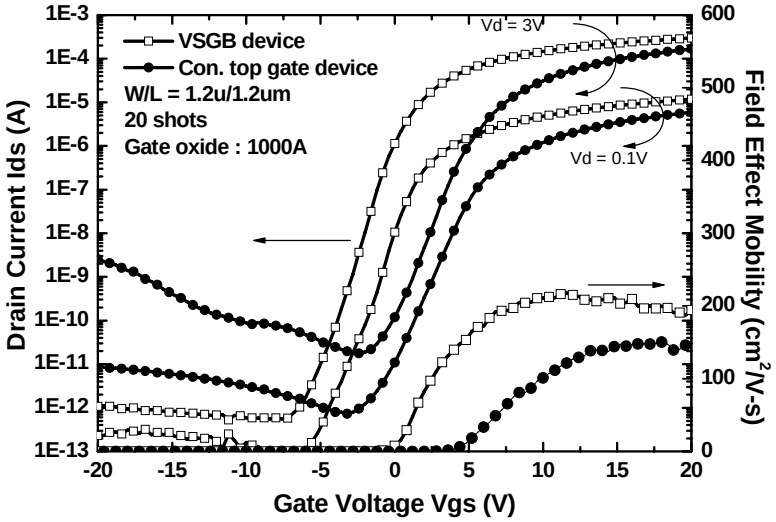


Fig. 3-9 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

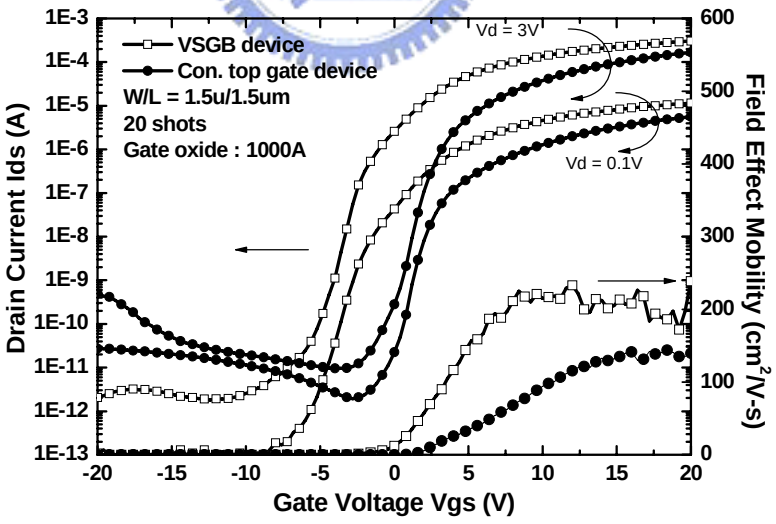


Fig. 3-10 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

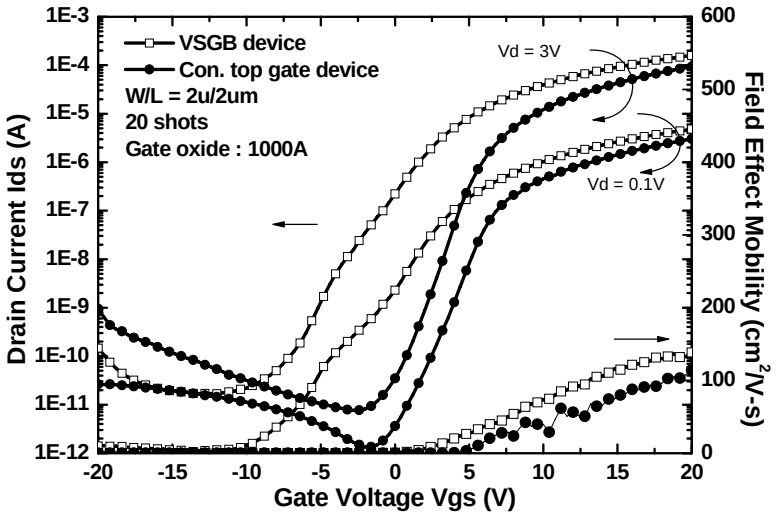


Fig. 3-11 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

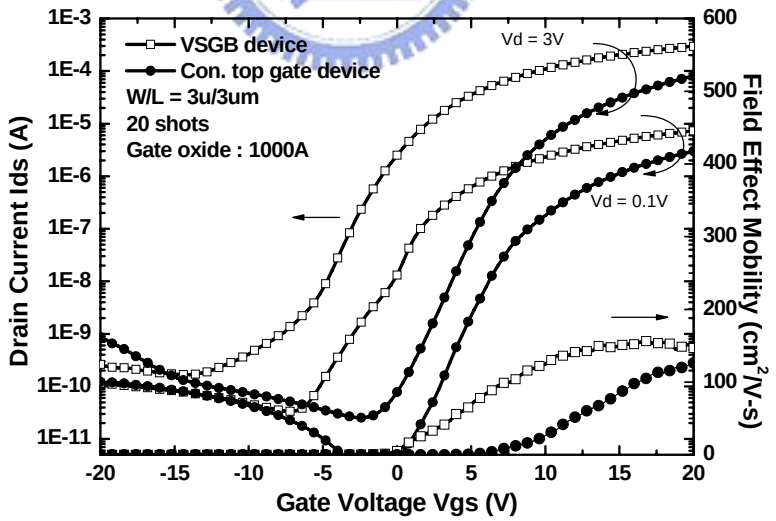


Fig. 3-12 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 3 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

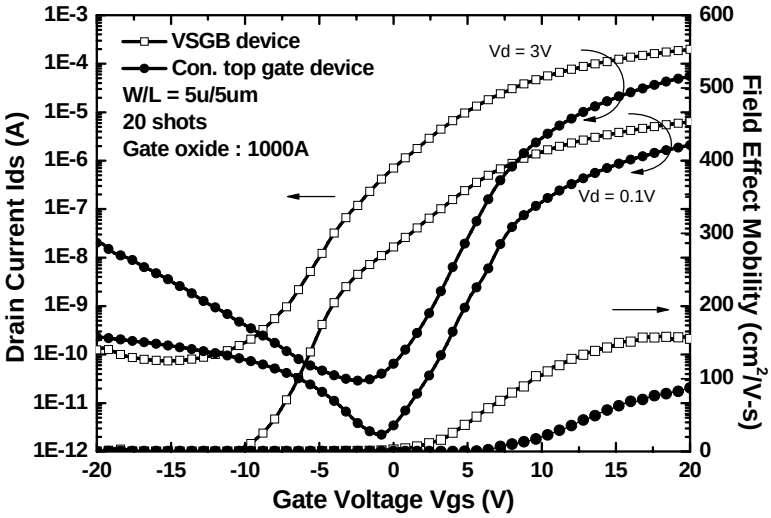


Fig. 3-13 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

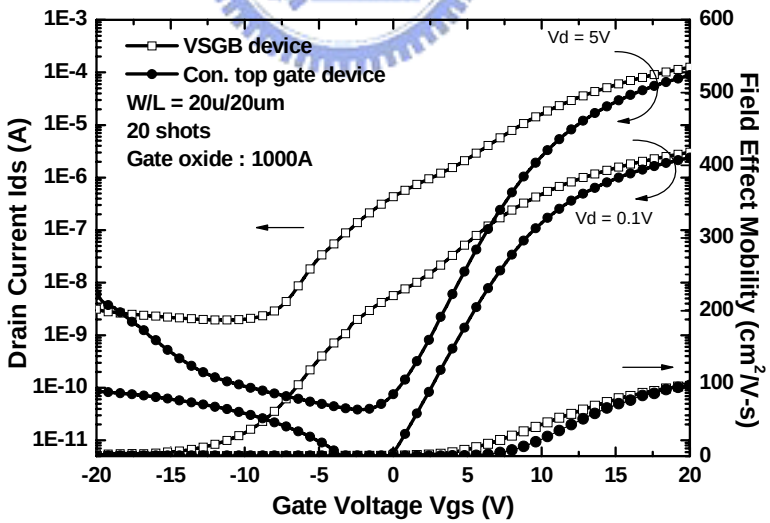


Fig. 3-14 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 20 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

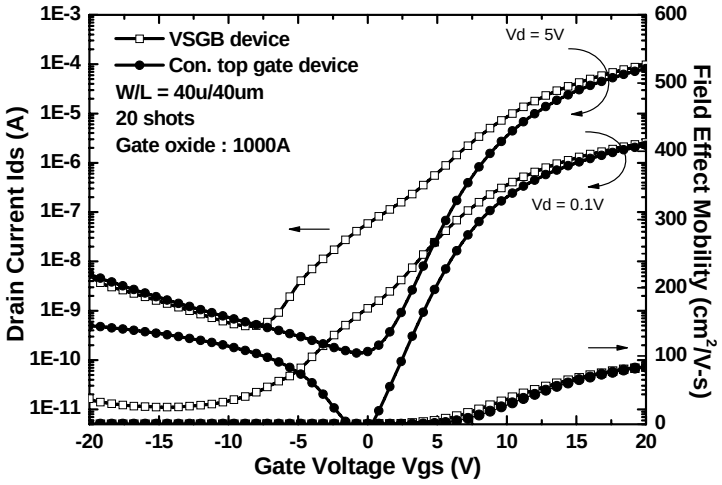


Fig. 3-15 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 40 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

20 shots Gate oxide: 1000 Å	Mobility (cm^2/V-s)	Sub-threshold swing (V/dec)	Vth (V)	on/off current ratio at Vds = 3 V
conventional top gate LTPS-TFT (W/L= 1.2/1.2um)	144.567	1.089	1.895	9.44E+06
VSGB-LTPS-TFT (W/L= 1.2/1.2um)	234.869	0.969	-1.238	5.60E+08
conventional top gate LTPS-TFT (W/L= 1.5/1.5um)	102.410	1.260	3.326	1.75E+07
VSGB-LTPS-TFT (W/L= 1.5/1.5um)	249.204	1.361	-1.104	1.68E+08
conventional top gate LTPS-TFT (W/L= 2/2um)	88.429	1.253	5.092	9.35E+06
VSGB-LTPS-TFT (W/L= 2/2um)	152.724	1.911	0.070	1.23E+07

Table 3. 2 Measured optimal electrical characteristics of TFTs crystallized with VSGB-LTPS structure and conventional structure in short channel devices. The thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

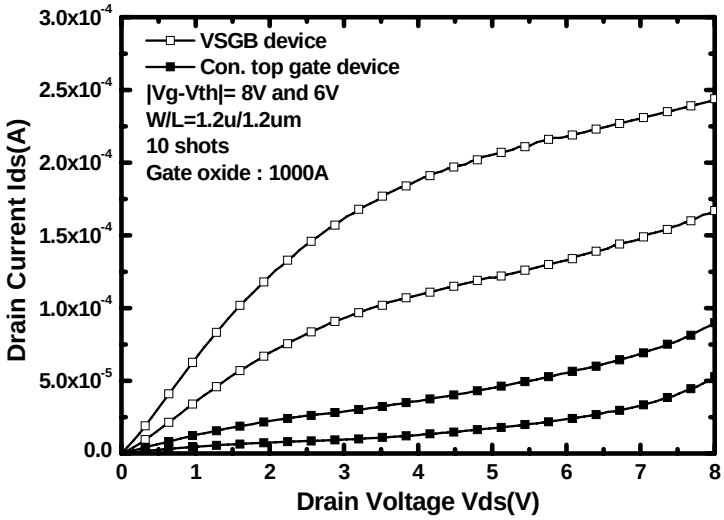


Fig. 3-16 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

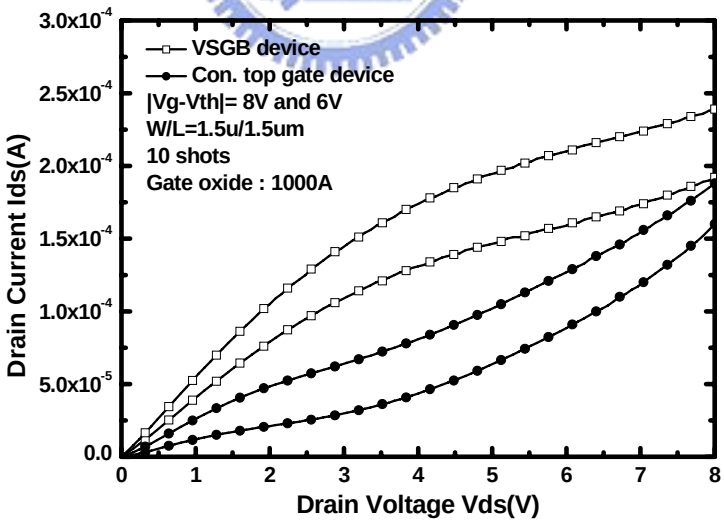


Fig. 3-17 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

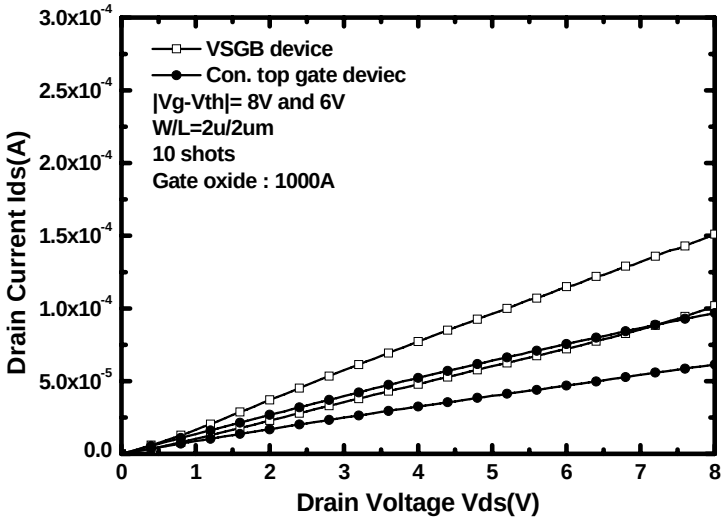


Fig. 3-18 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

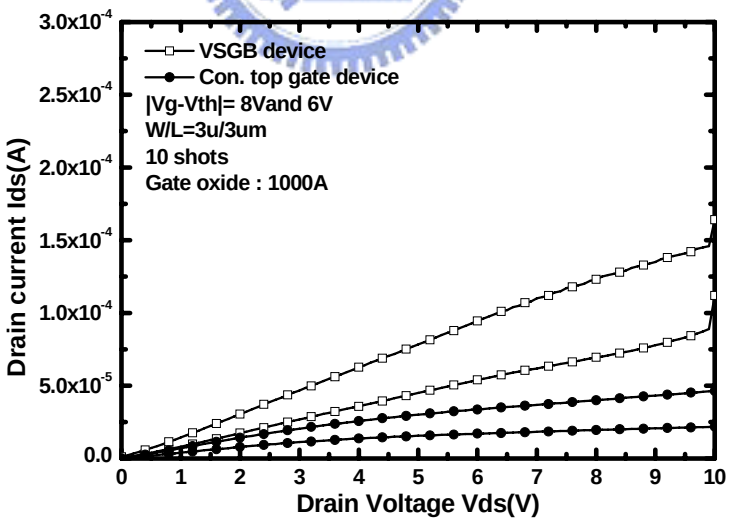


Fig. 3-19 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 3 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

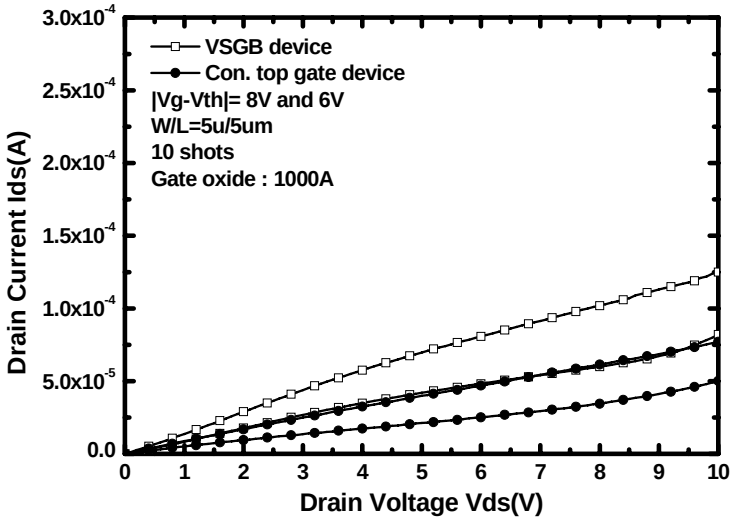


Fig. 3-20 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 20 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

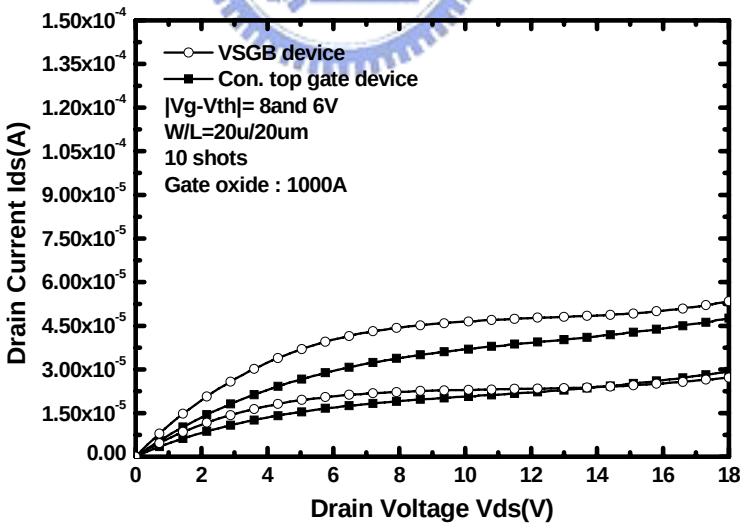


Fig. 3-21 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 20 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

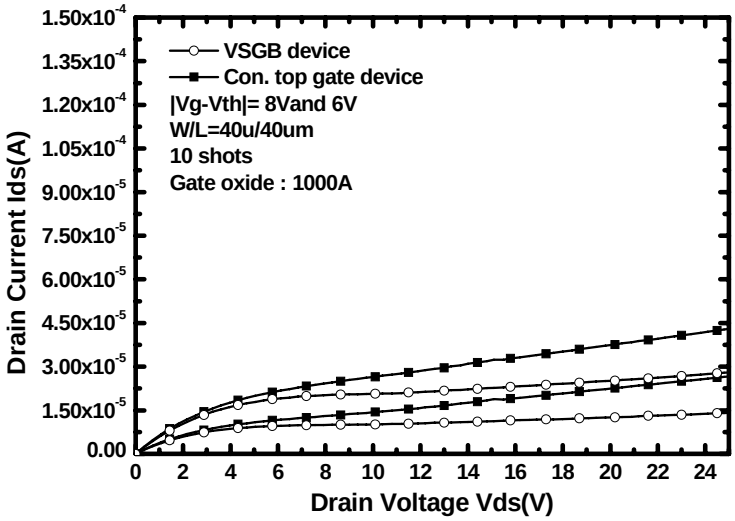


Fig. 3-22 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 40 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

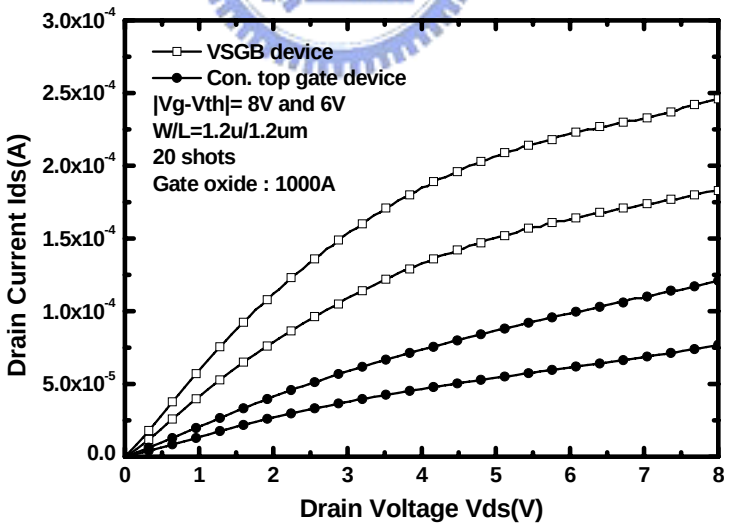


Fig. 3-23 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

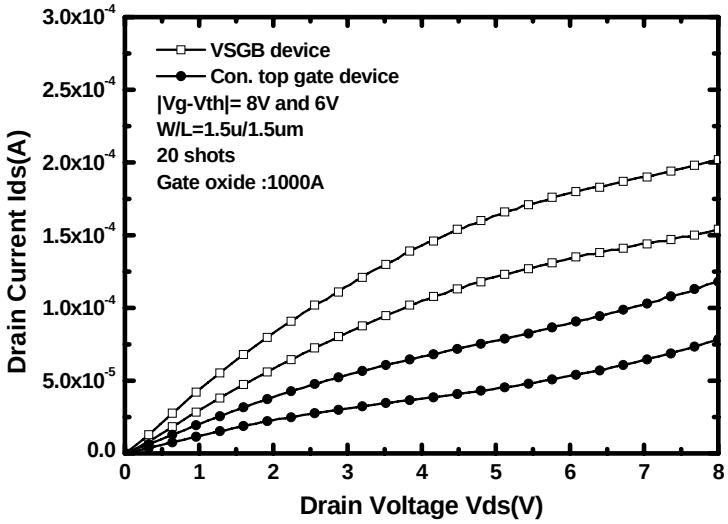


Fig. 3-24 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

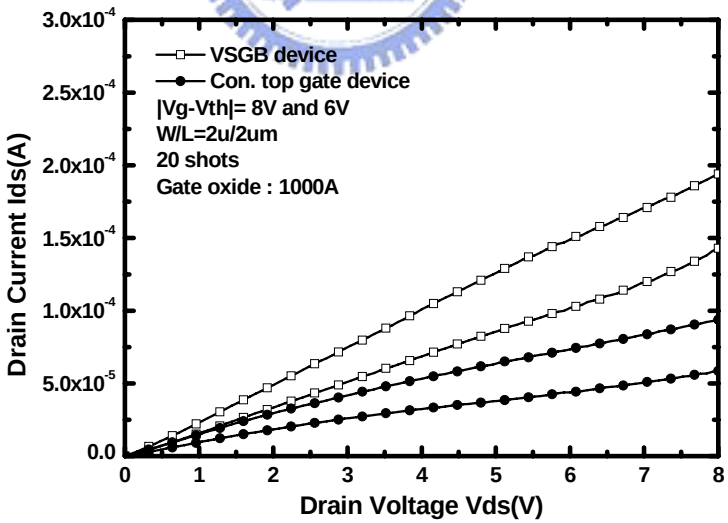


Fig. 3-25 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

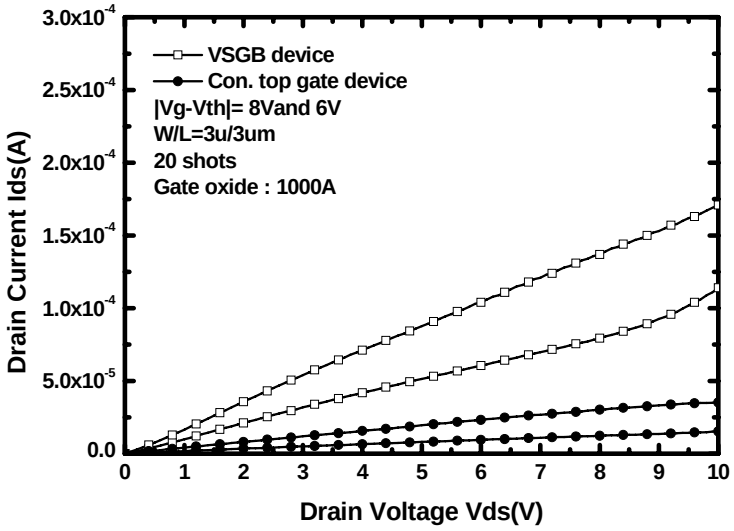


Fig. 3-26 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 3 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

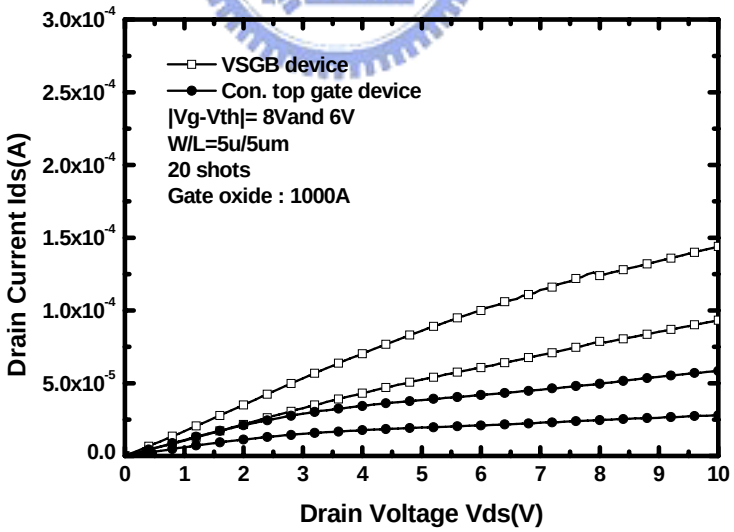


Fig. 3-27 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

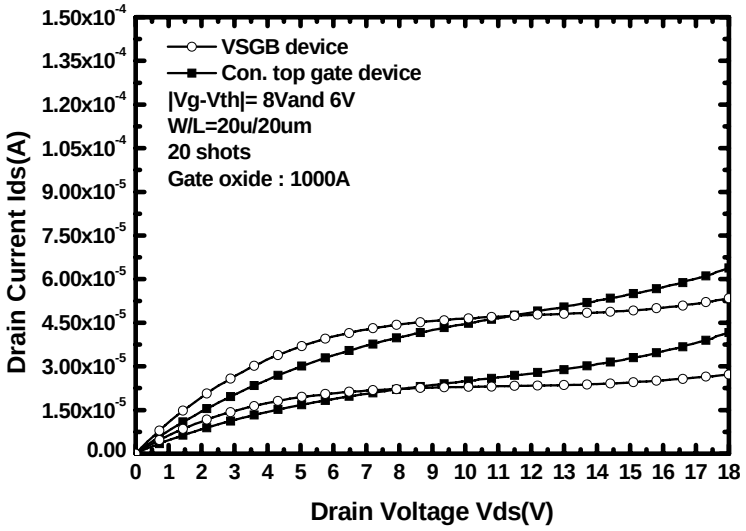


Fig. 3-28 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 20 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

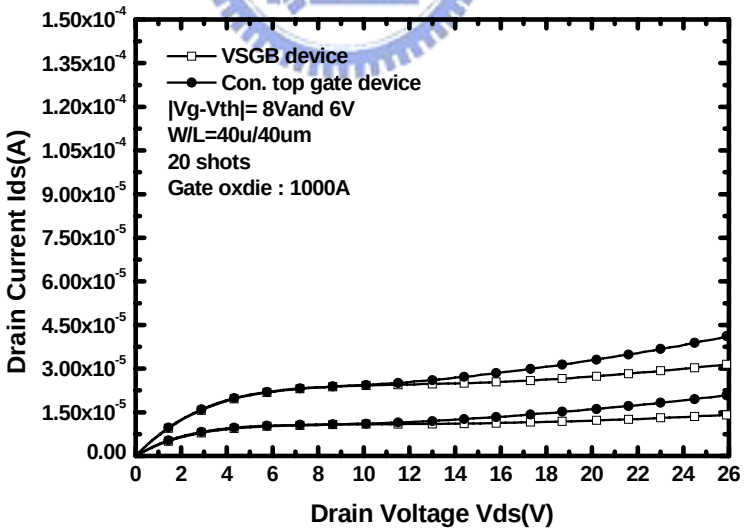


Fig. 3-29 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 40 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

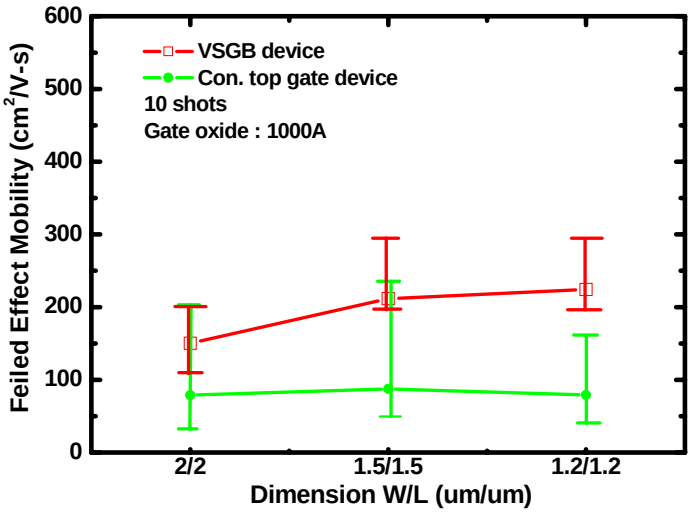


Fig. 3-30 The dependence of field-effect mobility on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

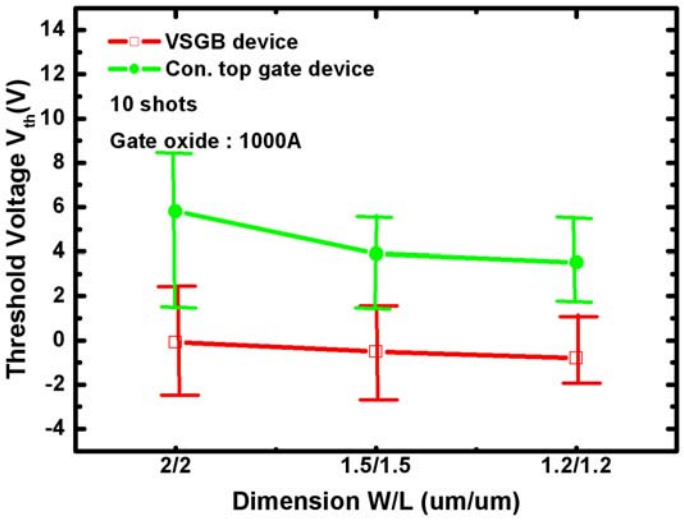


Fig. 3-31 The dependence of threshold voltage on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

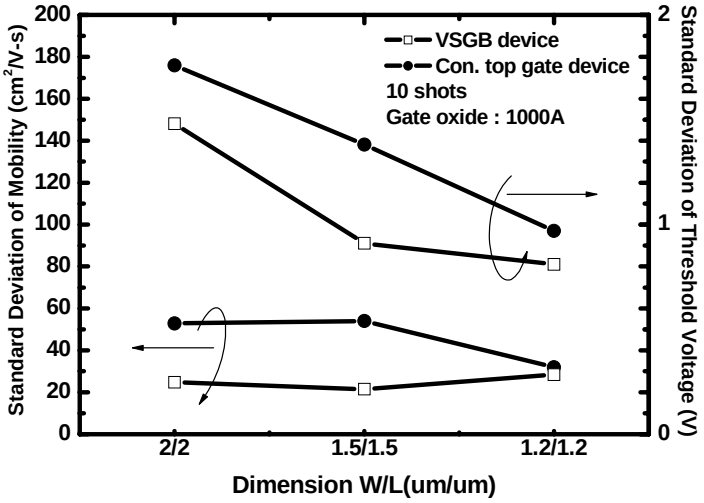


Fig. 3-32 The dependences of standard deviation of field-effect mobility and threshold voltage on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping).

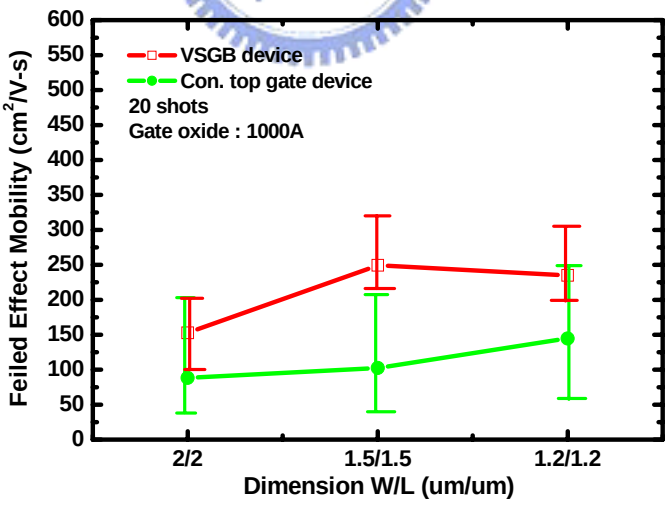


Fig. 3-33 The dependence of field-effect mobility on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

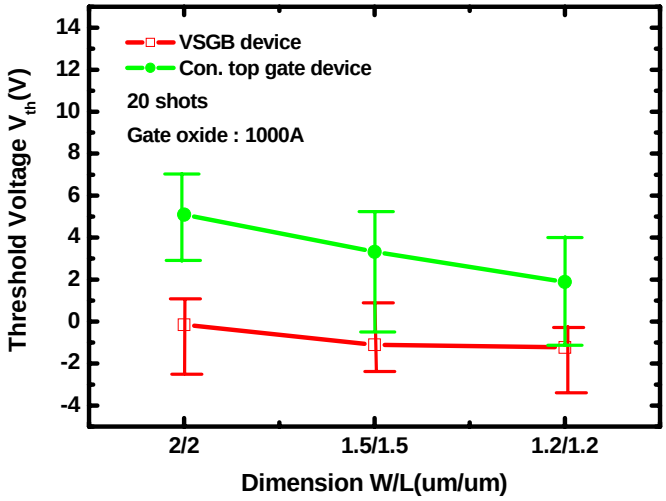


Fig. 3-34 The dependence of threshold voltage on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

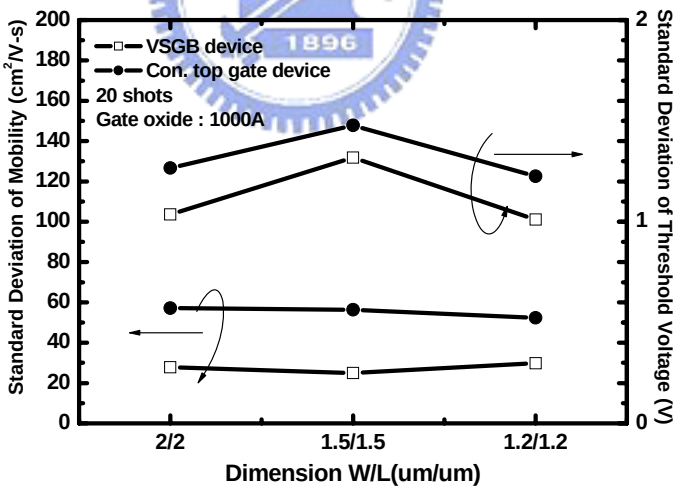


Fig. 3-35 The dependences of standard deviation of field-effect mobility and threshold voltage on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping).

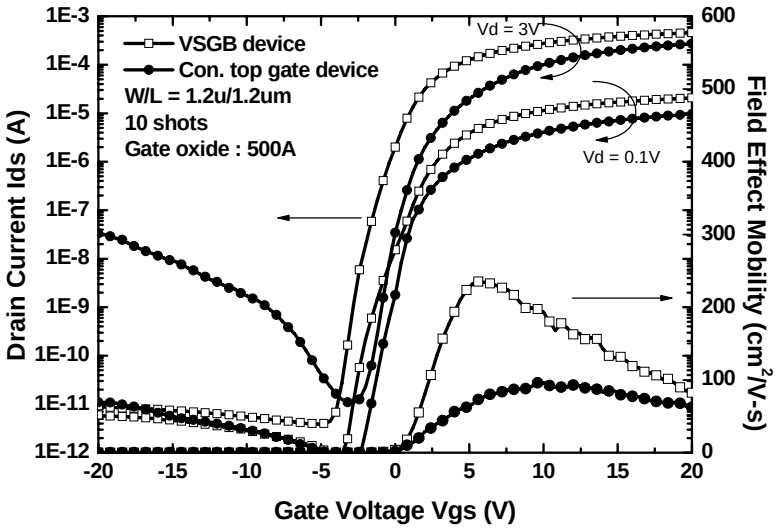


Fig. 3-36 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

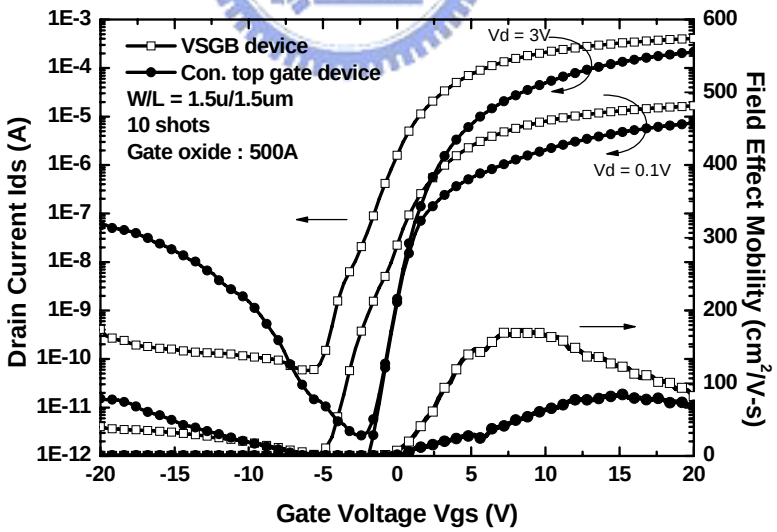


Fig. 3-37 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

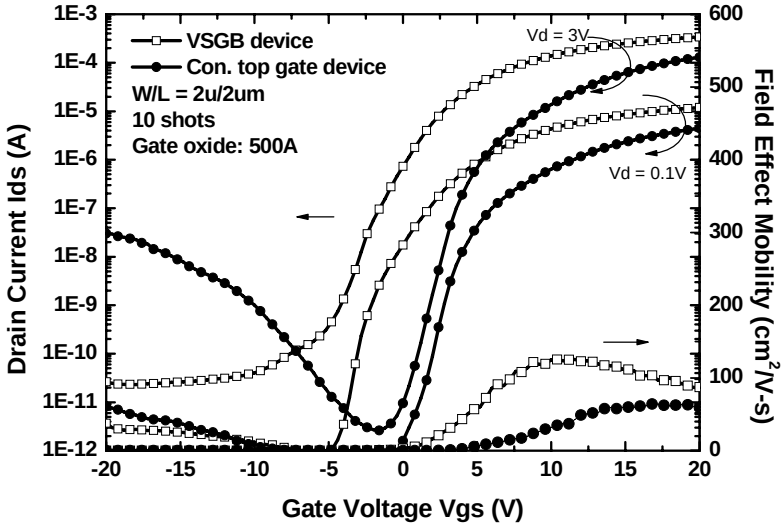


Fig. 3-38 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 2 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

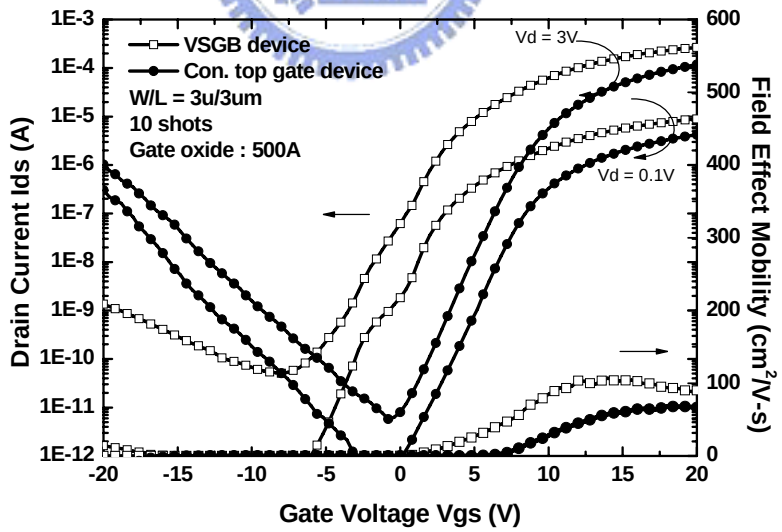


Fig. 3-39 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 3 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

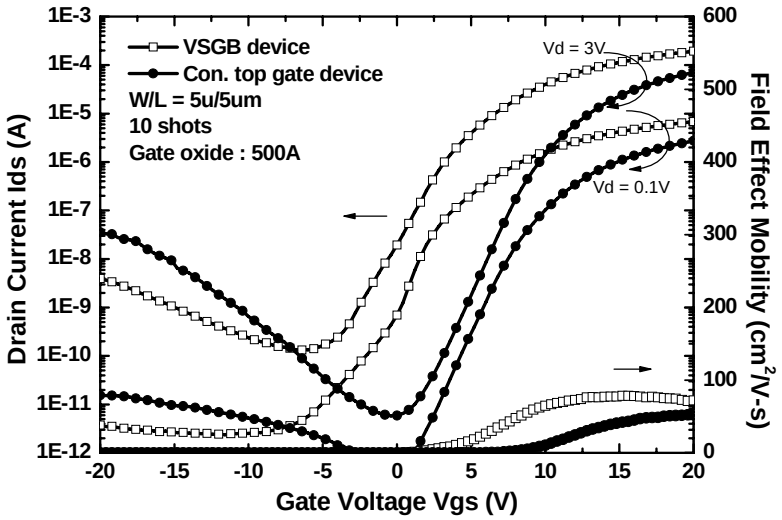


Fig. 3-40 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 5 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

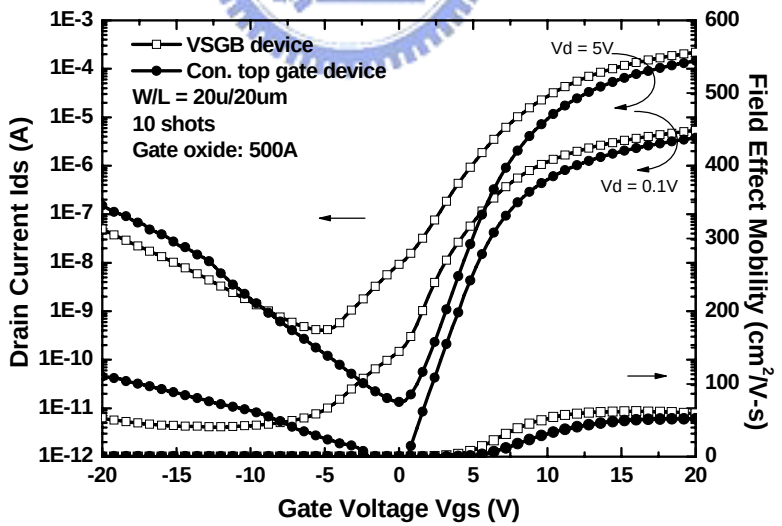


Fig. 3-41 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 20 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

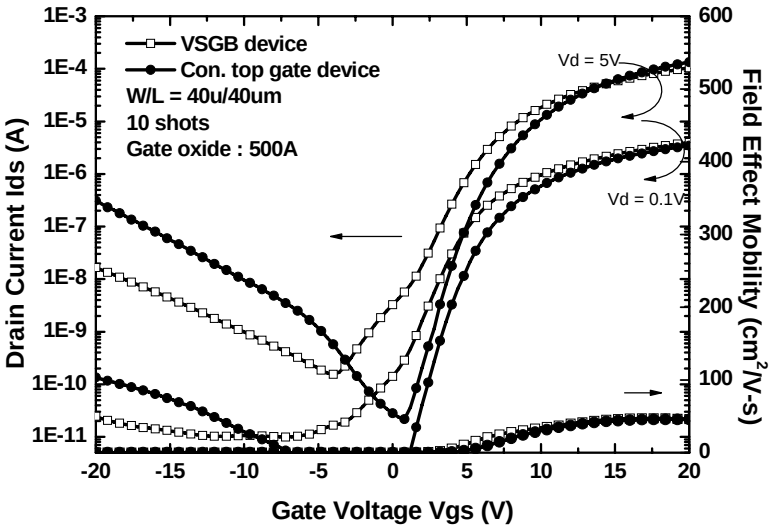


Fig. 3-42 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 40 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

10 shots Gate oxide: 500 Å	Mobility (cm^2/V-s)	Sub-threshold swing (V/dec)	Vth (V)	on/off current ratio at Vds = 3 V
conventional top gate LTPS-TFT (W/L= 1.2/1.2um)	76.867	0.514	0.006	2.53E+07
VSGB-LTPS-TFT (W/L= 1.2/1.2um)	203.123	0.482	-0.465	1.19E+08
conventional top gate LTPS-TFT (W/L= 1.5/1.5um)	78.659	0.617	0.861	7.05E+06
VSGB-LTPS-TFT (W/L= 1.5/1.5um)	171.951	0.661	-0.890	8.17E+07
conventional top gate LTPS-TFT (W/L= 2/2um)	65.038	0.861	3.969	5.00E+07
VSGB-LTPS-TFT (W/L= 2/2um)	122.796	1.040	-0.082	1.47E+07

Table 3. 3 Measured optimal electrical characteristics of TFTs crystallized with VSGB-LTPS structure and conventional structure in short channel devices. The thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

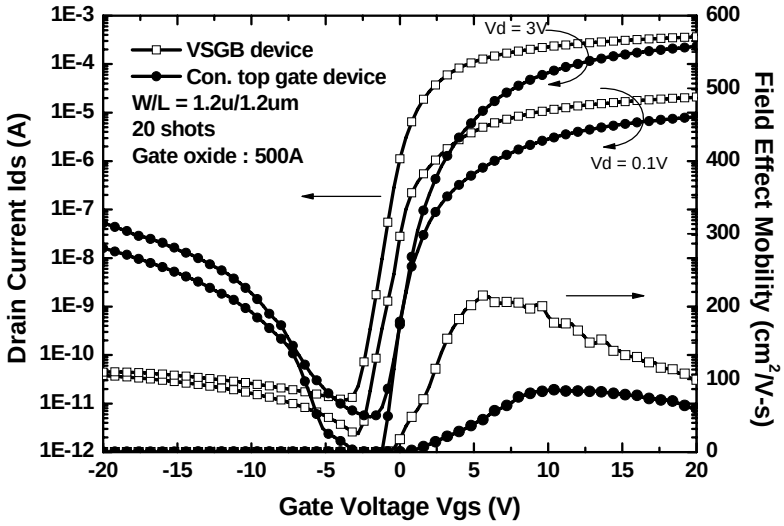


Fig. 3-43 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

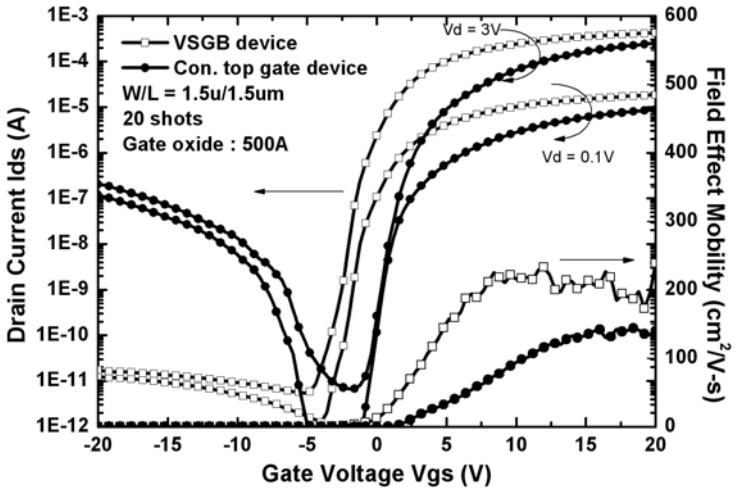


Fig. 3-44 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

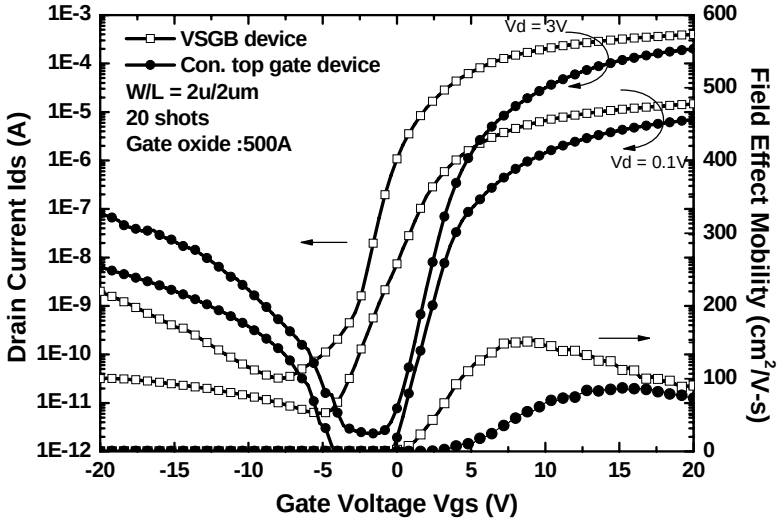


Fig. 3-45 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 2 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

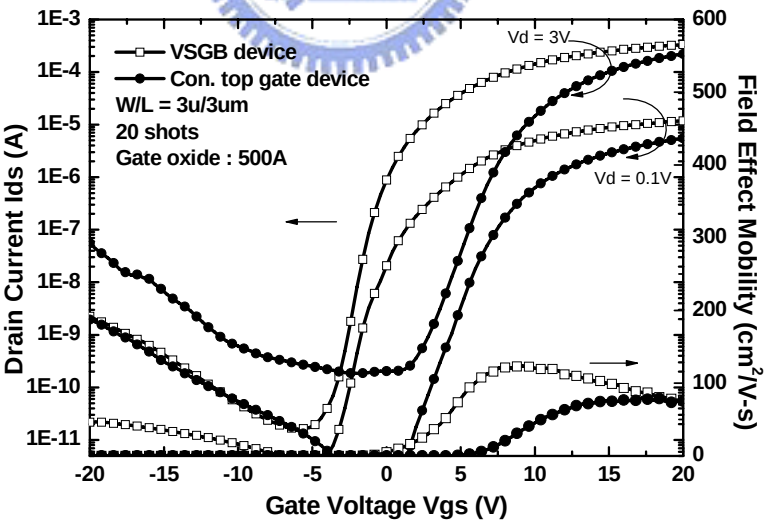


Fig. 3-46 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 3 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

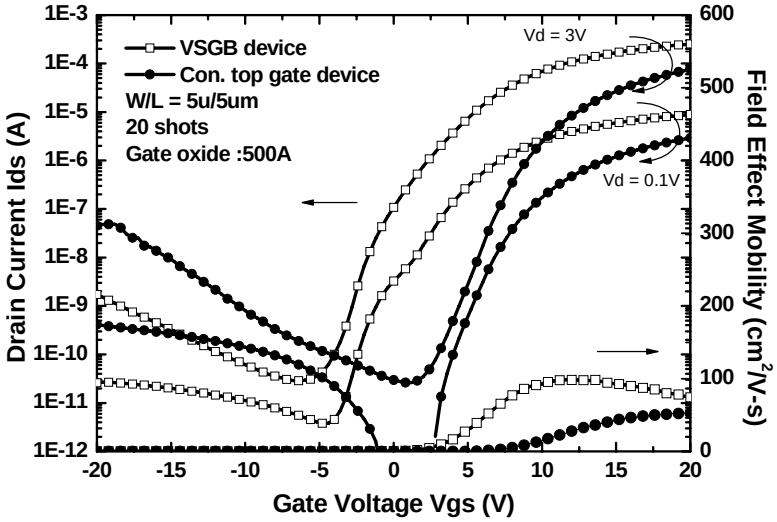


Fig. 3-47 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 5 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

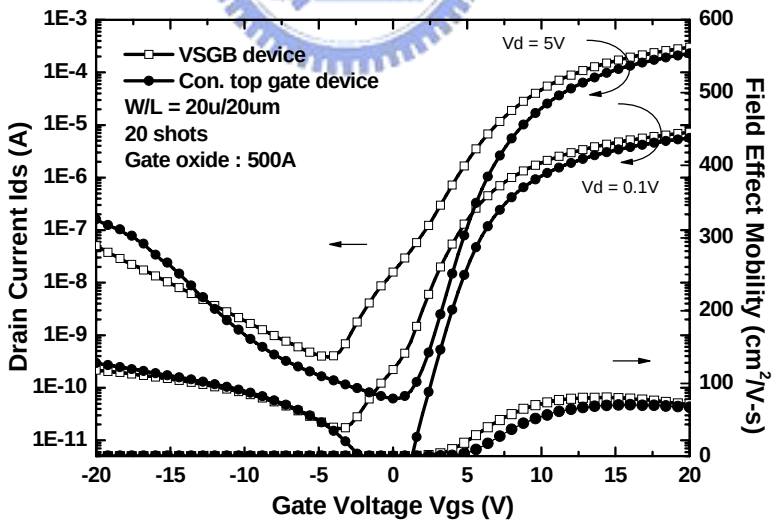


Fig. 3-48 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 20 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

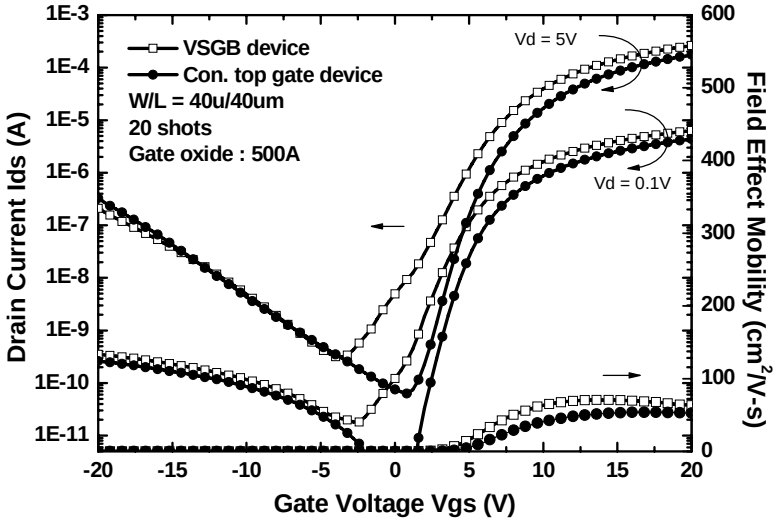


Fig. 3-49 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 40 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

20 shots Gate oxide: 500 Å	Mobility (cm^2/V-s)	Sub-threshold swing (V/dec)	Vth (V)	on/off current ratio at Vds = 3 V
conventional top gate LTPS-TFT (W/L= 1.2/1.2um)	79.865	0.478	1.247	3.06E+07
VSGB-LTPS-TFT (W/L= 1.2/1.2um)	201.822	0.464	-0.604	4.33E+07
conventional top gate LTPS-TFT (W/L= 1.5/1.5um)	78.380	0.527	1.840	3.73E+07
VSGB-LTPS-TFT (W/L= 1.5/1.5um)	175.784	0.476	-0.367	7.77E+07
conventional top gate LTPS-TFT (W/L= 2/2um)	69.511	0.861	3.520	8.63E+07
VSGB-LTPS-TFT (W/L= 2/2um)	141.230	0.956	0.108	1.24E+07

Table 3. 4 Measured optimal electrical characteristics of TFTs crystallized with VSGB-LTPS structure and conventional structure in short channel devices. The thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

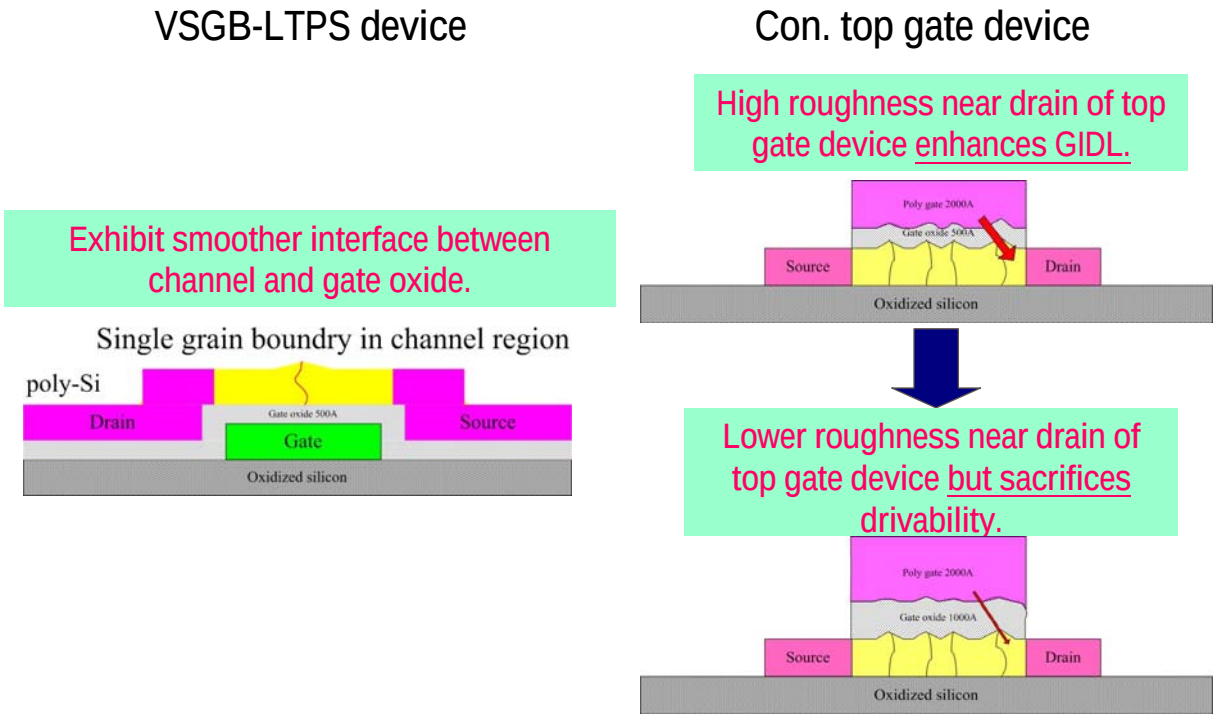


Fig. 3-50 Mechanism of the higher GIDL in conventional top-gate device.

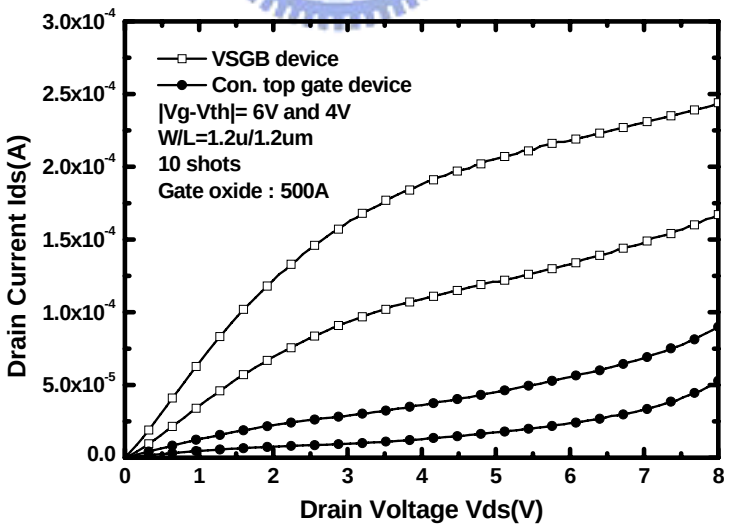


Fig. 3-51 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

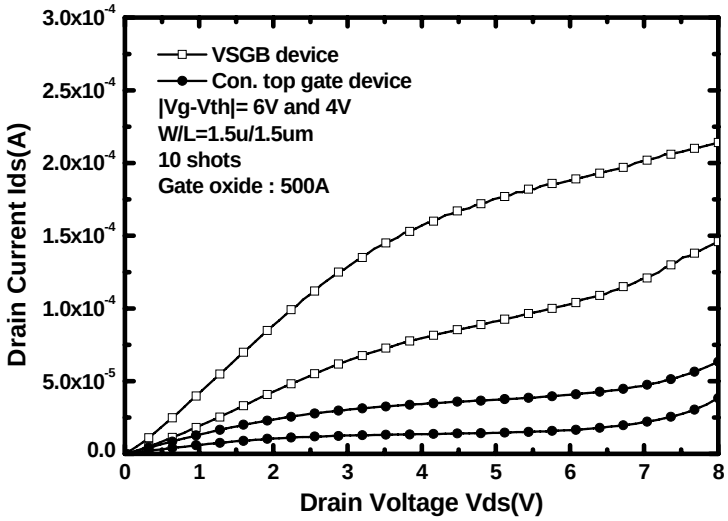


Fig. 3-52 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

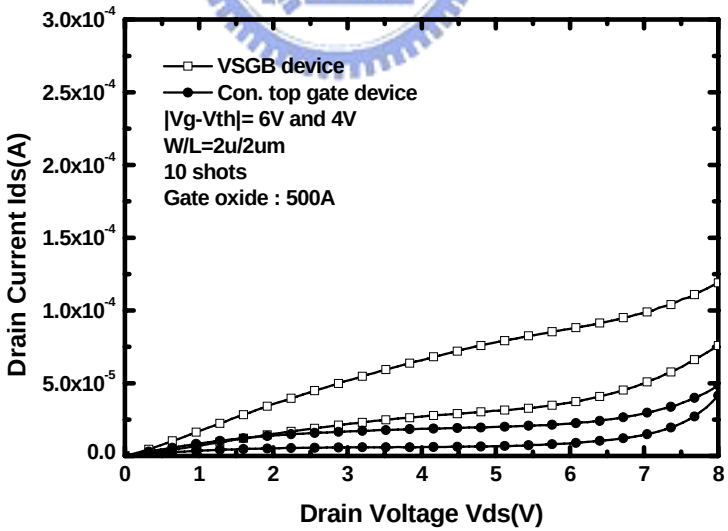


Fig. 3-53 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 2 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

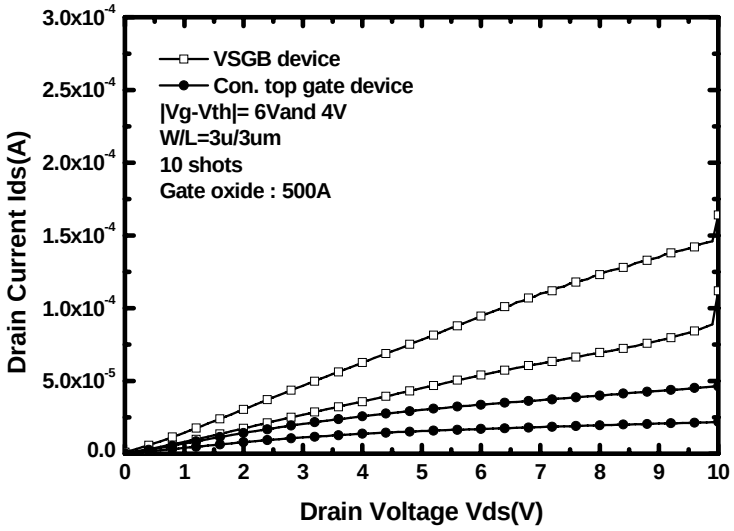


Fig. 3-54 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 3 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

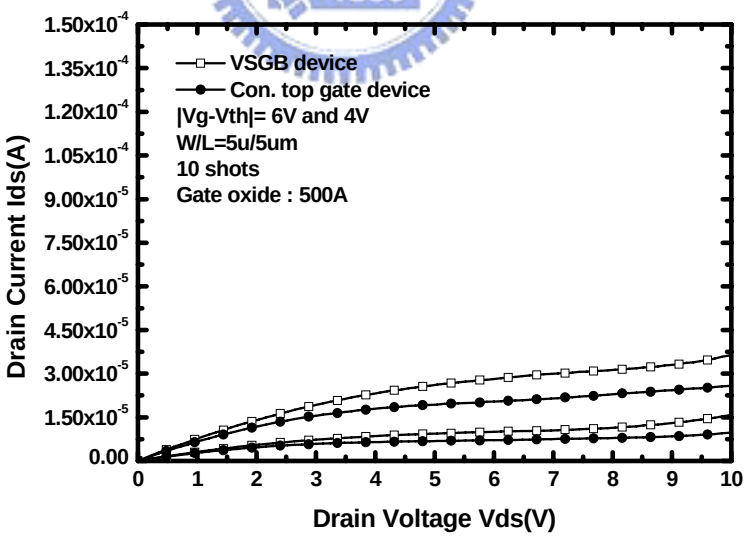


Fig. 3-55 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 5 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

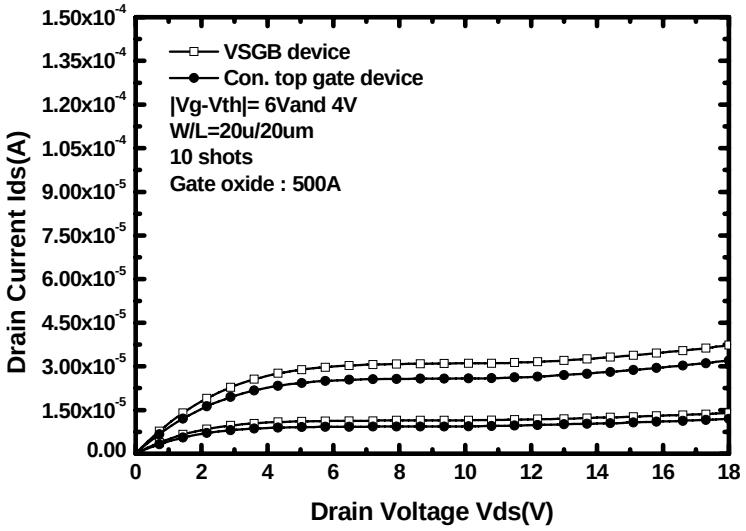


Fig. 3-56 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 20 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

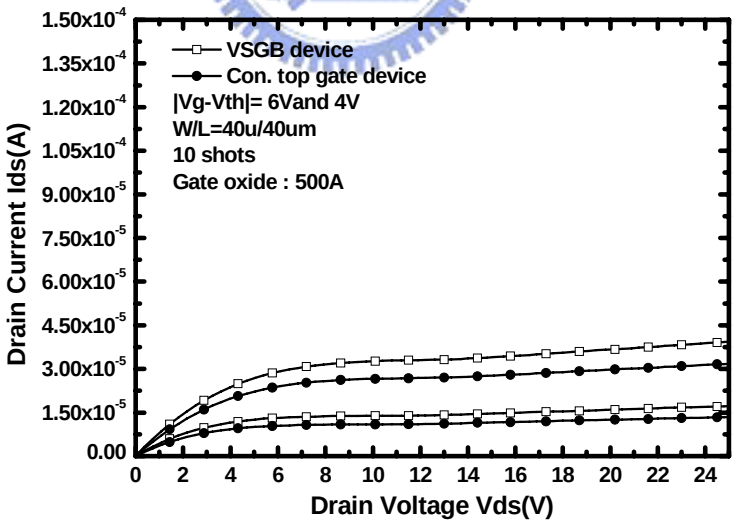


Fig. 3-57 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 40 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

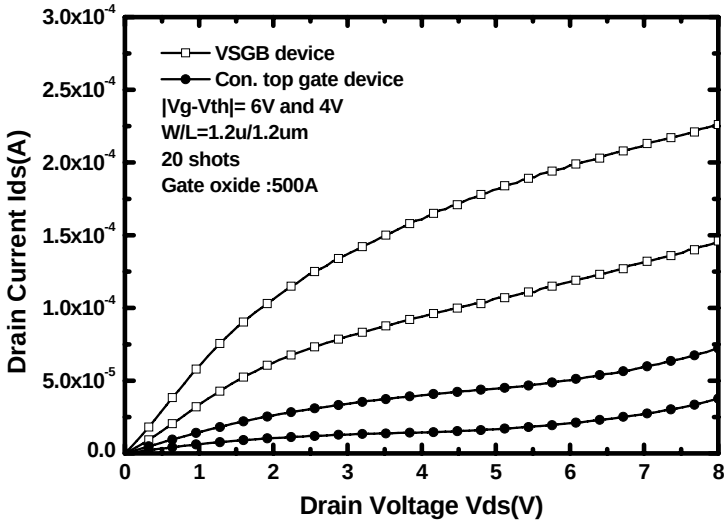


Fig. 3-58 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

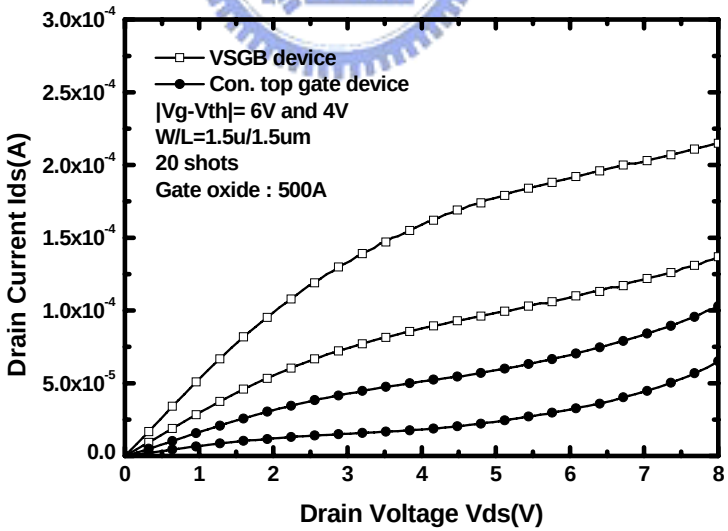


Fig. 3-59 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

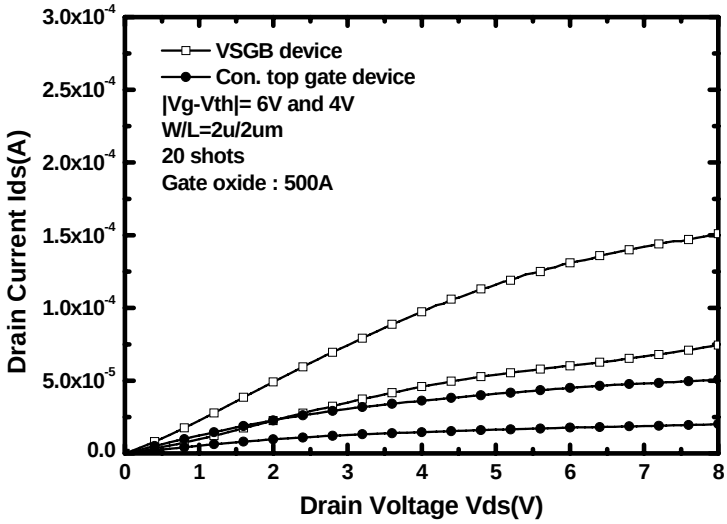


Fig. 3-60 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 2 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

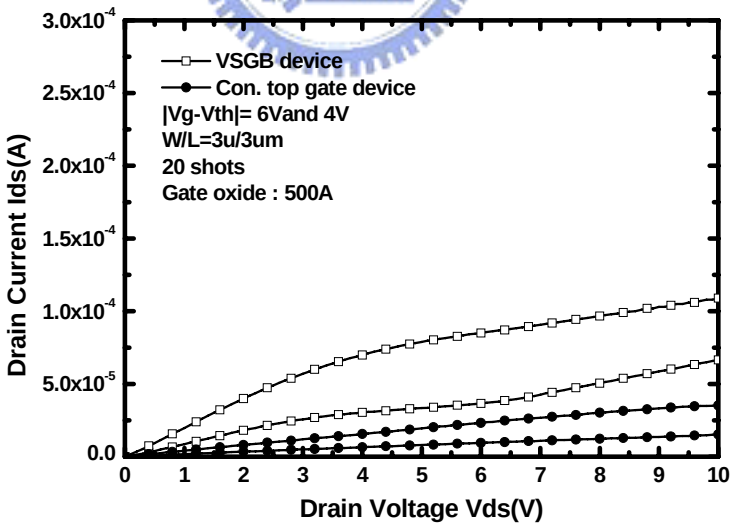


Fig. 3-61 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 3 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping)

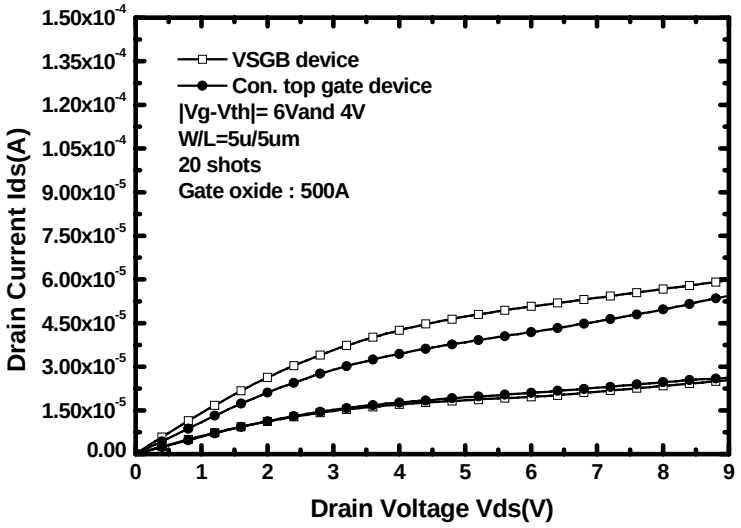


Fig. 3-62 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 5 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping)

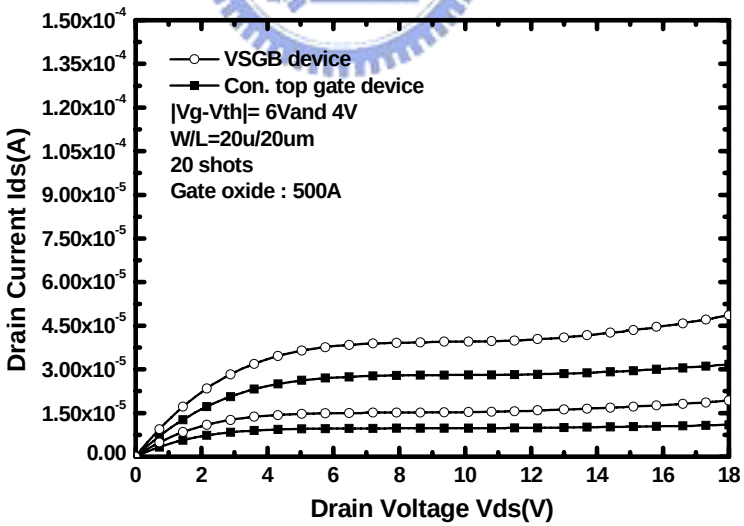


Fig. 3-63 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 20 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping)

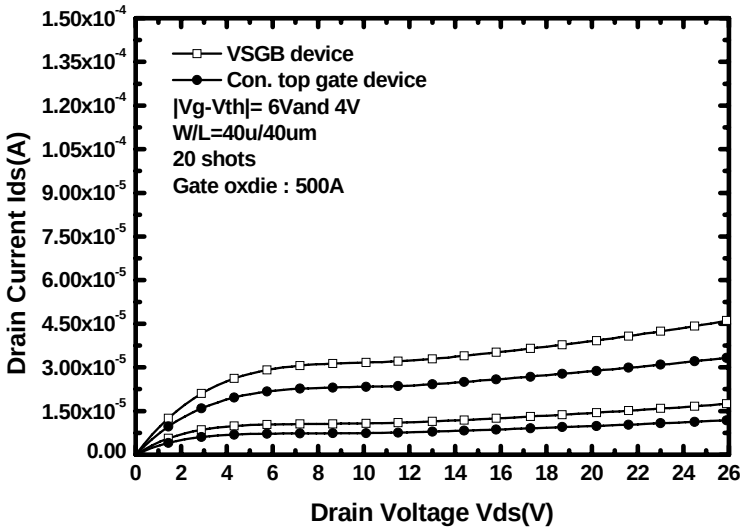


Fig. 3-64 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 40 μm, in which the thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping)

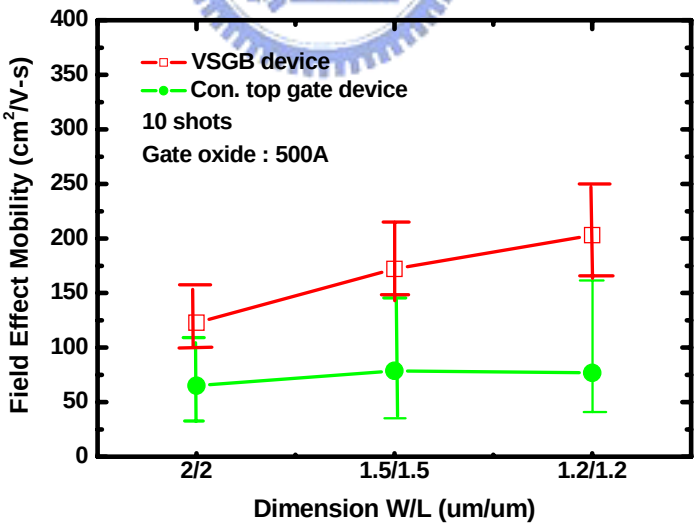


Fig. 3-65 The dependence of field-effect mobility on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

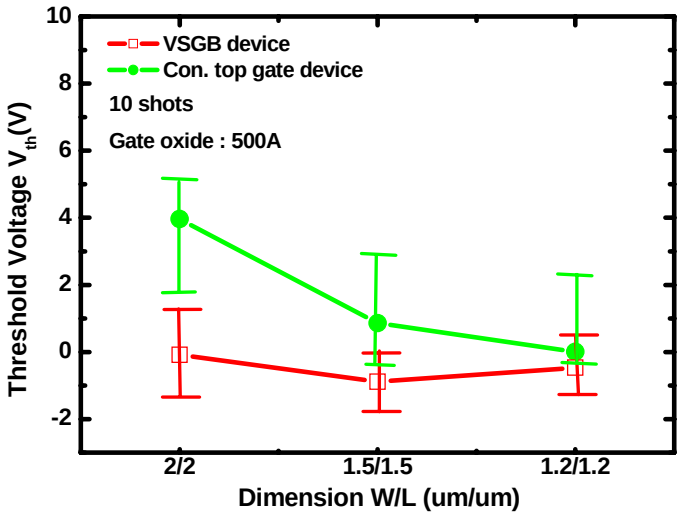


Fig. 3-66 The dependence of threshold voltage on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping)

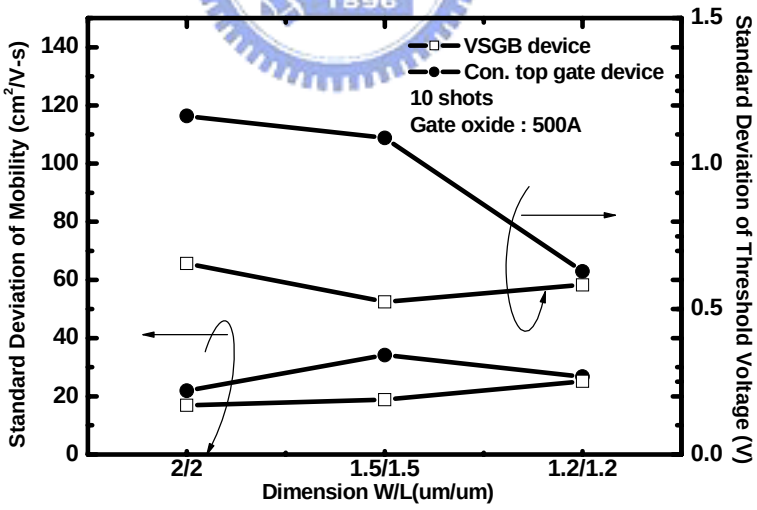


Fig. 3-67 The dependences of standard deviation of field-effect mobility and threshold voltage on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 500Å. The number of laser shots was 10(ie. 90% overlapping).

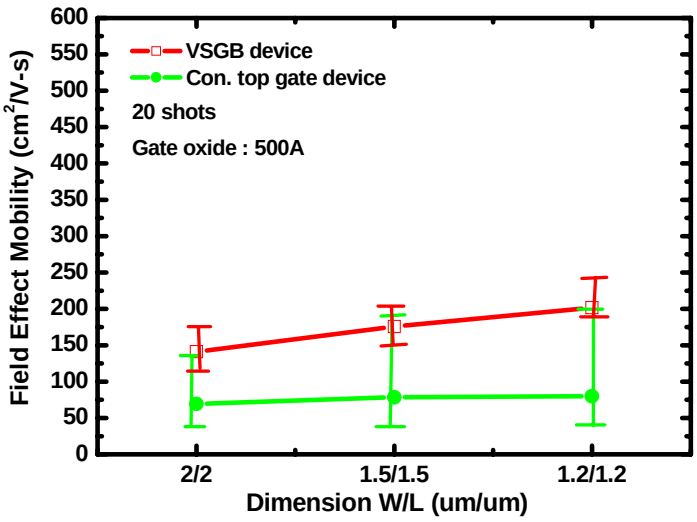


Fig. 3-68 The dependence of field-effect mobility on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

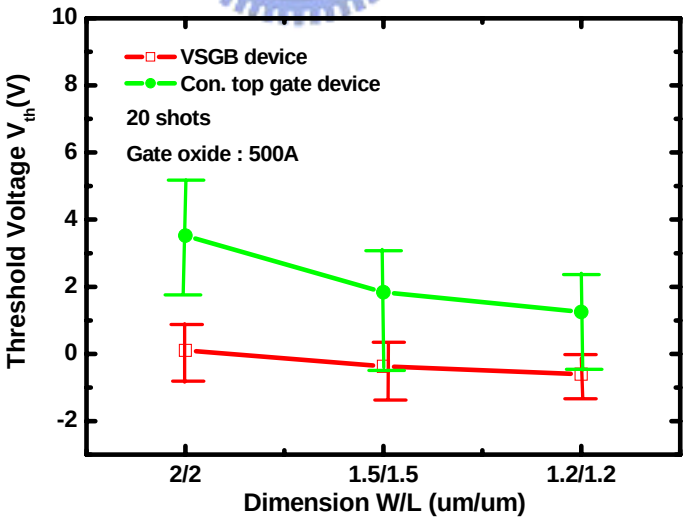


Fig. 3-69 The dependence of threshold voltage on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

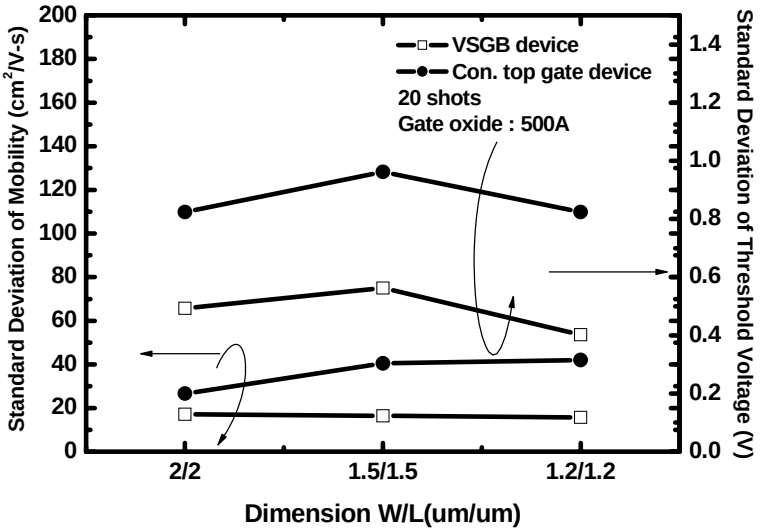


Fig. 3-70 The dependences of standard deviation of field-effect mobility and threshold voltage on the channel length of LTPS TFTs crystallized with VSGB-LTPS and conventional top-gate structures. The thickness of gate oxide was 500Å. The number of laser shots was 20(ie. 95% overlapping).

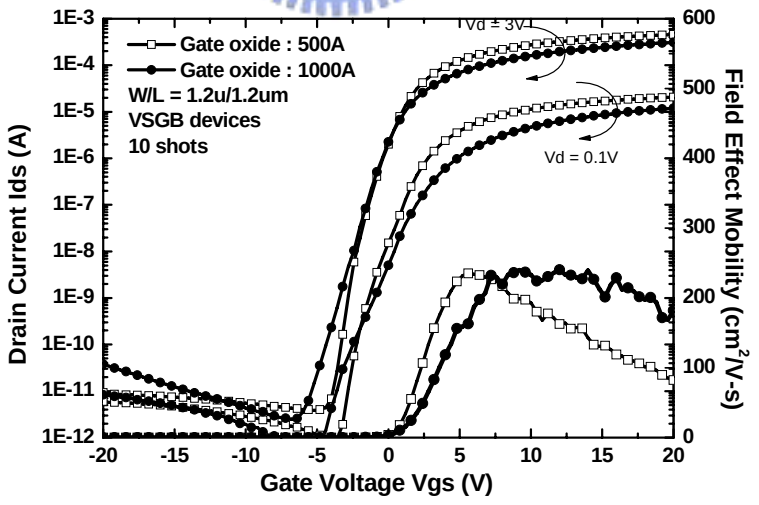


Fig. 3-71 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS TFTs structure with channel length of 1.2 μm, in which the thickness of gate oxide was 500 Å and 1000Å. The number of laser shots was 10(ie. 90% overlapping).

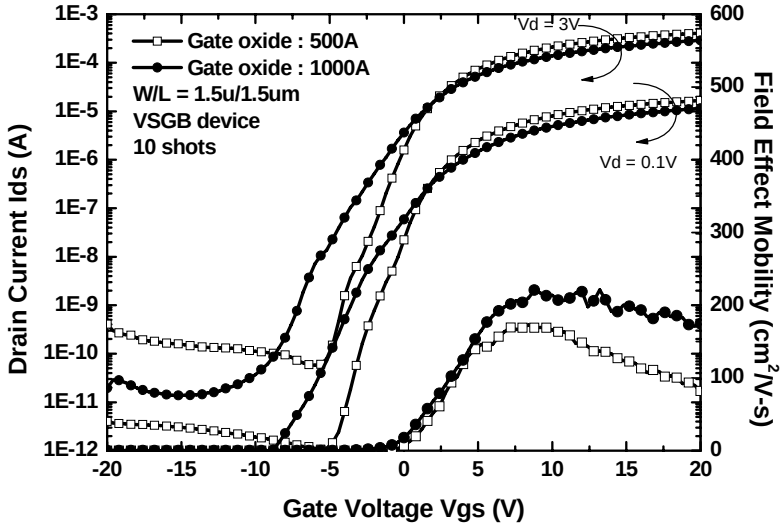


Fig. 3-72 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS TFTs structure with channel length of 1.5 μm, in which the thickness of gate oxide was 500 Å and 1000Å. The number of laser shots was 10(ie. 90% overlapping).

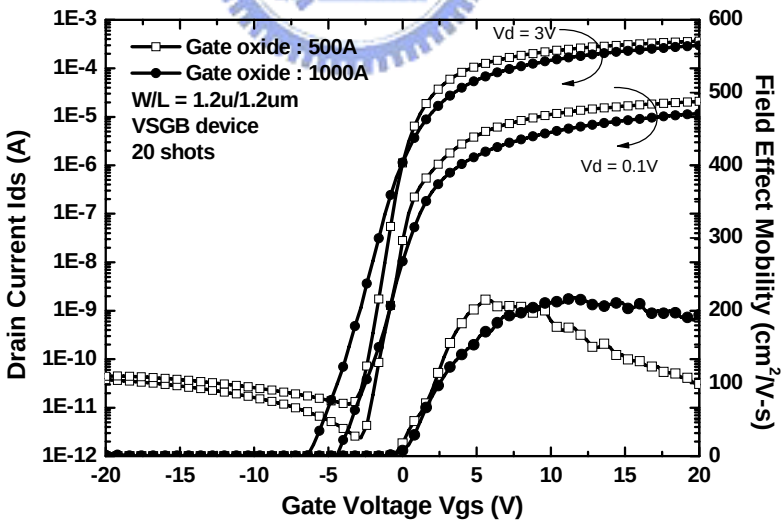


Fig. 3-73 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS TFTs structure with channel length of 1.2 μm, in which the thickness of gate oxide was 500 Å and 1000Å. The number of laser shots was 20(ie. 95% overlapping).

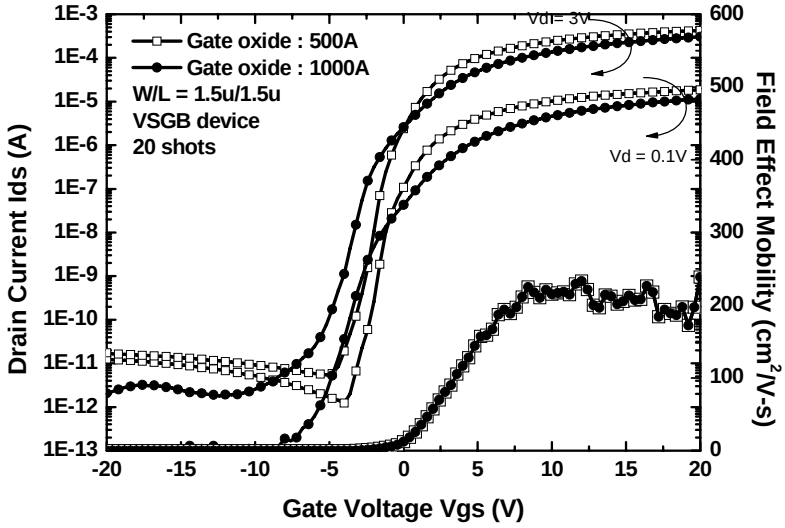


Fig. 3-74 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS TFTs structure with channel length of 1.5 μm, in which the thickness of gate oxide was 500 Å and 1000Å. The number of laser shots was 20(ie. 95% overlapping).

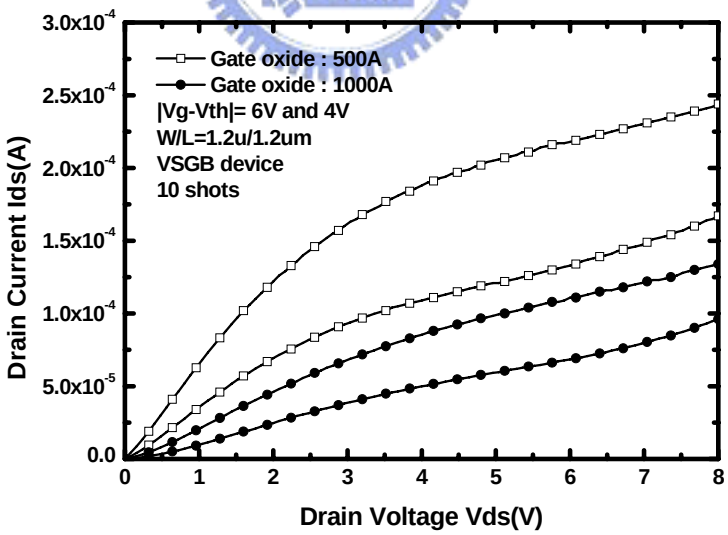


Fig. 3-75 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS TFTs structure with channel length of 1.2 μm, in which the thickness of gate oxide was 500 Å and 1000Å. The number of laser shots was 10(ie. 90% overlapping).

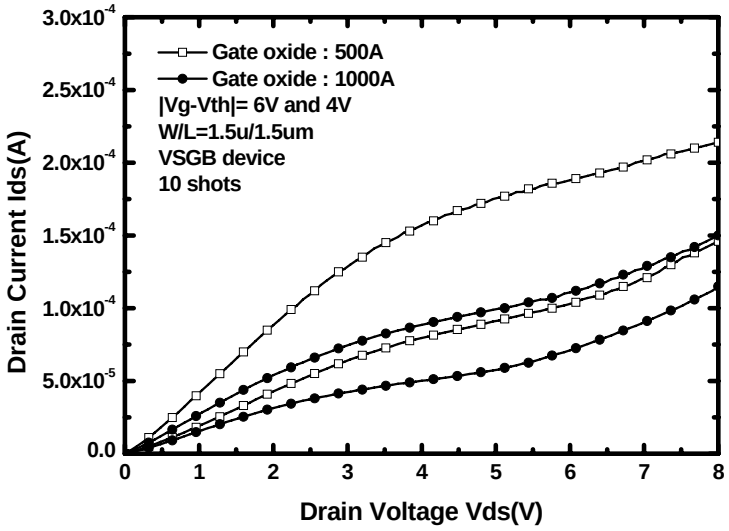


Fig. 3-76 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 500 Å and 1000Å. The number of laser shots was 10(ie. 90% overlapping).

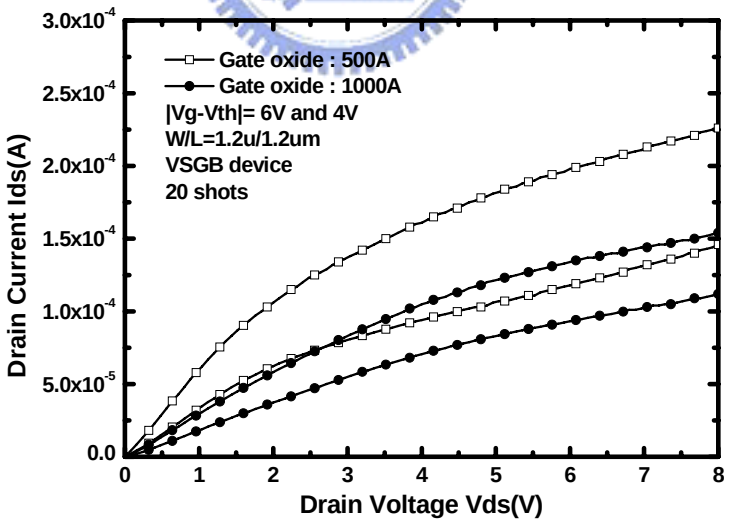


Fig. 3-77 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 500 Å and 1000Å. The number of laser shots was 20(ie. 95% overlapping).

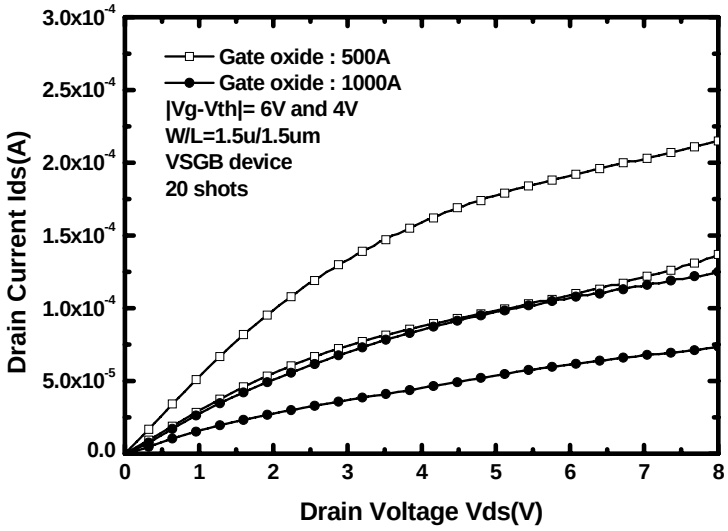


Fig. 3-78 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 500 Å and 1000Å. The number of laser shots was 20(ie. 95% overlapping).

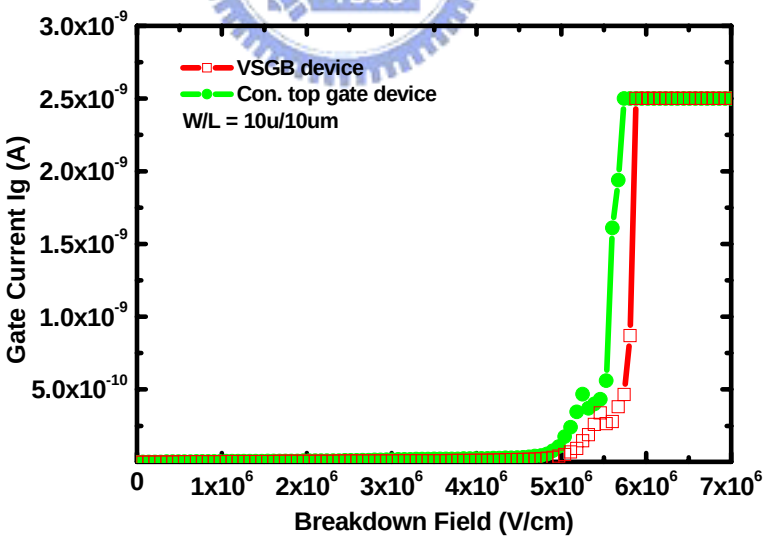


Fig. 3-79 The breakdown field of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure and conventional top gate structure. The thickness of gate oxide was 1000Å.

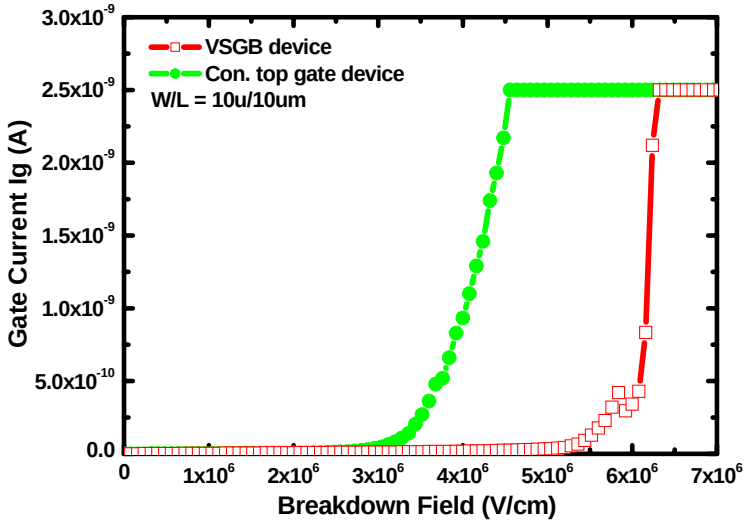


Fig. 3-80 The breakdown field of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure and conventional top gate structure. The thickness of gate oxide was 500Å.

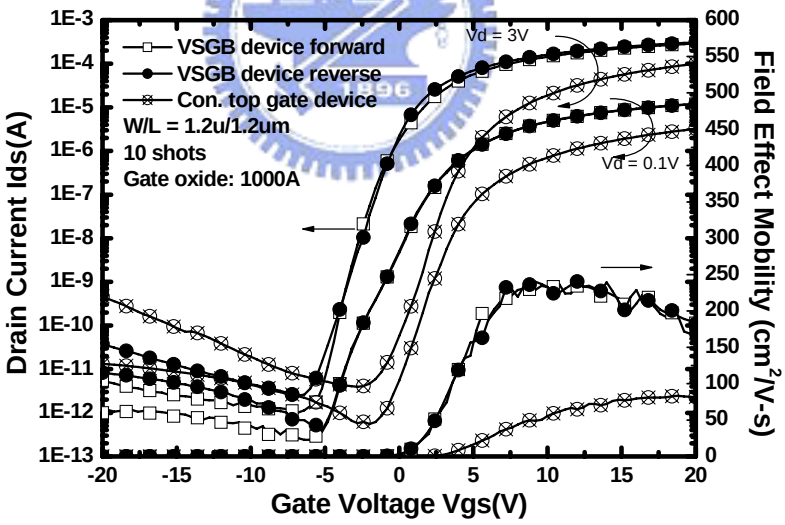


Fig. 3-81 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping). The roles of source and drain were changed for forward and reverse measurements.

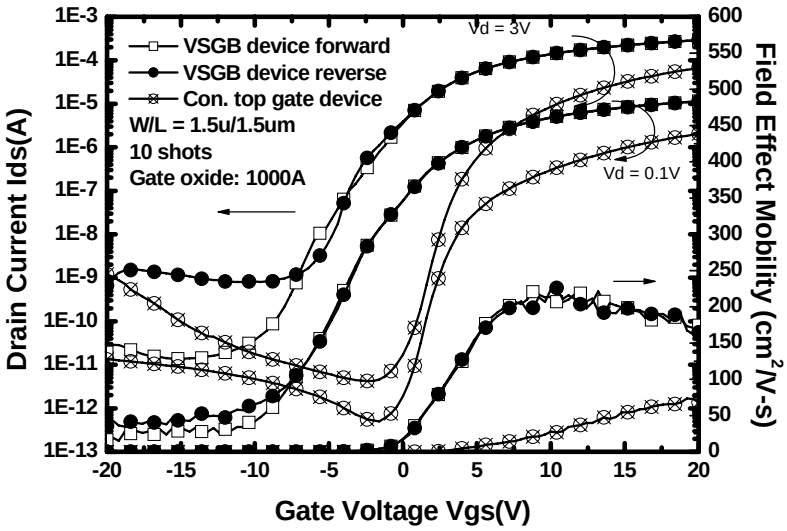


Fig. 3-82 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10(ie. 90% overlapping). The roles of source and drain were changed for forward and reverse measurements.

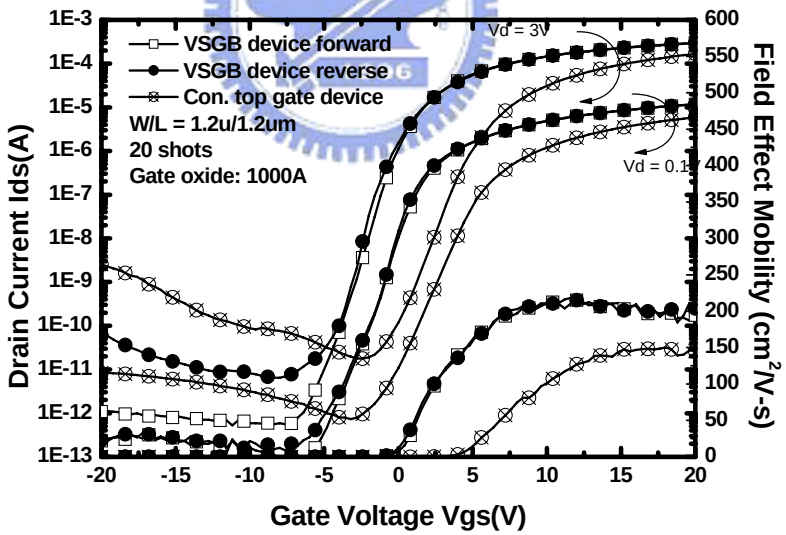


Fig. 3-83 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS TFTs structure with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping). The roles of source and drain were changed for forward and reverse measurements.

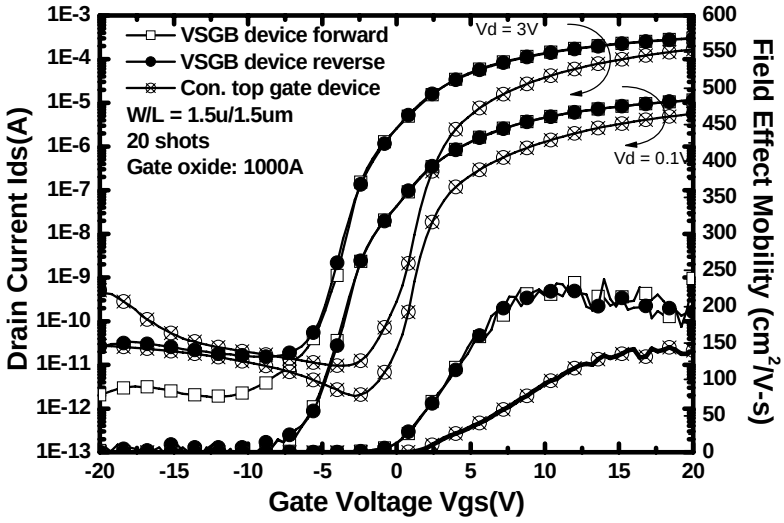


Fig. 3-84 The typical transfer characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping). The roles of source and drain were changed for forward and reverse measurements.

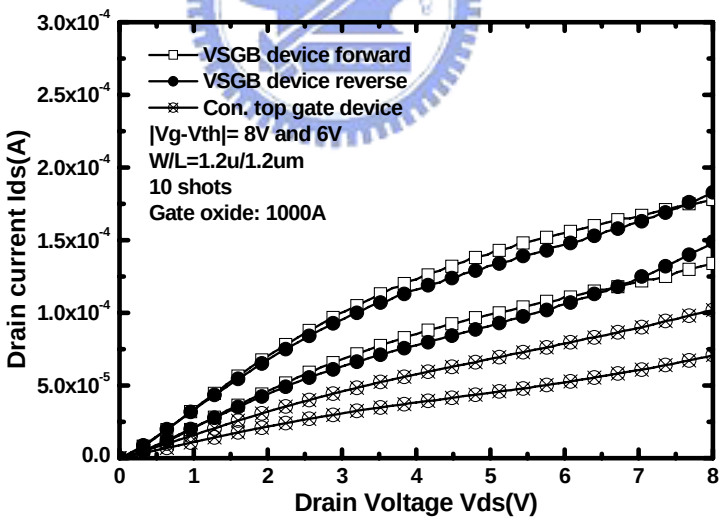


Fig. 3-85 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping). The roles of source and drain were changed for forward and reverse measurements.

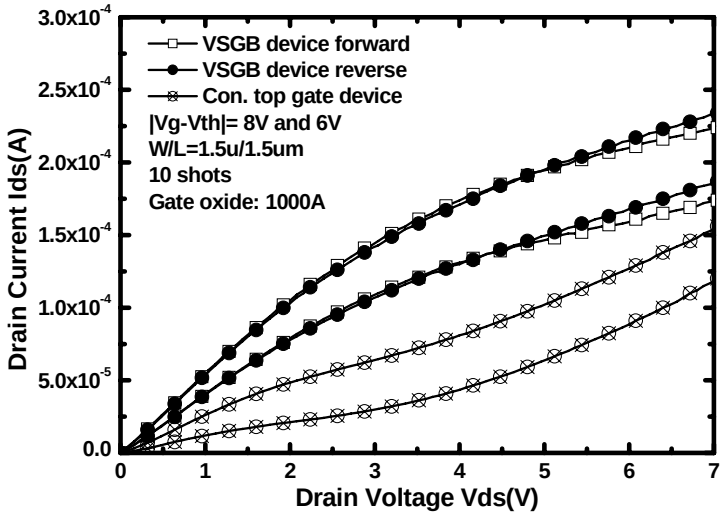


Fig. 3-86 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 10 (ie. 90% overlapping). The roles of source and drain were changed for forward and reverse measurements.

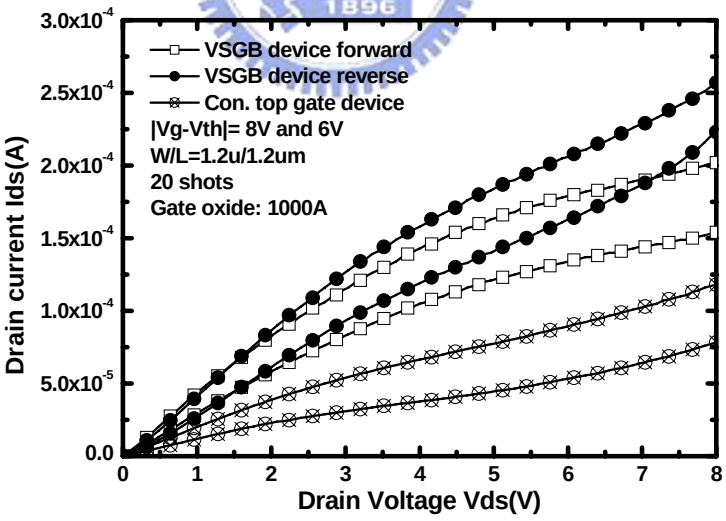


Fig. 3-87 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.2 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping). The roles of source and drain were changed for forward and reverse measurements.

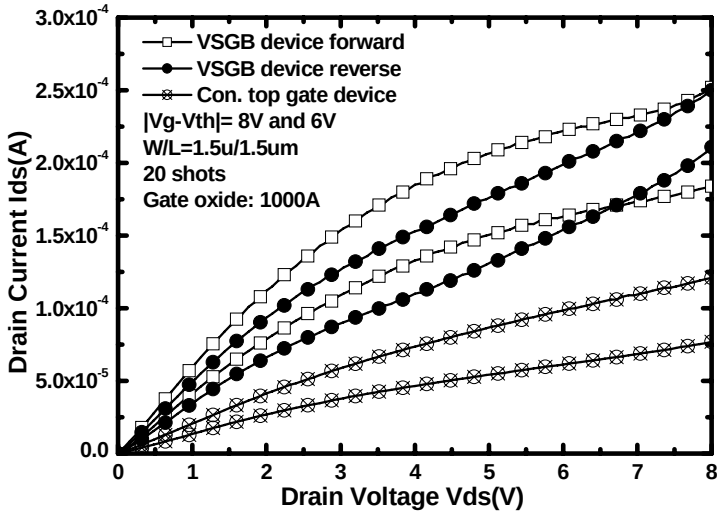


Fig. 3-88 The output characteristic of polycrystalline silicon TFTs crystallized using VSGB-LTPS structure with channel length of 1.5 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20 (ie. 95% overlapping). The roles of source and drain were changed for forward and reverse measurements.

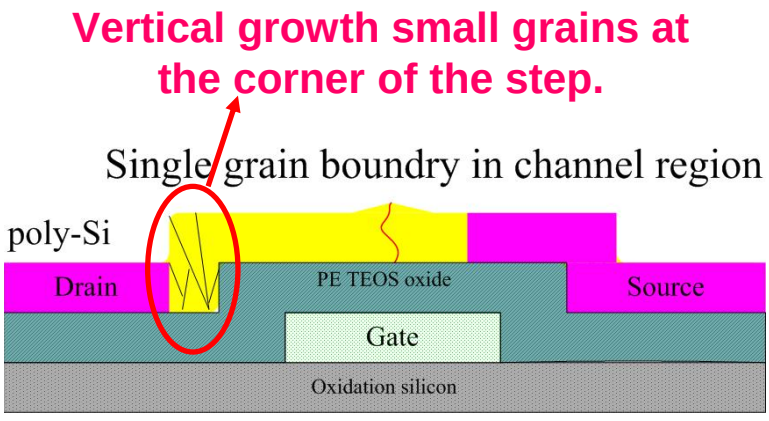


Fig. 3-89 The mis-aligned ion implantation of source and drain.

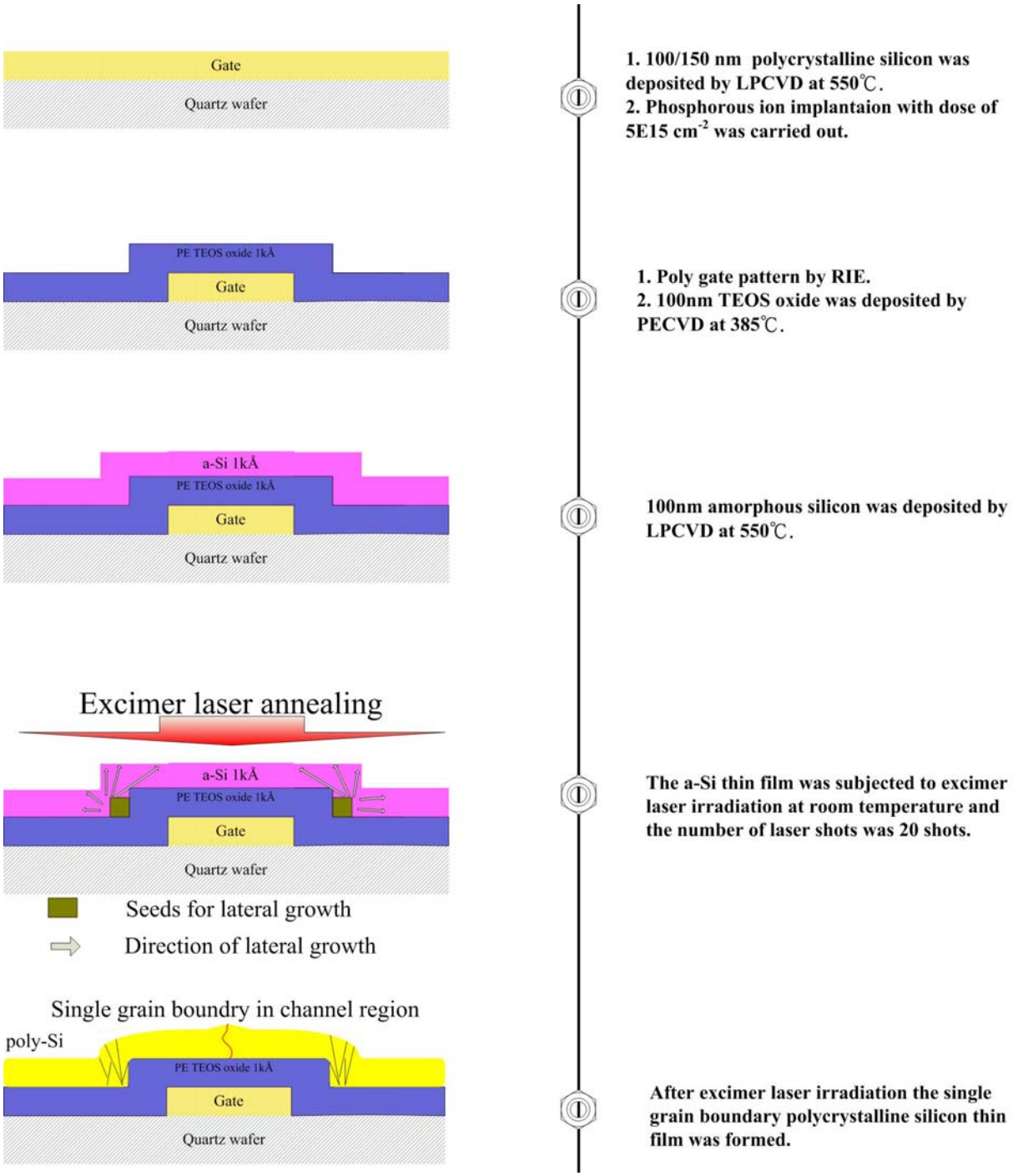


Fig. 4-1 The key processes for fabrication of SA-VSGB-LTPS-TFTs (I)

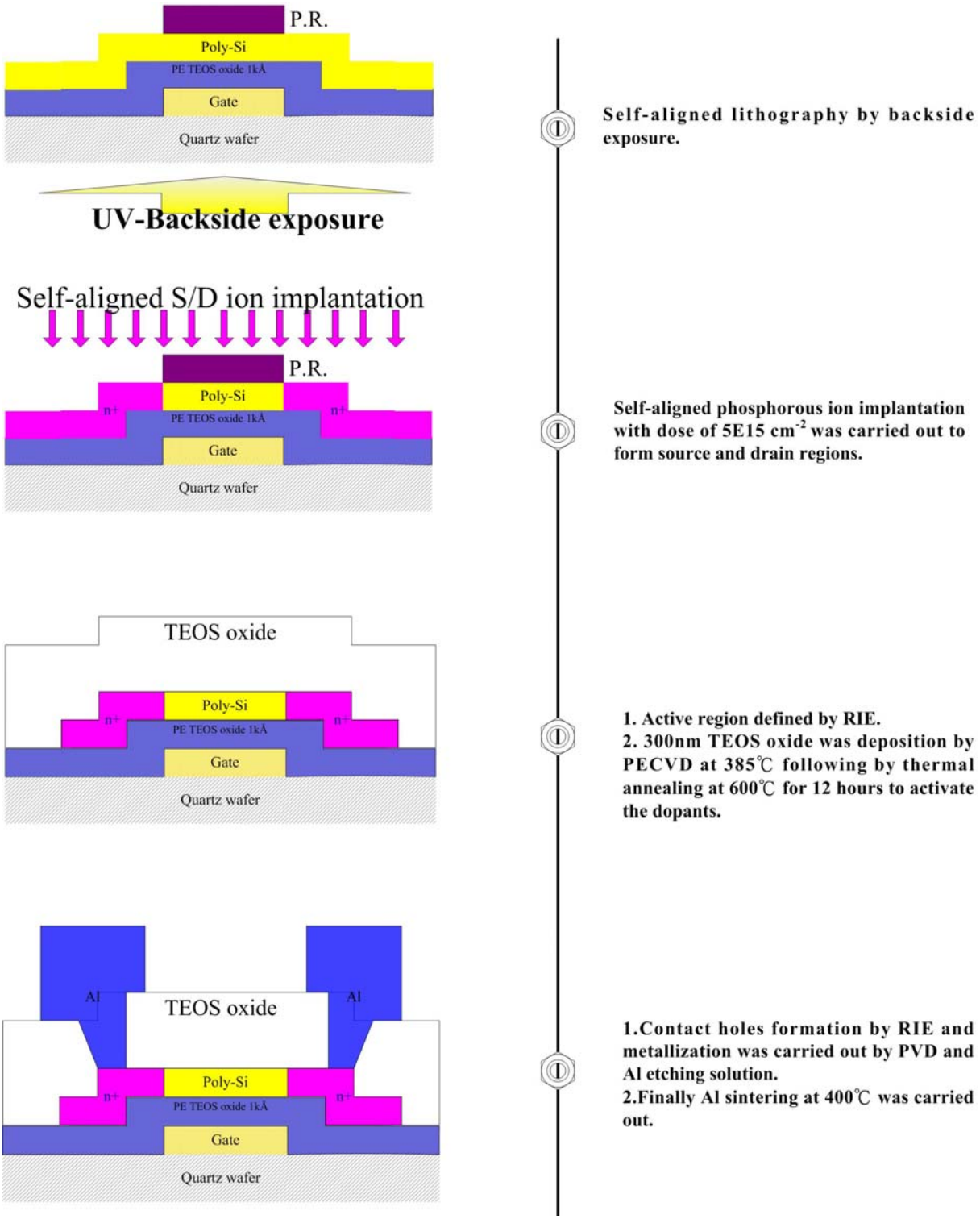


Fig. 4-1 The key processes for fabrication of SA-VSGB-LTPS-TFTs (II)

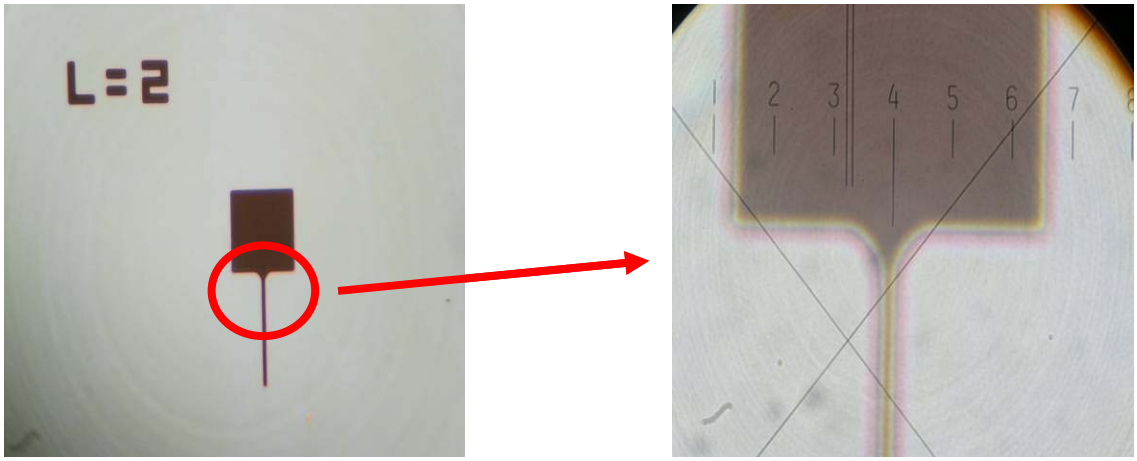


Fig. 4-2 OM images of self-aligned implantation devices from transparent light source. The channel length was 2μm.

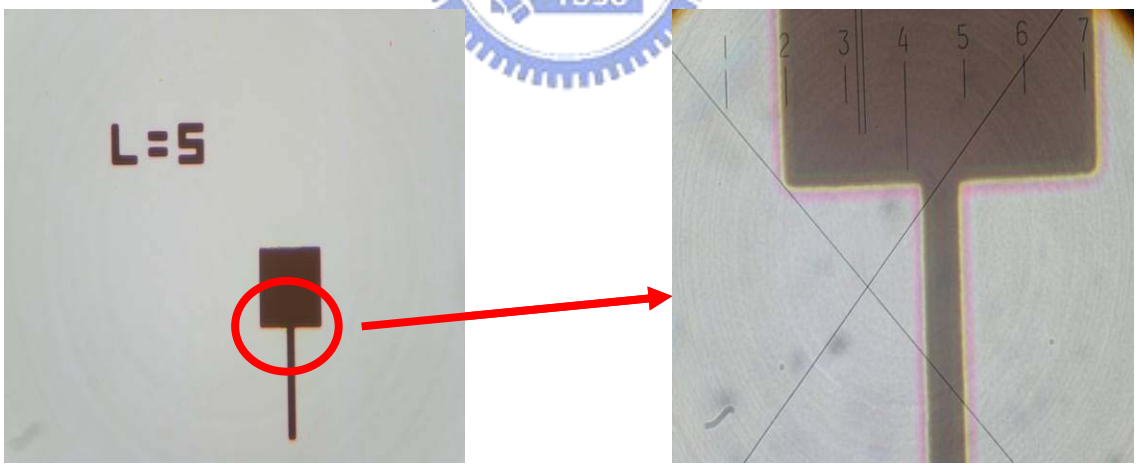


Fig. 4-3 OM images of self-aligned implantation devices from transparent light source The channel length was 5μm.

Fig. 4-4 OM images of mis-aligned implantation devices after lithography. The channel length was 2μm.

Fig. 4-5 OM images of self-aligned implantation devices after lithography. The channel length was 2μm.

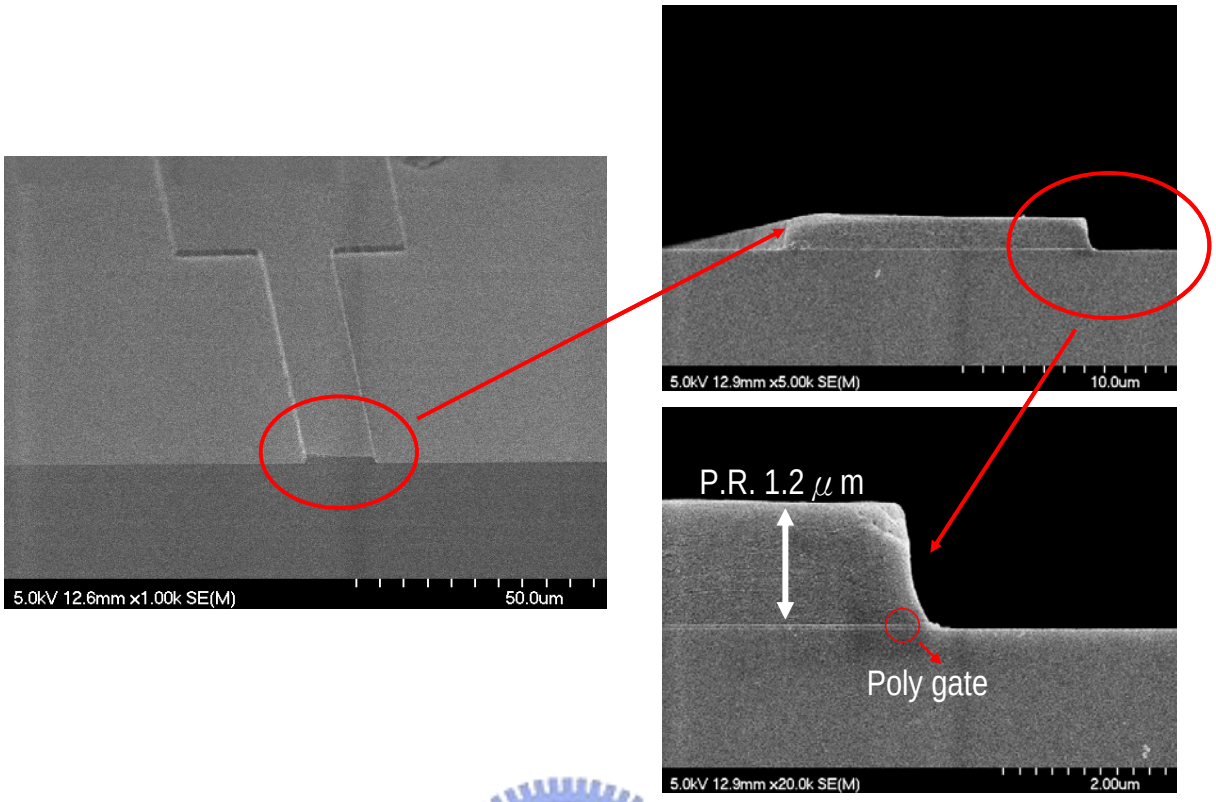


Fig. 4-6 SEM graphs of self-aligned implantation devices after lithography.

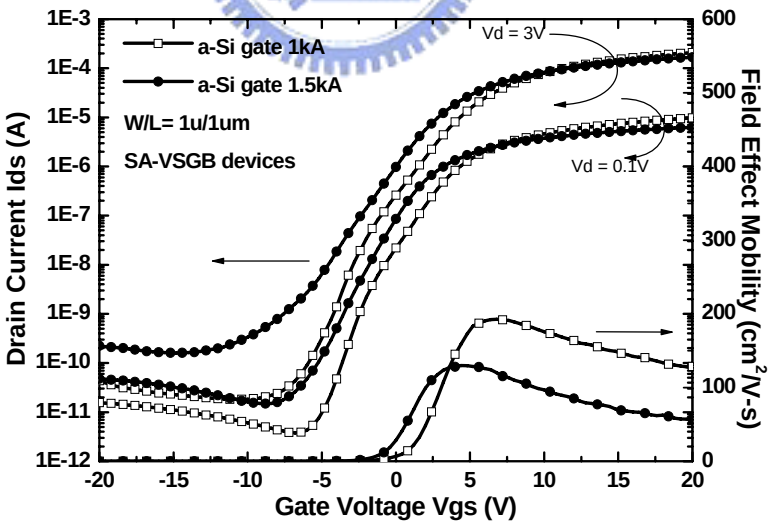


Fig. 4-7 The typical transfer characteristic of SA-VSGB-LTPS TFTs with amorphous gate thickness of 1000Å and 1500Å. The number of laser shots was 20 (ie. 95% overlapping).

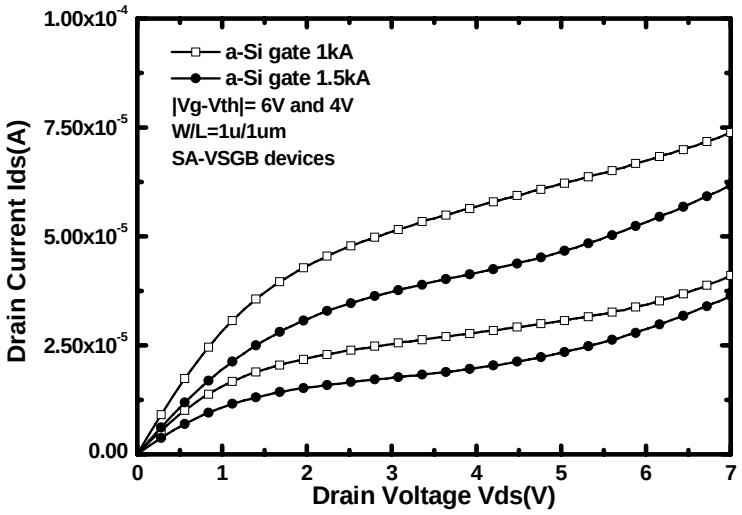


Fig. 4-8 The output characteristic of SA-VSGB-LTPS TFTs with amorphous gate thickness of 1000Å and 1500Å. The number of laser shots was 20 (ie. 95% overlapping).

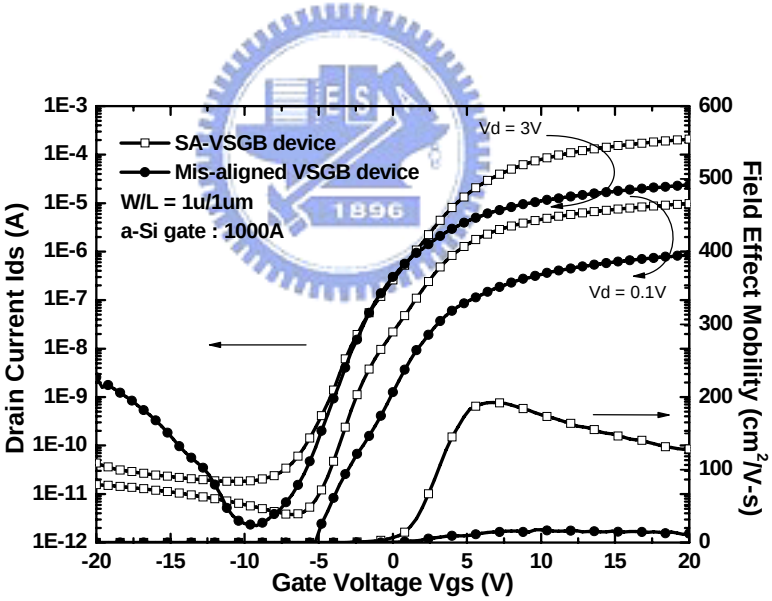


Fig. 4-9 The typical transfer characteristic of SA-VSGB-LTPS TFTs with amorphous gate thickness of 1000Å. The channel length was 1μm. The number of laser shots was 20 (ie. 95% overlapping).

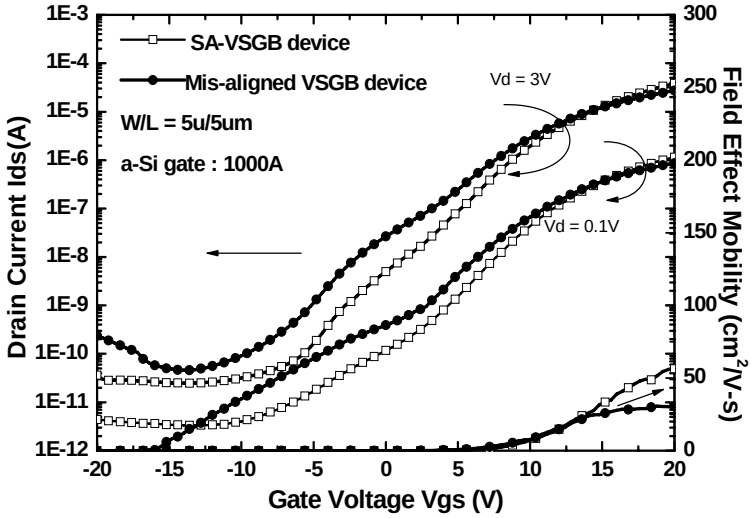


Fig. 4-10 The typical transfer characteristic of SA-VSGB-LTPS TFTs with amorphous gate thickness of 1000Å. The channel length was 5μm. The number of laser shots was 20 (ie. 95% overlapping).

Laser shots: 20 shots Gate oxide: 1000 Å Poly gate: 1000 Å	Mobility (cm^2/V-s)	Sub-threshold swing SS (V/dec)	Threshold voltage Vth (V)	on/off current ratio
Self-aligned (W/L =1 μm/1 μm)	192.546	1.197	-0.768	1.14E+07
Mis-aligned (W/L =1 μm/1 μm)	17.767	1.247	1.679	1.07E+07
Self-aligned (W/L =5 μm/5 μm)	56.405	3.129	7.603	1.55E+06
Mis-aligned (W/L =5 μm/5 μm)	30.667	3.122	6.385	5.93E+05

Table 4. 1 Measured optimal electrical characteristics of SA-VSGB-LTPS TFTs and mis-aligned VSGB-LTPS TFTs. The number of laser shots was 20(ie. 95% overlapping).

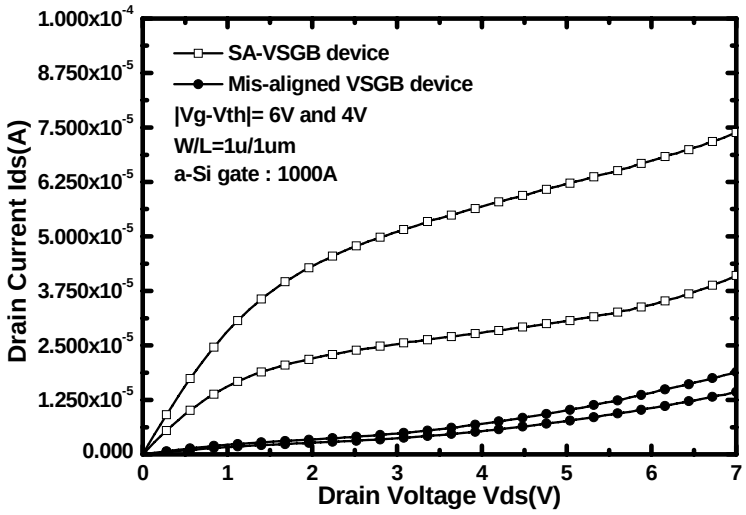


Fig. 4-11 The output characteristic of SA-VSGB-LTPS TFTs with amorphous gate thickness of 1000Å. The channel length was 1μm. The number of laser shots was 20 (ie. 95% overlapping).

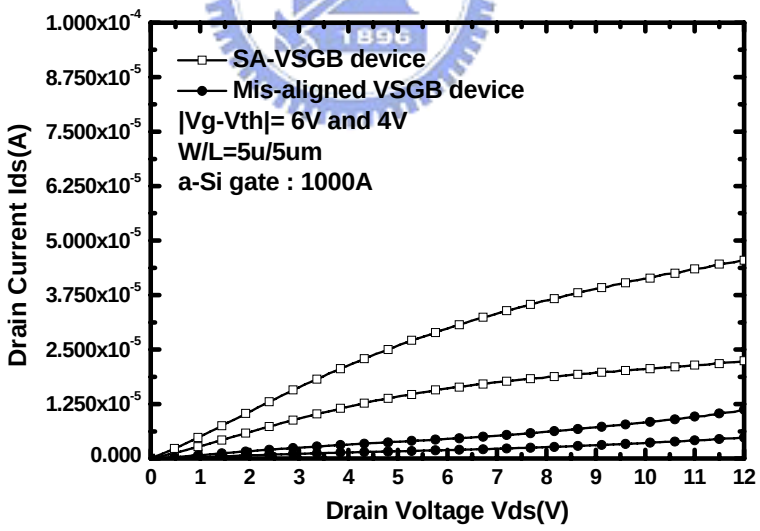


Fig. 4-12 The output characteristic of SA-VSGB-LTPS TFTs with amorphous gate thickness of 1000Å. The channel length was 5μm. The number of laser shots was 20 (ie. 95% overlapping).

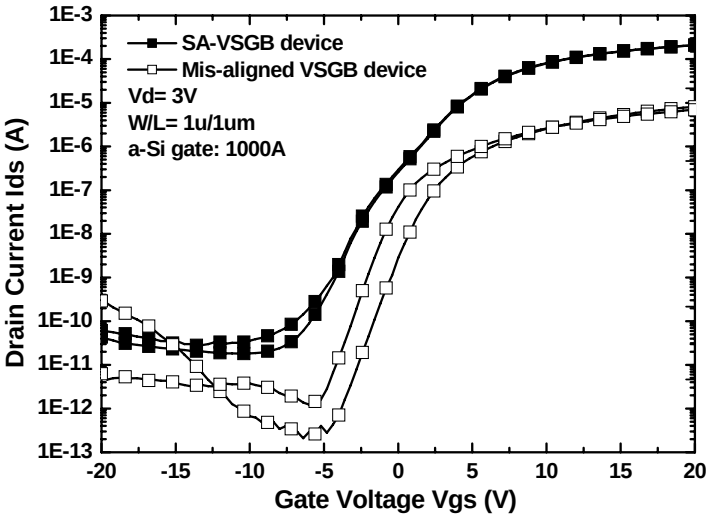


Fig. 4-13 The typical transfer characteristic of SA-VSGB-LTPS TFTs with channel length of 1 μm, in which the thickness of gate oxide was 1000Å. The number of laser shots was 20(ie. 95% overlapping). The roles of source and drain were changed for forward and reverse measurements.

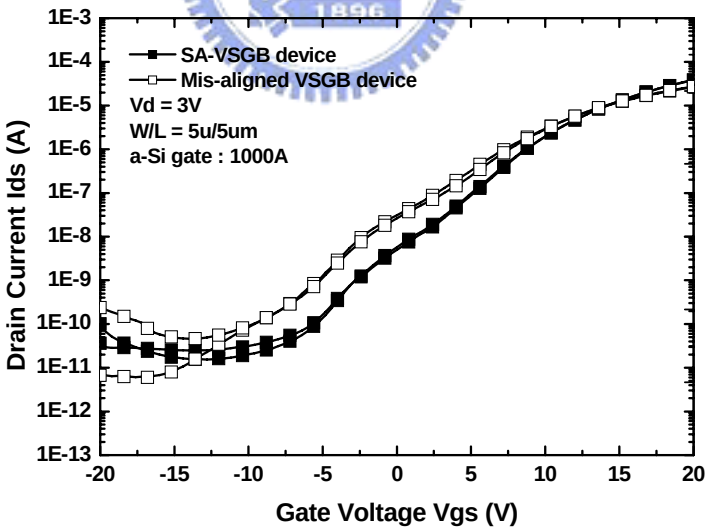


Fig. 4-14 The typical transfer characteristic of SA-VSGB-LTPS TFTs with channel length of 5 μm. The number of laser shots was 20(ie. 95% overlapping). The roles of source and drain were changed for forward and reverse measurements.

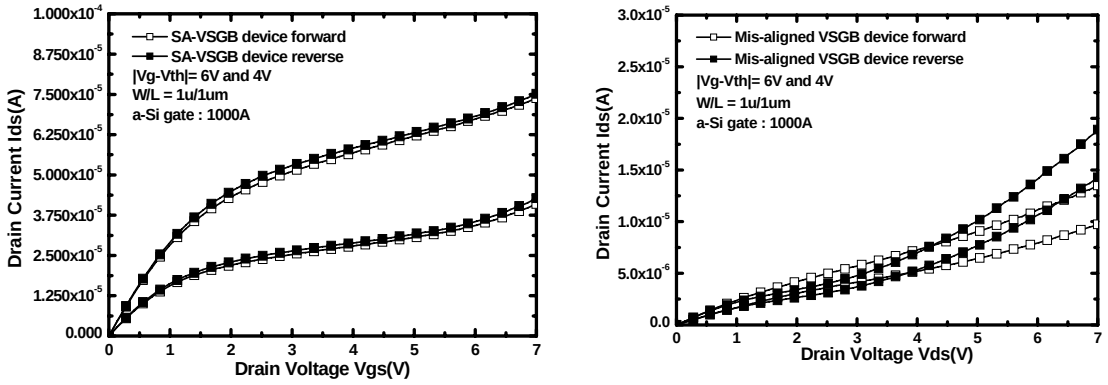


Fig. 4-15 The output characteristic of SA-VSGB-LTPS TFTs (left) and mis-aligned VSGB-LTPS-TFTs (right) with channel length of 1 μm. The number of laser shots was 20(ie. 95% overlapping). The roles of source and drain were changed for forward and reverse measurements.

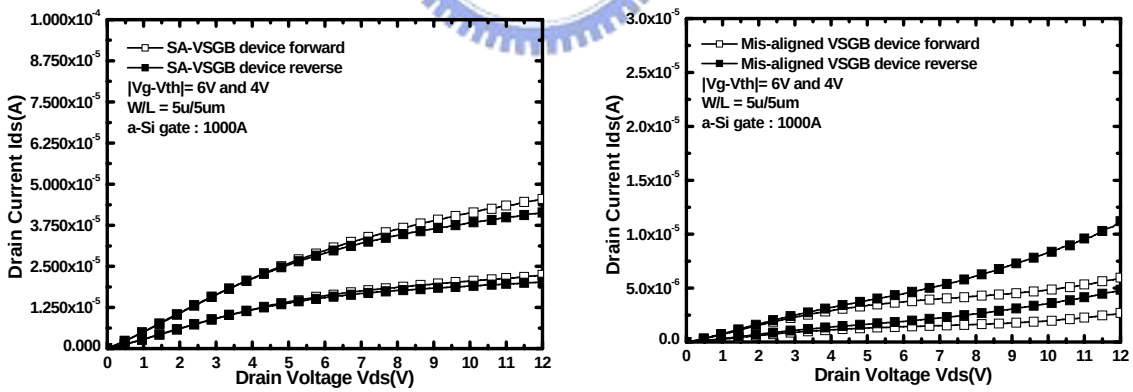


Fig. 4-16 The output characteristic of SA-VSGB-LTPS TFTs (left) and mis-aligned VSGB-LTPS-TFTs (right) with channel length of 5 μm. The number of laser shots was 20(ie. 95% overlapping). The roles of source and drain were changed for forward and reverse measurements.

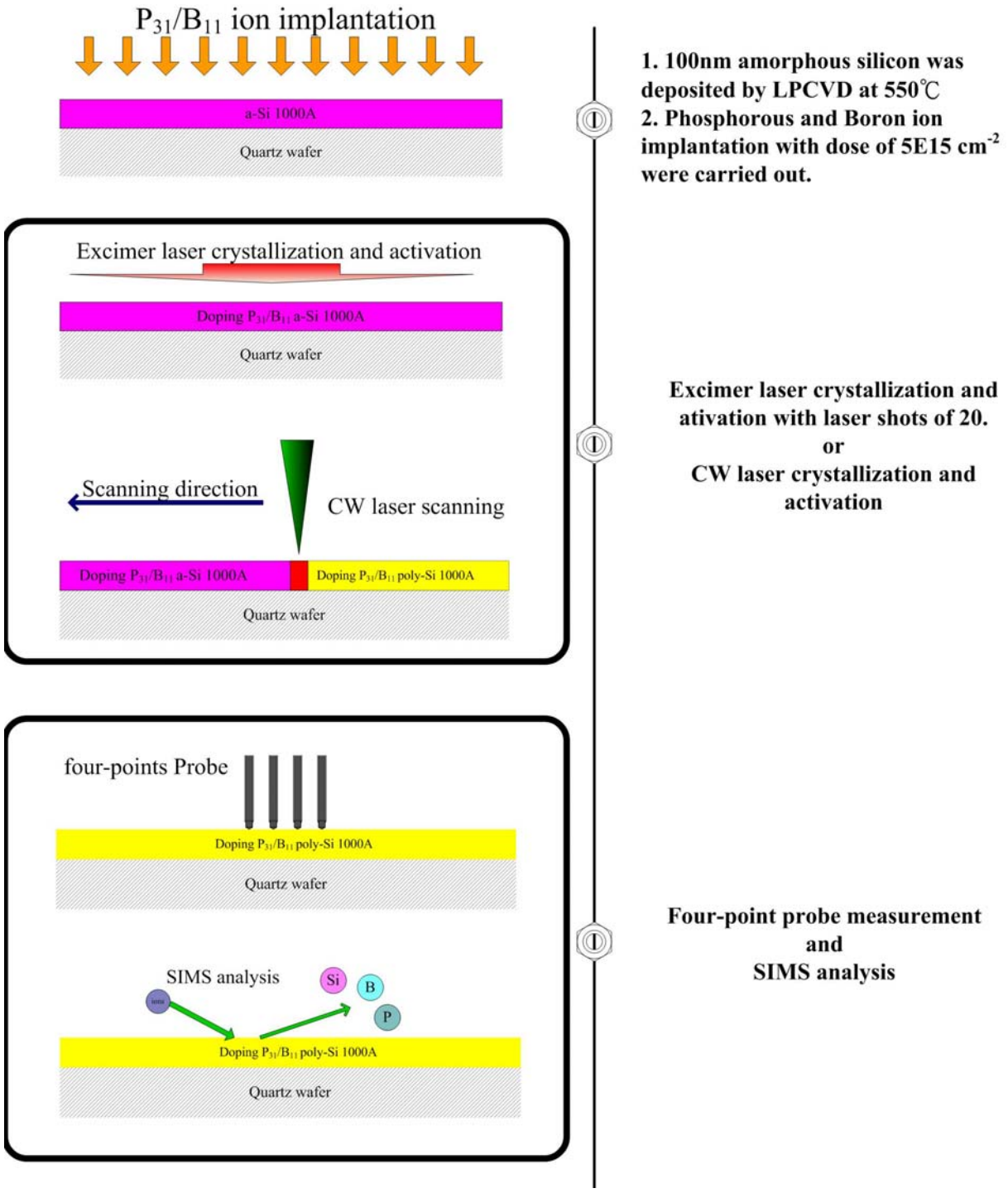


Fig. 5-1 Process flows of dopant activation by CW laser annealing.

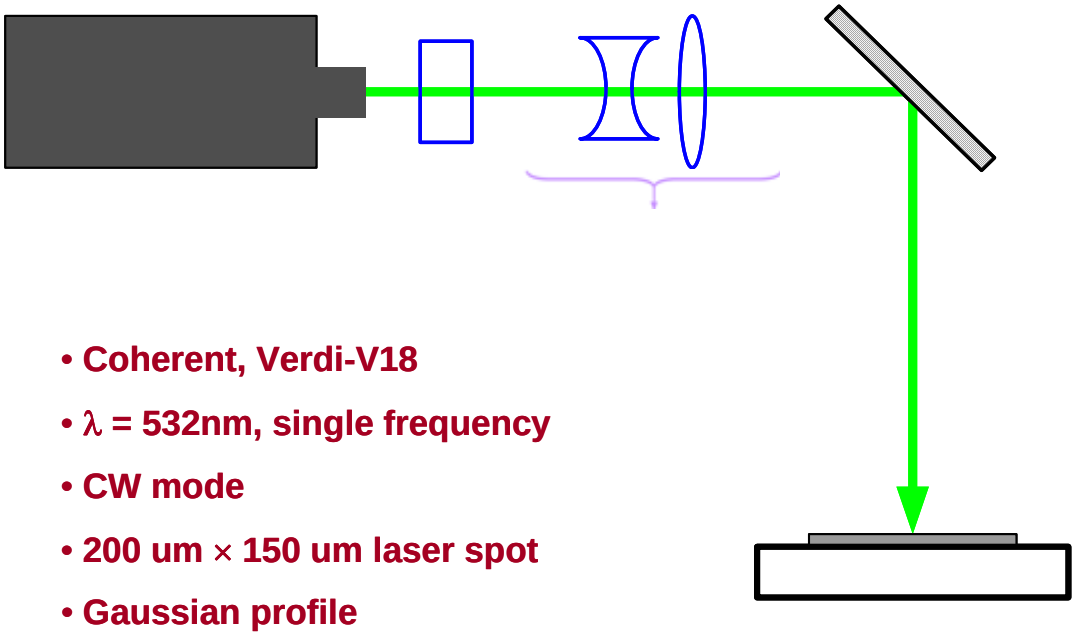


Fig. 5-2 A brief schematic of the CW laser system

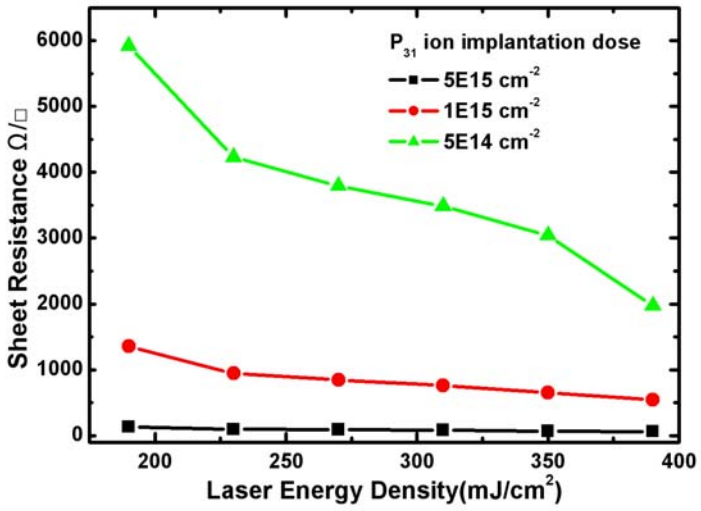


Fig. 5-3 The sheet resistance after excimer laser activation. The dopant was phosphorus. The energy densities of excimer laser were varied from 190 to 390 mJ/cm^2. The ion implantation doses were varied from 5X10^{15} to 5X10^{14} cm^{-2}.

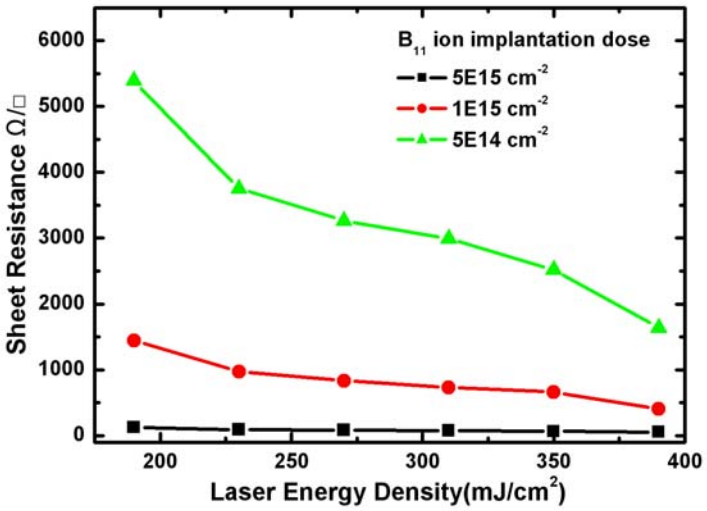


Fig. 5-4 The sheet resistance after excimer laser activation. The dopant was boron. The energy densities of excimer laser were varied from 190 to 390 mJ/cm^2. The ion implantation doses were varied from 5X10^{15} to 5X10^{14} cm^{-2}.

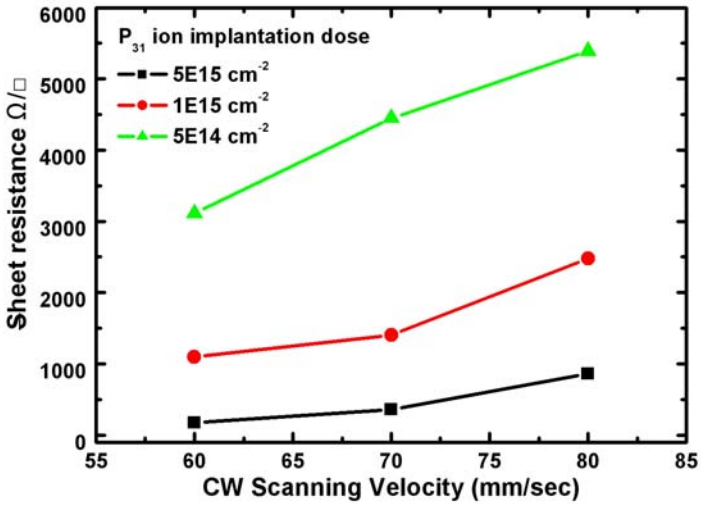


Fig. 5-5 The sheet resistance after CW laser activation. The dopant was phosphorus. The power of CW laser was 10W. The scanning rate was varied from 80mm/sec to 60mm/sec. The ion implantation doses were varied from 5X10^{15} to 5X10^{14} cm^{-2}.

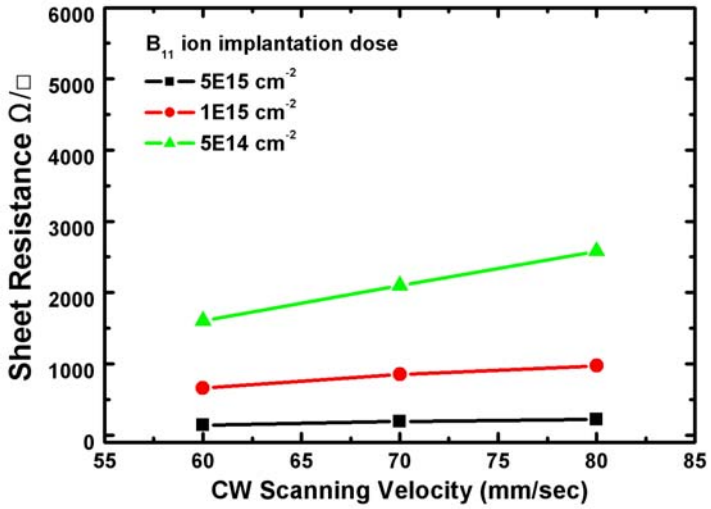


Fig. 5-6 The sheet resistance after CW laser activation. The dopant was boron. The power of CW laser was 10W. The scanning rate was varied from 80mm/sec to 60mm/sec. The ion implantation doses were varied from $5X10^{15}$ to $5X10^{14}$ cm^{-2}.

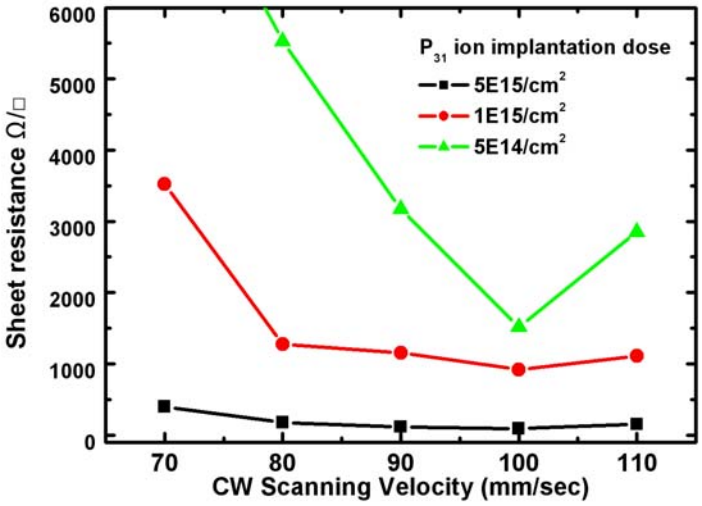


Fig. 5-7 The sheet resistance after CW laser activation. The dopant was phosphorus. The power of CW laser was 15W. The scanning rate was varied from 110mm/sec to 70mm/sec. The ion implantation doses were varied from $5X10^{15}$ to $5X10^{14}$ cm^{-2}.

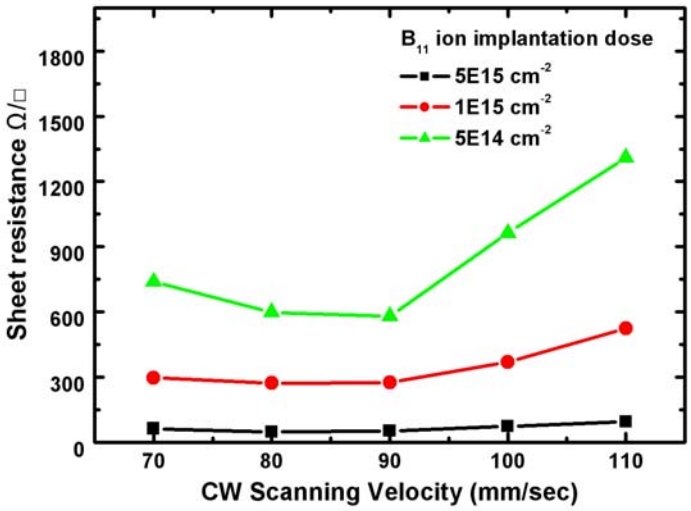


Fig. 5-8 The sheet resistance after CW laser activation. The dopant was boron. The power of CW laser was 15W. The scanning rate was varied from 110mm/sec to 70mm/sec. The ion implantation doses were varied from $5X10^{15}$ to $5X10^{14}$ cm^{-2}.

Sheet resistance Ω/□	P_{31} 5E15	B_{11} 5E15
CW laser 15 W	92.0	47.6
CW laser 10 W	174	141
Excimer laser 390 mJ/cm²	63.4	54.6

Table 5. 1 Summary of the sheet resistances after CW laser and excimer laser activation.

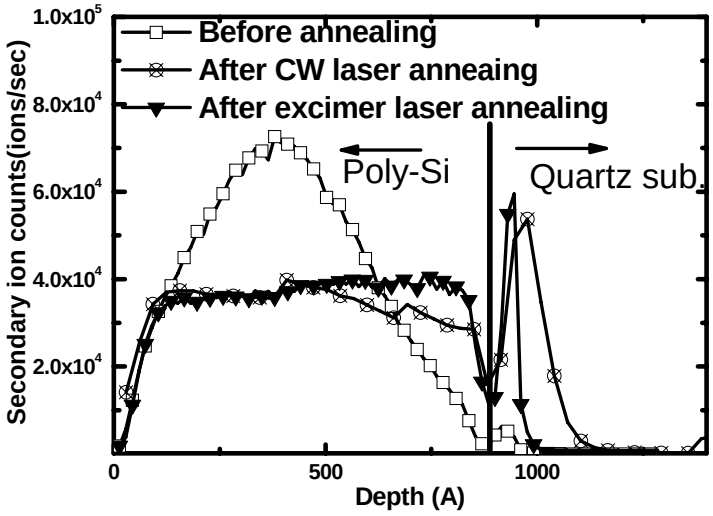


Fig. 5-9 The redistribution profiles of P31 after excimer and continuous wave laser annealings. The power of CW laser was 15W. The scanning rate was 100mm/sec. The energy density of excimer laser was 390 mJ/cm2. The number of laser shots was 20(ie. 95% overlapping). The ion implantation dose was 5X1015cm-2.

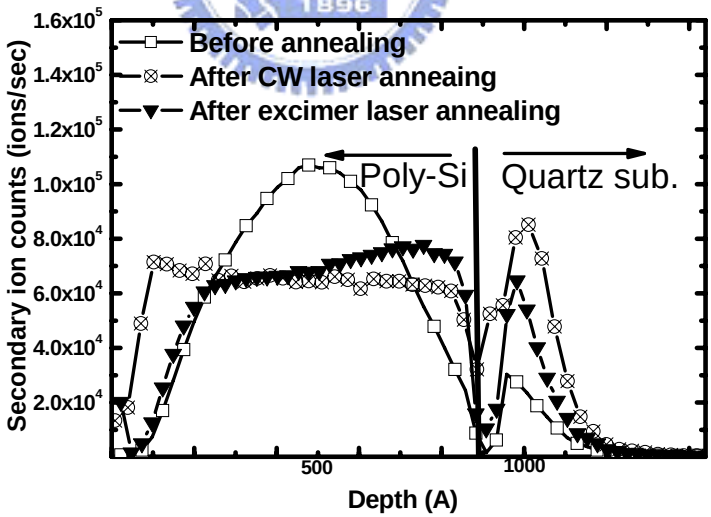


Fig. 5-10 The redistribution profiles of B_{11} after excimer and continuous wave laser annealings. The power of CW laser was 15W. The scanning rate was 90mm/sec. The energy density of excimer laser was 390 mJ/cm^2. The number of laser shots was 20(ie. 95% overlapping). The ion implantation dose was 5X10^{15}cm^{-2}.

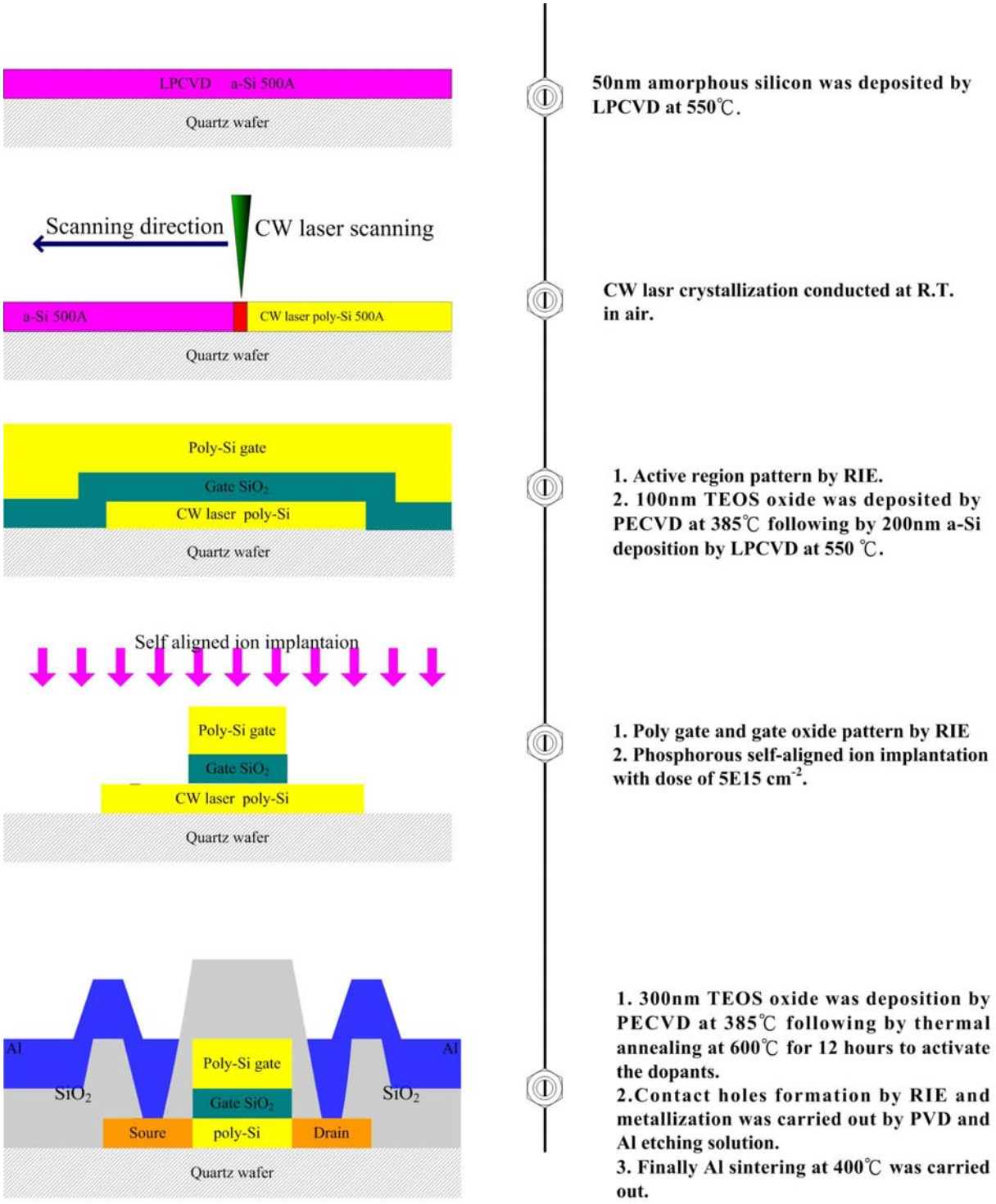


Fig. 5-11 Process flows of high-performance LTPS-TFTs fabricated by CW laser annealing.

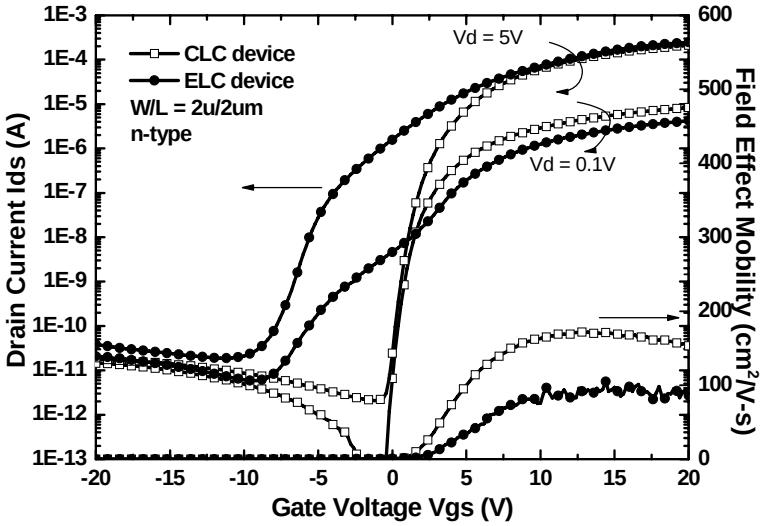


Fig. 5-12 The typical transfer characteristics of n-type CLC-LTPS-TFTs with channel lengths of 2μm.

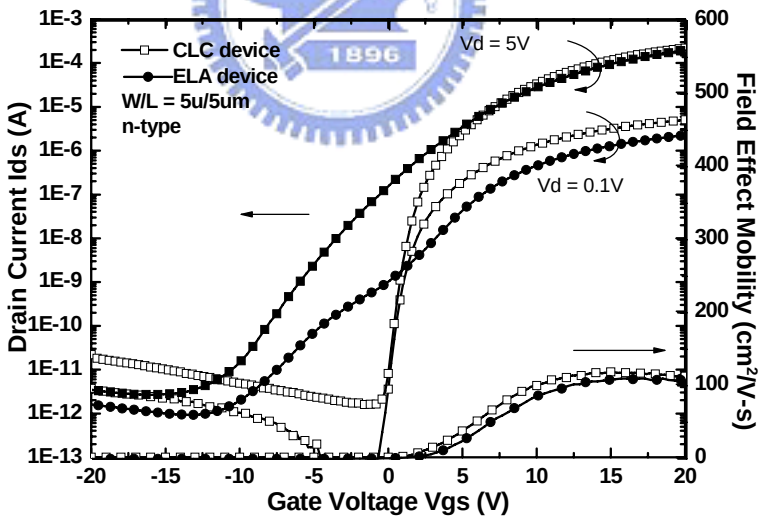


Fig. 5-13 The typical transfer characteristics of n-type CLC-LTPS-TFTs with channel lengths of 5μm.

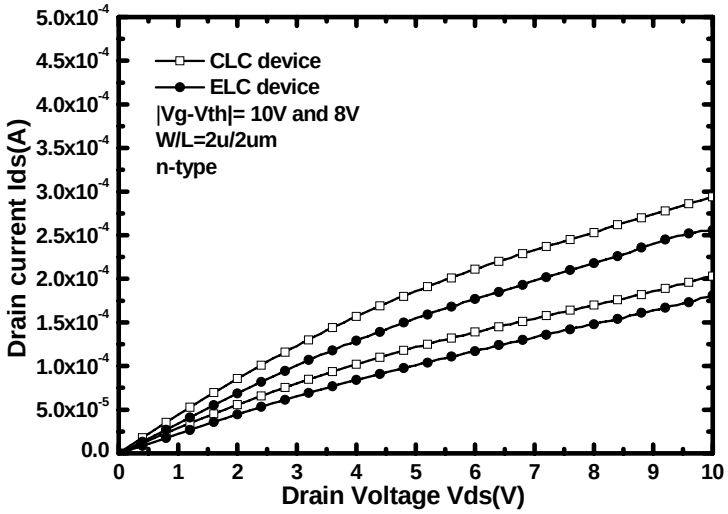


Fig. 5-14 The output characteristics of n-type CLC-LTPS-TFTs with channel lengths of 2μm

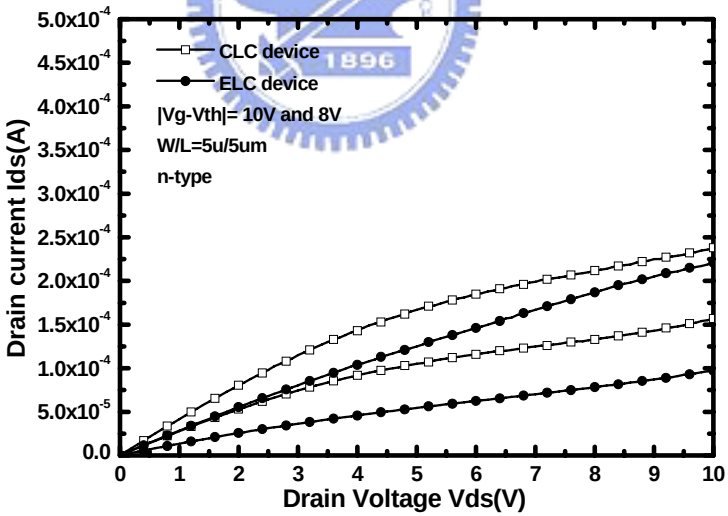


Fig. 5-15 The output characteristics of n-type CLC-LTPS-TFTs with channel lengths of 5μm

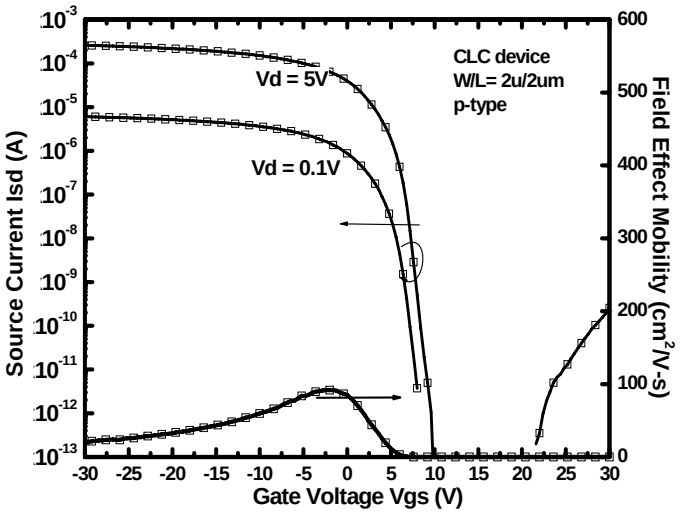


Fig. 5-16 The typical transfer characteristics of p-type CLC-LTPS-TFTs with channel lengths of 2μm.

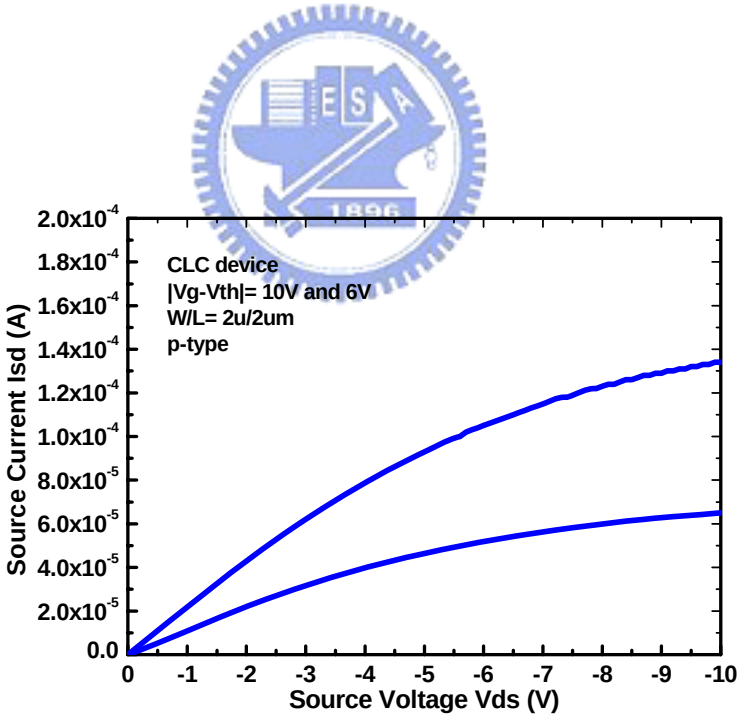


Fig. 5-17 The output characteristics of p-type CLC-LTPS-TFTs with channel lengths of 2μm.

	Mobility (cm^2/V-s)	Sub-threshold swing (V/dec)	Threshold voltage Vth (V)	on/off current ratio
CLC n-type LTPS-TFT (W/L= 2 μm/2 μm)	192	0.225	1.49	1.02E+08
ELC n-type LTPS-TFT (W/L= 2 μm/2 μm)	105	1.9	1.29	1.31E+07
CLC n-type LTPS-TFT (W/L= 5 μm/5 μm)	117	0.384	1.93	1.39E+08
ELC n-type LTPS-TFT (W/L= 5 μm/5 μm)	110	2.99	1.32	1.94E+07
CLC p-type LTPS-TFT (W/L= 2 μm/2 μm)	92	0.604	5.6	1.84E+08

Table 5. 2 Measured optimal electrical characteristics of CLC-LTPS-TFTs and ELC-LTPS-TFTs.

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論文題目：Study on High-Performance Low-Temperature Poly-Silicon Thin Film Transistors with Excimer and Continuous-Wave Laser Annealings

利用準分子及連續波雷射退火製作高效能低溫複晶矽薄膜電晶體之研究