國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩士論文

高介電材料及奈米微晶粒捕陷層在快閃記憶體之研究

The Study of Flash Memory with High-K Material and Nano-crystal Trapping Layer

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摘　　要

在本論文中，首先，我們製作出一個閘極長度為55奈米的氧化鉿奈米微晶粒記憶體在SOI晶片上。從實驗結果得知我們的元件有擁有記憶視窗大的特性、資料寫入/抹除速度快與資料保存能力好的特點，並且我們達成即使閘極長度為55奈米還可完成一個單元儲存2個位元的記憶體操作，並且我們的製程可與現今CMOS元件製程相配合。因此相信此元件在高密度儲存方面上的應用應該是有機會的。

接著，我們使用高介電常數材料當作捕陷層成功的製作出了SONOS型非揮發性快閃記憶體，此材料為氧化鑭。我們在此實驗中達成有快速的寫入/抹除速度、大的記憶窗口、儲存資料持久性、以及寫入、清除操作造成的性能退化少的非揮發性快閃記憶體。並且，我們也成功的再此元件上設計出一個單元儲存2個位元的記憶體操作。因此相信使用氧化鑭來取代氮化矽在SONOS非揮發性快閃記憶體上是有機會的。

最後，我們使用另一種高介電常數材料當捕陷層製作出了SONOS型非揮發性快閃記憶體，此材料為氧化鐠。我們在此實驗中，達成了電荷捕捉效率佳、有

快速的寫入/抹除速度、大的記憶窗口的非揮發性快閃記憶體，但是其儲存資料持久性並不好。

The Study of Flash Memory with High-K Material and Nano-crystal Trapping Layer

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ABSTRACT

In this thesis, first a tri-gate 55nm SONOS-type memories on SOI with HfSiOx nanocrystal trapping layers was proposed and demonstrated. We use CHE programming, FN programming, BTBHH erasing and FN erasing for the memory operation. Experimental results reveal that large memory windows, relative high P/E speed and good retention can achieve for SONOS-type memories and it is fully compatible to current CMOS technologies. In summary, tri-gate 55nm SONOS-type memories on SOI are the candidates used for the high density storage application.

Then, a SONOS-type memories by using high-κ dielectric materials Lanthanum oxide trapping layers was proposed and demonstrated. We use CHE programming and BTBHH erasing for the memory operation. Experimental results reveal that large memory windows, relative high P/E speed and good retention can achieve for SONOS-type memories. In summary, La_2O_3 are the candidates used for the trapping layers for the SONOS-type memories and two-bit application.

Finally, a SONOS-type memories by using high-κ dielectric materials Praseodymium oxide trapping layers was proposed and demonstrated. The SONOS-type Pr_2O_3 flash memories exhibit that they have large memory windows, relative high P/E speed but poor retention.

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謝謝你們的支持與鼓勵，僅以此論文獻給你們。

Contents

TABLE CAPTIONS

Chapter 1

Chapter 2

Chapter 3

Chapter 4

FIGURE CAPTIONS

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 1

Introduction

1.1 Overview of Nonvolatile Flash Memory

With the development of information technology, people put more and more emphasis on the materials and techniques of semiconductor memory, especially for the consumer electronic products.

Memory can be divided in to two kinds by whether the storage data can be affect by the power supply. One is volatile memory, and the other s non-volatile memory. Volatile memory defines as that the data that stored in memory need power supply to maintain. On the other hand, non-volatile memory means that even if it encounters the break of power supply, the data in the memory also can maintain for a long time. For example, Dynamics Random Access Memory (DRAM) and Static Dynamics Random Access Memory (SDRAM) belong to volatile memory, and Read Only Memory (ROM), Electrically Programmable Read Only Memory (EPROM), and Flash memory belong to non-volatile memory. The speed of non-volatile memory although can not compare with volatile memory, but the data in non-volatile memory can maintain for a long time without power supply. Because of the advantage, non-volatile memory becomes more and more important and was used in all kinds of electronic products.

In 1967, D. Kahng and S. M. Sze invented the first Floating-gate (FG) non-volatile memory at Bell Labs [1]. After that, all kinds of non-volatile memory were invented and were applied in our daily life. Read Only Memory (ROM) was the

early products of non-volatile memory. This memory programs its data in its fabrication process and it has the advantages of cheap and high density. Hence, ROM was applied widely in all kinds of electric products such as personal computer, printer, video game and etc. However, this memory is not convenient, because if we want to change one bit, we need a new mask.

Latter, one kind of memory called Programmable Read Only Memory (PROM) was invented, which didn't need specific mask for specific function because the data was written in after the whole ic chip fabrication. Hence, it has the advantage of fast production. Although PROM can be programmed according to the need of consumers, but the data in the memory can not be erased by the users.

In order to solve the program, Electrically Programmable Read Only Memory (EPROM) was invented, and it programs the memory cell by electrical method such as channel hot electron (CHE). However, EPROM can't erase by electrical method, and it need to illuminate the UV light to erase it. Because of this reason, a quartz window is necessary on the package of the EPROM. Thus, quartz window package lead to the expansive package cost and make EPROM inconvenient.

The appearances of Electrically Erasable Programmable Read Only Memory (EEPROM) solve the program of EPROM that described above. It can both program and erase by electrical method, but it need a select transistor to achieve the advantage. Hence, the density of EEPROM is lower than EPROM and EEPROM is more expensive.

Flash memory follows the basic structure of EEPROM without select transistor. Unlike EPROM and EEPROM, flash memory cell provides single-cell electrical program and fast simultaneous block electrical erase [2]. Thus, a small cell size is combined with a fast in-system erase capability, and flash memory has the advantage of long life time, low production cost, low power, and robust flash systems. Hence,

flash memory is good for consumer electric products such as mobile phone, pager, digital cameras, MP3 player, PDA and etc. Table1 compare the characteristics of the flash memory with PROM, EPROM, and EEROM [3].

The basic concept of Floating-gate (FG) non-volatile memory (as Figure.1(a)) is a MOSFET with a modified gate stack structure that has a control gate (CG) and a floating gate (FG) embedded in a dielectric material such as silicon dioxide (SiO_2), and both the CG and FG is conductor. The MOSFET operated as a switch with the control gate modulating the electron current flow between the source and drain. The memory storage element is the isolated floating gate disconnected from the terminal voltage. It sits between the control gate and the channel.

The storage charge will affect the threshold voltage. By the different threshold voltage, we can define that the operation voltage Vg of memory cell is at the middle of the two threshold voltage. Thus, the programming state can be determined by measuring the current in the MOSFET with the operation voltage Vg (as Figure.2).

Because of manipulating electric field to control the data to program or erase, the tunneling oxide should be thin enough to let charge inject into the floating gate. However, if the tunneling oxide is too thin or it has local defect or it has stress induce leakage current (SILC) path (as Figure. 1(b)), it will lead to leak charge. And the floating gate is also a conductor, so it will lead to whole charge leak out. This is a big problem for data retention.

In order to solve the problem, one method is that it can replace the conductive floating gate with insulator which has a large mount of trap sites (as Figure. 3), such as SiN_3 [4], Al_2O_3 [5], HfO_2 [6], ZrO_2 [7] and some high-K materials [8]. This method uses the materials which are easy to trap charge to increase the capability of charge retention, and it stores the charge in the discrete trap site. Because the charge in the trap site will not interact, the local defect of tunneling oxide will not leak out all of the

charge. Besides, the high-k materials have higher dielectric constant. So they can reduce the equivalent oxide thickness of the gate stack and reduce the operation voltage.

Another method is that it can replace the conductive floating gate with nanocrystals as charge storage node, such as Si nanocrystals [9], Ge nanocrystals [10], HfO_2 nanocrystals [11], and metal nanocrystals [12,13] (as Figure. 4). Nanocrystals memory has separate and discontinuous charge storage node. Hence, the migration of charge in horizontal and vertical direction can be suppressed by the silicon dioxide. Thus, nanocrystals flash memory has good charge retention. Moreover, it can have thinner tunneling oxide and smaller operation voltage with good programming and erasing speed. So, it meets the requirements of low power and voltage in VLSI.

1-2 Motivation

Future high density flash memories for stand-alone data storage application require device with minimum feature smaller and smaller, such as 50nm. In this range it has been shown that silicon-oxide-nitride-oxide-silicon (SONOS) structure have promising scaling behavior in tri gate structure [14,15] due to the improved electrostatic control of the channeling region.

And *Lee et al.* has reported that a high-k nanocrystal charge-trapping layer can be fabricated by annealing high-k silicate materials, such as $HfSi_xO_y$. After applying a rapid thermal anneal to the silicates, phase-separation happens. HfO_2 nanocrystals [16] are formed and surrounded by SiO_2. The stored charges will be trapped in or around the nanocrystals and isolated by silicon dioxides. Hence, less opportunity of charge loss is expected and a local defect of tunnel oxide won't cause a severe charge loss. With such a nanocrystal structure as the charge-trapping layer, the retention of

nonvolatile memories can be further improved.

Because of all of above, we want to fabricate a device with a gate length 60nm by using tri gate structure and HfO_2 nanocrystals as charge trapping layer. And the device show that it has large memory window, good program /erase speed, good retention, and good endurance.

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In floating gate device, there are some problems in the scaling down. The floating gate device should use thick tunneling oxide, which is required to guarantee long charge retention time. Thus, they need high voltage operation for program and erase. Recently, silicon-oxide-nitride-oxide-silicon (SONOS) structure of charging device become attractive because they do not have planar scaling problem for floating gate isolation and they show good retention characteristic due to the discrete and deep traps in the nitride trapping layer. Therefore, low voltage operation by application of thin tunneling oxide is practicable [17]. Besides, the localized carrier trapping in the trapping layer makes a 2-bits operation possible.

From all of above, we want to fabricate a high performance nonvolatile memory with a high-k charge-trapping layer. The high-k dielectric material are La_2O_3 and Pr_2O_3. These high-k layer replace the silicon nitride layer in the SONOS structure. These materials provide high trapping state densities and deep trapping levels, therefore they can enhance the retention of nonvolatile memories. The charge-trapping efficiency can be improved, and larger operation window can be achieved. The application of high-k materials can further reduce the operation voltage and potentially can help memory device scaling.

1.3 Organization of the Thesis

In the following section, we will show our research efforts.

In chapter 2, the electrical characteristics and fabrication process of 55nm tri-gate flash memory with HfO_2 nanocrystal trapping layer will be proposed. The Experiment results reveal that the program/erase speed and endurance of our device have good performance.

In chapter 3, the electrical characteristics and fabrication process of Characteristics of SONOS-type Memories by Using Lanthanum Oxide Trapping Layers will be proposed. The Experiment results reveal that the program/erase speed and endurance of our device have good performance.

In chapter 4, the electrical characteristics and fabrication process of Characteristics of SONOS-type Memories by Using Praseodymium Oxide Trapping Layers will be proposed. The Experiment results reveal that the program/erase speed and endurance of our device have good performance.

At the end of this thesis, we will make a conclusion in chapter 4.

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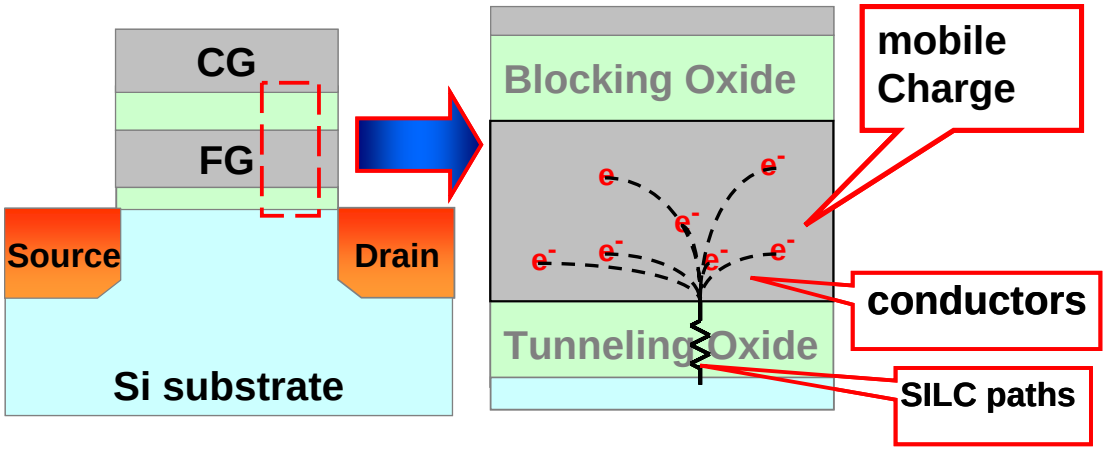
	UV-EPROM	PROM	EEPROM	FLASH
Package	Ceramic with window	Plastic	Plastic	Plastic
Erase Time	20 min	No erase	1 ms	100 ms
Program Time	<1 ms	<1 ms	<1 ms	200 μs
Cell Area	Small	Small	Large	Small
Eraser	UV light	No need	Electrically	Electrically
Structure	Double Poly-Si	Double Poly-Si	Double Poly-Si	Triple Poly-Si

Table.1-1 The comparison of the flash memory with PROM, EPROM, and EEROM



(a) (b)

Fig. 1-1 The basic concept of Floating-gate (FG) non-volatile memory

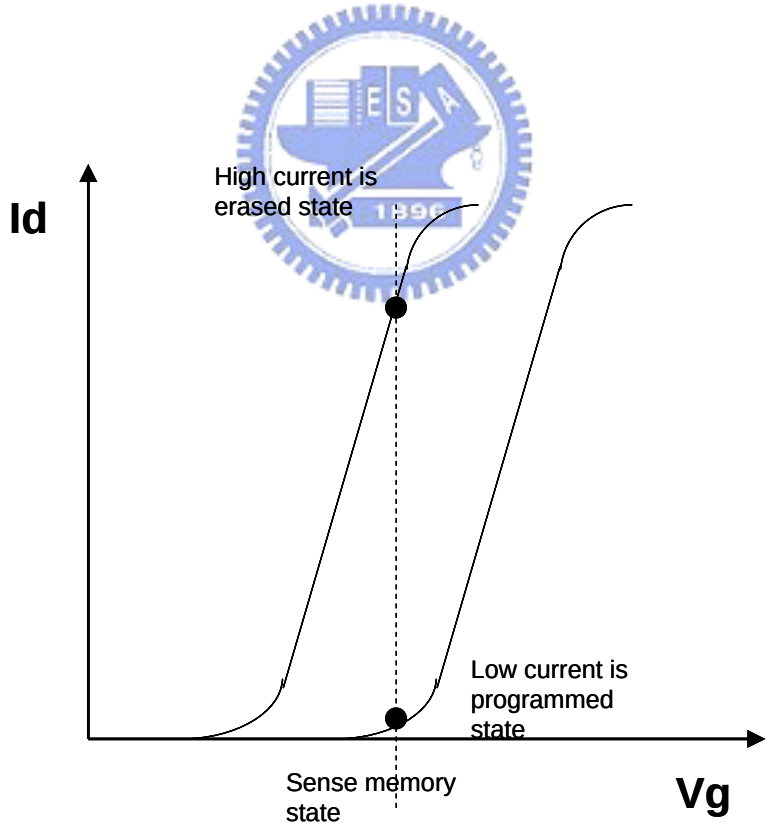


Fig. 1-2 The basic concept of the reading of the memory cell

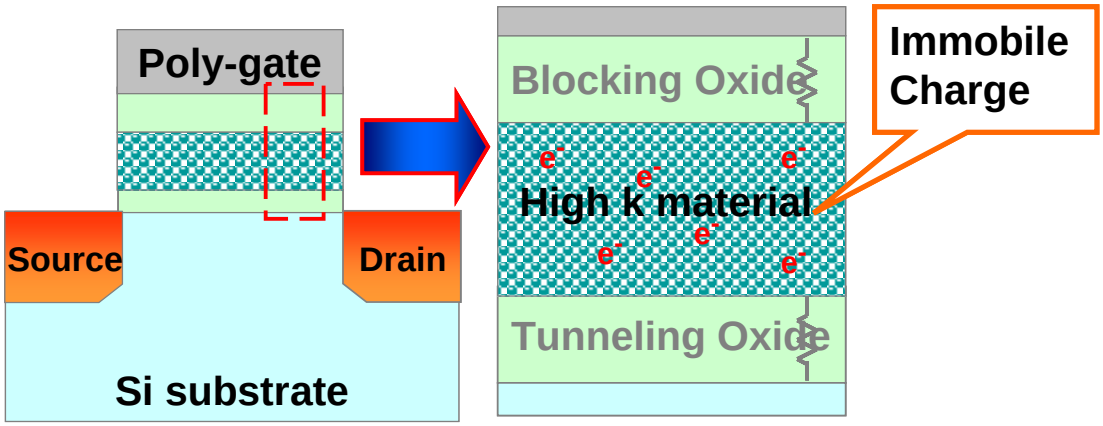


Fig. 1-3 The basic concept of SONOS-type non-volatile memory

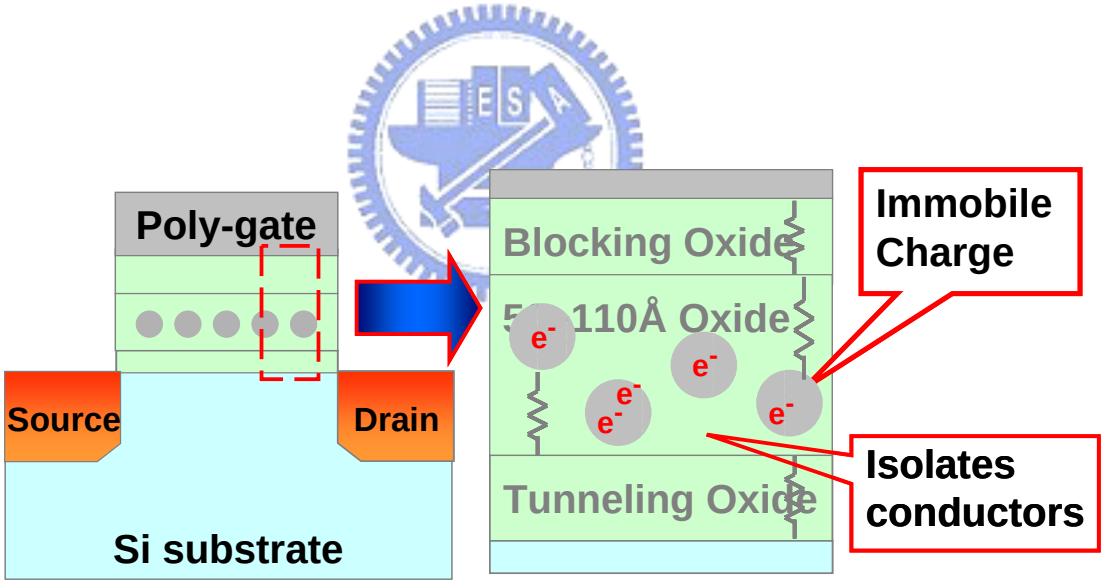


Fig. 1-4 The basic concept of nanocrystal non-volatile memory

Chapter 2

Characteristic of tri-gate Flash Memory with HfO_2 nanocrystal Trapping Layer

2.1 Introduction

With the development of semiconductor industry, high density flash memories for stand-alone data storage application require device with minimum feature smaller and smaller, such as 50nm. However, the conventional floating gate (FG) nonvolatile memory (NVM) devices use a poly-Si film as charge storage layer in which the information is stored by injecting charges from the inversion or accumulation layer of a MOSFET. Improvements of their performance are based on the shrinkage of the technology and, such as the reduction of the gate length and the thickness of the tunnel oxide. However, further scaling of the floating gate nonvolatile memories is facing severe reliability issues such as the difficulty to maintain long data retention times.

In order to overcome the scaling limit, the idea of the discrete-trap mechanism has been proposed. It means that we can replace the floating gate of nonvolatile memories by many discrete trapping centers, which can be made by natural traps in an appropriate insulator such as a nitride layer in SONOS [1][2] memories or by nanocrystals. And it also has been shown that tri gate structure [3] can suppress short channel effects and drain-induced barrier lowering (DIBL) due to the improved electrostatic control of the channeling region.

And *Lee et al.* [4] has reported that a high-k nanocrystal charge-trapping layer can be fabricated by annealing high-k silicate materials, such as $HfSi_xO_y$. After applying a

rapid thermal anneal to the silicates, phase-separation happens. HfO_2 nanocrystals [] are formed and surrounded by SiO_2. Hence with the nanocrystals charge trapping layer, the stored charges will be trapped in or around the nanocrystals and isolated by silicon dioxides. Hence, less opportunity of charge loss is expected and a local defect of tunnel oxide won't cause a severe charge loss. With such a nanocrystal structure as the charge-trapping layer, the retention of nonvolatile memories can be further improved.

In this work, an ONO sandwich structure gate-dielectric stack with HfO_2 nanocrystals trapping layer is form on Si in order to fabricate a tri-gate memory device. And the device show that it has large memory window, good program /erase speed, good retention, and good endurance.

2-2 Experimental

Figure 2-1 schematically depicts the process flow of the proposed flash memory. First, the active region was patterned by E-beam lithography and etching system. Then, a 2-nm tunneling oxide was grown at 1000°C in vertical furnace system. The trapping layer of amorphous HfSiOx silicate layer was deposited by co-sputtering method with pure Silicon (99.9999% pure) and pure Hafnium (99.9% pure) in the oxygen and argon gas ambient. Then, a blocking oxide of about 85nm was then deposited by plasma-enhanced chemical vapor deposition (PECVD) system. Subsequently, 50-nm amorphous silicon (a-Si) gate and 50-nm SiN_3 were deposited by LPCVD. The a-Si gate layer was divided into in-situ n^+ doped gate. The dopant of in-situ n^+ doped a-Si gate was phosphorus. After gate patterning, the remaining oxide on source/drain regions was removed by diluted HF. Then, a self-aligned implantation was used to perform the n^+ source/drain with As^+ to dose 5×10^{15} cm^{-2}

and energy 20 keV, tilt 30^{o}.After implantation, and a 50-nm TEOS oxide sidewall spacer was formed by deposition and etching of TEOS oxide. After that the dopants were activated by RTA at 950°C for 10s and at the same time, HfSiOx silicate layer was converted into the separate HfO_2 and SiO_2 phase. Finally, the nitride layer was etched by H_3PO_4 solution.

2-3 Results and Discussion

2.3.1 Material Analysis of HfO_2 Nanocrystals

Figure 2-2 shows the scanning electron microscopy (SEM) image and Figure 2-3 shows cross-section-view high-resolution transmission microscopy (HRTEM) image of the HfO_2 nanocrystals tri-gate device. Clearly, the gate length is about 55nm from the HRTEM image and the thicknesses of the tunnel oxide and blocking oxide layer are 2.2nm, 8nm, respectively. The trapping layer thicknesses are 7.9nm and the nanocrystals were separated in two dimensions within the SiO_2; in which the average distance is >5 nm. This isolation of the nanocrystals prevents the formation of effective conductive paths between adjacent nodes. The mechanism responsible for the formation of HfO_2 nanocrystal is through the phase separation of hafnium silicate into a crystallized structure [5]. For the Hf-silicate layer, the compositions within metastable extensions of the spinodal are unstable and HfO_2 nanocrystal will be formed and enclosed by SiO_2 after cooling down from RTA processing. All devices described in this paper had dimensions of L = 50nm.

2.3.2 Characteristics of Fresh Devices

Figure 2-4 shows the I_{ds}-V_{gs} curves of the tri-gate HfO_2 nanocrystal tri-gate memory devices with programming time of 0.3. Fowler-Nordheim tunneling injection was employed for programming and erasing. A memory window of about 1.5V can be

achieved at the V_g=8V program operation. Program characteristics of different pulse width for different operation conditions are shown in Figure. 2-5. We employed channel hot-electron injection and Fowler-Nordheim tunneling injection in Figure 2-5(a) and Figure 2-5(b). The "V_t shift" is defined as the threshold voltage change of a device between the written and the erased states. For channel hot-electron injection with V_g=11V V_d=4V, relatively high speed (0.1ms) programming performance can be achieved with a memory window of about 1.8V. For Fowler-Nordheim tunneling injection with V_g=11V, a memory window of about 1.8V can be achieved with 1ms pulse width. Hence, the speed of channel hot-electron injection is faster that of Fowler-Nordheim tunneling injection Meanwhile, Figure 2-6 displays the erase characteristics as a function of various operation voltages. Again, excellent erase speed of around 1 ms can be obtained with Vg=-3V Vd=4V for band to band hot hole injection.

The retention characteristics of the HfO_2 nanocrystal tri-gate memory devices at room temperature (T=25°C) and higher temperature (T=85°C, 125°C) are illustrated in Figure 2-7. The retention time can be up to 10^8 seconds for 17% charge loss at room temperature and 40% charge loss and 65% charge loss for the 85°C and 125°C s conditions. We ascribe these results to the combining effects of the tight embrace of HfO_2 nanocrystals by SiO_2-rich matrix and the sufficiently deep trap energy level [6,7]. As a result, superior retention characteristic of the charge storage can be procured[8-11].

The endurance characteristics after 10^4 P/E cycles are also shown in Figure 2-8. The programming and erasing conditions are V_g=11V V_d=4V for 1ms and V_g=-3V, V_d=4V for 1ms, respectively. Slight memory window narrowing has been displaye and the individual threshold voltage shifts in program and erase states become visible after 10^3 cycles.. This trend indicates the formation of operation-induced trapped

electrons. Certainly, this is intimately related to the use of ultra-thin tunnel oxide and very minute amount of residual charges in the HfO_2 nanocrystals after cycling.

The cycling retention is an important issue for flash memory. Therefore, we studied the retention loss behavior of the device before and after 10K cycling. Figure 2-9 show the cycling retention behavior of the cell at room temperature (25^{o}C).As we can see in Figure 2-9, the charge loss behavior of the device with 10K cycling is more serious than the device without 10K cycling under room temperature condition. The retention time can be up to 10^8 seconds with 70% charge for cycling device. We ascribe these results to that the tunneling oxide was damage after10K P/E cycling. Hence, the capability of charge storage was decreased.

2.3.3 Characteristics of 2-bit operation

Figure 2-10 demonstrates the feasibility of performing two-bit operation with our HfO_2 nanocrystal tri-gate memories through forward and reverse read scheme in a single cell. From the I_{ds}–V_{gs} curves, it is clear that we could employ forward and reverse reads to detect the information stored in the programmed bit1 and bit2, respectively. Table 2-1 summarizes the bias conditions for two-bit operation. Figure 2-11 shows the 2-bit retention characteristics of the HfO_2 nanocrystal tri-gate memories. The retention time can be up to 10^8 seconds with 0.8V memory window between programmed bit-1 and erased bit-2. We can see that charge loss occurred for programmed bit-1 and charge gain for erased bit-2. This suggests that there is lateral migration of trapped electron.[12]

2.3.4 Disturbance

Figure 2-12 demonstrates the read disturbance induced erase-state threshold voltage instability in a localized HfO_2 nanocrystal tri-gate Flash memory cell under several operation conditions. For two-bit operation, the applied bitline voltage in a

reverse-read scheme must be sufficiently large (>1.5 V) to be able to “read through” the trapped charge in the neighboring bit. The read-disturb effect is the result of two factors: the word-line and the bit-line. The word-line voltage during read may enhance room temperature (RT) drift in the neighboring bit [12]. On the other hand, a relatively large read bit-line voltage may cause unwanted channel hot-electron injection and, subsequently, result in a significant threshold voltage shift of the neighboring bit. In our measurements, the gate and drain biases were applied and the source was grounded. The results demonstrate clearly that almost no read disturbance occurred in our HfO_2 nanocrystal tri-gate Flash memory under low-voltage reading (V_g =1.5 V; V_d = 1.5 V). For a larger memory window, we found that only a small read disturbance can be observed after operation at V_d = 2 V after 1000 s at 25 °C.

Figure 2-13 shows the programming drain disturbance of our HfO_2 nanocrystal tri-gate Flash memory. Drain disturbance may occur during programming for the cells sharing a common bit-line while one of the cells is being programmed and gate disturbance may occur during programming for the cells sharing a common word-line while one of the cells is being programmed as in Figure 2-14. Two different drain voltages (V_d = 3 and 4 V) were applied in the programming drain disturbance measurements at room temperatures. We observed that a 1.5V drain disturb was observed after programming at a value of V_d of 4V under T = 25 °C and after stressing for 1000 s. Figure 2-15 shows the gate disturbance characteristics in the erasing state. Because we can program the device by Fowler-Nordheim tunneling injection, the gate disturbance will not be too small. Hence,we observed a threshold voltage shift of 2.5 V under the following conditions: V_g = 11 V; V_s = V_d = V_{sub} = 0 V; stressed for 1000 s. Hence, a non-negligible current will be present in the tunnel oxide when a voltage of 11 V is applied to the gate electrode.

2.4 Summary

In this chapter, we have proposed a novel simple, reproducible, reliable technique for preparation of 55nm high density HfO_2 nanocrystals tri-gate memory using spinodal decomposition of hafnium silicate on SOI. It has good characteristics in terms of large memory windows, high speed program/erase, good retention time, excellent endurance, and 2-bit operation.

With these superior performance, we believe that nano-scale HfO_2 nanocrystal flash memory on SOI is the candidates used for the high density storage application.

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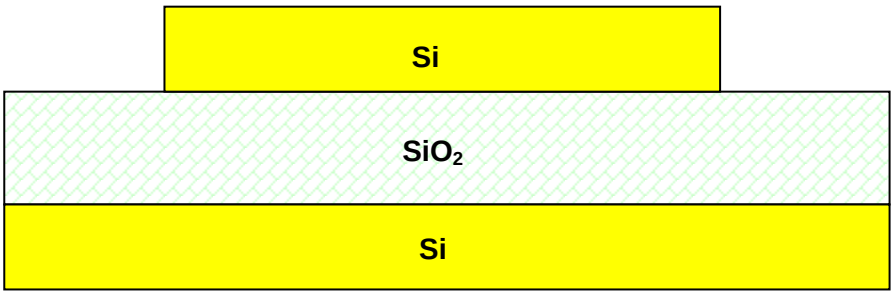
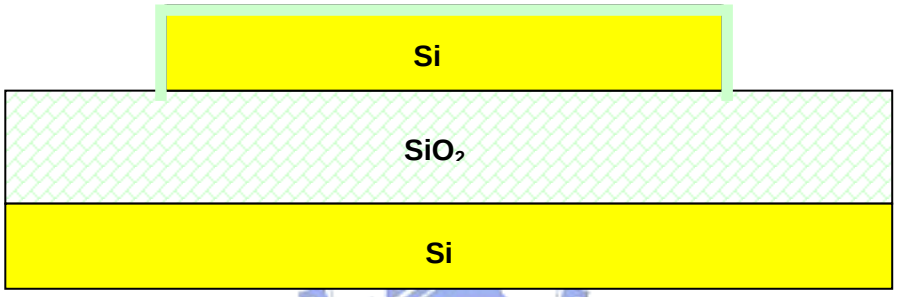
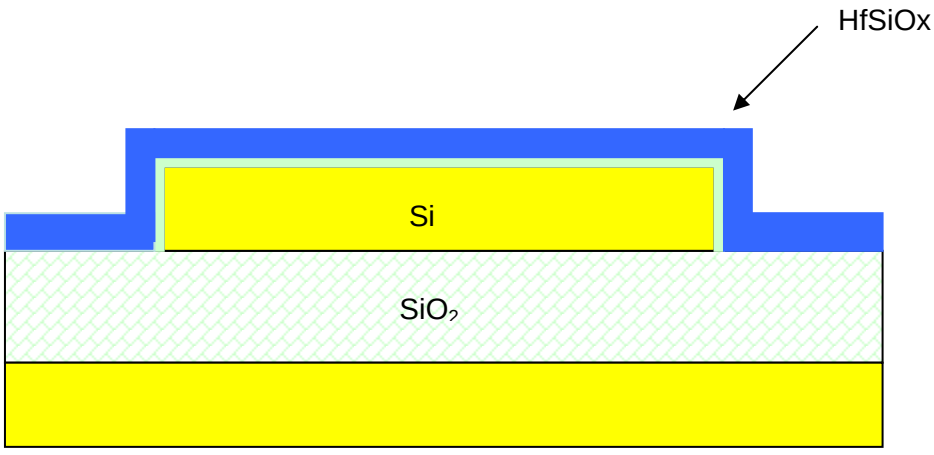


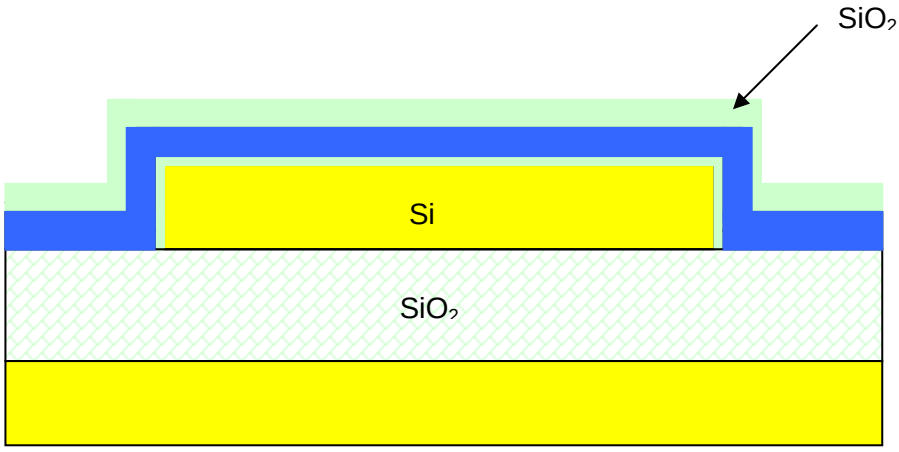
(a) The active region was patterned by E-beam lithography on SOI wafer



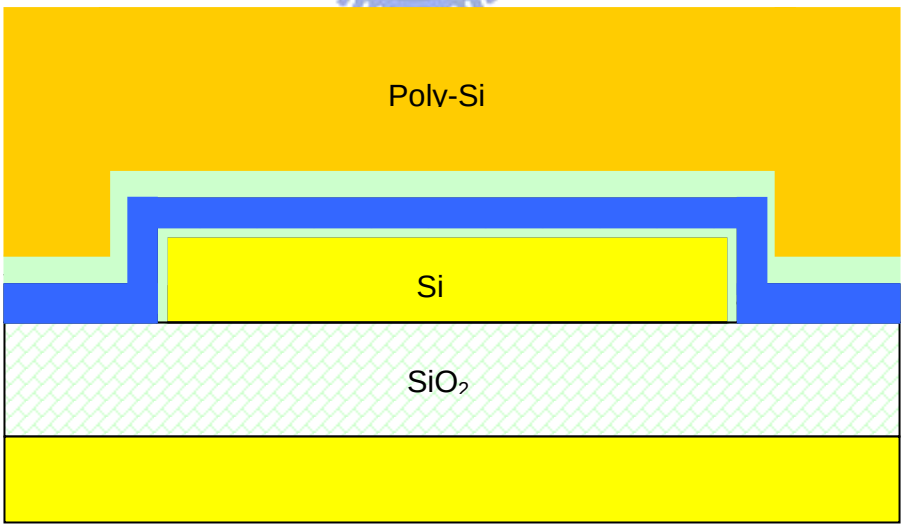
(b) Tunnel oxide was grown at 1000°C in furnace



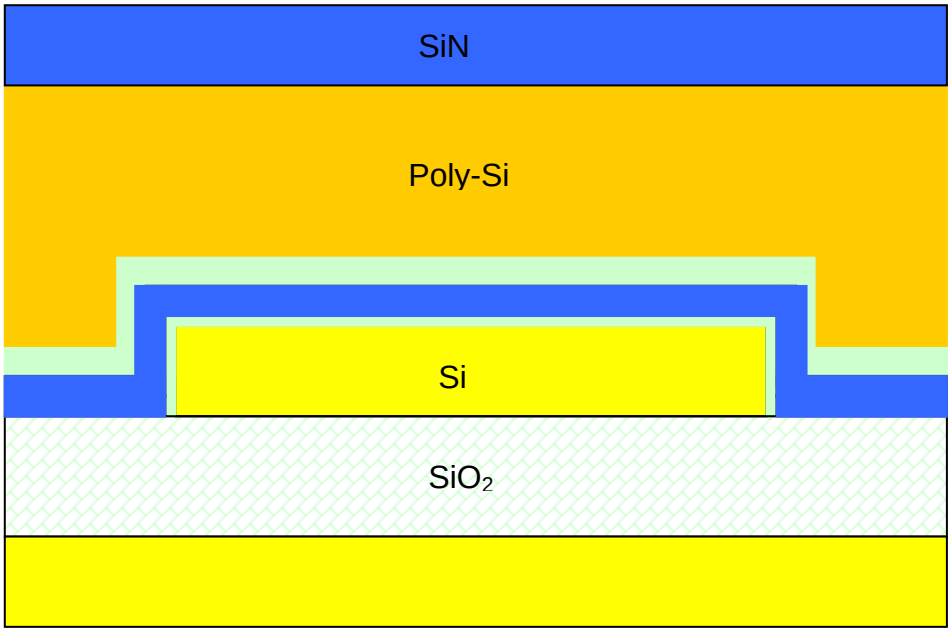
(c) HfSixOy deposited by sputter method as trapping laye



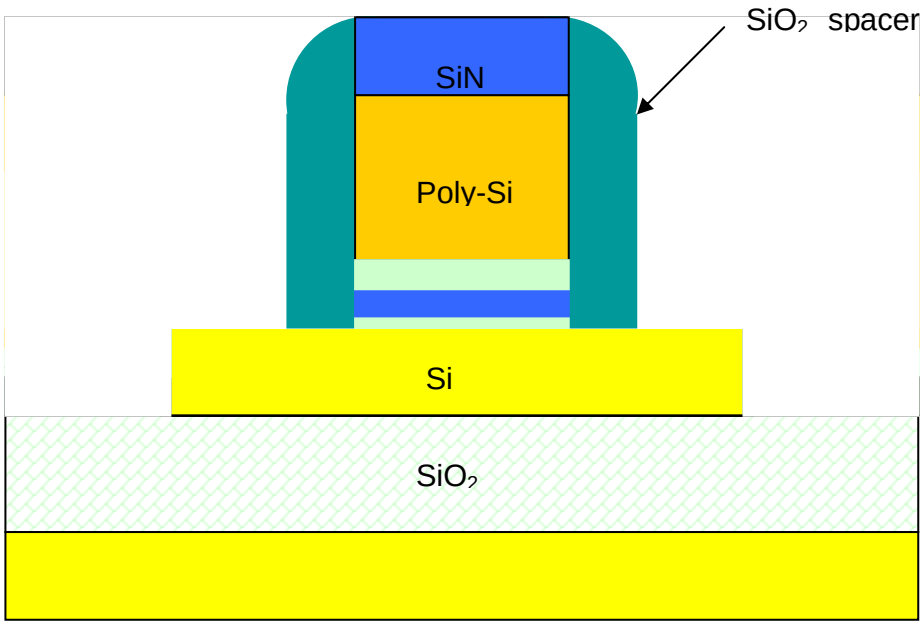
(d) blocking oxide then deposited by PECVD followed by 900°C in N_2 densification



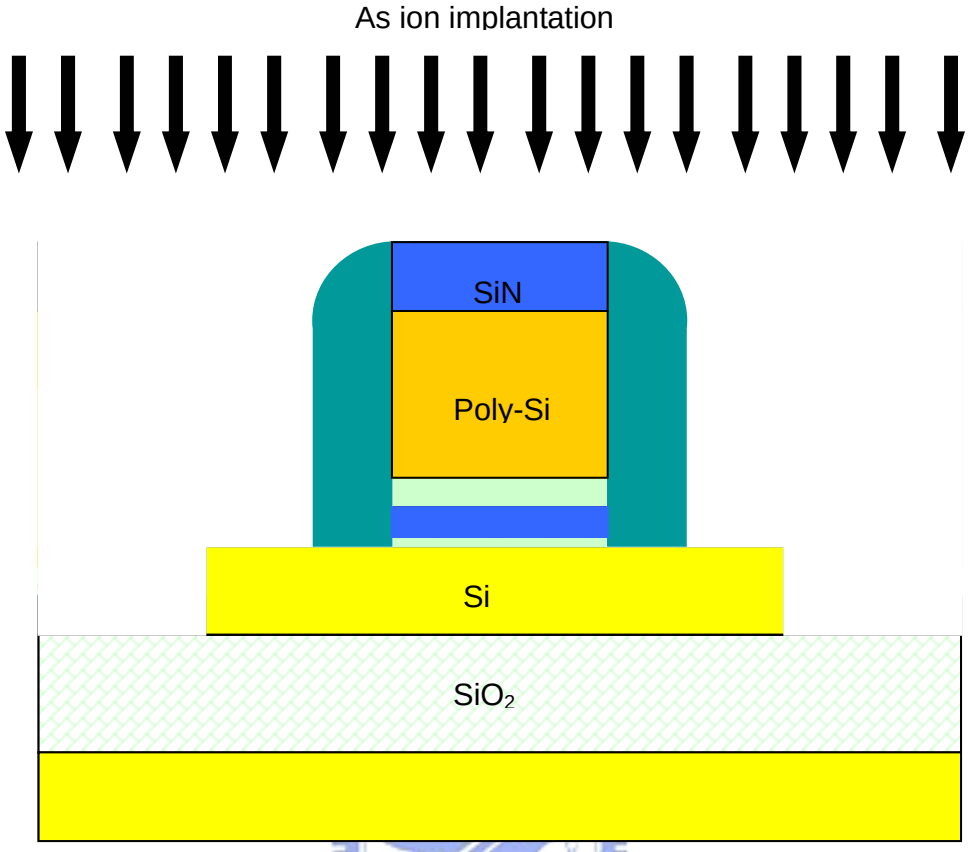
(e) Poly-Si deposited to serve as the gate electrode by LPCVD



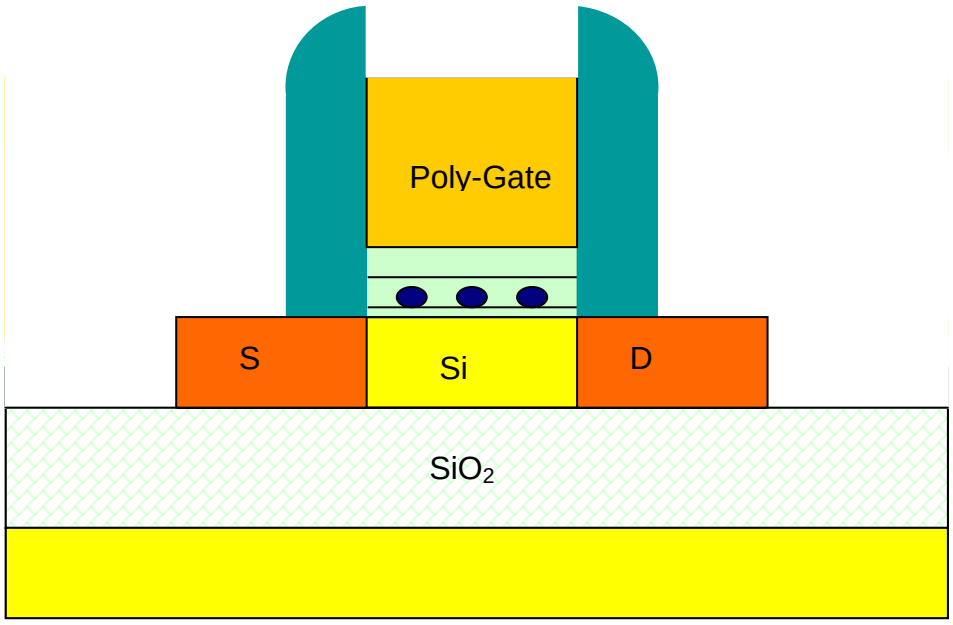
(f)SiN deposited as hard mask



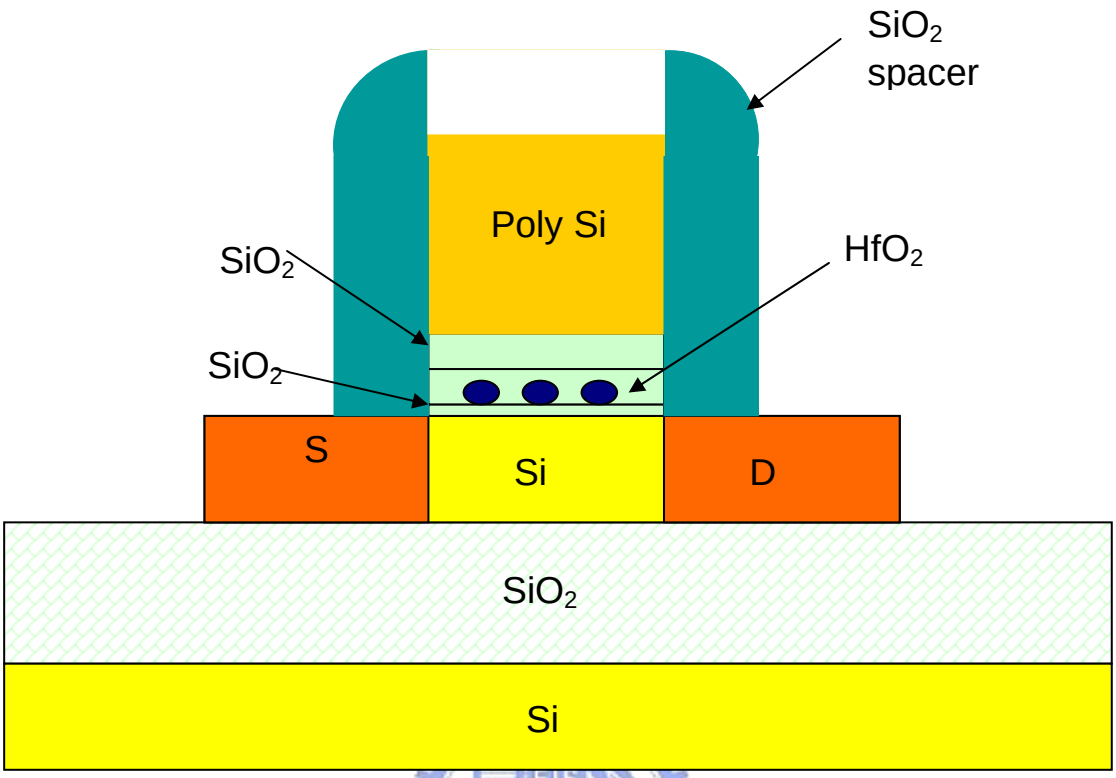
(g) Gate electrode patterned and oxide spacer was formed



(h) source/drain implanted by self-aligned As ion implantation



(i) Dopants were activated at 950°C and convert HfSixOy into HfO_2 dots



(j)

Fig.2- 1 Process flow of the flash memory and the cross-section of the flash memory

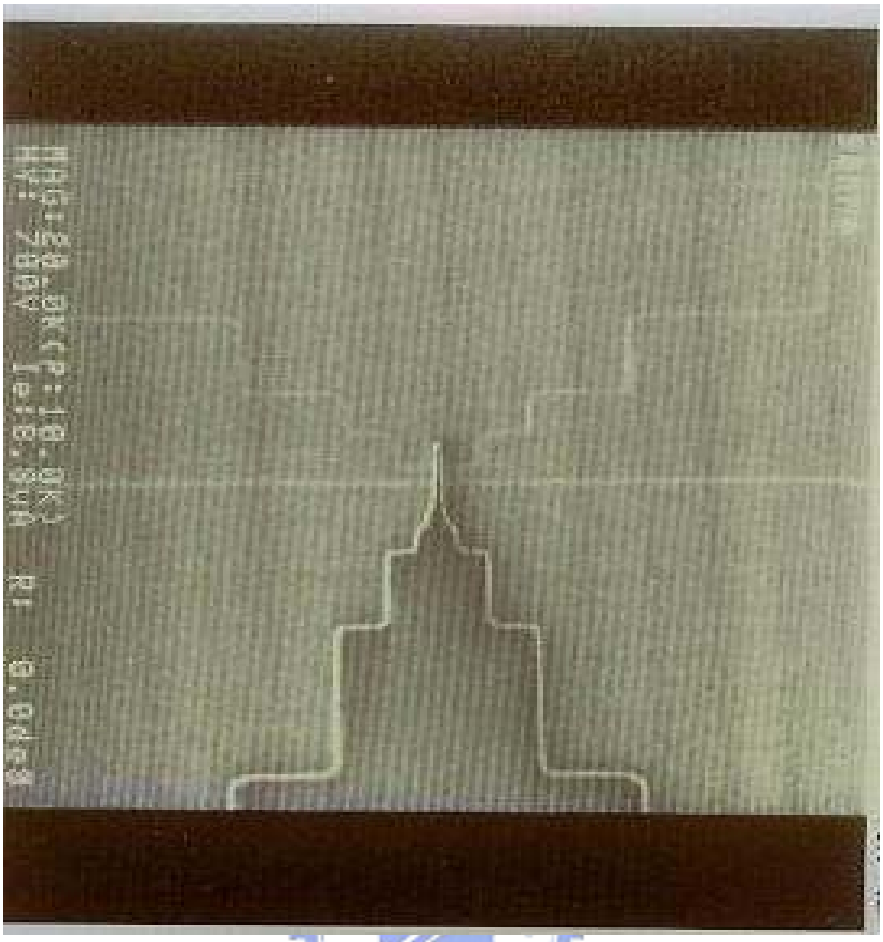
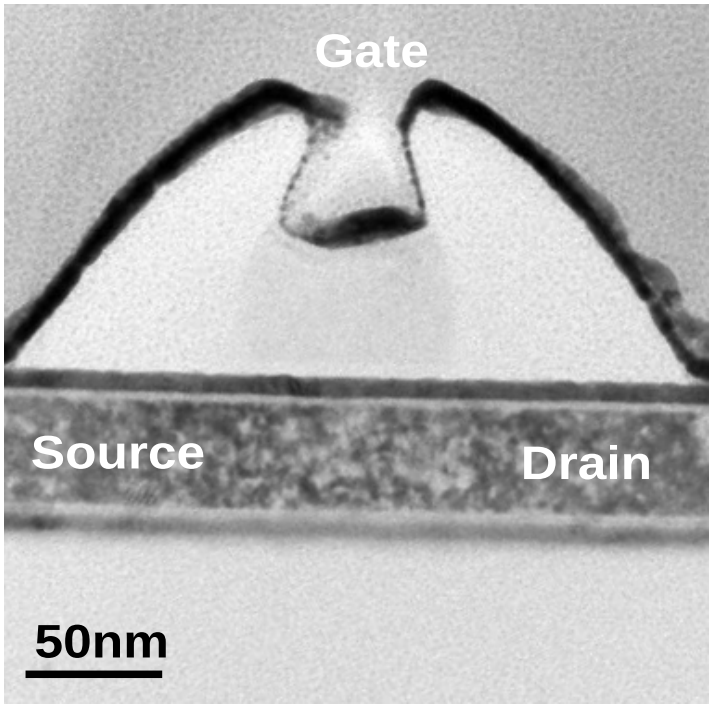
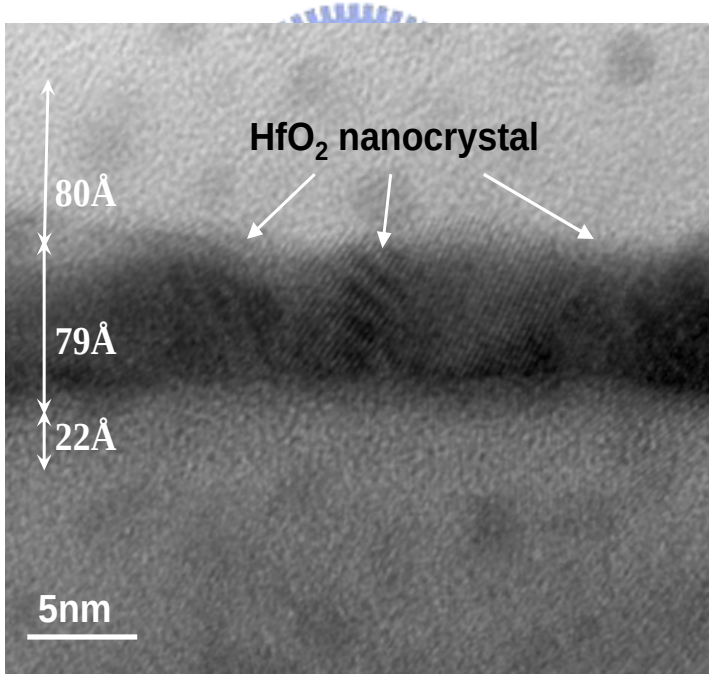


Fig.2-2 show the top view scanning electron micrograph of the memory devic



3(a)



3(b)

Fig.2-3a and 3b show the high-resolution TEM image of cross section and the ONO structure gate-dielectric stack are clearly seen. The gate length is around 55nm. Fig 3b show the high-resolution TEM image of the ONO-type gate stack The thickness of tunneling oxide, trapping layer, and blocking oxide are 22, 79, 80Å, respectively.

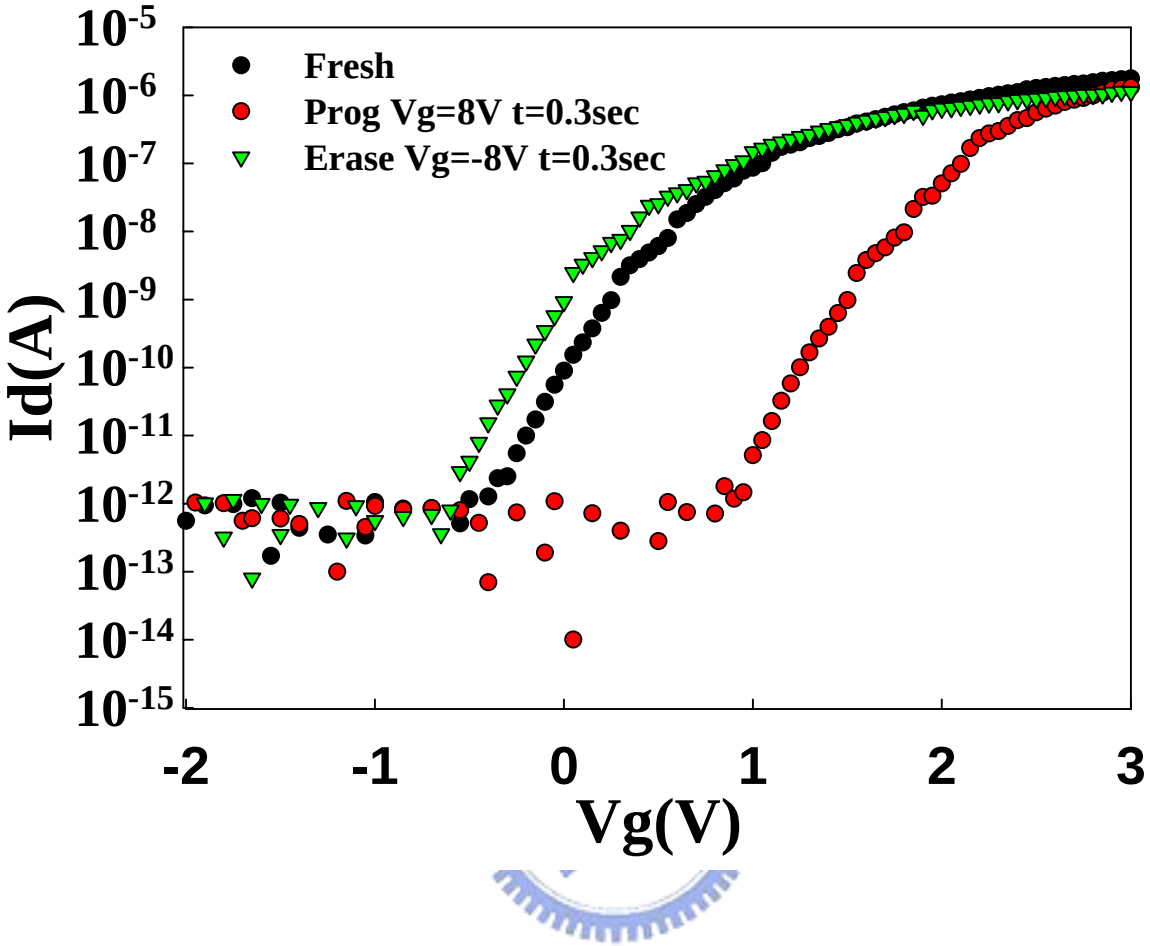
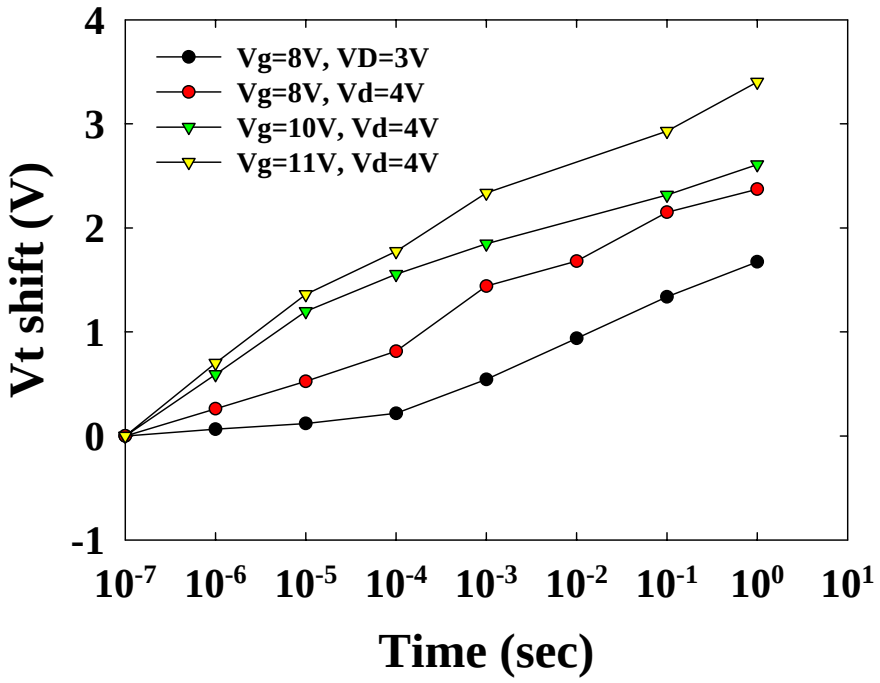
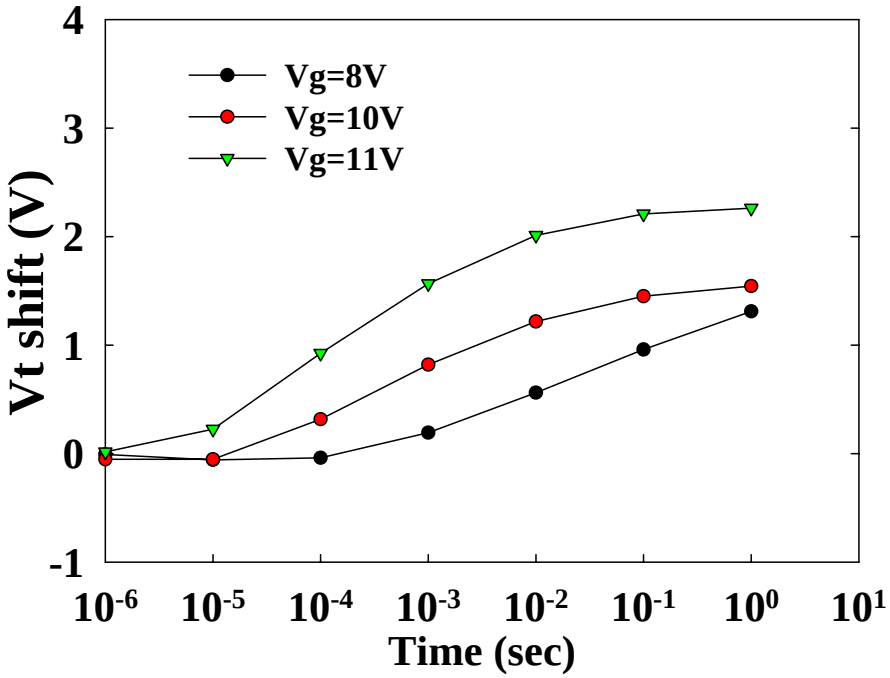


Fig. 2-4 show the Id-Vgs curves of the memory in the programmed/erased state. The programming and erasing times are 0.3 sec and a memory window of 2V can be achieved

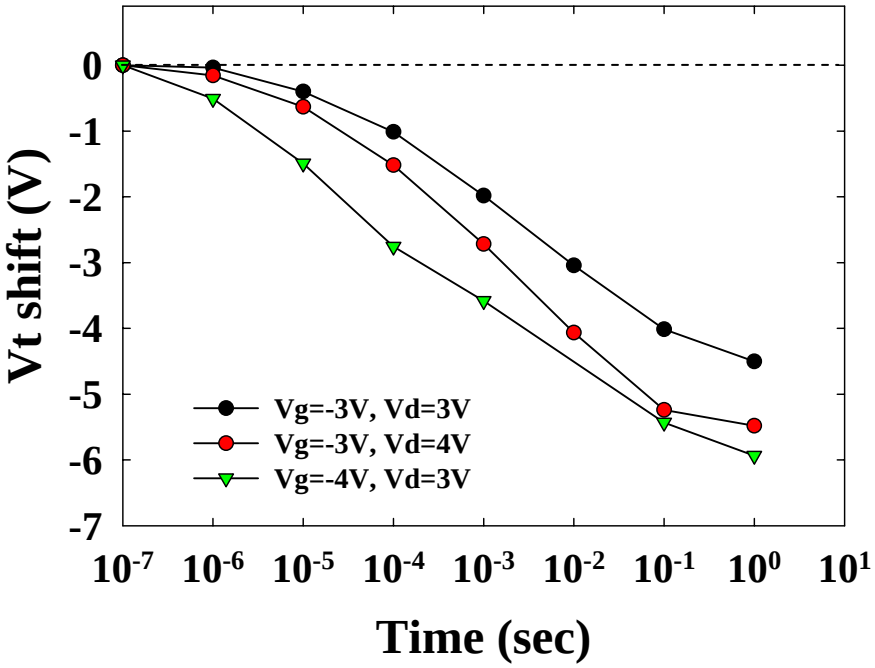


5(a)

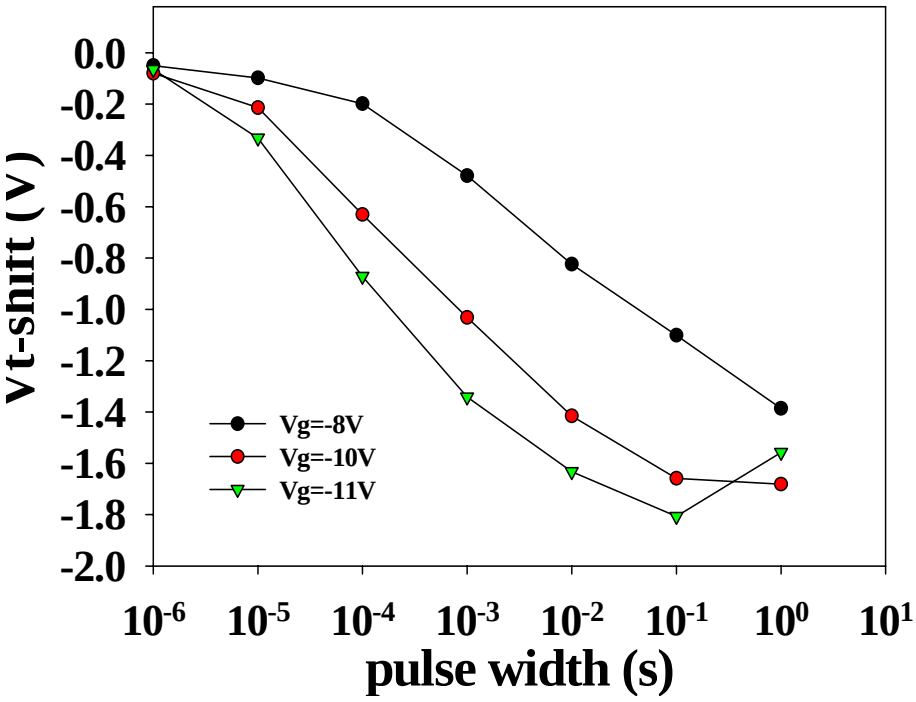


5(b)

Fig.2-5 Program characteristics of the memory devices with (a) CHE and (b) F-N programming .(a) A memory window of about 1.8V can be achieved with V_g=11V V_d=4V, and time=0.1ms for CHE programming operation. (b). A memory window of about 1.8V can be achieved with V_g=11V time=1ms for F-N programming operation.



6(a)



6(b)

Fig.2-6 Erase characteristics of the memory devices with (a) BTBHH and (b) F-N erasing conditions. The speed of BTBHH is faster than that of F-N method

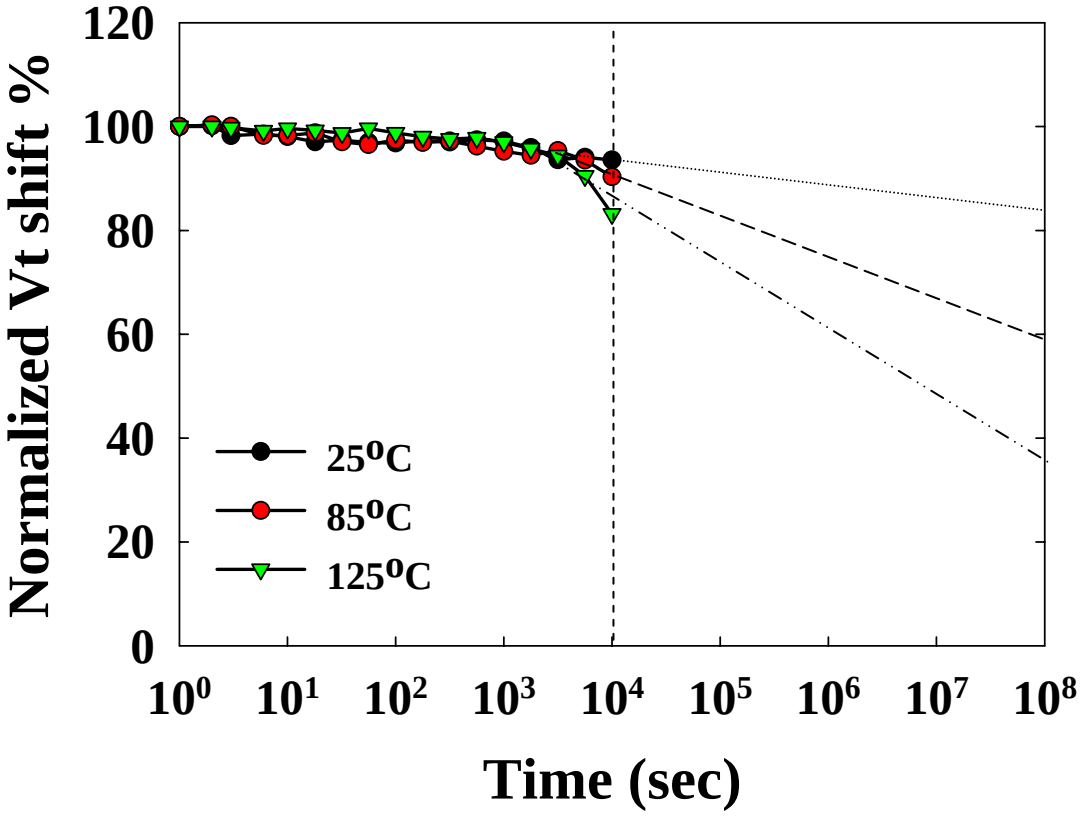


Fig.2-7 Retention characteristics of HfO_2 nanocrystal tri-gate memory devices at T=25°C, 85°C and 125°C. Very low charge loss is seen even after 10^4 seconds

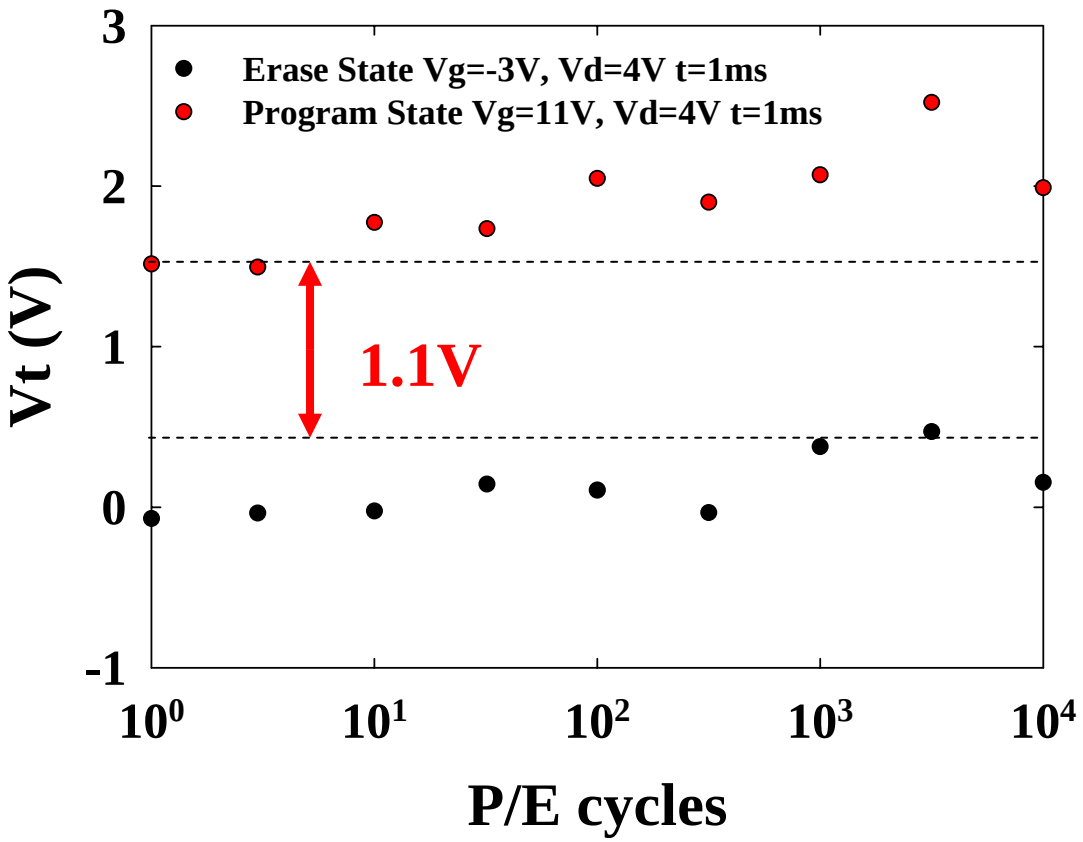


Fig. 2-8 Endurance characteristics of the HfO_2 nanocrystal tri-gate flash memory devices. Slight degradation is found after 10^3 P/E cycles

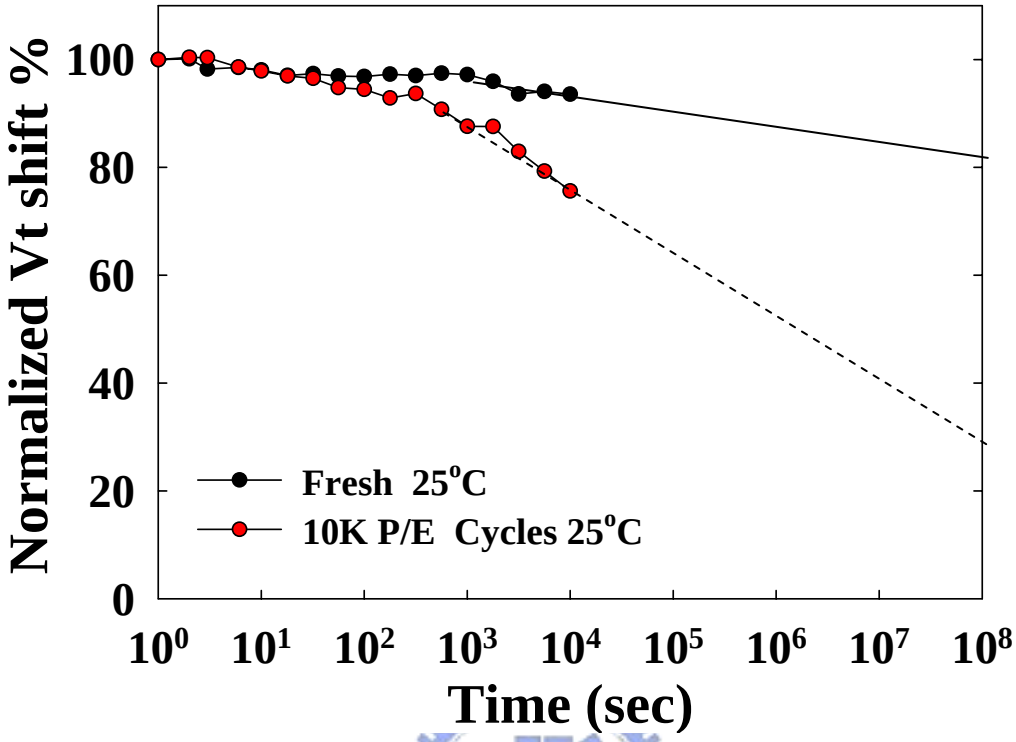


Fig.2-9 Retention characteristics of HfO_2 nanocrystal tri-gate memory devices with cycling and fresh at T=25°C.

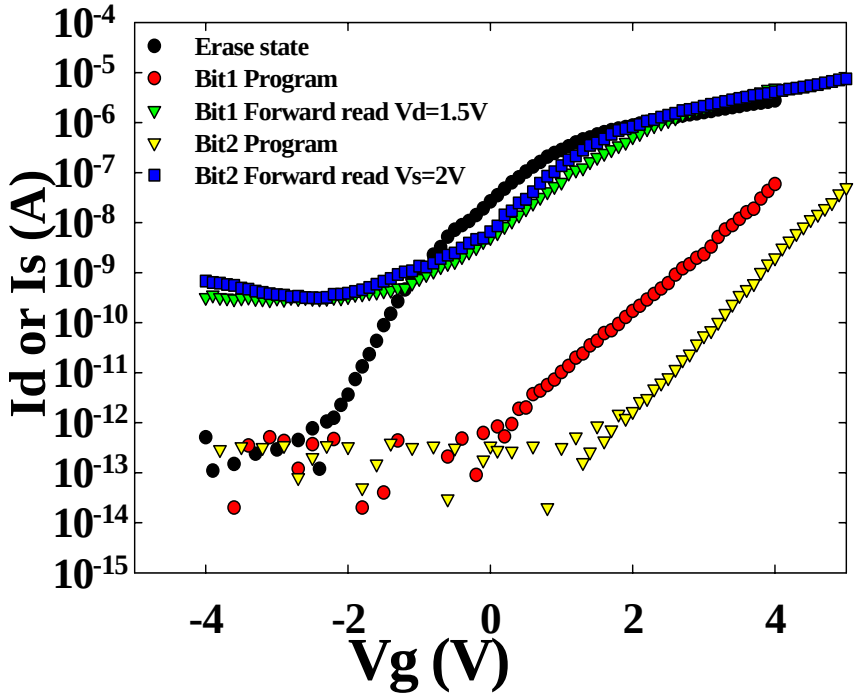
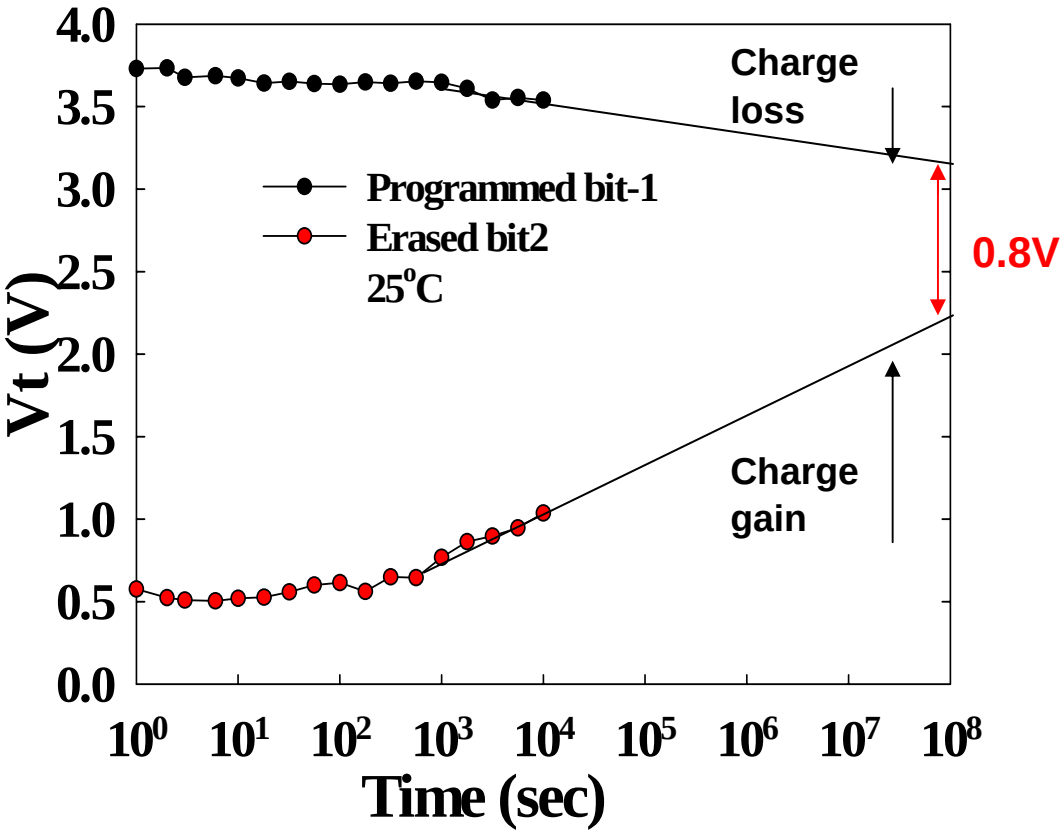


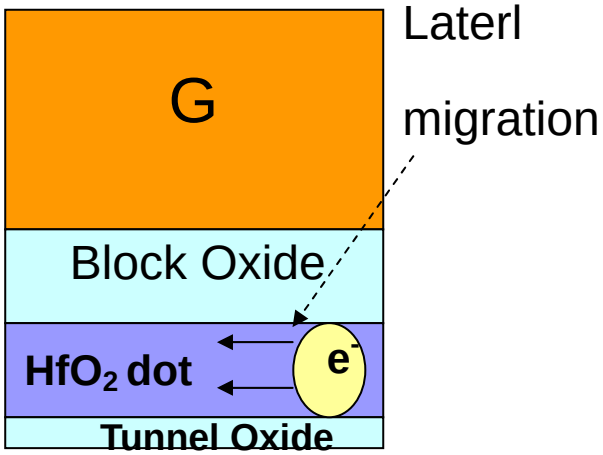
Fig. 2-10 Ids-Vgs curve of the memory in the 2-bit per cell operation. ; forward read and reverse read for programmed bit1 and programmed bit2

		Program	Erase	Read
Bit1	Vg	8V	-3V	1.5V
	Vd	4V	4V	0V
	Vs	0V	0V	>1.5V
Bit2	Vg	8V	-3V	1.5V
	Vd	0V	0V	>1.5V
	Vs	4V	4V	0V

Table.2-1 Operation principles and bias conditions utilized during the operation of the HfO_2 nanocrystal tri-gate Flash memory cell



(a)



(b)

Fig.2-11 Retention characteristics of the memory devices with Programmed bit-1 and Erased bit-2 at T=25°C. (b) show the schematic of Lateral migration.

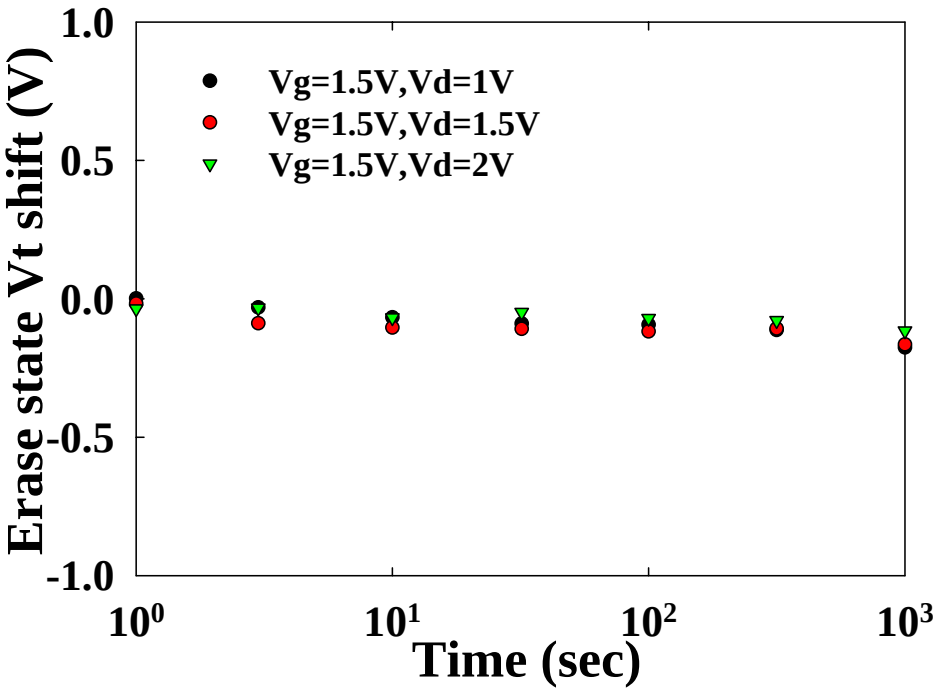


Fig. 2-12 Read disturbance characteristics of the HfO_2 nanocrystal tri-gate flash memory. No significant V_t shift occurred for $V_d < 2$, even after 1000 s at 25 °C

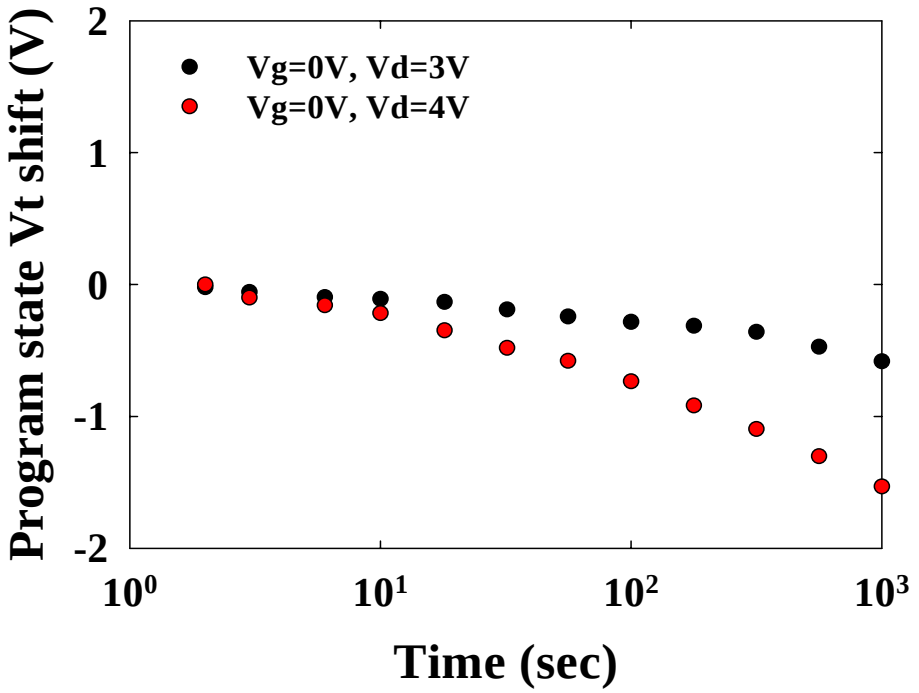


Fig. 2-13 Drain disturbance characteristics of the HfO_2 nanocrystal tri-gate flash memory cells. After 1000 s at 25 °C, a 1.5V drain disturb was observed for Vd=4V condition.

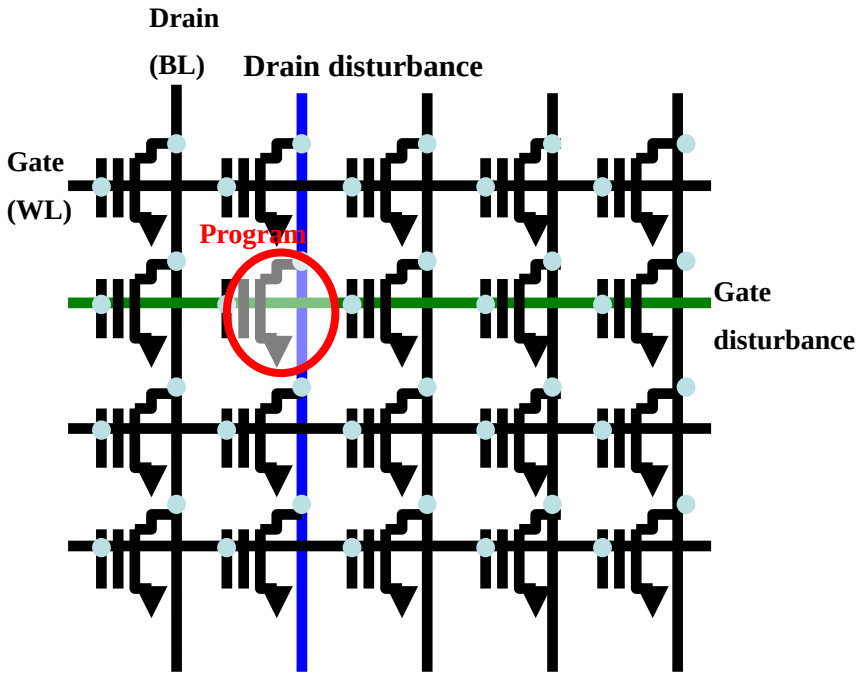


Fig. 2-14 The schematic illustration of disturb condition. When the cell is programming, those cell of the same word-line and the same bit-line are the gate disturb and drain disturb, respectively

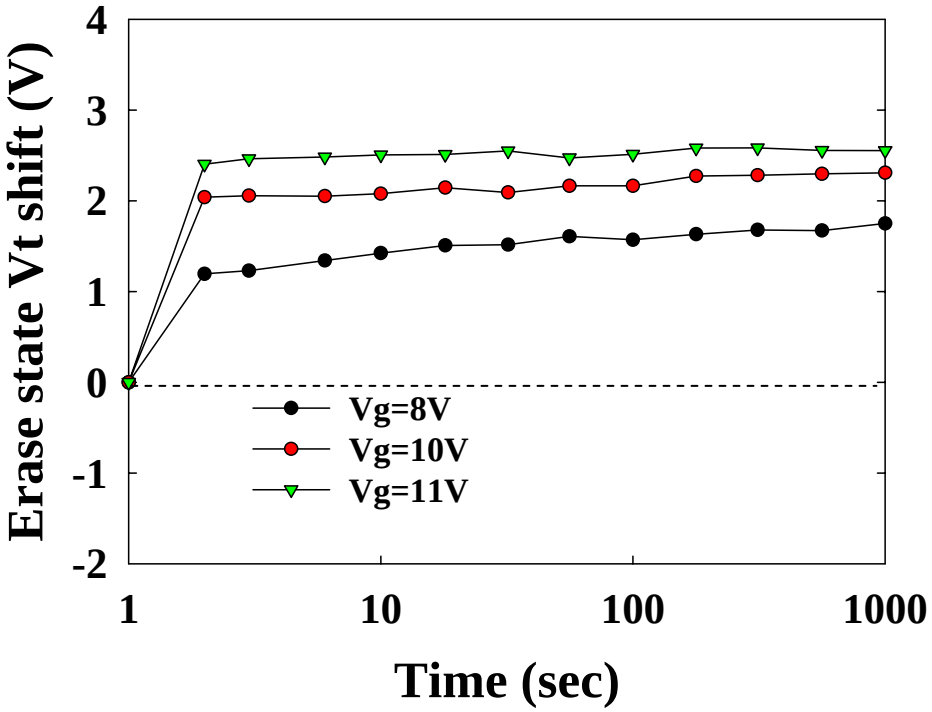


Fig. 2-15 Gate disturbance characteristics of the memory devices. A threshold voltage shift of 2.5 V occurred after stressing at V_g = 11 V and $V_s = V_d = V_{sub}$ = 0 V for 1000 s.

Chapter 3

Characteristic of SONOS-type Flash Memory by using La_2O_3 trapping layer

3.1 Introduction

In the field of nonvolatile semiconductor memory, there have been essentially two types of device structure. One is the floating gate structure and the other is the charge trap structure. The floating gate device store charge in the polycrystalline silicon as free charge with a continuous distribution in the conduction. In floating gate device, there are some problems in the scaling down. The floating gate device should use thick tunneling oxide, which is required to guarantee long charge retention time. Thus, they need high voltage operation for program and erase. Recently, silicon-oxide-nitride-oxide-silicon (SONOS) structure of charging device become attractive because they do not have planar scaling problem for floating gate isolation and they show great potential for achieving high program/erase speed, low programming voltage and low power performance [1]. Besides, the localized carrier trapping in the trapping layer makes a 2-bits operation possible. However, many concerning issues are still presented for SONOS memories. In recent years, many papers have ever shown Al_2O_3[2]trapping layer as the potential candidate for replacing Si_3N_4 [3] and also demonstrated different kinds of high-k[4-7] material to provide charge storage for the non-volatile memories.

In this work, we fabricate a high performance nonvolatile memory with a high-k charge-trapping layer. The high-k dielectric material is La_2O_3. This high-k layer replaces the silicon nitride layer in the SONOS structure. These materials provide

high trapping state densities and deep trapping levels, therefore they can enhance the retention of nonvolatile memories. The charge-trapping efficiency can be improved, and larger operation window can be achieved. The application of high-k materials can further reduce the operation voltage and potentially can help memory device scaling. It has good characteristics in terms of considerably large memory window, high speed program/erase, good retention time, good endurance, and good disturbance.

3-2 Experimental

Figure 3-1 schematically depicts the process flow of the proposed flash memory. First, the fabrication process of the Lanthanum oxide memory devices was started with LOCOS isolation process on a p-type, 5-10 Ω cm, (100) 150mm silicon substrates. First, a 2-nm-thick tunnel oxide was thermally grown at 1000°C in vertical furnace system. Next, a Lanthanum oxide layer was deposited by E-gun method with Lanthanum oxide targets. After that, the samples went through RTA treatment in O_2 ambient at 900°C for 1 minute. A blocking oxide of about 7-nm-thick was then deposited by high density plasma chemical vapor deposition (HDPCVD) followed by 900°C 1 minute N_2 densification process. Then, a 200-nm-tkick poly-Si was deposited to serve as the gate electrode by LPCVD. Then, the gate electrode was patterned and the source/drain (S/D) and gate were doped by self-aligned phosphorous ion implantation at the dosage and energy of $5x10^{15}$ ions/cm^{-2} and 20 KeV. Then the substrate contact was patterned and the sub-contact was implanted with BF_2 at the dosage and energy of $5x10^{15}$ ions/cm^{-2} and 40 KeV. Aftetr these implantations, the dopants were activated at 950^{o}C for 20 sec. The rest of the subsequent standard CMOS procedure were complete for fabricating the Lanthanum oxide high k memory devices.

3.3 Results and Discussion

3.3.1 Material Analysis of La_2O_3 SONOS type flash memory

Figure 3-2 shows the cross-sectional HRTEM images of the gate stacks of the La_2O_3 flash memories. For SONOS-type structure, the thicknesses of the tunnel oxide and blocking oxide layer are 2nm, 7nm, respectively. The La_2O_3 trapping layer thicknesses are 4nm. All devices described in this paper had dimensions of L/W = 2/1 μm.

3.3.2 Characteristics of Fresh Devices

Figure 3-3 shows the I_{ds}-V_{gs} curves of the La_2O_3 memory devices with programming time of 1s. Channel hot-electron injection and band-to-band hot-hole injection were employed for programming and erasing, respectively. A relatively large memory window of about 3V can be achieved at the V_g=V_d=10V program operation.

Program characteristics as a function of pulse width for different operation conditions are shown in Figure 3-4(a). Both source and substrate terminals were biased at 0V. The "V_t shift" is defined as the threshold voltage change of a device between the programmed and the erased states. With V_d=V_g=9V, relatively high speed (100μs) programming performance can be achieved with a memory window of about 2.2V. Meanwhile, Figure 3-4(b) displays the erase characteristics as a function of various operation voltages. Again, excellent erase speed of around 10 ms can be obtained. More important, there is only a very small amount of over-erase observed. The reason is owing to the fact that the vertical electric field decreases with decreasing amount of trapped electrons in the trapping layer during erasing and the hole injection into the trapping layer will reduce significantly [9].

Figure 3-5 illustrates the retention characteristics for comparing different temperature (T=25°C, 85°C, 125°C). The retention time of the memory with La_2O_3 trapping layer

can be up to 10^8 seconds for 22% charge loss at room temperature, which is believed to be related to the deep trap energy level in the high-κ dielectrics [10]. But the retention got worse as the temperature increased, 40% charge loss and 65% charge loss for the 85°C and 125°C s conditions have obtained up to 10^8 seconds [11–15].

The endurance characteristics after 10^4 P/E cycles are also shown in Figure 3-6. The programming and erasing conditions are $V_g=V_d=9V$ for 100μs and $V_g=-3V$, $V_d=10V$ for 1ms, respectively. Slight memory window narrowing has been displaye and the individual threshold voltage shifts in program and erase states become visible after 10^2 cycles. This indicates the formation of operation-induced trapped electrons [16] in the tunneling oxide or the mismatch between the localized spatial distributions for injected electron and holes by using channel hot-electron programming and band-to-band hot-hole erasing. The uncompensated electron, residual charges in the La_2O_3 layer, will then cause the Vt to increase gradually over P/E cycling [17].

The cycling retention is an important issue for flash memory. Therefore, we studied the retention loss behavior of the device before and after 100K cycling[18,19]. Figure 3-7 shows the cycling retention behavior of the cell at room temperature (25^oC) and high temperature (85^oC). As we can see in Figure 3-7, the charge loss behavior of the device with 100K cycling is more serious than the device without 100K cycling under room temperature condition. The retention time can be up to 10^8 seconds with 50% charge for cycling device. We ascribe these results to that the tunneling oxide was damage after100K P/E cycling. Hence, the trap assisted tunneling increase and the capability of charge storage was decreased.

3.3.3 Characteristics of 2-bit operation

Figure 3-8 demonstrates the feasibility of performing two-bit operation [20] with our La_2O_3 memories through a forward read and reverse read scheme in a single cell.

From the I_{ds}–V_{gs} curves, it is clear that we could employ forward and reverse reads to detect the information stored in the programmed bit-1 and bit-2, respectively. The read operation was achieved using a reverse read scheme. Table 1 summarizes the bias conditions for two-bit operation. Figure 3-9 shows the 2-bit retention characteristics of the La_2O_3 trapping layer. The retention time can be up to 10^8 seconds with 1.2V memory window between programmed bit-1 and erased bit-2. We can see that charge loss occurred both for a programmed bit-1 and erased bit-2. This suggests that there is vertical migration of trapped electron [21].

3.3.4 Disturbance

Figure 3-10 shows the programming drain disturbance of our La_2O_3 Flash memory. Three different drain voltages (V_d = 5, 7 and 9 V) were applied in the programming drain disturbance measurements at room temperatures. We observed that a programming drain disturb exists (ΔV_t < 1 V), even after programming at a value of V_d of 9V under room temperature and after stressing for 1000 s. Figure 3-11 shows the gate disturbance characteristics in the erasing state. Gate disturbance may occur during programming for the cells sharing a common word-line while one of the cells is being programmed. We observed a threshold voltage shift of 1 V under the following conditions: V_g = 10 V; V_s = V_d = V_{sub} = 0 V; stressed for 1000 s. The poor drain disturbance and gate disturbance was due to non-optimized process, such as thinner blocking oxide and tunneling oxide.

Figure 3-12 show s the drain currents from a selected cell, in both programmed (Vg=4V, Vt=5.3V) and erased state (Vg=4V, Vt=3V), and the leakage current from an unselected cell (Vg=0V, Vt=3V) during the reading operation. The read current is more than six orders of magnitude larger than the leakage current, for read drain voltage up to 4V. Hence, the program state and erase state will not be erroneous

judgment. Figure 3-13 demonstrates the read disturbance induced erase-state threshold voltage instability in a localized La_2O_3 trapping storage Flash memory cell under several operation conditions. For two-bit operation, the applied bitline voltage in a reverse-read scheme must be sufficiently large (>2 V) to be able to "read through" the trapped charge in the neighboring bit. The read-disturb effect is the result of two factors: the word-line and the bit-line. The word-line voltage during read may enhance room temperature (RT) drift in the neighboring bit. On the other hand, a relatively large read bit-line voltage may cause unwanted channel hot-electron injection and, subsequently, result in a significant threshold voltage shift of the neighboring bit. In our measurements, the gate and drain biases were applied and the source was grounded. The results demonstrate clearly that almost no read disturbance occurred in our La_2O_3 Flash memory under low-voltage reading (V_g = 4 V; V_d = 2 V). Even for a larger memory window, we found that almost no read disturbance (ca. 0.1 V) can be observed after operation at V_d = 4 V after 1000 s at 25 °C.

3.4 Summary

In this paper, we have investigated the memory effect on the performance of the La_2O_3 SONOS-type memories. It has good characteristics in terms of large memory windows, high speed program/erase, good retention time, excellent endurance, and 2-bit operation. Hence, La_2O_3 are the candidates used for the trapping layers for the SONOS-type memories.

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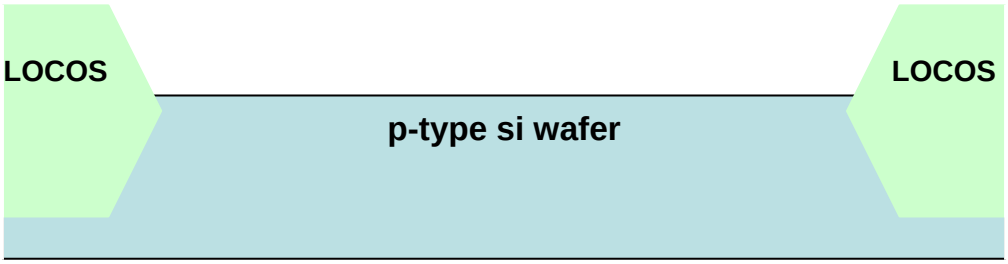
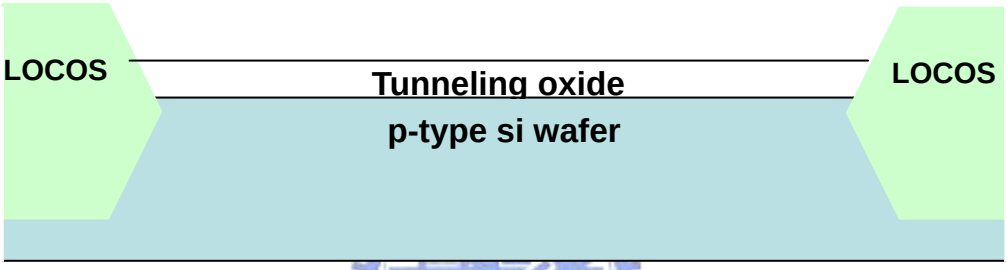
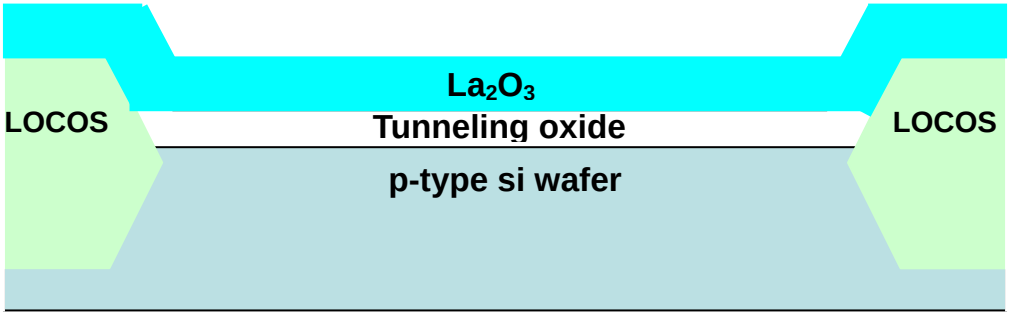


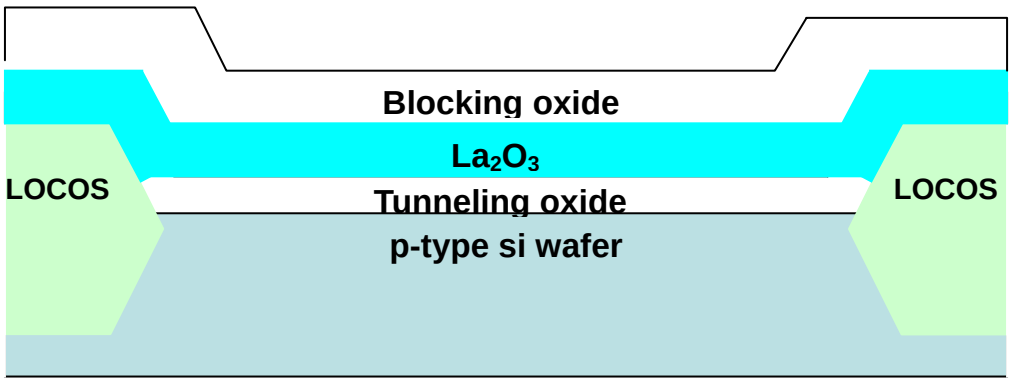
(a) LOCOS isolation on a p-type, 5-10 Ω cm, (100) 150mm silicon substrates



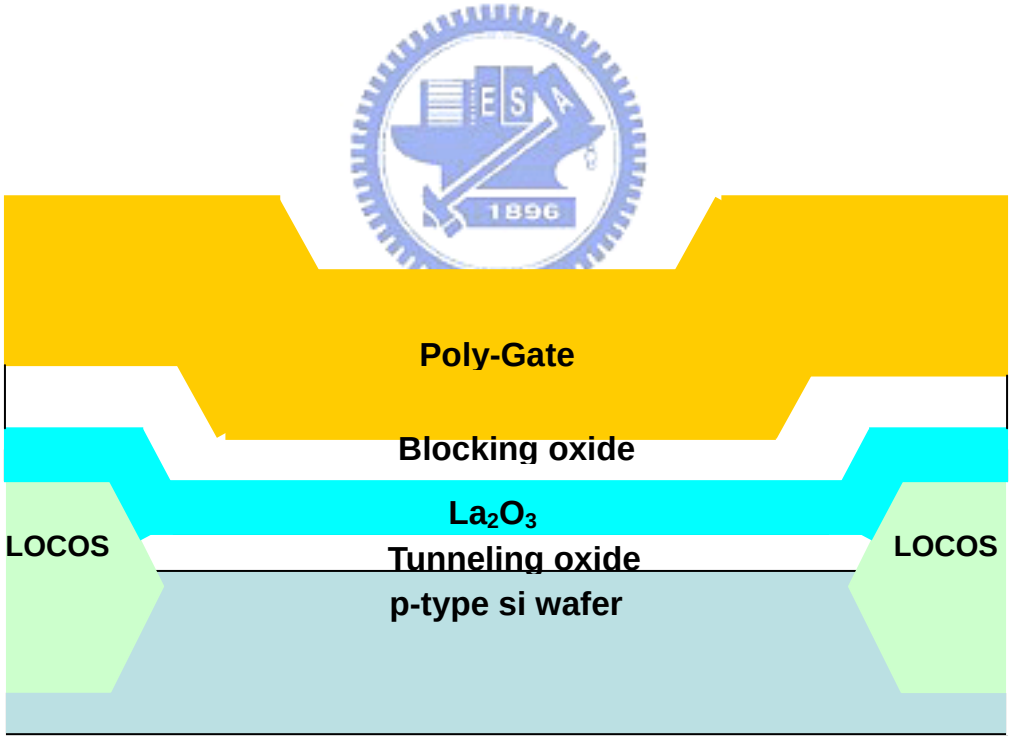
(b) Tunnel oxide was grown at 1000°C in furnace



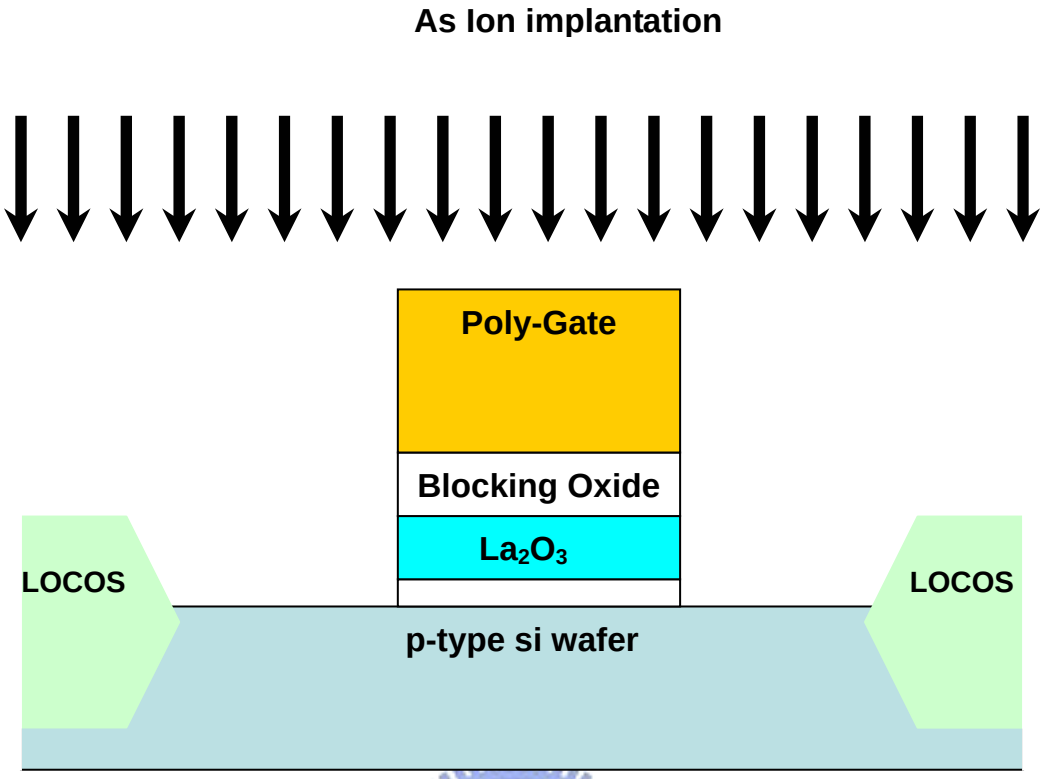
(c) Lanthanum oxide layer deposited by E-gun method as trapping layer



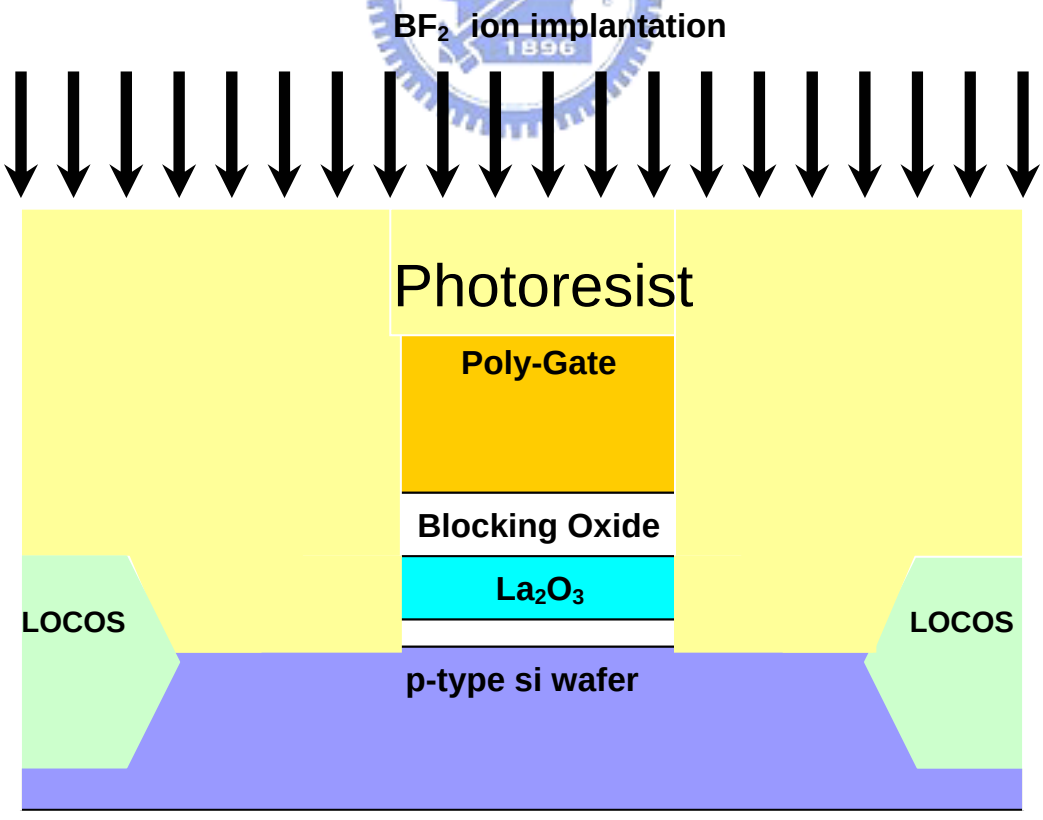
(d) RTA treatment in O_2 ambient at 900°C, blocking oxide then deposited by HDPCVD followed by 900°C in N_2 densification



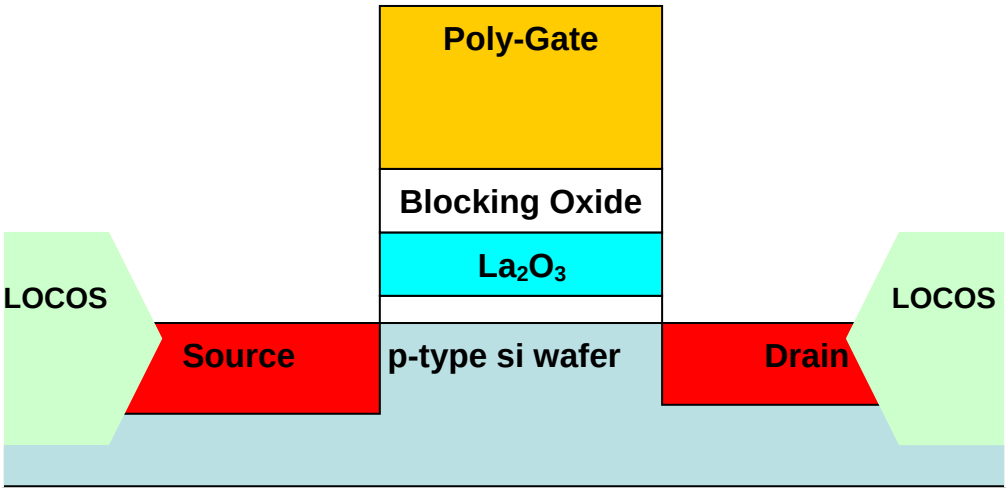
(e) Poly-Si deposited to serve as the gate electrode by LPCVD



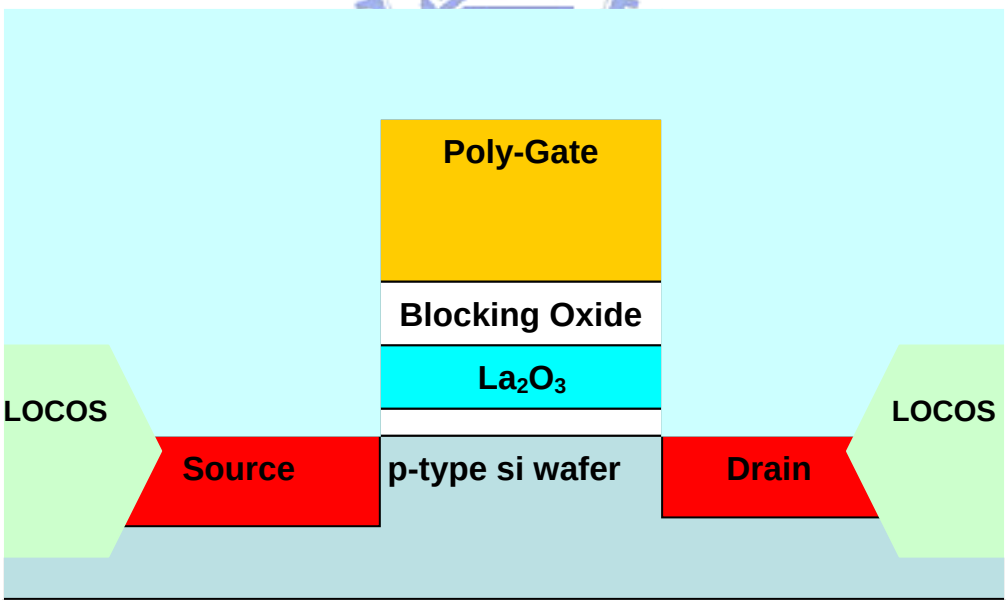
(f) Gate electrode patterned and the source/drain and gate implanted by self-aligned phosphorous ion implantation



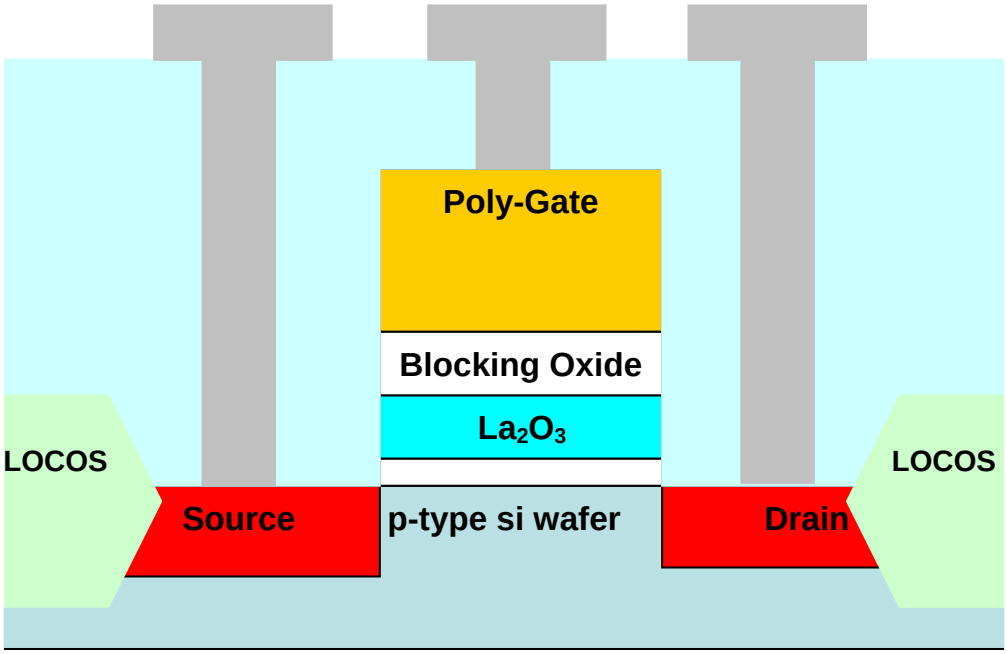
(g) Substrate contact patterned and the sub-contact was implanted with BF_2



(h) Dopants were activated at 950°C



(i)Deposition of passivation



(j)Contact hole opened and metal pads formation

Fig.3-1 Process flow of the proposed flash memory cell.

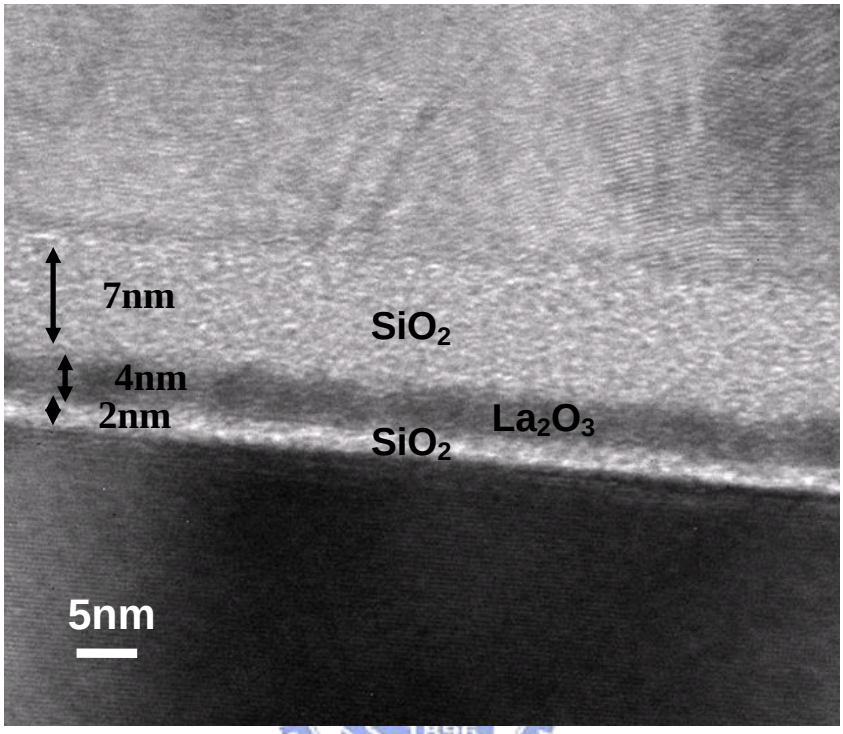


Fig.3-2 TEM image of the flash memory cell. The thickness of the O/N/O layers are 7/4/2 nm respectively.

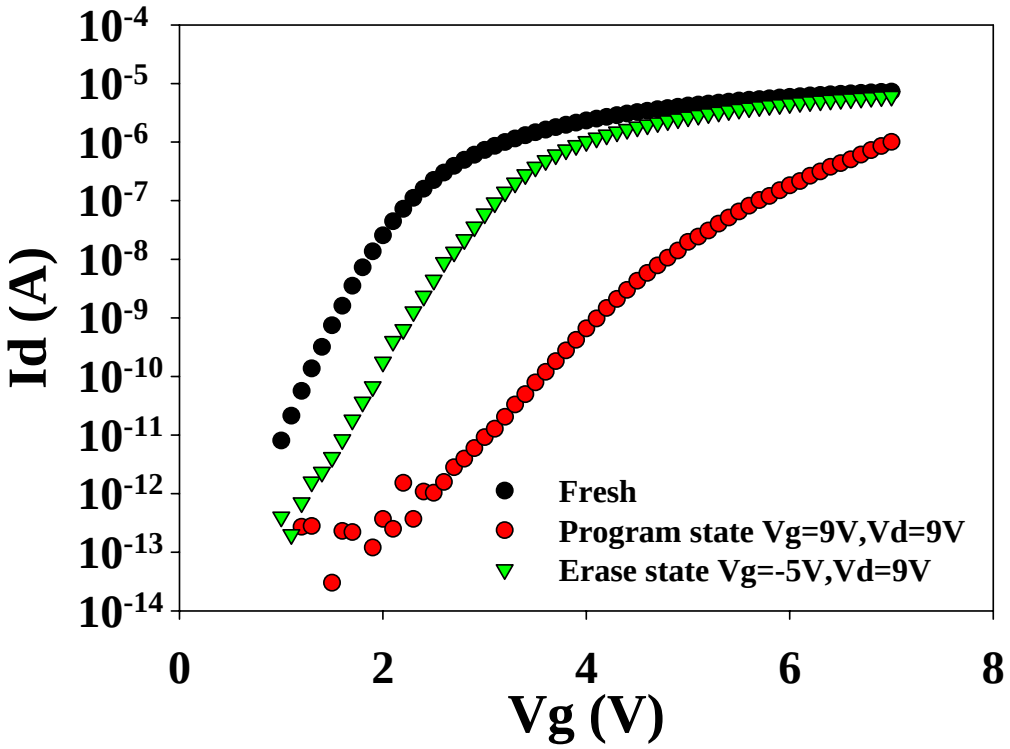
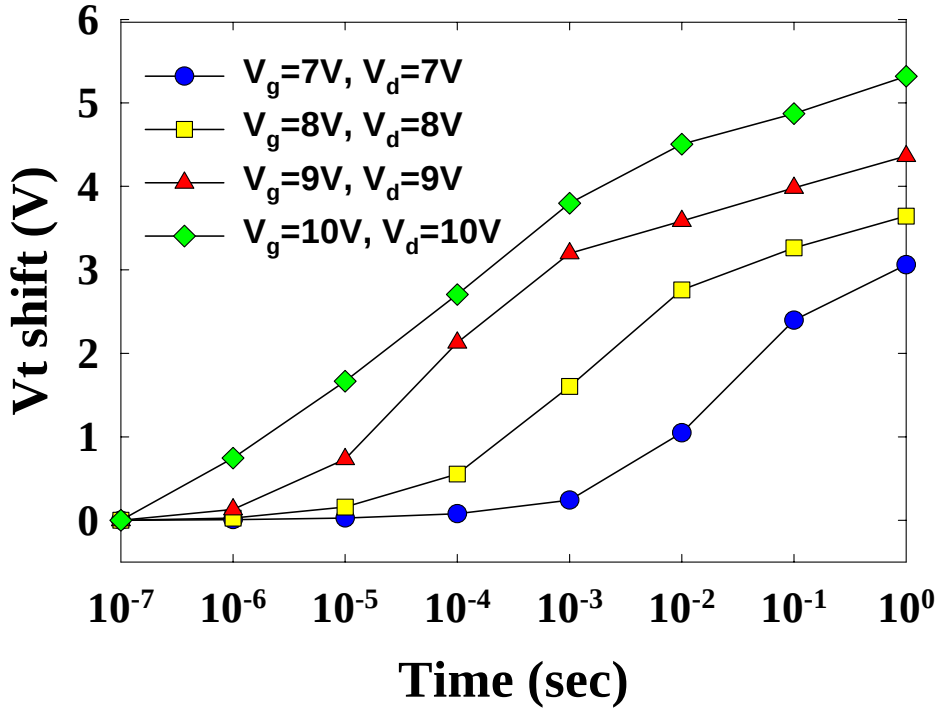
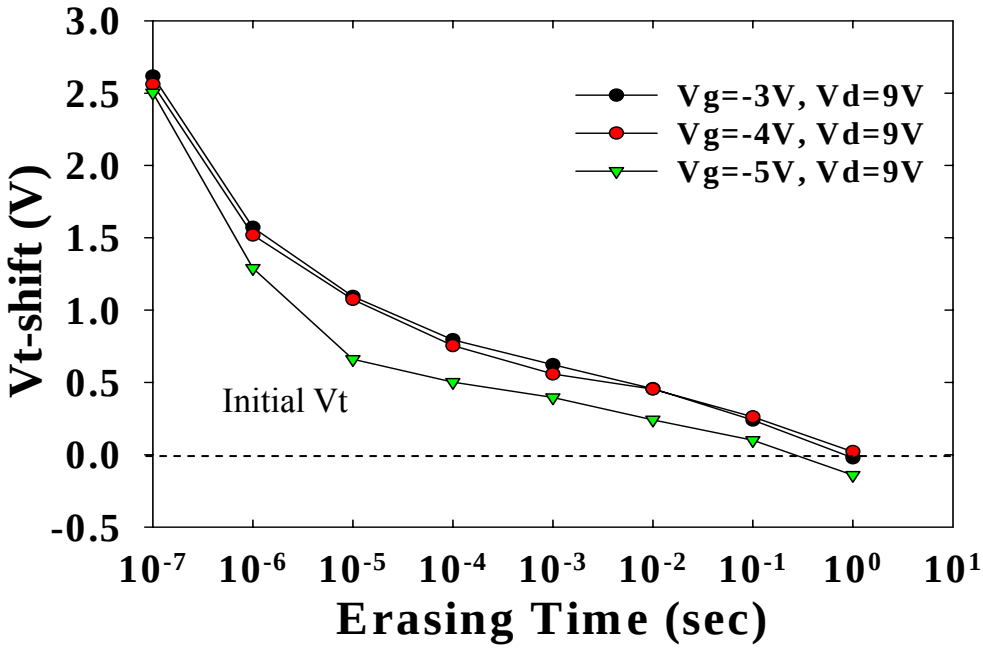


Fig. 3-3 I_{ds}-V_{gs} curves of the La_2O_3 memories. A memory window of larger than 3V can be achieved with V_g= V_d=9V programming operation



(a)



(b)

Fig.3-4 Program characteristics of the memory devices with different programming conditions. A memory window of about 3.5V can be achieved with V_g=V_d=10V, and time=1ms programming operation. (b). Erase characteristics of the memory devices with different erasing voltages.

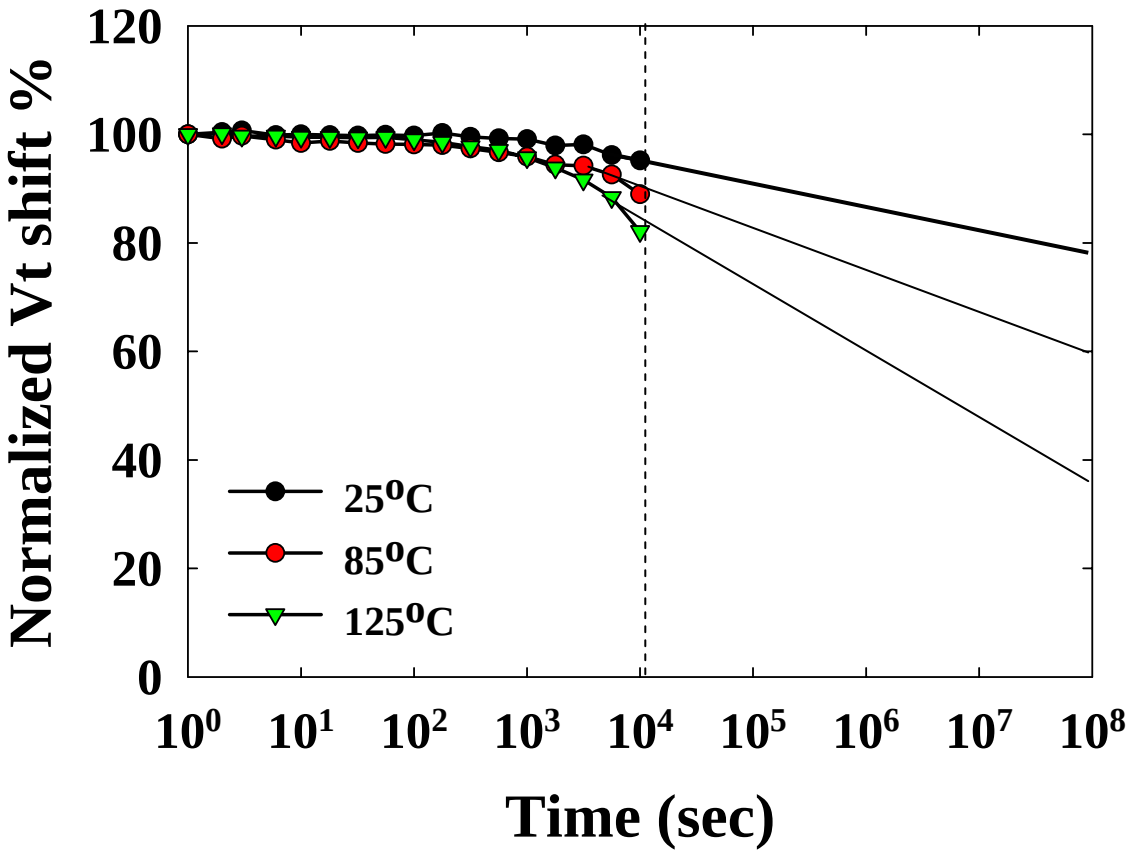


Fig.3-5 Retention characteristics of La_2O_3 memory devices at T=25°C, 85°C and 125°C. Very low charge loss is seen even after 10^4 seconds

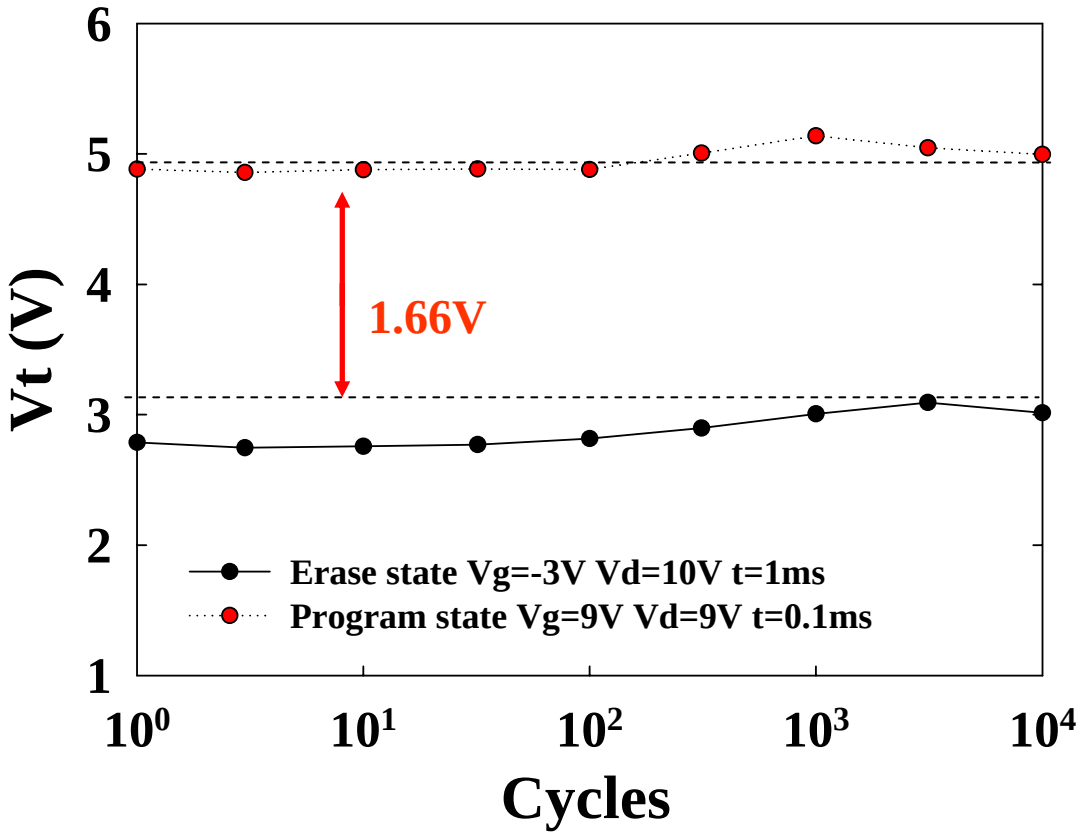


Fig. 3-6 Endurance characteristics of the La_2O_3 memory devices. Slight degradation is found after 10^2 P/E cycles

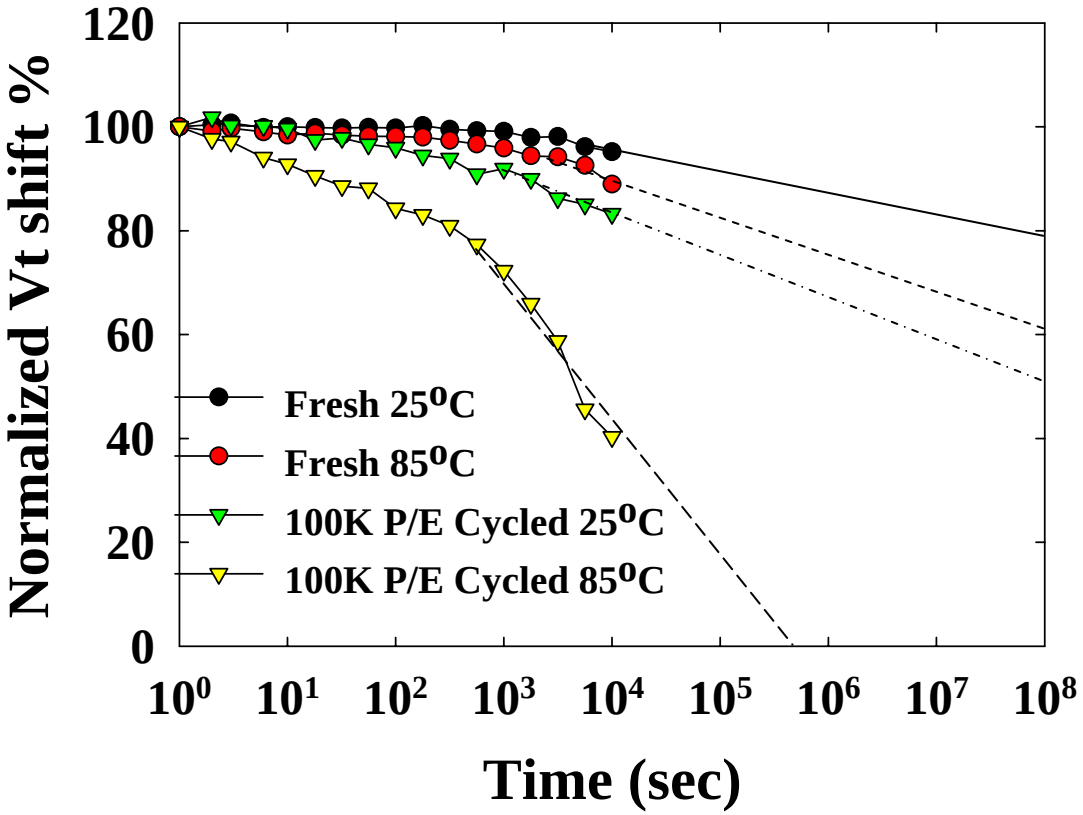


Fig.3-7 Retention characteristics of La_2O_3 memory devices with cycling and fresh at T=25°C, 85°C.

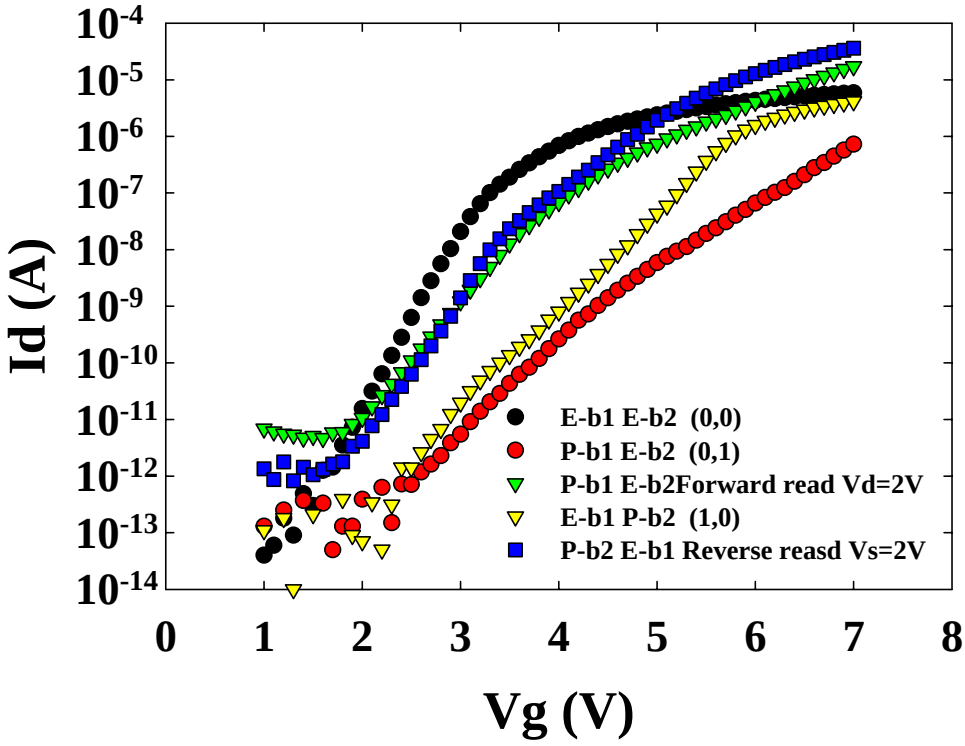
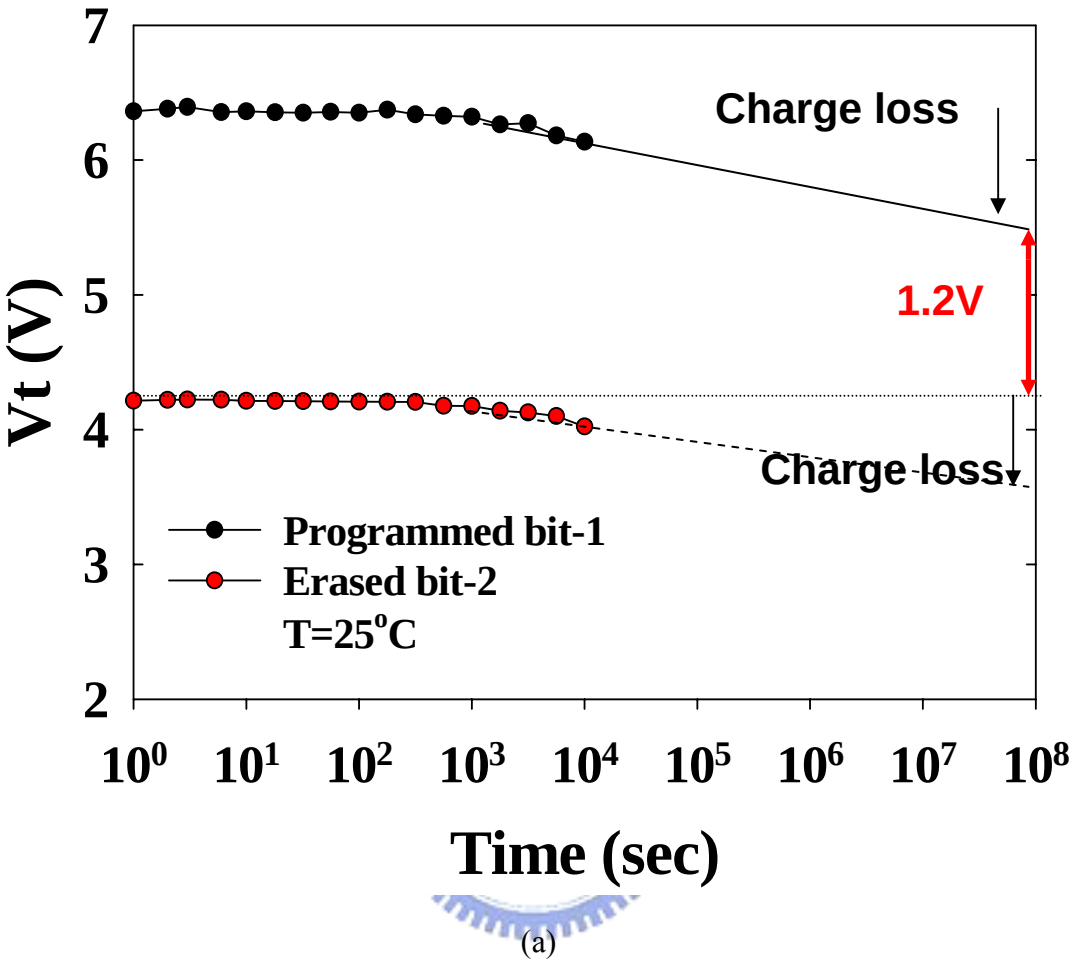


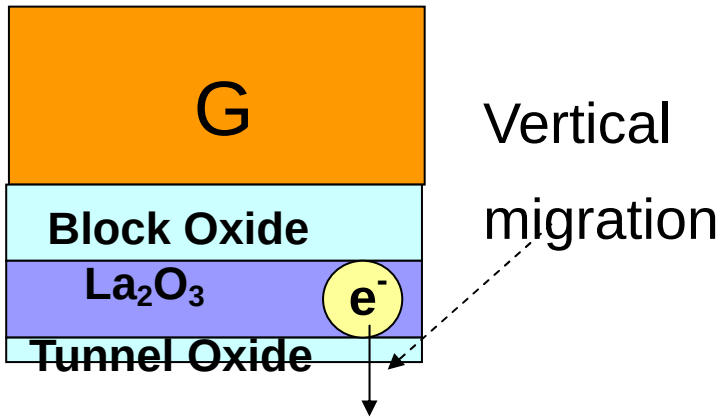
Fig.3-8 Ids-Vgs curve of the memory in the 2-bit per cell operation. ; forward read and reverse read for programmed bit1 and programmed bit2

		Program	Erase	Read
Bit1	Vg	9V	-3V	4V
	Vd	9V	10V	0V
	Vs	0V	0V	>2V
Bit2	Vg	9V	-3V	4V
	Vd	0V	0V	>2V
	Vs	9V	10V	0V

Table.3-1 Operation principles and bias conditions utilized during the operation of the La_2O_3 Flash memory cell



(a)



(b)

Fig.3-9 Retention characteristics of La_2O_3 memory devices with Programmed bit-1 and Erased bit-2 at T=25°C. (b) show the schematic of vertical migration.

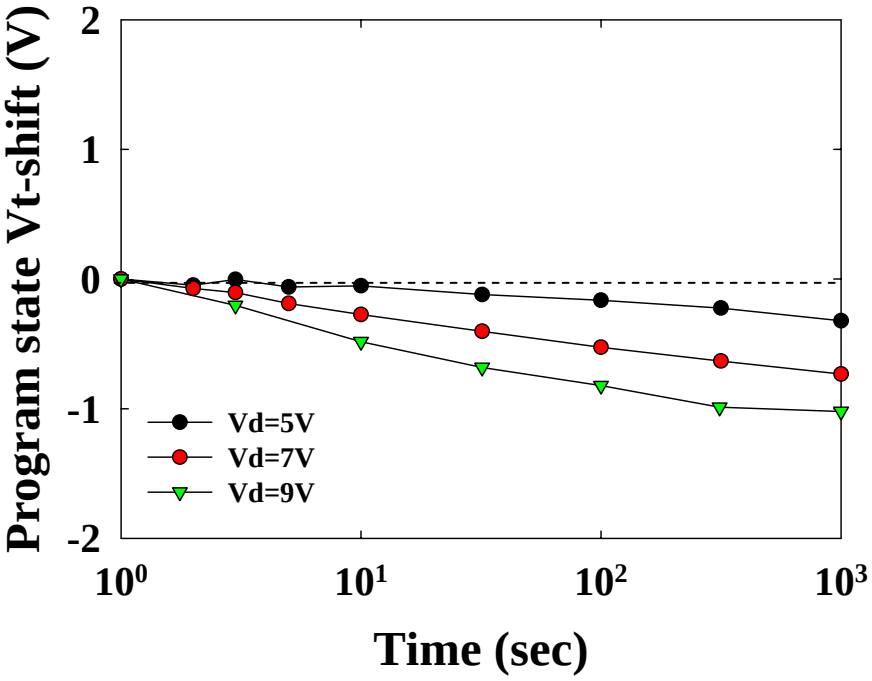


Fig. 3-10 Drain disturbance characteristics of the La_2O_3 memory cells. After 1000 s at 25 °C, only a 1V drain disturb was observed for Vd=9V condition.

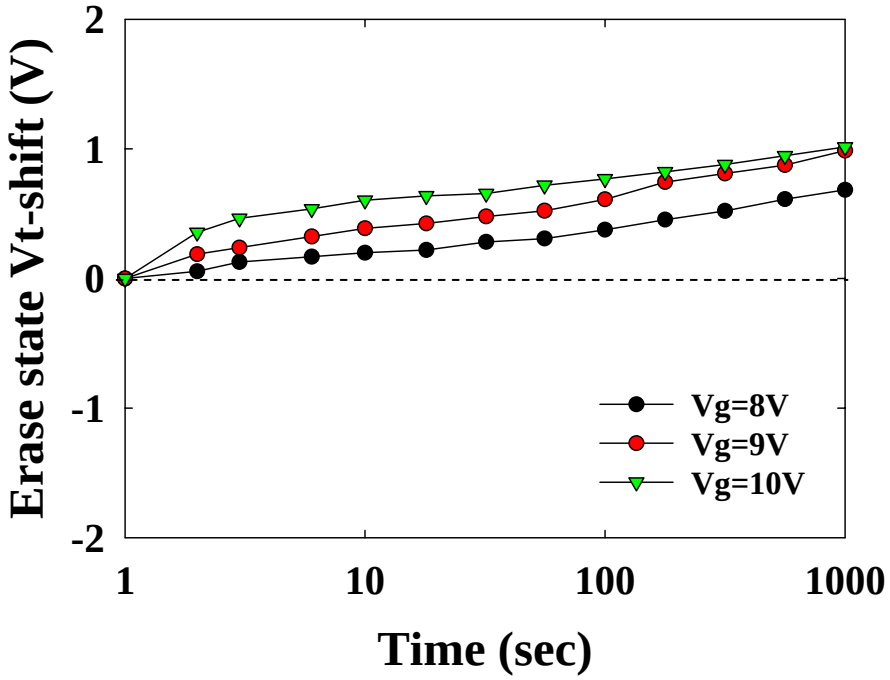


Fig. 3-11 Gate disturbance characteristics of the La_2O_3 memory devices. A threshold voltage shift of 1 V occurred after stressing at V_g = 10 V and $V_s = V_d = V_{sub}$ = 0 V for 1000 s.

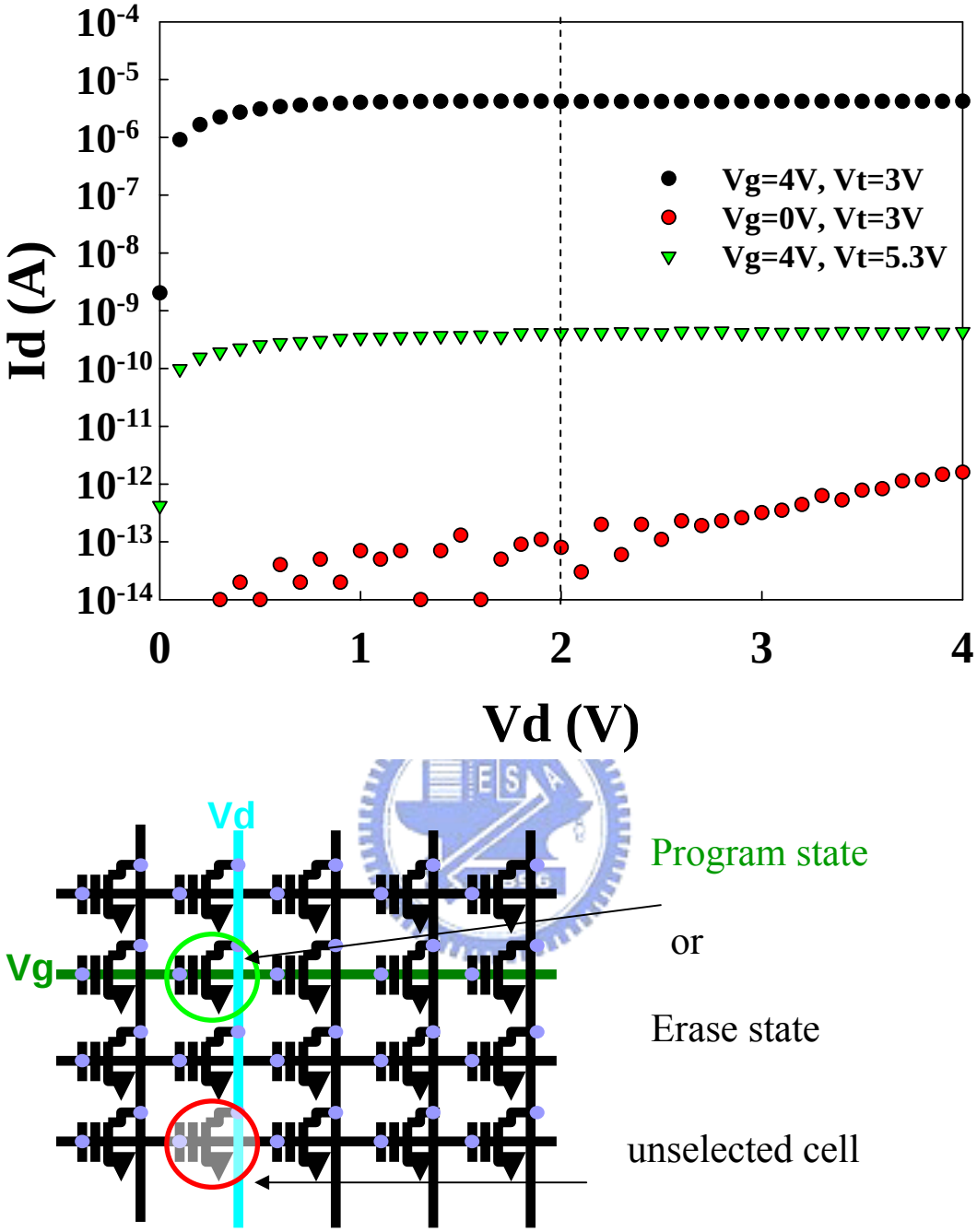


Fig. 3-12 Drain current comparison between the programmed cell, erased and unselected cell. Cell information can be read out at Vg=4V and Vd=2V.

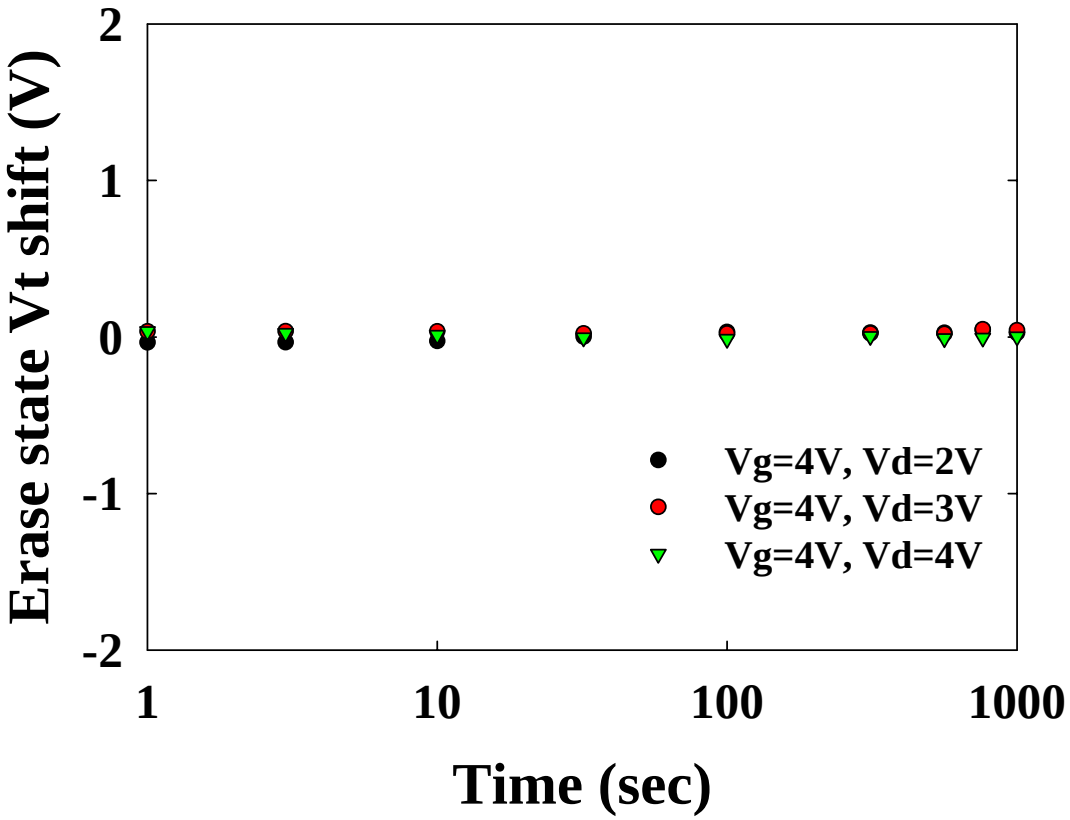


Fig. 3-13 Read disturbance characteristics of the La_2O_3 flash memory. No significant V_t shift occurred for $V_d < 4$, even after 1000 s at 25 °C.

Chapter 4

Characteristic of SONOS-type Flash Memory by using Pr_2O_3 trapping layer

4.1 Introduction

In floating gate device, there are some problems in the scaling down because that the floating gate device should use thick tunneling oxide, which is required to guarantee long charge retention time. Thus, they need high voltage operation for program and erase. Recently, silicon-oxide-nitride-oxide-silicon (SONOS) structure of charging device become attractive because they do not have planar scaling problem for floating gate isolation and they show great potential for achieving high program/erase speed, low programming voltage and low power performance [1]. However, many concerning issues are still presented for SONOS memories. In recent years, many papers have shown different kinds of high-k [2-5] trapping layer as the potential candidate for replacing Si_3N_4 [6,7] to provide charge storage for the non-volatile memories.

In this work, we fabricate a high performance nonvolatile memory with a high-k charge-trapping layer. The high-k dielectric material is Pr_2O_3. These materials provide high trapping state densities, therefore the charge-trapping efficiency can be improved, and larger operation window can be achieved. The application of high-k materials can further reduce the operation voltage and potentially can help memory device scaling. It has good characteristics in terms of considerably large memory window, high speed program/erase, good endurance, and good disturbance.

4-2 Experimental

Figure 4-1 schematically depicts the process flow of the proposed flash memory. First, the fabrication process of the Praseodymium oxide memory devices was started with LOCOS isolation process on a p-type, 5-10 Ω cm, (100) 150mm silicon substrates. First, a 2-nm-thick tunnel oxide was thermally grown at 1000°C in vertical furnace system. Next, a Praseodymium oxide layer was deposited by E-gun method with Praseodymium oxide targets. After that, the samples went through RTA treatment in N_2O ambient at 900°C for 1 minute. A blocking oxide of about 10-nm-thick was then deposited by high density plasma chemical vapor deposition (HDPCVD) followed by 900°C 1 minute N_2 densification process. Then, a 200-nm-tkick poly-Si was deposited to serve as the gate electrode by LPCVD. Then, the gate electrode was patterned and the source/drain (S/D) and gate were doped by self-aligned phosphorous ion implantation at the dosage and energy of $5x10^{15}$ ions/cm^{-2} and 20 KeV. Then the substrate contact was patterned and the sub-contact was implanted with BF_2 at the dosage and energy of $5x10^{15}$ ions/cm^{-2} and 40 KeV. Aftetr these implantations, the dopants were activated at 950^{o}C for 20 sec. The rest of the subsequent standard CMOS procedure were complete for fabricating the Lanthanum oxide high k memory devices.

Figure 4-2 shows the cross-sectional of the gate stacks of the La_2O_3 flash memories.

4.3 Results and Discussion

4.3.1 Characteristics of Fresh Devices

For the operation of our Pr_2O_3 memories, we employed channel hot-electron injection[8] and band-to-band hot-hole injection for the programming and erasing, respectively. All devices described in this paper had dimensions of L/W = 2/2 μm.

Program characteristics as a function of pulse width for different operation conditions are shown in Figure 4-3(a). Both source and substrate terminals were biased at 0V. The "V_t shift" is defined as the threshold voltage change of a device between the programmed and the erased states. With V_d=V_g=8V, relatively high speed (100μs) programming performance can be achieved with a memory window of about 2V. Meanwhile, Figure 4-3(b) displays the erase characteristics as a function of various operation voltages. Again, excellent erase speed of around 10 ms can be obtained. More important, there is only a very small amount of over-erase observed. The reason is owing to the fact that the vertical electric field decreases with decreasing amount of trapped electrons in the trapping layer during erasing and the hole injection into the trapping layer will reduce significantly [9].

Figure 4-4 illustrates the retention characteristics for comparing different temperature (T=25°C and 85°C). The retention time of the memory with Pr_2O_3 trapping layer can be up to 10^4 seconds for 13% charge loss at room temperature and the retention got worse as the temperature increased, 50% charge loss for the 85°C conditions have obtained up to 10^4 seconds [10–14].

The endurance characteristics after 10^4 P/E cycles are also shown in Figure 4-5. The programming and erasing conditions are V_g=V_d=9V for 100μs and V_g=-3V, V_d=10V for 1ms, respectively. Slight memory window narrowing has been displaye and the individual threshold voltage shifts in program and erase states become visible after 10^2 cycles. This indicates the formation of operation-induced trapped electrons [15] in the tunneling oxide or the mismatch between the localized spatial distributions for injected electron and holes by using channel hot-electron programming and band-to-band hot-hole erasing. The uncompensated electron, residual charges in the La_2O_3 layer, will then cause the Vt to increase gradually over P/E cycling [16].

4.3.2 Disturbance

Figure 4-6 shows the programming drain disturbance of our Pr_2O_3 Flash memory. Three different drain voltages (V_d = 5, 7 and 9 V) were applied in the programming drain disturbance measurements at room temperatures. We observed that a large programming drain disturb margin exists (ΔV_t < 1.5 V), after programming at a value of V_d of 9V under room temperature and after stressing for 1000 s. Figure 4-7 shows the gate disturbance characteristics in the erasing state. Gate disturbance may occur during programming for the cells sharing a common word-line while one of the cells is being programmed. We observed a threshold voltage shift of 0.25V under the following conditions: V_g = 10 V; $V_s = V_d = V_{sub}$ = 0 V; stressed for 1000 s. Because of the small voltage drop at the tunnel oxide due to thicker block oxide, this memory can exhibit such good gate disturb characteristics with such a thin tunnel oxide.

Figure 4-8 demonstrates the read disturbance induced erase-state threshold voltage instability in a localized Pr_2O_3 trapping storage Flash memory cell under several operation conditions. The read-disturb effect is the result of two factors: the word-line and the bit-line. The word-line voltage during read may enhance room temperature (RT) drift in the neighboring bit and a relatively large read bit-line voltage may cause unwanted channel hot-electron injection, subsequently, result in a significant threshold voltage shift of the neighboring bit. In our measurements, the gate and drain biases were applied and the source was grounded. The results demonstrate clearly that almost no read disturbance occurred in our Pr_2O_3 Flash memory under low-voltage reading (V_g = 4 V; V_d = 2 V). Even for a larger memory window, we found that almost no read disturbance (ca. 0.1 V) can be observed after operation at V_d = 4 V after 1000 s at 25 °C.

In table 4-1, we summarized the results of the above two experiments. From the

table, we can find that Pr_2O_3 devices have better performance than La_2O_3 devices except poor retention. Pr_2O_3 devices have faster program speed may be due to its higher trapping efficiency such as Figure 4-9.

4.4 Summary

In this paper, we have investigated the memory effect on the performance of the Pr_2O_3 SONOS-type flash memories. It has good characteristics in terms of large memory windows, high speed program/erase, excellent endurance, but poor retention. Hence, Pr_2O_3 may be the candidates used for the trapping layers for the SONOS-type memories, if the retention was improved by using thicker tunneling oxide.

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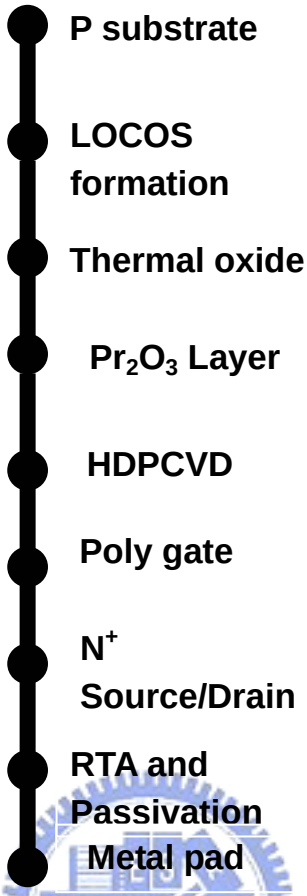


Fig.4-1 Process flow of the proposed flash memory cell

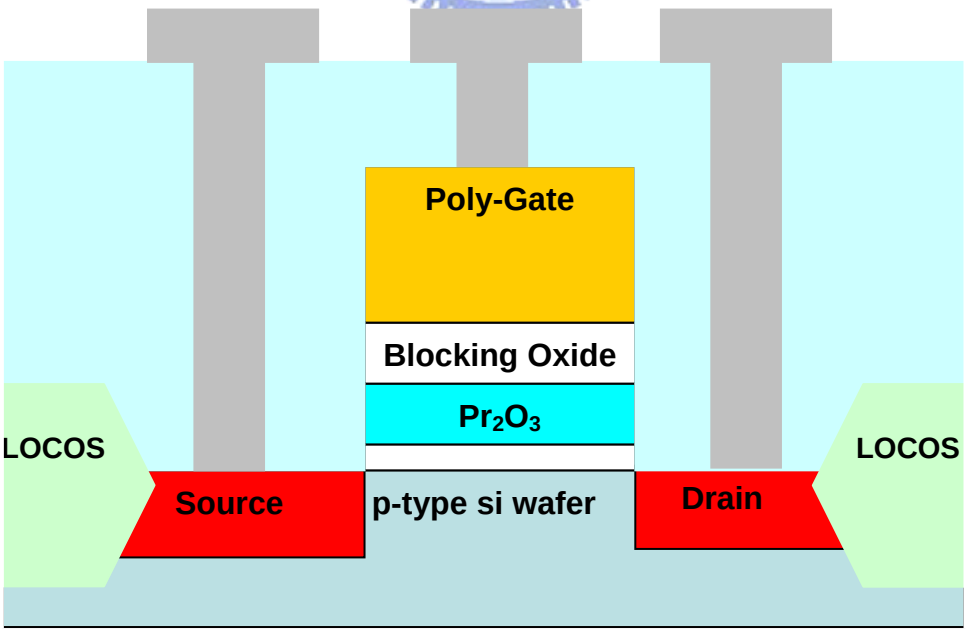
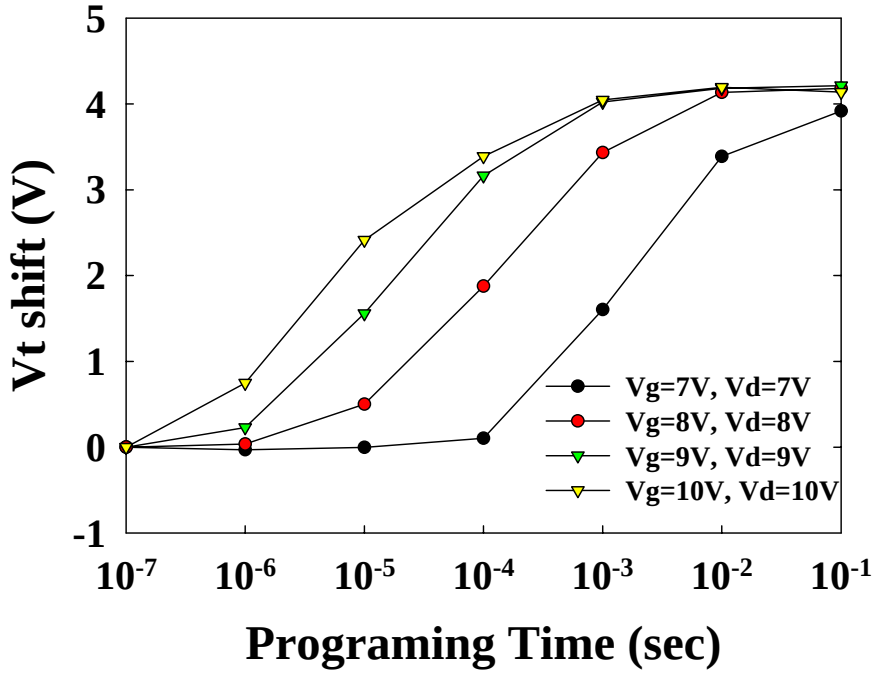
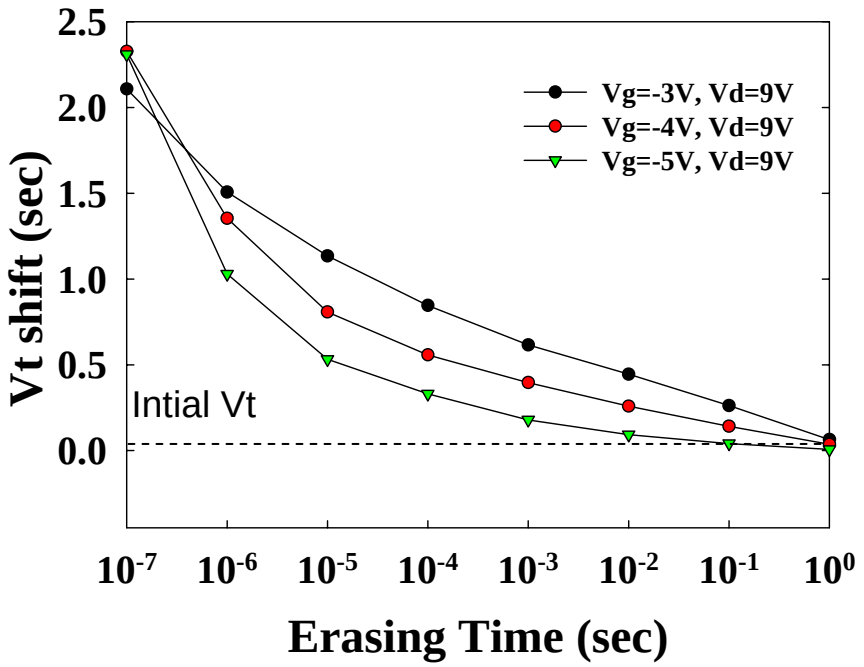


Fig.4-2 Cross-section of the proposed flash memory cell.



(a)



(b)

Fig.4-3 Program characteristics of the memory devices with different programming conditions. A memory window of about 3.5V can be achieved with V_g=V_d=10V, and time=0.1ms programming operation. (b). Erase characteristics of the memory devices with different erasing voltages.

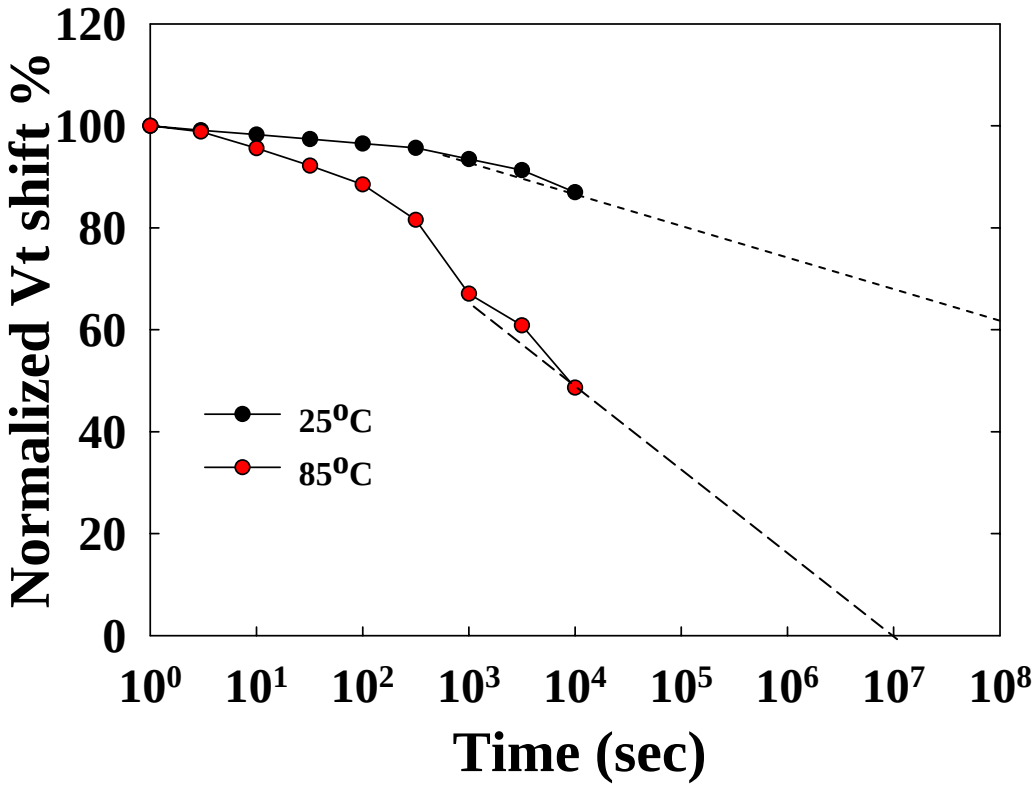


Fig.4-4 Retention characteristics of Pr_2O_3 memory devices at T=25°C and 85°C.

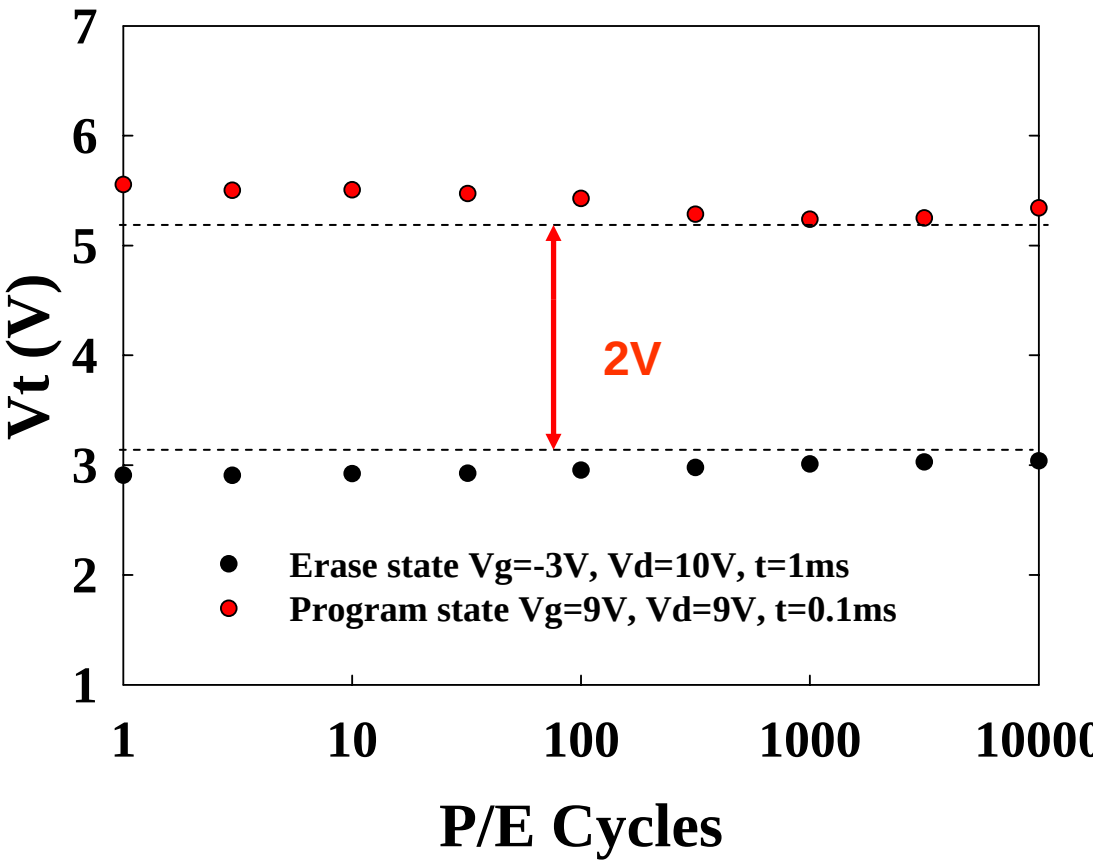


Fig. 4-5 Endurance characteristics of the Pr_2O_3 memory devices. Slight degradation is found after 10^2 P/E cycles

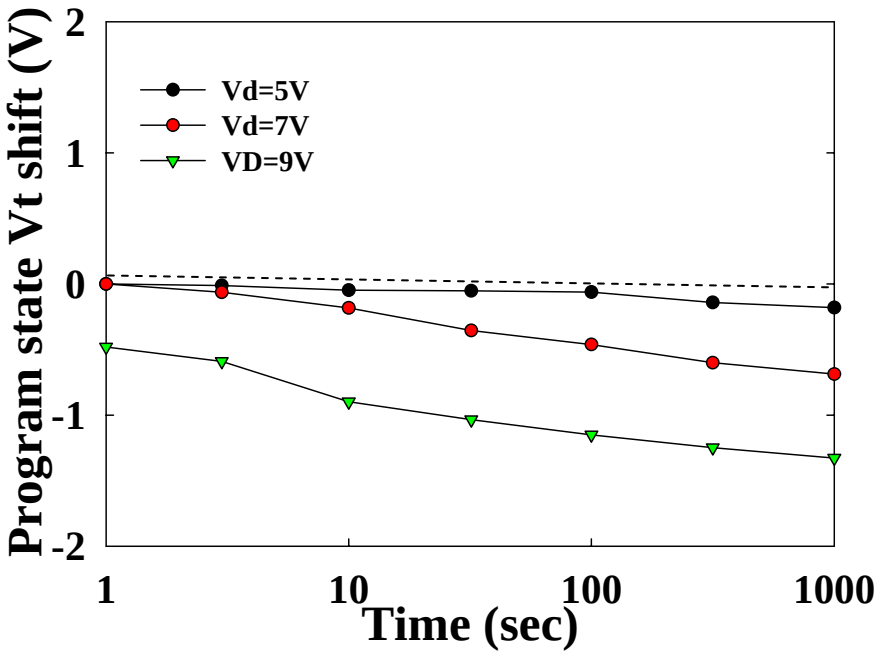


Fig. 4-6 Drain disturbance characteristics of the Pr_2O_3 memory cells. After 1000 s at 25 °C, 1.5V drain disturb was observed for Vd=9V condition.

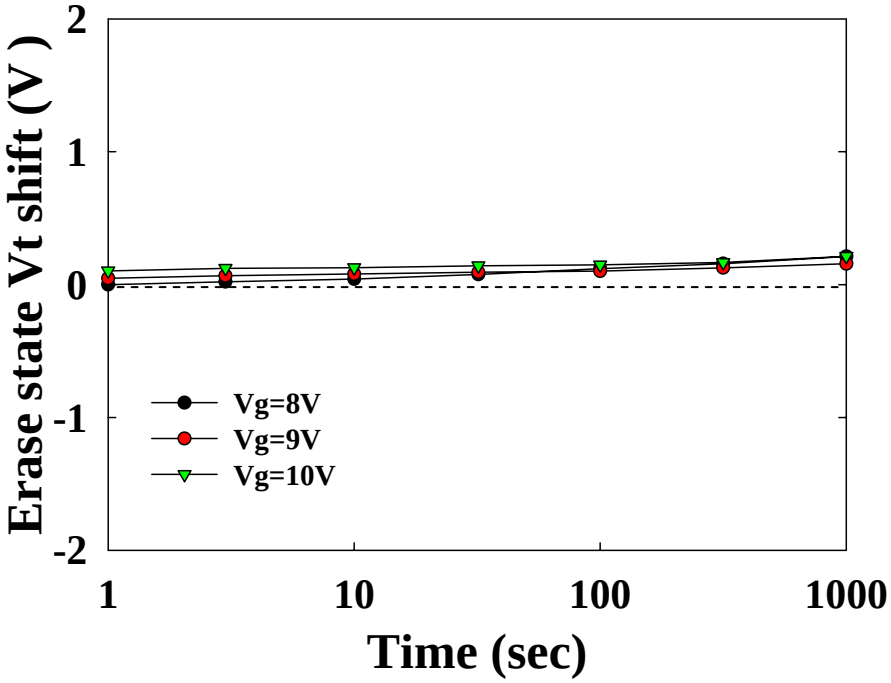


Fig. 4-7 Gate disturbance characteristics of the Pr_2O_3 memory devices. A threshold voltage shift of 0.25 V occurred after stressing at V_g = 10 V and $V_s = V_d = V_{sub}$ = 0 V for 1000 s.

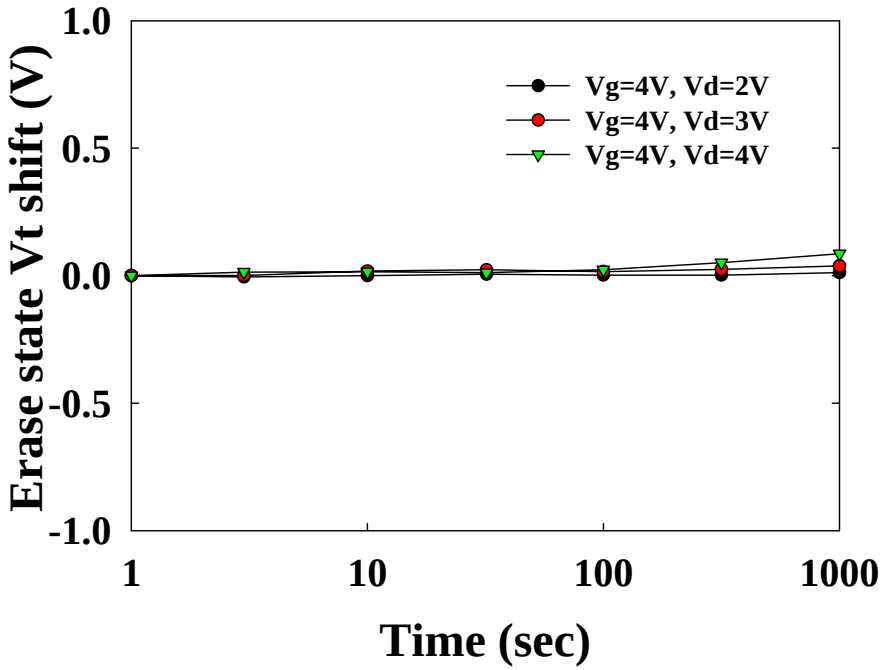


Fig. 4-8 Read disturbance characteristics of the Pr_2O_3 flash memory. Slight V_t shift occurred for $V_d < 4$, after 1000 s at 25 °C.

	Program Speed (2Vwindow)	**Erase Speed (2V window)**	**Retention (20%loss @25°C)**	**Endurance (10k P/E cycles)**
La_2O_3 Device	100μs	1ms	10^8sec	good
Pr_2O_3 device	10~100μs	0.1ms	10^5~10^6sec	good

Table 4-1 The summary of performance for La_2O_3 and Pr_2O_3 SONOS-like Flash memory.

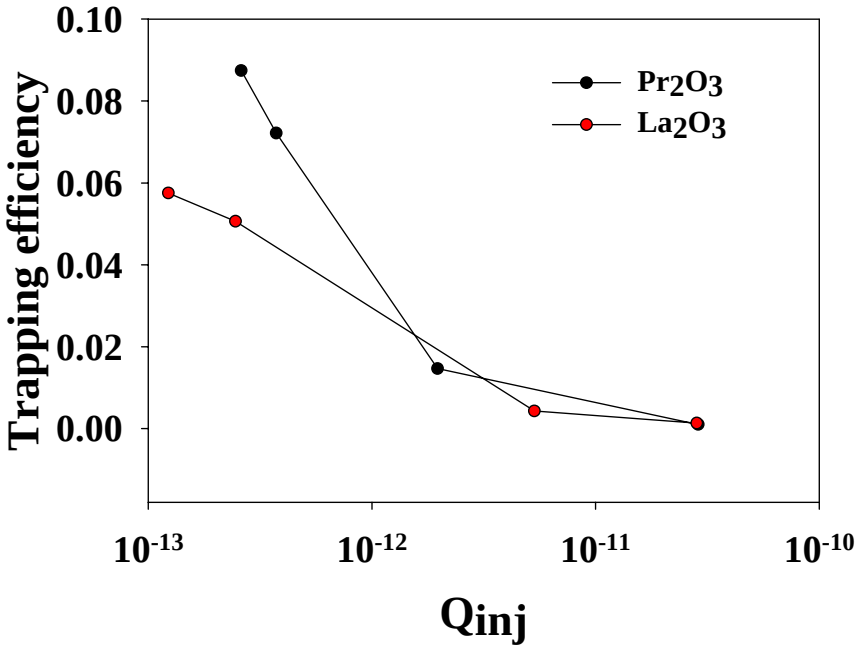


Fig. 4-9 Trapping efficiency of the Pr_2O_3 and La_2O_3 device. Pr_2O_3 device has higher trapping efficiency than La_2O_3 device.

Chapter 5

Conclusion

In this thesis, first, we have proposed a novel simple, reproducible, reliable technique for preparation of 50nm high density HfO_2 nanocrystals using spinodal decomposition of hafnium silicate on SOI and it is compatible to CMOS process. From the experiment result, it has good characteristics in terms of large memory windows, high speed program/erase, good retention time, excellent endurance, and 2-bit operation. With these superior performance, we believe that nano-scale HfO_2 nanocrystal flash memory on SOI is the candidates used for the high density storage application

Then, a SONOS-type flash memory with La_2O_3 trapping layer was proposed. We have also investigated the memory effect on the performance of the La_2O_3 SONOS-type memories. From the experiment result, it has good characteristics in terms of large memory windows, high speed program/erase, good retention time, excellent endurance, and 2-bit operation. Hence, La_2O_3 are the candidates used for the trapping layers for the SONOS-type memories.

Finally, we have investigated the memory effect on the performance of the Pr_2O_3 SONOS-type memories. It has good characteristics in terms of large memory windows, high speed program/erase, excellent endurance, but poor retention. Hence, Pr_2O_3 may be the candidates used for the trapping layers for the SONOS-type memories, if the retention was improved by using thicker tunneling oxide.

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The Study of Flash Memory with High-K Material and Nano-crystal Trapping Layer

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