Chapter 1

Introduction

1.1 Motivation and background

The aggressive scaling of CMOS technology has driven the MOSFET down to sub-100nm scale. For nanometer-scale devices, the pads and metal line would contribute non-negligible parasitic effects. The increasing parasitic effects render significant concern and how to extract the intrinsic device parameters accurately through justified de-embedding process becomes very important. Besides, the circuit designers have critical concern about the accuracy of simulation model. The proliferated challenges trigger our motivation to explore and develop a reliable parameter extraction method for accurate parameters extraction. For miniaturized devices, both intrinsic and extrinsic parameters play an important role in determining model accuracy and simulation reliability.

The major goal for this research work is to develop a reliable and accurate parameter extraction method, which can be applied to nano-scale RF MOSFET of 3-terminal or 4-terminal configurations. De-embedding method and parameter extraction are fundamental of this study and small signal equivalent circuit model built by the extracted parameters will be verified by using ADS simulator to justify the parameter extraction method and model parameter accuracy.

Although the parameters can be extracted under saturation condition [1,2], the equivalent circuit is too complicated to extract parameters easily and accurately. The current gain and high impedance in channel region add the difficulty of extraction. Besides, how to accurately extract the metal line parasitic brings another challenging

issue. To explore the solutions for the mentioned problems, the equivalent circuit was simplified under a specific bias condition, V_{ds}=0V and V_{gs}=V_{dd} to derive simple analytical formulas for extraction of all parasitic RLC parameters. Regarding the published approach adopting equivalent circuit under saturation condition [1,2], there exists further issue with the parameter extraction and optimization, particularly for fitting to S_{22} and Y_{22}. Therefore, equivalent circuits of new schematics under zero V_{ds} or saturation condition were developed and verified in the thesis.

In this work, substrate network parameter extraction is identified as the most difficult problem. Existing publication [3-5] proposed Y-parameter method for substrate resistance extraction. However, the extracted substrate resistance near very low frequency is generally too steep to obtain accurate value through extrapolation to near DC condition. Some other research works [6-7] proposed a modified method to enable direct extraction of each parameter including substrate resistance using linear regression by Y-parameter analysis on the proposed equivalent circuit for high frequency. Due to the fact that the Y-parameter analysis generally leads to lengthy formulas including the model parameters to be extracted, approximation is necessary to simplify the formulas and enable the direct extraction. Unfortunately, their results reveal that optimization cannot be avoided to get sufficiently good match with measurement. Therefore, accurate extraction of substrate resistance remains an open issue to be solved.

One more contribution from this thesis is the adoption of a new parameter noted as C_{dnw} in our proposed equivalent circuit for accurate RF MOSFET modeling. C_{dnw} represents the deep N-well to P-substrate junction capacitance, which exists for current RF CMOS technology adopting deep N-well process for substrate noise isolation and isolation between RF, analog and digital circuit blocks. It is for the first time being proposed and proven through this study that it is a critically essential

parameter to significantly improve simulation accuracy in mid-range of frequencies (5~20 GHz for finger number of 72 and 10~25 GHz for finger number of 36).

1.2 Thesis Organization

The theme of this thesis is the development of a new model parameter extraction method for both intrinsic and extrinsic components to enable accurate simulation for 3-terminal (3T) and 4-terminal (4T) RF MOSFETs.

In Chapter 2, the RF MOSFET layout will be introduced and the differences between 3T and 4T devices will be discussed. Through this work, the major impact on the gate capacitance and substrate network parameters from the differences of 3T and 4T MOSFETs has been identified and will be described in the following chapters.

In Chapter 3, small signal equivalent circuits of new schematics for 3T and 4T RF MOSFETs will be build through circuit analysis under different bias conditions for model parameter extraction. The accuracy of new small signal equivalent circuits has been verified and justified by good matching with measured S-parameters and Y-parameters in linear and saturation regions.

In Chapter 4 and Chapter 5, model parameter extraction methods were derived for 3T and 4T RF MOSFETs respectively. The derivation of equations for parameter extraction will be described in detail and the analysis of extracted parameters will be provided as well.

In Chapter 6, the proposed small signal equivalent circuits will be verified through ADS simulation to justify the accuracy and reliability of the equivalent circuits. Based on ADS simulation, the influence of substrate network on the RF MOSFET high frequency characteristics can be extensively explored. We got important conclusion that 4T MOSFET is necessary to extract the real values of substrate network model

parameters (R_{bulk} and C_{dnw}). 3T MOSEFT itself cannot provide sufficient data for accurate extraction of substrate network parameters.

Chapter 7 addresses the future work for further study. Finally, the appendices provide analytical model development results for parasitic gate capacitances through the assistance of interconnect RC simulation by Raphael. The accuracy of the developed analytical model was verified and justified by good match with Raphael simulation results. The parasitic gate capacitances play an increasingly important role for nano-scale CMOS devices in terms of high frequency operation and the adoption of the parasitic parameters in the gate capacitance model is essential to ensure the accuracy of AC and high frequency simulation required for RF CMOS circuit design.