Chapter 3

RF MOSFET Small Signal Equivalent Circuit Model Analysis

3.1 Preface

In this chapter, I would like to introduce and analyze the small signal equivalent circuit for 3T and 4T devices. The parameters in equivalent circuit would be extracted and discussed in the following chapters. Finally, the equivalent circuit will be completed with all extracted parameters and verified by comparison between measurement and simulation. Following the development of model parameter extraction, the work would be completed with verification of parameters' accuracy.

3.2 3T MOSFET under linear and saturation regions

I specifically focus on three kinds of bias conditions: 1. V_{gs}=V_{ds}=0V; 2. V_{gs}=1.2V, V_{ds}=0V; 3. V_{gs}=V_{ds}=1.2V. After extensive verification, we can prove that most of the model parameters extracted from 3T device can be applicable for 4T device.

3.2.1 Linear region

In this section, I would like to focus on two bias conditions: 1. V_{gs}=V_{ds}=0V, 2. V_{gs}=1.2V, V_{ds}=0V. In the reference [3], Fig. 3-1 is the illustration of device after open and short de-embedding at V_{gs}=V_{ds}=0V bias condition because there is no parasitic resistance and inductance. At low frequency, the extraction equations can be assumed that $\omega^2 R_{sub}^2 \left(C_{gb}+C_{js}+C_{jd}\right)^2 << 1$ and ω^3-terms are negligible compared with

the ω-terms. Therefore, the extraction equations can be approximated as:

$$\mathrm{Im}[Y_{11}] \approx \omega(C_{gso} + C_{gdo} + C_{gb}) \tag{3.1}$$

$$\mathrm{Im}[Y_{12}] \approx -\omega C_{gdo} \tag{3.2}$$

$$\mathrm{Im}[Y_{22}] \approx \omega(C_{gdo} + C_{jd}) \tag{3.3}$$

$$\mathrm{Re}[Y_{22}] \approx \omega^2 R_{sub} C_{jd}^2 \tag{3.4}$$

The capacitance extraction equations of (3.1) ~ (3.4) are well-known and used frequently. But R_{sub} value extracted from $Re[Y_{22}]$ has accuracy issue to be solved. We find that the R_{sub} value still needs a great change to make simulation matched with measurement.

In order to make the equivalent circuit more completed, I add C_{dnw} which is parallel to R_{bulk} and some parasitic parameters into the equivalent circuit as shown in Fig. 3-2 which illustrates the equivalent circuit after open de-embedding corresponding to $V_{gs}=V_{ds}=0V$. In the equivalent circuit, C_{js} and C_{jd} are diffusion capacitances at source and drain to substrate junctions. C_{dnw} is junction capacitance between p-substrate (P-well) and deep N-well. Under the bias at $V_{gs}=0$, the inversion layer doesn't exist and the electronic signal will go through the source-to-substrate and drain-to-substrate junctions. The electronic signals going through the source/drain junctions will experience not only the junction capacitances C_{js} and C_{jd} but also resistive impedances represented by R_{S_diff} and R_{D_diff}. That is why I add two parameters, R_{D_diff} and R_{S_diff}, at the drain and source terminals to represent the resistances of diffusion regions.

It would be more convenient for us to extract intrinsic parameters after open and short de-embedding. Fig. 3-3 is the equivalent circuit of device after 2-step de-embedding. After deriving the extraction equations from the equivalent circuit, the

equations can be shown as:

$$\mathrm{Re}\left(Z_{11}^{dut}\right) = R_{g,\mathrm{int}} + R_{S\_diff} \tag{3.5}$$

$$\mathrm{Re}\left(Z_{22}^{dut}\right) = R_{D\_diff} + R_{S\_diff} \tag{3.6}$$

$$R_{D\_diff} = \frac{\frac{N_F}{2}+1}{\frac{N_F}{2}} R_{S\_diff} \tag{3.7}$$

The third equation is because R_{D_diff} and R_{S_diff} have a structure relation about diffusion regions. The number of source diffusion region always equals the number of drain diffusion region plus one. I extract the $\mathrm{Re}\left(Z_{11}^{dut}\right)$ and $\mathrm{Re}\left(Z_{22}^{dut}\right)$ by averaging the data of 38 ~ 40 GHz. Table 3-1 is the list of extracted resistances.

Table 3-1 The extracted resistance for 3T device at $V_{gs}=V_{ds}=0V$

Average data from 38 ~ 40 GHz ; $V_{gs}=V_{ds}=0V$					
	$Re(Z_{11})$	$Re(Z_{22})$	R_{S_diff} (Ω)	R_{D_diff} (Ω)	$R_{g,int}$ (Ω)
N_F=18	10.32	18.78	8.90	9.88	1.42
N_F=36	5.33	9.03	4.39	4.64	0.94
N_F=72	2.76	4.26	2.10	2.16	0.66

In Fig. 3-4, we can observe good geometry dependence of extracted resistances, especially $R_{g,int}$. The reason for $R_{g,int}$ will be discussed in the next chapter.

For capacitances extraction, we use (3.1) ~ (3.3) in Y-parameter to extract them. The extraction equations are listed below;

$$\mathrm{Im}\left(Y_{11}^{dut}\right) = \omega\left(C_{gdo} + C_{gso} + C_{gb}\right) \tag{3.8}$$

$$\mathrm{Im}\left(Y_{22}^{dut}\right) = \omega\left(C_{gdo} + C_{jd}\right) \tag{3.9}$$

$$-\mathrm{Im}\left(Y_{12}^{dut}\right) = \omega C_{gdo} \tag{3.10}$$

In Table 3-2, I list all extracted capacitances together. Here, I assume that C_{gdo} equals

to C_{gso} and C_{jd} equals to C_{js} because of symmetry structure at this bias condition.

Table 3-2 The extracted capacitances for 3T device at $V_{gs}=V_{ds}=0V$

Average data from 2 ~ 5 GHz ; $V_{gs}=V_{ds}=0V$				
	C_{gg} (fF)	$C_{gdo}=C_{gso}$ (fF)	C_{gb} (fF)	$C_{jd}=C_{js}$ (fF)
N_F=18	65.85	29.32	7.21	42.20
N_F=36	132.68	59.45	13.78	82.68
N_F=72	266.57	120.10	26.37	161.52

Unfortunately, the two parameters, R_{bulk} and C_{dnw}, can not be extracted accurately. Although there are many papers [3]-[5] addressing R_{bulk} extraction, the accuracy of extracted value remains an open issue problem to be solved. In the references [6]-[7], they developed another method to extract R_{bulk}. Specially, they analyze the equivalent circuit at saturation region. Their equivalent circuit is shown in Fig. 3-5. It is composed of physical-based parameters, including nonreciprocal capacitance and substrate-related parameters. They propose a direct extraction method of elements related to the substrate parameter for a three-terminal configuration. In a three-terminal configuration, C_{js} and R_{subs} are excluded because the substrate is tied to the source, as in most high-frequency applications.

For extraction of the substrate components, R_{subd} and C_{jd}, Y_{sub} is defined as follow:

$$\begin{aligned} Y_{sub} &= Y_{22} - g_{ds} - j\omega C_{sd} - j\omega C_{gd} \\ &= \frac{\omega^2 C_{jd}^2 R_{subd}}{1+\omega^2 R_{subd}^2 C_{jd}^2} + \frac{j\omega C_{jd}}{1+\omega^2 R_{subd}^2 C_{jd}^2} \end{aligned} \tag{3.11}$$

By plotting $\omega^2/\mathrm{Re}(Y_{sub})$ against ω^2, the substrate resistance R_{subd} can be obtained from the slope of plot:

$$\frac{\omega^2}{\mathrm{Re}(Y_{sub})} = \omega^2 R_{subd} + \frac{1}{R_{subd} C_{jd}^2} \tag{3.12}$$

According to (3.12), we indeed can obtain the R_{subd} from the slope of plot. But the

extracted and optimized values listed in the reference [7] show that the accuracy issue still exists.

The C_{dnw} parameter is new parameter introduced through our study. For R_{bulk} and C_{dnw}, the difficulty of extracting these two substrate parameters is that these two parameters are too deep inside the equivalent circuit and extracting them is the bottleneck for 2-port measurement. Therefore, the feasible way I can do is optimizing these two parameters by ADS simulator to make measured data and simulation result consistent. In the future, advanced research of 3-port or 4-port measurement might solve the extraction problem of R_{bulk} and C_{dnw} because the substrate could be individually connected to GSG pad.

Fig. 3-6 and 3-7 show the configurations of equivalent circuit at V_{gs}=1.2V, V_{ds}=0V bias condition. The inversion layer exists and uniformly distributes under gate oxide. The R_{ch} represents the resistance of this layer. In order to extract the most important parameter, R_{ch}, we have to make some assumption to simplify the equivalent circuit. 1. Extracting parameter at low frequency. 2. Neglecting substrate network at low frequency. The simplified equivalent circuit is shown as Fig. 3-8. In the figure, the center π model consists of C_{gs}, C_{gd}, and R_{ch}. Translating it into T model is a feasible way to use Z-parameter to represent total equivalent circuit. The detailed extraction will be discussed in the next chapter.

3.2.2 Saturation region

The equivalent circuit of this bias condition is the most difficult task because of asymmetry structure and current gain. Fig. 3-9 is the configuration of equivalent circuit at saturation bias condition. There are two current gains, g_m and g_{ds}. The values of g_m and g_{ds} can be achieved from the differentiation of drain current I_d versus gate bias V_{gs}

and drain bias V_{ds} respectively.

Under this bias condition, the pinch off occurs near drain side and the distribution inversion layer is asymmetric. From pinch-off point to source diffusion region, the inversion layer exists and I use a resistance R_{ch} to represent it. Along the opposite direction i.e. the depletion region defined by pinch-off point and drain junction, the inversion layer doesn't exist but there remains a flowing path for current and coupling capacitance between inversion layer and drain diffusion region. Therefore, I use a parallel network, R_{ds} and C_{ds}, to represent this region.

The extraction of C_{ds} relies on imaginary part of Y_{22}. Before extracting C_{ds}, we have to know C_{gd} and C_{jd}. Capacitance C_{gd} can be ectracted from $Im(Y_{12})$ at $V_{gs}=V_{ds}=1.2V$. But C_{jd} has to be extracted from $Im(Y_{22})$ at $V_{gs}=0V$, $V_{ds}=1.2V$ because $Im(Y_{22})$ equals to $\omega(C_{gd}+C_{jd})$ under this bias condition. Of course the capacitance C_{jd} wouldn't be the same at two different bias conditions. But this is also another bottleneck of extraction. After knowing C_{gd} and C_{jd}, the C_{ds} is almost certain under $V_{gs}=V_{ds}=1.2V$.

Theoretically, C_{ds} extracted from above discussion is feasible at low frequency. But practically, the curve drops steeply at low frequency and the measured data start at 2GHz. Therefore, smaller values of extracted C_{ds} can be expected. We will find out that C_{ds} has to be larger than extracted value for simulation results matching accurately the measured data.

Finding resistances, R_{ch} and R_{ds}, has to use g_{ds}. The reciprocal of g_{ds} represents the sum of R_{ch} and R_{ds} for small signal to pass through. But how to separate them from the sum is the next important work. Recalling the ratios of C_{gs}/C_{gg} and C_{gd}/C_{gg}, it can inspire something important in me. The definition of capacitance is the ratio of charge variation to voltage variation. Larger capacitance represents more charge carriers free to response to voltage. Therefore, I command that the ratio of R_{ch}/R_{ds} equals to the ratio of C_{gd}/C_{gs}. Finally, the values of R_{ch} and R_{ds} can be found out.

3.3 4T MOSFET under linear and saturation regions

For 4T device, I also try to construct the equivalent circuit at the same bias conditions compared with 3T device. The metal-3 layer is the only difference between 3T and 4T devices. Therefore, the equivalent circuits for 3T device can be used for 4T device after slightly modifying at source/bulk terminals. Fig. 3-10 ~ 3-12 are equivalent circuits for 4T device at three specific bias conditions. We can see that there are individual RL branches at source and bulk terminals. The R_S and L_S of 4T device will be extracted in the Chapter 5. The extraction of R_B and L_B needs another helpful results—parasitic parameters of short pad, to command $R_B||R_S=R_{s,ext}$ and $L_B||L_S=L_{s,ext}$.

I command the C_{ds} of 3T and 4T devices to be the same. So are g_m and g_{ds}. The reason of the commands is because the intrinsic layout under metal-3 layer of 3T and 4T are totally the same. I believe that, therefore, intrinsic parameters should be equal.

3.4 Comparison between 3T and 4T MOSFET

The most obvious difference between 3T and 4T MOSFET is the common metal-3 layer. The following sections discuss the influences accompanying this metal-3 layer.

3.4.1 Substrate network

Basically, the substrate networks of 3T and 4T devices at any bias conditions are the same. But the 4T device lacks the common metal-3 layer. Therefore, its substrate network and source terminals would connect the ground individually. This difference can’t be ignored because the substrate network of 4T device is very sensitive to device performance especially for the signal coming into from port 2. I will verify and discuss it in the Chapter 6.

3.4.2 Parasitic resistance, capacitances, inductances

For the device after open de-embedding, the capacitances of 3T and 4T device will be the same. The reason is that the coupling terminals of capacitances are under metal-3 layer. It‘s worthy to mention that the capacitance extraction for 4T device has to be revised to obtain real physically values compared with 3T device.

For resistances and inductances, all parameters are also the same except those of source and bulk branches. There are only one resistance and one inductance at source terminal for 3T device because the source and bulk branches are parallel. Obviously, the values of source resistance and source inductance of 3T device are certainly smaller than those of 4T device. We will observe later that the inductance at source terminal would influence the phase dominantly. Therefore, extracting accurate inductance of 3T and 4T device is important for matched simulation.

3.4.3 De-embedding methods

It can be de-embedded directly by 2-step de-embedding for 3T device because short pad layout is designed for 3T device. But it can only do open de-embedding for 4T device. Without doing short de-embedding for 4T device, we need to extract capacitance carefully because the parasitic effect induced by remained source resistance would seriously affect the capacitance extraction. Therefore, specific capacitance extraction method for 4T device due to short de-embedding banning is developed accordingly.

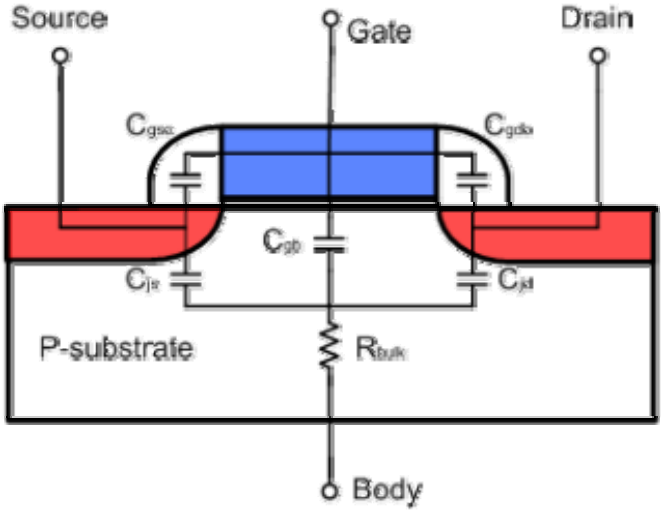

Fig. 3-1 Equivalent circuit of an RF MOSFET at V_{gs}=V_{ds}=0V

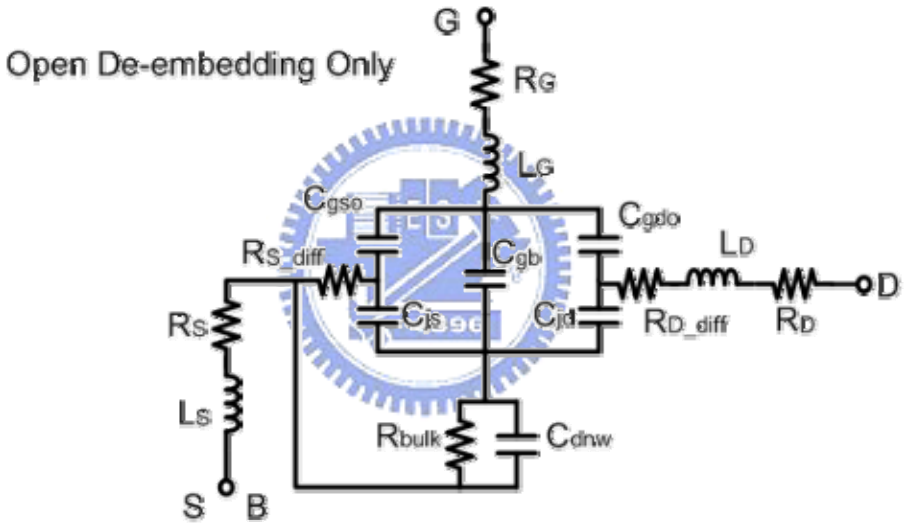

Fig. 3-2 The equivalent circuit of 3T device at V_{gs}=V_{ds}=0V (Open_de)

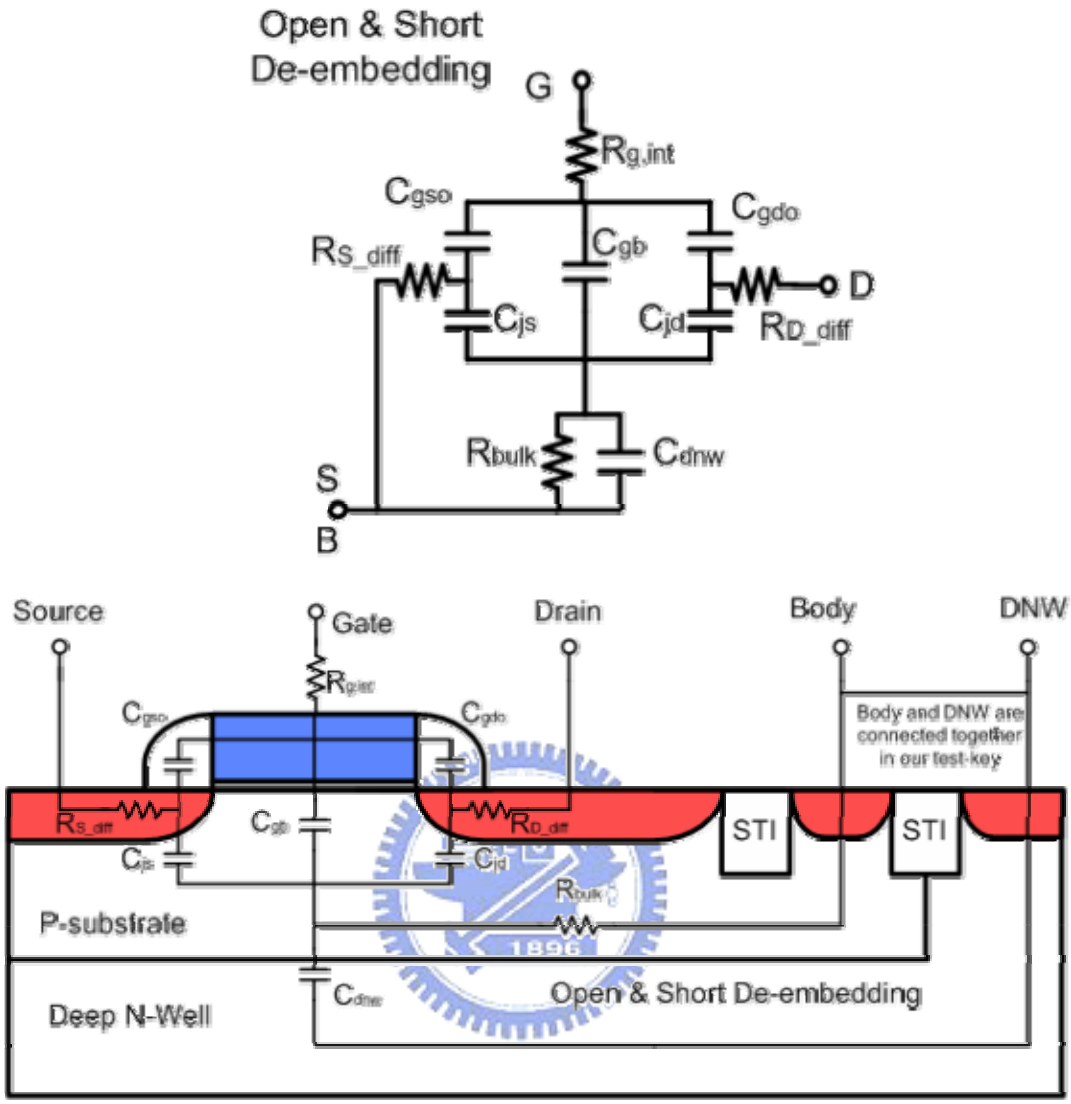

Fig. 3-3 The equivalent circuit of 3T device at V_{gs}=V_{ds}=0V (Open+Short_de)

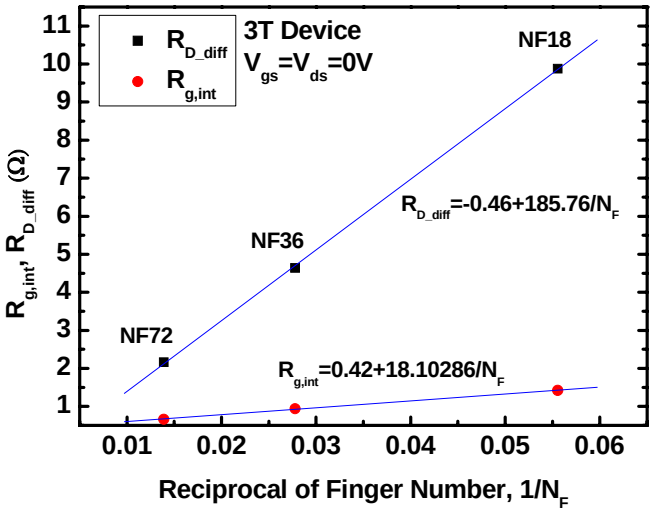

Fig. 3-4 The geometry dependence of extracted resistances at V_{gs}=V_{ds}=0V for 3T

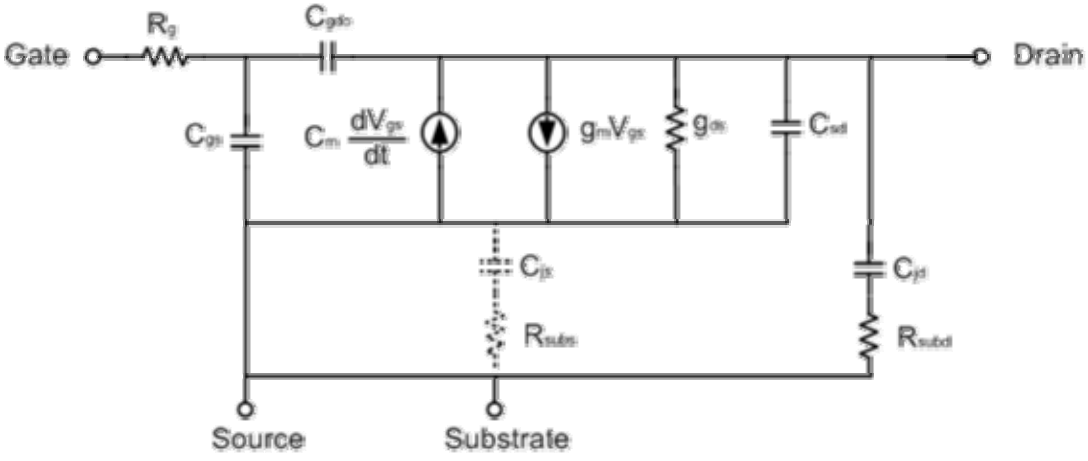

Fig. 3-5 Small signal equivalent circuit of the MOSFET at saturation region

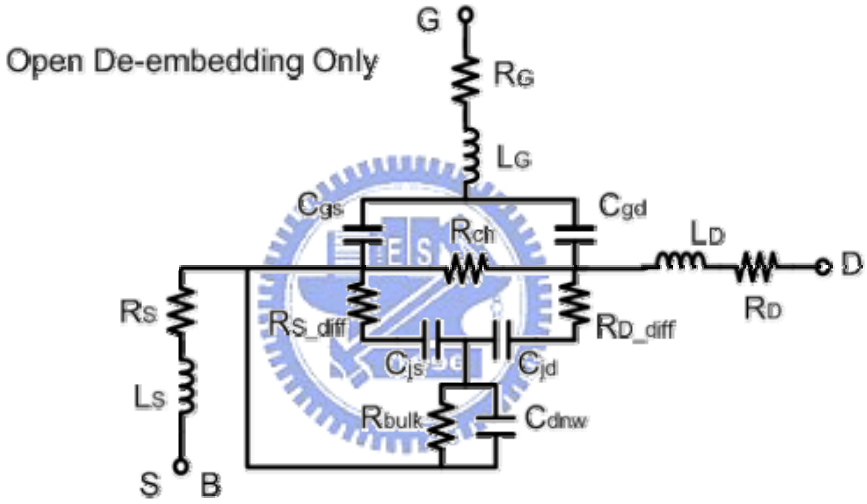

Fig. 3-6 The equivalent circuit of 3T device at V_{gs}=1.2V, V_{ds}=0V (Open_de)

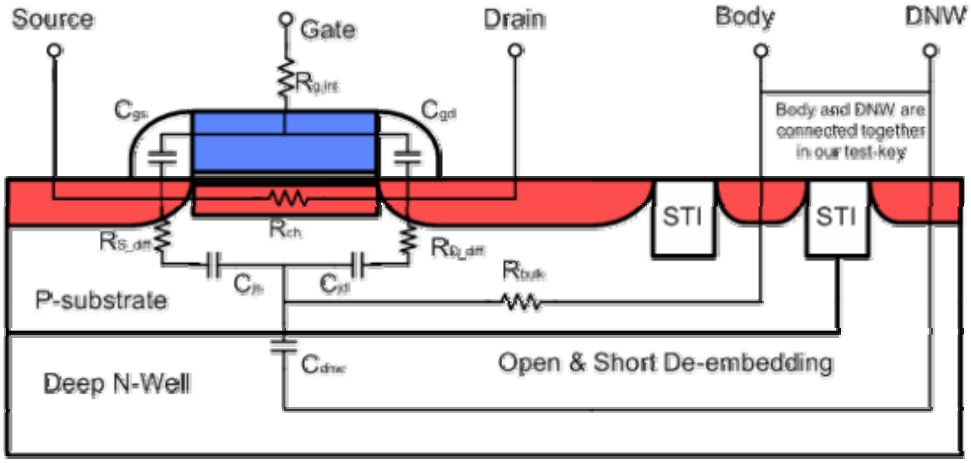

Fig. 3-7 The configuration of equivalent circuit of 3T at V_{gs}=1.2V, V_{ds}=0V

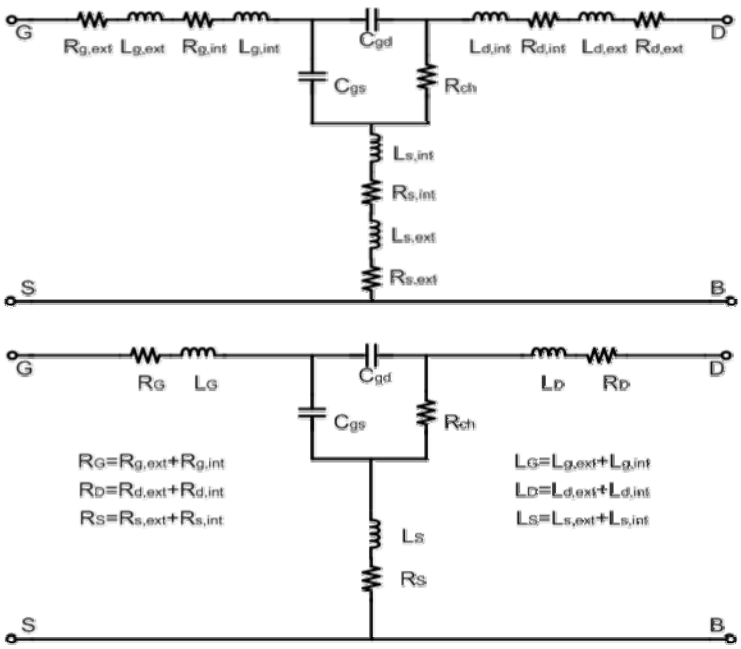

Fig. 3-8 The equivalent circuit of device at $V_{gs}>V_{th}$; $V_{ds}=0V$

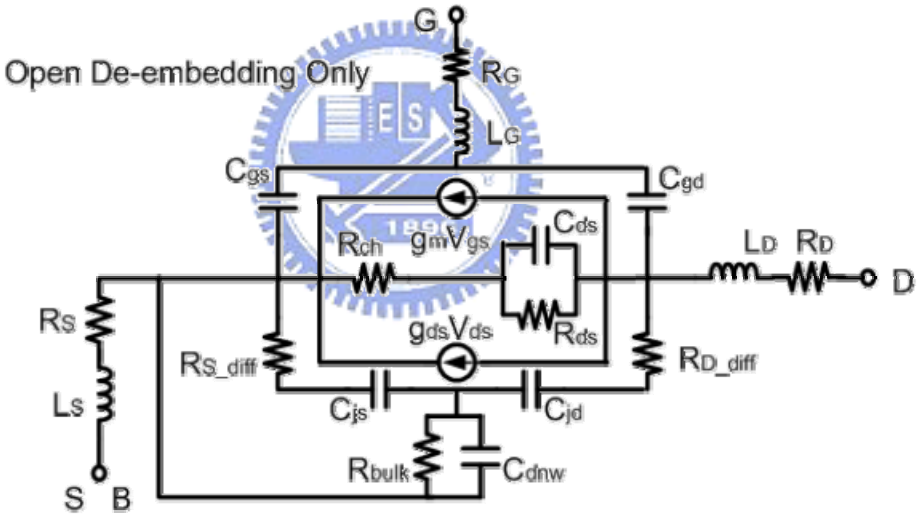

Fig. 3-9 The equivalent circuit of 3T device at $V_{gs}=V_{ds}=1.2V$ (Open_de)

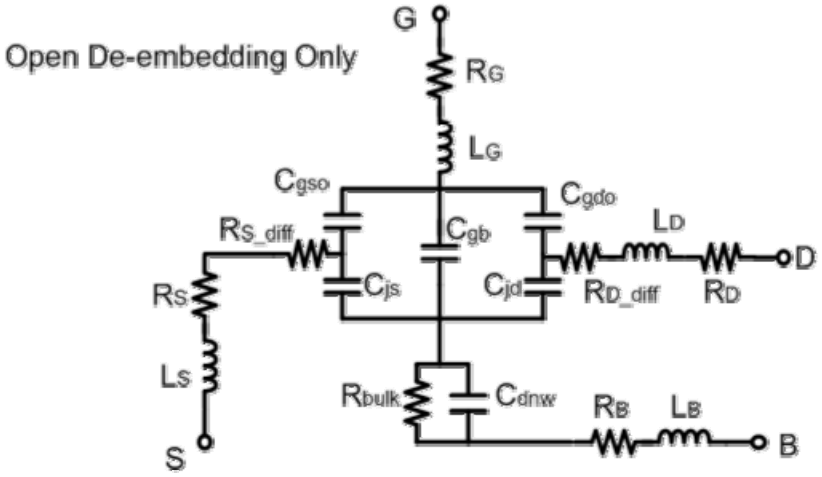

Fig. 3-10 The equivalent circuit of 4T device at V_{gs}=V_{ds}=0V (Open_de)

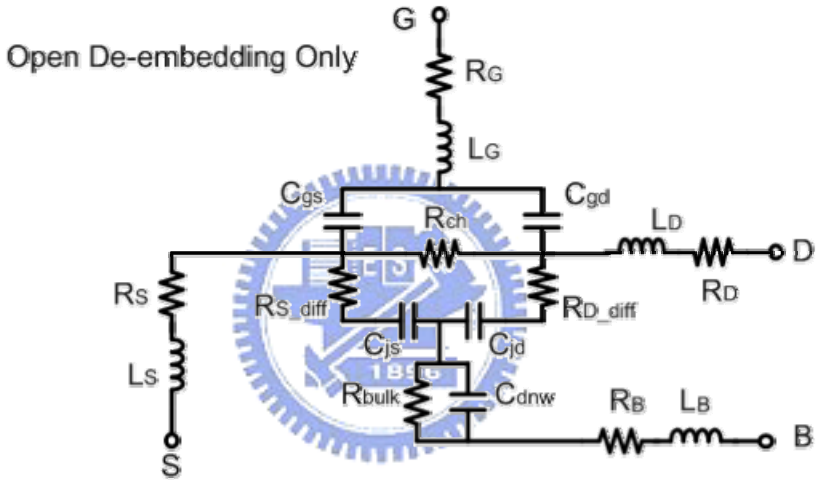

Fig. 3-11 The equivalent circuit of 4T device at V_{gs}=1.2V, V_{ds}=0V (Open_de)

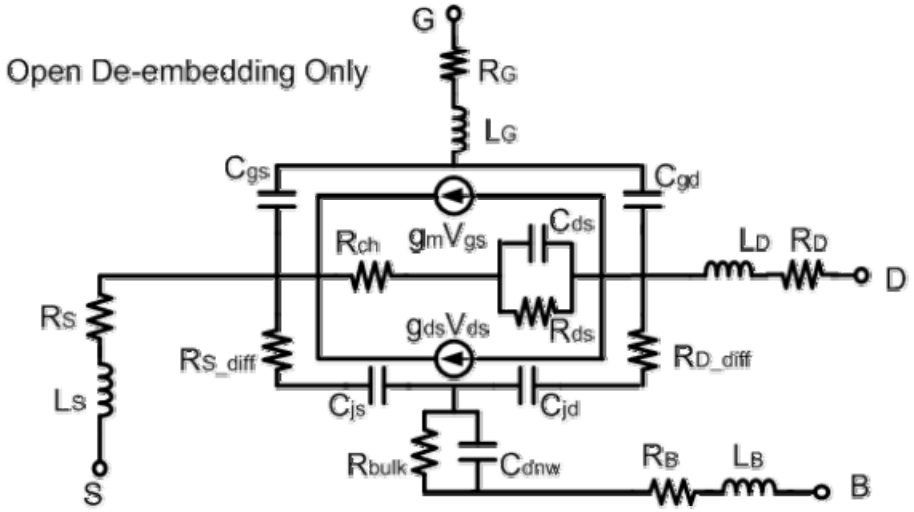

Fig. 3-12 The equivalent circuit of 4T device at V_{gs}=V_{ds}=1.2V (Open_de)