Chapter 4

3T RF MOSFET Model Parameter Extraction

4.1 De-embedding methods

For the purpose of extracting MOSFET parameters from measured data, the on-chip RF measurement is adopted. After calibration of measurement system, we suppose to make the reference planes locate at the probe tips as shown in Fig. 4-1. The remaining work is focused on how we get device parameters from measured data which excludes parasitic effects by using de-embedding method.

4.1.1 Open de-embedding

The open pad is a structure excluding DUT. Before doing any de-embedding step, we have to transform measured S-parameter with pads into measured Y-parameter. The representation is shown in Fig. 4-2. Also, the measured S-parameter for open pad has to be transformed into measured Y-parameter.

From Fig. 4-3 for open pad as an equivalent circuit and Fig. 4-2 for device with pad, we can construct the Y-parameter matrices to represent device with pad given by (4.1) and open pad given by (4.2).

$$S_{mea} \rightarrow Y_{mea} \tag{4.1}$$

$$S_{open} \rightarrow Y_{open} \;\; ; \;\; Y_{open} = \begin{bmatrix} Y_{C1} + Y_{C3} & -Y_{C3} \\ -Y_{C3} & Y_{C2} + Y_{C3} \end{bmatrix} \tag{4.2}$$

where Y_{C1} and Y_{C2} are admittance between two signals and reference ground respectively. Y_{C3} is the admittance between two signal pads. In Fig. 4-2, Z_{RL1}, Z_{RL2}, and Z_{RL3} are related to short pad layout and will be discussed in section 4.1.2.

So far, we can use equations (4.1) and (4.2) to do the first step of de-embedding, i.e. open de-embedding. The capacitive coupling effect can be de-embedded through open de-embedding.

$$Y_{mea_o} = Y_{mea} - Y_{open} \tag{4.3}$$

But Z_{RL1}, Z_{RL2}, and Z_{RL3} are remained in Y_{mea_o} matrix.

4.1.2 Short de-embedding

The short pad is a structure with device taken off and all terminals connected together by metal. As shown in Fig. 4-4, we can observe that the short pad equivalent circuit includes metal line parasitic impedance (Z_{RL1}, Z_{RL2}, Z_{RL3}) and pad coupling admittance (Y_{C1}, Y_{C2}, Y_{C3}). Before we use short pad measured data to do de-embedding, the short pad S-parameter need to be transformed into Y-parameter to proceed open pad de-embedding. Doing open de-embedding for short pad first is in order to avoid subtracting coupling parameters (Y_{C1}, Y_{C2}, Y_{C3}) twice.

According to discussion in last paragraph, the de-embedding equations can be written as:

$$S_{short} \rightarrow Y_{short} \;\; ; \;\; Y_{short} - Y_{open} = Y_{short_o} \tag{4.4}$$

For equation (4.4), we suppose that there is only metal line parasitic parameters (Z_{RL1} ~ Z_{RL3}) in Y_{short_o} matrix. So, we need to use Y_{short_o} to proceed short de-embedding on Y_{mea_o} extracted by equation (4.3). Before doing short de-embedding on Y_{mea_o}, we can not subtract these two matrices each other directly in form of Y-parameter. We have to transform these two matrices into Z-parameter and proceed with short de-embedding.

$$Y_{mea_o} \rightarrow Z_{mea_o} \;\; ; \;\; Y_{short_o} \rightarrow Z_{short_o} \;\; ; \;\; Z_{short_o} = \begin{bmatrix} Z_{RL1} + Z_{RL3} & Z_{RL3} \\ Z_{RL3} & Z_{RL2} + Z_{RL3} \end{bmatrix}$$

$$Z_{dut} = Z_{mea_o} - Z_{short_o} \quad (4.5)$$

Through equations (4.1) ~ (4.5), we get Z_{dut} matrix finally. This matrix also can be transformed into Y-parameter form depending on our needs.

$$Z_{dut} \rightarrow Y_{dut} \quad (4.6)$$

Fig. 4-5 illustrates the two step de-embedding procedures with open and short de-embedding.

4.2 Parasitic resistance and inductance extraction and analysis

In this section, we focus on the extraction of resistance and inductance. From short pad, we can get parasitic resistance and inductance associated with metal-8 to metal-3 layers. These parasitic parameters can not provide us the necessary information about device geometry dependence because of common usage of short pad for every device. To find out total parasitic resistances and inductances of metal-8 to metal-1 layers, we must extract the parameters from device under specific bias condition. We will demonstrate the result with good device geometry dependence.

The research devices are fabricated by foundry standard logic CMOS process technology and measured by NDL 40 GHz S-parameter measurement systems.

4.2.1 Parasitic RL extraction from short pad

The equivalent circuit of short pad after open de-embedding can be represented as Fig. 4-6. The equivalent circuit is very simple. I only use resistance and inductance parameters to represent the metal line. The resistances and inductances extracted from short pad are defined with “ext” index to represent extrinsic parasitic parameters.

In Fig. 4-6, the matrix of equivalent circuit represented by Z-parameter is shown below:

$$Z_{short_o}=\begin{bmatrix}(R_{g,ext}+j\omega L_{g,ext})+(R_{s,ext}+j\omega L_{s,ext}) & R_{s,ext}+j\omega L_{s,ext}\\ R_{s,ext}+j\omega L_{s,ext} & (R_{d,ext}+j\omega L_{d,ext})+(R_{s,ext}+j\omega L_{s,ext})\end{bmatrix} \quad (4.7)$$

From the Z_{short_o} matrix represented as (4.7), we can extract all extrinsic parameters by using the elements of matrix. The extraction equations of parameters are:

$$R_{s,ext}=\mathrm{Re}\left(Z_{12}^{short_o}\right)\ ;\ L_{s,ext}=\mathrm{Im}\left(Z_{12}^{short_o}\right)/\omega \quad (4.8)$$

$$R_{g,ext}=\mathrm{Re}\left(Z_{11}^{short_o}-Z_{12}^{short_o}\right)\ ;\ L_{g,ext}=\mathrm{Im}\left(Z_{11}^{short_o}-Z_{12}^{short_o}\right)/\omega \quad (4.9)$$

$$R_{d,ext}=\mathrm{Re}\left(Z_{22}^{short_o}-Z_{12}^{short_o}\right)\ ;\ L_{d,ext}=\mathrm{Re}\left(Z_{22}^{short_o}-Z_{12}^{short_o}\right)/\omega \quad (4.10)$$

The extracted extrinsic inductance shows flat lines and indicates its frequency independence. We expect that the frequency independence would happen to resistances. However, the extracted extrinsic resistances show frequency dependence except $R_{s,ext}$. The experience told us that this situation may be caused by ground shielding through poly-Si plate under the signal pad. However we don't have evidence to prove the assumption. This open question can be defined as future work. Note that open de-embedding to metal-3 instead of metal-1 was done for short pad to more accurate result.

Neglecting the frequency dependence of resistance temporarily, we can extract the resistance and inductance values by averaging the data at lower frequencies from 2 to 5GHz. The reason of extracting parameter values at low frequency is that we try to minimize complicated coupling effect which always becomes worse at higher frequencies.

The extracted extrinsic parameter values are listed in Table 4-1.

Table 4-1 The extracted extrinsic resistances and inductances of short pad

Average data from 2 ~ 5 GHz					
$R_{g,ext}$ (Ω)	$R_{d,ext}$ (Ω)	$R_{s,ext}$ (Ω)	$L_{g,ext}$ (pH)	$L_{d,ext}$ (pH)	$L_{s,ext}$ (pH)
0.328	0.314	0.308	55.43	51.51	17.67

4.2.2 Parasitic RL extraction from device

In the reference [1], Fig. 4-7 shows a small-signal MOSFET equivalent circuit used for the accurate extraction. Parasitic inductances (L_g, L_d, L_s) are associated with their interconnection line. In addition, R_g is the gate resistance due to n^+ poly-silicon gate, R_d and R_s are drain and source series resistance respectively.

The intrinsic part of dotted box in Fig. 4-7 is described as the following Y^i-parameters:

$$Y_{11}{}^i = j\omega(C_{gs} + C_{gd}) \tag{4.11}$$

$$Y_{12}{}^i = -j\omega C_{gd} \tag{4.12}$$

$$Y_{21}{}^i = g_m - j\omega C_{gd} \tag{4.13}$$

$$Y_{22}{}^i = g_{ds} + j\omega(C_{ds} + C_{gd}) \tag{4.14}$$

After the Y^i-parameters are converted to Z^i-parameters and subsequently series resistances and inductances are added. Fig. 4-7 is described by the following Z parameters:

$$Z_{11} = R_g + R_s + j\omega(L_g + L_s) + \frac{g_{ds} - j\omega(C_{gd} + C_{ds})}{D} \tag{4.15}$$

$$Z_{12} = R_s + j\omega L_s + \frac{j\omega C_{gd}}{D} \tag{4.16}$$

$$Z_{21} = R_s + j\omega L_s - \frac{g_m - j\omega C_{gd}}{D} \tag{4.17}$$

$$Z_{22} = R_d + R_s + j\omega(L_d + L_s) + \frac{j\omega(C_{gd} + C_{gs})}{D} \tag{4.18}$$

where
$$\begin{aligned} D &= Y_{11}{}^{i} Y_{22}{}^{i} - Y_{12}{}^{i} Y_{21}{}^{i} \\ &= -\omega^2 (C_{gs} C_{ds} + C_{gs} C_{gd} + C_{gd} C_{ds}) + j\omega[g_m C_{gd} + g_{ds}(C_{gs} + C_{gd})] \end{aligned} \tag{4.19}$$

In the reference [1], the extraction method has been discussed and developed in detail. Resistances and inductances are defined as the limiting values at infinite frequency. Since it is very difficult to measure the infinite values directly, they obtain the limiting values through the curve-fitting of their plot vs. frequency over the entire measurement frequency range. But there are many parameters involved in the small-signal equivalent circuit at saturation regions. Besides, I can't obtain reasonable parameter values when I use the same method developed in reference [1]. So, this inspires me to extract parameters by using simpler equivalent circuit.

Fig. 4-8 is the illustration of device after open de-embedding under V_{ds}=0V and V_{gs}>V_{th}. It is modified from Fig. 4-7. In the equivalent circuit, there is no current gain and C_{ds}. We don't have to consider C_{ds} parameter because the strong inversion layer connects the drain and source terminals together. The parameter R_{ch} represents the resistance of inversion layer. The metal-3 layer is the boundary of extrinsic and intrinsic parasitic RL parameters because of short pad layout. The extrinsic RL parameters have been extracted from short pad in last section. Another approach is to extract total parasitic RL parameters from device after open de-embedding. Because I use the simplest equivalent circuit, I extract parameters at lower frequencies as far as I can.

First of all work, we deal with the device after open and short de-embedding. In this situation, the extrinsic parasitic RL parameters should be de-embedded and left the part under metal-3 layer. Under V_{gs}>V_{th} and V_{ds}=0V bias condition, we define $C_{gd} = C_{gs}$ and the real part of matrix Z_{dut} at low frequency can be shown as:

$$\mathrm{Re}(Z_{dut}) = \begin{bmatrix} R_{g,\mathrm{int}} + R_{s,\mathrm{int}} + \dfrac{R_{ch}}{4} & R_{s,\mathrm{int}} + \dfrac{R_{ch}}{2} \\ R_{s,\mathrm{int}} + \dfrac{R_{ch}}{2} & R_{d,\mathrm{int}} + R_{s,\mathrm{int}} + R_{ch} \end{bmatrix} \quad (4.20)$$

Fortunately, at this bias condition and very low frequency, we can derive the matrix to a simple form. According to the matrix (4.20), we discuss the off diagonal element, i.e. $\mathrm{Re}(Z_{12}^{dut})$ given by (4.20).

$$\mathrm{Re}(Z_{12}^{dut}) = R_{s,\mathrm{int}} + \frac{R_{ch}}{2} \quad (4.21)$$

in which there are two terms, one is $R_{s,int}$ and another is $R_{ch}/2$. From last section, we have extracted $R_{s,ext}$ of 0.308Ω. Now, we have to decide the value of $R_{s,int}$ with $R_{s,ext}$. According to the layout, $R_{s,ext}$ represents the resistance of metal-8 to metal-3 layer and $R_{s,int}$ represents the resistance of metal-3 down to contact. Through metal line layout analysis and calculation of resistance by $R = \rho \cdot \frac{L}{A}$,to estimate the ratio of $R_{s,ext}/R_{s,int}$, we get the ratio of $R_{s,ext}/R_{s,int}$ at about 15. It means that the $R_{s,int}$ is only about 0.021Ω. We can almost neglect this term in (4.21) and easily extract the channel resistance R_{ch}. If the term $R_{s,int}$ can not be neglected, we will not get the channel resistance with strong finger number dependence. The equation (4.21), therefore, can be rewritten as:

$$\mathrm{Re}(Z_{12}^{dut}) \approx \frac{R_{ch}}{2} \Rightarrow R_{ch} = 2 \cdot \mathrm{Re}(Z_{12}^{dut}) \quad (4.22)$$

I extract the R_{ch} by averaging the data in the range of 2 ~ 5 GHz. Table 4-2 is the list of R_{ch} under V_{ds}=0V and varies V_{gs}.

Table 4-2　The extracted channel resistance R_{ch}

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; R_{ch}(Ω)				
V_{gs} (V)	1.2	1.0	0.8	0.6
N_F=18	6.270	7.756	11.342	25.645

N_F=36	3.118	3.852	5.618	12.649
N_F=72	1.574	1.943	2.833	6.384

Now, we back to research the device after open de-embedding only. Also, we define $C_{gd} = C_{gs}$ and the real part of Z-parameter matrix at low frequency can be represented as:

$$\mathrm{Re}(Z_{mea_o}) = \begin{bmatrix} R_G + R_S + \frac{R_{ch}}{4} & R_S + \frac{R_{ch}}{2} \\ R_S + \frac{R_{ch}}{2} & R_D + R_S + R_{ch} \end{bmatrix} \tag{4.23}$$

Similarly, from $\mathrm{Re}(Z_{12}^{mea_o})$ and equation (4.22), we can extract total parasitic source resistance—R_S. We get the result that R_S is equal to $R_{s,ext}$ extracted from short pad. It is because we make an assumption that $R_{s,int} << R_{s,ext}$. Therefore, R_S can be approximated by $R_{s,ext}$, $R_S \approx R_{s,ext}$. The R_S was calculated by averaging the data in the range of 2 ~ 5 GHz. Table 4-3 summarizes R_S versus gate voltage.

Table 4-3 The extracted total parasitic source resistance R_S

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; $R_S(\Omega)$					
V_{gs} (V)	1.2	1.0	0.8	0.6	Avg.
N_F=18	0.308	0.308	0.308	0.308	0.308
N_F=36	0.308	0.308	0.308	0.308	0.308
N_F=72	0.307	0.307	0.307	0.307	0.307

From the matrix given by (4.23), we can extract R_D and R_G parameters by following equations for known R_S and R_{ch}.

$$\mathrm{Re}(Z_{22}^{mea_o}) = R_D + R_S + R_{ch} \tag{4.24}$$

$$\mathrm{Re}(Z_{11}^{mea_o}) = R_G + R_S + \frac{R_{ch}}{4} \tag{4.25}$$

R_D and R_G were calculated by averaging the data in the range of 2 ~ 5 GHz. Table 4-4

and 4-5 indicate R_D and R_G under varying gate voltages.

Table 4-4 The extracted total parasitic drain resistance R_D

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; R_D(Ω)					
V_{gs} (V)	1.2	1.0	0.8	0.6	Avg.
N_F=18	0.427	0.421	0.395	0.394	0.409
N_F=36	0.393	0.392	0.386	0.375	0.387
N_F=72	0.349	0.347	0.345	0.338	0.345

Table 4-5 The extracted total parasitic gate resistance R_G

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; R_G(Ω)					
V_{gs} (V)	1.2	1.0	0.8	0.6	Avg.
N_F=18	4.804	4.860	4.790	4.995	4.862
N_F=36	2.819	2.793	2.769	2.932	2.828
N_F=72	1.755	1.692	1.693	1.781	1.730

Following the same extraction flow discussed above, we work on total parasitic inductor extraction. $C_{gd} = C_{gs}$ under V_{ds}=0V. The imaginary part of Z_{mea_o} matrix at low frequency can be written as:

$$\mathrm{Im}(Z_{mea_o}) = \begin{bmatrix} \omega\left(L_G + L_S - \frac{1}{2\omega^2 C_{gd}}\right) & \omega\left(L_S - \frac{C_{gd}R_{ch}^2}{4}\right) \\ \omega\left(L_S - \frac{C_{gd}R_{ch}^2}{4}\right) & \omega\left(L_D + L_S - \frac{C_{gd}R_{ch}^2}{2}\right) \end{bmatrix} \tag{4.26}$$

$$\left.\frac{\mathrm{Im}(Z_{12}^{mea_o})}{\omega}\right|_{\omega\to 0} = L_S - \frac{C_{gd}R_{ch}^2}{4} \tag{4.27}$$

$$\left.\frac{\mathrm{Im}(Z_{22}^{mea_o})}{\omega}\right|_{\omega\to 0} = L_D + L_S - \frac{C_{gd}R_{ch}^2}{2} \tag{4.28}$$

$$\left.\frac{\mathrm{Im}\left(Z_{11}^{mea_o}\right)}{\omega}\right|_{\omega\to 0}=L_G+L_S-\frac{1}{2\omega^2 C_{gd}} \quad (4.29)$$

With given R_{ch}, we have to extract C_{gd} at first to solve L_S, L_D, and L_G from (4.27), (4.28), and (4.29). From measurement S-parameters after open and short de-embedding, we can use Y_{dut} matrix to extract C_{gd} parameter from the equation given by $\mathrm{Im}\left(Y_{12}^{dut}\right)=-\omega C_{gd}$ (discussed later). The L_S and L_D were calculated by averaging the data within 2 ~ 5 GHz while L_G was calculated by averaging under higher frequencies in 30 ~ 40 GHz. There is an abrupt peak in L_G versus frequency plot. I think that it may be caused by angular frequency in L_G at very low frequency. From L_G extraction equation given by (4.29), the third term has ω^2-term in denominator. It may cause big error at very low frequency. To minimize the error, L_G was extracted at higher frequency. Table 4-6 ~ 4-8 list L_S, L_D, and L_G under varying gate voltages.

Table 4-6 The extracted total parasitic source inductance L_S

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; L_S(pH)				
V_{gs} (V)	1.2	1.0	0.8	Avg.
N_F=18	15.88	15.56	14.68	15.37
N_F=36	16.49	16.37	16.08	16.31
N_F=72	16.60	16.51	16.24	16.45

Table 4-7 The extracted total parasitic drain inductance L_D

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; L_D(pH)				
V_{gs} (V)	1.2	1.0	0.8	Avg.
N_F=18	50.84	50.54	49.21	50.20
N_F=36	50.58	50.30	49.56	50.15
N_F=72	49.17	49.13	48.96	49.09

Table 4-8 The extracted total parasitic gate inductance L_G

Average data from 30 ~ 40 GHz ; V_{ds}=0V ; L_G(pH)				
V_{gs} (V)	1.2	1.0	0.8	Avg.
N_F=18	70.93	67.46	63.55	67.31
N_F=36	55.24	54.45	53.36	54.68
N_F=72	47.50	47.70	47.88	47.69

Through the comparison with the extrinsic inductances extracted from short pad as shown in Table 4-1, all three extrinsic inductances show close value between those extracted from MOSFET and those from short pad. Because the total parasitic inductances extracted from MOSFET (DUT) include metal-3 to metal-1, the values should be larger than those of short pad as we anticipated. Maybe the measurement error and layout difference between DUT and short pad would have some influence on what we extracted but the extracted inductances are consider to keep reasonable accuracy.

We can verify the extraction matrices of (4.23) and (4.26) for validity. Taking the extraction equations derived in the reference [1] as the standard. When we command the g_m and C_{ds} values to be equal zero, the equation (4.15) ~ (4.19) certainly can be approximated as the extraction matrices derived in my thesis. After verifying the validity extraction matrices, we can extract accurate parameters more easily and avoid extracting at infinite frequency by curve-fitting.

4.2.3 Frequency and bias dependence

In last section, we have extracted parasitic resistances (R) and inductances (L) associated with MOSFET's 3 terminals (G, S, D). These parasitic R and L are dominated by metal lines. Due to the fact, we expect that these parameters are bias independent. Indeed, we observe that there is almost no bias dependence in the

extracted extrinsic R and L with gate biases varied from 0.6V ~ 1.2V. All the extracted R and L reveal some variation with frequency, particularly at increasing frequency. And all the parasitic parameters were extracted by average in sufficiently low frequencies where the extraction equations derived keep valid. As long as the accuracy of extraction equations is justified under reasonable assumptions, the parameters extracted at low frequency can be justified accordingly.

4.2.4 Device geometry dependence

In the following, the finger number effect on R_{ch} and terminal parasitic resistances (R_S, R_D, and R_G) will be verified. The channel resistances, R_{ch} shown in Fig. 4-9 indicate good linear dependence on the inverse of finger number ($1/N_F$). The larger N_F, the smaller R_{ch} can be easily explained by parallel resistance theory. Regarding the gate bias (V_{gs}) effect, the higher V_{gs}, the smaller R_{ch} accounts for the increasing inversion carrier induced smaller channel resistance. Besides, all R_{ch} curves under various V_{gs} almost intersect at an identical point near the origin. The results suggest the accuracy of extracted R_{ch}.

Three terminal resistances R_S, R_D, and R_G are shown in Fig. 4-10. R_S indicate near constants versus N_F. From layout structure, no matters which finger numbers, all devices have the same current path from metal-3 to metal-8. Although there is difference in the current path through metal-3 to metal-1 for different finger number devices, the resistance contributed from this part is very small and the introduced difference can be neglected.

As for R_D, it intersects Y-axis at around 0.334Ω and decreases with increasing finger number. The smaller R_D associated with larger N_F can be explained easily by drain metal layout. It is because that the drain contacts formed through metal-1 layer

led to drain metal-1 resistance in parallel through multiple fingers. The smaller R_D associated with larger N_F, i.e. smaller $1/N_F$ results in the positive slope in R_D vs. $1/N_F$. The intersection, 0.334Ω, is considered reasonable due to good match with $R_{d,ext}$ extracted from short pad (M3 ~ M8) and given by 0.314Ω.

R_G is contributed mostly by poly-gate. Therefore, R_G is larger than the other two resistances R_S and R_D contributed by metal lines. As shown in Fig. 4-10, R_G reveal obvious finger number dependence. The intersection, 0.713Ω, represents the resistance contributed from metal-2 ~ metal-8 and is about twice as large as the $R_{g,ext}$ extracted from short pad. The larger resistance comes from a ring at metal-2 layer to connect all poly fingers. This part metal line contributes non-negligible resistance, which can not be extracted from short pad.

In Fig. 3-4, we can observe good geometry dependence of extracted resistances, especially $R_{g,int}$. $R_{g,int}$ is dominated mostly by poly-gate and the intersection of $R_{g,int}$ fit line and Y-axis represents the metal resistance from metal-3 to metal-1. Recalling the R_G in Fig. 4-10, $R_{g,ext}$ in Table 4-1, and $R_{g,int}$ in Fig. 3-4, the most surprising thing is that the intersection in Fig. 4-9 almost equals to the one in Fig. 3-4 plus $R_{g,ext}$ in Table 4-1.

4.3 Capacitance extraction and analysis

We usually use Y-parameter matrix to extract capacitances because the coupling capacitances for specific terminal are in parallel. For two port measurement, one signal pad (port1) is connected to gate terminal of MOSFET and the other (port2) is connected to drain terminal. Therefore, we can use following equations to extract the capacitances associated with gate and drain terminals.

$$\left.\frac{\operatorname{Im}\left(Y_{11}^{dut}\right)}{\omega}\right|_{\omega\to 0} = C_{gg} \tag{4.30}$$

$$\left.\frac{\mathrm{Im}\left(Y_{12}^{dut}\right)}{\omega}\right|_{\omega\to 0} = -C_{gd} \qquad (4.31)$$

$$\left.\frac{\mathrm{Im}\left(Y_{22}^{dut}\right)}{\omega}\right|_{\omega\to 0} = C_{gd} + C_{jd} \qquad (4.32)$$

For $V_{gs}>V_{th}$, $C_{gg} = C_{gd} + C_{gs}$ (4.33)

For $V_{gs}<V_{th}$, $C_{gg} = C_{gdo} + C_{gso} + C_{gb}$ (4.34)

4.3.1 Bias dependence

As we discussed early, we still have to extract capacitances at very low frequency. Fig. 4-11 indicates C_{gg} under varying gate voltages. The eventual C_{gg} was calculated by averaging measured data in 2 ~ 5 GHz. Table 4-9 summarizes C_{gg} for various N_F and under varying V_{gs}.

Following the same extraction method, the extracted C_{gd} for various N_F and under varying V_{gs} are shown in Fig. 4-12 and listed in Table 4-10

Table 4-9 The C_{gg} capacitances versus gate voltage at V_{ds}=0V for 3T

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; C_{gg}(fF)							
V_{gs} (V)	0.0	0.2	0.4	0.6	0.8	1.0	1..2
N_F=18	65.85	69.64	85.53	102.55	106.48	106.69	105.94
N_F=36	132.68	140.49	172.91	206.97	214.80	215.23	213.77
N_F=72	266.57	281.89	347.11	416.39	432.04	432.87	429.93

Table 4-10 The C_{gd} capacitances versus gate voltage at V_{ds}=0V for 3T

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; C_{gd}(fF)							
V_{gs} (V)	0.0	0.2	0.4	0.6	0.8	1.0	1..2
N_F=18	29.32	31.92	41.20	51.11	52.87	52.62	52.03

N_F=36	59.45	64.61	83.07	102.98	106.03	105.46	104.24
N_F=72	120.10	130.05	167.34	207.35	213.60	212.64	210.09

We can observe that the C_{gd} is equal to the half of C_{gg} under V_{ds}=0V and V_{gs}>V_{th}, i.e. $C_{gd} = C_{gs} = \frac{C_{gg}}{2}$. The equal partition of gate capacitances between gate to drain and gate to source under V_{ds}=0V accounts for the uniform distribution of inversion carriers in the channel under zero drain bias.

Using (4.30) ~ (4.32), we can also extract C_{gg} and C_{gd} under saturation condition at V_{ds}=1.2V. Table 4-11 ~ 4-13 indicate C_{gg} and C_{gd} extracted for various N_F and under varying gate biases. Figs. 4-13, 4-14 present the C_{gg} and C_{gd} averaged through frequency versus V_{gs} for various N_F. The smaller C_{gg} and C_{gd} under lower V_{gs} account for the drain depletion effect under non-zero V_{ds}.

Table 4-11 The C_{gg} and C_{gd} capacitances versus gate voltage at V_{ds}=1.2V for N_F=18

Average data from 2 ~ 5 GHz ; V_{ds}=1.2V ; N_F=18					
V_{gs} (V)	0.340	0.400	0.454	0.598	0.708
C_{gg} (fF)	69.5	73.0	76.5	84.6	88.4
C_{gd} (fF)	26.7	26.7	26.8	26.9	27.2
V_{gs} (V)	0.800	0.900	0.976	1.064	1.200
C_{gg} (fF)	90.4	91.9	92.7	93.3	94.0
C_{gd} (fF)	27.5	27.8	28.1	28.5	29.1

Table 4-12 The C_{gg} and C_{gd} capacitances versus gate voltage at V_{ds}=1.2V for N_F=36

Average data from 2 ~ 5 GHz ; V_{ds}=1.2V ; N_F=36						
V_{gs} (V)	0.305	0.375	0.400	0.523	0.598	0.711
C_{gg} (fF)	137.0	144.4	147.4	162.9	170.6	178.6
C_{gd} (fF)	53.8	53.9	53.9	54.0	54.2	54.7
V_{gs} (V)	0.804	0.900	0.989	1.173	1.200	

C_{gg} (fF)	182.7	185.5	187.4	189.8	190.0	
C_{gd} (fF)	55.2	55.9	56.6	58.3	58.5	

Table 4-13 The C_{gg} and C_{gd} capacitances versus gate voltage at V_{ds}=1.2V for N_F=72

Average data from 2 ~ 5 GHz ; V_{ds}=1.2V ; N_F=72						
V_{gs} (V)	0.275	0.345	0.400	0.470	0.601	0.717
C_{gg} (fF)	269.9	282.5	295.2	313.6	342.8	358.7
C_{gd} (fF)	108.6	108.7	108.8	108.7	109.3	110.3
V_{gs} (V)	0.770	0.867	0.900	1.000	1.200	
C_{gg} (fF)	363.7	370.3	372.1	376.4	382.2	
C_{gd} (fF)	110.9	112.1	112.6	114.2	118.1	

The extracted C_{gg} and C_{gd} indicate larger capacitance corresponding to increasing V_{gs}, for both V_{ds}=0 and V_{ds}=V_{dd}=1.2V. The experimental results match with the prediction by theory of MOSFET physics that the higher V_{gs} leads to larger gate overdrive and stronger inversion in which more inversion carriers are provided to respond to ac signal.

Besides, C_{gg} tends to decrease at higher V_{ds} even under sufficiently large V_{gs}. Again, it accounts for carrier depletion near drain due to higher V_{ds}.

4.3.2 Frequency dependence

After doing open and short de-embedding for 3T device, it is expected that there should be no parasitic resistance and inductance remained at source terminal. I compile the results and show it in Fig. 4-15 ~ 4-16. We can observe that C_{gg} and C_{gd} are almost frequency independent. This represents that there is indeed no remained parasitic resistance and inductance at source terminal. In the next chapter, I will discuss the capacitance frequency dependence for 4T device in detail to prove that

remained parasitic parameters at source terminal due to short de-embedding banning for 4T device indeed affects capacitance behavior with frequency.

4.3.3 Device geometry dependence

For given gate and drain voltages, we expect that the C_{gg} and C_{gd} capacitances are proportional to finger number (N_F). Take the extracted capacitances under V_{gs}=1.2V, V_{ds}=0 and 1.2V as an example shown in Figs. 4-17 and 4-18, C_{gg} and C_{gd} present good linear relation w.r.t. finger number (N_F). The linear regression lines didn't intersect exactly at the origin.

According to the equivalent circuit of open and short pad shown in Figs. 4-3 and 4-4, the Y_{C3} of open pad includes the coupling capacitance between interconnection metal lines down to metal-1 but, strictly speaking, Y_{C3} of short pad doesn't exist because all metal lines are connected together. Therefore, if we follow the original open de-embedding for short pad, the Y_{C3} term would be subtracted once again. Actually, the Y_{C3} term has been subtracted in advance when we do open de-embedding for measurement. That's why we obtain negative value of intersection in Figs. 4-17 and 4-18. Fortunately, the Y_{C3} term doesn't affect the good geometry dependence greatly and it can be verified by a few fF capacitance values of intersection in figures and coupling capacitance actually extracted from measurement.

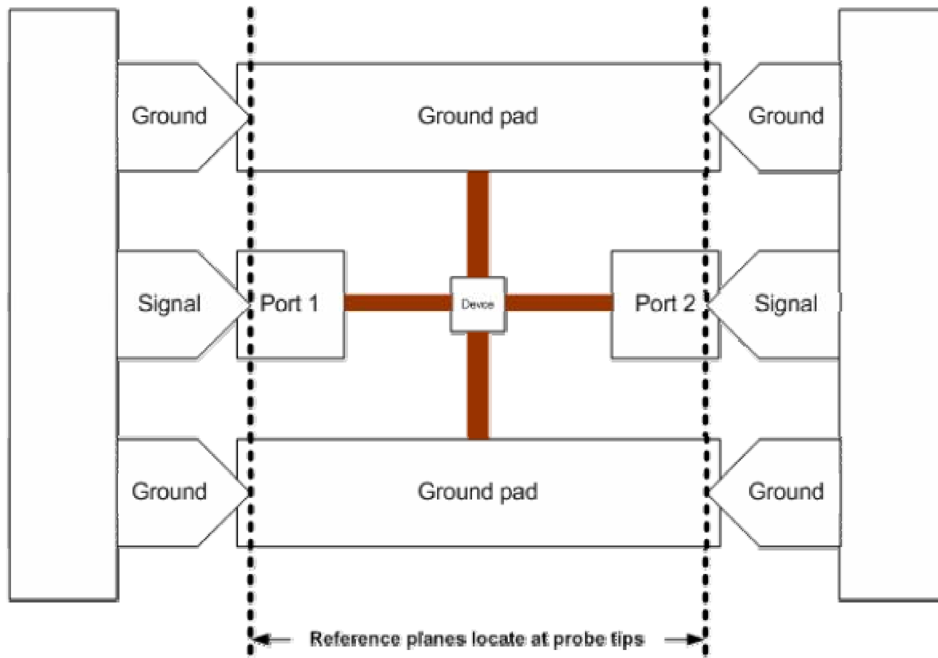

Fig. 4-1 RF measurement for a two-port system

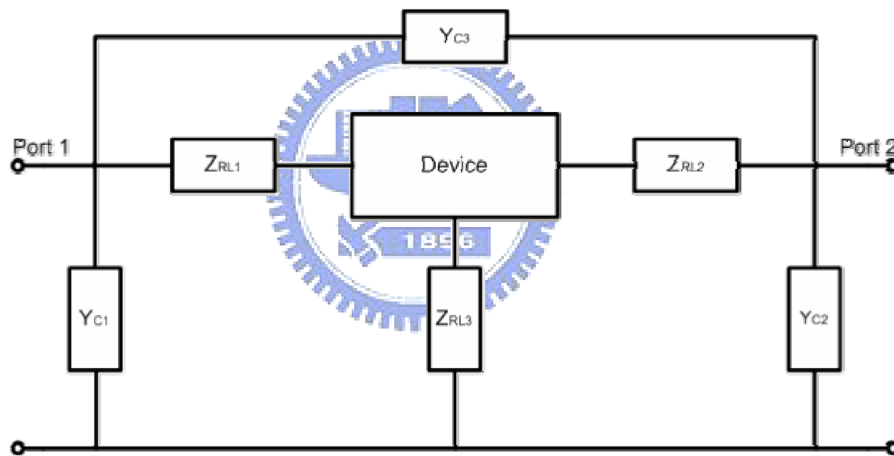

Fig. 4-2 The equivalent circuit of 3T device with pad

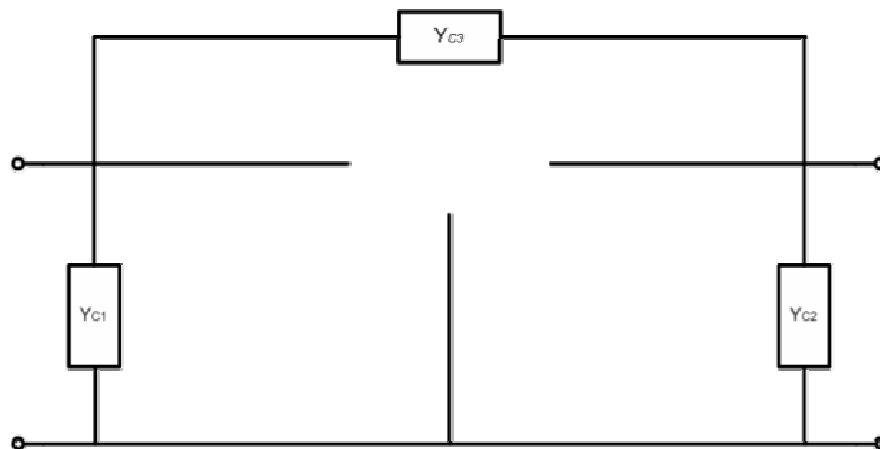

Fig. 4-3 The equivalent circuit of open pad

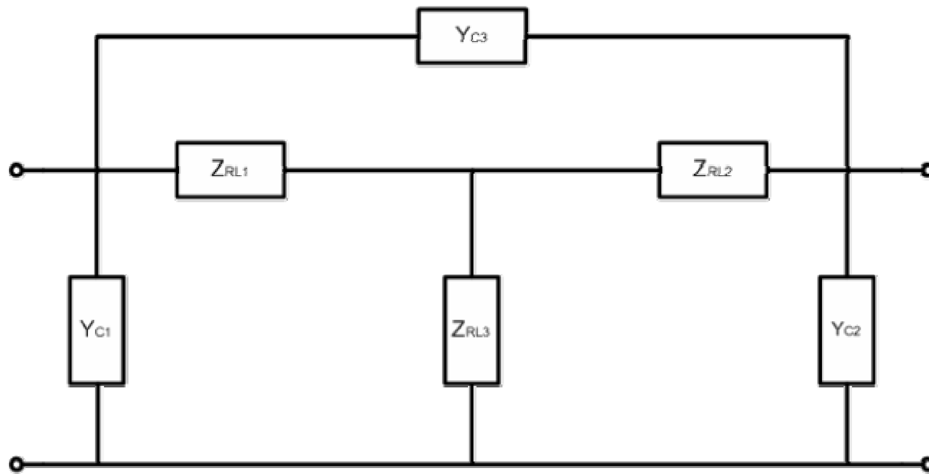

Fig. 4-4 The equivalent circuit of short pad

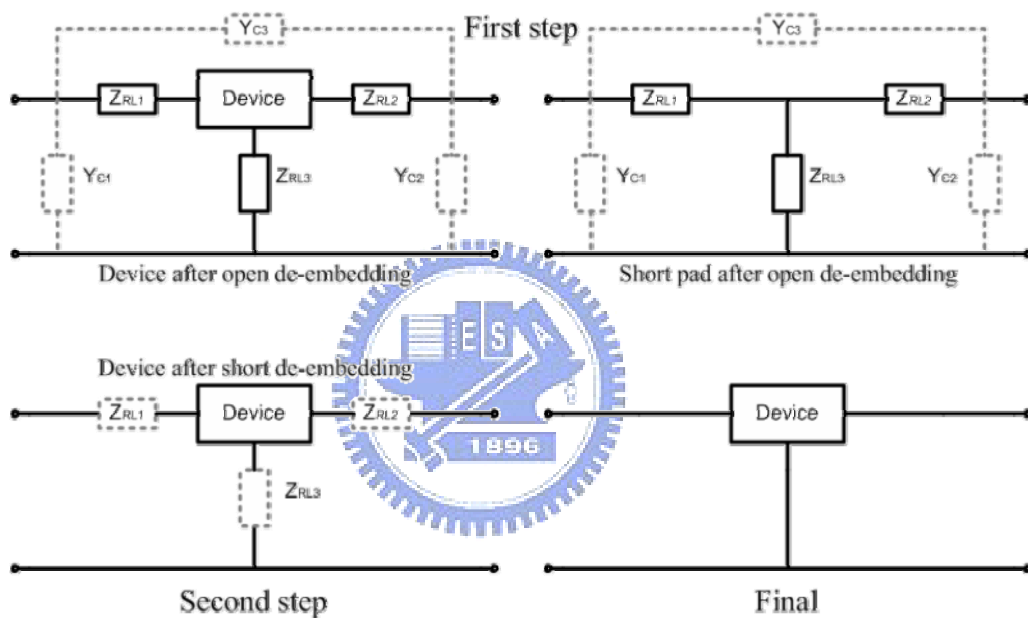

Fig. 4-5 The illustration of de-embedding procedure for 3T device

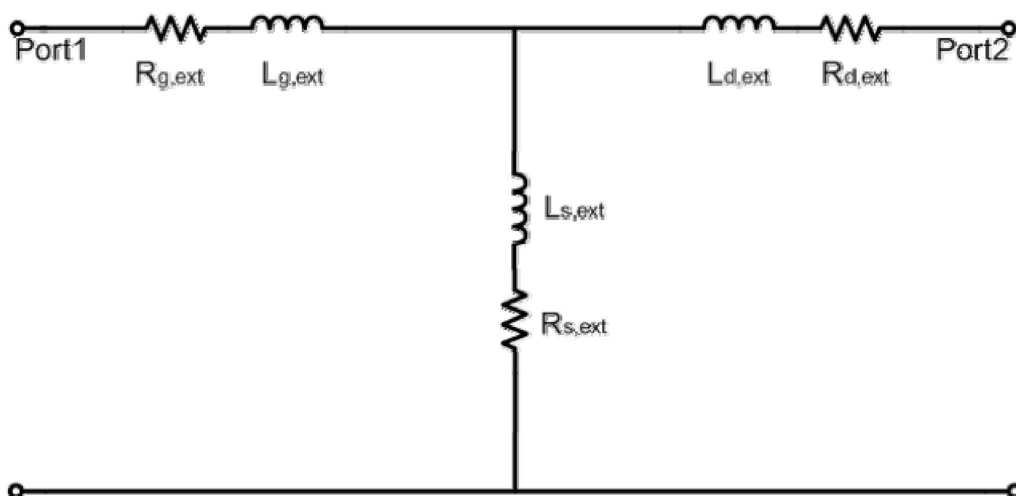

Fig. 4-6 The equivalent circuit of short pad after open de-embedding

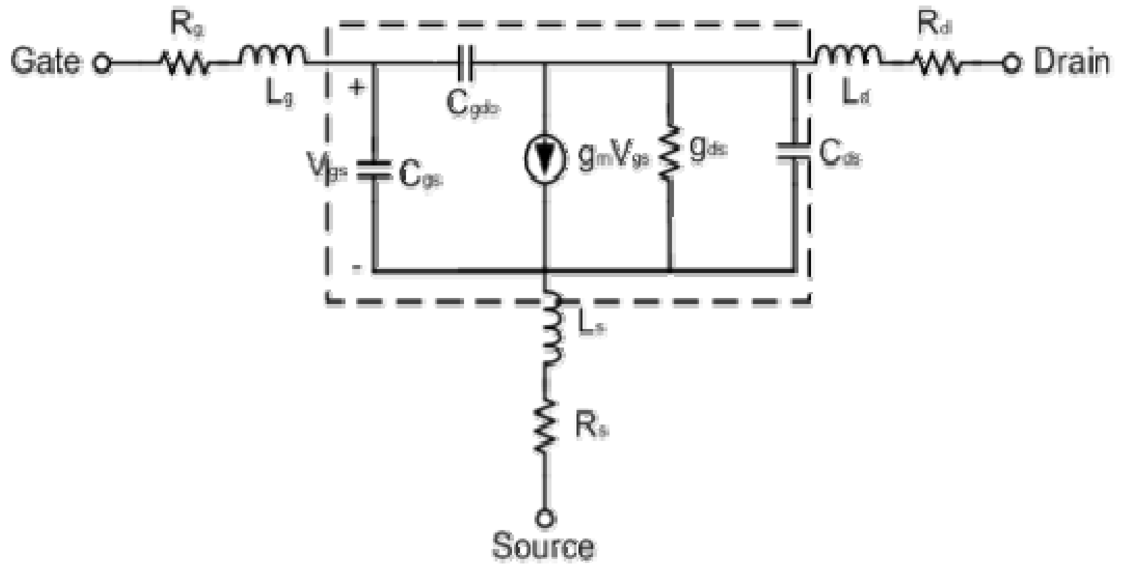

Fig. 4-7 A small-signal equivalent circuit model at saturation region

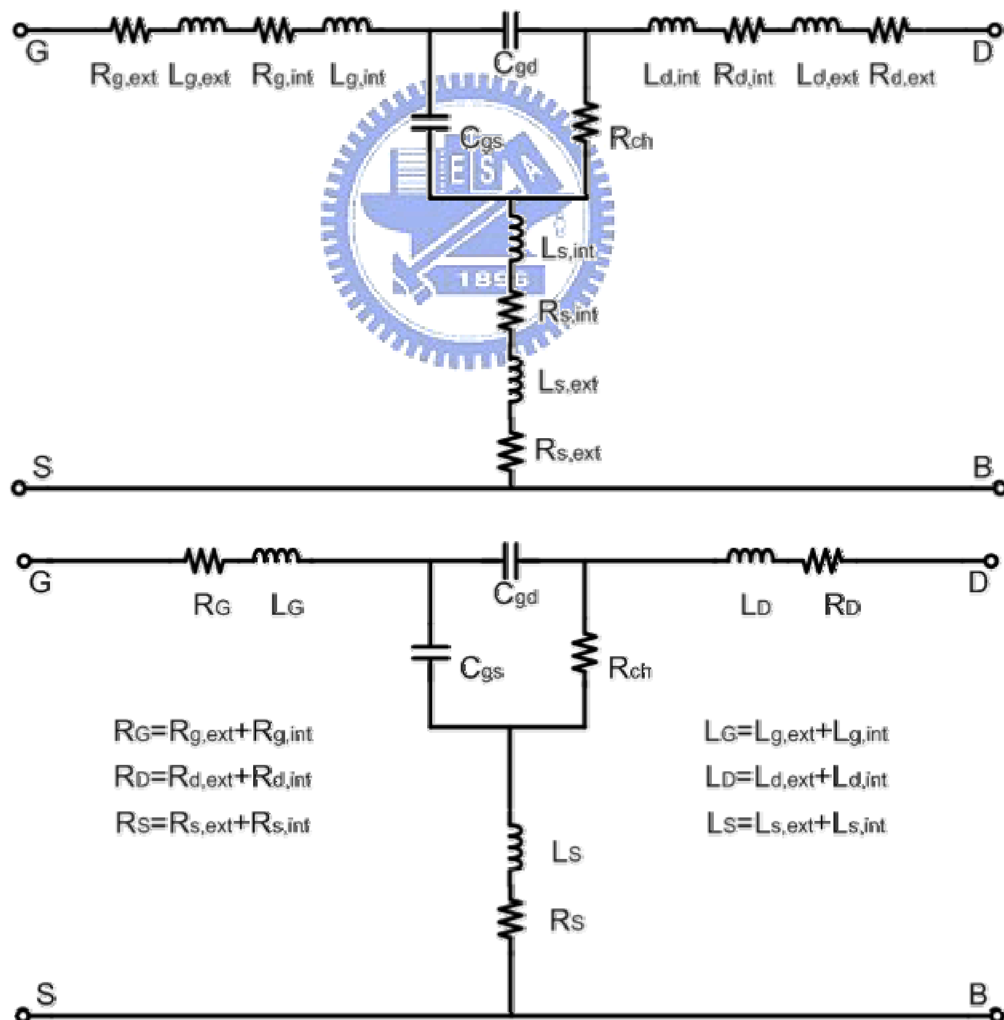

Fig. 4-8 The equivalent circuit of device at $V_{gs}>V_{th}$; $V_{ds}=0V$

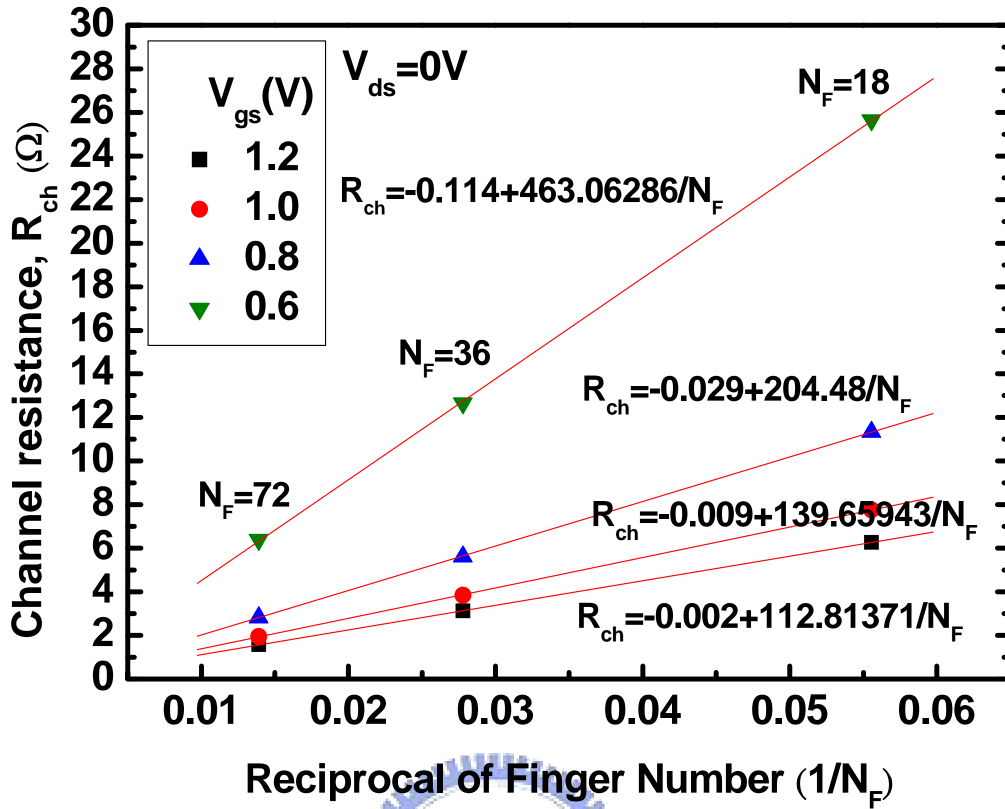

Fig. 4-9 The R_{ch} versus reciprocal of finger number ($1/N_F$)

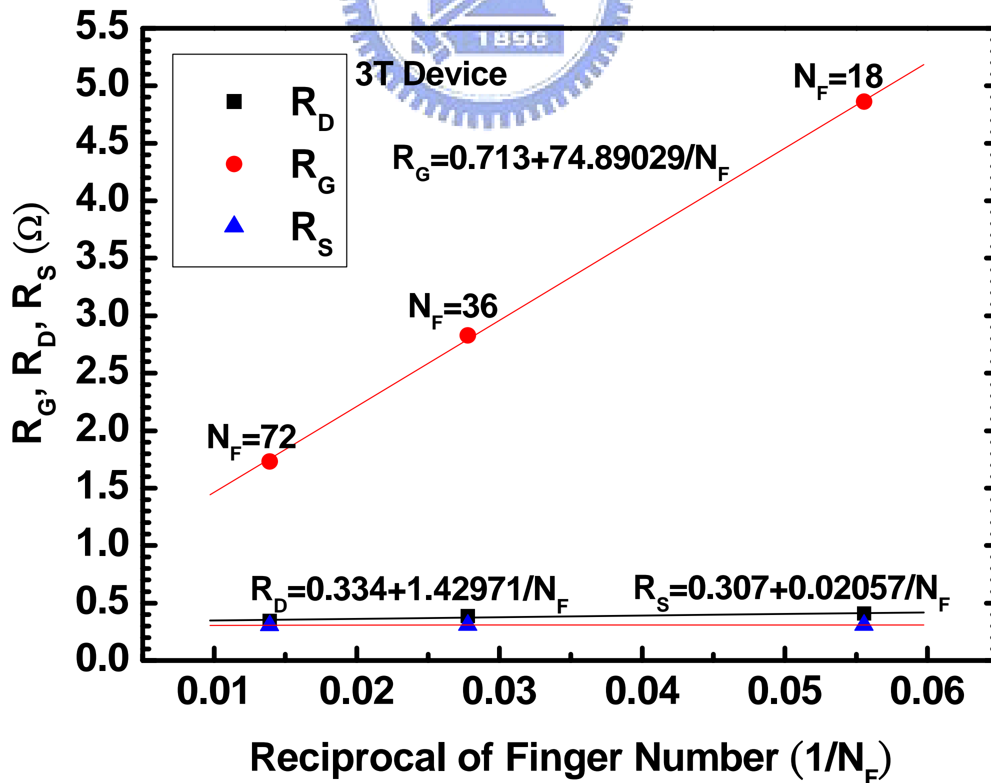

Fig. 4-10 The total parasitic resistance vs. reciprocal of finger number ($1/N_F$) for 3T

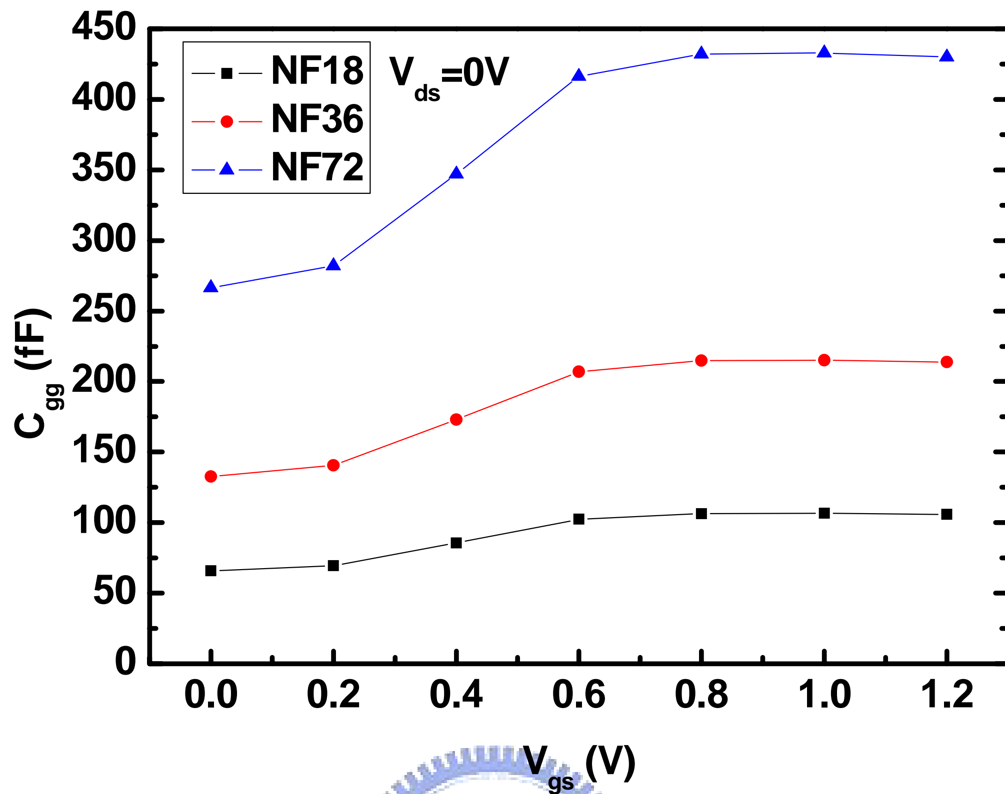

Fig. 4-11 The C_{gg} capacitance vs. gate voltage (V_{gs}) at V_{ds}=0V for 3T

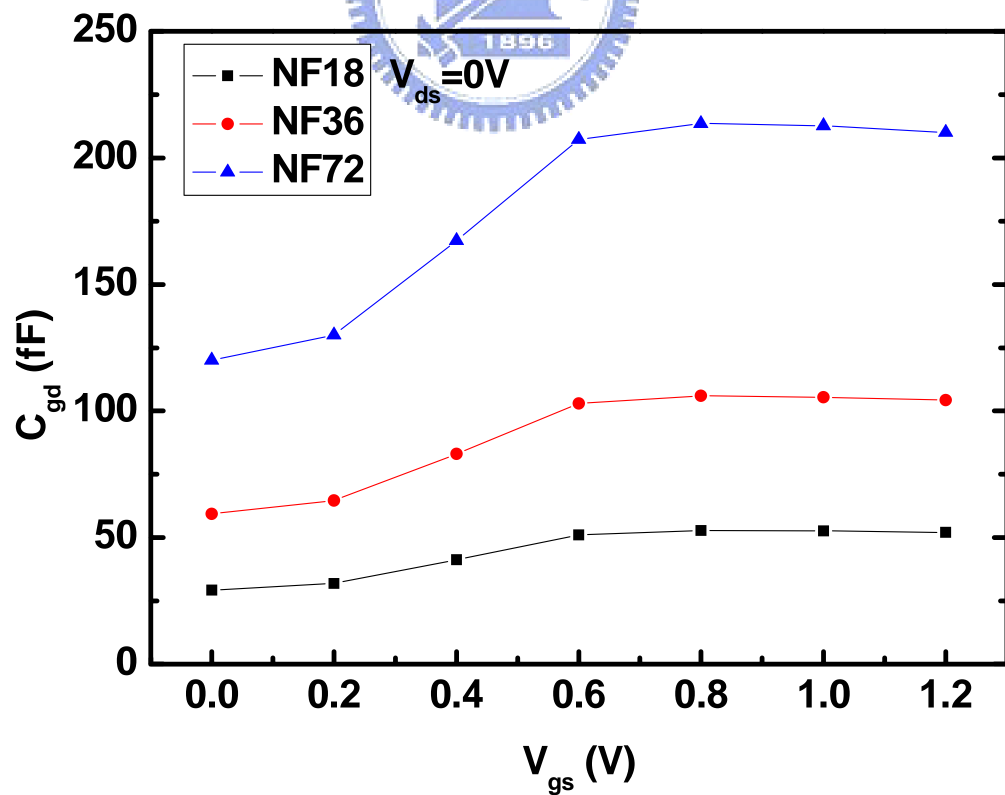

Fig. 4-12 The C_{gd} capacitance vs. gate voltage (V_{gs}) at V_{ds}=0V for 3T

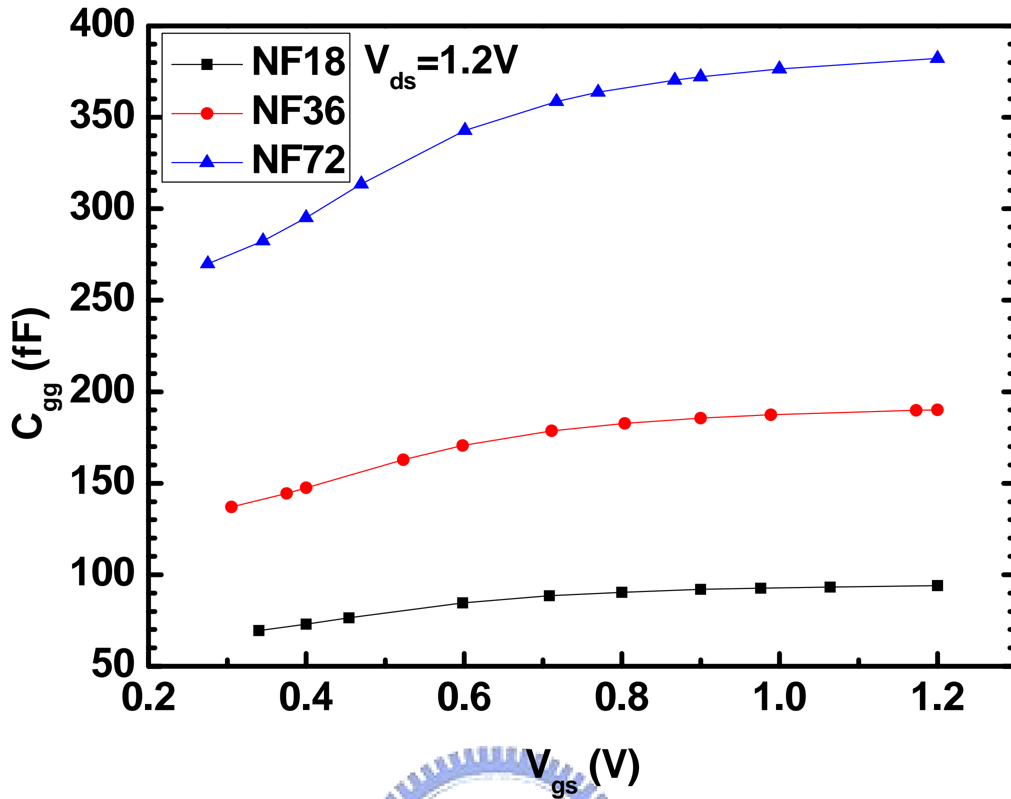

Fig. 4-13 The C_{gg} capacitance vs. gate voltage (V_{gs}) at V_{ds}=1.2V for 3T

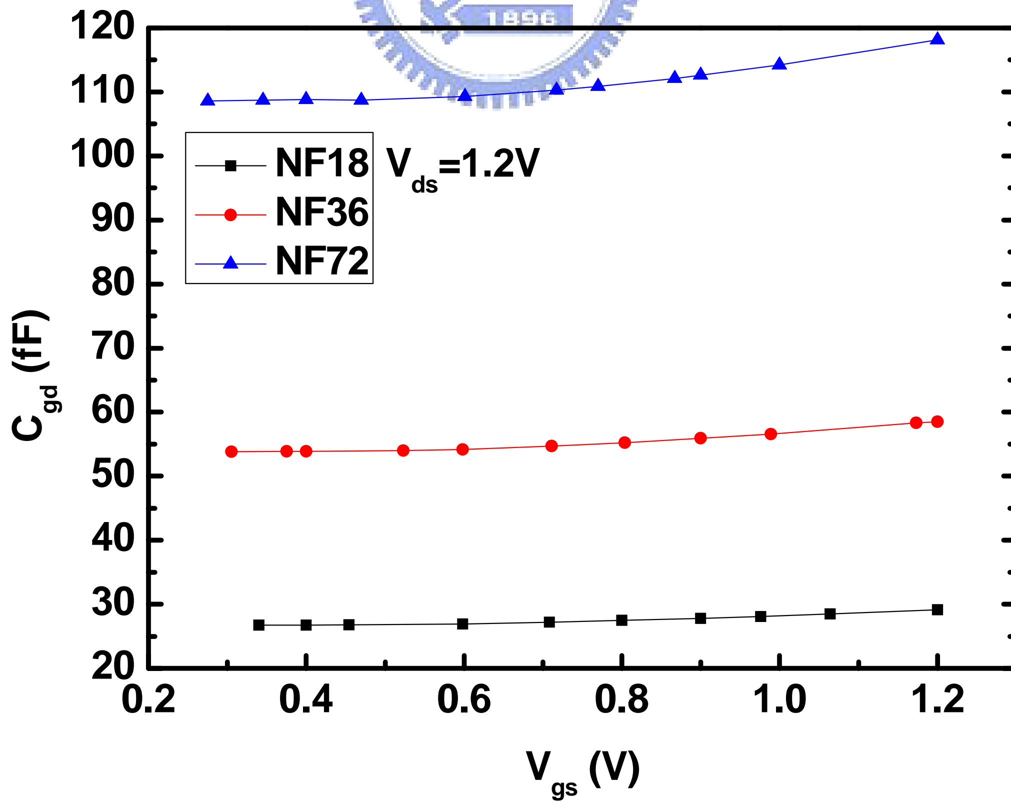

Fig. 4-14 The C_{gd} capacitance vs. gate voltage (V_{gs}) at V_{ds}=1.2V for 3T

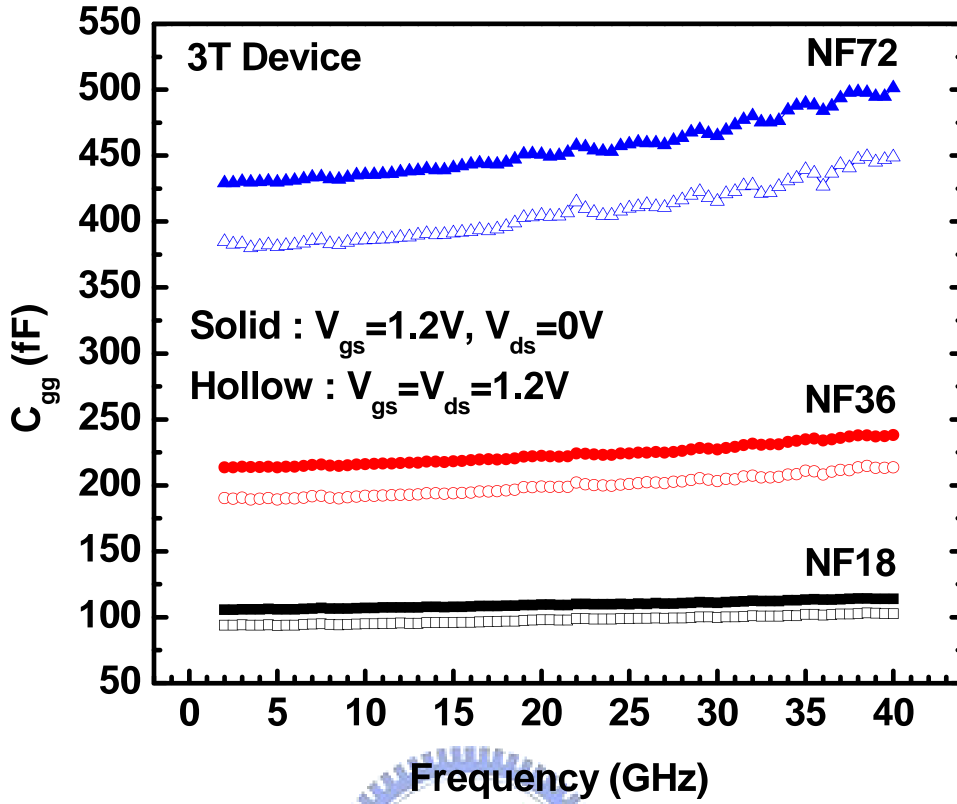

Fig. 4-15 The C_{gg} capacitance vs. frequency at V_{gs}=1.2V with varying V_{ds} for 3T

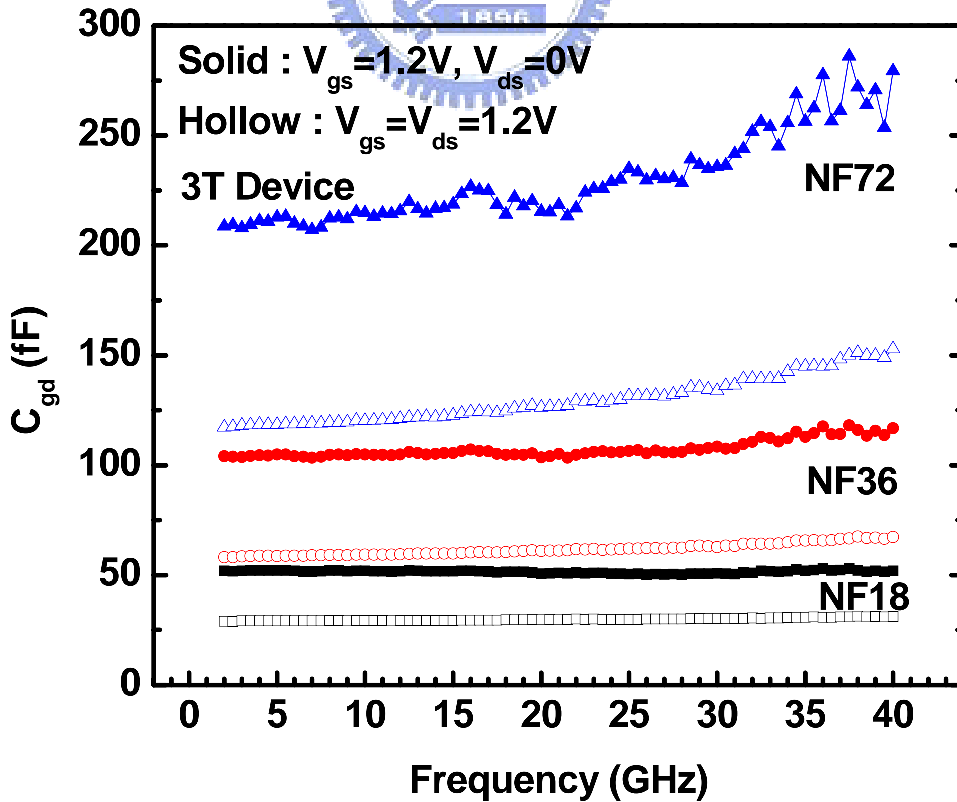

Fig. 4-16 The C_{gd} capacitance vs. frequency at V_{gs}=1.2V with varying V_{ds} for 3T

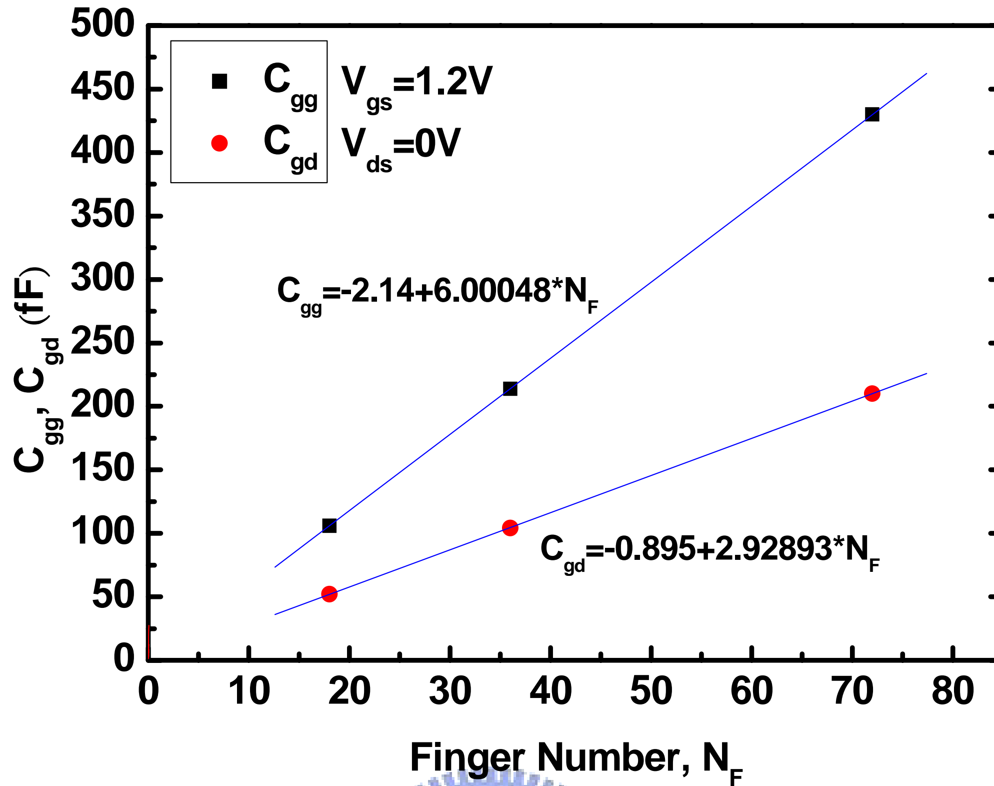

Fig. 4-17 The capacitances vs. finger number at V_{gs}=1.2V and V_{ds}=0V for 3T

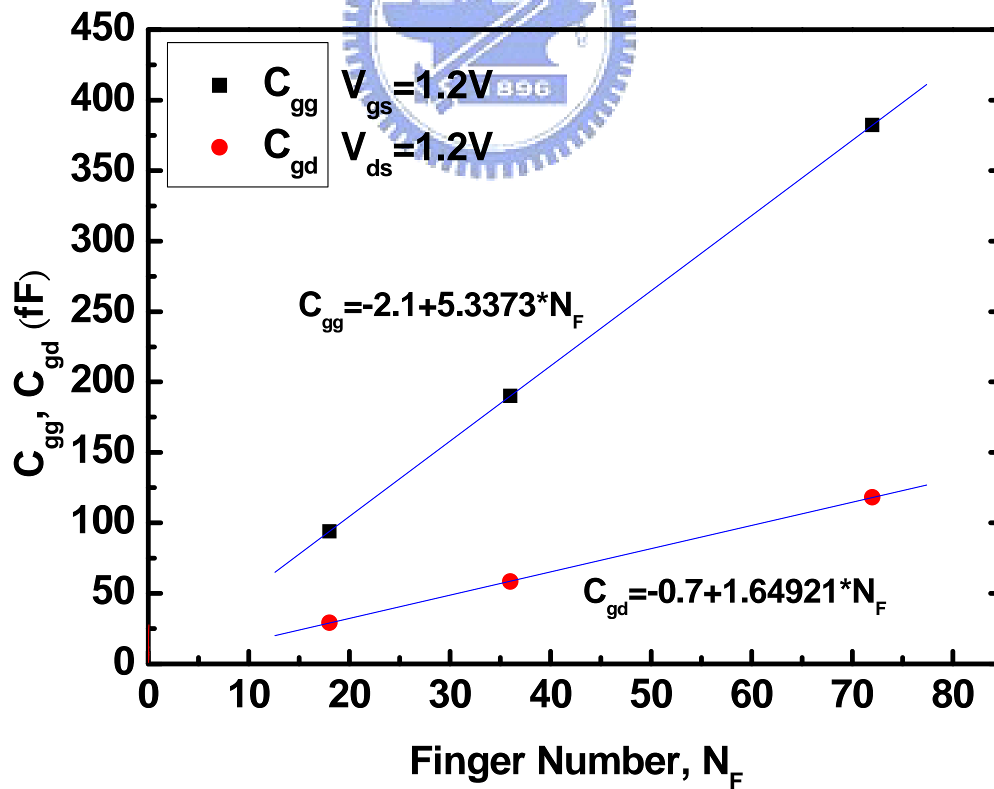

Fig. 4-18 The capacitances vs. finger number at V_{gs}=1.2V and V_{ds}=1.2V for 3T