Chapter 5

4T RF MOSFET Model Parameter Extraction

5.1 De-embedding methods

The device whose source and bulk terminals are separated is called 4T device. The equivalent circuit is illustrated in Fig. 5-1. Obviously, we can do open de-embedding directly on the DUT but difficulty comes out for short de-embedding because source and body are two independent terminals which are connected to ground individually. For this situation, we have to modify our extraction method slightly.

Fig. 5-2 illustrates the de-embedding flow for 4T device. The open de-embedding can be done on both device and short pad but there is difficulty to complete the short de-embedding for 4T structure. Even though Z_{RL1} and Z_{RL2} can be extracted from short pad individually and then be used to take off the parasitic impedance associated with gate and drain terminals. The revised de-embedding method will leave Z_{RL3} and Z_{RL4}, which cannot be extracted directly by short pad.

5.2 Parasitic resistance and inductance extraction and analysis

To perform parasitic resistance and inductance extraction for 4T MOSFETs, we make an assumption that R_{ch} resistances of 3T and 4T devices are equal under the same gate voltage. This assumption is reasonable because of the same layout for all layers under metal-3 and manufacturing technology. Based on this assumption, we can do parameters extraction as follows.

5.2.1 Parasitic RL extraction from device

Fig. 5-3 illustrates the device schematic after open de-embedding under $V_{gs}>V_{th}$ and V_{ds}=0V. As long as we extract parameters at low frequency, there should be no any difference in equivalent circuit for 3T and 4T device. Therefore, the extraction method discussed in previous chapter is reusable. Based on comparison of layout between 3T and 4T devices, we expect that the parasitic resistances and inductances of 4T device will be the same as those of 3T device except R_S and L_S.

Using the following equations derived in previous chapter and the assumption in 5.2 section, all parameters for 4T device can be extracted.

$$\mathrm{Re}\left(Z_{12}^{dut}\right) \approx \frac{R_{ch}}{2} \Rightarrow R_{ch} = 2 \cdot \mathrm{Re}\left(Z_{12}^{dut}\right) \quad (4.22)$$

$$\mathrm{Re}\left(Z_{12}^{mea_o}\right) = R_S + \frac{R_{ch}}{2} \quad (4.23)$$

$$\mathrm{Re}\left(Z_{22}^{mea_o}\right) = R_D + R_S + R_{ch} \quad (4.24)$$

$$\mathrm{Re}\left(Z_{11}^{mea_o}\right) = R_G + R_S + \frac{R_{ch}}{4} \quad (4.25)$$

$$\left.\frac{\mathrm{Im}\left(Z_{12}^{mea_o}\right)}{\omega}\right|_{\omega \to 0} = L_S - \frac{C_{gd} R_{ch}^2}{4} \quad (4.27)$$

$$\left.\frac{\mathrm{Im}\left(Z_{22}^{mea_o}\right)}{\omega}\right|_{\omega \to 0} = L_D + L_S - \frac{C_{gd} R_{ch}^2}{2} \quad (4.28)$$

$$\left.\frac{\mathrm{Im}\left(Z_{11}^{mea_o}\right)}{\omega}\right|_{\omega \to 0} = L_G + L_S - \frac{1}{2\omega^2 C_{gd}} \quad (4.29)$$

I extract the R_S by averaging the data of 2 ~ 5 GHz. Table 5-1 is the list of R_S versus gate voltage.

Table 5-1 The extracted total parasitic source resistance R_S

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; $R_S(\Omega)$

V_{gs} (V)	1.2	1.0	0.8	0.6	Avg.
N_F=18	0.770	0.773	0.767	0.748	0.765
N_F=36	0.833	0.832	0.833	0.840	0.835
N_F=72	0.917	0.917	0.914	0.897	0.911

The R_D and R_G were calculated by averaging the data in 2 ~ 5 GHz. Table 5-2 and 5-3 summarize R_D and R_G under varying gate voltage.

Table 5-2 The extracted total parasitic drain resistance R_D

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; $R_D(\Omega)$					
V_{gs} (V)	1.2	1.0	0.8	0.6	Avg.
N_F=18	0.436	0.419	0.381	~~0.255~~	0.412
N_F=36	0.381	0.379	0.372	0.368	0.375
N_F=72	0.343	0.341	0.335	0.320	0.335

Table 5-3 The extracted total parasitic gate resistance R_G

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; $R_G(\Omega)$					
V_{gs} (V)	1.2	1.0	0.8	0.6	Avg.
N_F=18	3.834	3.626	3.618	3.790	3.717
N_F=36	2.635	2.541	2.511	2.634	2.580
N_F=72	1.725	1.675	1.668	1.742	1.703

As shown in Table 5-4, the comparison between 3T and 4T devices for R_G and R_D indicates very close value except the abnormally large difference at R_G for N_F=18. It accounts for measurement error. We concluded that R_G extracted from 3T device is more reliable due to better device geometry dependence. The results match with our expectation very well.

Table 5-4 The comparison of parasitic resistances of 3T and 4T devices

	R_G (Ω)			R_D (Ω)			R_S (Ω)		
	3T	4T	Short	3T	4T	Short	3T	4T	Short
N_F=18	4.862	3.717	0.328 (M8 ~M3)	0.409	0.412	0.314 (M8 ~M3)	0.308	0.765	0.308 (M8 ~M3)
N_F=36	2.828	2.580		0.387	0.375		0.308	0.835	
N_F=72	1.730	1.703		0.345	0.335		0.307	0.911	

Larger R_S extracted for 4T device can be explained by the major layout difference at source and bulk between 3T and 4T devices. For 3T device layout, there are two parallel paths for signal to propagate to source because source and bulk terminals are shorted together. But there is only one way for 4T device to go to source terminal.

The eventual L_S and L_D were calculated by averaging the data in 2 ~ 5 GHz. But L_G was calculated by averaging the data over higher frequencies in 30 ~ 40 GHz. The reason has been discussed in previous chapter. Table 5-5 ~ 5-7 summarize L_S, L_D, and L_G versus gate voltage.

Table 5-5 The extracted total parasitic source inductance L_S

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; L_S(pH)				
V_{gs} (V)	1.2	1.0	0.8	Avg.
N_F=18	53.43	52.83	51.31	53.19
N_F=36	55.83	55.57	54.84	55.41
N_F=72	56.81	56.67	56.15	56.54

Table 5-6 The extracted total parasitic drain inductance L_D

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; L_D(pH)				
V_{gs} (V)	1.2	1.0	0.8	Avg.
N_F=18	54.25	54.02	52.93	53.73

N_F=36	51.53	51.36	50.48	51.12
N_F=72	49.88	49.66	49.28	49.61

Table 5-7 The extracted total parasitic gate inductance L_G

Average data from 30 ~ 40 GHz ; V_{ds}=0V ; L_G(pH)				
V_{gs} (V)	1.2	1.0	0.8	Avg.
N_F=18	69.50	66.10	62.31	65.97
N_F=36	55.46	54.72	53.74	54.64
N_F=72	48.67	48.92	49.18	48.92

Table 5-8 The comparison of parasitic inductances of 3T and 4T devices

	L_G (Ω)			L_D (Ω)			L_S (Ω)		
	3T	4T	Short	3T	4T	Short	3T	4T	Short
N_F=18	67.31	65.97	55.43	50.20	53.73	51.51	15.37	53.19	17.67
N_F=36	54.68	54.64	(M8	50.15	51.12	(M8	16.31	55.41	(M8
N_F=72	47.69	48.92	~M3)	49.09	49.61	~M3)	16.45	56.54	~M3)

The comparison of all three terminal parasitic inductances, L_G, L_D, and L_S between 3T and 4T was demonstrated in Table 5-8. We can see that 3T and 4T devices show very close values in term of L_G and L_D. It accounts for the same layout at gate and drain terminals for 3T and 4T devices. As for the source inductance (L_S), the obviously larger L_S revealed by 4T device can be resorted to the same reason described for R_S.

5.2.2 Frequency and bias dependence

Obviously, the extracted resistance and inductance of 4T device are like those of 3T device—bias independent. This means that we can obtain the same parameter values of metal line under any gate voltage as long as we extract them under V_{gs}>V_{th} and V_{ds}=0V.

But there are two parameters, R_S and L_S, have obvious frequency dependence. Because the source and bulk terminals of 4T device are not parallel, we can expect that the values of R_S and L_S will be larger than those of 3T device naturally. The large L_S is the key parameter that induces frequency dependence. That is why the R_S and L_S have large change range with frequency. And we will discuss later that L_S is also the key parameter to capacitance frequency dependence for 4T device.

5.2.3 Device geometry dependence

In Fig. 5-4, it shows three kinds of total parasitic resistance—R_S, R_D, and R_G. R_S is not a constant versus finger number anymore. In chapter 4, we mentioned that the resistance contributed by metal-3 ~ metal-1 is very small and can be neglected. As for 4T device layout, larger finger number may lead to larger R_S resistance because of longer metal line from metal-8 to metal-3. As shown in Fig. 5-4, the negative slope revealed by R_S versus $1/N_F$ accounts for our expectation.

The R_D resistances extracted from 4T device are very close to those of 3T device. This result is consistent with our prediction. Similarly, there should be the same result for R_G. We indeed observe that R_G resistances of 3T and 4T devices are close except N_F=18. The deviation may come from measurement error. Due to the fact we suggest to take those of 3T device as the standard and reference values.

5.3 Capacitance extraction and analysis

Although we can not do short de-embedding directly for 4T devices, we still can use Y-parameter matrix to extract capacitances. Based on the extraction equations discussed in chapter 4, the extraction equations for 4T devices are shown below:

$$\left.\frac{\mathrm{Im}\left(Y_{11}^{mea_o}\right)}{\omega}\right|_{\omega\to 0} = C_{gg} \quad (5.1)$$

$$\left.\frac{\mathrm{Im}\left(Y_{12}^{mea_o}\right)}{\omega}\right|_{\omega\to 0} = -C_{gd} \quad (5.2)$$

$$\left.\frac{\mathrm{Im}\left(Y_{22}^{mea_o}\right)}{\omega}\right|_{\omega\to 0} = C_{gd} + C_{jd} \quad (5.3)$$

For $V_{gs}>V_{th}$, $C_{gg} = C_{gd} + C_{gs}$ (5.4)

For $V_{gs}<V_{th}$, $C_{gg} = C_{gdo} + C_{gso} + C_{gb}$ (5.5)

Regarding the 3T and 4T layout on gate capacitances, an interesting result has been identified and will be demonstrated in the following sections. Source terminal parasitic R and L which can not be de-embedded directly would influence greatly the extracted gate capacitances of 4T devices. We will discuss what the real capacitances are for 4T devices in terms of device physics and circuit design.

5.3.1 Bias dependence

Following the extraction equations given by (5.1) ~ (5.3), the gate capacitances were extracted in very low frequencies. Figs. 5-6 ~ 5-7 present C_{gg} and C_{gd} under varying gate voltage. C_{gg} was extracted by averaging measured data in 2 ~ 5 GHz. The averaged data is listed in Table 5-9.

$$\left.\frac{\mathrm{Im}\left(Y_{11}^{mea_o}\right)}{\omega}\right|_{\omega\to 0} = C_{gg} \quad ; \quad \left.\frac{\mathrm{Im}\left(Y_{12}^{mea_o}\right)}{\omega}\right|_{\omega\to 0} = -C_{gd}$$

Table 5-9 The C_{gg} capacitances versus gate voltage at V_{ds}=0V for 3T

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; C_{gg}(fF)							
V_{gs} (V)	0.0	0.2	0.4	0.6	0.8	1.0	1..2
N_F=18	65.30	69.19	85.10	102.07	106.02	106.21	105.46

N_F=36	132.56	140.39	172.56	207.00	214.93	215.34	213.84
N_F=72	268.70	284.54	350.90	421.55	437.42	438.17	435.08

Following the same extraction method, the results of C_{gd} are listed in Table 5-10.

Table 5-10 The C_{gd} capacitances versus gate voltage at V_{ds}=0V for 3T

Average data from 2 ~ 5 GHz ; V_{ds}=0V ; C_{gd}(fF)							
V_{gs} (V)	0.0	0.2	0.4	0.6	0.8	1.0	1..2
N_F=18	29.44	32.10	41.47	51.96	54.53	54.97	54.76
N_F=36	59.82	64.97	83.67	107.01	114.23	116.08	116.19
N_F=72	121.91	132.15	171.61	226.30	244.82	248.90	248.59

Figs. 5-8 and 5-9 indicate the comparison between 3T and 4T devices for extracted C_{gg} and C_{gd}. We can observe clearly that C_{gg} is almost the same but C_{gd} of 4T device is obviously larger than that of 3T device. The equivalent circuit illustrated in Fig. 5-10 is proposed to explain the mechanism responsible for 3T and 4T configuration effect on extracted C_{gg} and C_{gd}. Extraction equations are shown as follows:

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} \quad (5.6)$$

$$I_1 = sC_{gd}V_1 + sC_{gs}(V_1 - V_{ns})$$

$$Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0} \quad (5.7)$$

$$-I_1 = sC_{gd}V_2 + sC_{gs}V_{ns}$$

Due to the fact that source and bulk terminals are separated for 4T device, the general short de-embedding is no longer valid for 4T device. Therefore, the parasitic impedance was remained at source terminal in the equivalent circuit. For extraction of C_{gg} through (5.6), port 2 is ground (V_2=0) and the internal source node voltage, V_{ns}, approach zero. So, we can get C_{gg} with nearly identical value for 3T and 4T devices. But the situation for C_{gd} extraction is totally different. When I use Y_{12} to extract C_{gd}, port 1 is grounded but port 2 is connected to V_2 ($V_2 \neq 0$). The non-zero voltage at port 2 would raise the internal source node voltage V_{ns} and then add extra current of

$sC_{gs}V_{ns}$ to the gate terminal current I_1. According to (5.7) to extract C_{gd}, the increase of I_1 will lead to larger C_{gd}.

Using (5.1) ~ (5.3), we also can extract C_{gg} and C_{gd} capacitances under V_{ds}=1.2V. Table 5-11 ~ 5-13 summarize the extracted C_{gg} and C_{gd} for 4T MOSFET of various N_F under varying V_{gs}. Note that C_{gg} and C_{gd} were calculated by averaging the capacitance in 2 ~ 5 GHz. Some interesting results will be demonstrated as follows.

Table 5-11 The C_{gg} and C_{gd} capacitances versus gate voltage at V_{ds}=1.2V for N_F=18

Average data from 2 ~ 5 GHz ; V_{ds}=1.2V ; N_F=18				
V_{gs} (V)	0.400	0.453	0.598	0.708
C_{gg} (fF)	72.4	75.5	82.7	86.1
C_{gd} (fF)	26.9	26.9	27.1	27.4
V_{gs} (V)	0.805	0.986	1.076	1.200
C_{gg} (fF)	87.9	89.9	90.5	91.2
C_{gd} (fF)	27.7	28.3	28.7	29.3

Table 5-12 The C_{gg} and C_{gd} capacitances versus gate voltage at V_{ds}=1.2V for N_F=36

Average data from 2 ~ 5 GHz ; V_{ds}=1.2V ; N_F=36				
V_{gs} (V)	0.400	0.525	0.601	0.720
C_{gg} (fF)	146.3	159.1	164.6	170.0
C_{gd} (fF)	54.3	54.5	54.8	55.4
V_{gs} (V)	0.820	0.900	1.017	1.200
C_{gg} (fF)	172.9	174.6	176.6	179.0
C_{gd} (fF)	56.1	56.7	57.8	59.6

Table 5-13 The C_{gg} and C_{gd} capacitances versus gate voltage at V_{ds}=1.2V for N_F=72

Average data from 2 ~ 5 GHz ; V_{ds}=1.2V ; N_F=72					
V_{gs} (V)	0.400	0.470	0.530	0.614	0.680

C_{gg} (fF)	294.1	306.7	314.2	320.4	323.6
C_{gd} (fF)	110.4	110.6	111.0	112.0	112.9
V_{gs} (V)	0.742	0.801	0.900	1.080	1.200
C_{gg} (fF)	325.9	328.0	331.1	336.2	339.5
C_{gd} (fF)	113.8	114.8	116.5	120.2	123.0

Figs. 5-11 and 5-12 indicate C_{gg} and C_{gd} extracted for 4T MOSFET of various N_F under varying V_{gs}. Figs. 5-13 and 5-14 present the comparison between 3T and 4T device in terms of C_{gg} and C_{gd}. We can observe that C_{gd} of 4T device are larger than those of 3T device while C_{gg} reveal opposite trend, i.e. the 4T devices demonstrate smaller C_{gg} than 3T. Fig. 5-15 illustrate the equivalent circuit schematics to explain internal source node voltage V_{ns} effect on extraction of C_{gg}, C_{gd} under V_{ds}=1.2V. Under drain bias at 1.2V (V_{ds}=1.2V), there is a current flowing through the source impedance Z_{ns}. Consequently, the voltage V_{ns} would not be zero and will increase with increasing finger number due to larger g_m associated with N_F. For example, 4T N_F=72 device has the largest g_m and drain current than the other two finger numbers. Therefore, it will experience the highest V_{ns}. From (5.6), $I_1 = sC_{gd}V_1 + sC_{gs}(V_1 - V_{ns})$ for extraction of C_{gg}, we can understand why the extracted C_{gg} is always smaller for 4T devices than that of 3T device and the difference in extracted C_{gg} tends to increase with increasing finger number (N_F).

The same explanation can be applied to C_{gd}. Based on (4.7) given by, $-I_1 = sC_{gd}V_2 + sC_{gs}V_{ns}$, C_{gd} extracted for 4T devices will be always larger than that of 3T device. Again, the difference between 3T and 4T devices in terms of C_{gd} will increase with increasing finger number (N_F).

5.3.2 Revised method to extract gate capacitances

We believe that the gate capacitances of 3T and 4T devices should be equal because of the same layout under metal-3 layer. The difference revealed by Fig. 5-13 and 5-14 is caused by the failure of Z_{ns} removal through short de-embedding.

According to the above discussion, we have to derive another method to take off parasitic source impedance Z_{ns}. To begin the work, we follow the original extraction principle, i.e. to extract the gate capacitances at very low frequency. At sufficiently low frequency, we can neglect bulk terminal and parasitic inductances. Based on the validated approximation, we can use the source resistance we've extracted to construct a source impedance matrix Z_{ns}. This matrix can help us to de-embed Z_{ns} and extract gate capacitances of better consistence with that of 3T device. The source impedance matrix is represented as follows.

$$Z_{ns} = \begin{bmatrix} R_S & R_S \\ R_S & R_S \end{bmatrix} \tag{5.8}$$

$$Z_{mea_o} - Z_{ns} = Z^{\text{int}}; \quad Z^{\text{int}} \rightarrow Y^{\text{int}} \tag{5.9}$$

$$\text{Im}\left(Y_{11}^{\text{int}}\right) = \omega C_{gg} \tag{5.10}$$

$$\text{Im}\left(Y_{12}^{\text{int}}\right) = -\omega C_{gd} \tag{5.11}$$

Table 5-14 ~ 5-18 indicate the capacitances extracted following source impedance de-embedding. Figs. 5-16 ~ 5-19 present the comparison between 3T and 4T devices after Z_{ns} de-embedding. Much better consistence between 3T and 4T devices is realized for both C_{gg} and C_{gd}.

Table 5-14 The C_{gg} capacitances versus gate voltage at V_{ds}=0V by revised method

(Source impedance de-embedding method) Average data from 2 ~ 5 GHz ; C_{gg}(fF)							
V_{gs} (V)	0.0	0.2	0.4	0.6	0.8	1.0	1.2
N_F=18	65.30	69.20	85.10	102.04	105.99	106.19	105.45

N_F=36	132.57	140.40	172.53	206.87	214.85	215.30	213.82
N_F=72	268.76	284.60	350.80	421.15	437.28	438.14	435.09

Table 5-15 The C_{gd} capacitances versus gate voltage at V_{ds}=0V by revised method

(Source impedance de-embedding method) Average data from 2 ~ 5 GHz ; C_{gd}(fF)							
V_{gs} (V)	0.0	0.2	0.4	0.6	0.8	1.0	1..2
N_F=18	29.43	32.08	41.27	50.47	51.28	50.54	49.61
N_F=36	59.79	64.91	82.87	100.69	101.98	100.96	99.83
N_F=72	121.75	131.91	168.30	202.09	207.56	208.85	208.41

Table 5-16 The C_{gg} and C_{gd} capacitances versus gate at V_{ds}=1.2V voltage for N_F=18

(Source impedance de-embedding method) Average data from 2 ~ 5 GHz ; N_F=18				
V_{gs} (V)	0.400	0.453	0.598	0.708
C_{gg} (fF)	72.7	76.1	84.4	88.3
C_{gd} (fF)	26.9	26.9	27.0	27.2
V_{gs} (V)	0.805	0.986	1.076	1.200
C_{gg} (fF)	90.4	92.7	93.3	93.9
C_{gd} (fF)	27.5	28.1	28.5	29.1

Table 5-17 The C_{gg} and C_{gd} capacitances versus gate voltage at V_{ds}=1.2V for N_F=36

(Source impedance de-embedding method) Average data from 2 ~ 5 GHz ; N_F=36				
V_{gs} (V)	0.400	0.525	0.601	0.720
C_{gg} (fF)	147.6	163.8	171.5	179.4
C_{gd} (fF)	54.2	54.2	54.3	54.7
V_{gs} (V)	0.820	0.900	1.017	1.200
C_{gg} (fF)	183.3	185.4	187.6	189.8
C_{gd} (fF)	55.3	55.8	56.7	58.4

Table 5-18 The C_{gg} and C_{gd} capacitances versus gate voltage at V_{ds}=1.2V for N_F=72

(Source impedance de-embedding method) Average data from 2 ~ 5 GHz ; N_F=72					
V_{gs} (V)	0.400	0.470	0.530	0.614	0.680
C_{gg} (fF)	299.4	318.8	333.4	347.6	354.8
C_{gd} (fF)	110.0	109.7	109.6	109.9	110.3
V_{gs} (V)	0.742	0.801	0.900	1.080	1.200
C_{gg} (fF)	359.6	363.0	367.4	372.9	375.7
C_{gd} (fF)	111.0	111.7	113.0	116.1	118.7

5.3.3 Frequency dependence

We compile some capacitance results which are done open de-embedding only in Fig. 5-20 ~ 5-21 to discuss the frequency dependence. We can observe that the results of 4T device have obvious frequency dependence.

Fig. 5-22 is the simplified equivalent circuit seeing into from source node, Z_{ns}, to outer ground. The real and imaginary part of $Z_{ns}(\omega)$ extraction equations are below:

$$\begin{aligned} \mathrm{Re}(Z_{ns}(\omega)) &\cong \frac{R_S + \omega^4 R_b L_S^2 C_{js}^2 + \omega^2 R_S R_b (R_S + R_b) C_{js}^2}{(1-\omega^2 L_S C_{js})^2 + \omega^2 (R_S + R_b)^2 C_{js}^2} \\ \mathrm{Im}(Z_{ns}(\omega)) &\cong \frac{\omega L_S - \omega R_S^2 C_{js} - \omega^3 L_S^2 C_{js} + \omega^3 R_b^2 L_S C_{js}^2}{(1-\omega^2 L_S C_{js})^2 + \omega^2 (R_S + R_b)^2 C_{js}^2} \end{aligned} \quad (5.8)$$

The imaginary part approaches ωL_S. But the real part increases with frequency. So, the voltage at the Z_{ns} node increases with frequency when drain current flows through. We can observe in the figures that C_{gg} is almost constant at V_{ds}=0V, but drops very quickly at V_{ds}=1.2V with increasing frequency. However, C_{gd} has opposite trend to C_{gg}. Equations (5.4) and (5.8) can give us good explanation to this phenomena. Besides, larger finger number device has larger drain current and higher voltage at Z_{ns} node. This would lead more obvious frequency dependence with larger finger number.

5.3.4 Device geometry dependence

For given gate and drain voltages, we expect that the C_{gg} and C_{gd} capacitances are proportional to finger number (N_F). Take the extracted capacitances under V_{gs}=1.2V, V_{ds}=0 and 1.2V as an example shown in Fig. 5-23 and 5-24, C_{gg} and C_{gd} present good linear relation w.r.t. finger number (N_F). The linear regression lines didn't intersect exactly at the origin. We have explained it in 4.3.3 section.

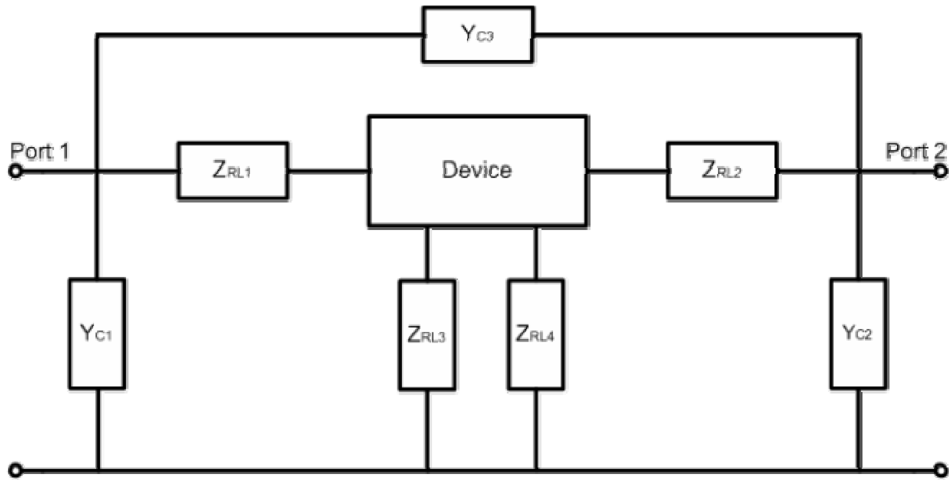


Fig. 5-1 The equivalent circuit of 4T device with pad

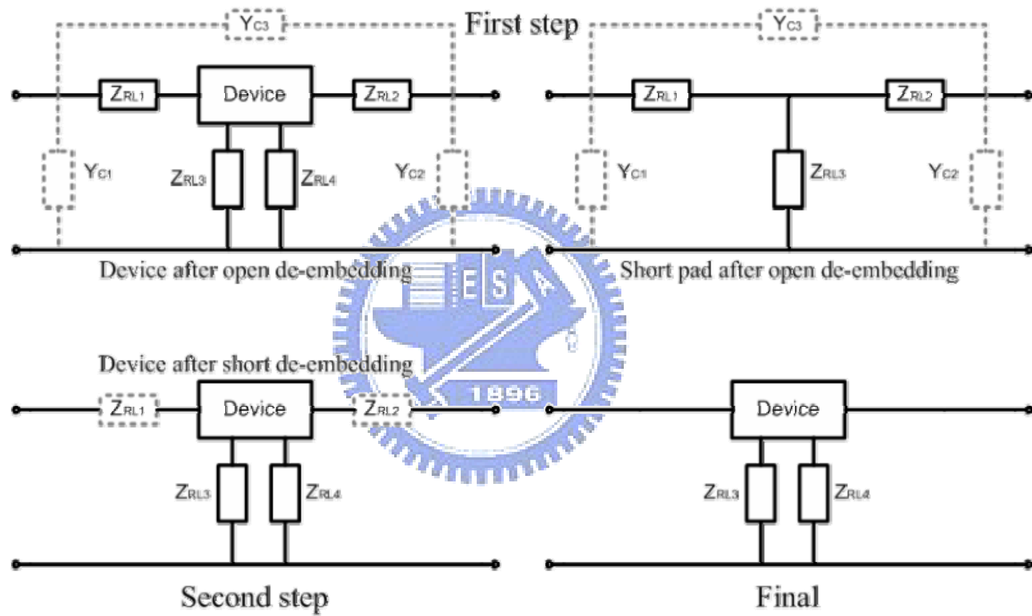


Fig. 5-2 The illustration of de-embedding procedure for 4T device

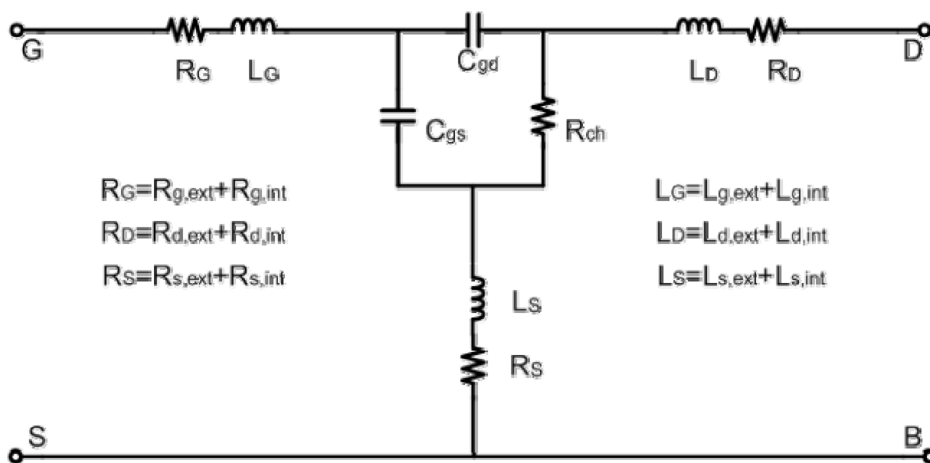


Fig. 5-3 The equivalent circuit of device at $V_{gs}>V_{th}$; $V_{ds}=0V$

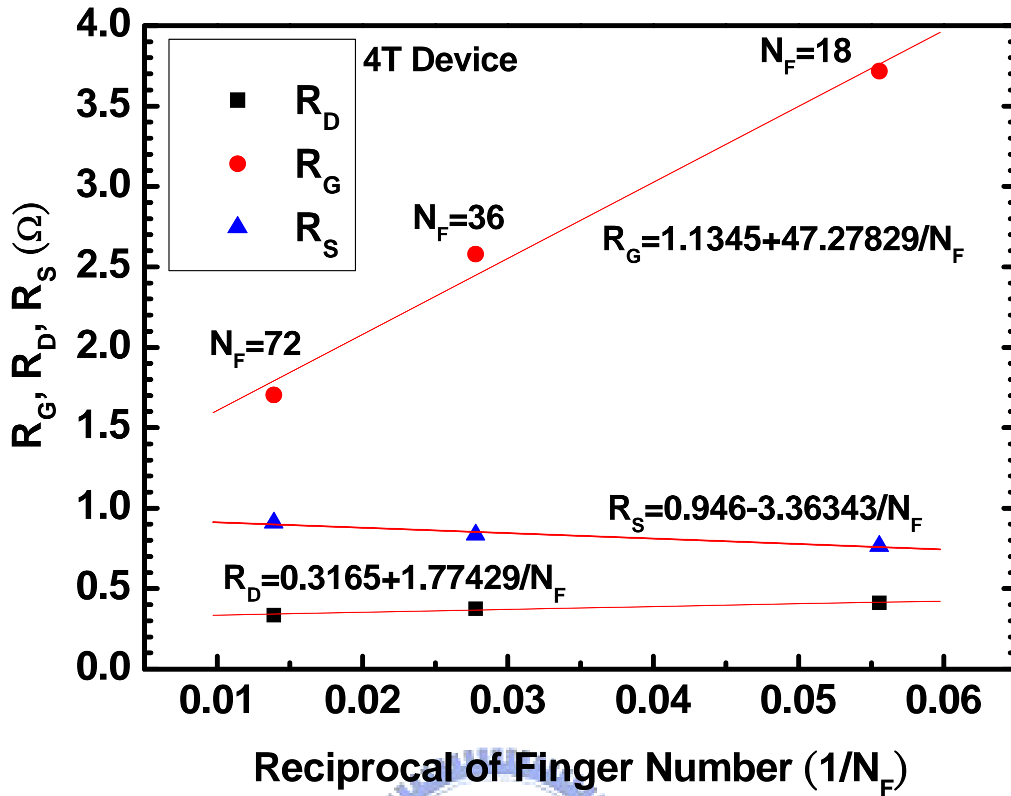


Fig. 5-4 The total parasitic resistance vs. reciprocal of finger number ($1/N_F$) for 4T

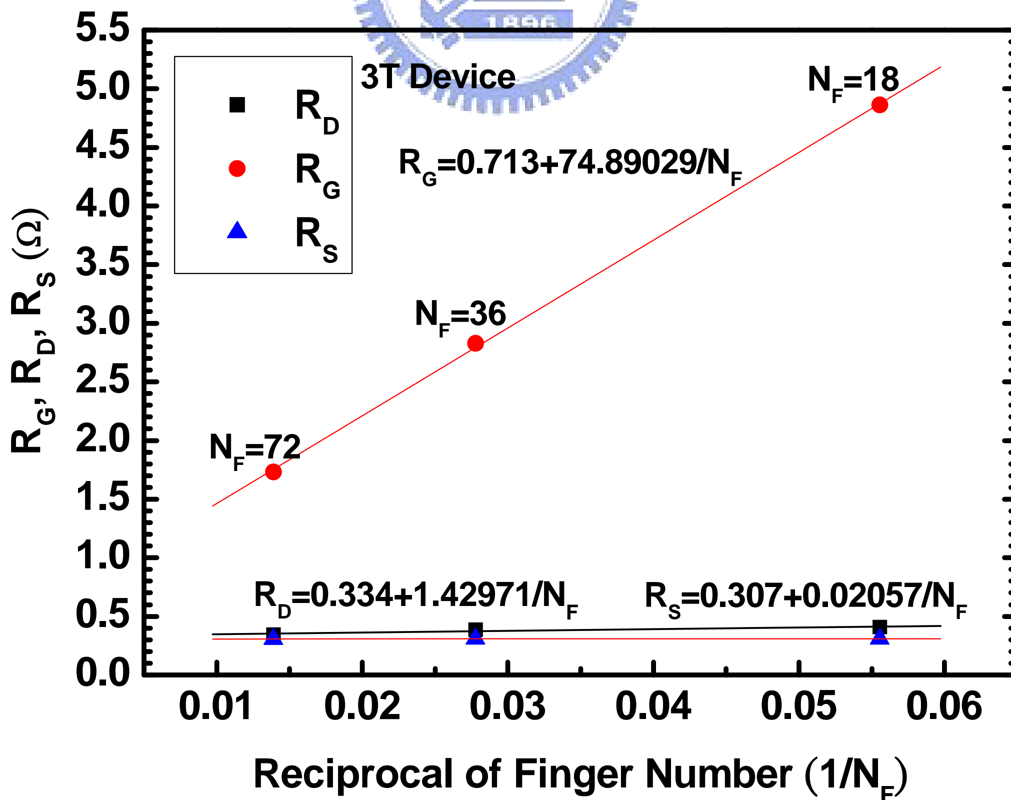


Fig. 5-5 The total parasitic resistance vs. reciprocal of finger number ($1/N_F$) for 3T

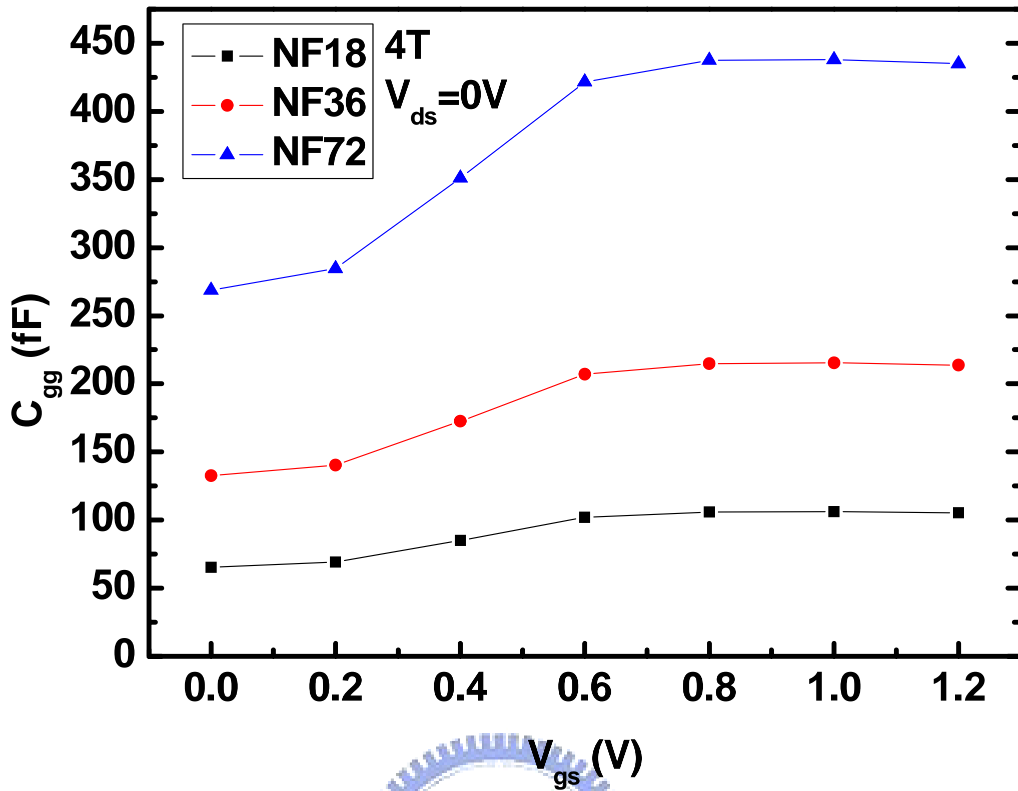


Fig. 5-6 4T MOSFET C_{gg} capacitance vs. gate voltage (V_{gs}) at V_{ds}=0V

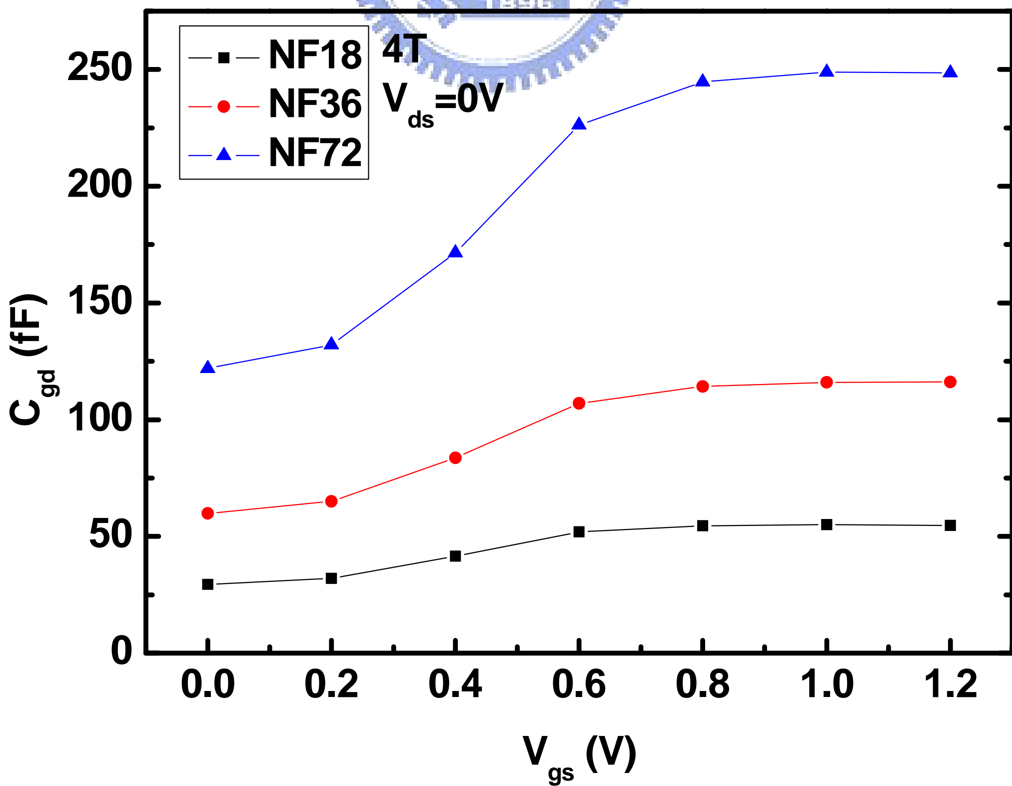


Fig. 5-7 4T MOSFET C_{gd} capacitance vs. gate voltage (V_{gs}) at V_{ds}=0V

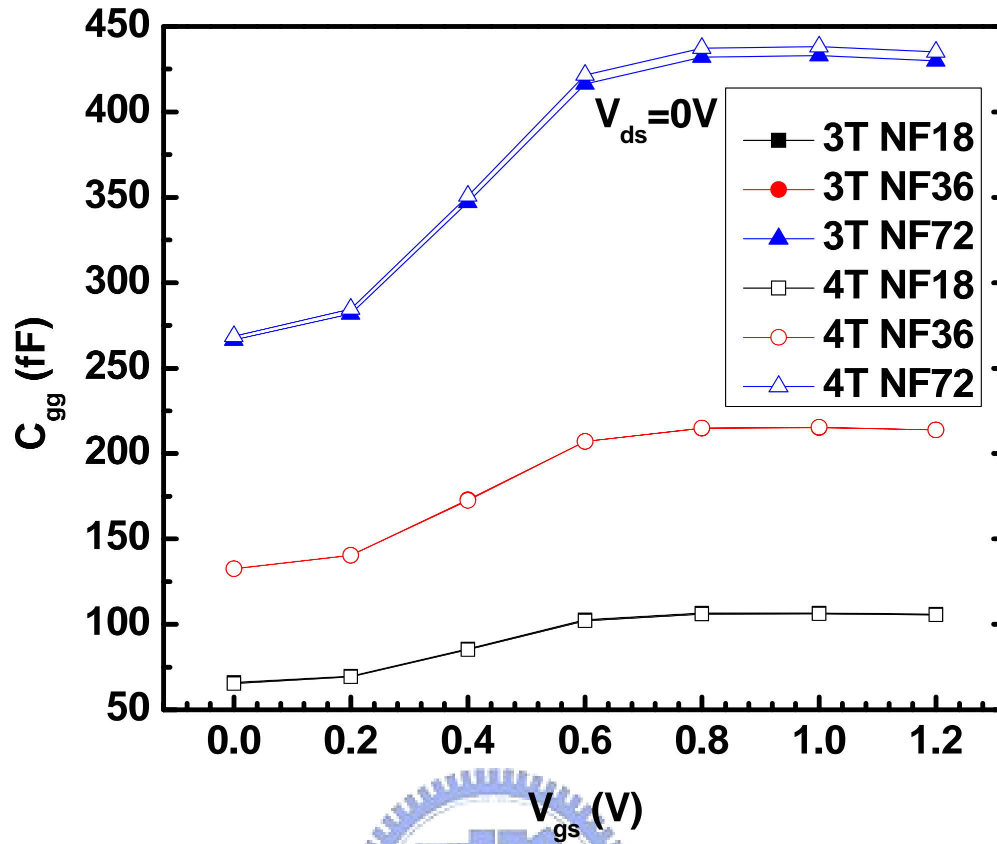


Fig. 5-8 The C_{gg} capacitances comparison of 3T and 4T devices at V_{ds}=0V

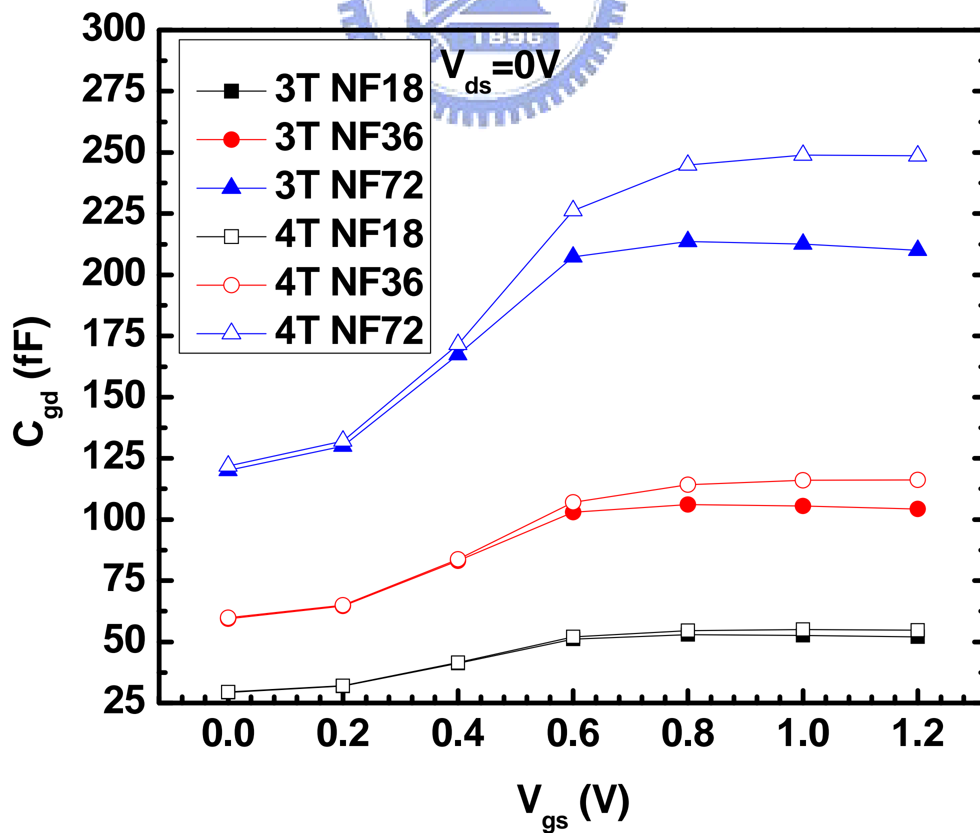


Fig. 5-9 The C_{gd} capacitances comparison of 3T and 4T devices at V_{ds}=0V

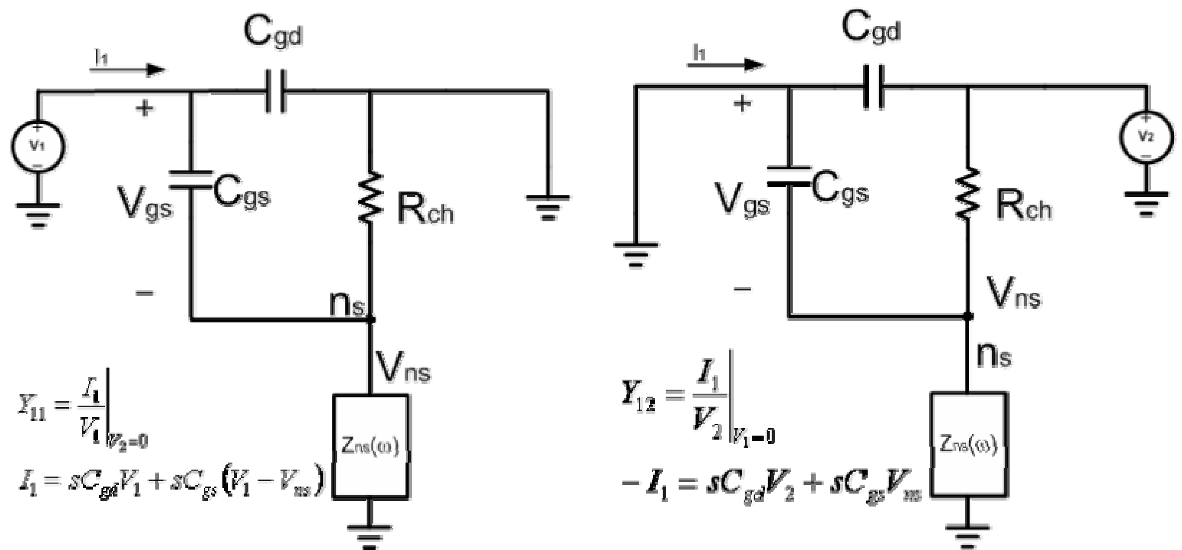


Fig. 5-10 The equivalent circuit schematics to illustrate internal source node voltage, V_{ns} effect on extraction of C_{gg} and C_{gd} under V_{ds}=0V

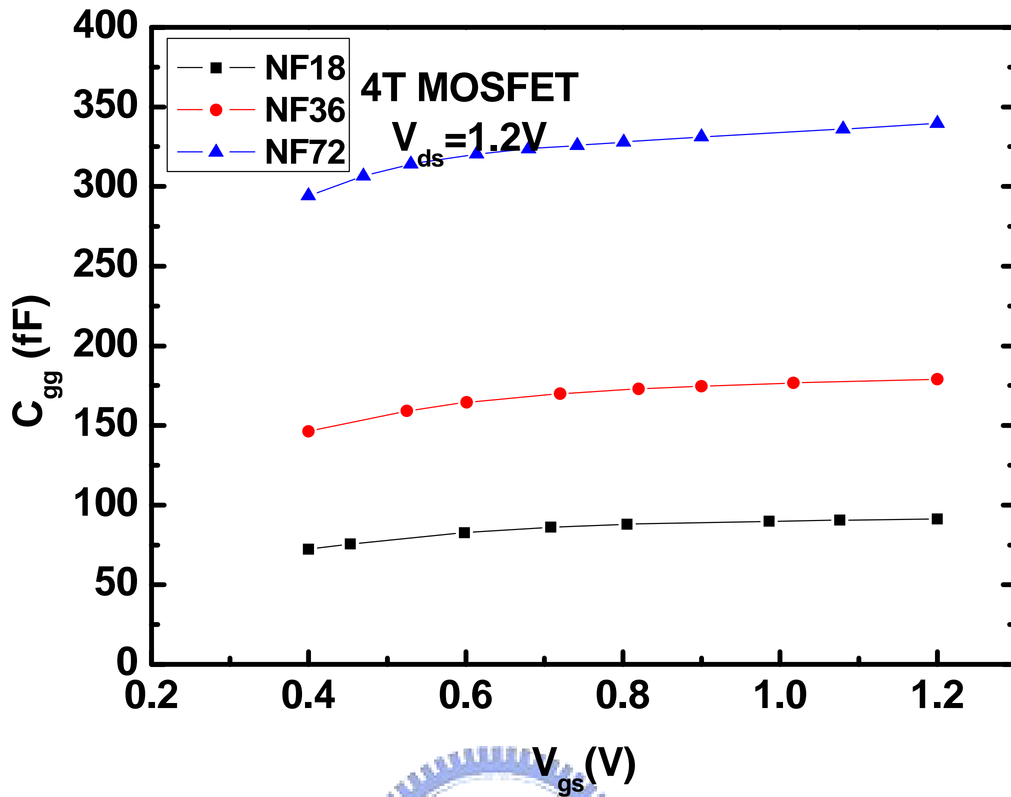


Fig. 5-11 4T MOSFET C_{gg} capacitance vs. gate voltage (V_{gs}) at V_{ds}=1.2V

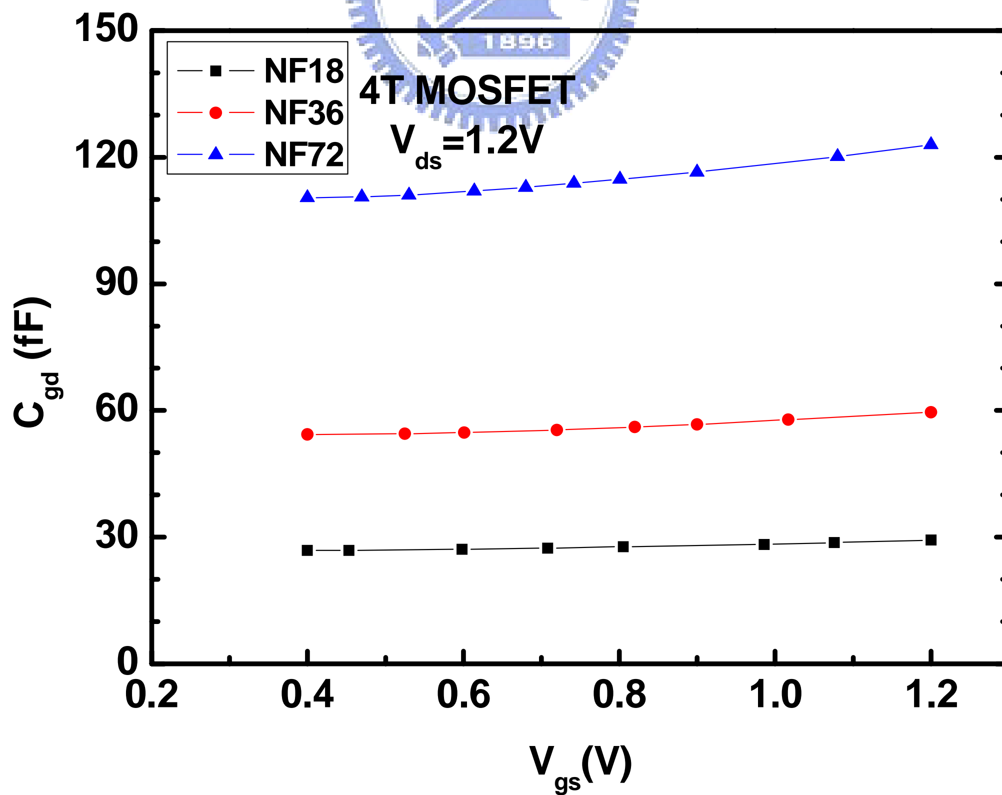


Fig. 5-12 4T MOSFET C_{gd} capacitance vs. gate voltage (V_{gs}) at V_{ds}=1.2V

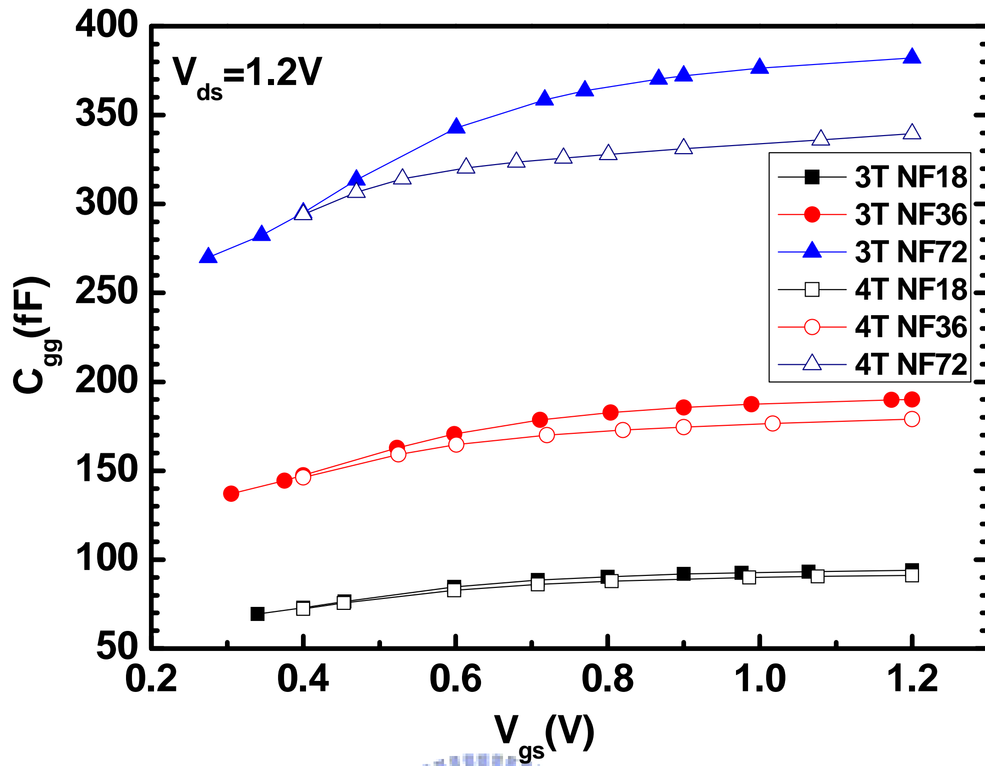


Fig. 5-13 The C_{gg} capacitances comparison of 3T and 4T devices at V_{ds}=1.2V

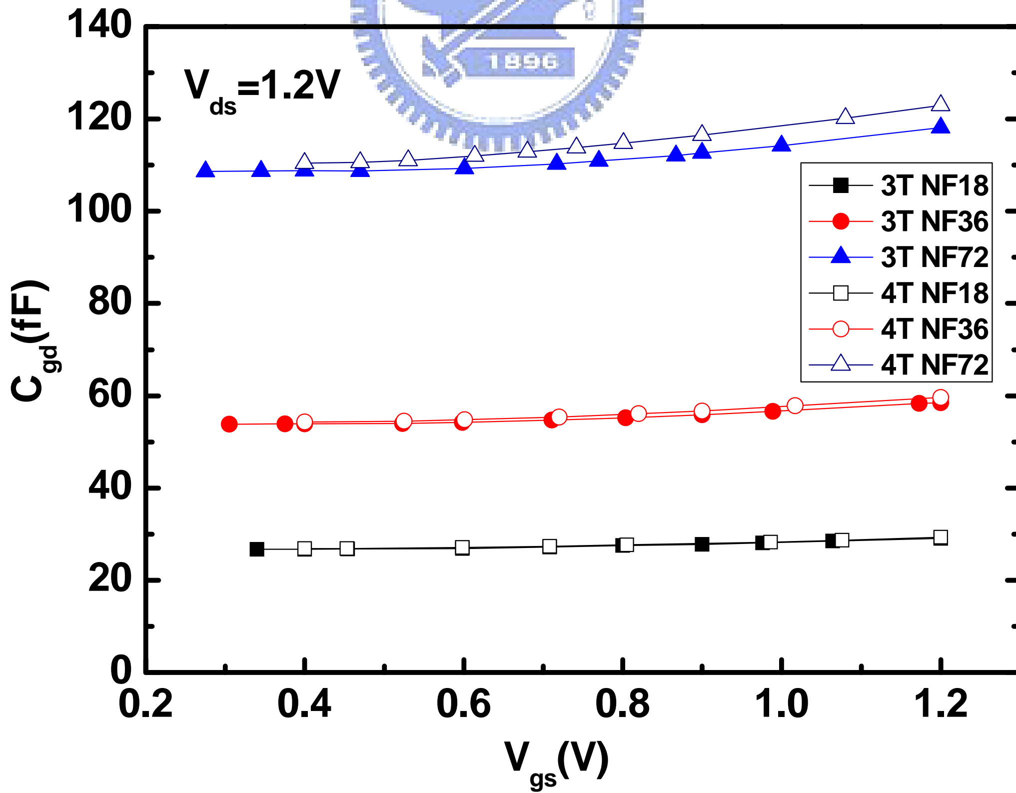


Fig. 5-14 The C_{gd} capacitances comparison of 3T and 4T devices at V_{ds}=1.2V

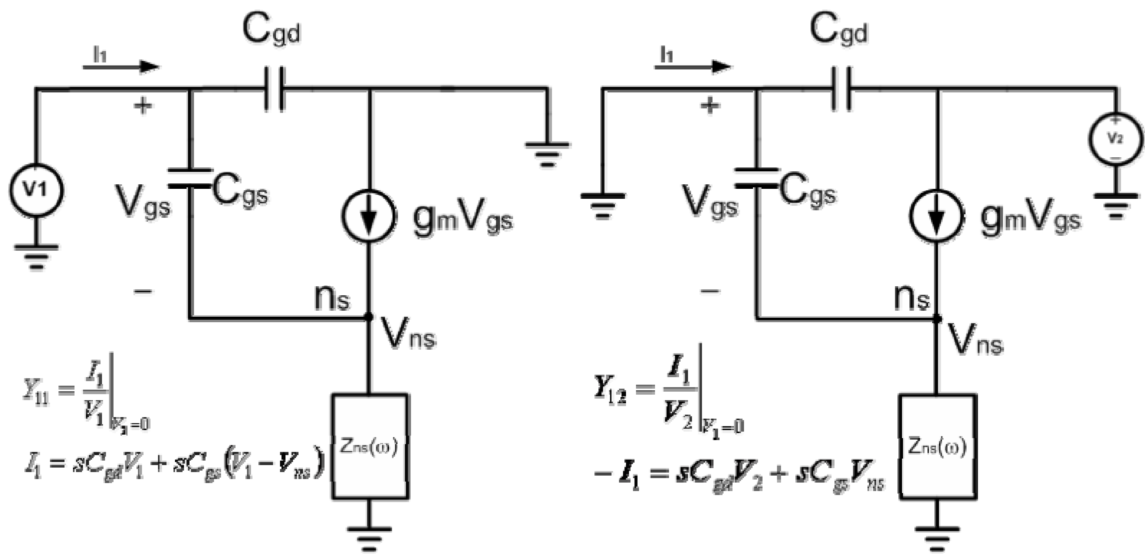


Fig. 5-15 The equivalent circuit schematics to illustrate internal source node voltage, V_{ns} effect on extraction of C_{gg} and C_{gd} under V_{ds}=1.2V

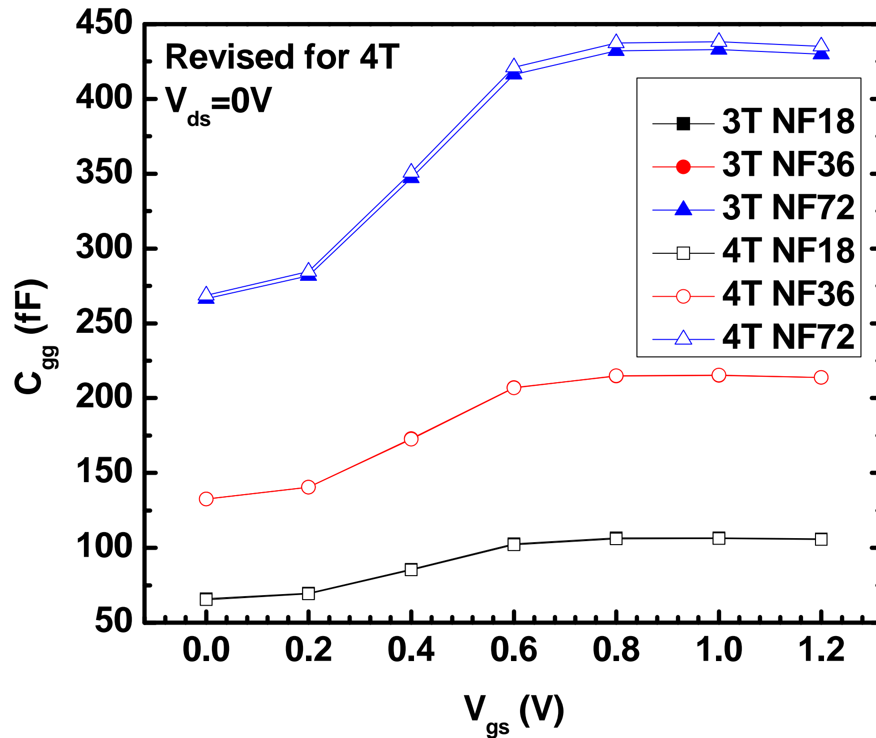


Fig. 5-16 The C_{gg} capacitances comparison of 3T and 4T devices at V_{ds}=0V (Source impedance de-embedding)

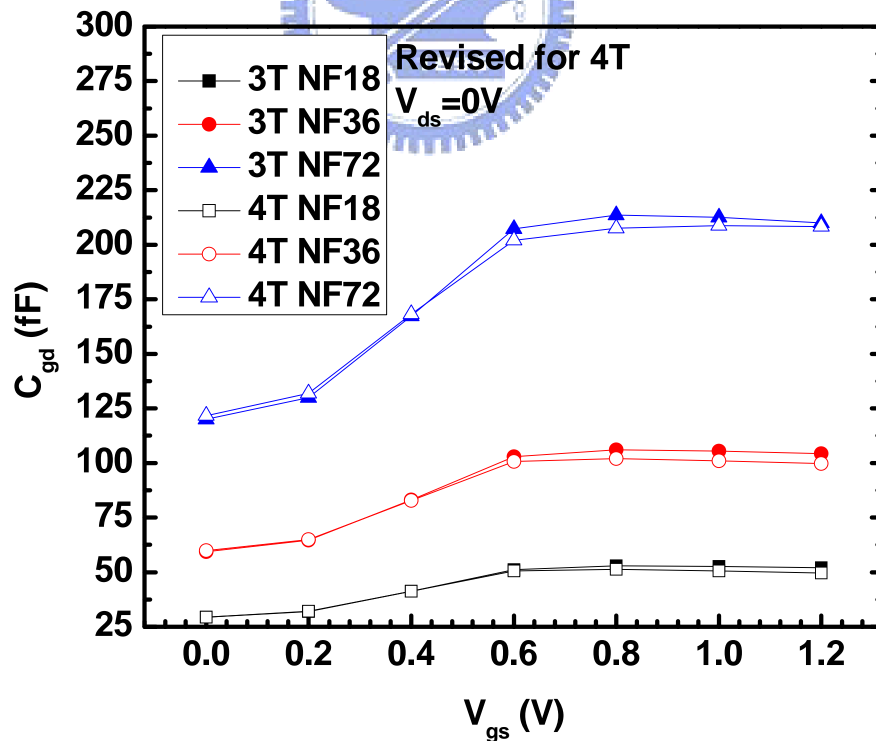


Fig. 5-17 The C_{gd} capacitances comparison of 3T and 4T devices at V_{ds}=0V (Source impedance de-embedding)

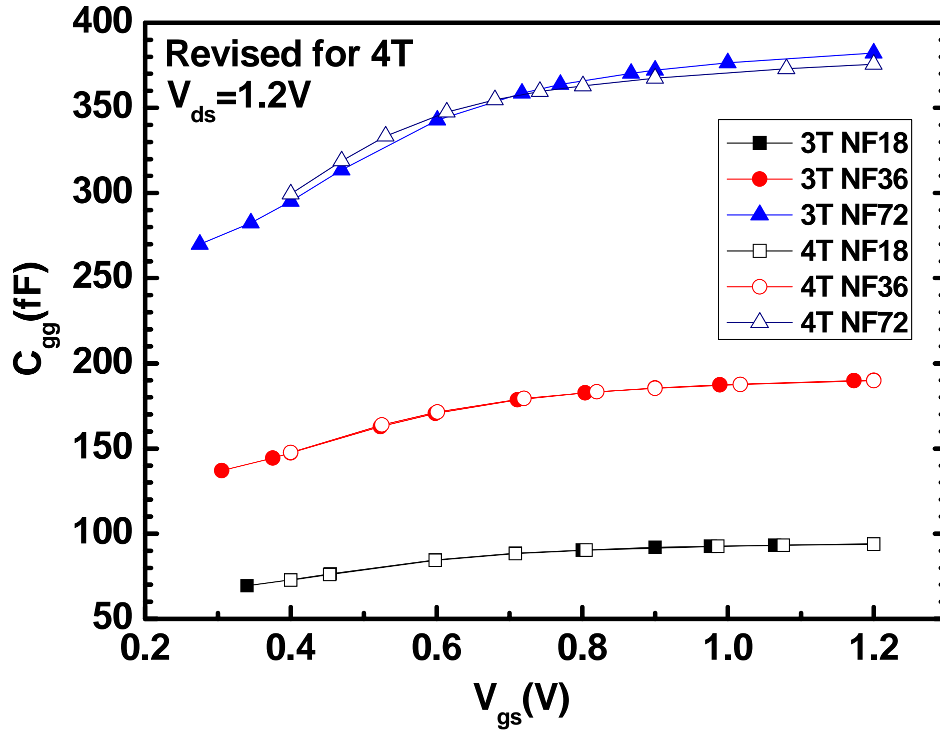


Fig. 5-18 The C_{gg} capacitances comparison of 3T and 4T devices at V_{ds}=1.2V (Source impedance de-embedding)

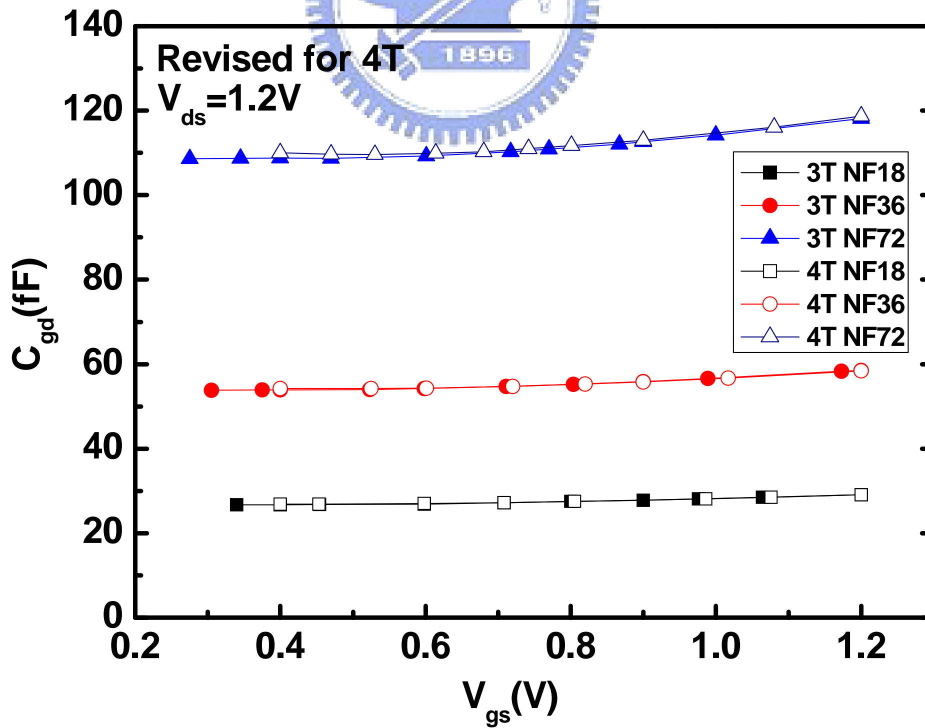


Fig. 5-19 The C_{gd} capacitances comparison of 3T and 4T devices at V_{ds}=1.2V (Source impedance de-embedding)

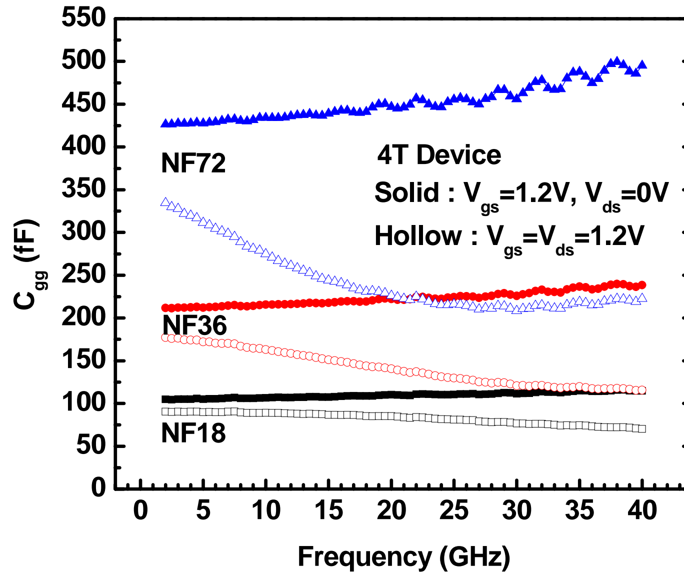


Fig. 5-20 The C_{gg} of 4T vs. frequency at V_{gs}=1.2V with varying V_{ds}

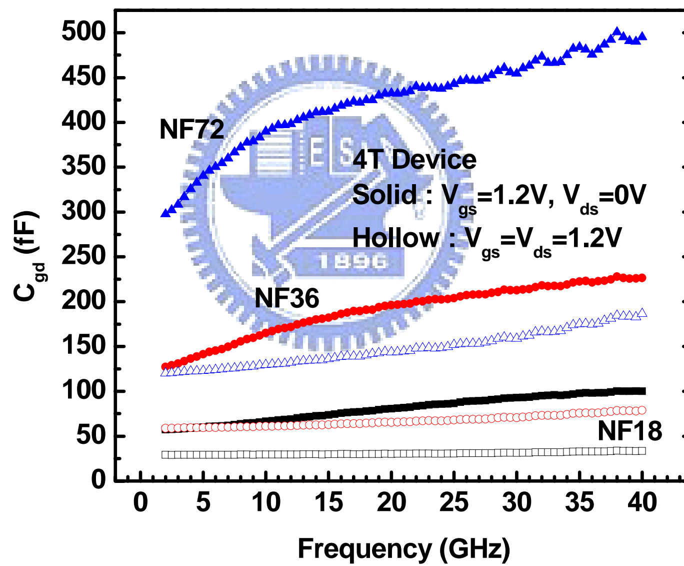
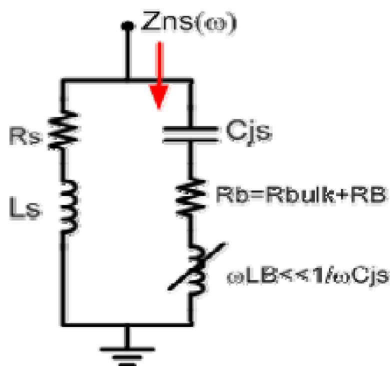


Fig. 5-21 The C_{gd} of 4T vs. frequency at V_{gs}=1.2V with varying V_{ds}



$$\mathrm{Re}(Z_{ns}(\omega)) \cong \frac{R_S + \omega^4 R_b L_S^2 C_{js}^2 + \omega^2 R_S R_b (R_S + R_b) C_{js}^2}{(1-\omega^2 L_S C_{js})^2 + \omega^2 (R_S + R_b)^2 C_{js}^2}$$

$$\mathrm{Im}(Z_{ns}(\omega)) \cong \frac{\omega L_S - \omega R_S^2 C_{js} - \omega^3 L_S^2 C_{js} + \omega^3 R_b^2 L_S C_{js}^2}{(1-\omega^2 L_S C_{js})^2 + \omega^2 (R_S + R_b)^2 C_{js}^2}$$

Fig. 5-22 $Z_{ns}(\omega)$ analysis

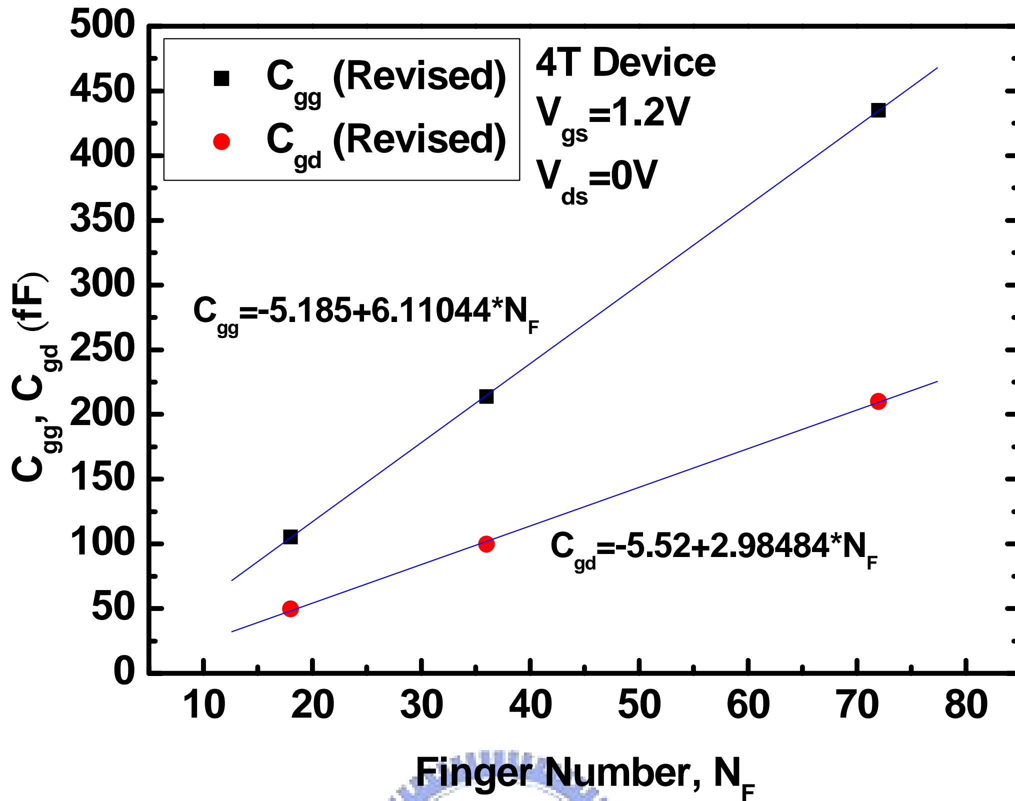


Fig. 5-23 The capacitances vs. finger number at V_{gs}=1.2V and V_{ds}=0V for 4T

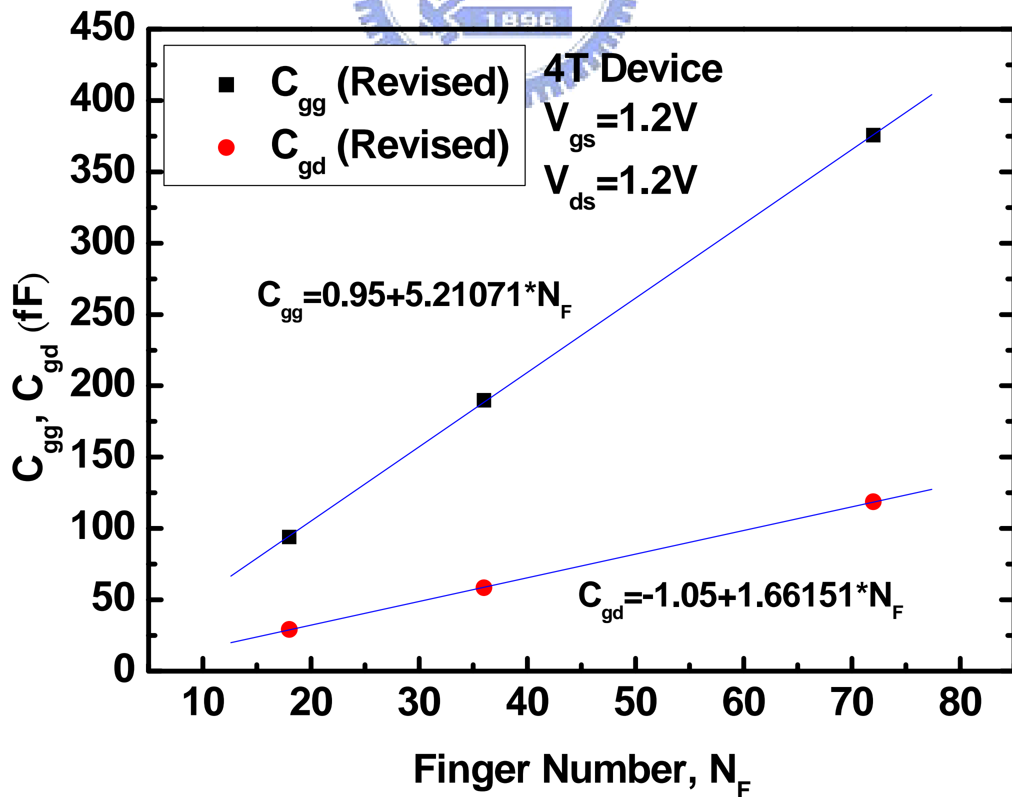


Fig. 5-24 The capacitances vs. finger number at V_{gs}=1.2V and V_{ds}=1.2V for 4T