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碩　士　論　文

增強靜電放電保護元件導通均勻度之設計

Design to Enhance Turn-on Uniformity of Multi-Finger ESD Protection Devices

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中華民國九十五年七月

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摘要

大尺寸 N 型金氧半電晶體(NMOS)應用於靜電放電防護電路時，通常會以多指狀結構(multi-finger)來佈局，以降低元件所佔佈局面積。然而由於 N 型金氧半電晶體具有明顯的驟回崩潰特性，以及佈局上每根指狀 N 型寄生橫向雙載子電晶體之等效基極電阻之不同，造成多指狀結構 N 型金氧半電晶體在靜電放電轟擊下，並不會均勻的導通來排放靜電放電電流，而是集中於某些指狀 N 型金氧半電晶體。此不均勻導通的現象使得 N 型金氧半電晶體之靜電放電耐受度無法隨著元件尺寸增加而線性增加，造成靜電放電防護電路設計上的困難。

此篇論文主旨在改善多指狀結構 N 型金氧半電晶體之不均勻導通現象，並增強其靜電放電耐受度。設計宗旨為不需額外的觸發電路以及佈局面積，僅利用改變多指狀 N 型金氧半電晶體元件本身之電路接線，來改善不均勻導通之現象。第一個設計為自我基體觸發技術(self-substrate-triggered technique)，應用於閘極接地之 N 型金氧半電晶體。其原理為利用多指狀 N 型金氧半電晶體中，在靜電放電下最易先導通的中間之指狀 N 型金氧半電晶體元件來對所有指狀元件作基體觸發，以促進多指狀 N 型金氧半電晶體均勻導通。此設計已成功驗證於 0.13 微米互補式金氧半導體製程中，其靜電放電耐受度在相同元件尺寸下，比傳統的閘極接地 N 型金氧半電晶體提升了兩倍。第二個設計為等基體電位技術(equal-substrate-potential technique)，應用於串疊 N 型金氧半電晶體(stacked-NMOS)。其原理為利用佈局技巧，使每個指狀串疊 N 型金氧半電晶體

寄生之橫向雙載子電晶體具有相同的基極電位，以促進元件導通均勻度。此設計驗證於 0.18 微米互補式金氧半導體製程，實驗結果顯示其導通電阻較傳統結構小，人體放電模式(Human-Body-Model, HBM)靜電放電耐受度較傳統串疊 N 型金氧半電晶體高，而機械放電模式(Machine-Model, MM)之靜電放電耐受度則沒有差別。

本論文之研究成果已發表於國際研討會論文，並投稿至國際期刊，已被接受。

Design to Enhance Turn-on Uniformity of Multi-Finger ESD Protection Devices

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ABSTRACT

To sustain the required ESD levels, the device size of NMOS used in ESD protection circuit is often designed with large device dimensions, which are often drawn with the multi-finger layout style to reduce the total occupied silicon area. However, because of the obvious snapback breakdown characteristic of NMOS transistor and the layout geometry effect on the distributed base resistance of each parasitic lateral bipolar transistor, multi-finger NMOS cannot be triggered on uniformly under ESD stress. The ESD current is only concentrated on some fingers. Therefore, the ESD robustness of multi-finger NMOS cannot be increased linearly with the increase of device size.

The aim of this thesis is to improve the turn-on uniformity of multi-finger NMOS. Objective of the proposed designs are to solve the non-uniform turn-on issue through simple circuit wiring of the multi-finger NMOS itself, and without external triggering circuit and increase of layout area. The first proposal is self-substrate-triggered technique applied to gate-grounded NMOS (GGNMOS). The design concept is to utilize the current of the most easily turned-on center fingers to trigger the substrate of all the other fingers. This design has

been successfully verified in a 0.13-μm CMOS process, and the ESD robustness of self-substrate-triggered GGNMOS could be improve twice larger than that of traditional GGNMOS. The second proposal is equal-substrate-potential technique applied to stacked-NMOS devices, and the design is verified in a 0.18-μm CMOS process. The design concept is to equalize the substrate-potential of each parasitic lateral BJT inherent in stacked-NMOS and thus improve the turn-on uniformity. The experimental results show that equal-substrate-potential stacked-NMOS has smaller turn-on resistance than traditional stacked NMOS. The HBM ESD level could be improved through this design, but the MM ESD level is the same as traditional stacked-NMOS.

Contents of this thesis have already been published on an international conference, a local conference, and accepted by an international journal.

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首先要感謝我的指導教授 柯明道博士兩年來的耐心指導與鼓勵，使我能夠順利完成碩士學位。專業上，在老師循序漸進的指導下，讓我在靜電放電防護電路領域，能從入門開始，累積知識概念，達到能夠獨立研究相關設計的能力；在人格上，從老師認真的研究態度，以及講求效率及水準的做事方法，無形中帶給我許多做人處事該有的智慧。畢業後無論從事任何研究，我都會謹記老師的至理名言：smart 等於做事有效率，成果有水準。

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陳　佳　惠

僅誌於竹塹交大

九十五年　七月

CONTENTS

FIGURE CAPTIONS

Chapter 1
Introduction

1.1 MOTIVATION

With the process evolution, the device size is continually scaled down and the salicided process used to improve the operating speed of CMOS ICs. However, the electrostatic discharge (ESD) robustness of devices in the advanced CMOS technology becomes inferior. To sustain a reasonable ESD robustness in nano-scale CMOS ICs, on-chip ESD protection circuits must be added into the chips [1]. The typical ESD levels of general commercial IC products are 2kV in human-body-model (HBM) ESD test and 200V in machine-model (MM) ESD test [2]. To sustain the required ESD levels, ESD protection devices are often designed with large device dimensions, which are often drawn with the multi-finger layout style to reduce the total occupied silicon area [3]. Typically, multi-finger NMOS devices are widely used as ESD protection structures owing to the effectiveness of parasitic lateral n-p-n BJT in handling high ESD current. However, it has been reported that multi-finger NMOS can not be uniformly turned on under ESD stress [4]-[7]. That is, even if a larger multi-finger NMOS is used as the ESD protection device, uniform conduction of all fingers is hard to achieve, and hence the expected ESD level can not be realized [7]. A novel self-substrate-triggered technique to solve the non-uniform turn-on issue of multi-finger gate-grounded NMOS (GGNMOS) is proposed in this thesis, and the design has been successfully verified in a 0.13-μm CMOS process [8].

In modern IC chips, though the power supply voltage of internal circuits keeps lowering to reduce the power consumption and the heat dissipation, their input/output (I/O) interfaces are still operated at higher voltage levels to cooperate with the peripheral components. For such mixed-voltage applications, special design through circuit structure or process

modification is needed to avoid the gate-oxide reliability issue. A better solution to both overall system performance and cost is to propose a high-voltage tolerant (HVT) circuit that can be operated under high power-supply voltage using only low-voltage devices. In this case, stacked-NMOS is widely used. However, because the stacked-NMOS has higher trigger voltage, higher snapback holding voltage, and lower It2 level, the stacked-NMOS usually has worse ESD robustness than single NMOS structure. In this thesis, an equal-substrate-potential technique is proposed to enhance the ESD robustness of stacked NMOS, and the design has been fabricated and verified in a 0.18-μm CMOS process.

1.2 THESIS ORGANIZATION

To improve the turn-on uniformity of multi-finger ESD protection devices, two designs applied to multi-finger GGNMOS and multi-finger stacked NMOS are proposed and discussed in this thesis. This thesis contains five chapters. Chapter 2 introduces the background of ESD event and the turn-on mechanism of NMOS transistors under ESD condition. Then, the mechanism that results in non-uniform turn-on phenomenon of multi-finger NMOS transistors is illustrated. In chapter 3, a gate-grounded NMOS (GGNMOS) with self-substrate-triggered technique is first proposed for effective on-chip ESD protection. The self-substrate-triggered GGNMOS is fabricated and verified in a 0.13-μm CMOS process. The prior designs to overcome the non-uniform turn-on issue of GGNMOS are reviewed in chapter 3, and the design concept of self-substrate-triggered technique is then proposed. The measurement setup and experimental results including the dc characteristics, TLP-*IV* curves, ESD robustness, and turn-on analysis by emission microscope (EMMI) are stated in detail in chapter 3. In chapter 4, the equal-substrate-potential technique, a method to improve the turn-on uniformity of stacked NMOS is proposed and verified in a 0.18-μm CMOS process. There is a brief introduction to the high-voltage-tolerant (HVT) I/O circuit and the application of stacked NMOS in HVT circuits. The design concept of

equal-substrate-potential is illustrated and then the measurement results including dc characteristics, TLP-*IV* curves, and ESD robustness are stated in detail. In the end of this thesis, a short conclusion and future work are given in the chapter 5.

Chapter 2

Non-Uniform Turn-on Phenomenon in Multi-Finger ESD Protection NMOS

2.1 General Introduction to ESD

The phenomenon of electrostatic discharge (ESD) occurs when an electrostatic voltage slowly develops between an object and its surrounding environment, commonly referred to as earth or ground, then spontaneously discharges as an electrical current impulse [9]. ESD can be brought about by different origins, it can be classified to human-body model (HBM), machine-model (MM), and charged-device model (CDM) according to different discharging methods and sources of electrostatic charges.

2.2 ESD Protection Circuit with MOS Transistors

MOS transistors are the most common ESD protection devices in CMOS ICs. Fig. 2.1 shows the typical design of efficient ESD protection circuits in a CMOS IC to protect the internal circuits against ESD damage [10]. For the input ESD protection circuit, the gates of Mp1/Mn1 are connected to VDD/VSS to avoid interference with the normal circuit operation. While for output ESD protection, because the device size of the output buffer is usually very large, the output PMOS/NMOS (Mp2/Mn2) could be used as self-protection device. To achieve better ESD robustness, VDD-to-VSS power clamped circuit is added between power lines. And the power clamped circuit are realized by an ESD detection circuit and the main ESD protection device (a large size NMOS, Mn3, in this case). The ESD detection circuit can provide a voltage at the gate of Mn3 to help Mn3 turn on more quickly under ESD stress condition, and bias the gate of Mn3 to ground to keep the Mn3 off under normal circuit operation condition.

2.3 TURN-ON MECHANISM OF MOS TRANSISTOR UNDER ESD CONDITION

Under ESD stress conditions the MOS transistor in the ESD path is required to carry amperes of current. The inherent lateral bipolar transistor (BJT) presents in both NMOS and PMOS transistors is triggered on to snapback region to carry such high ESD current, and the mechanisms involve both avalanche breakdown and turn-on of the parasitic lateral BJT. For better comprehension, the following statements concentrate on NMOS transistor. Fig. 2.2(a) depicts the cross section of a NMOS transistor including the parasitic lateral n-p-n BJT and associated currents [9]. The N+ drain junction, P-substrate and the N+ source junction of a NMOS device construct a parasitic lateral n-p-n bipolar transistor. When the high ESD stress voltage occurs, the parasitic n–p-n bipolar junction transistor inherent in NMOS device structure can be turned on to carry the huge ESD current and to clamp down the ESD voltage to protect gate oxide of internal circuits.

To illustrate the turn-on mechanism of MOS transistor under ESD condition, a NMOS with gate, source, and substrate at zero potential is considered. The corresponding high current *I-V* curve is shown in Fig. 2.2(b). As the drain current is increased, the reverse-biased drain-substrate junction is initially in high impedance. The only current is the reverse current at the drain-substrate junction. Eventually the drain-substrate junction begins to avalanche due to the high voltage across it, and electron-hole pairs are generated. The electrons are swept across the drain junction towards the drain contact, adding to the drain current, while the holes drifts towards the substrate contact giving rise to a substrate current, Isub. As Isub increases, the potential at the source-substrate junction increases and forward biases this junction. Then the parasitic LBJT can be considered to be turned on. In Fig. 2.2(b), Vt1 is the trigger voltage of the parasitic BJT and the trigger current is It1. The above-mentioned is effectively self-biased bipolar operation, since the bias current is generated by the intrinsic avalanching at the drain-substrate junction. Once the parasitic lateral BJT turns on, the drain voltage

decreases and a negative resistance is observed due to the availability of more carriers for multiplication until a minimum voltage, called snapback holding voltage (Vhold), is reached. The *I-V* curve now show a positive resistance as further increase in the injected current results in conductivity modulation of the substrate region that reduces the intrinsic substrate resistance. A higher Isub is required to maintain the transistor in the on-state [9]. Finally, the parasitic BJT will be permanent damaged due to thermal failure, and the failure current/voltage level is called second breakdown current (It2)/voltage (Vt2).

2.4 SNAPBACK CHARACTERISTICS OF NMOS AND PMOS TRANSISTORS

Fig. 2.3 shows the measured snapback *I-V* curves of NMOS and PMOS with a channel width of 360μm and channel length of 0.25μm in a 0.18-μm CMOS process, and the inset shows the measurement setup. The experimental results show that NMOS transistor have obvious snapback characteristic, while the snapback of PMOS transistor is unobvious. Besides, the trigger current of PMOS (~18mA) is much larger than that of NMOS (~4mA). It is because that the current gain of p-n-p bipolar junction transistor in CMOS process is much smaller than that of n-p-n bipolar junction transistor; thus the *I-V* curve of PMOS under ESD stresses usually have no, or weak, snapback phenomenon. Because the snapback holding voltage and trigger voltage of PMOS is nearly the same, any finger breakdown would not clamp the pad to a low voltage, thus multi-finger PMOS can be turned on uniformly under ESD condition. On the other hand, if any finger is turned on first in multi-finger NMOS, the pad would be clamped to the low snapback holding voltage and prevent other fingers from being turned on, and results in non-uniform turn-on issue of multi-finger NMOS. Therefore, in this thesis, the work is concentrated on improving the turn-on uniformity of multi-finger NMOS transistors.

2.5 MECHANISM OF NON-UNIFORM TURN-ON PHENOMENON IN NMOS

There are two main causes of non-uniform turn-on issue in multi-finger NMOS transistor. One is the obvious snapback characteristic of NMOS device, the other is the layout geometry effect on the distributed substrate resistance of the n-p-n bipolar transistor. Fig. 2.4 shows the layout and cross-sectional view of traditional multi-finger NMOS. In the multi-finger NMOS structure with P+ guard ring surrounding it, due to the different distances from the base regions of each parasitic lateral n-p-n BJT to the substrate guard ring, the base resistance of parasitic lateral n-p-n BJT in the central region of the multi-finger NMOS is higher than those in the side regions. Therefore, in the multi-finger NMOS structure, the center NMOS fingers are always triggered on faster than the others under ESD stress. As long as the center NMOS fingers are triggered on, the ESD overstress voltage is clamped to the snapback holding voltage of NMOS. Moreover, if the secondary breakdown voltage (Vt2) of NMOS is smaller than its trigger voltage (Vt1), the other non-turned-on NMOS fingers in the side region cannot be triggered on before the first turned-on NMOS fingers are burned out [5]. Therefore, the ESD current will be only discharged through some local regions. Fig. 2.5 shows the observed non-uniform turn-on phenomenon of a gate-grounded NMOS in Ref. [5]. The current are concentrated on the central regions of multi-finger gate-grounded NMOS, indicating the occurrence of non-uniform turn-on phenomenon.

Therefore, ESD robustness of multi-finger NMOS cannot be efficiently increased by increasing the device dimension due to non-uniform turn-on issue. To solve this problem, some circuit designs such as gate-coupled [11]-[15] or substrate-triggered [16]-[19] techniques have been proposed to reduce the trigger voltage (Vt1) of NMOS for improving the turn-on uniformity of multi-finger NMOS. In this thesis, two designs of self-substrate-triggered and equal-substrate-potential are proposed to enhance turn-on uniformity of large-size NMOS devices.

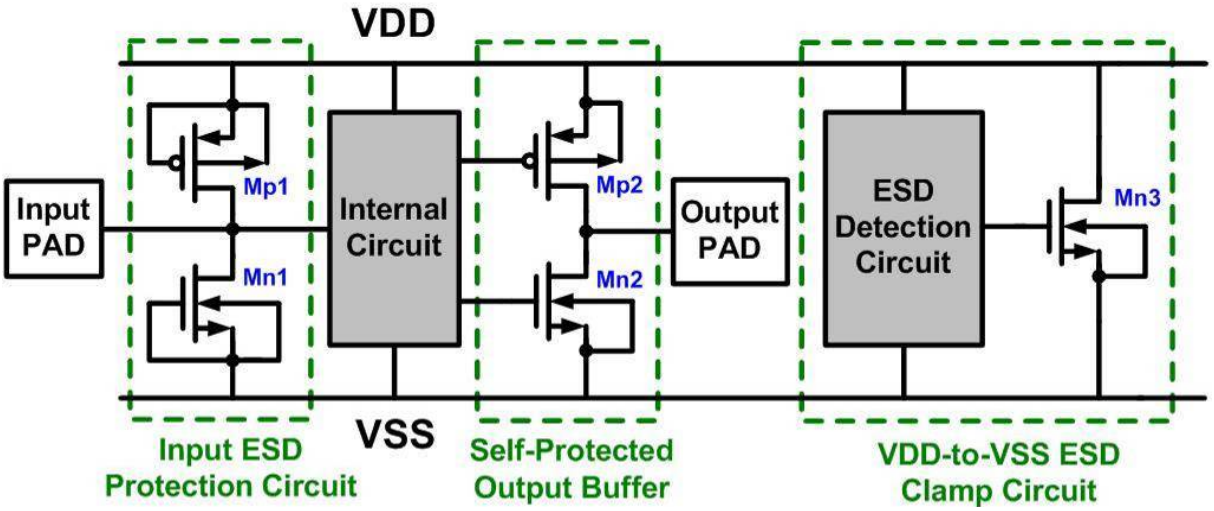
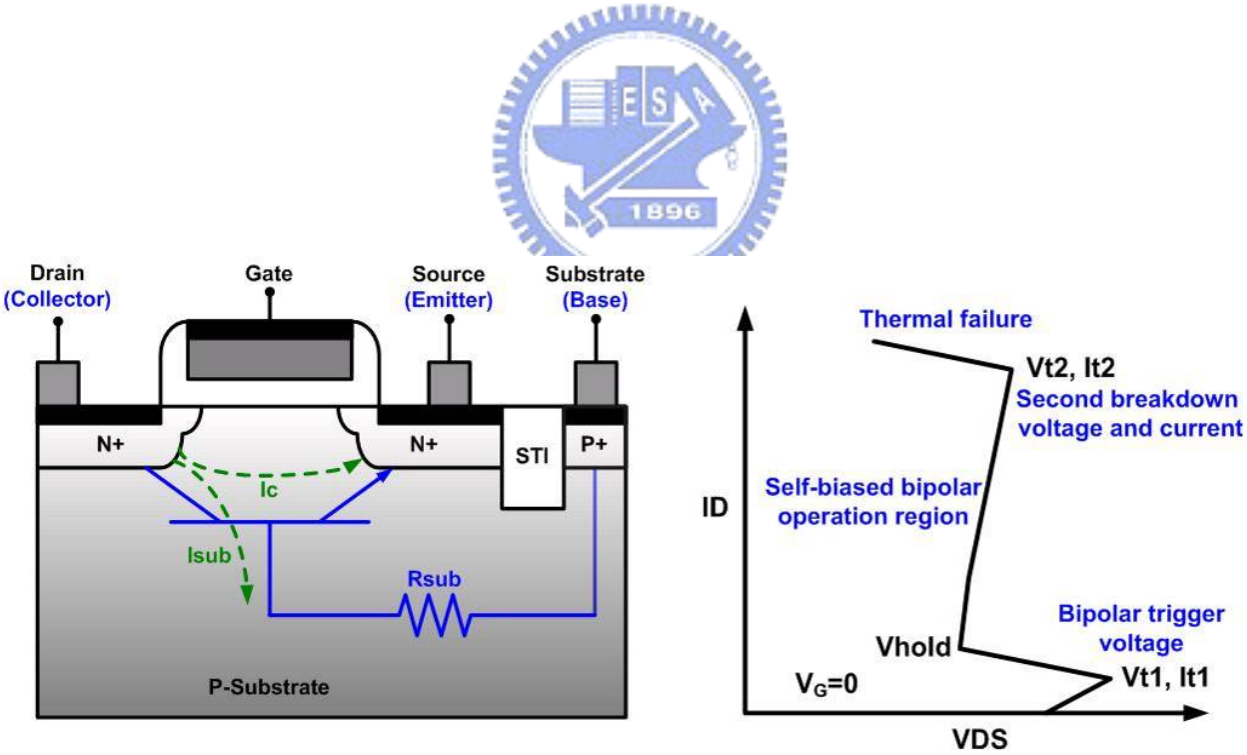
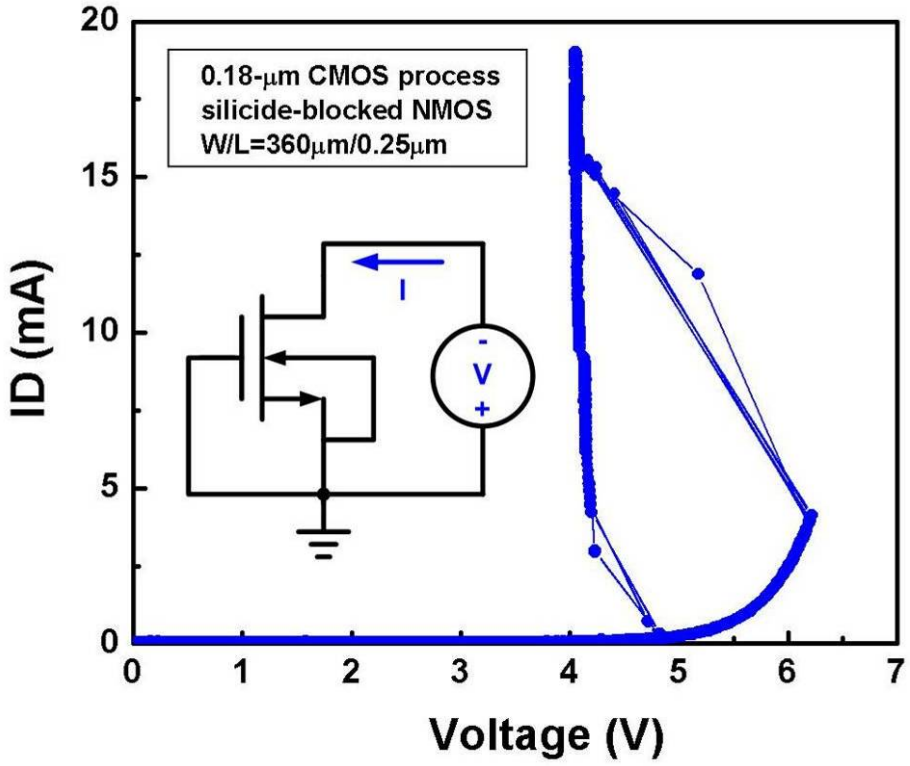


Fig. 2.1 Typical on-chip ESD protection circuit in CMOS ICs.

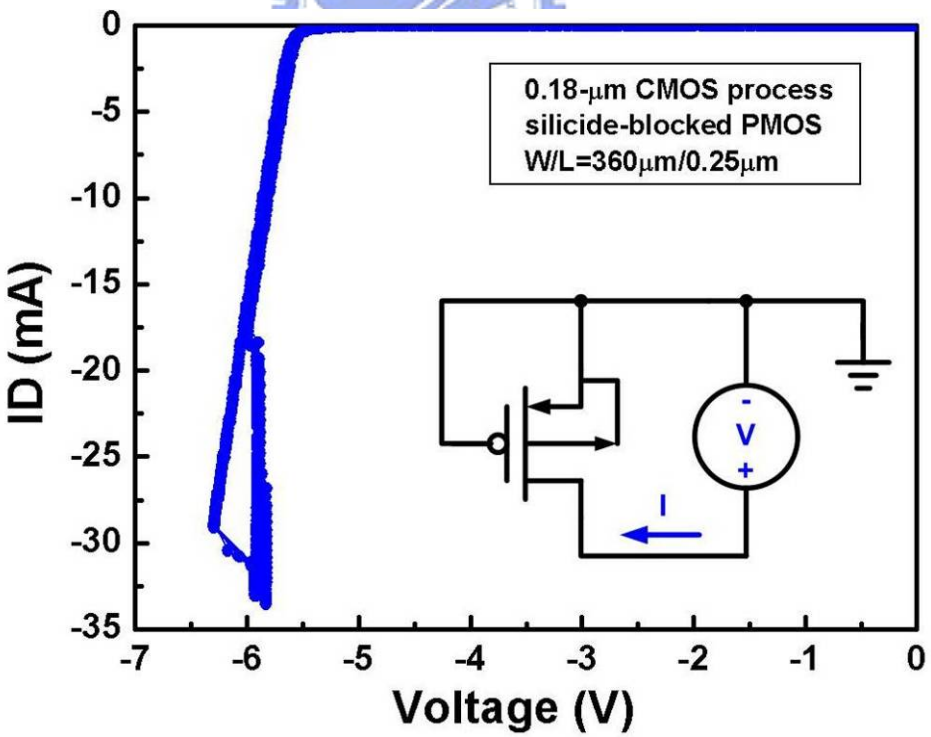


(a) (b)

Fig. 2.2 (a) Cross section of an NMOS transistor showing the parasitic lateral n-p-n bipolar transistor and associated currents. (b) High current *I-V* curve of an NMOS transistor with gate, source, and substrate at zero volts [9].

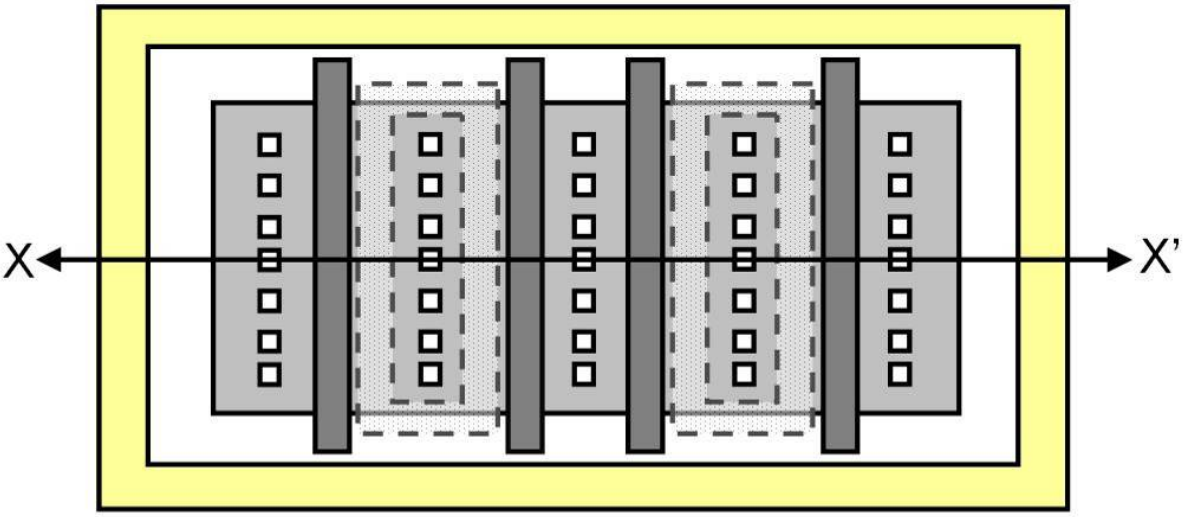


(a)

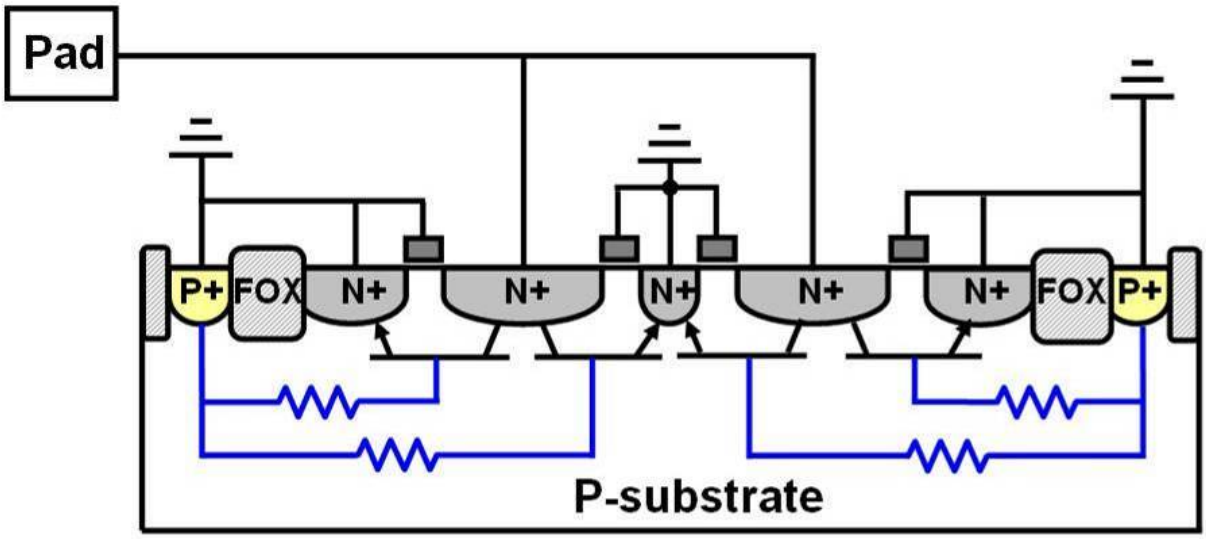


(b)

Fig. 2.3 Measured snapback *I-V* curves of (a) NMOS and (b) PMOS, with a channel width of 360μm and channel length of 0.25μm in a 0.18-μm CMOS process.



(a)



(b)

Fig. 2.4 (a) The layout top-view and (b) the X-X' cross-sectional view of traditional multi-finger gate-grounded NMOS, indicating that the central parasitic lateral BJTs have larger substrate resistance due to layout geometry.

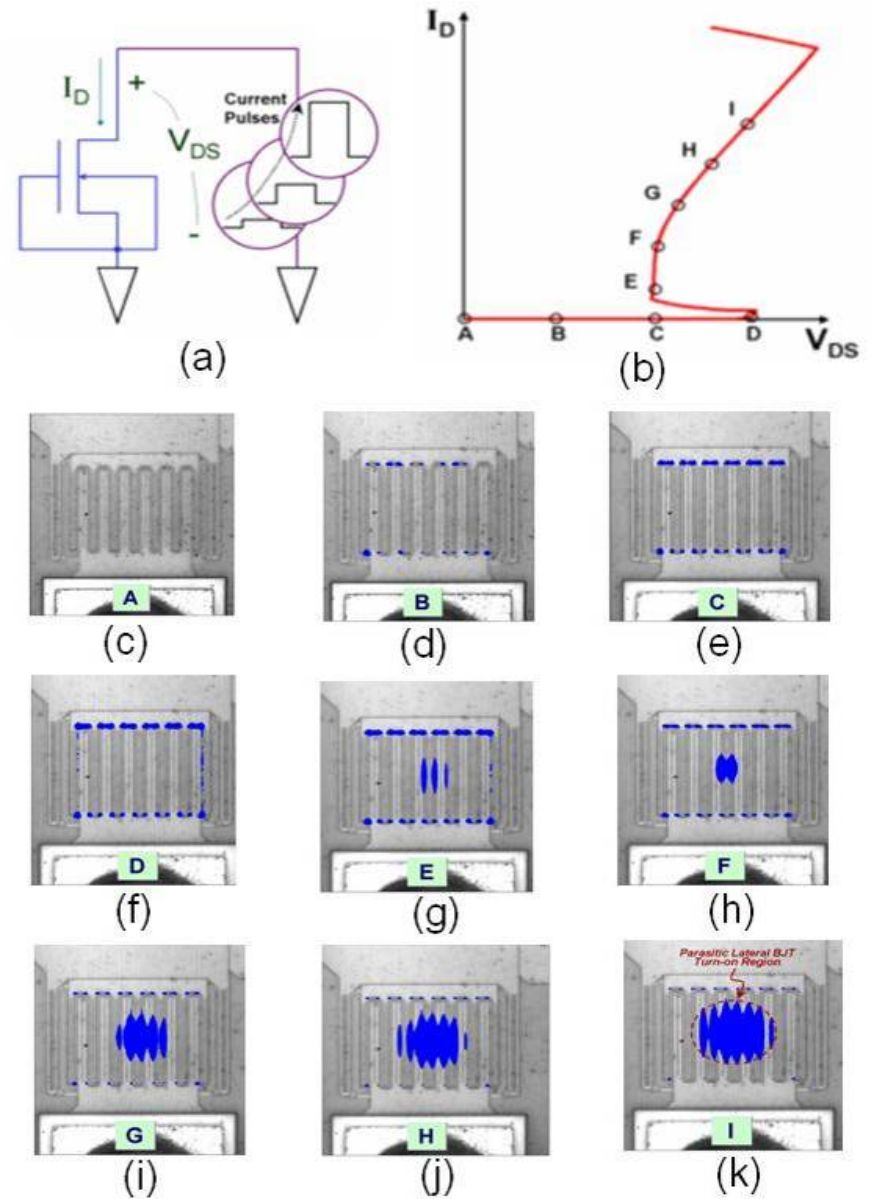


Fig. 2.5 EMMI photographs on a gate-grounded NMOS (W/L = 300μm=0.5μm) to show its turn-on behavior under the stress of different pulsed currents. (a) The measurement setup. (b) The corresponding I–V curve of a gate-grounded NMOS. (c)–(f) The hot spots in the gate-grounded NMOS before it enters into the snapback region. (g)–(k) The hot spots in the gate-grounded NMOS after it enters into the snapback region [5].

Chapter 3

Self-Substrate-Triggered Technique to Enhance the Turn-on Uniformity of Multi-Finger ESD Protection Devices

3.1 PRIOR DESIGNS TO ENHANCE TURN-ON UNIFORMITY OF GGNMOS

3.1.1 Layout Skill

In the traditional layout style of multi-finger GGNMOS, the difference in the base resistance of each parasitic BJT is a main reason to cause non-uniform turn-on phenomenon. Fig. 3.1 shows a layout style that can make the base resistance of each parasitic lateral n-p-n BJT in the multi-finger GGNMOS approximately equal, which is implemented by inserting a P+ diffusion region adjacent to the source terminals of each finger NMOS transistor [20]. With the equal base resistance, all parasitic lateral n-p-n BJTs can be triggered on simultaneously to discharge ESD current. However, the layout area is greatly increased by the insertion of P+ diffusion region into each source region. Also, such a layout style is strictly prohibited in the deep-submicron CMOS processes, because the substrate resistance of each finger NMOS drawn in this layout style becomes so small that all parasitic lateral n-p-n BJTs in the NMOS fingers are hard to be triggered on quickly to protect the thin gate-oxide of internal circuits [21].

3.1.2 Gate-Coupled Technique

Fig. 3.2 shows the ESD protection circuit with gate-coupled technique [11]. The NMOS/PMOS is configured with its drain connected to the input pad and its source connected to the VSS/VDD. A capacitor is connected between the input pad and the gate of

NMOS/PMOS transistor. A resistor is connected between the VSS/VDD and the gate of NMOS/PMOS transistor. By tuning the resistance and capacitance, a suitable voltage can be coupled to the gate of NMOS/PMOS only under the high-voltage ESD stress condition, thus lowering the trigger voltage of NMOS/PMOS. The non-uniform turn-on issue of large-sized multi-finger NMOS can be overcome through the gate-coupled technique. However, the higher gate bias coupled to NMOS/PMOS will induce more channel current and higher electric field to rupture the thin gate oxide of NMOS/PMOS. Therefore, the ESD robustness of ESD protection device will be suddenly degraded at the higher coupled gate bias during ESD stresses, i.e. over-gate-driven effect [5], [13]-[15]. Gate-coupled ESD protection circuit must be carefully designed and optimized to avoid the sudden degradation on ESD level.

3.1.3 Substrate-Triggered Technique

One ESD protection circuit with substrate-triggered technique is shown in Fig. 3.3 [16]. The capacitance and resistance must be tuned for coupling a suitable voltage to the body of parasitic lateral n-p-n BJT (or the substrate of GGNMOS) only under ESD stress condition to lower the trigger voltage of GGNMOS, which can improve the turn-on uniformity of GGNMOS.

As compared with the gate-coupled design, the substrate-triggered technique is to increase the base voltage of the parasitic BJT, thus avoiding the channel current and the overstress across the gate oxide. Therefore, the substrate-triggered technique can continually improve ESD robustness of the ESD protection devices without the sudden degradation as that in the gate-coupled design. The substrate-triggered design can safely and effectively improve the ESD robustness of ESD protection devices [5], [17], [18].

3.1.4 Multi-Finger Turn-on Technique

Fig. 3.4 depicts the domino-type multi-finger turn-on technique [22] to solve the non-uniform turn-on issue of GGNMOS, where the R_{Dn}/R_{Sn} is the drain/source ballast resistor. The resistor $R_{Si,MFT}$ in each finger NMOS transistor is used to generate a voltage bias to the adjacent gate. After one arbitrary finger is triggered on as indicated by the arrow at finger F_2, the initial ESD current flows through resistor $R_{S2,MFT}$ and builds up a potential V_{Si2} to bias the NMOS gate of finger F_3. Therefore, the parasitic BJT inherent in the finger F_3 can be triggered on due to the well-known gate-coupled effect. The same mechanism transfers the internal source signal at Si_3 to the gate of finger F_4, thus triggering the finger F_4. Through this domino effect of subsequently triggered fingers, the entire fingers in the GGNMOS structure are eventually forced into a homogenous conduction state [22]. The values of the resistors in this circuit should be designed appropriately to achieve the expected results, and the layout realization is more complicated.

3.2 SELF-SUBSTRATE-TRIGGERED TECHNIQUE

There are two main issues those responsible for the non-uniform turn-on problems of multi-finger GGNMOS. One is that the parasitic lateral n-p-n BJTs of center fingers usually have the largest substrate (base) resistance under traditional layout style, which makes the center-finger NMOS transistors be triggered on earlier. The other is the obvious snapback characteristics of the parasitic lateral n-p-n BJT inherent in NMOS, which makes the first turned-on center fingers solely sustain the high ESD current. In this work, the above-mentioned characteristics that originally lead to non-uniform turn-on phenomenon will be used to improve the turn-on uniformity of multi-finger GGNMOS.

The proposed self-substrate-triggered GGNMOS (SST_GGNMOS) just utilizes the current of the first triggered-on center NMOS fingers as the substrate-triggered current for promoting the turn-on uniformity among the fingers. The equivalent circuits of

SST_GGNMOS for on-chip ESD protection designs of the input and output pads to VSS are shown in Fig. 3.5(a) and (b), respectively. The configurations are similar to the traditional multi-finger GGNMOS, except that the source of the center-finger NMOS transistors is connected to the parasitic bipolar base terminals of all the other fingers instead of connecting to ground. For the output ESD protection application in Fig. 3.5(b), the gates of the center-finger NMOS transistors are connected to ground instead of the pre-driver to avoid disturbance of normal circuit function. While ESD pulse is applied to the I/O pad, the center-finger NMOS transistors are turned on first and then the current flows from the center fingers to the bases of all the other parasitic lateral n-p-n BJTs. The current from the center-finger NMOS transistors will result in a voltage drop across the substrate (base) resistor to elevate the voltage of base terminals, which will make the parasitic n-p-n lateral BJTs turn on more efficiently to discharge ESD current and thus improve ESD levels.

Fig. 3.6(a) and (b) show the layout top-view and cross-sectional view of SST_GGNMOS, respectively. The layout is realized by inserting the P+ diffusion regions in the drain of each finger NMOS transistor as the substrate-triggered nodes. The source terminal of the center-finger NMOS transistors is connected to these substrate-triggered nodes. Because the drain area is usually larger than its source area in the layout of multi-finger GGNMOS with silicide blocked region, inserting the P+ triggered nodes does not increase the total layout area. Besides, no additional masks (such as ESD implantation [23]) and external triggering circuits are needed in the proposed self-substrate-triggered GGNMOS. That is, ESD level can be improved without increasing the layout area and fabrication cost through the self-substrate-triggered technique.

3.3 EXPERIMENTAL RESULTS AND DISCUSSION

The novel SST_GGNMOS has been realized in a 0.13-μm CMOS process with gate-oxide thickness of 25Å. To guarantee that the center-finger NMOS transistors can be turned on first

to trigger on the others, the channel lengths of the center-finger NMOS transistors (Lcf) are drawn with the minimum rule of 0.13μm, whereas those of the other fingers are drawn with 0.18μm in the SST_GGNMOS structure. The traditional multi-finger GGNMOS with all channel lengths of 0.18μm is also fabricated in the same chip for comparison. Each finger width of these two devices is kept as 30μm, and the maximum finger number is as many as 20. Both of traditional GGNMOS and the proposed SST_GGNMOS have silicide blocked region on their drain sides. After silicon fabrication, the dc characteristics of the SST_GGNMOS device are measured by the parameter analyzer (*HP 4156B*). The automatic transmission line pulsing (TLP) system [24], [25], the human-body-model (HBM), and the machine-model (MM) ESD testers are used to verify the ESD levels of the traditional GGNMOS and the new-proposed SST_GGNMOS. The Emission Microscope (EMMI) is used to distinguish the turn-on behaviors between the new proposed SST_GGNMOS and the traditional GGNMOS.

3.3.1 Characteristics of the SST_GGNMOS

To investigate the characteristics of SST_GGNMOS, the layout of the SST_GGNMOS with W/L = 360μm/0.18μm (Lcf = 0.13μm) is slightly modified in the test chip. The source of the center fingers is not connected to the P+ triggered nodes but connected to ground. The P+ triggered nodes are connected outward to a bond pad as the base terminal of the parasitic BJT inherent in the SST_GGNMOS structure. Fig. 3.7 shows the experimental setup and the definitions of the current and voltage components in this measurement. The parameter analyzer (*HP 4156B*) is used to measure the dc characteristics of the SST_GGNMOS. The equivalent P-well resistance inherent in the P+ trigger nodes to the P+ substrate guard ring is denoted as R_well. The applied current into the P+ triggered node is denoted as I_T and the current into the base-to-emitter (B-E) junction is denoted as I_B in Fig. 3.7.

The measured base-to-emitter dc *I-V* curve of the SST_GGNMOS with channel width of 360μm is shown in Fig. 3.8. The inset shows the experimental setup. The collector terminal of

the parasitic lateral n-p-n BJT is floating, and a voltage is applied to the base and emitter terminals to investigate the characteristics of the B-E junction diode. Because the reverse-bias saturation current of B-E junction diode is quite small and omissible, the *I-V* data of negative VBE is fit linearly to define the equivalent P_well resistance. As shown in Fig. 3.8, the B-E junction diode is in parallel with an inherent P-well resistance (R_well) of ~172Ω, and the B-E junction diode does not dominate the *I-V* characteristics until the base-to-emitter voltage (VBE) is larger than 1.1V. That is, the voltage drop across the effective P-well resistance must be ~1.1V to turn the parasitic lateral BJT 'on' by forward biasing the base-to-emitter junction. The relation between the substrate-triggered current and the corresponding value of VBE under the condition of VCE = 1.2V is shown in Fig. 3.9. For the substrate-triggered current between 0mA and 6mA, VBE is smaller than 1.1V, so the R_well dominates the *I-V* characteristics and the base-to-emitter voltage (VBE) increases linearly with the substrate-triggered current (I_T) as expected. The substrate-triggered current must be greater than ~7mA to make the base-to-emitter voltage higher than 1.1V, as indicated by the dotted line in Fig. 3.9.

The relation between the current gain of parasitic lateral n-p-n BJT in the SST_GGNMOS structure (W = 360μm) and the substrate-triggered current under the measured conditions of VCE = 1.2V and VBE = 0 - 2V is shown in Fig. 3.10. The base current I_B is calculated as

$$I_B = I_T - \frac{VBE}{R\_well} \tag{1}$$

where R_well is the equivalent P-well resistance inherent in the SST_GGNMOS structure. The current gain is defined as the differential value of I_C to I_B. As indicated by the dotted line in Fig. 3.10, the substrate-triggered current must be larger than 6.2mA for the current gain of the parasitic lateral n-p-n BJT to be greater than unity, which is the key factor of effective conduction of parasitic lateral n-p-n BJT.

The measured dc *I-V* curves of SST_GGNMOS device under different substrate-triggered currents (I_T) are shown in Fig. 3.11. When the substrate-triggered current injected at the P+ triggered nodes is increased from 0mA to 6mA, the trigger voltage of the SST_GGNMOS device is only reduced slightly from 4.8V to 4.4V, and the SST_GGNMOS still goes through snapback region. On the contrary, when the substrate-triggered currents are above 7mA, the parasitic BJT is initially turned on and the SST_GGNMOS device can conduct high current without the snapback mechanism. From the above experimental results, it is concluded that the substrate-triggered current must be greater than ~7mA to achieve the substrate-triggered effect for the SST_GGNMOS with channel width of 360μm in this testchip.

3.3.2 Substrate-Triggered Current Provided by the Center Fingers

As shown in Fig. 3.12(a), to observe the substrate-triggered current provided by the center fingers, the voltage pulses with different pulse amplitudes generated by the 100-ns TLP system are applied to the drain terminal of the SST_GGNMOS with channel width of 360μm. The pulse width generated by the TLP system is as short as 100ns to simulate the ESD condition. With the specially drawn testchip, the source of the center-finger NMOS transistors and the source of the others are separately connected to different bond pads, and then wired to each other with a current probe on it for measuring the transient current generated by the center fingers. As shown in Fig. 3.12(b) and (c), the measured substrate-triggering currents provided by the center fingers are as large as 20mA and 180mA under the applied 0-to-5V and 0-to-30V TLP voltage pulses, respectively. The measured current waveform shows that the center fingers are turned on under TLP pulses and can quickly generate substrate-triggered currents. Fig. 3.12(d) shows the relation between the TLP voltage magnitude and the substrate-triggered current provided by the center fingers (Icf). When the magnitude of the TLP voltage pulse is smaller than the trigger voltage of the center fingers (~4.8V), the center

fingers are not turned on, thus the substrate-triggered current is zero for TLP voltage from 1V to 4V. As long as the TLP voltage is larger than the trigger voltage of the center fingers, the center fingers are turned on to provide triggering current much larger than 7mA. That is, the center fingers can provide adequate substrate-triggered current to effectively promote turn-on uniformity of SST_GGNMOS. To further reduce the trigger voltage of center fingers, the gate-coupled technique (with a small capacitance from the pad to the gate of center fingers) can be added into this SST_GGNMOS. Such a small capacitance can be realized by the overlap metal layers under the bond pad, therefore the overall layout area of I/O cell is still kept the same.

In reality, the source of the center fingers is connected to the substrate-triggered nodes in the SST_GGNMOS structure. Thus, the current of the center fingers will flow through the inherent resistor R_well to create a voltage drop between the base and emitter terminals and to trigger on the other fingers. As long as the other fingers are triggered on, the center fingers would be suppressed to turn off because the voltage potential between the base and emitter terminals of the center fingers becomes approximately zero.

3.3.3 TLP Measurement Results

The TLP system provides a single and continually-increasing-amplitude pulse to the device under test, the pulse width is as short as 100ns to simulate the ESD condition. By using the TLP measurement, the snapback characteristics and the secondary breakdown currents (It2) of the devices can be investigated. It2 is the index for HBM ESD robustness, which is indicated as the corresponding current when the leakage current under the voltage bias of 1.2V is above 1μA in this work. The relation between It2 and HBM ESD level (VESD) can be approximated as VESD≅It2×1.5kΩ, where 1.5kΩ is the equivalent resistance of human body.

Fig. 3.13(a) and (b) show the TLP-measured I-V curves and the corresponding leakage currents of the traditional GGNMOS and the SST_GGNMOS under different channel widths, respectively. In the SST_GGNMOS structure, the center fingers with shorter channel length will go through snapback region first. Therefore in Fig. 3.13(b), the SST_GGNMOS still have obvious snapback characteristics like the traditional GGNMOS as shown in Fig. 3.13(a). The It2 of GGNMOS and SST_GGNMOS both increase with channel width, but the It2 of the SST_GGNMOS (3.5A) is greater than that of traditional GGNMOS (2.9A) under the same device size (channel width of 480μm). To more clearly distinguish between these two devices, the dependence of It2 per unit channel width on device total channel width is shown in Fig. 3.13(c).

In Fig. 3.13(c), the It2 per unit channel width of traditional GGNMOS decreases from 7.4mA/μm to 5.8mA/μm when the channel width increases from 240μm to 480μm. In Fig. 3.13(c), the It2 of traditional GGNMOS cannot increase linearly with channel width, which is due to the non-uniform turn-on issue among the multiple fingers of large-sized GGNMOS. On the contrary, the It2 per unit channel width of the SST_GGNMOS remains higher than 7.4mA/μm as the channel width increases to 600μm. Moreover, when the device channel width increases, the It2 per channel width is still almost kept the same (with only a little degradation) in the SST_GGNMOS. This implies that the turn-on uniformity can be effectively achieved by the proposed self-substrate-triggered technique. From these experimental results, the It2 of the proposed SST_GGNMOS has better width scalability, and the SST_GGNMOS can sustain more ESD current than that of traditional GGNMOS under the same layout area.

3.3.4 ESD Robustness

The HBM and MM ESD stresses are applied to the ESD protection devices to verify their ESD robustness. In these ESD verifications, the devices are tested under the

positive-to-VSS ESD stress, and the failure criterion is defined as the measured voltage at the current level of 1μA shifted 30% from its original value. The comparison of the ESD levels between the traditional GGNMOS and the SST_GNMOS is shown in Fig. 3.14. In Fig. 3.14, under the same device dimension (channel widths of 360μm and 480μm), the HBM ESD level of the SST_GGNMOS is two times larger than that of traditional GGNMOS. When the device channel width is increased, the HBM ESD level of the SST_GGNMOS is increased considerably, however, that of GGNMOS is only increased a little. The experimental results show that the HBM ESD level can be greatly improved through the self-substrate-triggered technique, which is consistent with the TLP measurement results (higher It2 leads to higher HBM ESD level). However, in the experimental results, the correlation between It2 and HBM ESD levels of traditional GGNMOS and SST_GGNMOS is different. The equivalent HBM resistance (HBM ESD level divided by It2) of traditional GGNMOS is smaller than that of SST_GGNMOS. Such miscorrelation may result from circuit splits, which had also been observed in a 0.13- m CMOS process [26].

Fig. 3.15 shows the relation between the device channel widths and the MM ESD levels of GGNMOS and SST_GGNMOS. For the traditional GGNMOS, even the device channel width increases to 480μm, the MM ESD level (only 100V) is still below the typical commercial specification of 200V. But, the MM ESD levels of the proposed SST_GGNMOS are 200V, 250V, and 375V for device channel widths of 360μm, 480μm, and 600μm, respectively. The experimental results of HBM and MM ESD levels have verified that the SST_GGNMOS has superior ESD robustness than the traditional GGNMOS.

3.3.5 Turn-on Analysis by EMMI

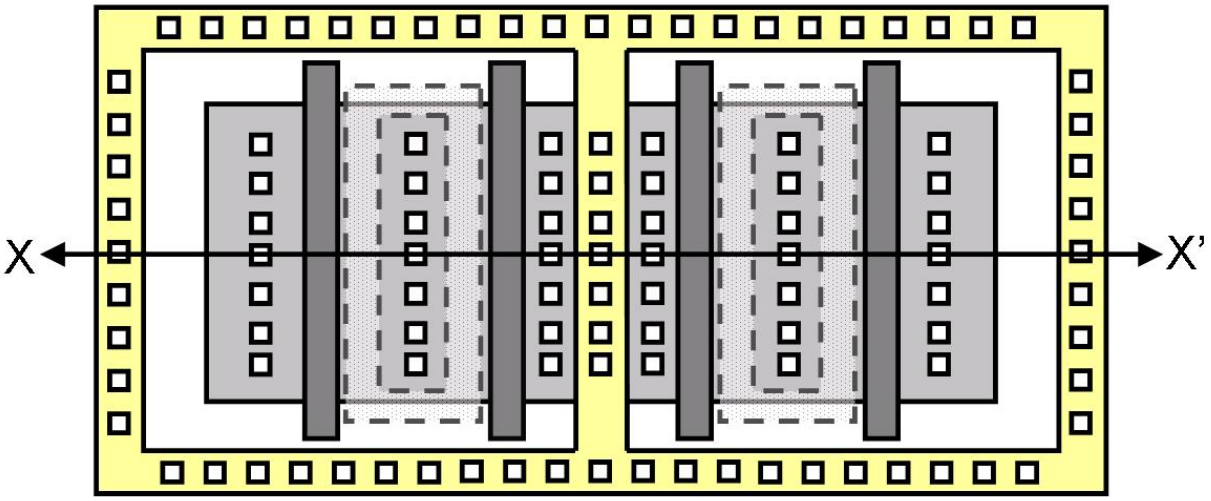
To compare the turn-on behaviors between the traditional GGNMOS and the new proposed SST_GGNMOS, the spatial distribution of ESD-like currents were directly observed by using EMMI analysis on these two devices. EMMI is a widely used technique for

wafer-level reliability and yield analysis for semiconductor devices. In general, the analysis is performed by collecting the emitted visible and near infrared wavelength photons when impact ionization and the recombination of electron-hole pairs occurs [4]. In this work, the packaged testchip was thinned on the back-side to allow the detection of the photons emission from the back side of the devices, which has been referred as back-side EMMI analysis. The back-side EMMI analysis can avoid the emitted photons covered by the overlying layers such as dielectrics and metal interconnections, and thus can observe the turn-on regions more clearly.

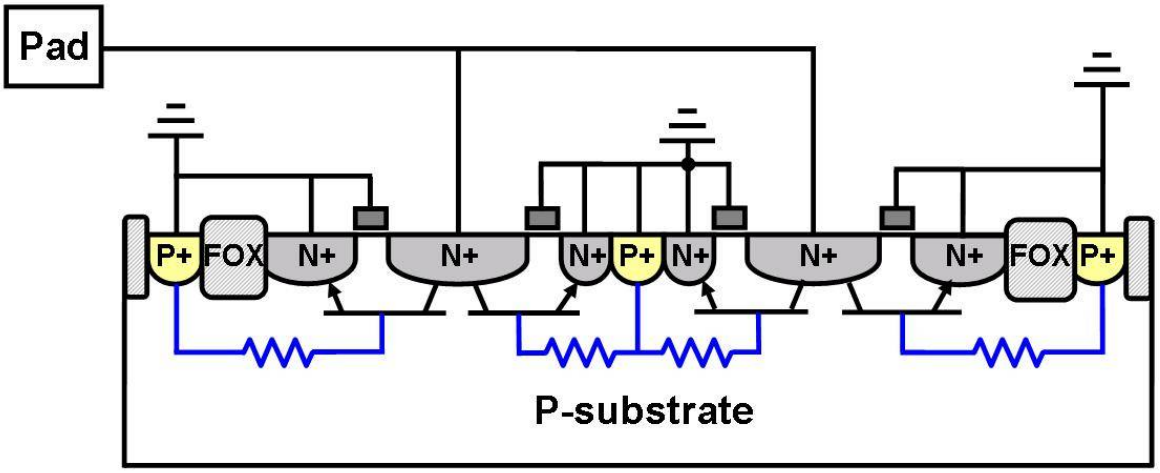
Fig. 3.16 (a) and (b) show the back-side EMMI photographs of traditional GGNMOS and the SST_GGNMOS when ESD-like current pulses with magnitude of 50mA is injected into their drain regions through the bond pad, respectively. The channel widths of these two devices are both 480μm, and the width of unit finger is 30μm (the total finger number is 16). Fig. 3.16(a) confirms that the turn-on regions of the traditional GGNMOS are only located at the center regions (two center fingers) of whole device area. However, as the colored images shown in Fig. 3.16(b), the currents are uniformly distributed through the SST_GGNMOS except the two center fingers. As long as the center fingers trigger the others on, the current will be mainly discharged through the other 14 fingers, and the center fingers will be off. The turn-on time of the center fingers are too short for the EMMI system to collect enough photons. So, in the back-side EMMI photograph, the regions of the center fingers are not colored. The EMMI photographs have practically proven that the turn-on uniformity of the SST_GGNMOS is superior to that of the traditional GGNMOS.

3.4 CONCLUSION

To improve the turn-on uniformity of multi-finger GGNMOS, a novel self-substrate-triggered technique has been designed and verified in a 0.13-μm CMOS process with gate-oxide thickness of 25Å. The device characteristics of SST_GGNMOS have been successfully verified in silicon and the experimental results have confirmed that the center-finger NMOS transistors can provide the SST_GGNMOS with sufficient substrate-triggered current. The HBM ESD level, MM ESD level, and the It2 per unit channel width of the SST_GGNMOS are all much higher than those of the traditional GGNMOS. Furthermore, the back-side EMMI photographs confirm that the SST_GGNMOS has superior turn-on uniformly than that of traditional GGNMOS under ESD-like current pulse stresses. The proposed SST_GGNMOS is a good solution for ESD protection design in the nano-scale CMOS technology.



(a)



(b)

Fig. 3.1 (a) The layout top-view and (b) the X-X' cross-sectional view of the layout skill that makes the base resistance of each parasitic BJT approximately equal by inserting a P+ diffusion adjacent to the source terminal of each finger NMOS transistor [20].

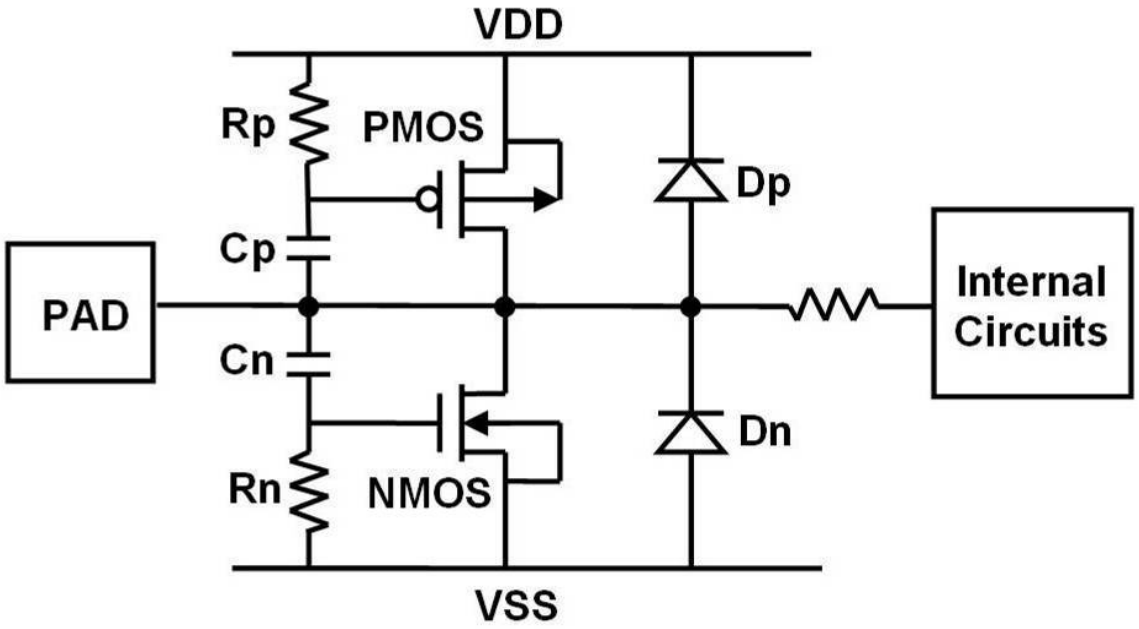


Fig. 3.2 ESD protection circuit with gate-coupled technique [11].

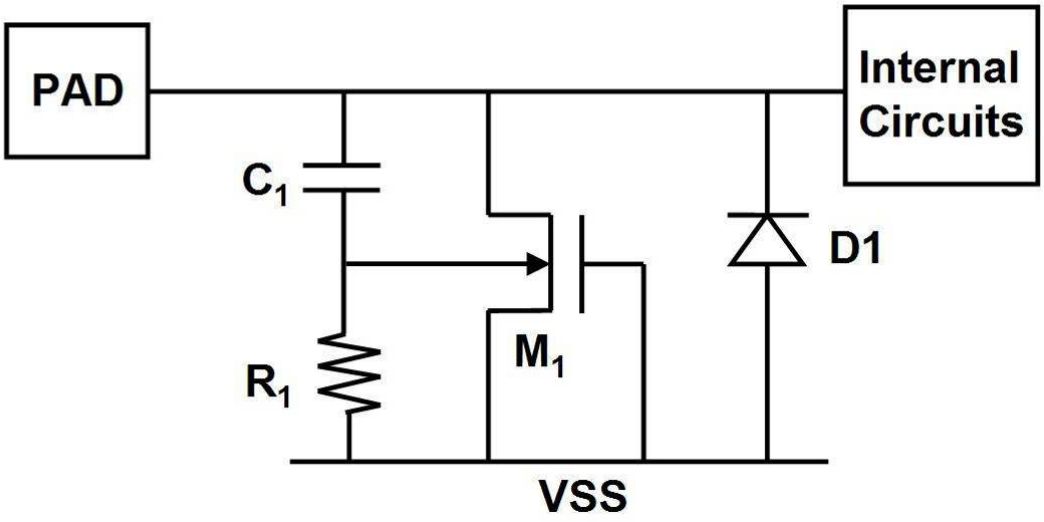


Fig. 3.3 ESD protection circuit with substrate-triggered technique [16].

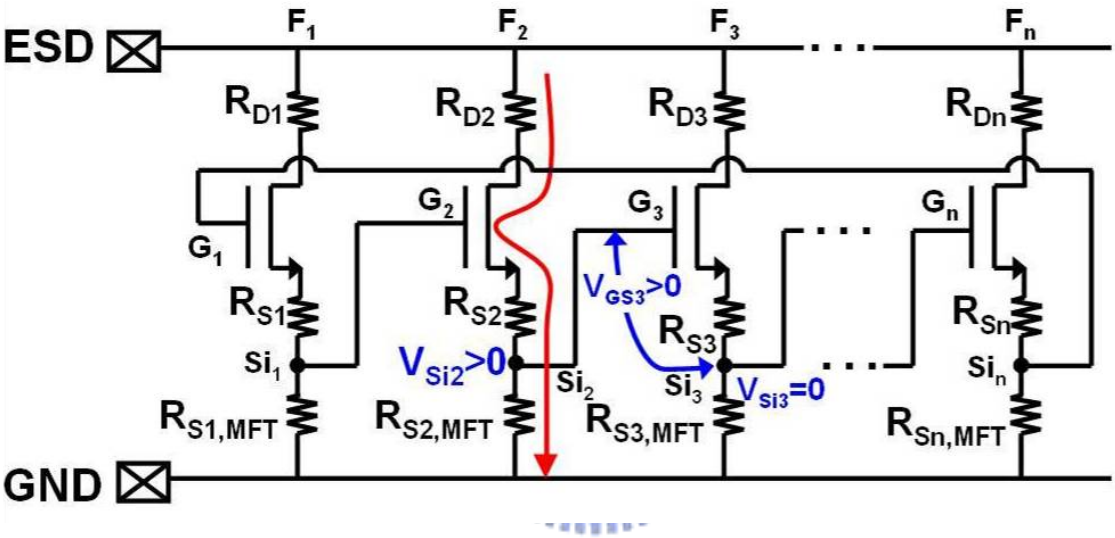
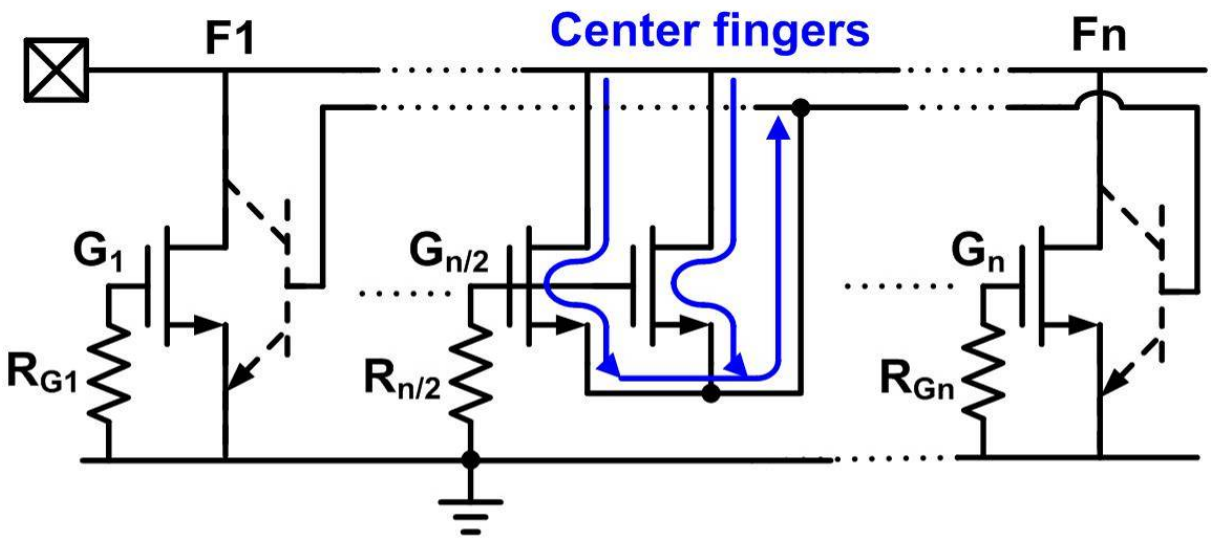
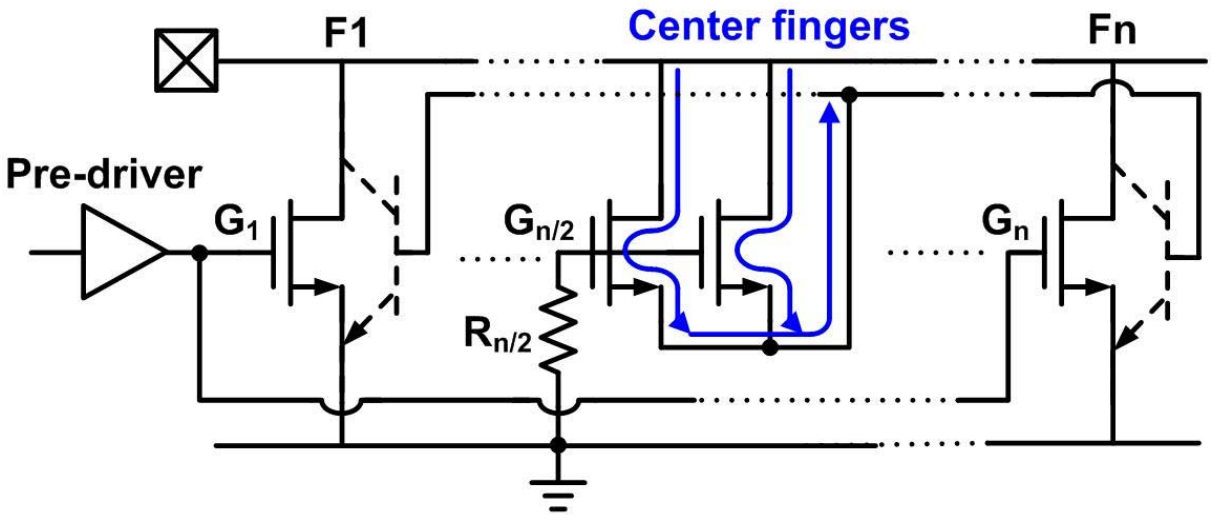


Fig. 3.4 Equivalent circuit of domino-type multi-finger turn on (source-gate-coupled) NMOS for subsequent finger triggering indicating the function of the device [22].

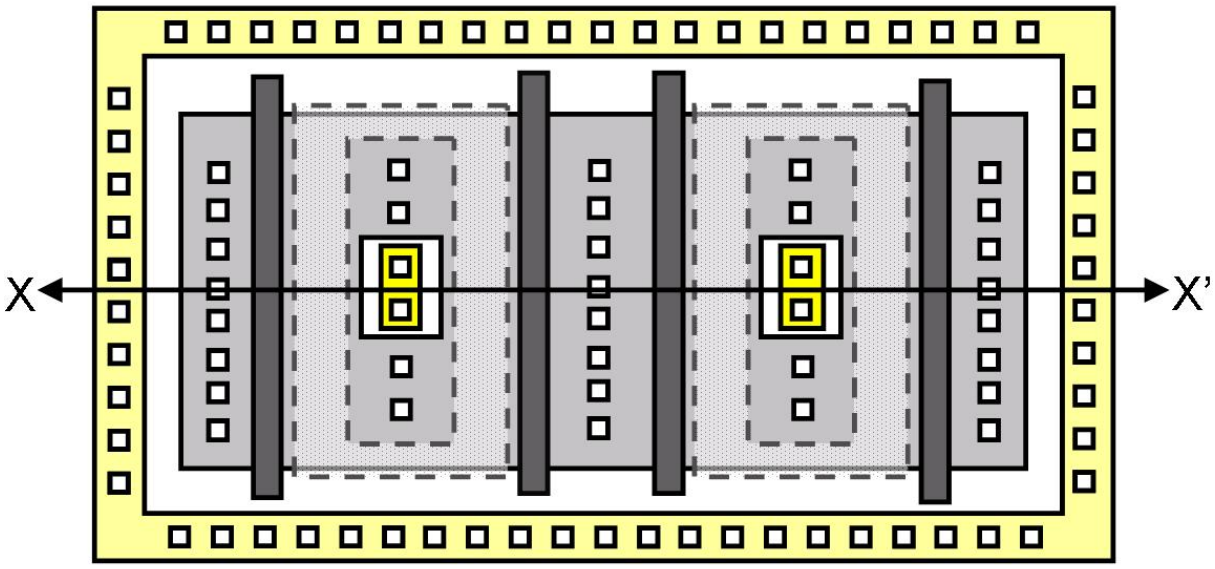


(a)

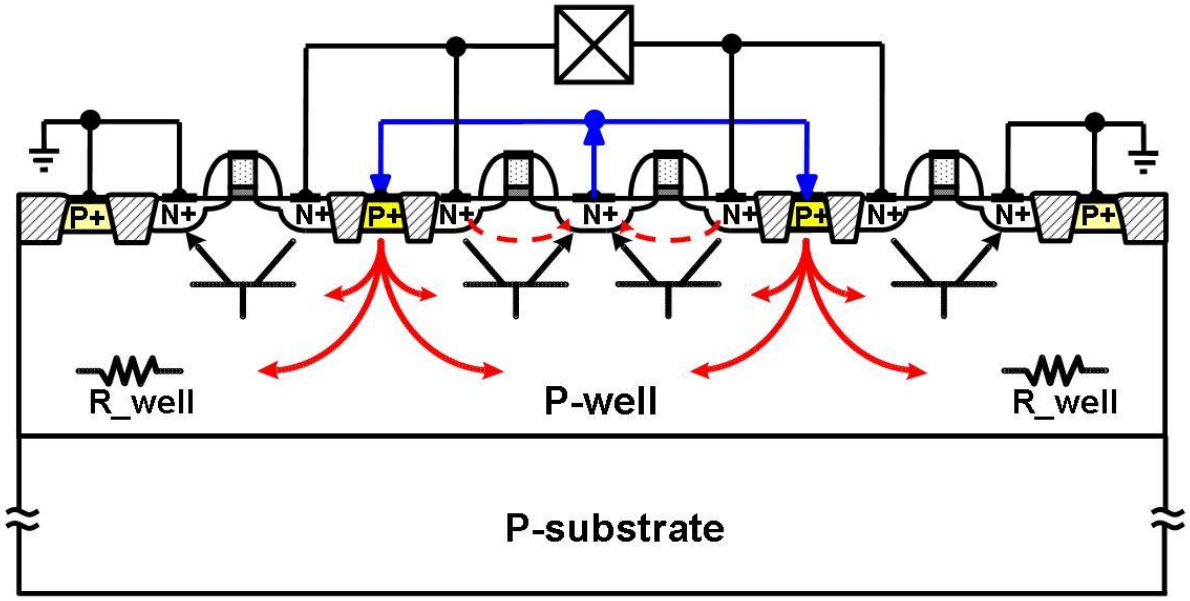


(b)

Fig. 3.5 The equivalent circuits of the self-substrate-triggered GGNMOS (SST_GGNMOS) for on-chip ESD protection design for (a) the input pad to VSS and (b) output pad to VSS.



(a)



(b)

Fig. 3.6 (a) The layout top view and (b) the X-X' cross-sectional view of the SST_GGNMOS. The P+ diffusion regions inserted to the drain of each finger as the substrate-triggered nodes are connected to the source terminal of the center-finger NMOS transistors.

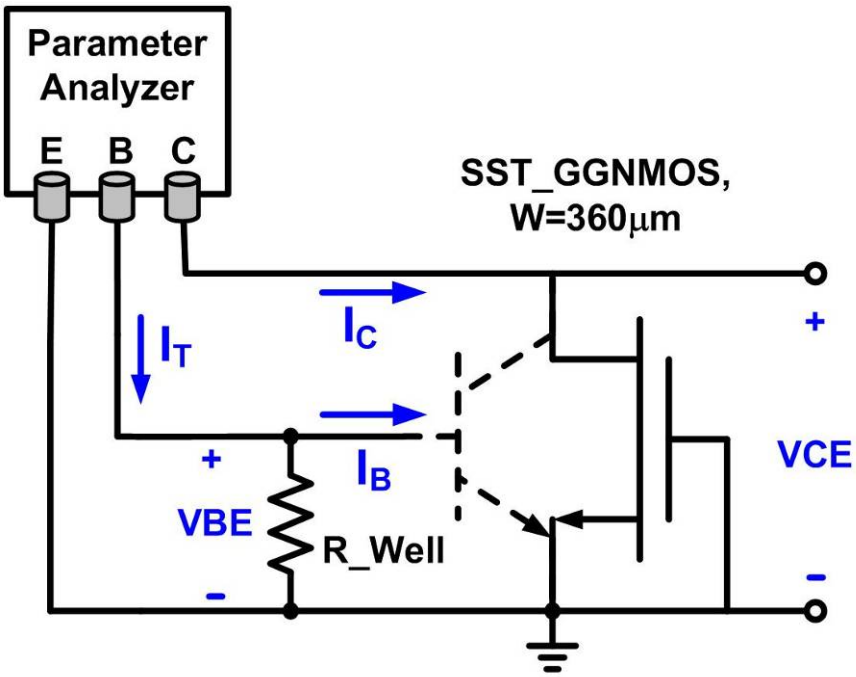


Fig. 3.7 The experimental setup and definitions of the current and voltage components to measure the dc characteristics of the SST_GGNMOS with channel width of 360μm.

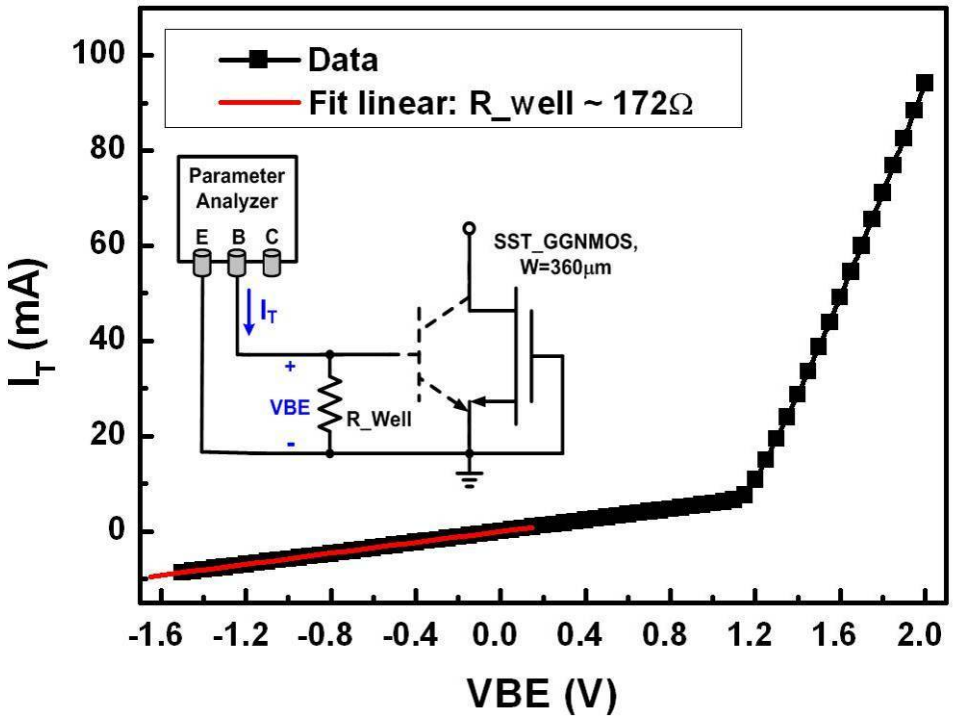


Fig. 3.8 The measured base-to-emitter dc I-V curve of the SST_GGNMOS with channel width of 360μm in an open-collector configuration.

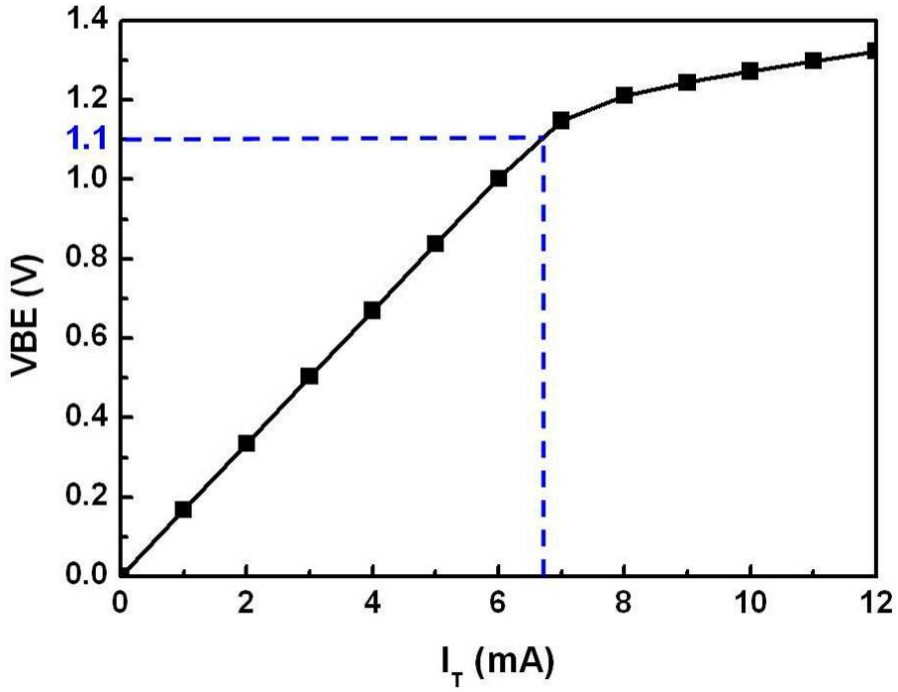


Fig. 3.9 The relation between the substrate-triggered current and the corresponding base-to-emitter voltage (VBE) under VCE of 1.2V.

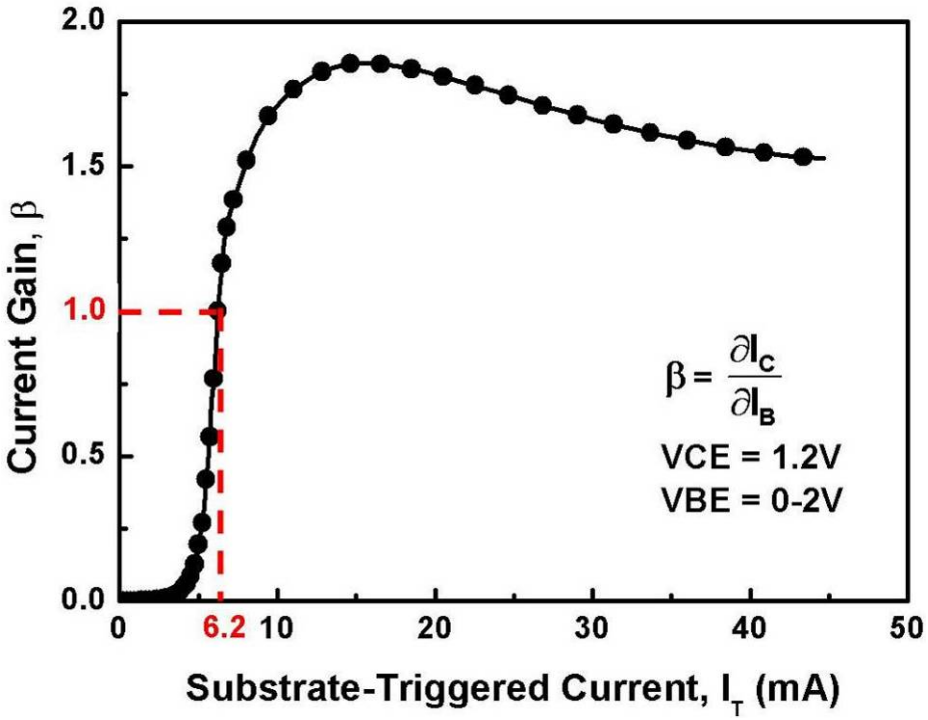


Fig. 3.10 The relation between the current gain of parasitic lateral n-p-n bipolar transistor inherent in the SST_GGNMOS and the substrate-triggered current under VCE of 1.2V and VBE from 0 to 2V.

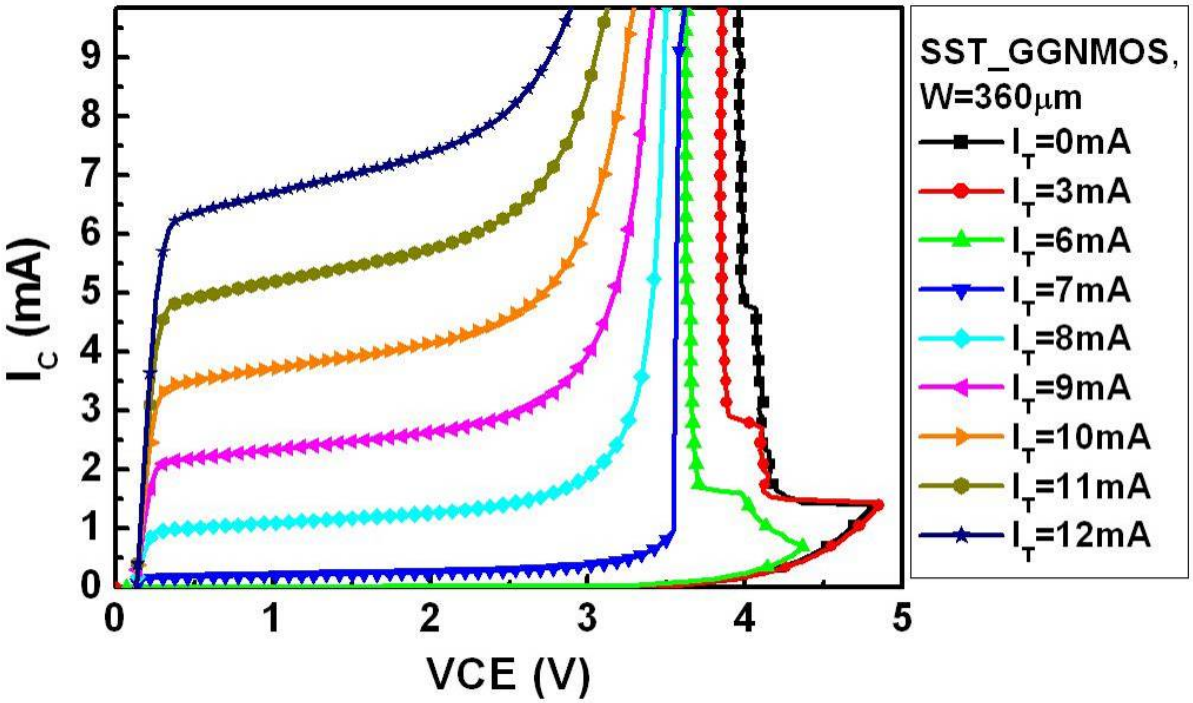


Fig. 3.11 The measured dc *I-V* curves of the SST_GGNMOS with channel width of 360μm under different substrate-triggered currents.

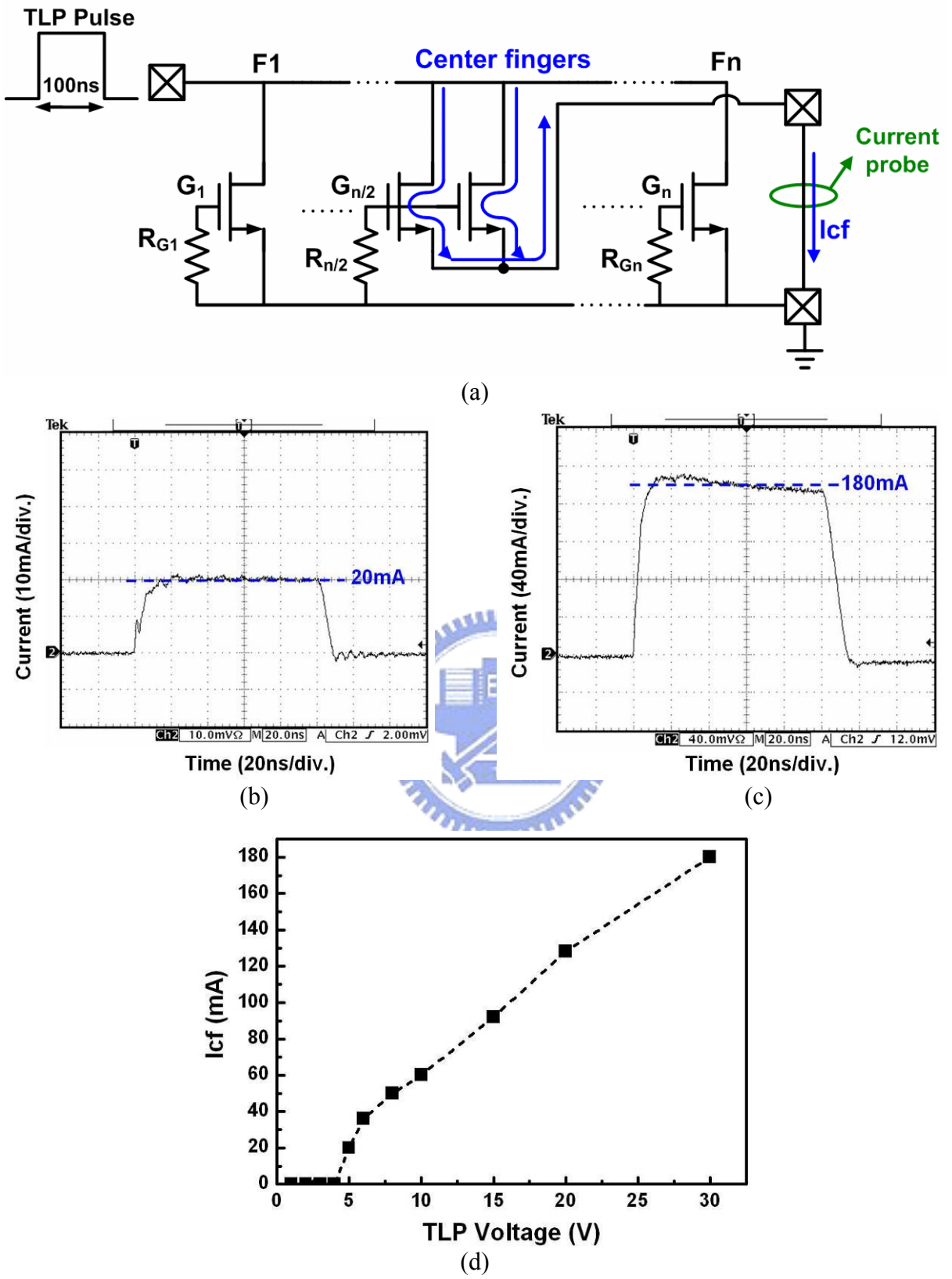
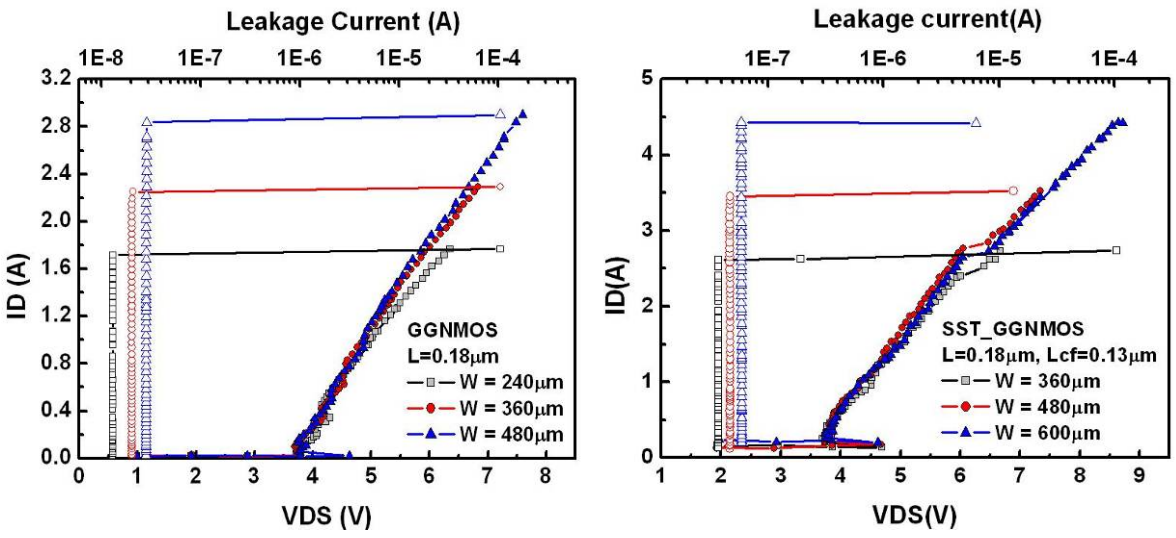
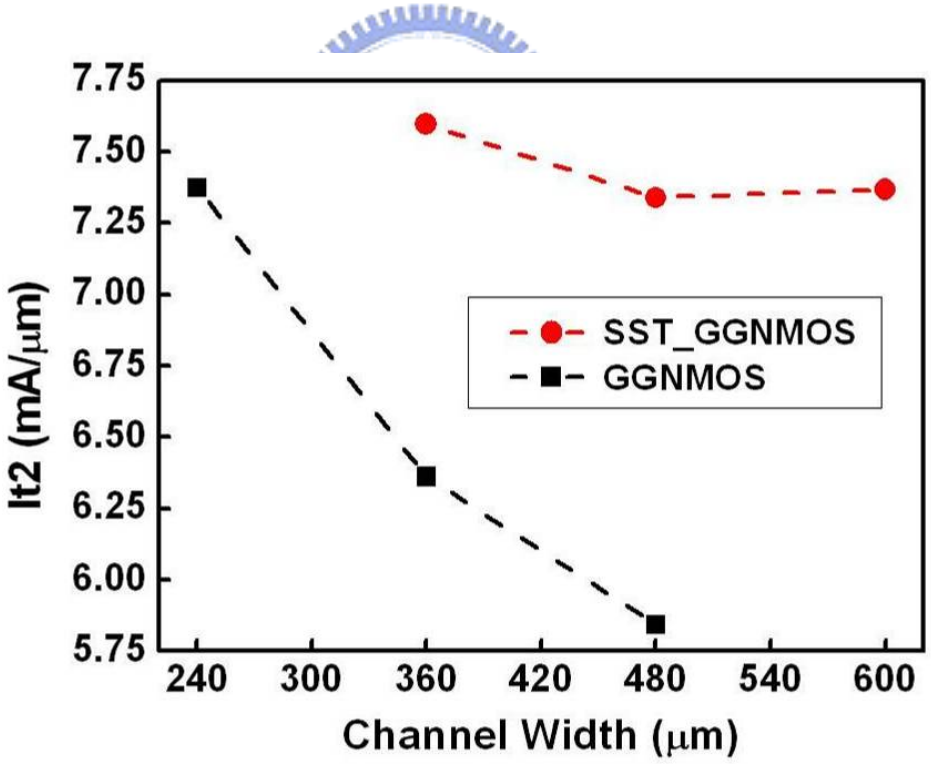


Fig. 3.12 (a) The measurement setup to observe the triggering current provided by the center fingers. The triggering current waveforms under the TLP pulse magnitude of (b) 5V and (c) 30V. (d) The relation between the TLP voltage magnitude and the triggering current provided by the center fingers (Icf).



(a) (b)



(c)

Fig. 3.13 The TLP-measured *I-V* curves of (a) the traditional GGNMOS and (b) the SST_GGNMOS under different channel widths, including the corresponding leakage currents under the drain voltage bias of 1.2V. (c) The comparison of It2 per micron between the traditional GGNMOS and the proposed SST_GGNMOS under different channel widths.

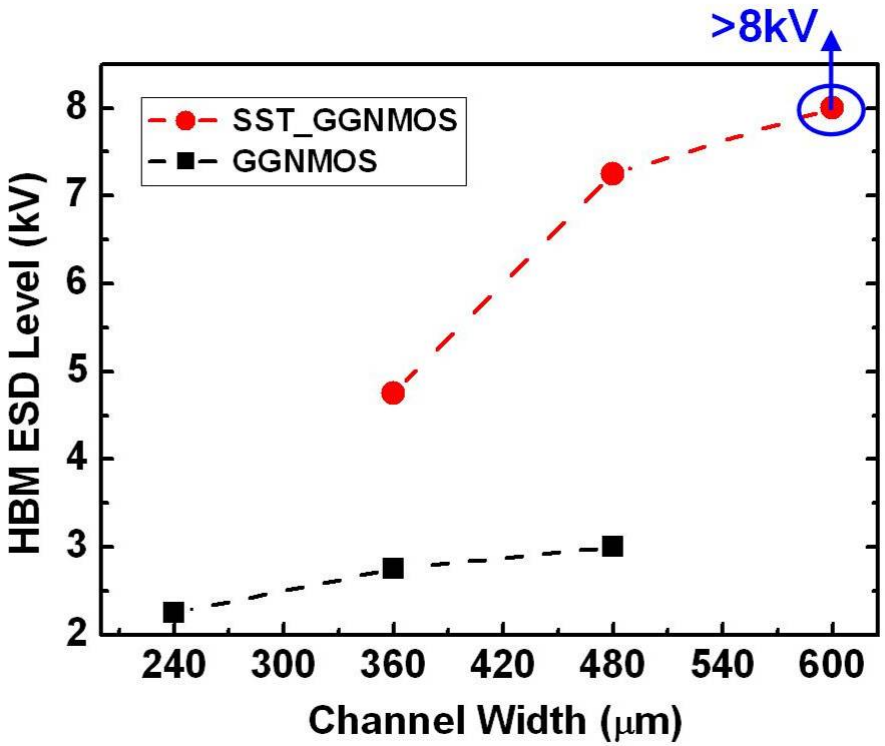


Fig. 3.14 The relation between the HBM ESD levels and channel widths of traditional GGNMOS and the proposed SST_GGNMOS.

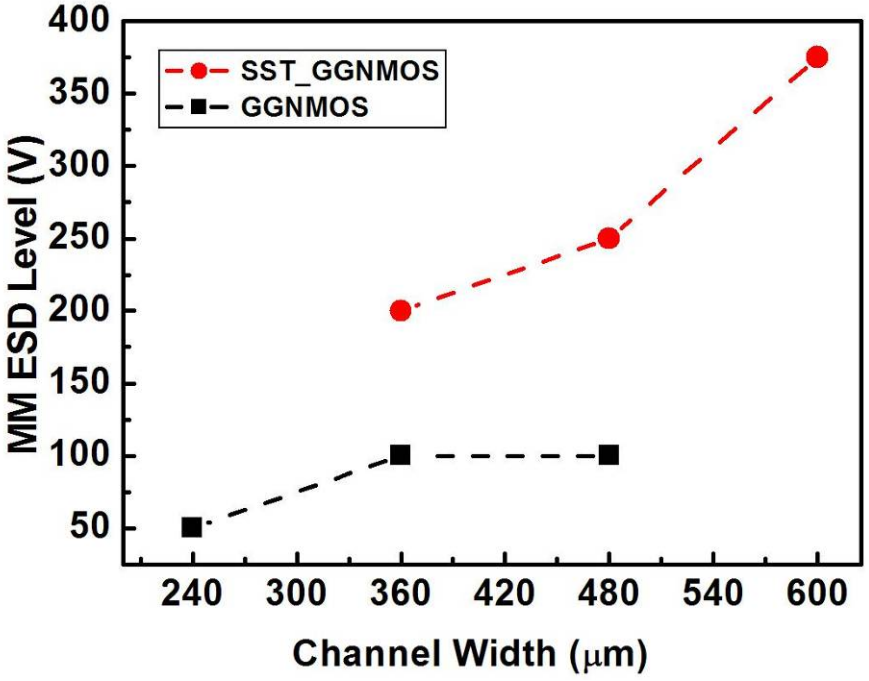
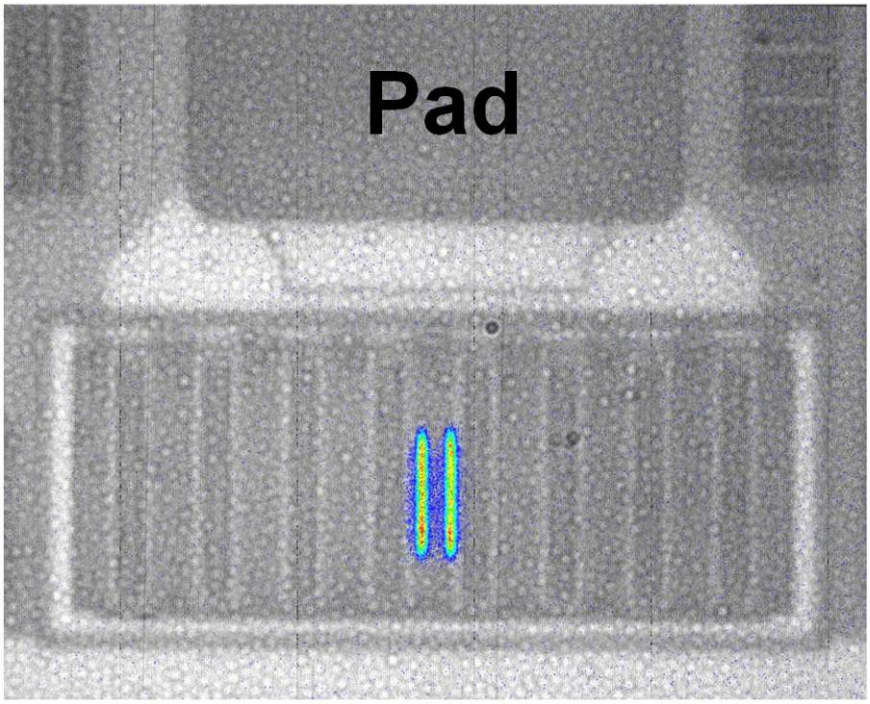
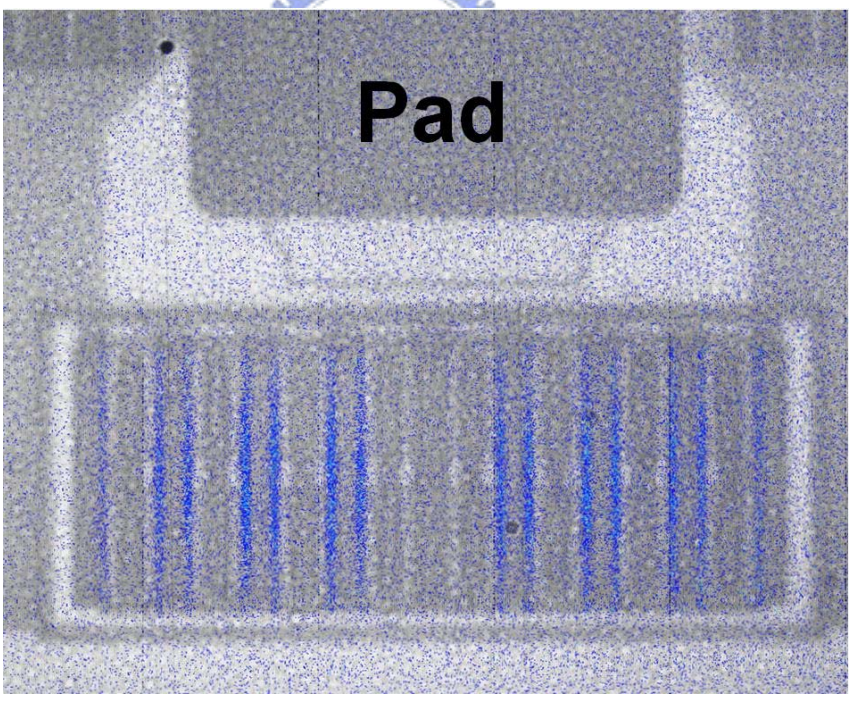


Fig. 3.15 The relation between the MM ESD levels and channel widths of traditional GGNMOS and the proposed SST_GGNMOS.



(a)



(b)

Fig. 3.16 Back-side EMMI photographs on (a) the traditional GGNMOS (W/L = 480μm/0.18μm) and (b) the SST_GGNMOS (W/L = 480μm/0.18μm, Lcf = 0.13μm) under current pulse of 50mA. The current distributions are shown with color in these two pictures, where are among the two center fingers in the traditional GGNMOS and among all fingers except the two center fingers in the SST_GGNMOS.

Chapter 4

Equal-Substrate-Potential Technique to Enhance ESD Robustness of Stacked-NMOS

4.1 INTRODUCTION

As semiconductor devices push to deep sub-micron geometries, the power supply voltages of integrated circuits have also scaled downwards for low power consumption and to meet the gate-oxide reliability. However, system-level power supplies have scaled at a much slower rate than chip supplies, since most systems today necessarily consist of mix chips fabricated in newer and older technologies, thus an electronic system could have chips operated at different voltage levels. This requirement has forced the interface circuits of chips manufactured in newer technologies to be backward compatible with the signal levels associated with older chips. Fortunately, the problem is usually reduced to that of high voltage tolerance, which requires the ability to receive rather than generate high voltage signals [27].

The conventional tri-state I/O buffer with 1.8-V gate-oxide devices in a 0.18-μm CMOS process is shown in Fig. 4.1, where the power supply voltage (VDD) is 1.8V. For high-voltage-tolerant (HVT) I/O interface application, the input signal at the I/O pad may rise up to 3.3V in the tri-state input mode. Thus, the channel of the output PMOS (Mp) and the parasitic drain-to-well junction diode inherent in the Mp will be conducted and cause the leakage current paths from the I/O pad to VDD [28], [29], as the dashed line shown in Fig. 4.1. Moreover, the gate-oxides of the output NMOS (Mn) and the input inverter stage are over-stressed by the 3.3-V input signal to cause the gate-oxide reliability problems [30] and

hot-carrier degradation [31]. Thus the conventional I/O circuits are unsuitable anymore to interface these chips with different voltage levels.

By using the additional thick gate-oxide process (or called as dual gate-oxide CMOS process [32], [33]), the gate-oxide reliability issue can be avoided, but the process complexity and wafer cost are increased. To solve the gate-oxide reliability issue without using the additional thick gate-oxide process, the stacked-NMOS structure had been widely used in the HVT I/O circuits. Fig. 4.2 shows the typical 1.8V/3.3V-tolerant I/O circuit. When the input signal at the I/O pad is 3.3V, the voltage at node X is about 1.2V (1.8-0.6 = 1.2) because the gate terminal of the top NMOS (Mn_top) is connected to 1.8V (VDD) and the threshold voltage of the devices is about 0.6V. Hence, the gate-drain voltages and gate-source voltages of the stacked devices, Mn_top and Mn_bot, are limited below 1.8V even if the input signal at the I/O pad is 3.3V. Therefore, the stacked-NMOS (Mn_top and Mn_bot) can solve the gate-oxide reliability problems. Besides, the pull-up PMOS (Mp1) has the gate-tracking circuit for tracking its gate voltage and N-well self-biased circuit for tracking its N-well voltage, which are designed to avoid the undesired leakage current paths through Mp when the 3.3-V input signals enter the I/O pad [34]-[37].

The on-chip ESD protection circuit for HVT I/O interfaces should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths during normal circuit operation condition. The above design constraints severely complicate the ESD protection circuits for HVT I/O interfaces. Besides, compared with single NMOS, stacked-NMOS has higher trigger voltage, higher snapback holding voltage, and lower It2. Therefore, the stacked-NMOS configuration usually has much lower ESD level compared with the single NMOS. The stacked-NMOS for ESD protection usually needs additional ESD detection circuit to improve its ESD level. In this chapter, an equal-substrate-potential technique is proposed to enhance the ESD robustness of stacked-NMOS without additional ESD trigger circuit.

4.2 EQUAL-SUBSTRATE-POTENTIAL STACKED-NMOS (ESP_STNMOS)

In the multi-finger NMOS layout structure, the substrate (base) resistances of the parasitic BJTs in central regions are higher than those in the side regions. Under ESD stress, the parasitic BJT with higher substrate resistance is usually turned-on first because the substrate potential is elevated higher in the self-biased mode. Therefore, the difference in substrate potential among each parasitic n-p-n BJT inherent in the multi-finger NMOS is a main reason to cause the non-uniform turn-on issue and degrade the ESD robustness of large-size multi-finger NMOS.

In this thesis, a novel circuit called equal-substrate-potential technique is proposed to solve the non-uniform turn-on problem by equalizing the substrate potential of each parasitic BJTs in multi-finger stacked NMOS. The equivalent circuit of equal-substrate-potential stacked-NMOS used as self-protection device is shown in Fig. 4.3. As shown in Fig. 4.3, there is a local substrate-node in each parasitic BJT of NMOS finger, and all of those local substrate-nodes are tied together to make the substrate-potential of the entire MOSFET approximately equal. As long as any finger is first turned on, the substrate potential of the first turned-on BJT can be transferred to all the other substrate-nodes, and thus all of the other fingers could be triggered on simultaneously to solve the non-uniform turn-on issue. Thus, the equal-substrate-potential technique can improve the ESD robustness of multi-finger stNMOS and reduce the turn-on resistance of MOSFET.

Fig. 4.4 shows the testkey for both stNMOS and ESP_stNMOS, the gate of top NMOS (top gate) is connected to VDD pad through a resistor of about 200Ω and a gate-grounded NMOS (W/L=240μm/0.25μm) is used to protect the top gate. The gate of bottom NMOS (bottom gate) is biased by an inverter whose input signal is VDD. Under dc leakage measurement, the bottom gate is biased to ground through an inverter, and the dc leakage current of stacked-NMOS can be measured. While under ESD-like condition (eg. under TLP

or ZapMaster measurements), the VDD pad, top gate, and bottom gate are all floating to approach the real condition.

Fig. 4.5(a) and (b) show the layout top-view and cross-sectional view of ESP_stNMOS, respectively. The layout realization is quite simple by inserting the P+ diffusion regions at the drain of each top NMOS transistor as the substrate-nodes. As shown in Fig. 4.5(b), the substrate-nodes are all connected together by metal line. The top gates are connected to VDD, and the bottom gates are connected to pre-driver. Because the layout area of top drain is usually larger in the multi-finger stNMOS layout style with silicide blocked region, inserting the P+ triggered nodes does not increase the total layout area. Moreover, there are no needs of external trigger circuits. That is, ESD level can be improved without increasing the layout area and fabrication cost through the equal-substrate-potential technique.

4.3 EXPERIMENTAL RESULTS AND DISCUSSION

The novel ESP_stNMOS has been realized in a 0.18-μm CMOS process. The channel lengths of both stNMOS and ESP_stNMOS are drawn with 0.25μm, and the unit finger width (Wf) is 60μm. There are four different size traditional stNMOS (channel widths of 240 μm, 360 μm, 480 μm, and 600μm) and one size ESP_stNMOS for comparison (channel width of 480μm). After silicon fabrication, the dc characteristics of the SST_GGNMOS device is measured by the parameter analyzer (*HP 4156B*). The automatic transmission line pulsing (TLP) system, the human-body-model (HBM), and the machine-model (MM) ESD testers are used to verify the ESD levels of the traditional stNMOS and the new-proposed ESP_stNMOS.

4.3.1 Characteristics of the ESP_stNMOS

The dc leakage current of traditional stNMOS and ESP_stNMOS under channel width of 480μm at a room temperature of 25ºC is shown in Fig. 4.6. The leakage current of

ESP_stNMOS is about one order larger than that of the traditional stNMOS under VDS of 3.3V and VDD of 1.8V. The larger leakage current of ESP_stNMOS may result from the inserted substrate-nodes, which influence the current distribution of ESP_stNMOS. The larger leakage current of ESP_stNMOS may be the side effect of equal-substrate-potential technique. Although the leakage current of ESP_stNMOS is larger, the leakage current is still below acceptable value.

To investigate the characteristics of ESP_stNMOS, the layout of the ESP_stNMOS with W/L = 480μm/0.25μm is slightly modified in the test chip. The substrate-nodes of the ESP_stNMOS are connected outward to a pad as the base terminal of the parasitic BJT inherent in the ESP_stNMOS structure. Fig. 4.7 shows the experimental setup and the definitions of the current and voltage components in this measurement. The parameter analyzer (*HP 4156B*) is used to measure the dc characteristics of the ESP_stNMOS. The equivalent P-well resistance inherent in the substrate-nodes to the P+ substrate guard ring is denoted as R_well. The applied current into the substrate-nodes is denoted as I_T and the current into the base-to-emitter (B-E) junction is denoted as I_B in Fig. 4.7.

The measured base-to-emitter dc *I-V* curve of the ESP_stNMOS with channel width of 480μm is shown in Fig. 4.8. The inset shows the experimental setup. The collector terminal of the parasitic lateral n-p-n BJT is floating, and voltage is applied to the base and emitter terminals to investigate the characteristics of the B-E junction diode. As shown in Fig. 4.8, the B-E junction diode is in parallel with an inherent P-well resistance (R_well) of ~156Ω. Because the reverse-bias saturation current of B-E junction diode is quite small and omissible, the *I-V* data of negative VBE is fit linearly to define the equivalent P_well resistance. The B-E junction diode does not dominate the *I-V* characteristics until the base-to-emitter voltage (VBE) is larger than 0.9V. That is, the voltage drop across the effective P-well resistance must be ~0.9V to turn the parasitic lateral BJT 'on' by forward biasing the base-to-emitter junction.

The relation between the current gain of parasitic lateral n-p-n BJT in the ESP_stNMOS

structure (W = 480μm) and the collector current under the measured conditions of VCE = 3.3V and VBE = 0 - 1.4V is shown in Fig. 4.9(a). The base current I_B is calculated as equation (1). The current gain is defined as the differential value of I_C to I_B. The maximum current gain is 3.4 at IC of 4mA. Fig. 4.9(b) shows the relation between the current gain and the substrate potential VBE. The maximum current gain is 3.4 at VBE=1V. The base-to-emitter voltage must be greater than 0.8V for the current gain of the parasitic lateral n-p-n BJT to be greater than unity, which is the key factor of effective conduction of parasitic lateral n-p-n BJT.

4.3.2 Substrate Potential of ESP_stNMOS

To observe the substrate potential of ESP_stNMOS under ESD-like voltage stress, voltage pulses with period of 100ns and rise/fall time of 5ns generated by *HP8110A* are applied to the drain terminal of ESP_stNMOS with channel width of 480μm. An oscilloscope is used to observe the voltage pulse provided by *HP8110A*, the clamped voltage at drain, and the corresponding substrate potential of ESP_stNMOS.

Fig. 4.10(a) shows the waveforms of the applied 0-to-5V voltage pulse at drain terminal by *HP8110A*. Fig. 4.10(b) and (c) show the clamped voltage at drain and the corresponding substrate potential, respectively. Because the applied voltage at drain is smaller than the trigger voltage of parasitic BJT, the waveform at drain (Fig. 4.10(b)) is approximately the same as the input waveform (Fig. 4.10(a)), and the substrate potential is only 20mV. Fig. 4.11 and Fig. 4.12 show the waveforms of input voltage, clamped voltage at drain, and substrate potential under the applied 0-to-8.5V voltage pulse and 0-to-14V voltage pulse, respectively. From Fig. 4.11(b) and Fig. 4.12(b), it is shown that for input voltage larger than the trigger voltage, the parasitic BJT is turned on and thus the drain voltage would be clamped to the snapback holding voltage of parasitic BJT, which is about 5V. The substrate potential is about 0.7V and 0.95V under the applied 0-to-8.5V voltage pulse and 0-to-14V voltage pulse at drain, respectively.

Fig. 4. 13 shows the relations among the substrate potential, the clamped voltage at drain and the magnitude of the applied voltage pulse at drain. It is shown that the magnitude of the applied pulse must be greater than 8V for the parasitic BJT to be turned on, and the corresponding substrate potential is 0.6V. The substrate potential is increased rapidly before the parasitic BJT is turned on, while increased slowly after the parasitic BJT is turned on. The experimental results show that the voltage of the substrate-nodes of ESP_stNMOS can be elevated uniformly under ESD-like voltage stress.

4.3.3 TLP Measurement Results

To investigate the turn-on behavior of the stacked-NMOS device during high ESD current stress, TLP generator with a pulse width of 100ns is used to measure the second breakdown current (It2) of the device. Fig. 4.14 shows the TLP-measured *I-V* curves and the corresponding leakage currents of traditional stacked-NMOS under different channel width. The leakage currents are measured under VDS (voltage drop between the drain of top NMOS and the source of bottom NMOS) of 3.3V and VDD of 1.8V. The dependence of It2 per unit channel width on device total channel width for unit finger width of 60μm is shown in Fig. 4.15. As shown in Fig. 4.15, the It2 per unit channel width of traditional stacked-NMOS decreases as the device total channel width (or the number of fingers) increases. The It2 of traditional stacked-NMOS cannot increase linearly with channel width, which is due to the non-uniform turn-on issue among the multiple fingers of large-sized stacked-NMOS.

Fig. 4.16(a) shows the TLP *I-V* curves of traditional stNMOS and ESP_stNMOS under device channel width of 480μm. As shown in Fig. 4.16(a), the It2 of ESP_stNMOS is slightly larger than that of traditional stNMOS. Besides, the turn-on resistance (Ron) of ESP_stNMOS is 0.9Ω smaller than that of traditional stNMOS, which is beneficial for ESD protection circuits. The smaller Ron implies that the ESP_stNMOS is turned on more uniformly. Fig. 4.16(b) shows the enlarged view of Fig. 4.16(a) around snapback region of the devices. The

snapback holding voltage (Vh) of ESP_stNMOS is about 0.1V lower than that of the traditional stNMOS. The above experimental results show that the equal-substrate-potential technique can lead to higher It2, lower turn-on resistance and holding voltage for stacked-NMOS device.

4.3.4 ESD Robustness

The ZapMaster is used to verify the HBM and MM ESD robustness of the devices. In these ESD verifications, the devices are tested under the positive-to-VSS ESD stress, and the failure criterion is defined as the measured voltage at the current level of 1μA shifted 30% from its original value. The comparison of the ESD levels between the traditional stNMOS and the ESP_stNMOS is shown in Fig. 4.17. In Fig. 4.17, under the same device dimension (channel width of 480μm), the HBM ESD level of the ESP_stNMOS is larger than that of traditional stNMOS, and the result is consistent with the TLP measurement results.

The MM ESD pulse has faster rise time (~10ns) and ringing waveform, and thus the MM ESD level of a semiconductor device is generally 8~12 times smaller than its HBM ESD level. In the equal-substrate-potential stNMOS, it takes time to equalize the substrate potential among multi-finger, and thus the turn on speed of ESP_stNMOS is not quick enough to response to the MM ESD pulse. Therefore, the MM ESD level of ESP_stNMOS is kept the same as that of traditional stNMOS.

4.4 CONCLUSION

To improve the turn-on uniformity of multi-finger stacked NMOS, a novel equal-substrate-potential technique has been designed and verified in a 0.18-μm CMOS process. The device characteristics of SST_GGNMOS have been verified in the silicon chip and the experimental results have confirmed that the substrate potential of ESP_stNMOS can be elevated uniformly under ESD-like stress. The TLP *I-V* measurement results show that the ESP_stNMOS has smaller turn-on resistance and snapback holding voltage, which is beneficial for ESD protection circuits. The HBM ESD level of stacked NMOS is improved through equal-substrate-potential technique, while MM ESD level does not change. The testkey in this thesis is stand-alone devices, if taking the ESD design window (holding voltage of device must be larger than power supply voltage and voltage drop across ESD protection device must be smaller than the internal gate-oxide breakdown voltage) into consideration, the effectiveness of equal-substrate-potential technique should be more evident.

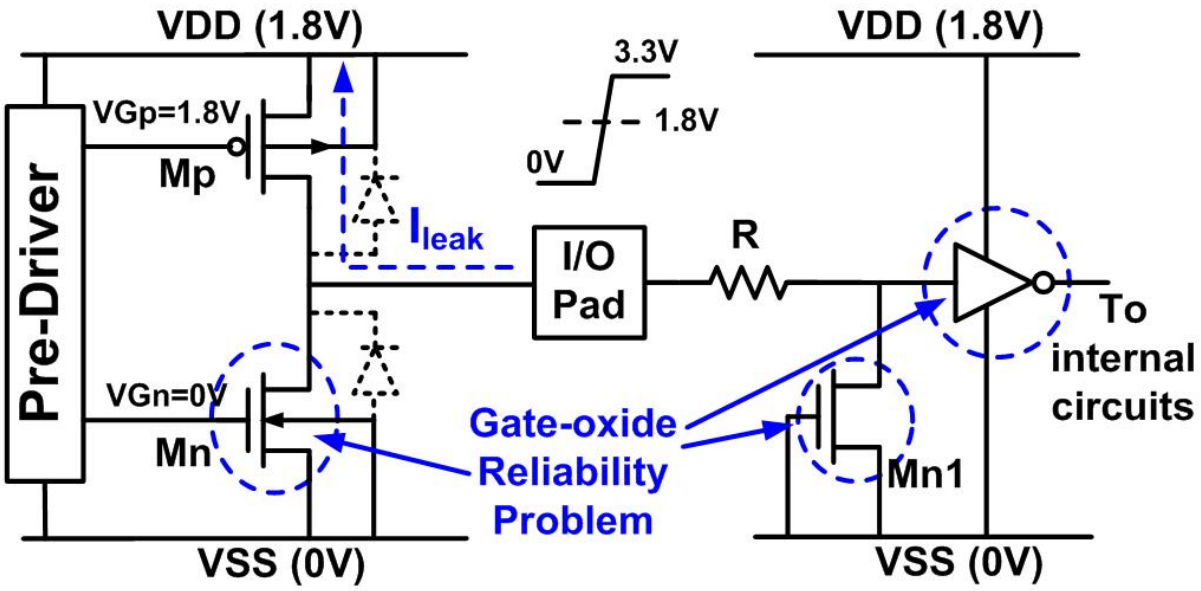


Fig. 4.1 Illustrations of the problems that would arise when the traditional CMOS I/O buffer used as high-voltage-tolerant I/O buffer.

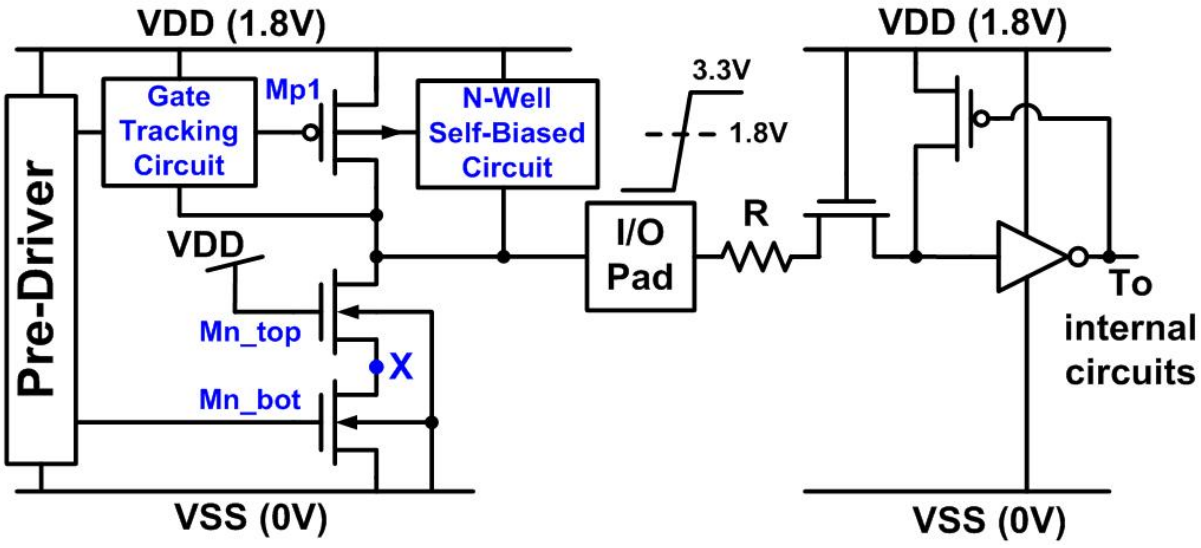


Fig. 4.2 Typical circuit diagram for high-voltage-tolerant I/O circuits with the stacked-NMOS structure. The N-well self-biased circuit and the gate tracking circuit is used to eliminate the leakage current paths through PMOS.

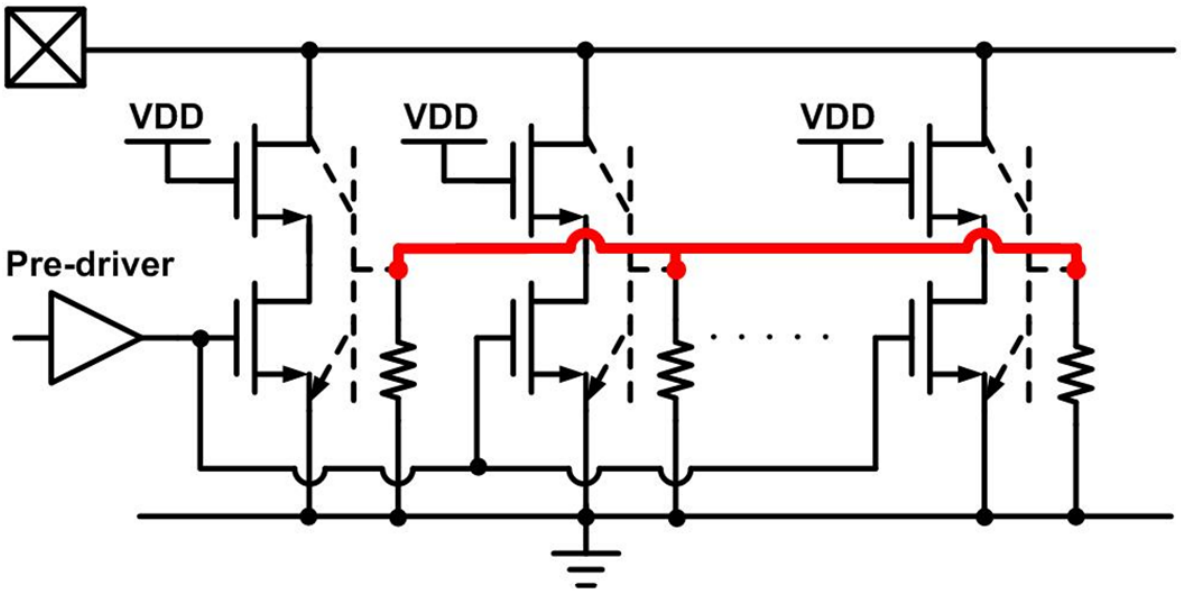


Fig. 4.3 The equivalent circuit of equal-substrate-potential stacked-NMOS used as self-protection device.

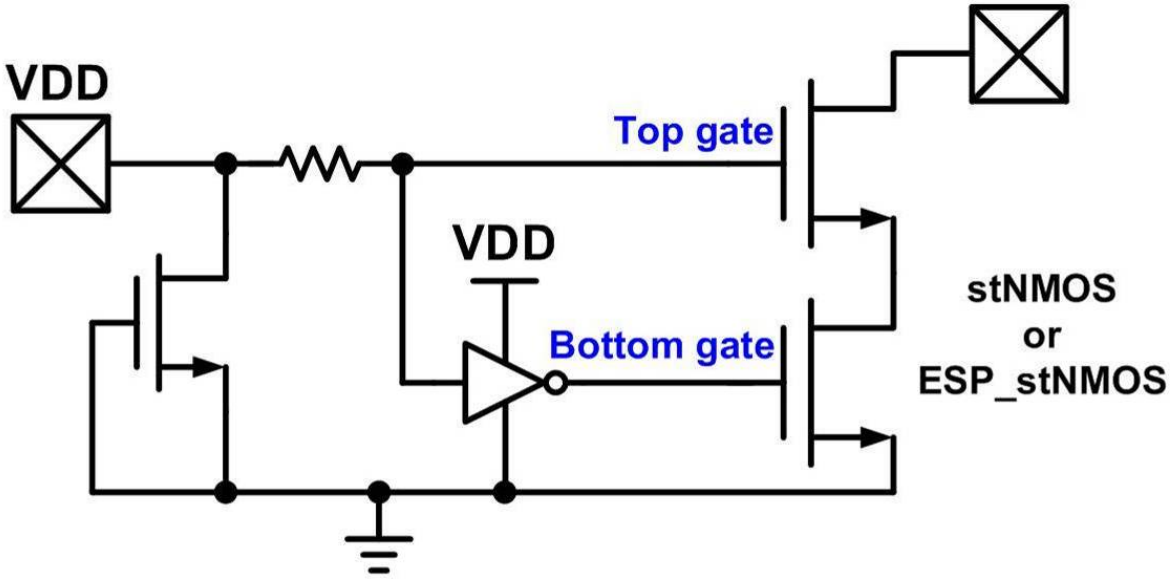
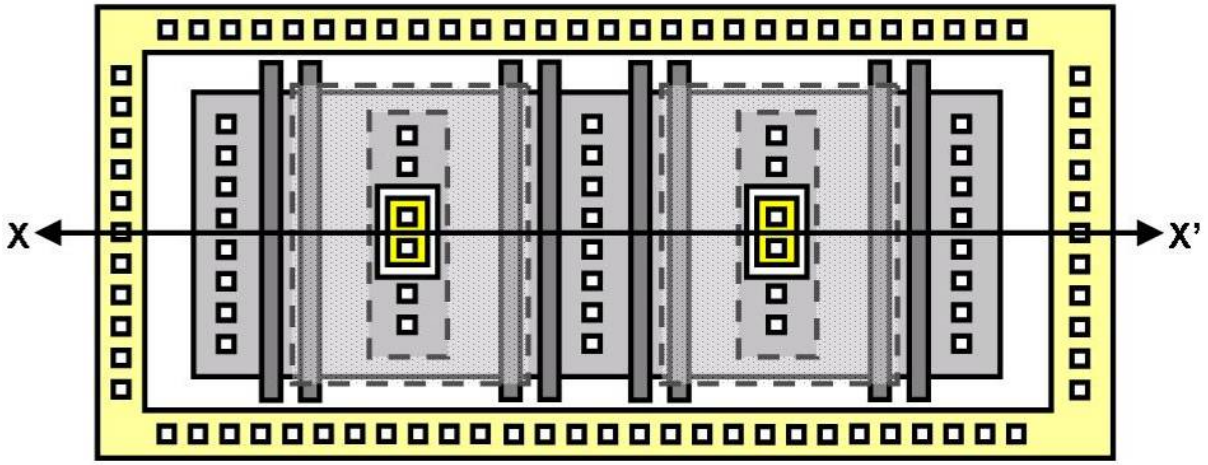
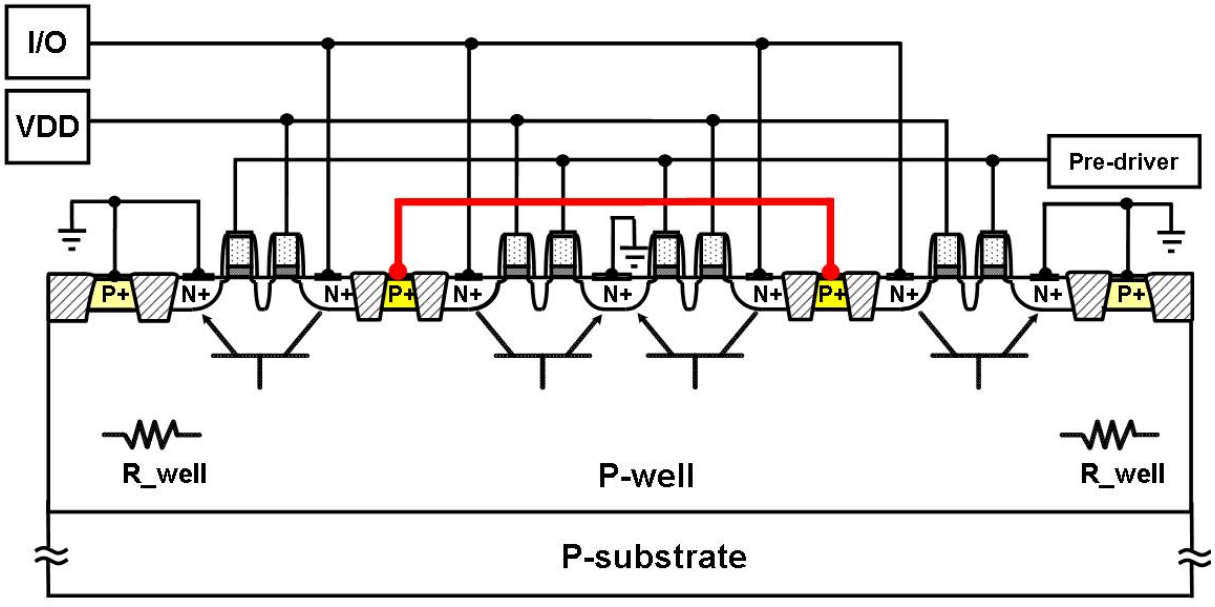


Fig. 4.4 The testkey for both stNMOS and SST_stNMOS, the top gate is connected to VDD pad through a resistor, and a gate-grounded NMOS is used to protect the top gate. The bottom gate is biased through an inverter whose input signal is VDD.



(a)



(b)

Fig. 4.5 The layout top view and (b) the X-X' cross-sectional view of the ESP_stNMOS. The P+ diffusion regions inserted at the drain of each finger as the substrate-nodes are connected together by metal line. The top gates are connected to VDD, and the bottom gates are connected to pre-driver.

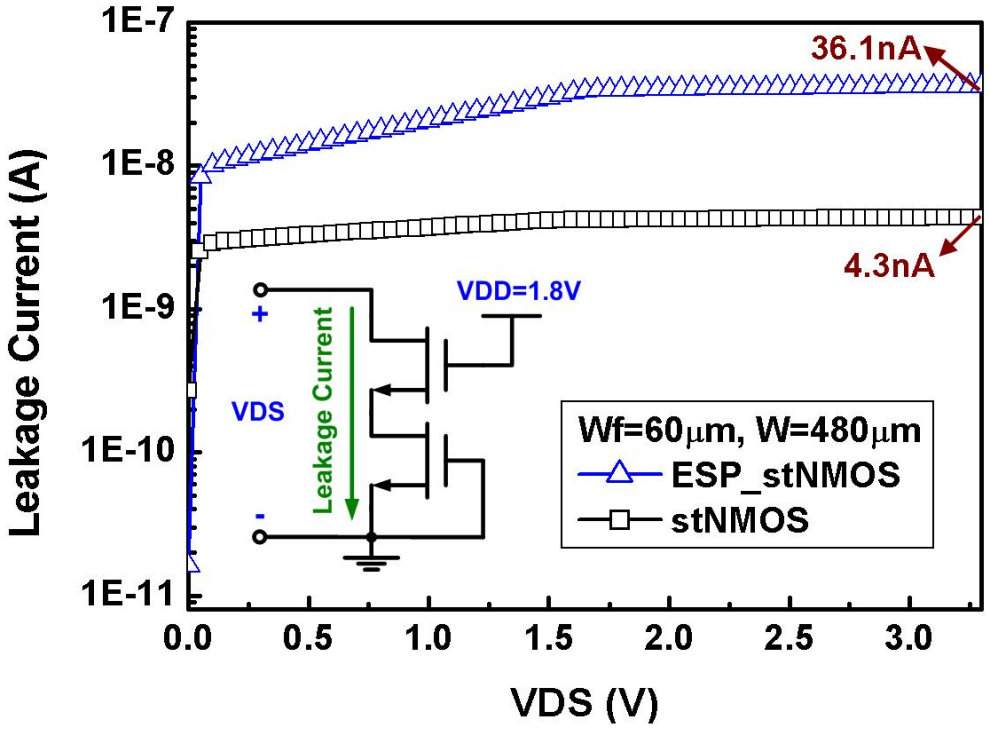


Fig. 4.6 The dc leakage current of traditional stNMOS and ESP_stNMOS under channel width of 480μm at a room temperature of 25ºC.

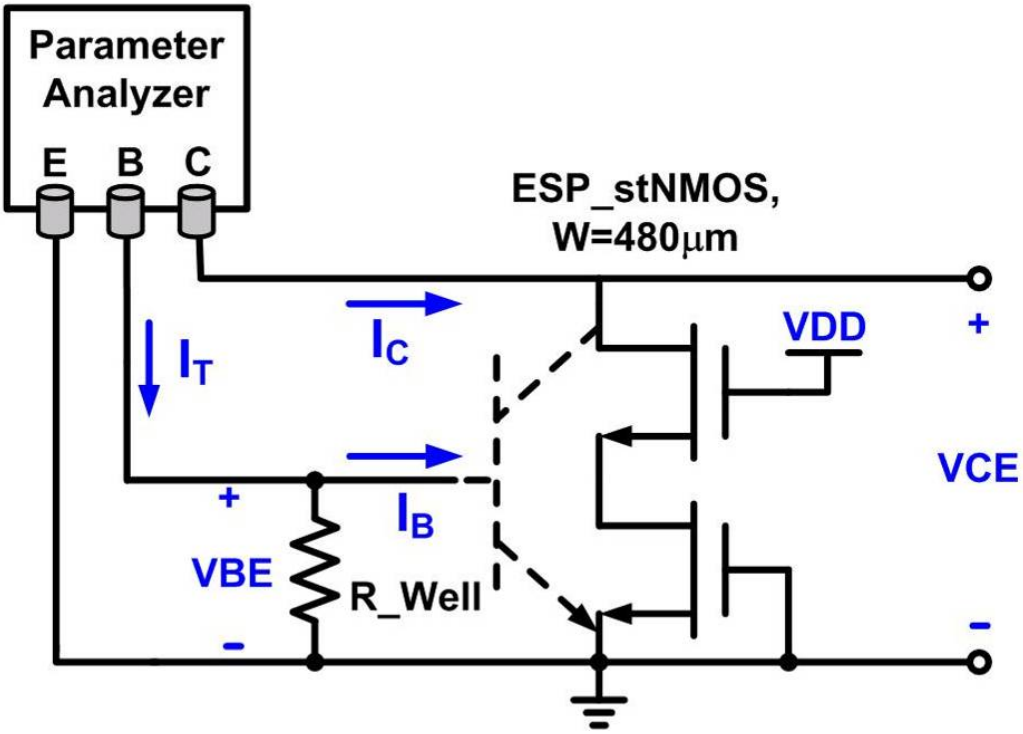


Fig. 4.7 The experimental setup and definitions of the current and voltage components to measure the dc characteristics of the ESP_stNMOS with channel width of 480μm.

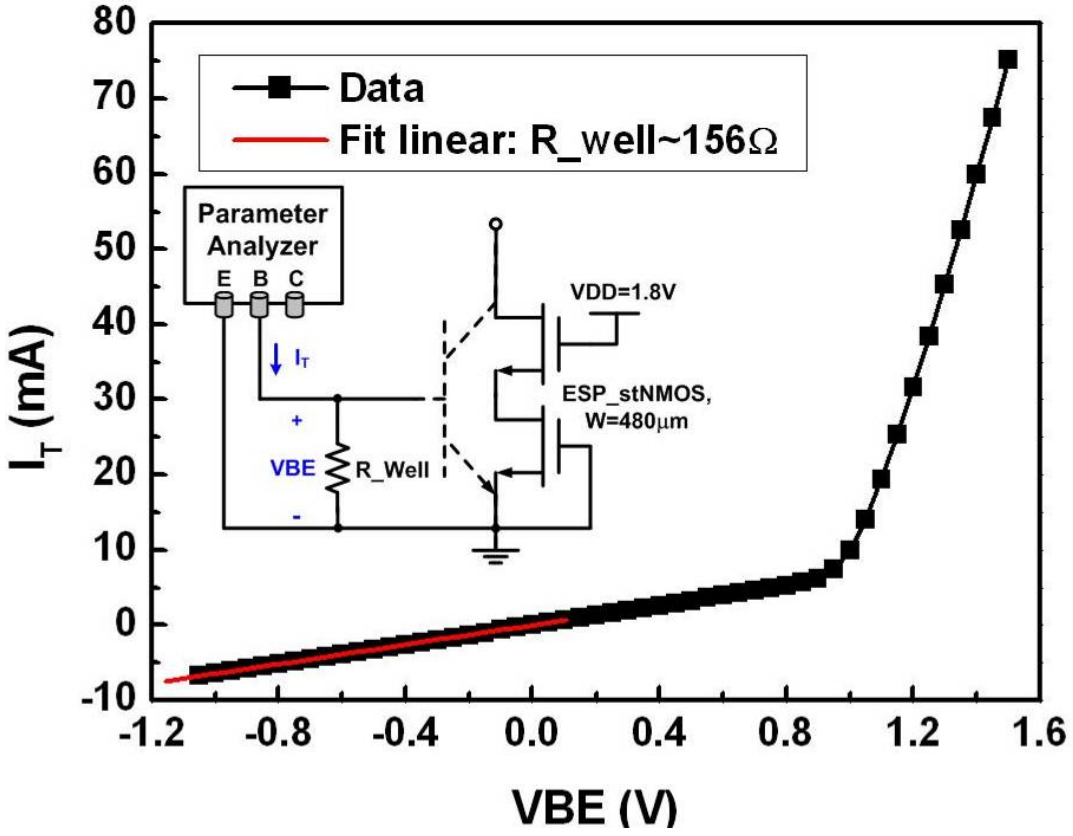
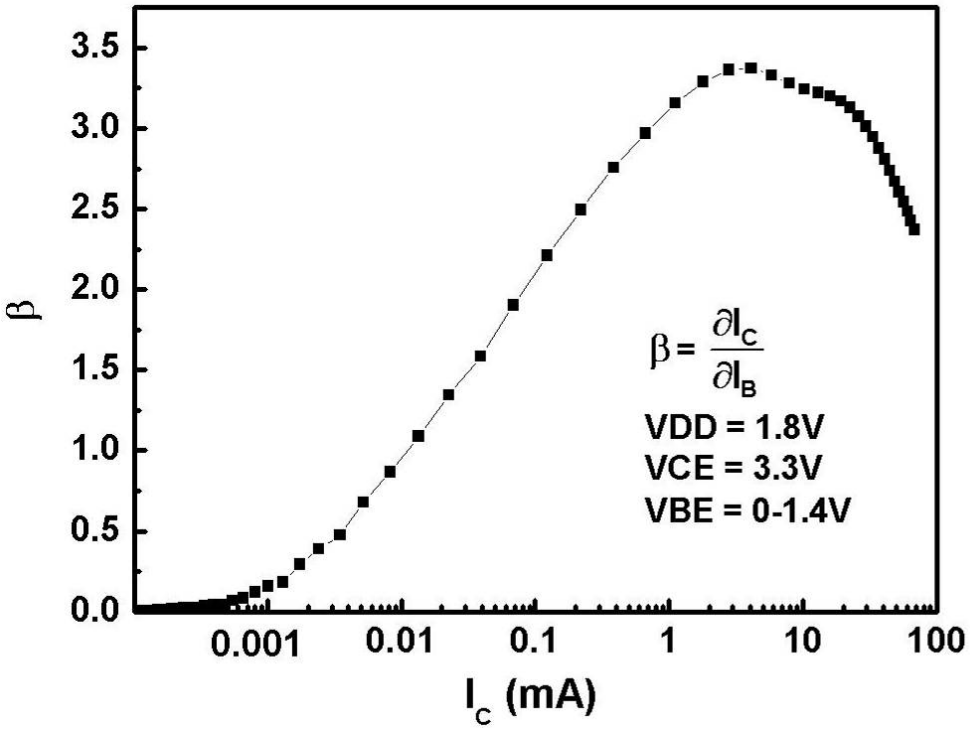
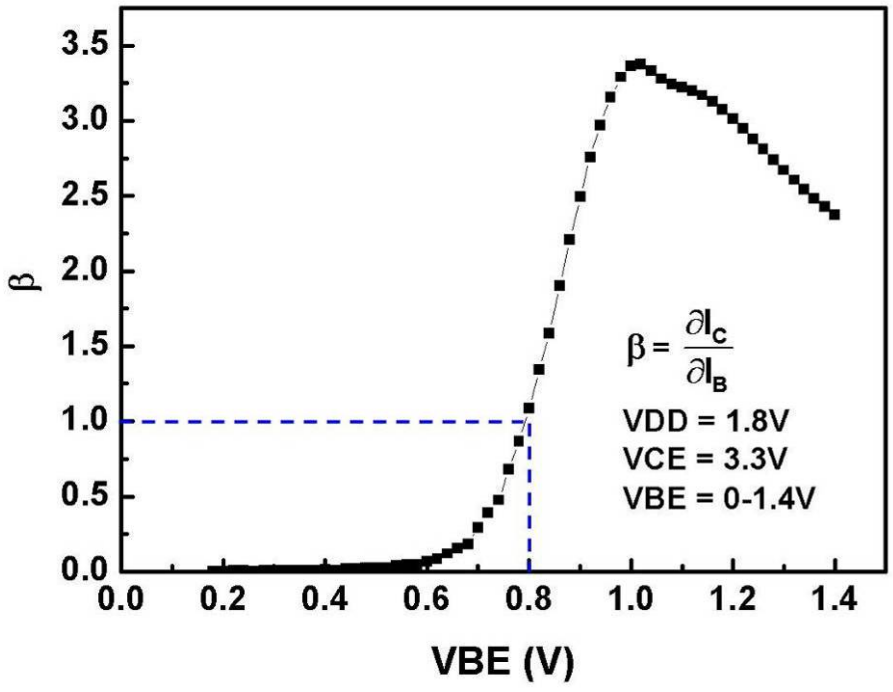


Fig. 4.8 The measured base-to-emitter dc I-V curve of the ESP_stNMOS with channel width of 480μm in an open-collector configuration.

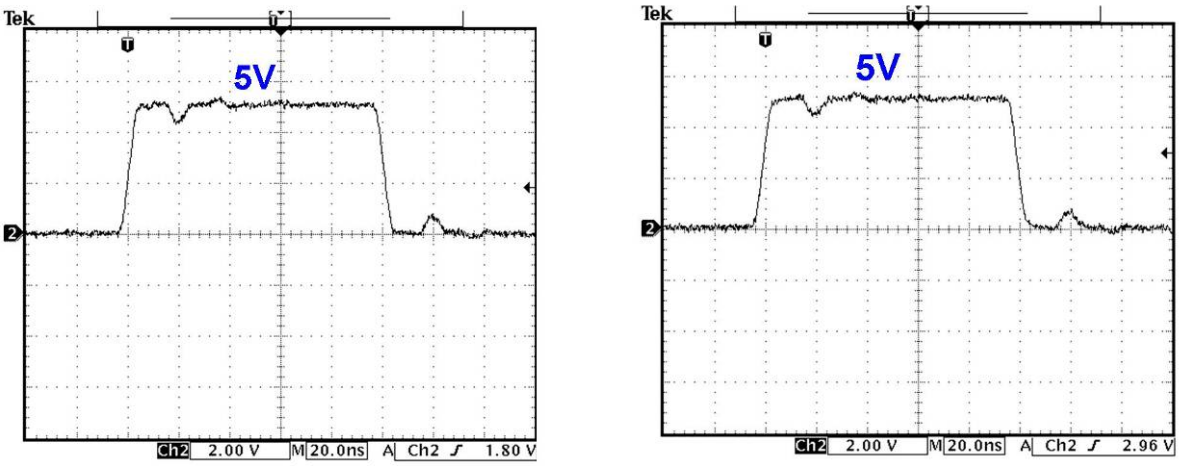


(a)

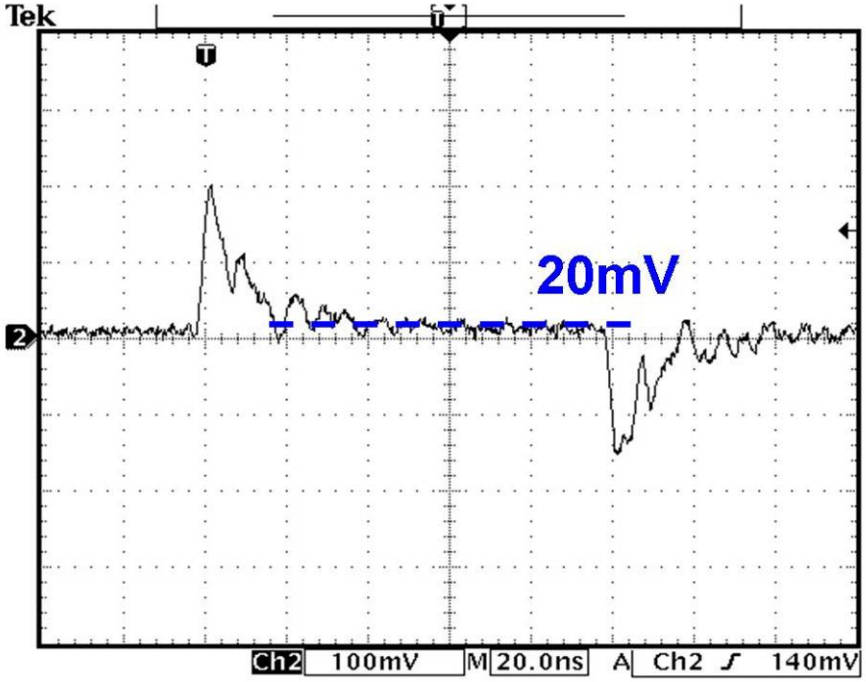


(b)

Fig. 4.9 The dependences of the current gain of the parasitic lateral n-p-n bipolar transistor inherent in the ESP_stNMOS on (a) the collector current, and (b) the base-to-emitter voltage under VCE of 3.3V and VBE from 0 to 1.5V.

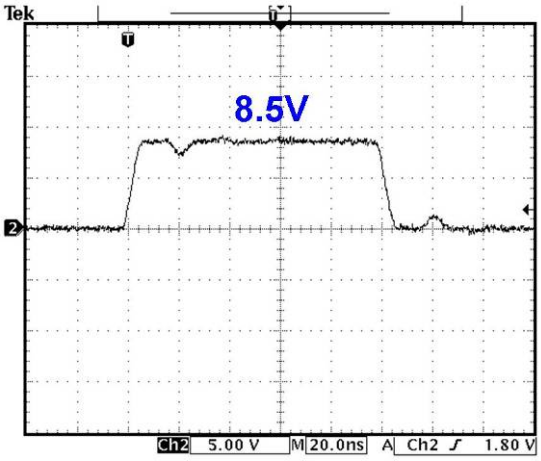


(a) (b)

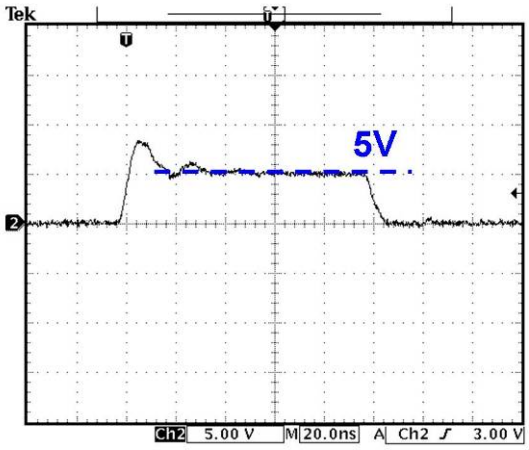


(c)

Fig. 4.10 The waveforms of (a) the applied 0-to-5V voltage pulse at drain terminal by *HP8110A*, (b) the clamped voltage at drain, and (c) the corresponding substrate potential.



(a)



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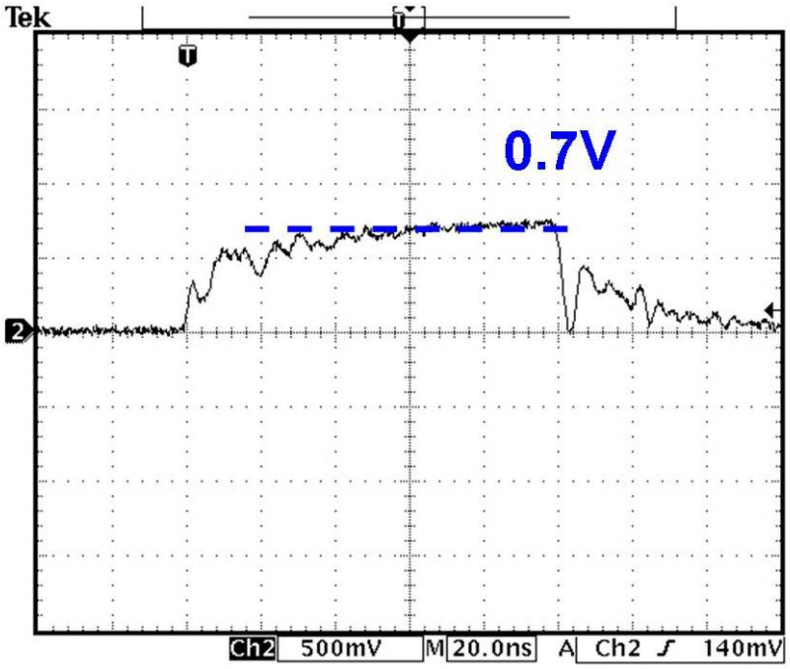
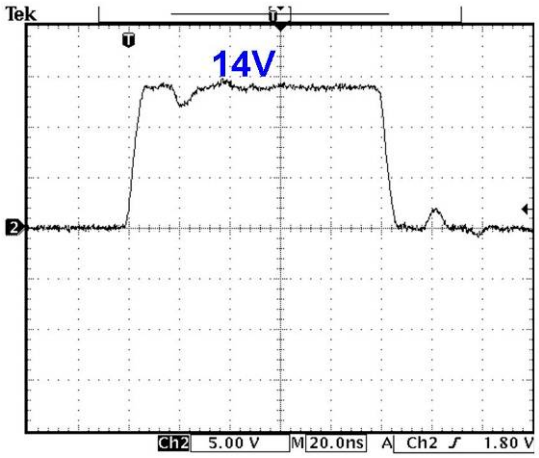
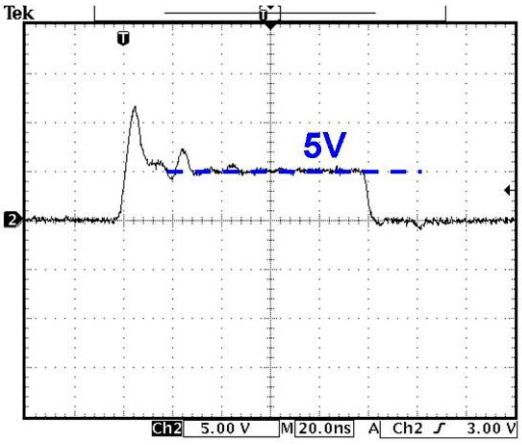


(c)

Fig. 4.11 The waveforms of (a) the applied 0-to-8.5V voltage pulse at drain terminal by *HP8110A*, (b) the clamped voltage at drain, and (c) the corresponding substrate potential.



(a)



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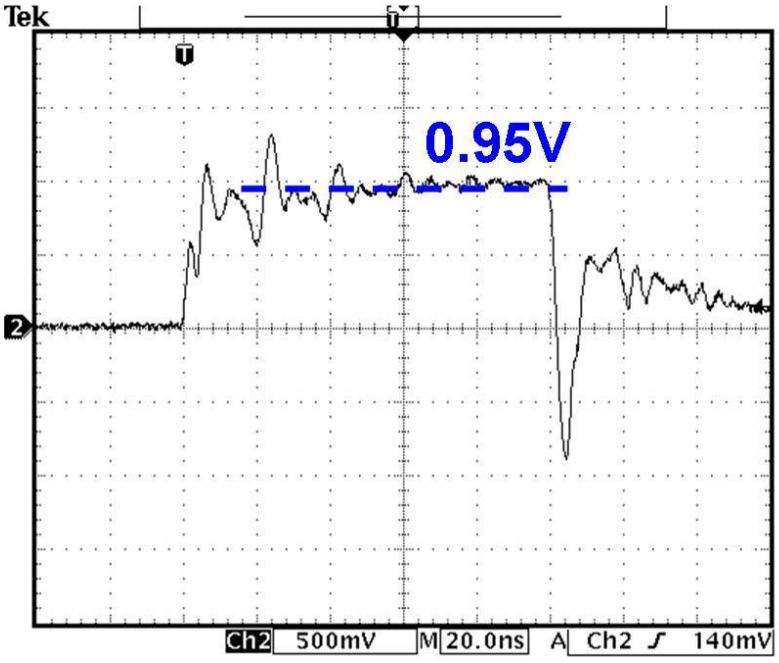


(c)

Fig. 4.12 The waveforms of (a) the applied 0-to-14V voltage pulse at drain terminal by *HP8110A*, (b) the clamped voltage at drain, and (c) the corresponding substrate potential.

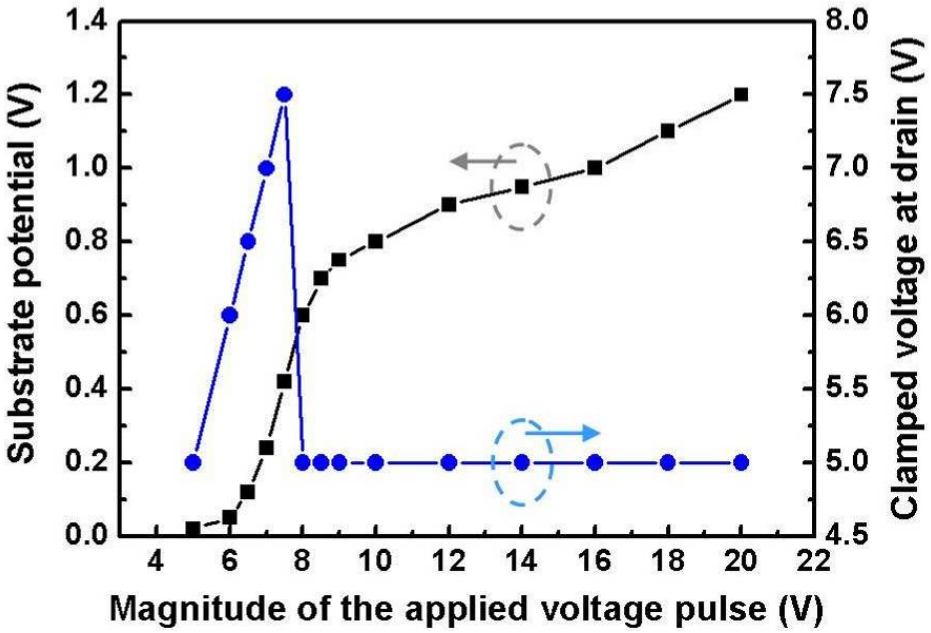


Fig. 4. 13 The relations among the substrate potential, the clamped voltage at drain, and the magnitude of the applied voltage pulse at drain.

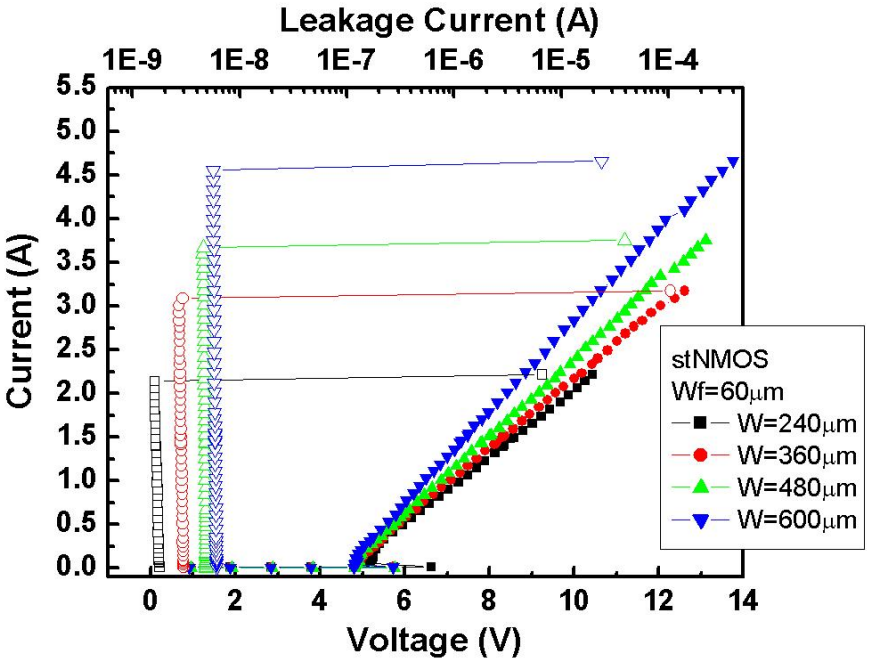


Fig. 4.14 The TLP-measured *I-V* curves of the traditional stNMOS under different channel widths, including the corresponding leakage currents under the drain voltage bias of 3.3V and VDD bias of 1.8V.

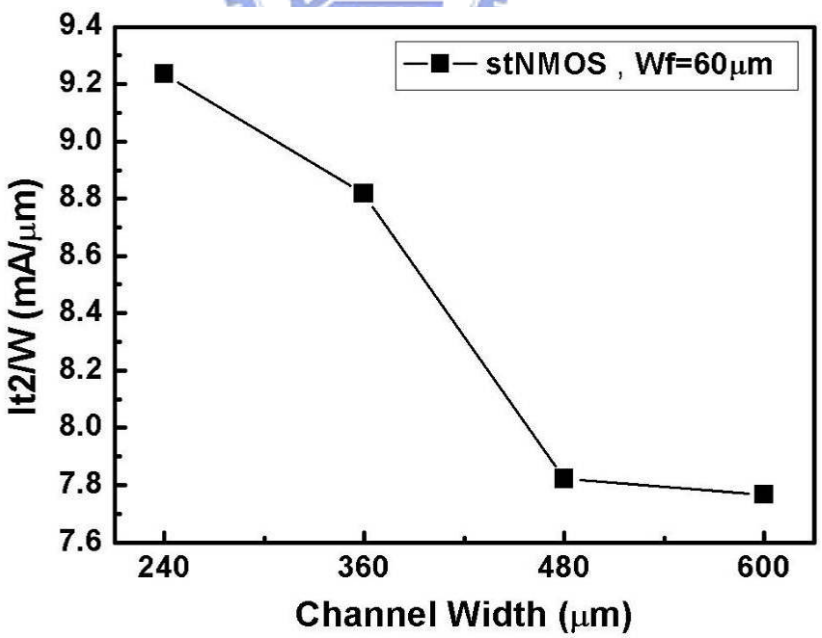
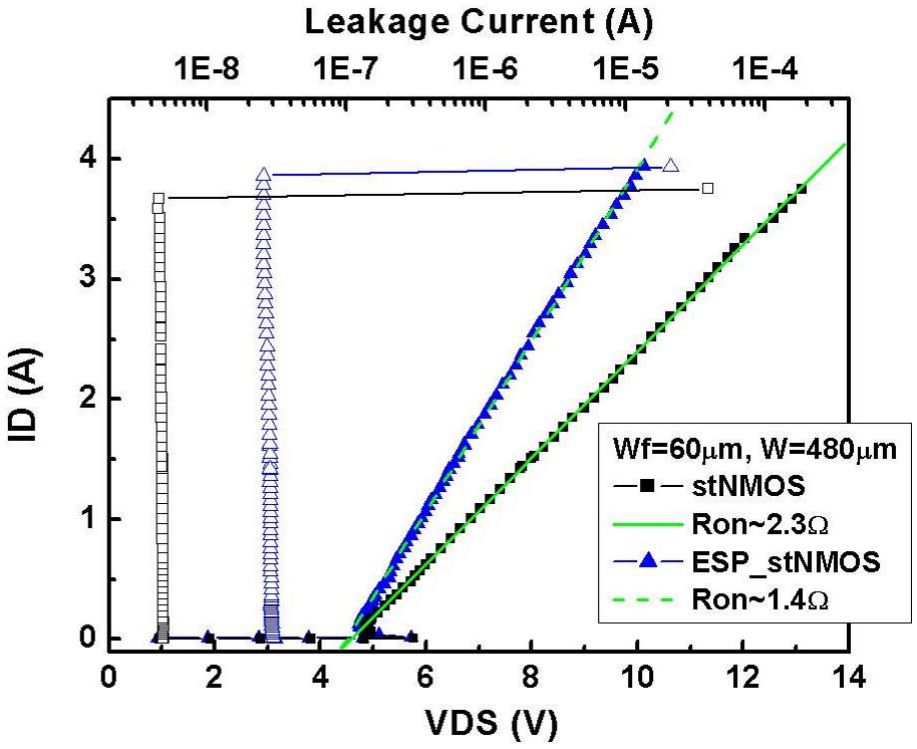
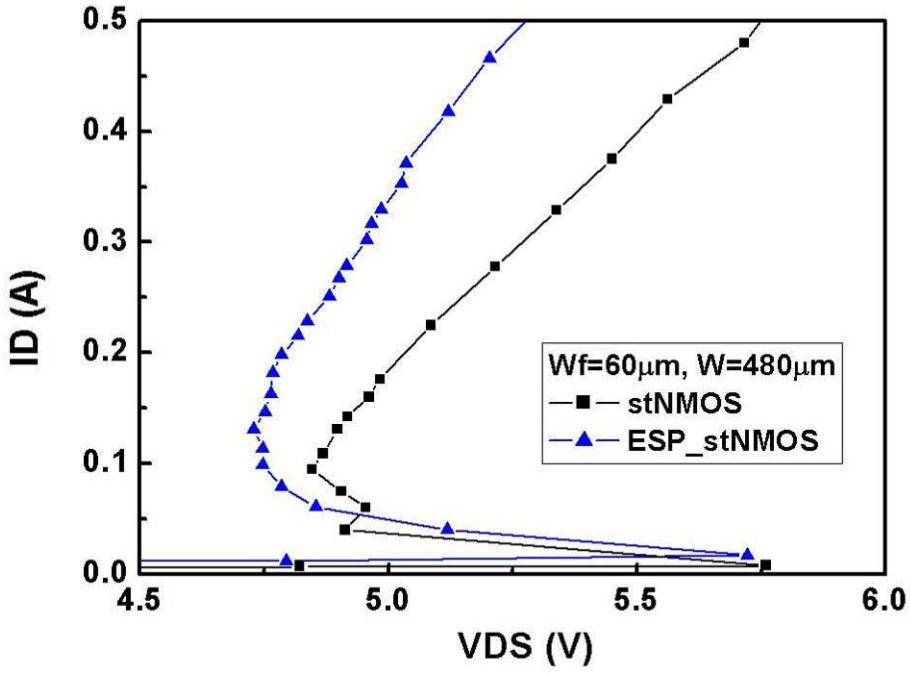


Fig. 4.15 The relation between the It2 per micron and channel width for the traditional stNMOS.



(a)



(b)

Fig. 4.16 (a) The TLP-measured *I-V* curves of ESP_stNMOS and the traditional stNMOS for device channel width of 480μm, and (b) the enlarged view of the TLP-measured *I-V* curves around the snapback region.

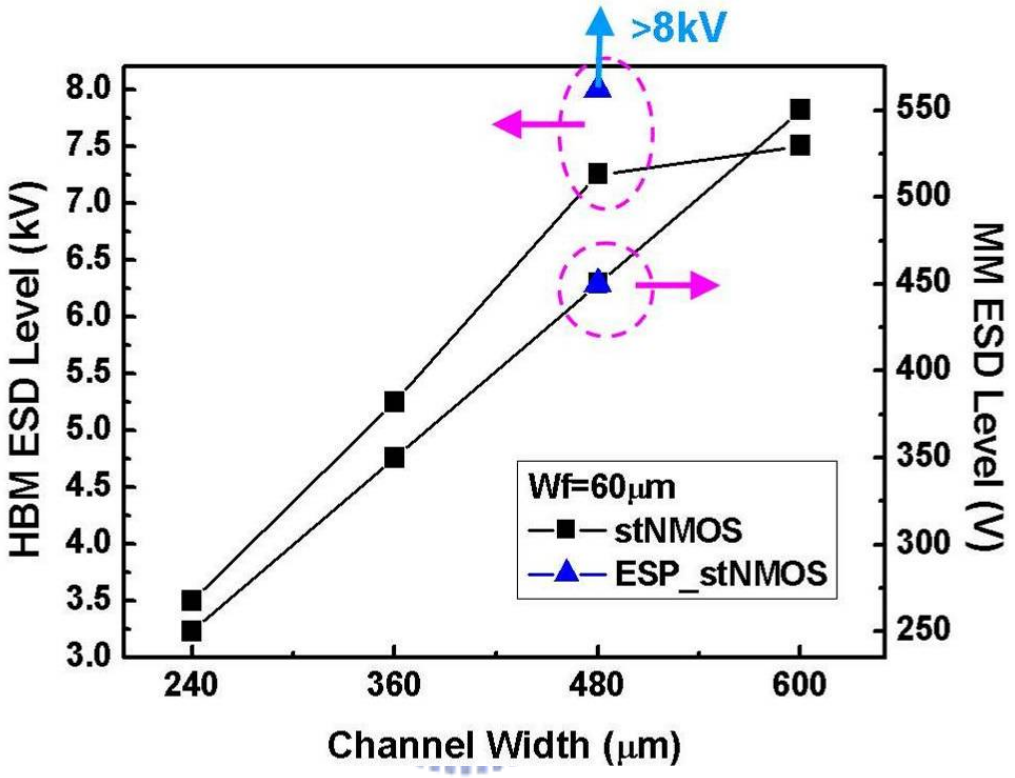


Fig. 4.17 The relations between the ESD levels and channel widths for traditional stNMOS and the proposed ESP_stNMOS.

Chapter 5

Conclusion and Future Work

5.1 CONCLUSION

In this thesis, two designs to enhance the turn-on uniformity of multi-finger NMOS has been proposed and verified in silicon testchip. In the first design, the self-substrate-triggered technique has been proposed to improve the turn-on uniformity of gate-ground NMOS (GGNMOS). The design is fabricated and verified in a 0.13-μm CMOS process. The experimental results have shown that the self-substrate-triggered can effectively enhance the ESD robustness and turn-on uniformity of gate-grounded NMOS without increasing device layout area.

The second design in this thesis, the equal-substrate-potential technique to enhance the ESD robustness of stacked NMOS, is verified in a 0.18-μm CMOS process. The experimental results have shown that the equal-substrate-potential can reduce the turn-on resistance of stacked NMOS, which is a superior characteristic for ESD protection circuit. The HBM ESD level can be improved through this equal-substrate-potential technique, but the MM ESD level does not change. It is concluded that the equal-substrate-potential technique can reduce the turn-on resistance of stacked-NMOS, and taking the ESD design window into consideration, the effectiveness of equal-substrate-potential technique should be more evident.

5.2 FUTURE WORK

The self-substrate-triggered technique can be applied to stacked-NMOS structure, and the equal-substrate-potential technique can also be applied to gate-grounded NMOS structure to compare the efficacy between these two designs. The side effect for the proposed two designs is the increase of dc leakage currents, and further design to eliminate such side effect is required. The equal-substrate-potential stacked-NMOS needs more testkeys with different device size to further verify the effectiveness of the design. As shown in Fig. 5.1, the layout parameters including the RPO width (X, Y) and the size of substrate-node (a, b) should be investigated to see their impacts on the equal-substrate-potential design. The equal-substrate-potential technique can reduce the turn-on resistance of stacked-NMOS devices, which is attractive to protect the ultra-thin gate-oxide in advanced technology. Therefore it is desirable to further verify the equal-substrate-potential technique in nano-scale CMOS technology.

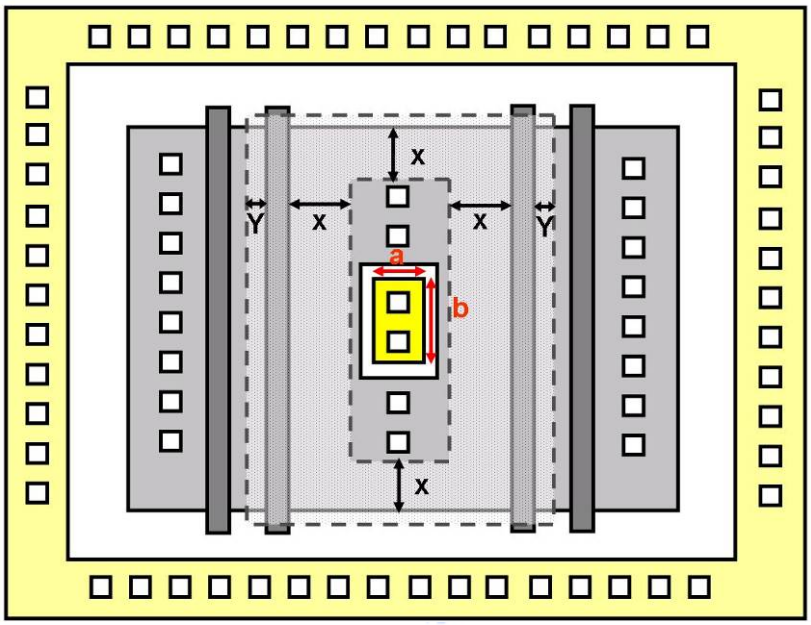


Fig. 5.1 The layout parameters that should be investigated in the equal-substrate-potential stacked-NMOS.

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