國立交通大學

電子工程學系　電子研究所

碩士論文

高性能金屬閘極多晶矽薄膜電晶體之研究

Studies Of High Performance Metal Gate Low Temperature Poly-Silicon Thin Film Transistor

研究生: 沈香谷

指導教授: 荊鳳德 博士

中華民國九十五年五月

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摘要

本論文將金屬閘極整合到使用高介電係數介電質的多晶矽薄膜電晶體上。我們選用鐿(擁有最低功函數的鑭系金屬,約 2.6 電子伏特)在 NMOS 上。我們得到了良好的薄膜電晶體的特性，例如，低臨界電壓、高驅動電流、低次臨界斜率、高閘極介電層崩潰電壓、以及很好的開關電流比例。這些良好的特性是因為擁有低功函數的鐿可以成功的將臨界電壓降低，還有高介電係數介電層閘極可以得到較薄的等效氧化層厚度。而本論文之研究不是用特殊的成晶步驟，我們只用了爐管來成晶就可以達到。

Studies OF High Performance Metal Gate Low Temperature Poly-Silicon Thin Film Transistor

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Department of Electronics Engineering & Institute of Electronics

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Abstract

We have integrated a Metal gate into Poly-Silicon (LTPS) thin-film transistors (TFTs) with high – κ gate dielectric. We use Ytterbium (Yb , has the lowest work-function in Lanthanide series metal ≒ 2.6 eV) for NMOS. We get good TFT performance in NMOS, such as a low threshold voltage, a high drive current, a low subthreshold slope, high gate–dielectric breakdown voltage, and a very good on/off current ratio. The good performance is related to the low work-function metal, Ytterbium, makes the threshold voltage lower successfully and small equivalent oxide thickness by high κ dielectric material. This was achieved without special crystallization steps, we only use furnace to crystallize.

Contents

Chapter 1 Introduction

Chapter 2 The Experimental Steps

Chapter 3 Result & Discussion

Figure Captions

Chapter 1 Introduction

Chapter 2 Experimental Steps

Chapter 3 Result & Discussion

Chapter 1

Introduction

1.1 Thin-Film Transistors

A transistor whose active, current-carrying layer is a thin film (usually a film of silicon), in contrast to MOSFETs, which are made on Silicon wafers and use the bulk-silicon as the active layer. In a flat-panel display, light must be able to pass through the substrate material to reach the viewer. Opaque silicon wafers obviously will not be suitable for these transmissive displays. Glass is the most commonly used starting substrate because it is highly transparent and is compatible with conventional semiconductor processing steps. Since glass is not a semiconductor like silicon, a thin film of silicon is deposited on top and the transistors are fabricated using this thin layer. Hence, the name "thin-film transistor."

1.2 Overview of Polycrystalline Silicon Thin-Film Transistors Technology

Polycrystalline silicon thin-film transistors (TFTs) have been investigated extensively for their use on the peripheral driving circuits in active matrix liquid crystal displays (AMLCDs) [1], high-density static random access memories (SRAMs) [2][3], linear image sensors [4], thermal printer heads [5], liquid crystal shutter arrays for printers [6], photodetector amplifier [7], and nonvolatile memories [8] ,etc.

Traditionally, AMLCDs were fabricated using hydrogentated amorphous silicon (α-Si:H) TFTs for the pixel switching devices [9]. The α-Si:H TFTs have many advantages, particularly its compatibility with low temperature process on large glass substrate and high off-state resistivity which result a low leakage current. However, the low electron field effect mobility in α-Si:H TFTs has limited the technology development for AMLCDs application. To integrate the switching elements with the driving circuits on the same substrate is very desirable not only to reduce the cost but also to improve the system performance. Therefore, poly-Si TFTs, which provide higher electron field effect mobility, have been developed as a substitute for α-Si:H TFTs. Besides, poly-Si TFTs have other advantages such as lower photocurrent, CMOS capability and better reliability [10], thus enables the integration of peripheral circuits as well as the active-matrix switching elements on the same substrate.

It should be noted that ‘Poly-Silicon’ covers a range of thin film materials, which vary in the methods of preparation, grain size and nature, distribution of intragranular and bulk defects, and surface roughness. Thus, the properties of any particular film will be dependent on these parameters, which have therefore been the subject of extensive studies to optimize key TFTs parameters such as off-current, on-current, subthreshold swing and mobility [11]. The performance of Poly-Silicon TFTs is strongly influenced by grain boundaries and intragranular defects. In order to enhance TFTs electrical characteristics, several techniques which are used to increase the grain sizes of poly-Si films have been proposed. The methods for recrystallization of α-Si to poly-Si at glass-compatible temperatures are the key technology for fabricating low-temperature process (LTP) Poly-Silicon TFTs on glass. It was reported that the α-Si film can be recrystallized by several techniques, such as: solid-phase crystallization (SPC) [12], excimer laser annealing (ELA) [13]-[15], metal-induce lateral crystallization (MILC) [16]-[18], rapid thermal annealing (RTA) [19], and microwave crystallization [20] to obtain larger grain sizes of poly-Si for high mobility.

The presence of grain-boundary and intragranular defects in the active region of Poly-Silicon TFTs places a major limitation on the devices' performance. The dangling bond midgap states affect threshold voltage and subthreshold swing, while the strain bond tail states influence leakage current and field-effect mobility [21]. The well-established method for reducing these trap states is hydrogenation in hydrogen plasma at 300℃ [21]-[23]. The atomic hydrogen, which has a higher diffusivity, diffuses rapidly into the Poly-Silicon film and then passivates defects. It was found that the dangling bonds have a faster response to bond with hydrogen, while the strain-bonds response slower. Only when the hydrogen concentration is so large as to fill both the midgap states and the tail states, a significant fraction of the tail states will be passivated. Although hydrogenation is successfully used to improve the performance of Poly-Silicon TFTs, it has been reported that TFTs exposed to hydrogen plasma suffer a low hot-carrier endurance and a low thermal stability [24]. In this study, we utilized ammonia (NH_3) plasma to replace the conventional hydrogen (H_2) plasma treatment for passivating defects of LTP Poly-Silicon TFTs. It is shown that NH_3-plasma passivation can improve enormously the TFT's performances, particularly in carrier mobility and reliability. These improvements were attributed to not only the hydrogen passivation of the defect states, but also the nitrogen pile-up at gate dielectric/Poly-Silicon interface and the strong Si-N bond formation to terminate the dangling bonds at the grain boundaries of the Poly-Silicon films. Furthermore, the gate oxide leakage current significantly decreases and the oxide breakdown voltage slightly increases after applying NH_3 plasma treatment.

1.3 Poly-Silicon Recrystallization Methods

The performance of Poly-Silicon TFTs is strongly influenced by grain boundaries and intragranular defects. In order to enhance TFTs characteristics, several techniques are used to increase the grain sizes of Poly-Silicon films have been proposed.

1.3.1 Solid-Phase Crystallization Method

One of prominent methods is the crystallization of amorphous silicon films deposited by low-pressure chemical vapor deposition (LPCVD). The grain sizes obtained by solid-phase crystallization of α-Si films is larger by several times and has smoother surface morphology than that of as-deposited poly-Si films. Traditionally, the silicon deposition in LPCVD reactors is performed at a temperature around 550℃ using SiH_4 gas, followed by SPC at 600℃. Recently, the use of disilane (Si_2H_6) as gas precursor in lieu of SiH_4 is being actively studied [25]. It was reported that in order to achieve a large grain size, the deposition rate of the as-deposition and annealing temperature must be low. Under such conditions, the nucleation rate during annealing is low and therefore grains can grow to a large size.

The crystallized silicon film structure is believed to related to the structural disorder of the initially deposited material. It has been shown previously that by increasing the disorder of silicon network, a significant enlargement of the grain size of the crystallized silicon can be achieved. The disorder of the underlying silicon network can be in turn increased with using low deposition temperature and high deposition rate. Disilane has been shown to result in high deposition rate compared to SiH_4 even at temperature below 470℃. After SPC, larger grain Poly-Silicon films can be obtained at low temperature below 600℃ with disilane as gas precursor to silane.

1.3.2 Excimer Laser Annealing Crystallization Method

Pulsed excimer laser annealing is also being investigated as an alternative crystallization technique to replace furnace annealing [13]-[15]. For fabricating high performance Poly-Silicon TFTs on a glass substrate, excimer laser crystallization method is very promising for the following reasons. First, it is a low-temperature process introduced no serious thermal shrinkage of the glass substrate caused by the effects of the short pulse and large absorption coefficient of silicon in the UV light regime. Secondly, it can crystallize the film selectively by partially irradiating the film surface, so both Poly-Silicon TFTs and amorphous Silicon TFTs can be formed on the same substrate. The laser process heats the thin silicon film to the melting point on a short time scale (tens of nanoseconds) that allows the film to melt and recrystallized without significantly heating the glass substrate. Since this process achieves higher annealing temperatures than a conventional furnace annealing, significantly higher-quality Poly-Silicon films can be obtained.

1.3.3 Metal-Induce Lateral Crystallization Method

Recently, the metal-induced lateral crystallization (MILC) process has been studied widely for polycrystalline silicon thin film transistor applications. Compared with the conventional solid-phase crystallization (SPC) process [12] of amorphous silicon (α-Si), MILC process offers the advantages of lower annealing temperature (≦ 600℃) and better crystallization film. In addition, Poly-Silicon films crystallized by the MILC process can be used as the basis for developing the low cost integrated circuits on glass substrate. At present, nickel (Ni) [16]-[18] and palladium (Pd) have been used to induce lateral crystallization of α-Si:H film. Experimental annealing temperatures and MILC rates obtained for Ni and Pd are 500℃, 1.6μm/h, and 500℃, 10μm/h, respectively. However, the annealing temperature (≦ 500℃) is still too high for Poly-Silicon TFT devices to be fabricated on conventional glass substrate, and the low MILC rate, i.e. long annealing time, also increases the thermal budget in the Poly-Silicon TFT fabrication process. So, gold (Au) has been employed to induce lateral crystallization of α-Si:H film owing its lower eutectic temperature (363℃). The crystallization of Au/α-Si:H film is observed starting from annealing treatment at 175℃, which is a much lower crystallized temperature than for Ni and Pd (500℃). After the discovery of Au-MILC where microtwin-free Si grains are obtained, MILC also has been successfully applied to the low-temperature fabrication of high-mobility N-channel TFTs.

1.3.4 Rapid Thermal Annealing Crystallization Method

To obtain the Poly-Silicon crystalline phase, laser crystallization can be used with very good results [14], but the process is expensive and difficult to control. On the other hand, for similar results, furnace annealing requires lower temperature and is much simple, can be better checked, and is cheaper [19]. So, to achieve desirable material properties for the Poly-Silicon films, RTA has been used in this work, thermal crystallization of amorphous silicon. For the Si films annealed at 750℃ or higher, using RTA, the grain average sizes are reduced whereas the electron/hole mobility are increased. This indicates that the Poly-Silicon film electrical properties depend not only on the grain size, but also on the crystalline quality of the grains. Moreover, it appears that the large amount of crystalline defects remaining in the so-called “grains” of the films annealed at 600℃ (SPC) are partially annihilated when the films are annealed at higher temperatures. With regards to the TFTs electrical characteristics, the work suggests combining SPC and RTA steps to obtain TFTs with improved electrical performance.

1.4 Gate Dielectric Film Option

1.4.1 Original Gate oxide Growth Technology

In order to achieve low temperature process of high quality gate dielectric film, several methods for deposition of gate dielectric were investigated such as plasma-enhanced chemical vapor deposition (PECVD), electron cyclotron resonance (ECR) plasma thermal oxide, liquid phase deposited (LPD) oxide. PECVD system which has good step coverage, high deposition rate, low temperature process at 300℃. The PECVD widely used for the deposition of many kinds of films such as silicon dioxide (using TEOS+O_2 as the source gases), silicon nitride, oxide/nitride/oxide (ONO) stack films (in-situ deposition). The tetraethylorthosilicate (TEOS) can be decomposed below 300℃ by the enhancement effects of plasma or ozone. TEOS silicon dioxide films were demonstrated superior step coverage at low temperature. However, the deposited TEOS oxide has a higher leakage current, lower breakdown voltage, and higher instability than thermal oxide due to the low integrity and high interface trapped charges. The deposited oxide also has the rough oxide/Poly-Silicon interface due to the localized enhancement of oxidant diffusion through the grain boundaries, which leads to higher local electric field. Recently, N_2O plasma oxide was investigated for gate dielectric of Poly-Silicon TFTs due to the combined effects of nitrogen-plasma and oxygen-plasma passivation and smoother interface.

1.4.2 Reason For Using $LaAlO_3$ For Gate Dielectric Film

To prevent from short channel effect in high speed transistors, thickness of gate oxide continues shrinking. With this condition, we first encounter the difficulty of uniformity of thin film. Next, on characteristic of device, we will encounter: (1) direct tunneling, which make large leakage current. (2) mobility degradation, surface scattering raises on account of increasing vertical electric field with thickness shirking. To solve the problem above, scientists use high dielectric constant material that get thicker physical thickness with the same EOT as silicon oxide for gate dielectric film. In this thesis, we use Sputtering (PVD)-$LaAlO_3$ for gate dielectric film. The $LaAlO_3$ combines the good dense property of Al_2O_3 and the high dielectric constant ($\kappa \sim 23$). The performance is due to the increase, by a factor of $\kappa_{\text{dielectric}}/\kappa_{\text{SiO2}}$, in the gate capacitance density. This lowers the threshold voltage and improves both the gate-leakage current and breakdown field, since the thickness of the high dielectric constant layer can be increased. And PVD (Physical Vapor Deposition) process is not higher than 600℃.

1.5 Metal Gate Technology

Poly-Silicon is conventional gate material for CMOS process, because of adjustable threshold voltage with different concentration of implantation. While the thickness of gate dielectric continue shrink, Poly-Silicon gate will face several problem. (1) the surface between Poly-Silicon and Metal oxide (high dielectric constant material, Fig 1.1)[26] will cause Fermi-Level Pinning Effect that causes high threshold voltage (Fig 1.2-1.3)[26]. (2) doped Poly-Silicon deprivation will cause larger parasitic capacitance. Base on the reason above, metal gate technology will be trend for CMOS process.

Metals which apply for CMOS process divide into two parts:

1.Middle Band-gap Metal: Ti、Mo etc.

To use the same metal that can cause symmetry threshold voltage between NMOS and PMOS

2.Dual Metal System: NMOS: Al、Ta、TaN etc. (Low work function)

PMOS: Au、Pt etc. (High work function)

To use different metal which has different work function adjusts threshold voltage that matches the threshold voltage of NMOS and PMOS.

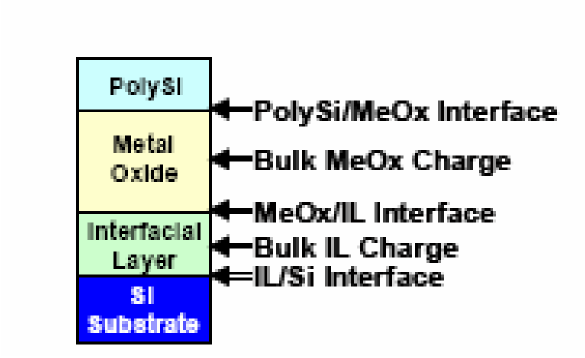


Fig 1.1 the structure of Poly-Silicon on Metal Oxide

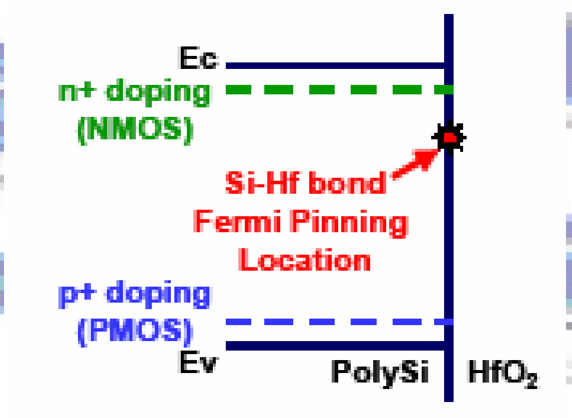


Fig 1.2 The Fermi level pining effect of Si-Hf bond

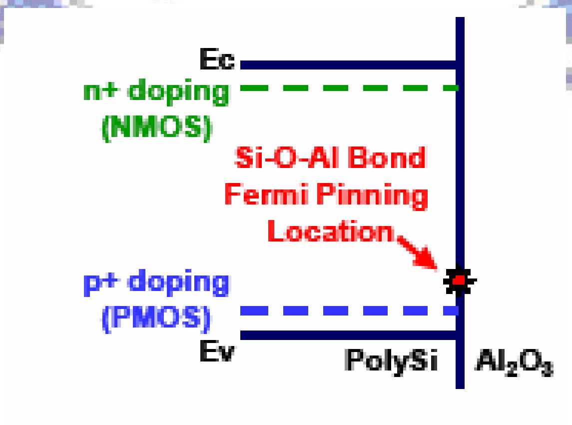


Fig 1.3 The Fermi level pining effect of Si-O-Al bond

1.6 Motivation

Although display technology does not suffer Fermi-Level Pinning Effect because of its thickness of gate dielectric film larger than 100nm, we still can adjust drive current (I_D) by using different metal which has different work-function. In this thesis, we use Ytterbium (Yb, the Lanthanide series metal that previously gave $YbSi_{2-x}$ low electron barrier to Si contact with good uniformity, work-function ≒ 2.6 eV) for gate material of NMOS, and will choose Iridium (Ir work-function ≒ 5.27 eV) for PMOS in the future research. From the threshold voltage equation[27]:

NMOS: $$V_{TN} = (|Q'_{SD}(\max)| - Q'_{ss})\left(\frac{t_{ox}}{\varepsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp}$$

PMOS: $$V_{TP} = (-|Q'_{SD}(\max)| - Q'_{ss})\left(\frac{t_{ox}}{\varepsilon_{ox}}\right) + \phi_{ms} - 2\phi_{fn}$$

The threshold voltage of NMOS decreases with lower ϕ_{ms}, and the threshold voltage of PMOS increases with higher ϕ_{ms}, relatively, and we can get higher drive current. So, we choose the low work-function metal, Ytterbium, for NMOS in our experiment.

We attempt to integrate this conception into Low Temperature Poly-Silicon technology that we can achieve high performance TFTs. In this thesis, we report $LaAlO_3$ gate dielectric with low work-function Ytterbium metal gate into LTPS TFTs NMOS, which show a high breakdown voltage, low sub-threshold slope, high field-effect mobility, large on-off-state drive current ratio (I_{on}/I_{off}) and high drive current. The high breakdown voltage and high transistor drive current suggest that the Ytterbium/$LaAlO_3$ TFTs can meet the device requirements for both pixel and display circuits. And then we hope that we can apply this technology for drive circuit on panel that realizes SOP (System On Panel).

1.7 Thesis Outline

In this thesis, we concentrate our efforts on metal gate for improving Poly-Silicon TFTs' performance.

In chapter 1, a brief overview of Poly-Silicon TFTs technology was given to describe the various applications and characteristics of Poly-Silicon TFTs. And it also shows our conception and motivation to use high $-\kappa$ gate dielectric and Ytterbium metal gate.

In chapter 2, the fabrication process flows of low temperature Poly-Silicon TFTs with metal gate and high $-\kappa$ gate dielectric, experimental recipes and device parameters extraction methods will be described.

In chapter 3, it shows the experimental data and the detail discussions of characteristics of high dielectric constant TFTs with metal gate includes high drive current, low threshold voltage, low sub-threshold slope, not bad mobility, and very good breakdown voltage. And it also shows the comparison between the performance of our conception and the performance of other TFTs' design.

Finally, conclusions and future works as well as suggestion for further research are given in chapter 4.

Chapter 2

The Experimental Steps

2.1 The Fabrication Steps

Fabrication of the TFTs started with the formation of a Poly-Silicon film, by depositing 100-nm amorphous Silicon on SiO_2/Si wafers (using LPCVD at 550 ^oC), followed by crystallization at 600^oC and 20 hour annealing in N_2. Then 500 nm thick PECVD oxide was deposited for isolation and device active region was formed by patterning and etching the isolation oxide. The source and drain regions in the active device region were implanted with phosphorus (35 KeV at 5×10^{15} cm^{-2}) and activated at 600^oC for 12 hour annealing under N_2. Then the 50 nm thick $LaAlO_3$ gate dielectric was deposited on previously patterned active region by sputtering from a $LaAlO_3$ source with 150 W power and 30 sccm Ar flow rate. A 400^oC and 30 min furnace O_2 treatment was applied to improve the gate oxide quality. Then gate was formed by depositing 200 nm Ytterbium using PVD. The TFTs devices were completed by gate definition with lift-off process, electrode formation and 400^oC sintering for 30 min under N_2 ambient without using hydrogenation plasma passivation treatment. The fabricated device has gate length and width of 4 μm and 100 μm, respectively.

2.2 The Structure of fabrication

1. Silicon substrate.

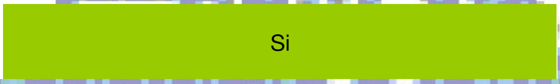


Fig 2.1 Step 1

2. Silicon dioxide growth (5000Å).

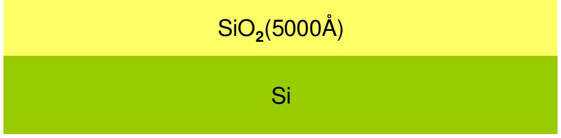


Fig 2.2 Step 2

3. Amorphous Silicon deposition by LPCVD at 550˚C (1000 Å).

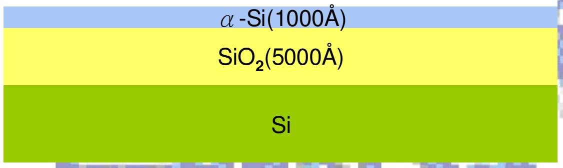


Fig 2.3 Step 3

4. Poly-Silicon recrystallization by annealing in N_2 at 600˚C for 20hr in furance.

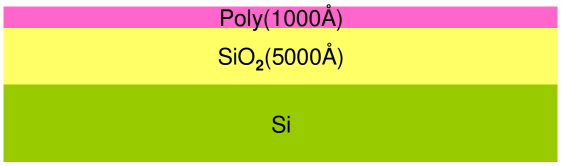


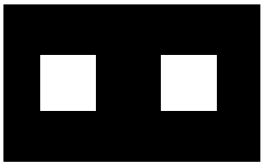
Fig 2.4 Step 4

5. Isolation oxide deposition by PECVD (5000 Å)

.

Fig 2.5 Step 5

6. Source and Drain region define, patterning, etching (MASK-1).



MASK-1

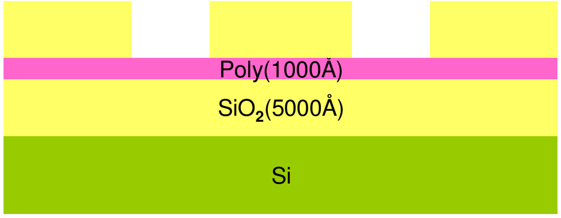


Fig 2.6 Step 6

7. Source and Drain implantation with phosphorus (35KeV at 5e15 cm^{-2}).

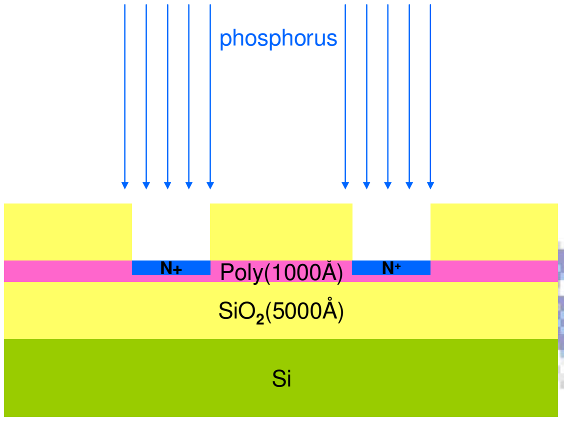
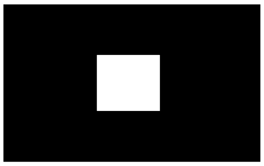


Fig 2.7 Step 7

8. Activating in N_2 at 600˚C for 12hr.
9. Removing Silicon on gate region (MASK-2).


MASK-2

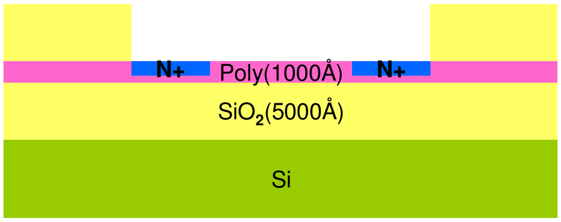


Fig 2.8 Step 8 9

10. $LaAlO_3$ deposition by PVD in Ar (150-W, 30-sccm, 500 Å).

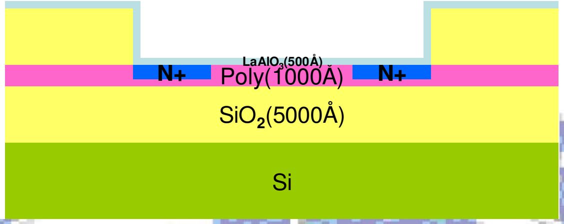
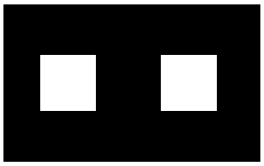


Fig 2.9 Step 10

11. Contact hole define, patterning, etching (MASK-3).



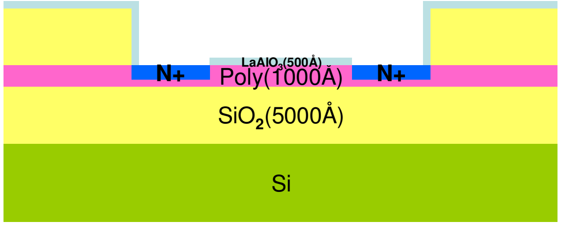


Fig 2.10 Step 11

12. Photoresist deposition

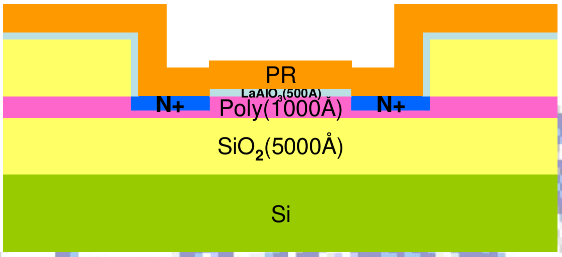


Fig 2.11 Step 12

13. Metal region definition (lift-off, MASK-4)

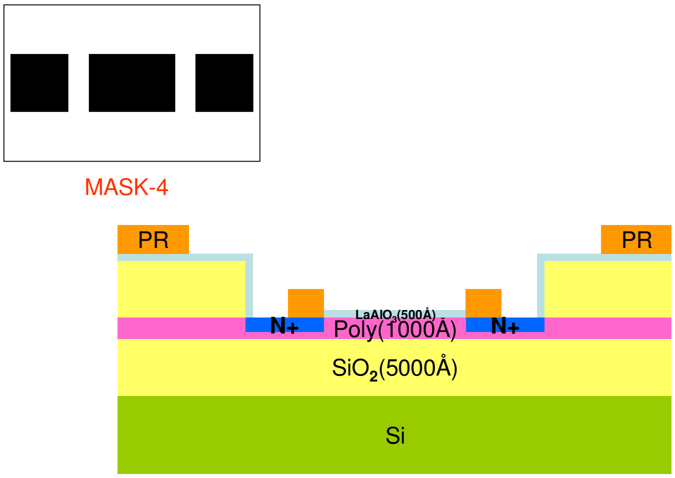


Fig 2.12 Step 13

14. PVD-Yb deposition (2000 Å)

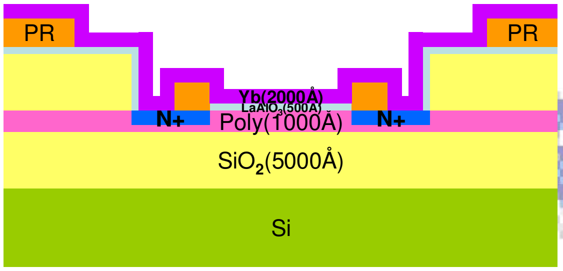


Fig 2.13 Step 14

15. Removing PR

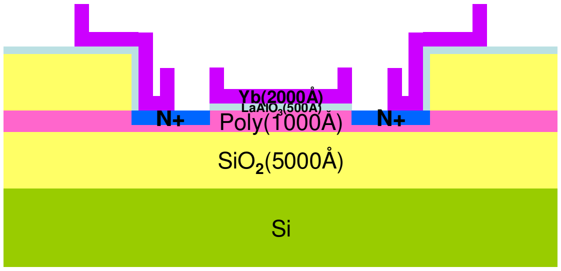


Fig 2.14 Step 15

Chapter 3

Result & Discussion

3.1 Method Of Device Parameter Extraction

In this thesis, we use Ellipsometer to measure the thickness of Poly-Silicon, amorphous-Si and dielectric films in the fabrication procedure. All the electrical characteristics of proposed Poly-Silicon TFTs were measured by HP 4156 Precision Semiconductor Parameter Analyzer. Many methods have been proposed to extract the characteristic parameters of Poly-Silicon TFTs. In this section, those methods are described.

3.1.1 Determination Of Threshold Voltage

Threshold voltage (V_{th}) is an important parameter required for the channel length-width and series resistance measurements. However, V_{th} is not uniquely defined. Various definitions have been proposed and the reason can be found in I_D-V_{GS} curves. One of the most common techniques is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of 50~100mV to ensure operation in the linear region [17]. The drain current is not zero when V_{GS} below threshold voltage and approaches zero asymptotically. Hence the I_{DS} versus V_{GS} curve can be extrapolated to I_D=0, and the V_{th} is determined from the extrapolated intercept of gate voltage (V_{GSi}) by

$$V_{th} = V_{GSi} - \frac{V_{DS}}{2} \quad \text{-- (Eq. 3.1)}$$

Equation (3.1) is strictly only valid for negligible series resistance. Fortunately series resistance is usually negligible at the low drain current when threshold voltage measurements are made. The I_{DS}-V_{GS} curve deviates from a straight line at gate voltage below V_{th} due to sub-threshold current and above V_{th} due to series resistance and mobility degradation effects. It is common practice to find the point of maximum slope of the I_{DS}-V_{GS} curve (the same as the max-value point of Field Effect Mobility, from Eq. 3.4)and fit a straight line to extrapolate to I_D=0 by means of finding the point of maximum of transconductance (Gm).

In other thesis, someone can use a simpler method to determinate the V_{th} called constant drain current method. The voltage at a specified threshold drain current is taken as the V_{th}. This method is adopted in the most studied papers of Poly-Silicon TFTs. It can be given a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current is specified at (W/L)×10nA for V_{DS}=0.1V and (W/L)×100nA for V_{DS}=5V, where W and L are channel width and channel length, respectively.

3.1.2 Determination Of Sub-threshold Slope

Sub-threshold slope (S.S.) is a typical parameter to describe the control ability of gate toward channel, which reflects the turn on/off speed of a device. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude.

The S.S. should be independent of drain voltage and gate voltage. However, in reality, the S.S. increases with drain voltage due to channel shortening effect such as charge sharing, avalanche multiplication and punchthrough effect. The sub-threshold slope is also related to gate voltage due to undesirable and inevitable factors such as the serial resistance and interface states.

In this thesis, the S.S. is defined as one-third of the gate voltage required to decrease the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

3.1.3 Determination Of Field Effect Mobility

Usually, field effect mobility (μ_{eff}) is determined from the maximum value of transconductance (Gm) at low drain bias. The transfer characteristics of Poly-Silicon TFTs are similar to those of conventional MOSFETs, so that the first order of I-V relation in the bulk Si MOSFETs can be applied to Poly-Silicon TFTs. The drain current in linear region ($V_{DS} < V_{GS} - V_{th}$) can be approximated as the following equation:

$$I_{DS} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}{}^{2} \right] \quad \text{----------------------- (Eq. 3.2)}$$

where W and L are channel width and channel length, respectively. C_{ox} is the gate oxide capacitance per unit area and V_{th} is the threshold voltage. Thus, the transconductance is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) V_{DS} \quad \text{-------------------------------------- (Eq. 3.3)}$$

Therefore, the field-effect mobility is

$$\mu_{eff} = \frac{L}{C_{ox} W V_{DS}} g_{m(\max)} \Big|_{V_{DS} \to 0} \quad \text{-- (Eq.3.4)}$$

3.1.4 Determination Of ON/OFF Current Ratio

On/Off current ratio is one of the most important parameters of Poly-Silicon TFTs since a high-performance device exhibits not only a large on-current but also a small off-current (leakage current). The leakage current mechanism in Poly-Silicon TFTs is not like that in MOSFET. In MOSFET, the channel is composed of single crystalline Si and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in Poly-Silicon TFTs, the channel is composed of Poly-Silicon. A large amount of trap state densities in grain structure attribute a lot of defect states in energy band gap to enhance the tunneling effect. Therefore, the leakage current is much larger in Poly-Silicon TFTs than in MOSFET. When the voltage drops between gate voltage and drain voltage increases, the band gap width decreases and the tunneling effect becomes much more severe. Normally we can find this effect in typical Poly-Silicon TFTs' I_{DS}-V_{GS} characteristics where the magnitude of leakage current will reach a minimum and then increase as the gate voltage decreases/increases for n/p-channel TFTs.

There are a lot of ways to specify the on and off-current. In this chapter, take n-channel Poly-Silicon TFTs for examples, the on-current is defined as the drain current when gate voltage at the maximum value and drain voltage is 0.1V. The off-current is specified as the minimum current when drain voltage equals to 0.1V.

$$\frac{I_{ON}}{I_{OFF}} = \frac{Maximum \;\; Current \;\; of \;\; I_{DS} - V_{GS} \;\; Plot \;\; at \;\; V_{DS} = 0.1V}{Minimum \;\; Current \;\; of \;\; I_{DS} - V_{GS} \;\; Plot \;\; at \;\; V_{DS} = 0.1V} \quad \text{-------- (Eq. 3.5)}$$

3.2 Experimental Data Result & Discussion

The fabricated devices were characterized using HP4156 and HP4284 Precision Semiconductor Parameter Analyzer. We first show the data of NMOS-TFT (Yb / $LaAlO_3$). The I_d-V_g characteristics of a representative TFT are shown in Fig. 3.1. The threshold voltage is 0.85 V which is better than the threshold voltage of the device with aluminum gate which we reported before (1.2 V, Fig 3.2). The threshold voltage decreases because that Ytterbium (≒2.6 eV) makes the lower ϕ_{ms}. Base on the threshold voltage equation: $V_{TN} = (|Q'_{SD}(\max)| - Q'_{ss})\left(\frac{t_{ox}}{\varepsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp}$ [27], lower ϕ_{ms} makes lower threshold voltage. And in Fig 3.3, we can see the sub-threshold slope of 0.58 V/decade, the low sub-threshold swing indicates a low interface trap density, and is consistent with the good electron field-effect mobility of 31.4 cm^2/Vs which is showed in Fig 3.4. This is because the sputtering and subsequent 400°C oxidation also oxidized the poly-silicon surface. Although this is the undesired feature in high-κ CMOS to lower down the EOT [28-31], the good high-κ/Ytterbium interface gives the not bad mobility and good sub-threshold slope. The I_{on} / I_{off} ratio of the Ytterbium/$LaAlO_3$ TFT is 1.63×10^6, even without performing hydrogen passivation.

And then the output characteristics (I_d-V_d) of the Ytterbium/$LaAlO_3$ TFT are shown in Fig. 3.5. The large drive current of 22 μA/μm, at 5 V, is attractive for high-speed display ICs. This good performance is related to the lower threshold voltage and the high gate-capacitance of 3.9×10^{-7} F/cm^2 from C-V measurements (Fig 3.6), which gives a small equivalent-oxide thickness (EOT) of 8.7 nm at a κ value of ~22.5 [28][29] This is the thinnest reported EOT TFTs so far [32-35], And the high drive current is higher than our past reported Al/LaAlO$_3$ (EOT=8.7 nm) thin film transistor, which is showed in Fig 3.7~3.13. It is because the work-function of Al (≒4 eV) is higher than that of Yb (≒2.6 eV). So the data affirm our conception. Our design also provides an alternative way to create high drive current, along with existing approaches such as excimer-laser crystallization (ELC) [32][36-38], metal-induced lateral crystallization [39] and electric field enhanced crystallization [40]. It shows that good uniformity is also obtained due to the furnace crystallization, in contrast with the narrow process window and poor uniformity in ELC TFTs [41].

The field dependence of the gate current density is showed in Fig 3.14 shows a gate dielectric breakdown voltage of 31-32 V. This corresponds to an electric field of 6.25 MV/cm that is slightly larger than PECVD TEOS oxide of 5.4 MV/cm[35]. This is high enough to drive a liquid crystal display. This high breakdown field is comparable with or better than that for PECVD TEOS oxide [32-34][42]. This is important for achieving good dielectric reliability [28-31]. It may arise from the plasma-free process used, which does not damage the gate dielectric.

Figure 3.15 shows the charge-trapping characteristics of the Ytterbium/LaAlO$_3$ TFTs under constant-current stress from 0.1 to 10 mA/cm^2 (or ~2.9 to 5.8 MV/cm electric field). The gate voltage shift is only 0.61 V even under 10 mA/cm^2 stress, which is much better than the 2.2 V shift in TEOS oxide TFTs under the same stress condition [43]. Such low charge-trapping indicates the good quality of the gate dielectric and is consistent with high – κ $LaAlO_3$ CMOSFETs also fabricated at low temperature [28-29] and good intersurface between metal gate and high – κ gate dielectric. Hence integrating high- κ gate dielectrics with Ytterbium metal gate into TFT-NMOS should not degrade the TFT device reliability, often dominated by the grain-boundary related hot-carrier degradation [44]

The important device parameters are summarized in Table 1, where the data from devices using PVD $LaAlO_3$ with Al gate, LPCVD SiO_2 with poly-silicon gate, PECVD TEOS oxides [33-35] with poly-silicon gate and Al_2O_3 gate dielectric with Poly-SiGe gate [45] are also shown for comparison. The better device performance of the Ytterbium/$LaAlO_3$ TFTs that compared with LPCVD, PECVD TEOS oxide TFTs (using the same furnace-crystallization process) and relative low – κ Al_2O_3 devices, is due to the lower threshold voltage which results from the higher capacitance density combining with low work-function Ytterbium metal gate ($V_{th}= \phi_{ms} + Q_{total}/C_{dielectric}$), and the plasma-free process.

Gate dielectric	This work	$LaAlO_3$ 50 nm (8.7 nm EOT)	LPCVD SiO_2 80 nm[33]	PECVD TEOS oxide 60 nm[34]	PECVD TEOS oxide 40 nm[35]	Al_2O_3 50 nm[45]
Gate electrode	Ytterbium	Aluminum	Poly-Si	Poly-Si	Poly-Si	Poly-SiGe
V_{th} (V)	0.85	1.2	5.6	8.14	Not extracted	3
μ_{FE} (cm^2/Vs)	31.4	40	20	12.44	3	47
Sub-threshold slope (V/decade)	0.58	0.31	1.4	1.97	2.67	0.44
I_{on}/I_{off}	1.63×10^6	1.5×10^6	3.5×10^5	2.97×10^5	Not extracted	3×10^5
Breakdown field (MV/cm)	6.25	6.3	Not extracted	Not extracted	5.4	Not extracted

Table 1

The primary parameter comparison of different structure thin film transistor

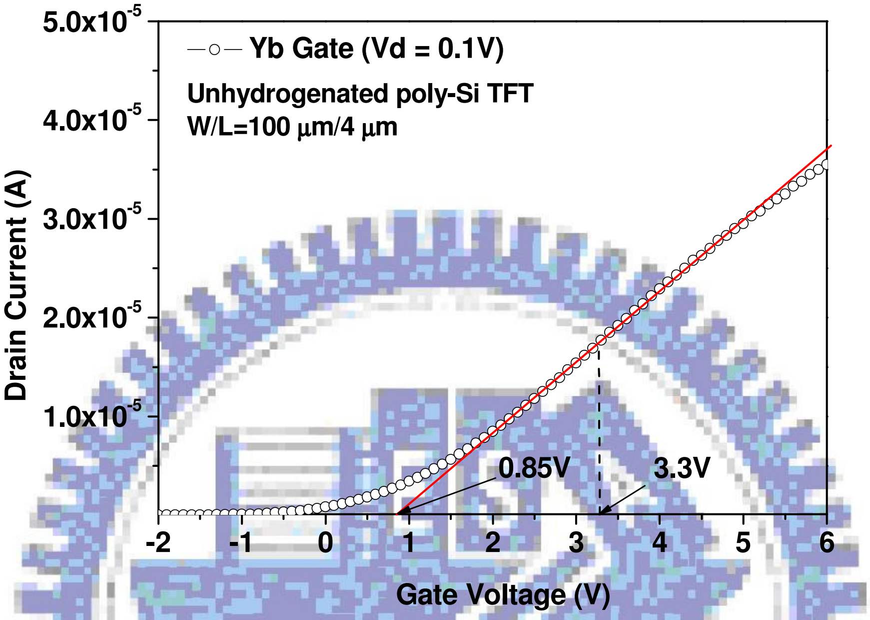


Fig 3.1 The threshold voltage of Yb/$LaAlO_3$ thin film transistor

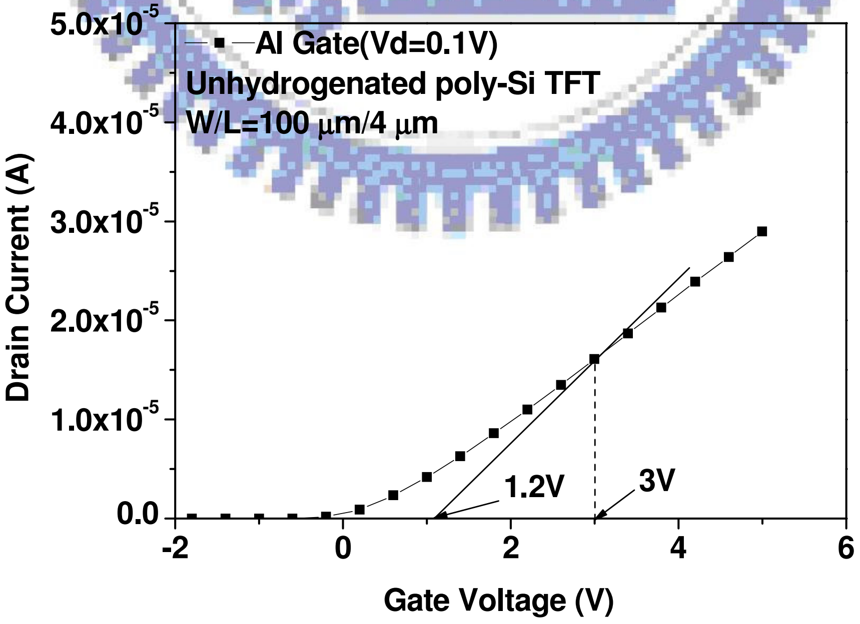


Fig 3.2 The threshold voltage of Al/LaAlO$_3$ thin film transistor

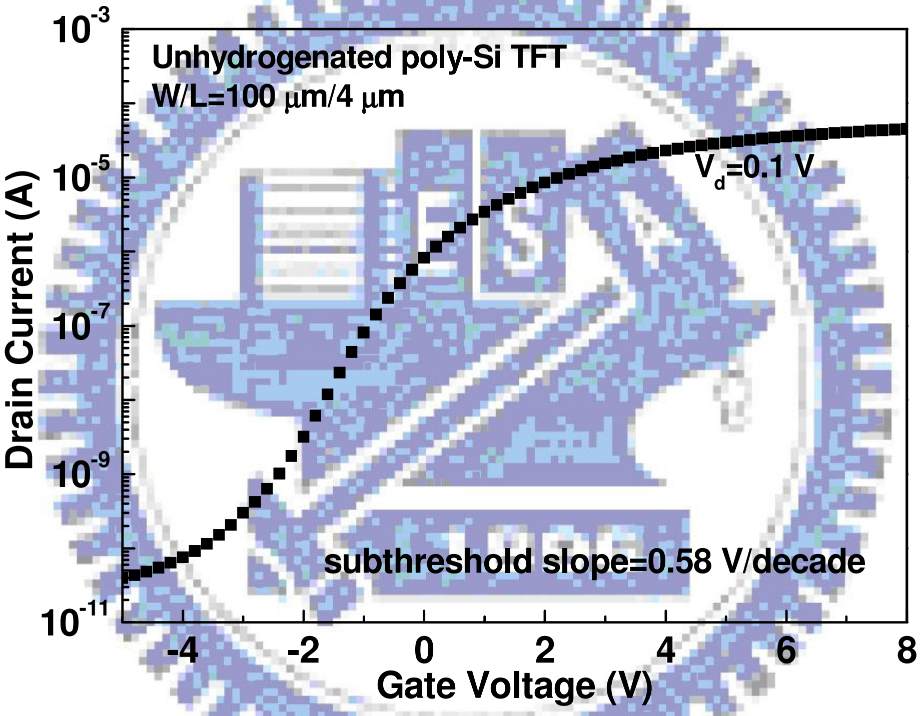


Fig 3.3 The low subthreshold slope of Yb/LaAlO3 thin film transistor

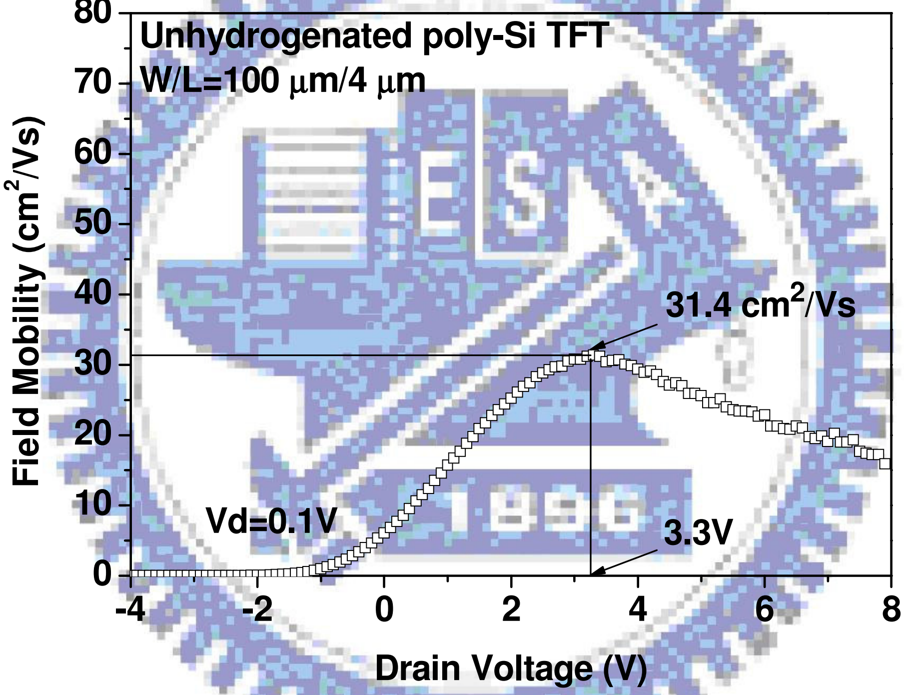


Fig 3.4 The mobility of Yb/LaAlO3 thin film transistor

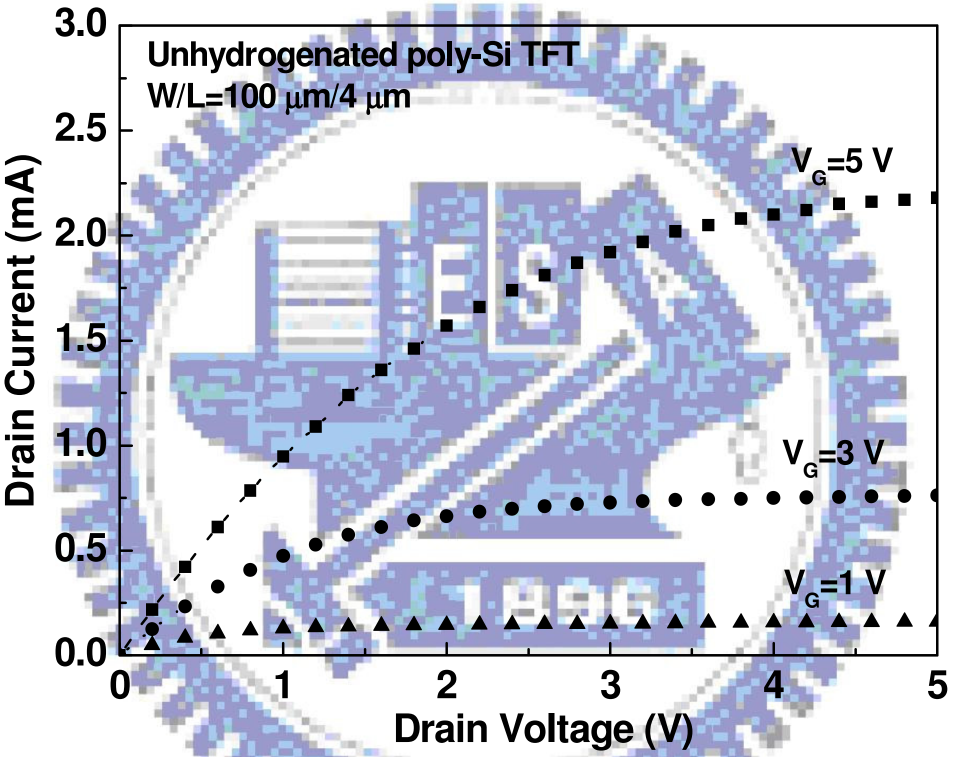


Fig 3.5 The drain current of Yb/LaAlO$_3$ thin film transistor at different voltage

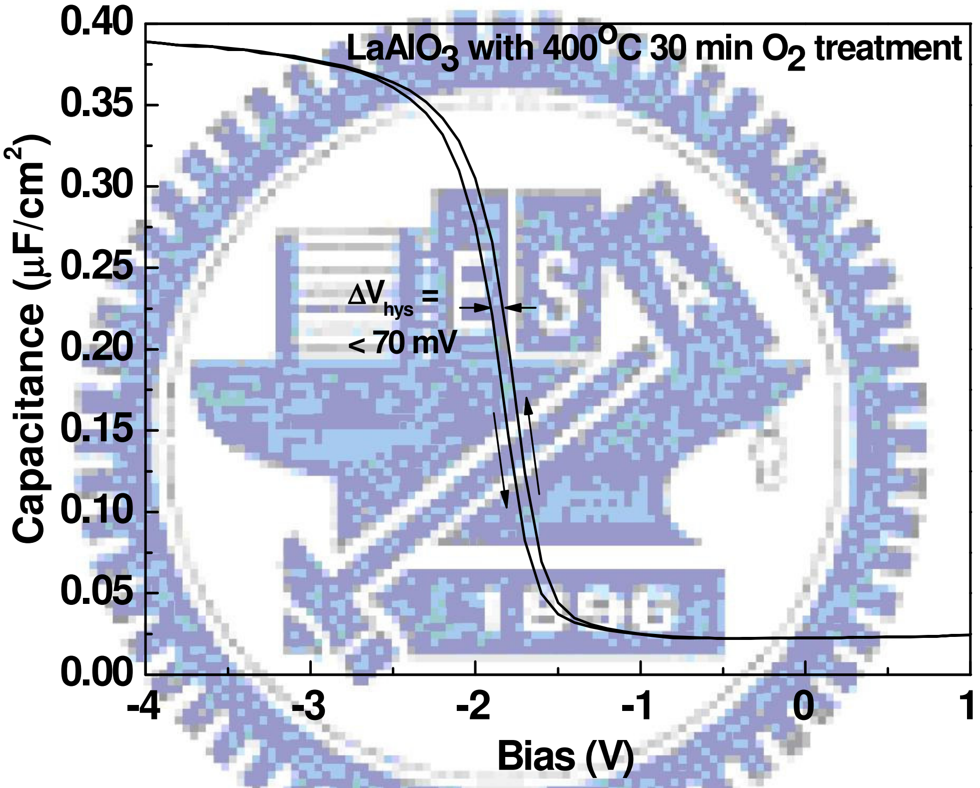


Fig 3.6 The C-V measurements of Yb/LaAlO$_3$ thin film transistor

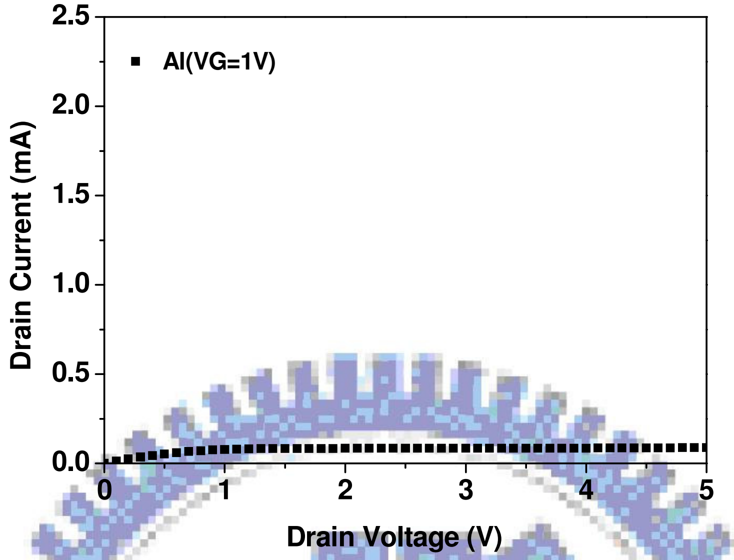


Fig 3.7 The drain current of Al/LaAlO$_3$ thin film transistor at Vg=1V

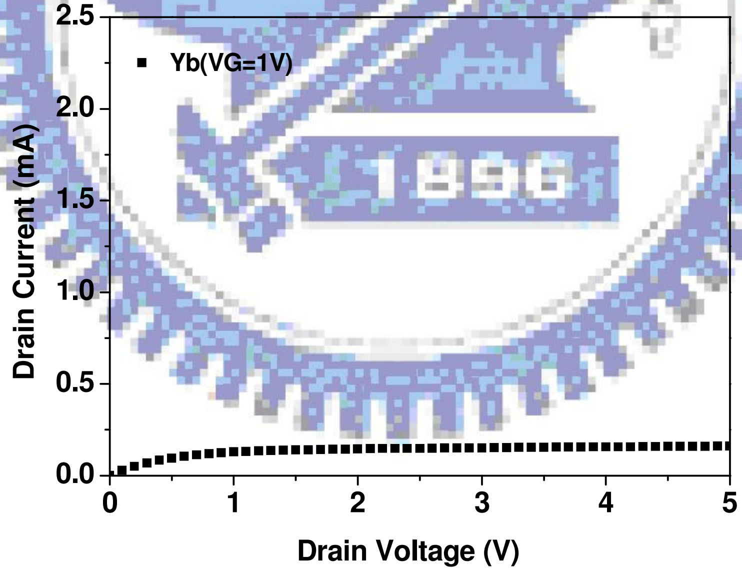


Fig 3.8 The drain current of Yb/LaAlO$_3$ thin film transistor at Vg=1V

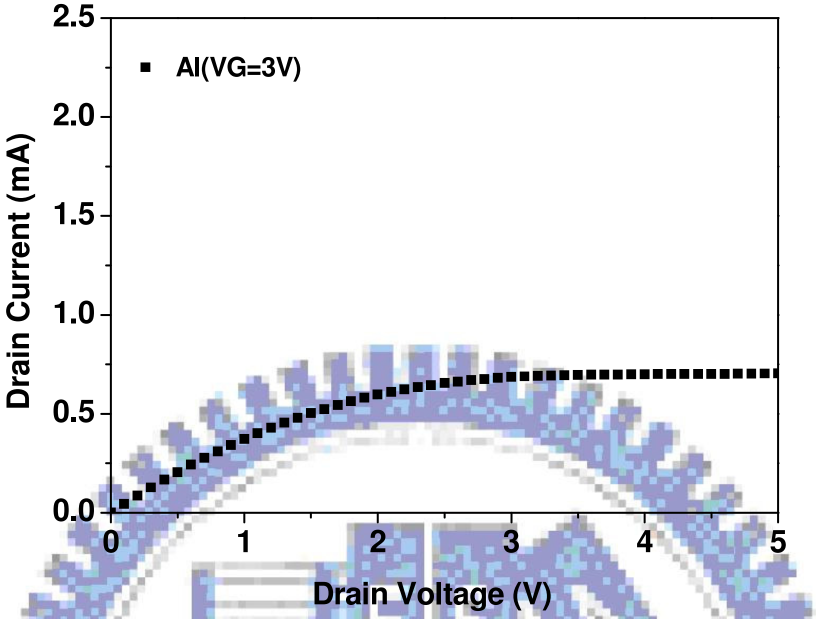


Fig 3.9 The drain current of Al/LaAlO$_3$ thin film transistor at Vg=3V

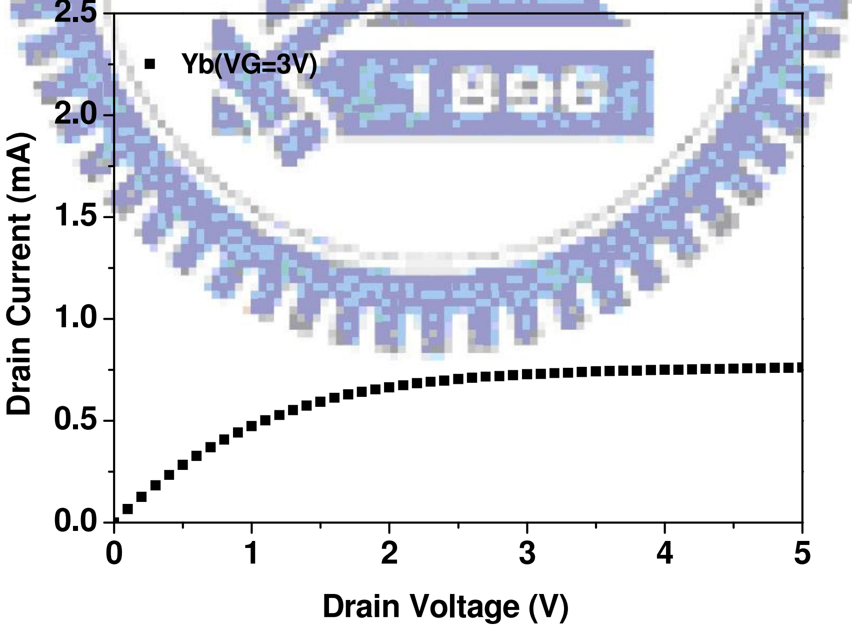


Fig 3.10 The drain current of Yb/LaAlO$_3$ thin film transistor at Vg=3V

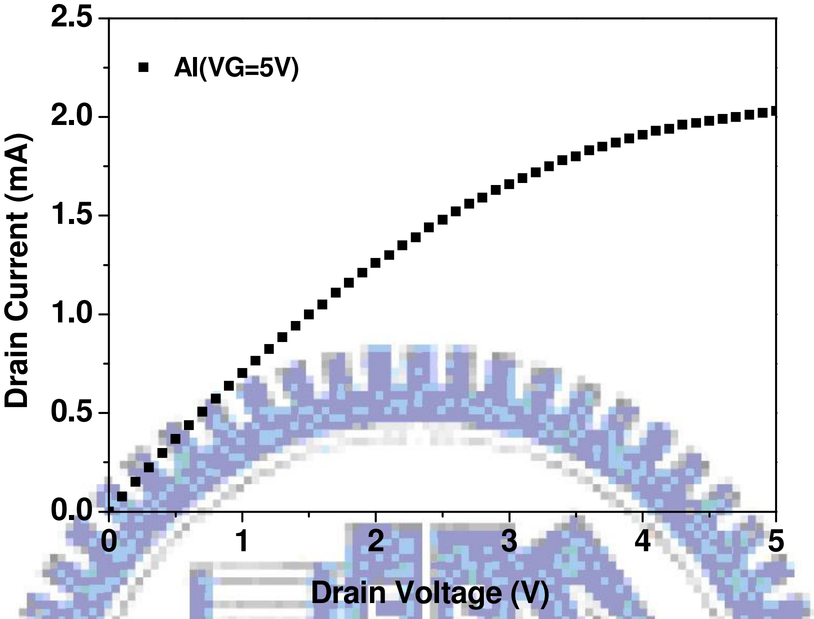


Fig 3.11 The drain current of Al/LaAlO$_3$ thin film transistor at Vg=5V

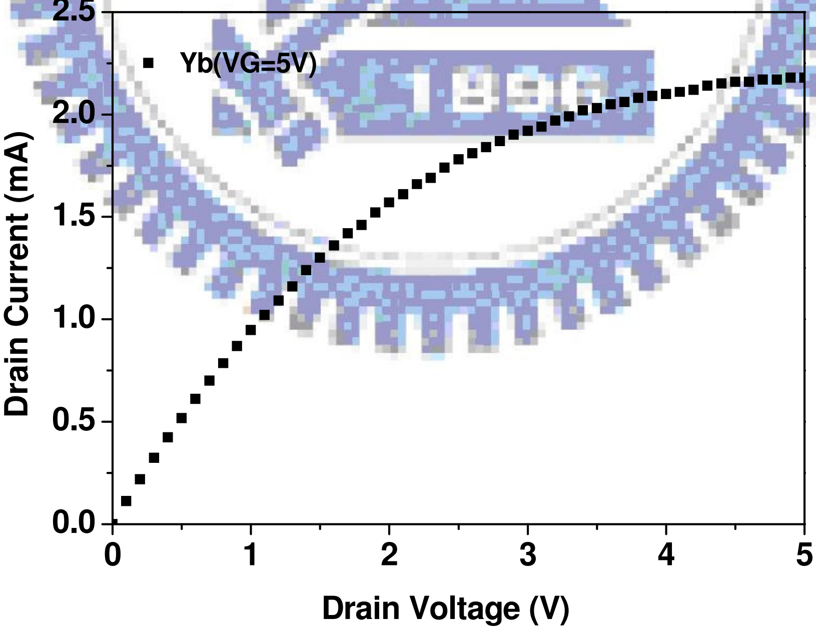


Fig 3.12 The drain current of Yb/LaAlO$_3$ thin film transistor at Vg=5V

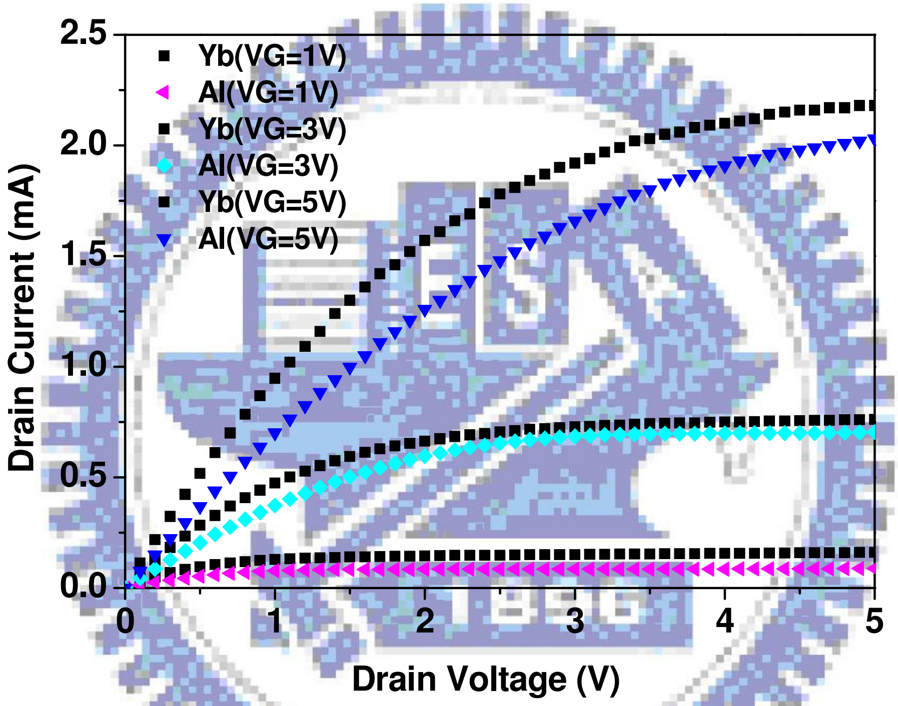


Fig 3.13

The comparison of drain current at different gate voltage between

Yb-gate and Al-gate

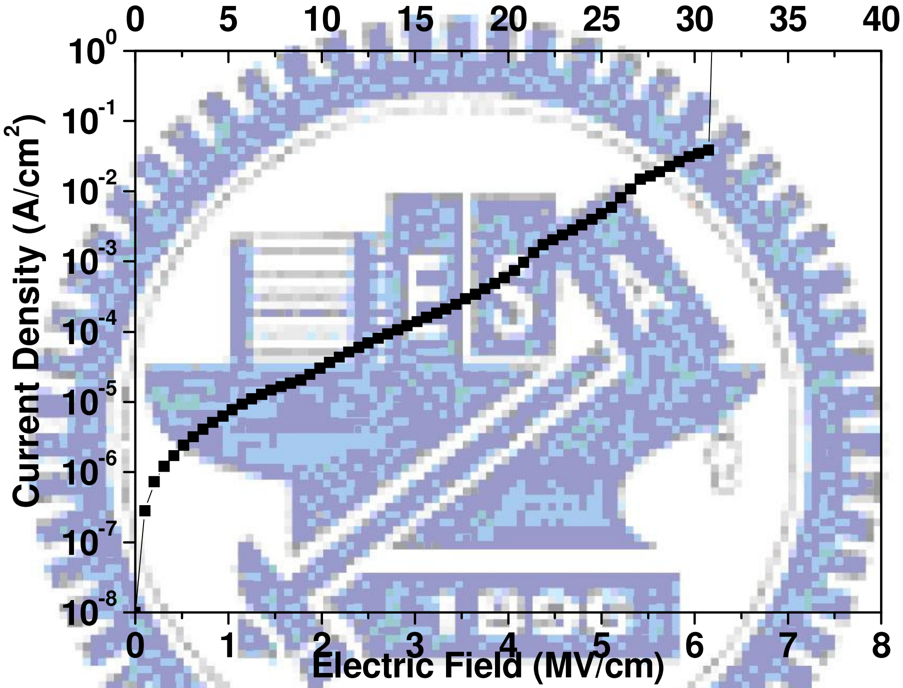


Fig 3.14 The breakdown voltage of Yb/LaAlO3 thin film transistor

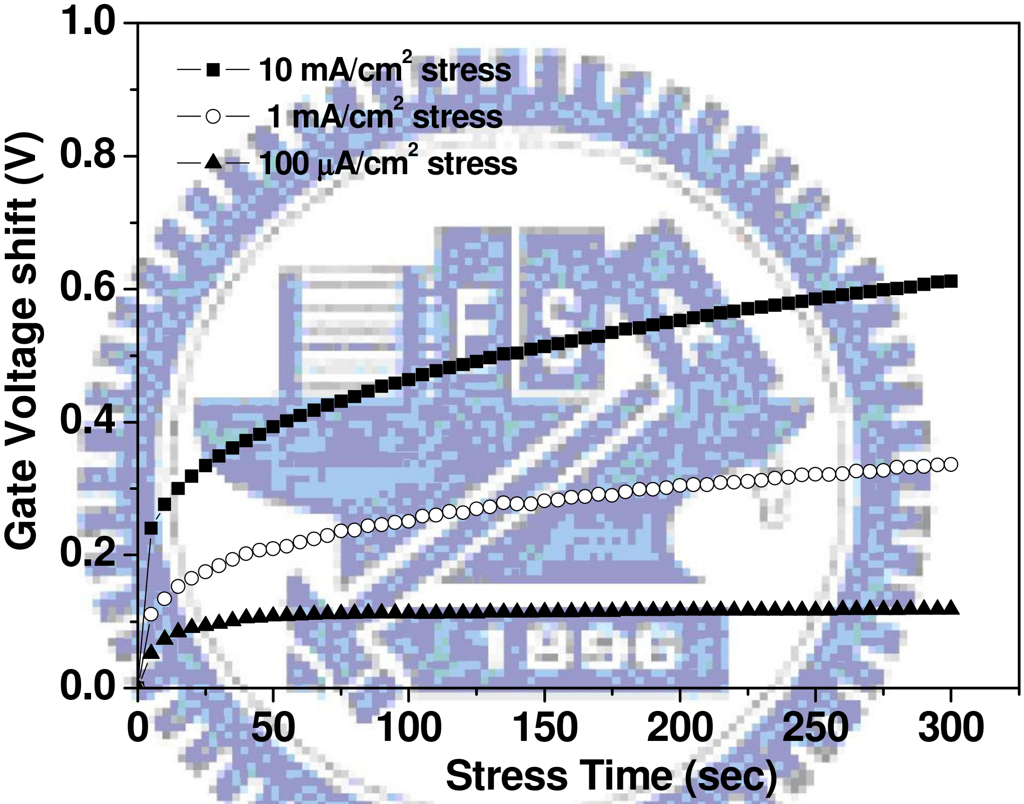


Fig 3.15 The gate voltage shift of Yb/LaAlO3 thin film transistor

4. Conclusion

We have fabricated and characterized high-performance LTPS TFTs-NMOS which incorporate high- κ $LaAlO_3$ dielectric with low work-function Ytterbium metal gate that provides good dielectric properties such as a high breakdown field, low threshold voltage, low leakage current and low charge trapping rate. These devices exhibit excellent electrical characteristics and high drive current, even without special process steps. We can expect that we may achieve better performance by using hydrogenation passivation or excimer laser crystallization process steps to improve the trap density on interface or get high quality Poly-Silicon film. And we will keep the same conception on TFTs-PMOS by using higher work-function metal such as the second highest work-function metal, Iridium. We do not expect to use Pt (The highest work-function metal) because that it is difficult to be etched in process.. And finally, we may integrate this high performance device for drive circuit on panel that realizes SOP (System On Panel).

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