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損耗基板之去寄生效應法與射頻金氧半
場效電晶體雜訊萃取之應用

Lossy Substrate De-embedding Method for RF MOSFET Intrinsic Noise Extraction

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摘要

閘極長度為 80 與 65 奈米之奈米級金氧半場效電晶體分別擁有高達 100 與 165GHz 的截止頻率。但是根據量測得到的雜訊特性，兩者的最低雜訊指數卻沒有因此而有明顯的差異。當閘極偏壓在對應元件最高截止頻率下操作，在頻率 10GHz 的最低雜訊指數甚至超過 5dB。另外，隨著閘極指叉數目增加其最低雜訊指數大幅減小，與指叉數目有很強的關連。上述現象並無法簡單地用閘極阻值因為指叉數目增加並聯後減少所導致的雜訊減低來完全解釋。因此，提出了元件量測雜訊特性之去寄生雜訊效應的方式，以獲得元件之真實特性。

在本論文中，首先整理金氧半電晶體相關的基本雜訊理論與高頻雜訊量測原理及設備，並討論傳統去寄生雜訊的方式以及其缺點。元件本質特性模型的部分，先透過量測電流-電壓特性、轉導以及導納參數校正元件本質特性模型的參數。接著探討不同的測試元件探針墊片佈局方式對量測特性的影響，根據相對應的探針墊片提出新式等校電路模型及其參數萃取方式並經大量實驗結果驗證後，再將探針墊片的等效電路搭配經過準確校正的元件模型構成完整電路，模擬直接量測到的散射參數以及雜訊參數。最後，將表現出高損耗特性的探針墊片模型從完整電路模型中移除，模擬元件之本質特性，最後根據所得到的元件雜訊參數進行分析及探討。

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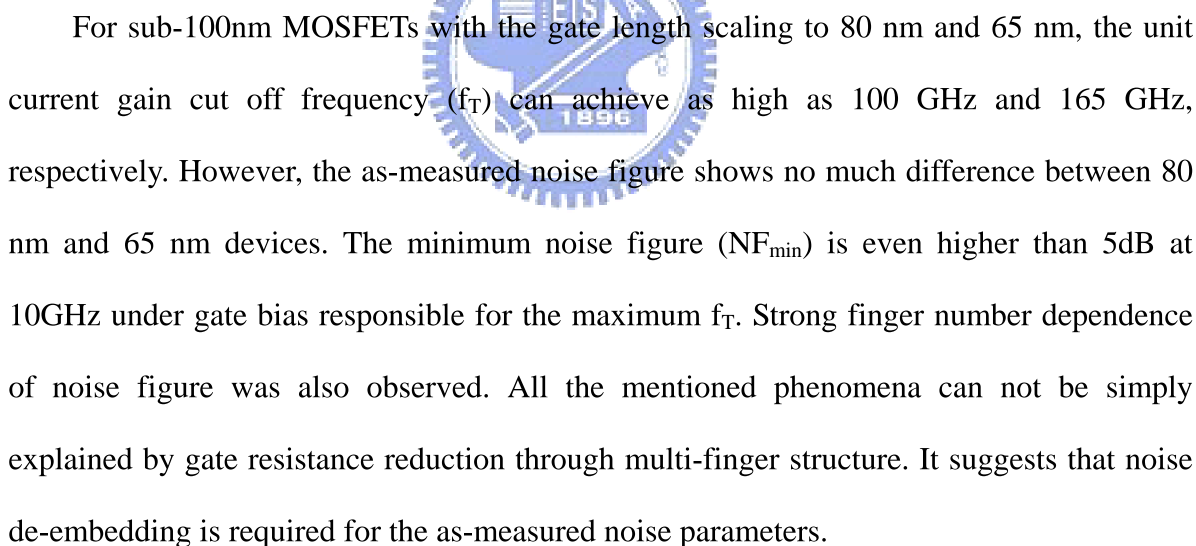
ABSTRACT



For sub-100nm MOSFETs with the gate length scaling to 80 nm and 65 nm, the unit current gain cut off frequency (f_T) can achieve as high as 100 GHz and 165 GHz, respectively. However, the as-measured noise figure shows no much difference between 80 nm and 65 nm devices. The minimum noise figure (NF_{min}) is even higher than 5dB at 10GHz under gate bias responsible for the maximum f_T. Strong finger number dependence of noise figure was also observed. All the mentioned phenomena can not be simply explained by gate resistance reduction through multi-finger structure. It suggests that noise de-embedding is required for the as-measured noise parameters.

In this thesis, the basic noise theory of MOSFET, noise measurement principles and instruments will be covered in the first place. Conventional noise correlation matrix de-embedding method will be reviewed. Regarding the intrinsic MOSFET model, I-V and C-V model calibration have been done based on the measured I-V, transconductance, and admittance by Y-parameters. Then discussion of different probing pad effect on device characterization, and the corresponding equivalent circuit model has been established and

extensively verified. A new equivalent circuit de-embedding method was proposed. Modeling of as-measured S-parameters and noise parameters was done by incorporating the pad model with a well calibrated MOSEFT model. The lossy pad and lossy substrate de-embedding has been conducted to obtain the intrinsic characteristic. Finally, the intrinsic performance of the device will be analyzed and discussed.

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兩年的碩士班生活很快地過去了，此論文是研究所期間所學到的重點內容整理。不只是此本論文的完成，包含兩年來所學到的以及生活的點點滴滴，都有很多人必須感謝。

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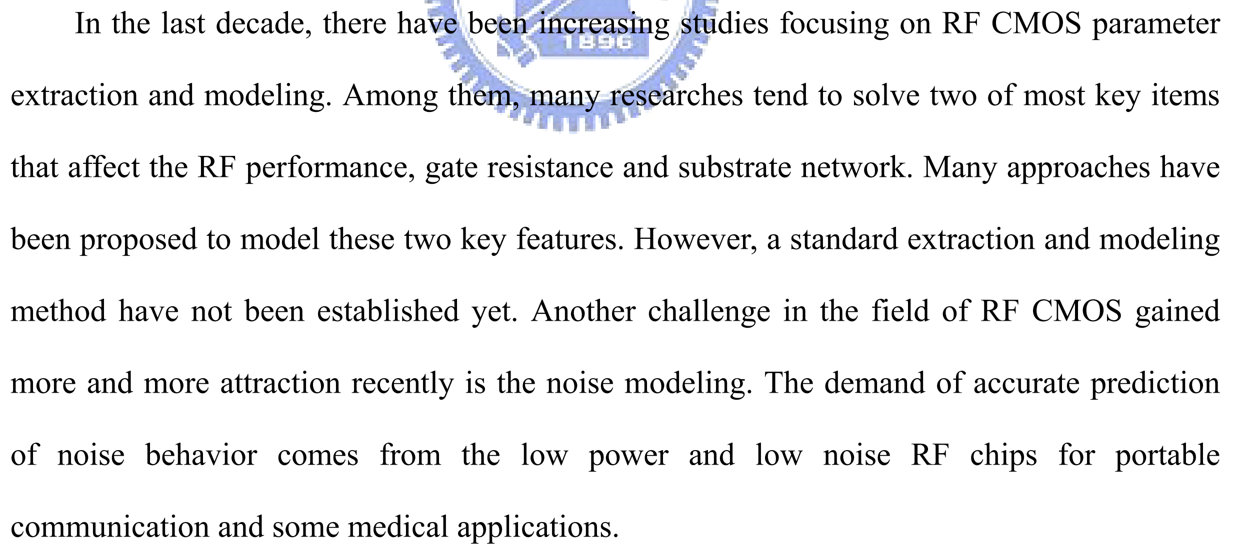
Chapter 1

Introduction

The aggressive scaling of CMOS technologies has resulted in remarkable improvement in the RF performance. Accompanied with its superiority in low cost, high integration and mature techniques, CMOS has become a promising candidate for RF circuit application. The rapid growing wireless communication industry and its severe competition increase the needs for RF chips and demand the reduction of product design cycle. Accuracy of the device model is one of the important factors that affect the circuit performance and its success. The complex signal coupling inside the device and the lossy characteristic of silicon substrate make parameter extraction and device modeling a challenge.

1.1 Motivation



In the last decade, there have been increasing studies focusing on RF CMOS parameter extraction and modeling. Among them, many researches tend to solve two of most key items that affect the RF performance, gate resistance and substrate network. Many approaches have been proposed to model these two key features. However, a standard extraction and modeling method have not been established yet. Another challenge in the field of RF CMOS gained more and more attraction recently is the noise modeling. The demand of accurate prediction of noise behavior comes from the low power and low noise RF chips for portable communication and some medical applications.

On-wafer measurement at microwave frequency is the best way to characterize the RF device. However, as we all know, measurement of high frequency characteristics always incorporated parasitic effects introduced by the test feature excluding the device of major interest. Accurate de-embedding procedure prior to parameter extraction and device modeling

can isolate those parasitics and generally make model more scalable. Therefore, de-embedding of parasitic components is also one of the important works. Regarding low noise RF CMOS design, noise modeling is absolutely more challenging than S-parameters modeling. The difficulty is due to the complex noise mechanism in MOSFET, limited knowledge about the noise source, and coupling introduced by low resistivity Si substrate. In recent years, many studies have been focused on noise current extraction [1] and noise mechanism modeling [2-5]. However, fewer studies were focused on the noise de-embedding and intrinsic noise extraction [6,7]. Noise de-embedding is also considered as an important procedure prior to noise modeling and simulation. In the research process, some suspicious features occurred in the as-measured noise characteristics. It suggests that appropriate de-embedding is indispensable. This stimulates our motivation of this study on the noise de-embedding techniques and triggers some new ideas proposed in this thesis.

1.2 Overview

The main objective of this thesis is to deal with one of important issues in MOSFET noise modeling, it is noise de-embedding. To achieve this goal, detailed information about MOSFET noise in terms of theoretical principle, measurement data and simulation results will be provided. This thesis has been organized into seven chapters as follows:

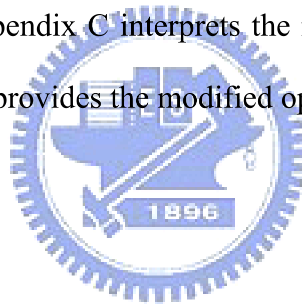
Chapter 2 gives an introduction to the classification and physical mechanism of noise in MOSFETs. The noise measurement theory and measurement system configuration are also covered. Chapter 3 begins with discussion of as-measured noise parameters and three interesting features identified in this study. In the following, conventional correlation matrix de-embedding method and its usability will be reviewed.

Chapter 4 presents the intrinsic model calibration in terms of I-V characteristics and gate capacitance feature, which were extracted from de-embedded Y-parameters at low frequency.

Key model parameters associated with I-V and C-V in BSIM model are discussed.

Chapter 5 addresses how to build the lossy pad equivalent circuit model associated with various layout structures. The extensive verification on full circuit model will be described. Good match with the measured extrinsic noise characteristics will be demonstrated. Chapter 6 discusses the equivalent circuit noise de-embedding results in which intrinsic noise performance for sub-100nm MOSFET has been extracted. It helps to identify the truly intrinsic performance of the devices and provide the circuit designers correct guideline for low noise design. Chapter 7 concludes with a summary and suggestions for future work.

Appendices A ~ D provide more detailed explanation of certain contents. Appendix A describes the derivation of noise parameters. Appendix B addresses the Y-factor method for noise figure measurement. Appendix C interprets the noise correlation matrix de-embedding technique. Finally appendix D provides the modified open and short de-embedding method.

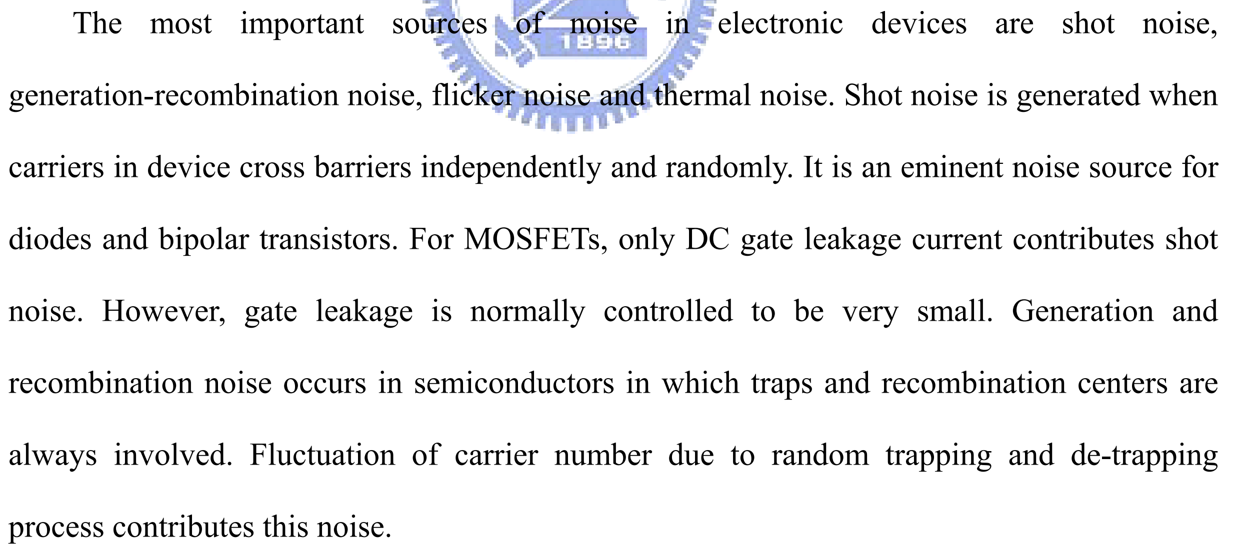


Chapter 2

Noise Theory and Noise Measurement Technique

Noise, briefly speaking, can be thought as a kind of signal that is undesirable for a device, circuit, or system. It is generally caused by the fluctuation of voltage or current in an electronic device or component. Noise set the lower limit of measurement or detection which is an important issue for engineering application. In this chapter, noise sources in electronic devices are summarized and high frequency noise in MOSFET, which is dominated by the thermal noise, is focused. Noise theory for noise behavior analysis of two-port network will be covered. Finally, high frequency noise characterization and analysis are provided in the end of the chapter.

2.1 Noise Sources



The most important sources of noise in electronic devices are shot noise, generation-recombination noise, flicker noise and thermal noise. Shot noise is generated when carriers in device cross barriers independently and randomly. It is an eminent noise source for diodes and bipolar transistors. For MOSFETs, only DC gate leakage current contributes shot noise. However, gate leakage is normally controlled to be very small. Generation and recombination noise occurs in semiconductors in which traps and recombination centers are always involved. Fluctuation of carrier number due to random trapping and de-trapping process contributes this noise.

The dominant noise sources of MOSFETs are flicker noise and thermal noise. The origin of flicker noise is generally proposed coming from the carrier number fluctuation due to trapping and de-trapping processes in the $Si\text{-}SiO_2$ interface or from mobility fluctuation of device on the basis of empirical results. It is also called, 1/f noise, due to its noise power

spectral density given by (2.1) in which a frequency dependence with slope n approaching unity is achieved

$$S_I(f) = K \cdot \frac{I^m}{f^n} \tag{2-1}$$

However, while working in microwave frequency, flicker noise is small compared with thermal noise. Therefore, thermal noise is the main concern for RF CMOS operation. Nevertheless, for some RF applications such as mixers or oscillators where low frequency signal may be converted up to an intermediate or high frequency, and deteriorate the phase noise and signal-to-noise ratio.

2.1.1 Thermal Noise

Thermal noise is originated from the current fluctuation caused by collision of lattice and carriers by means of random thermal motion. Thermal motion of carriers is ubiquitous in any electronic components as long as its temperature is not absolute zero. Because of the thermal nature, thermal noise power turns out to be exactly proportional to temperature. Starting from the quantum theory of a harmonic oscillator, available noise power of thermal noise is given by [7]

$$P_{av} = [\frac{1}{2}hf + \frac{hf}{e^{(hf/kT)} - 1}] \cdot \Delta f \tag{2-2}$$

where h is Plank’s constant, k is Boltzmann’s constant, f is the operating frequency and Δf is the frequency interval. For $hf/kT << 1$ (holds for general case) and based on the noisy resistor model shown in Fig. 2.1, the mean-square open circuit noise voltage and noise current can be obtained.

$$P_{av} = kT\Delta f = \frac{\overline{v_n^2}}{4R} \tag{2-3}$$

$$\overline{v_n^2} = 4kTR\Delta f \tag{2-4}$$

$$\overline{i_n^2} = \frac{4kT\Delta f}{R} = 4kTG\Delta f \tag{2-5}$$

Every component with electrical resistivity can be considered as a resistor. With known resistance value or equivalent resistance, noise voltage or noise current can be calculated.

2.1.2 Thermal Noise in MOSFETs

In MOSFETs, noise components include channel noise (or called drain current noise), induced gate noise and thermal noise due to terminal parasitic resistances (Rg, Rd, Rs).

The most broadly accepted noise model for MOSFETs is the van der Zeil model [8]. For a MOSFET under operation, the conducting channel behaves like a voltage-controlled resistor. This resistor contributes thermal noise at the drain terminal. The power spectral density can be derived from the drain current expression. Refer to Fig. 2.2, taking velocity saturation into consideration, drain current at a certain position along channel direction is given by [7]

$$I_D(x) = W_{eff} \cdot Q_I(x) \cdot v(x) = \left(\mu_{eff} \cdot W_{eff} \cdot Q_I(x) - \frac{I_D(x)}{E_C} \right) \cdot \frac{dV}{dx} \tag{2-6}$$

Integrating this current over the effective channel L_{eff}, drain current can be obtained

$$I_D = \frac{1}{L_{eff}} \int_{V_S}^{V_D} \left(\mu_{eff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right) \cdot dV \tag{2-7}$$

The mean square values of a current fluctuation $\Delta i_d(t)$ caused by $\Delta v(t)$ in a unit length segment is

$$\overline{(\Delta i_d)^2} = \frac{1}{L_{eff}^2} \left(\mu_{eff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right)^2 \cdot \overline{(\Delta v)^2} \tag{2-8}$$

where $\overline{(\Delta \nu)^2}$ is

$$\overline{(\Delta v)^2} = \frac{4kT_e(x_i)\cdot \Delta x}{\left(\mu_{eff}\cdot W_{eff}\cdot Q_I(x_i) - \frac{I_D(x_i)}{E_C}\right)} \Delta f \tag{2-9}$$

Finally, power spectral density of the noise current generated by the channel resistance includes velocity saturation effect and hot-electron effects is given

$$S_{Id} = \frac{\overline{(i_d)^2}}{\Delta f} = \frac{4k}{L_{eff}^2 \cdot I_D}\int_{V_S}^{V_D} T_e(x)\left(\mu_{eff}\cdot W_{eff}\cdot Q_I(V) - \frac{I_D}{E_C}\right)\cdot dV \tag{2-10}$$

where T_e is the effective electron temperature in which hot-electron effect is considered. This is a general expression for the thermal noise in a channel. For simplicity it can be written as

$$S_{Id} = \frac{\overline{(i_d)^2}}{\Delta f} = 4kT\gamma g_{d0} \tag{2-11}$$

where g_{d0} is the drain transconductance at V_{DS} is zero. For long channel devices, γ is close to unity in its triode region and decreases to about 2/3 when in saturation (i.e. $\frac{2}{3} \leq \gamma \leq 1$). In long channel case, g_{d0} is equal to the gate transconductance g_m in saturation region which leads to a familiar result

$$S_{Id} = \frac{\overline{(i_d)^2}}{\Delta f} = \frac{8}{3}kTg_{d0} = \frac{8}{3}kTg_m \tag{2-12}$$

Due to the carrier heating by the large electric fields in short channel devices, γ may become larger than 2 and even larger.

Besides the channel current noise, the induced gate noise has gained increasing attention. As the operation frequency increases, contribution of this noise can not be neglected. Noise model including this terms, thus, become essential. Induced gate noise is, as implied by the name, the noise induced by capacitive coupling from channel region to gate terminal due to the fluctuating potential. This noise can be expressed as [9]

$$S_{Ig}=\frac{\overline{(i_g)^2}}{\Delta f}=4kT\gamma g_g \tag{2-13}$$

where g_g is given by

$$g_g=\frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{2-14}$$

Because the channel noise and induced gate noise have a common origin, they do have correlation. The correlation coefficient is usually expressed as

$$c=\frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}}\sqrt{\overline{i_d^2}}} \tag{2-15}$$

As for noise contributed from parasitic resistances, they follow (2-5) and are given by

$$S_{I,Rg}=\frac{4kT}{R_g};\ S_{I,Rd}=\frac{4kT}{R_d};\ S_{I,Rs}=\frac{4kT}{R_s} \tag{2-16}$$

Among them, due to the larger sheet resistance of poly-Si, gate resistance (R_g) is typically much larger than drain and source resistance (R_d and R_s). Therefore, R_g is an important noise contributor which can greatly affect the noise figure of the device. Multi-finger gate structure is widely used in RF MOSFET design to reduce R_g. Not only noise behavior, several characteristics are related to R_g too, in which maximum oscillation frequency (f_{max}) is one of the example. Multi-finger gate gain some performance but pay the penalty of larger parasitic capacitance.

2.2 Two-Port Noise Theory

2.2.1 Noise Figure

As mentioned above, overall noise of a device is generally not from a single origin. It does need a simpler measure of noise performance. For device characterization and circuit

design application, noise figure or noise factor is the most popular expression used. Based on the two-port noisy network model and definition of noise figure, formula of noise parameters can be derived.

Noise factor is defined as the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output.

$$F \equiv \frac{S_i/N_i}{S_o/N_o} \tag{2-17}$$

From this definition, we can understand that noise factor of a network depicts the degradation of signal-to-noise ratio as signal goes through this network. Considering a network with gain G and noise N_a, noise factor then can be express as

$$F \equiv \frac{S_i/N_i}{S_o/N_o} = \frac{S_i/N_i}{GS_i/(N_a+GN_i)} = \frac{N_a+GN_i}{GN_i} \tag{2-18}$$

where N_a and G are the noise power and gain of the network. From the expression shown above, noise factor can be defined as the ratio of total noise power at the output to the output noise power which is due to the input noise. In short, the larger noise factor means the noisier of the network. In (2-18), it shows the value of noise factor is affected by the input noise power which is generally from the thermal noise of the source, kTΔf. This means noise factor depends on the source temperature. 290K was adopted as a standard temperature by IEEE because it makes the value of kT close to around 4×10^{-21} Joule. Generally we use this measure in the unit of dB, named noise figure

$$NF = 10 \log F \tag{2-19}$$

2.2.2 Noise Parameters

Further detail derivation of noise factor based on the noise model with noise sources at the input leads to the following expression [10]

$$F = F_{min} + \frac{R_n \left| Y_s - Y_{opt} \right|^2}{G_s} \tag{2-20}$$

where

$$Y_s = G_s + j\,B_s \tag{2-21}$$

$$Y_{opt} = G_{opt} + j\,B_{opt} \tag{2-22}$$

Here Y_s is the source admittance, G_s is the real part of Y_s, Y_{opt} is the optimum source admittance, and F_{min} is the minimum noise factor achieved in the network when the source admittance Y_s is equal to Y_{opt}. R_n is named the equivalent noise resistance which indicates how sensitive the noise factor is when Y_s differs from Y_{opt}. Replacing the source admittance with its corresponding reflection coefficient at specific characterization impedance Z_0, another common form of noise factor is obtained

$$F = F_{min} + \frac{4R_n}{Z_0} \frac{\left| \Gamma_s - \Gamma_{opt} \right|^2}{(1 - \left| \Gamma_{opt} \right|^2) \left| 1 + \Gamma_{opt} \right|^2} \tag{2-23}$$

$$Y_{opt} = \frac{1}{Z_0} \frac{1 - \Gamma_{opt}}{1 + \Gamma_{opt}} \tag{2-24}$$

$$Y_s = \frac{1}{Z_0} \frac{1 - \Gamma_s}{1 + \Gamma_s} \tag{2-25}$$

This gives us an idea that the noise figure of the network is not only determined by noise source inside but also the source admittance (Y_s) driving it. It is also our goal to get the smaller noise factor while keep sufficient gain by varying Y_s. The so-called noise parameters are the four parameters F_{min}, R_n, $Re(\Gamma_{opt})$ and $Im(\Gamma_{opt})$. These parameters are determined purely by the intrinsic noise source of the network, they are unique under a certain operation frequency and bias. Typical dependence of noise figure on source admittance at a fixed

frequency and bias is a 3-D parabolic curve (x-y-z axis: Re(Γ_{opt})-Im(Γ_{opt})-F_{min}), R_n is the curvature. Fig. 2.3 and Fig. 2.4 give noise factor plotted with respect to Re(Γ_{opt}) and Im(Γ_{opt}) with F_{min} = 1, Re(Γ_{sopt}) = Im(Γ_{sopt}) = 0.1 and R_n = 100 and 50 (Ω) respectively. They give a simple idea about the noise figure characteristics.

2.3 Thermal Noise Model

There are two models for channel thermal noise model supported by BSIM3v3.2.2. One is SPICE2 noise model and the other is BSIM3v3 noise model. Noise model flag is defined to invoke different noise model sets [11]:

noimod flag	Flicker noise model	Thermal noise model
1	SPICE2	SPICE2
2	BSIM3v3	BSIM3v3
3	BSIM3v3	SPICE2
4	SPICE2	BSIM3v3

Noise model selection was done by parameter *noimod*. Both flicker noise and thermal noise can be calculated using SPICE2 or BSIM3v3 model. Detailed equations for flicker noise are not covered in this thesis and they can be referred to BSIM3v3 manual. Another noise model supported by many simulators is the HSPICE model. In Agilent-ADS simulator, BSIM3 model selected by *noimod* is valid when *NLEV* < 1 or HSPICE model will be used according to *NLEV* values (*NLEV*=1, 2, or 3). In models mentioned above, velocity saturation and the hot-electron effect model which are considered as two important effects in sub-micron transistors were not included.

SPICE2 Model

For *noimod* = 1 or 3, thermal noise is calculated according to [12]

$$S_{Id} = \frac{8kT}{3}(g_m + g_{ds} + g_{mbs}) \tag{2-26}$$

This model is the modification of old HPSICE model shown below as with *NLEV* < 3, which improves the model accuracy in linear region.

BSIM3v3 Model

If *noimod* = 2 or 4, thermal noise power spectral density is calculated by [13]

$$S_{Id} = \frac{4kT\mu_{eff}}{L_{eff}^2}\left|Q_{inv}\right| \tag{2-27}$$

where Q_{inv} is the channel inversion charge calculated according to the capacitance models (*capMod*=0, 1, 2, or 3).

HSPICE Model

The HSPICE noise model has different equations to calculate the flicker and thermal noises. Equation selection is through a parameter, *NLEV*. For *NLEV* smaller than 3, different flicker noise model was used but the same thermal noise equation was implemented which is given by [14]

$$S_{Id} = \frac{8kT \cdot g_m}{3} \tag{2-28}$$

which is an old model and is lack of accuracy for modern devices.

If *NLEV* is set to 3, the noise equation is then given by [13]

$$S_{Id} = \frac{8kT}{3}\cdot\beta\cdot(V_{GS}-V_T)\cdot\frac{1+a+a^2}{1+a}\cdot Gdsnoi \tag{2-29}$$

where

$$\beta = \frac{W_{eff}}{L_{eff}}\cdot\mu_{eff}\cdot C_{ox} \tag{2-30}$$

$$\begin{aligned} a &= 1-\frac{V_{DS}}{V_{DSAT}}, \quad \text{Linear region} \\ &= 0, \quad \text{Saturation region} \end{aligned} \tag{2-31}$$

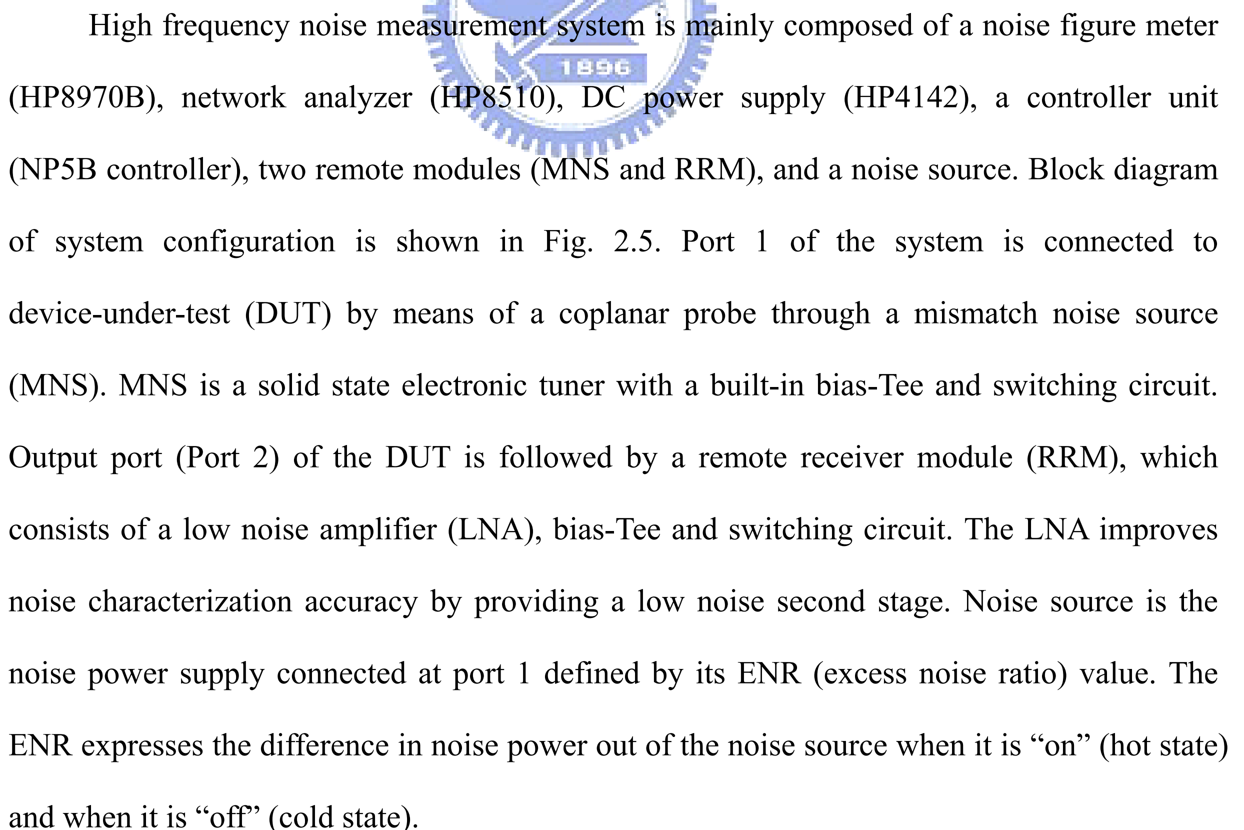
and *Gdsnoi* is the thermal noise coefficient with default value equal to 1.

Models mentioned above are integrated into various commercial simulators. Many other models have been proposed to consider velocity saturation effect, hot-electron effect or both [4, 5]. But they are not yet well accepted and verified. Noise simulation result comparison of different models was done in [15]. In this thesis, HSPICE model with *NLEV* set to 3 was used.

2.4 High Frequency Noise Measurement

In this work, high frequency noise measurement was supported by Radio Frequency Technology Center of National Nano Device Laboratory (NDL RFTC). On-wafer noise characterization was conducted using NP5 series noise parameter measurement system. The measurement system is introduced as follows.

2.4.1 System Configuration [16]



High frequency noise measurement system is mainly composed of a noise figure meter (HP8970B), network analyzer (HP8510), DC power supply (HP4142), a controller unit (NP5B controller), two remote modules (MNS and RRM), and a noise source. Block diagram of system configuration is shown in Fig. 2.5. Port 1 of the system is connected to device-under-test (DUT) by means of a coplanar probe through a mismatch noise source (MNS). MNS is a solid state electronic tuner with a built-in bias-Tee and switching circuit. Output port (Port 2) of the DUT is followed by a remote receiver module (RRM), which consists of a low noise amplifier (LNA), bias-Tee and switching circuit. The LNA improves noise characterization accuracy by providing a low noise second stage. Noise source is the noise power supply connected at port 1 defined by its ENR (excess noise ratio) value. The ENR expresses the difference in noise power out of the noise source when it is “on” (hot state) and when it is “off” (cold state).

2.4.2 System Calibration and Measurement

As high frequency characterization was conducted on the devices (DUT), the applied signals with short wavelength are comparable to the probe, connecting cables, adapters, bonding wires, and our interested device. Thus, losses caused by the connections will remarkably affect the measurement results, especially critical as measurement frequency increases. On the other hand, a measurement system has its own system error. Consequently, a system calibration should be performed to take those losses into consideration, calibrate the system errors and then shift the measurement signal reference plane to the DUT plane. The validity and accuracy of the calibration results depend on the calibration method used.

For S-parameter measurement, SOLT (short-open-load-through) calibration is a popular method to establish the DUT test plane nowadays. For the noise measurement system, there are several calibration steps required to build a noise measurement plane for DUT. A complete calibration procedure includes input SOL calibration, noise source calibration, network analyzer calibration, thru delay calibration, RRM calibration, MNS calibration and finally system noise parameter calibration. Since calibration details are not our focus, only rough idea is provided here. After the overall calibration procedure, noise contribution of the system will be characterized. Thus, real noise power of DUT can be separated from the noise power contributed from system. This can be verified by connecting the input and output with a known DUT, in our case a dummy “thru” pattern was used to check if the noise figure is less than 0.1dB.

After calibration, noise measurement reference plane is then established. In the beginning of noise parameter characterization, S-parameters measurement at the DUT reference plane should be done first. In the following, by varying the impedance presented to the input of the DUT around the Smith chart, output noise power (sometimes, also refers to noise temperature) of DUT plus the receiver as a function of Γ_s (source reflection coefficient)

was measured, each Γ_s and the corresponding noise power constructs a set of equations. The noise parameters are decided by solving the set of equations. Theoretically speaking, only four input states are needed for noise characterization because the noise behavior equation (2-23) has merely four unknown parameters. In practice, however, for the sake of reducing the influence of random errors more than four points were measured (generally 16 states or 20 states) and a proper fitting procedure was used to extract the parameters. Finally, four noise parameters: NF_{min}, R_n, Re (Γopt) or Re (Yopt) and Im (Γopt) or Im (Yopt) are obtained.

In the measurement process, the overall noise figure was calculated by Y-factor method technique. The overall noise figure is then under a noise figure correction step to determine the noise figure of the DUT. Details of Y-factor method and noise figure correction are included in Appendix B.

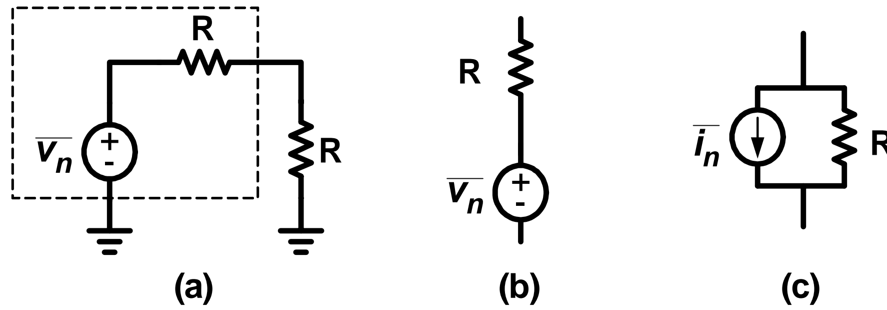


Fig. 2.1 (a) Equivalent network for computing thermal noise of a resistor.(b)(c) Thermal noise model for a resistor.

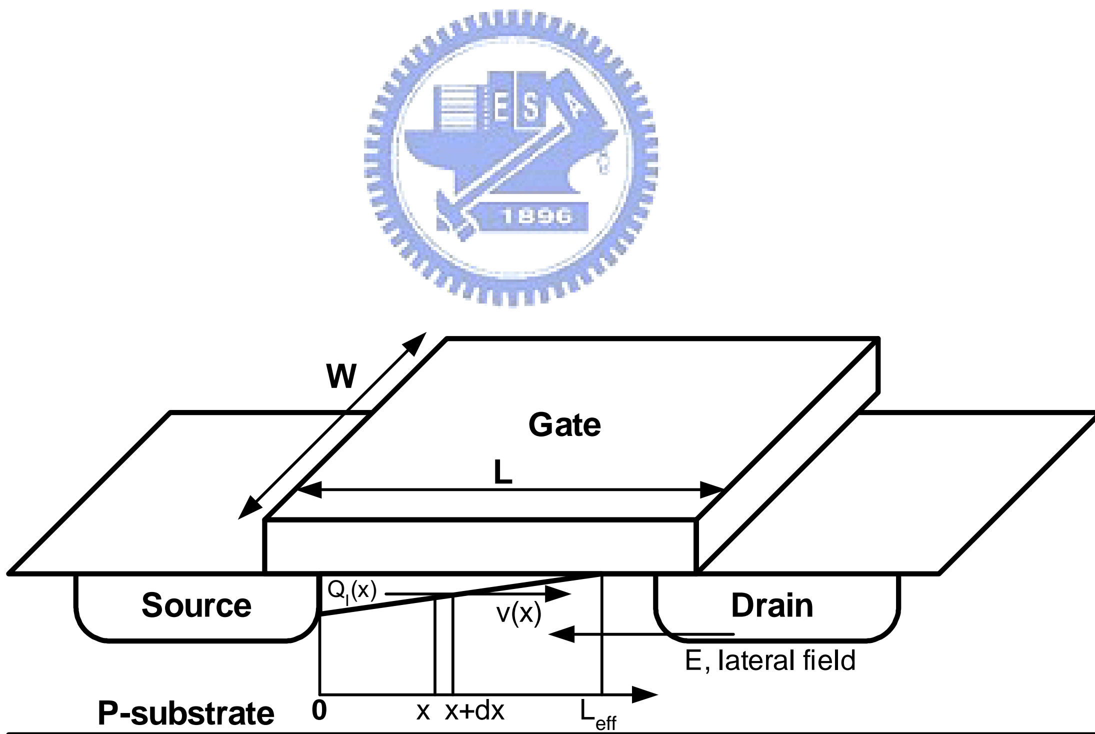
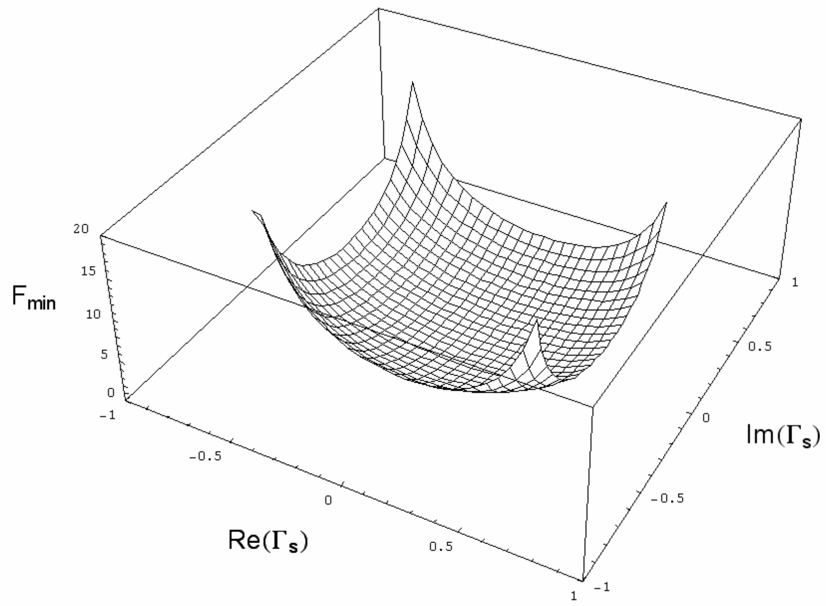
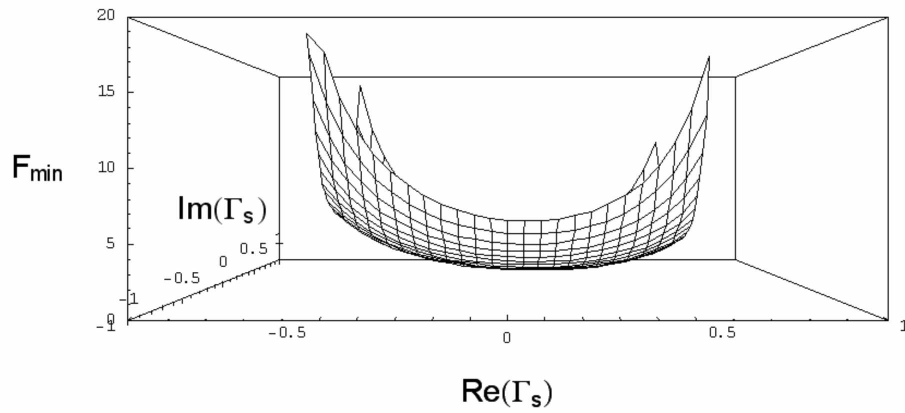


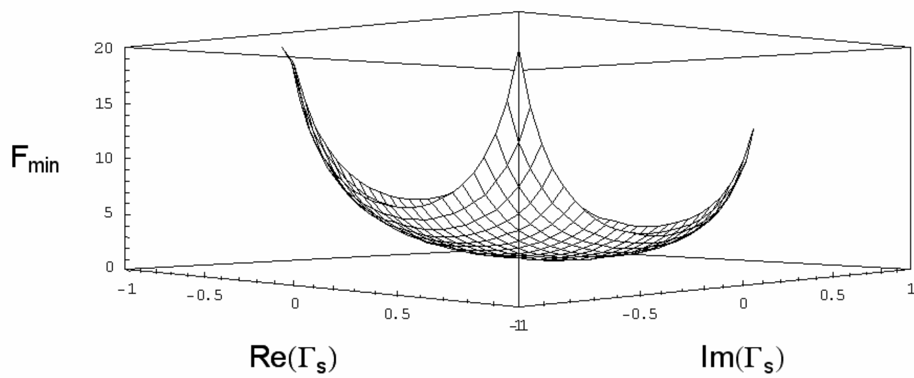
Fig. 2.2 Schematic diagram of a MOSFET operated in saturation condition.



(a)

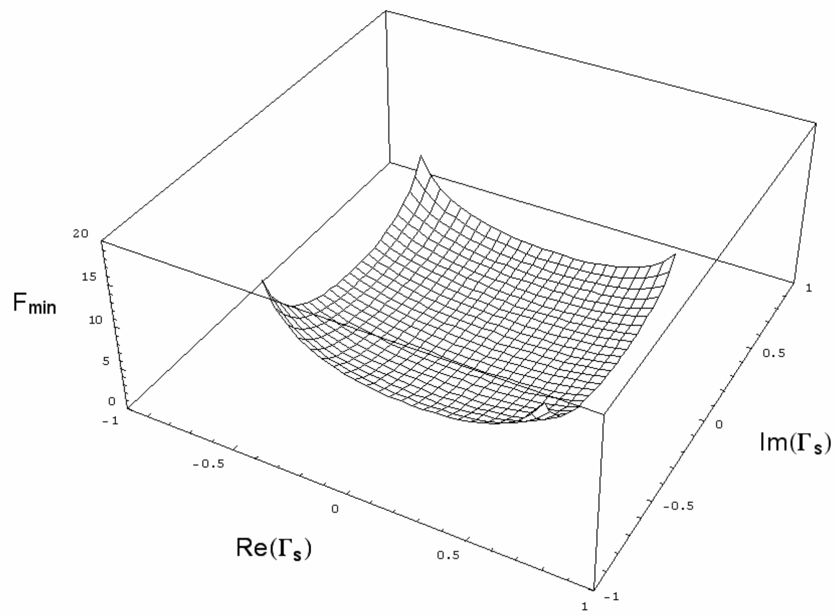


(b)

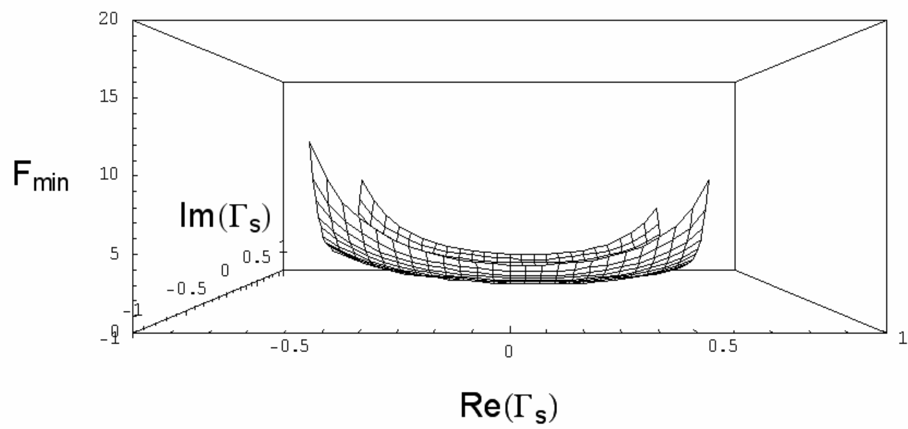


(c)

Fig. 2.3 (a)(b)(c) noise figure F plotted with respect to $Re(\Gamma_{opt})$ and $Im(\Gamma_{opt})$ with $F_{min} = 1$, $Re(\Gamma_{sopt}) = Im(\Gamma_{sopt}) = 0.1$ and $R_n = 100$.



(a)



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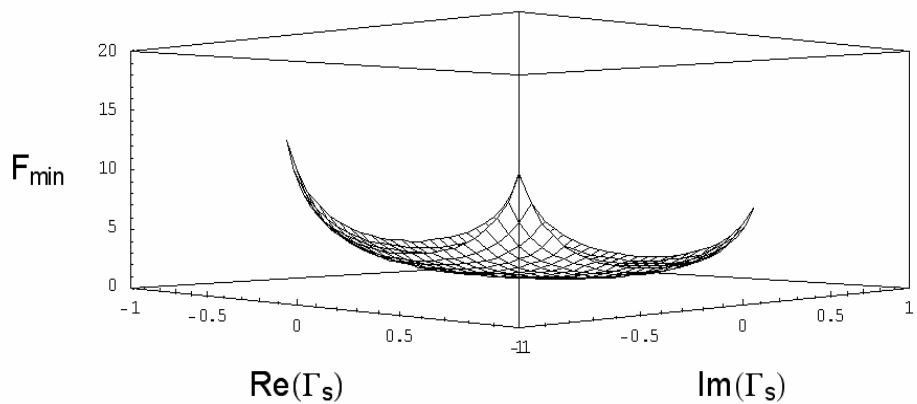


(c)

Fig. 2.4 (a)(b)(c) noise figure F plotted with respect to $Re(\Gamma_{opt})$ and $Im(\Gamma_{opt})$ with $F_{min} = 1$, $Re(\Gamma_{sopt}) = Im(\Gamma_{sopt}) = 0.1$ and $R_n = 50$.

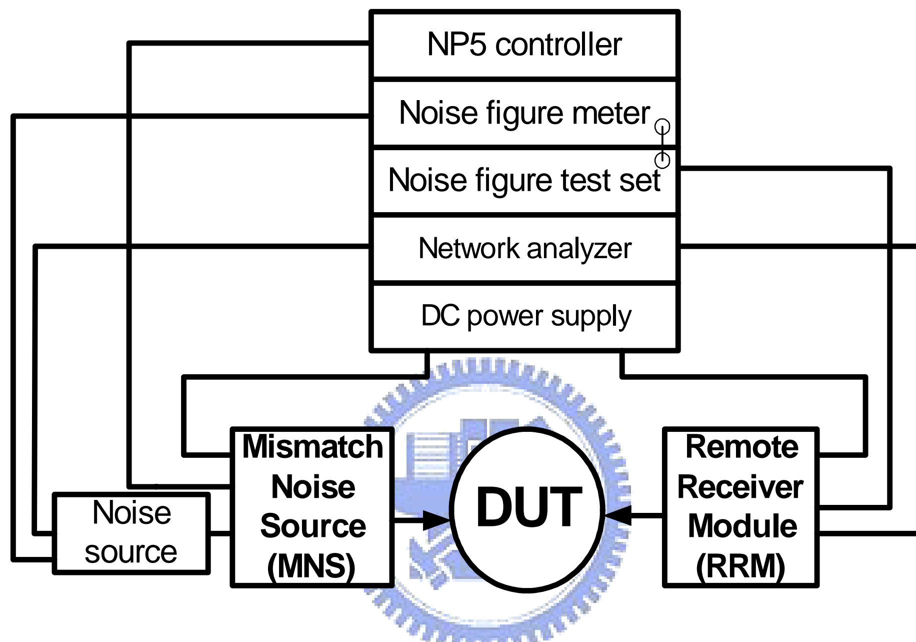


Fig. 2.5 Block diagram of ATN noise figure measurement system configuration.

Chapter 3

RF MOSFET Noise Characterization

3.1 Extrinsic Noise Characteristics

RF MOSFETs with 80nm and 65nm gate length were fabricated to study the nanoscale CMOS scaling effect on speed and noise performance. Multi-finger structure with fixed finger width (4μm) and various finger numbers (N_F=6, 18, 36, 72) are employed to reduce the gate resistance. Reduction of gate resistance shows no impact on cut-off frequency (f_T)

$$f_T = \frac{g_m}{2\pi\sqrt{C_{gg}^2 - C_{gd}^2}} \quad (3\text{-}1)$$

while other RF performance can be improved such as maximum oscillation frequency (f_{max}) and noise figure (NF_{min}) [17,18]. Fig. 3.1 indicates R_g extracted from Z-parameters and gate capacitances (C_g) extracted from Y-parameters for various finger numbers. It shows a trade-off between R_g and C_g (C_{gd}, C_{gs}).

Measured NF_{min} for 65nm and 80nm nMOS of various N_F are shown in Fig. 3.2 (a) and (b). One is biased under maximum g_m (Vgs = 0.7V for 80nm and Vgs = 0.6V for 65nm) which is corresponding to maximum f_T, the other is biased under minimum NF_{min} (Vgs = 0.55V for 80nm and Vgs = 0.35V for 65nm). They indicate there is certain gate voltage difference between maximum f_T and minimum NF_{min}. NF_{min} without de-embedding decreases remarkably with increasing N_F. One reason is the Rg reduction due to increase multi-finger gate number, however, this can not explain the dramatic difference such as 2.5~3dB between N_F = 6 and N_F = 72 in frequency range of 5~18GHz.

Fig. 3.3 illustrates the f_T extracted from extrapolation of $|H_{21}|$ to unity gain. R_g is decreasing as N_F increases at the expense of larger gate capacitance. (3-1) shows f_T is

dependent on g_m and gate capacitance. Both g_m and C_g are nearly proportion to the finger number, thus lead to weak dependence on N_F for f_T at around 100~105GHz for 80nm device. Scaling from 80nm to 65nm in gate length, about 20~30% increase in driving current and maximum transconductance and 20% reduction in gate capacitance lead to obvious 50~60% improvement in maximum f_T. The improvement indicates the advantage provided by device scaling for high speed CMOS applications. However, measured NF_{min} of these two sets of devices did not show significant difference.

Three interesting features are revealed in measured noise in Fig. 3.2. Firstly, there is an abnormal strong dependence on finger number while f_T is almost the same thought R_g is reduced. Secondly, weak dependence on gate length was observed even gained 50% f_T improvement. The last is the nonlinear frequency dependence of NF_{min} which can not be explained by the theoretical thermal noise behavior. As expressed in equivalent circuit element, NF_{min} was shown to be linearly dependent on frequency [18-20]. Consequently, it is suggested that lossy pad and lossy substrate contribute to these excess noise. Noise is coupled from the lossy substrate through capacitive probing pad and interconnects transmission line. To understand the pure noise behavior (intrinsic) of the DUT and further to model it, noise de-embedding on the measured one is indispensable.

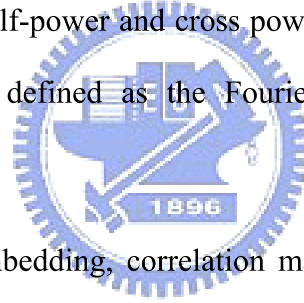
3.2 Conventional Noise De-embedding Method

Conventionally, there are two ways to characterize the intrinsic noise performance of MOSFET transistors. One is by directly de-embedding the external noise through matrix calculation that is similar to the S-parameter de-embedding but much more complicated. This popular technique is called noise correlation matrix de-embedding. The other method is to extract intrinsic noise parameters through the approach of equivalent circuit model. This is a new method developed in this study. By equivalent circuit implementation, measured noise parameters can be simulated and noise caused by probing pad can also be characterized. The

details will be described in chapter 5.

3.2.1 Noise Correlation Matrix De-embedding

According to the circuit theory of linear noisy networks, any two-port device can be separated into two parts: additional noise source part and noiseless device part. For common application three equivalent representations are used to describe the two-port devices, they are admittance, impedance, chain representation respectively [21]. Generally, chain representation is used mostly in which a voltage noise source and a current noise source are included. Chain representation of a noisy two-port network is shown in Fig. 3.4. The benefit of the representation is that it is easier to find the relation of input signal and noise level because it refers the entire device noise source to the input. Correlation matrices are described with the noise sources in the form of self-power and cross power spectral densities as matrix element. Power spectral densities are defined as the Fourier transform of their auto and cross correlation function.



To perform noise de-embedding, correlation matrices of the two-port circuit and the decomposed components should be known. The matrices are obtained from the measured noise parameters or calculated theoretically based on the physics (such as those passive elements). The noise parameters of a passive device are fully determined by its small-signal parameters. For an element with admittance Y, the correlation matrix is given in the form of

$$C_Y = 2K_B T \cdot \mathrm{Re}[Y] \tag{3-1}$$

Chain representation of the whole test fixture is estimated from the measured noise parameter (NF_{min}, R_n, Y_{opt}).

$$[C_A] = 2K_B T \begin{pmatrix} R_n & \dfrac{F_{min}-1}{2} - R_n Y_{opt} \\ \dfrac{F_{min}-1}{2} - R_n Y^{*}_{opt} & R_n |Y_{opt}|^2 \end{pmatrix} \tag{3-2}$$

Once the correlation matrices are known, according to the configuration of the two-port network, transformation of correlation matrices should be done. Appropriate matrix operation is applied to isolate the parasitic parts form the intrinsic correlation matrix. Noise parameters after de-embedding, called intrinsic noise parameters, and then could be computed as function of correlation matrix

$$F_{\min,DUT} = 1 + \frac{\mathrm{Re}[C_{A,12,DUT}]}{k_B T} + \frac{\sqrt{C_{A,11,DUT} C_{A,22,DUT} - (\mathrm{Im}[C_{A,12,DUT}])^2}}{k_B T} \tag{3-3}$$

$$Y_{sopt,DUT} = G_{sopt,DUT} + \mathrm{I} * B_{sopt,DUT} = \frac{\sqrt{C_{A,11,DUT} C_{A,22,DUT} - (\mathrm{Im}[C_{A,12,DUT}])^2} + \mathrm{I} * \mathrm{Im}[C_{A,12,DUT}]}{C_{A,11,DUT}} \tag{3-4}$$

$$R_{n,DUT} = \mathrm{Re}[\frac{C_{A,11,DUT}}{2k_B T}] \tag{3-5}$$

Details of correlation matrices de-embedding procedure are included in Appendix B.

3.2.2 De-embedding Results

For the purpose of studying the correlation matrix de-embedding on different devices. Three test-keys with different probing pad layout structures were implemented. The first one is 0.13µm low voltage technology (013LV) adopted for fabrication of 80nm and 65nm nMOS. The second one is RF CMOS technology using 0.13µm general purpose process (013G) with device target gate length at around 105nm. The last one is also a 0.13µm general purpose technology with target gate length at around 110nm. The three sets of DUT are all nMOS devices but with different probing pad layout structures. Details of these test structures will be discussed in Chapter 5 where the corresponding equivalent circuit will be introduced.

De-embedding work was done by writing equations in ADS data display window. The correlation matrix de-embedding results are shown in Fig. 3.5 ~ Fig. 3.7. In Fig. 3.5(a), NF_{min} after matrix de-embedding show great amount of reduction and almost the same level for

various N_F devices. But decrease of NF_{min} with increasing frequency in lower frequency region (3~5GHz) fails to follow the linear frequency dependence. Reduction of R_n is decreasing as N_F increases. The results suggest that more parasitic effect was originally suffered by smaller device, i.e. $N_F = 6$ than $N_F = 72$, and can be eliminated through de-embedding. Reduction of real part of optimum source admittance, $Re(Y_{sopt})$ was also appreciable and this also relates to the reduction of NF_{min}. Fig. 3.6 is the comparison of de-embedding results for lossy pad and normal pad test structures. Much more noise reduction for lossy pad than normal pad was observed. It suggests effective de-embedding realized for lossy pad. However, frequency dependence issue as shown in Fig. 3.5 still remains. As for pad structure with poly ground shielding under signal pad, less substrate coupling effect leads to small difference between as-measured data and de-embedded results.

In summary, no need to establish an equivalent circuit model required for the matrix correlation method makes it convenient to calculate the intrinsic noise parameters from the measured ones. But there are three major drawbacks make this method not that popular. Firstly, the data after de-embedding usually suffer severe fluctuation due to its limited measurement precision, i.e., de-embedded results are very sensitive to measured data accuracy, especially for novel devices with noise figure below 1dB. The second one is its critical dependence on open pad test structure design and limitation in fully extracting the TML induced extra coupling noise provided that it lacks of ground shielding. The last one drawback is its failure of full range coverage for circuit design application. Because noise parameters and S parameters corresponding to arbitrary biases or frequencies can not be predicted from the measured data limited to certain specified bias and frequency.

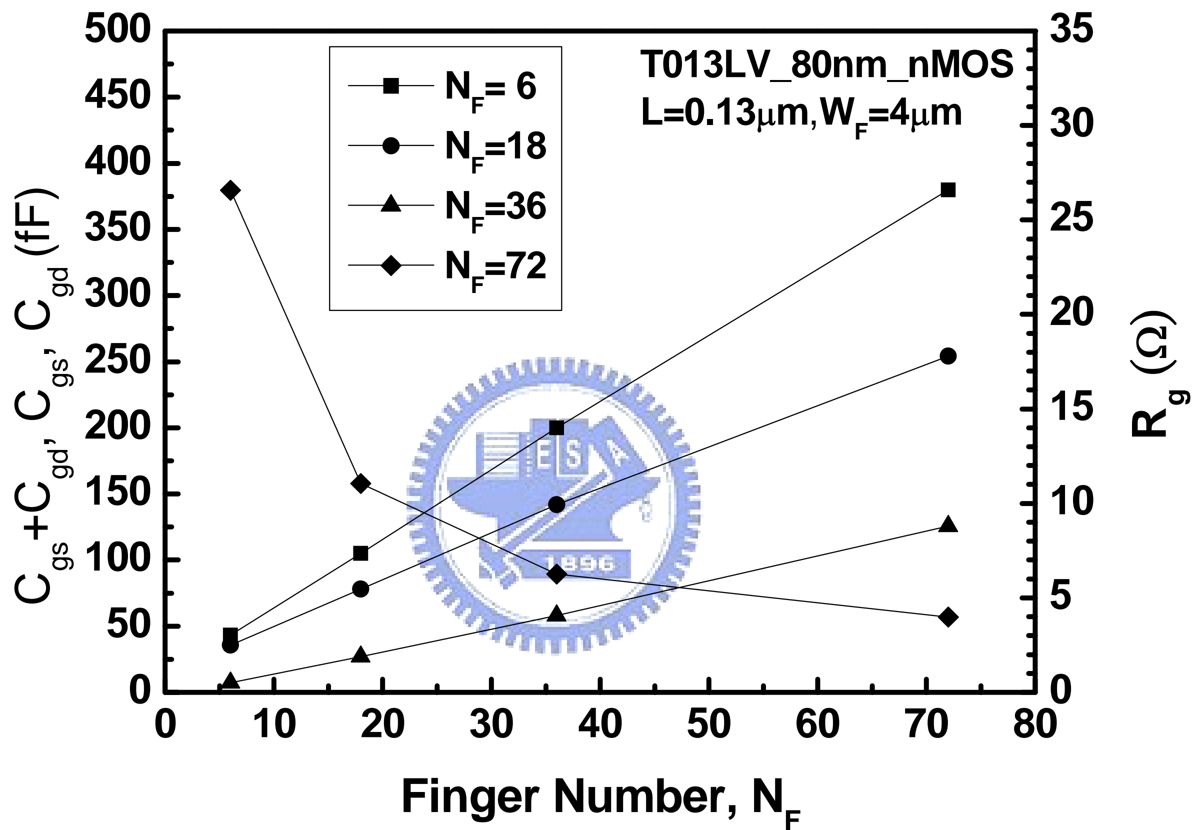
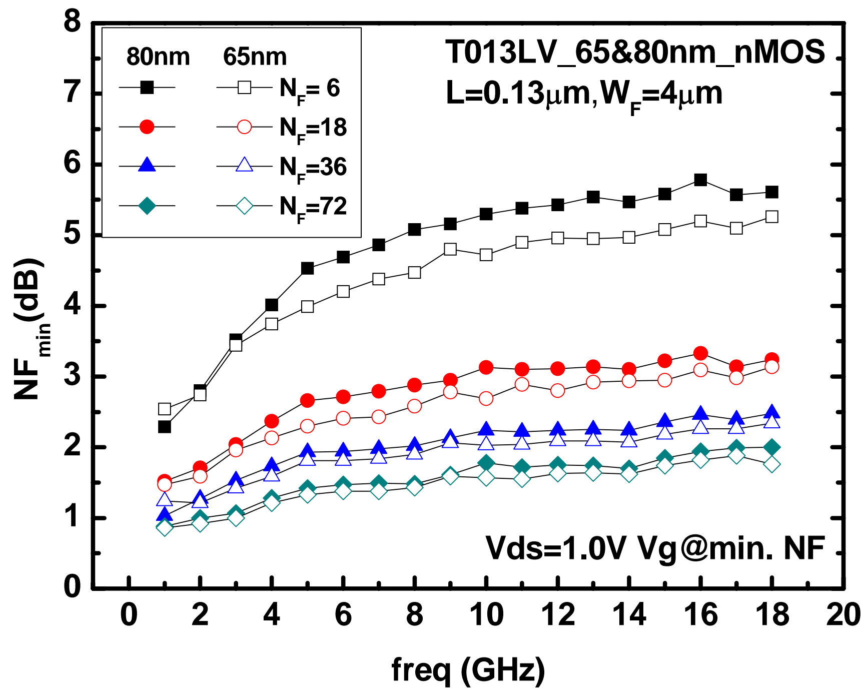
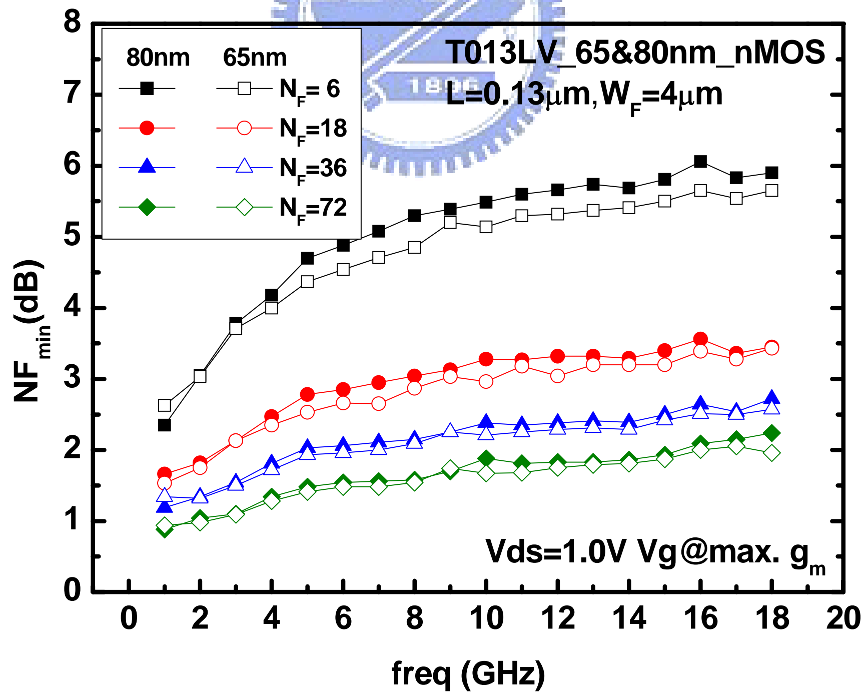


Fig. 3.1 80nm nMOS Rg and C_g (C_{gs}, C_{gd}, C_{gd}) extracted from Z- and Y- parameters. ($N_F = 6$, 18, 36, 72)



(a)



(b)

Fig. 3.2 Measured noise figure NF_{min} of 80 and 65nm nMOS for N_F = 6, 18, 36, 72 (a) Vd=1V, Vg at min. NF_{min} (Vgs=0.7/0.6V)(b) Vd=1V, Vg at max. g_m (Vgs=0.5/0.35V).

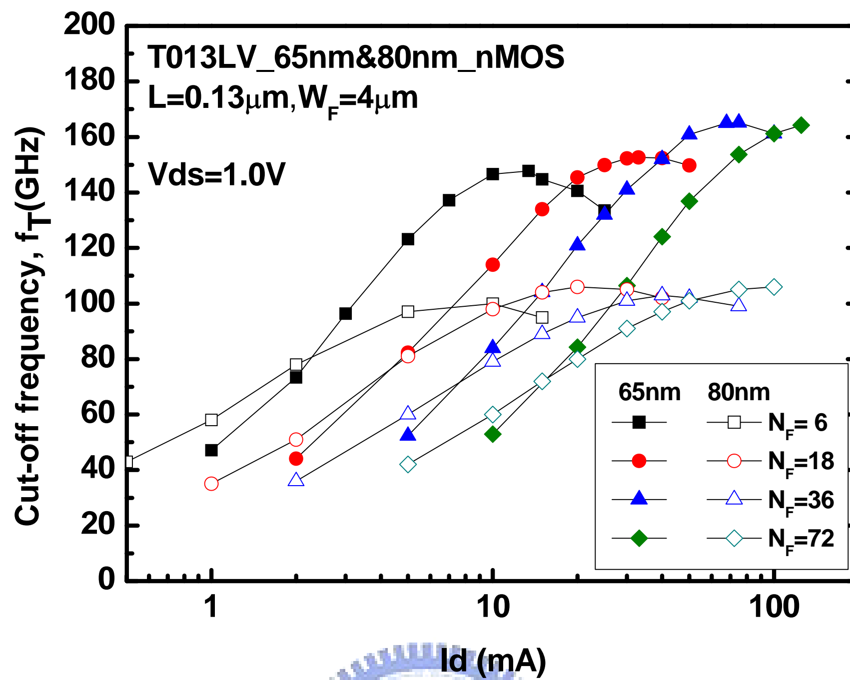


Fig. 3.3 Cut-off frequency f_T of 80 and 65 nm nMOS under various drain current extracted from extrapolation of $|H_{21}| = 1$.

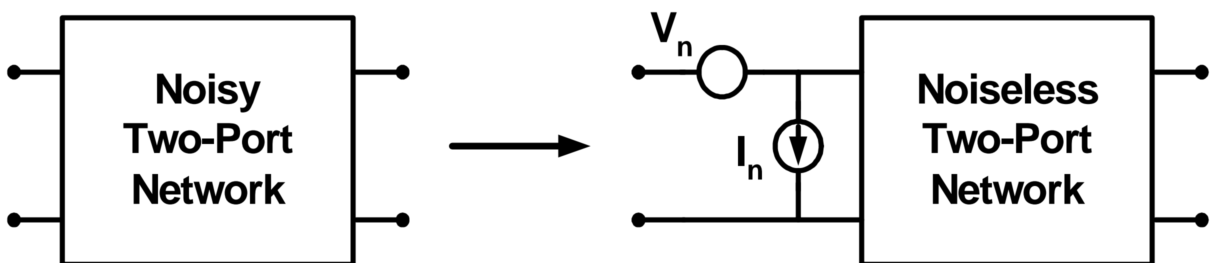
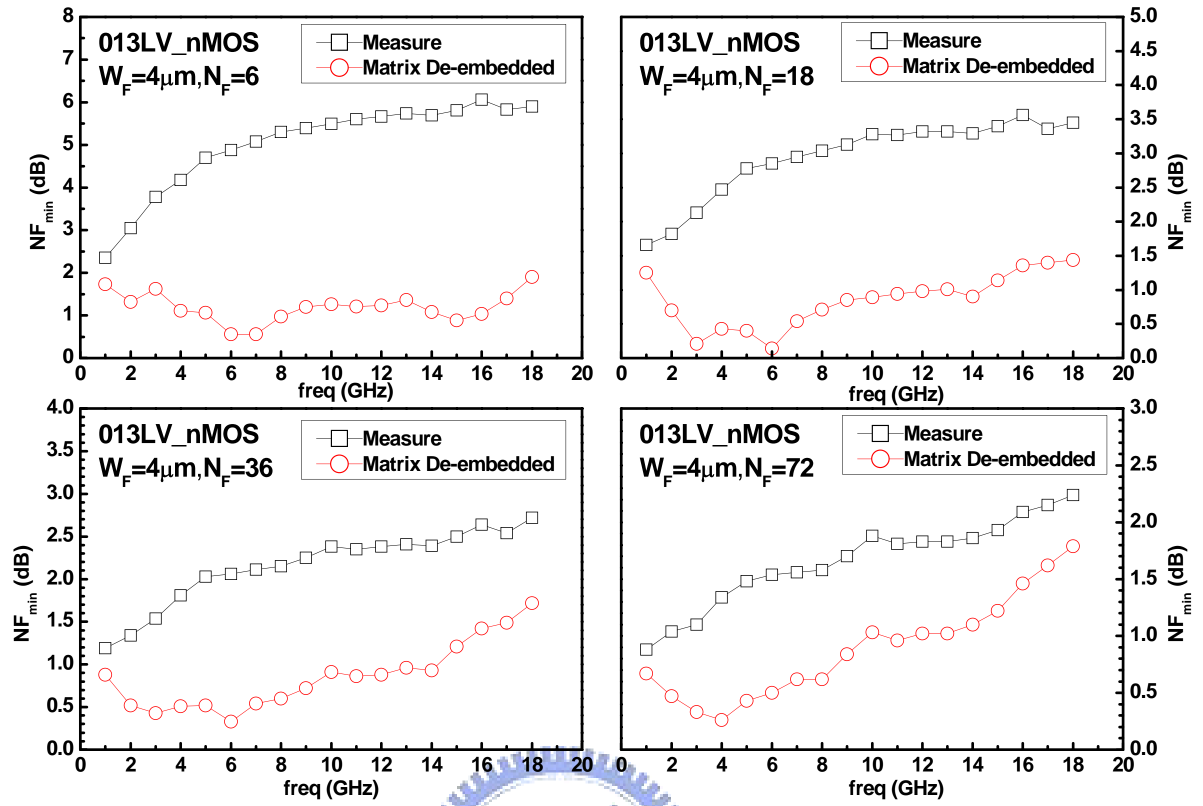
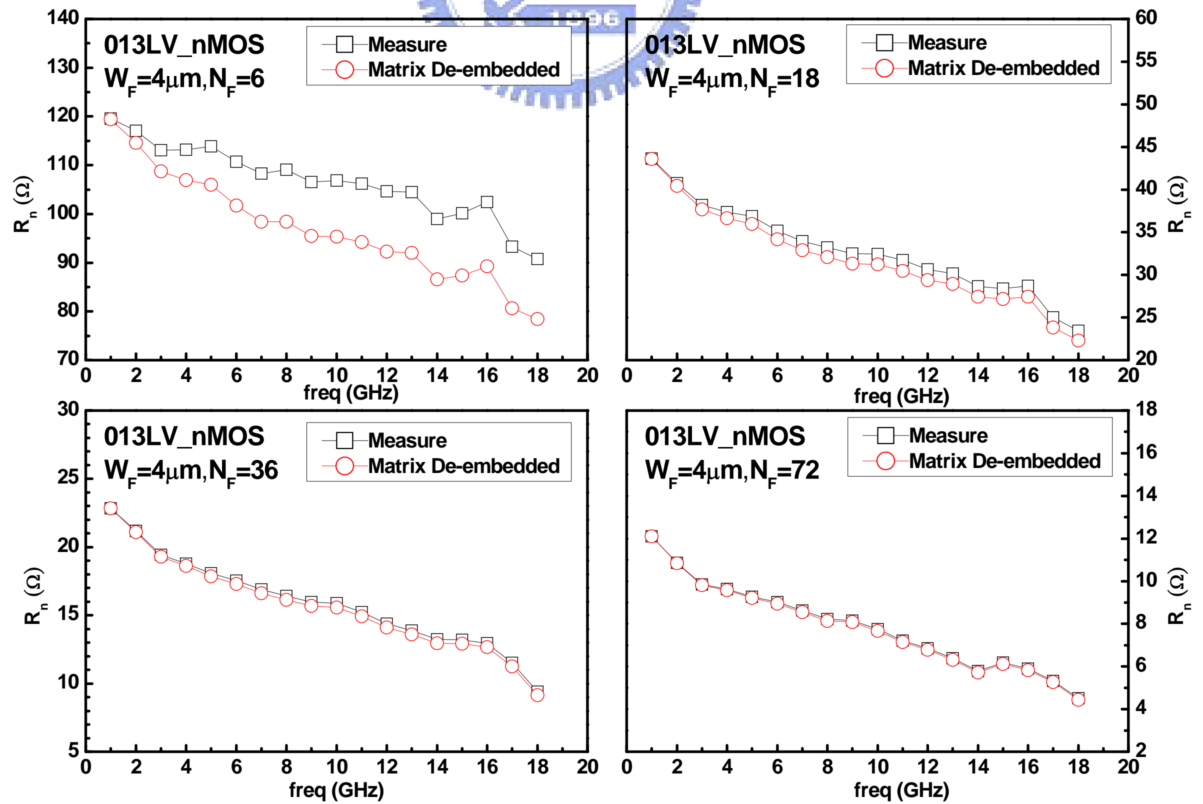


Fig. 3.4 Chain representation of a noisy two-port network with a voltage source and a current source in the input port.



(a)



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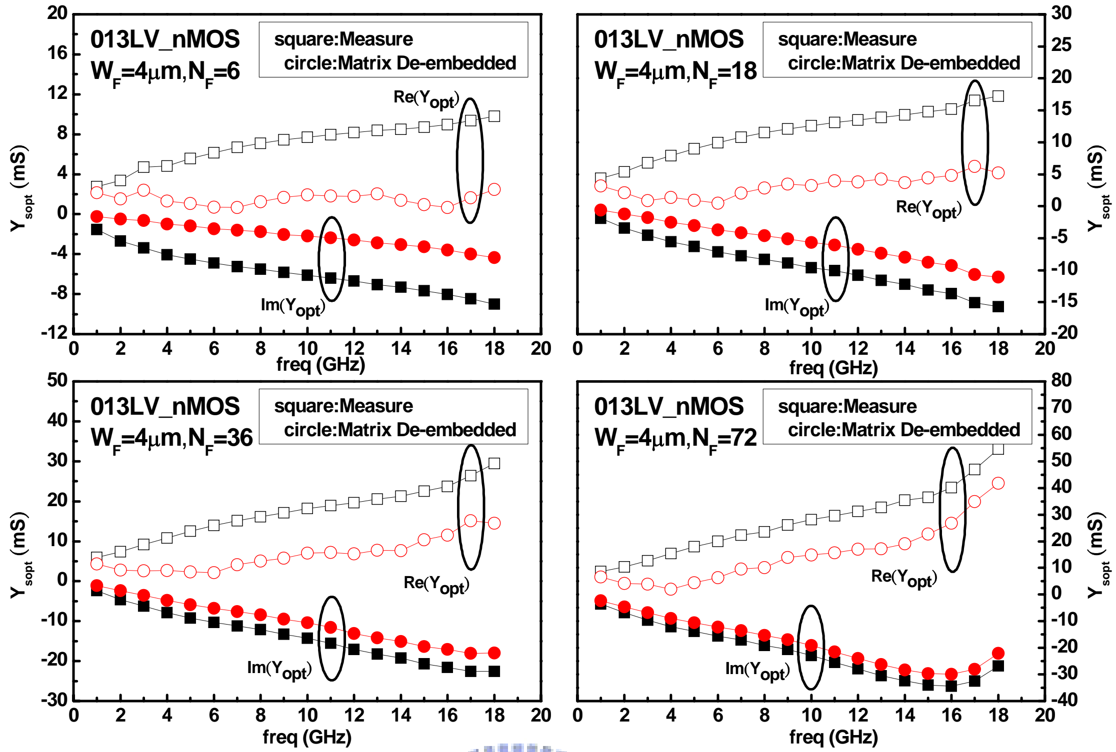
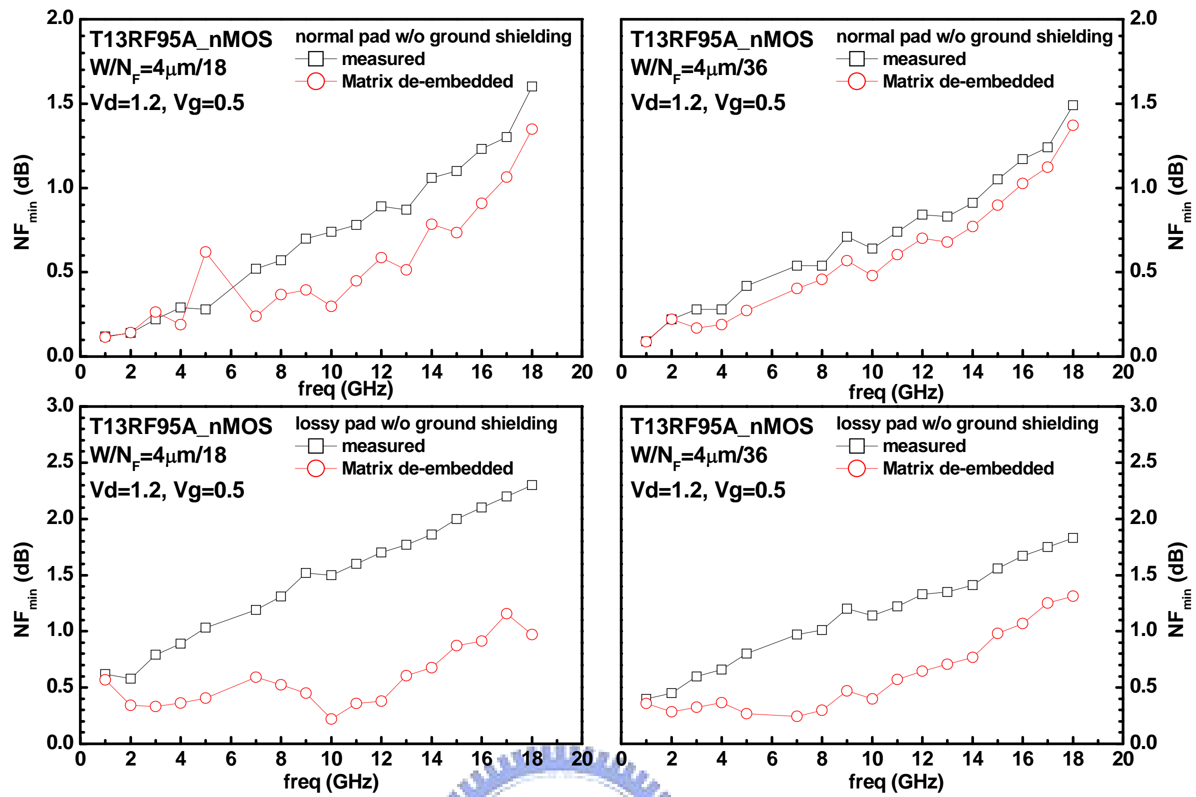
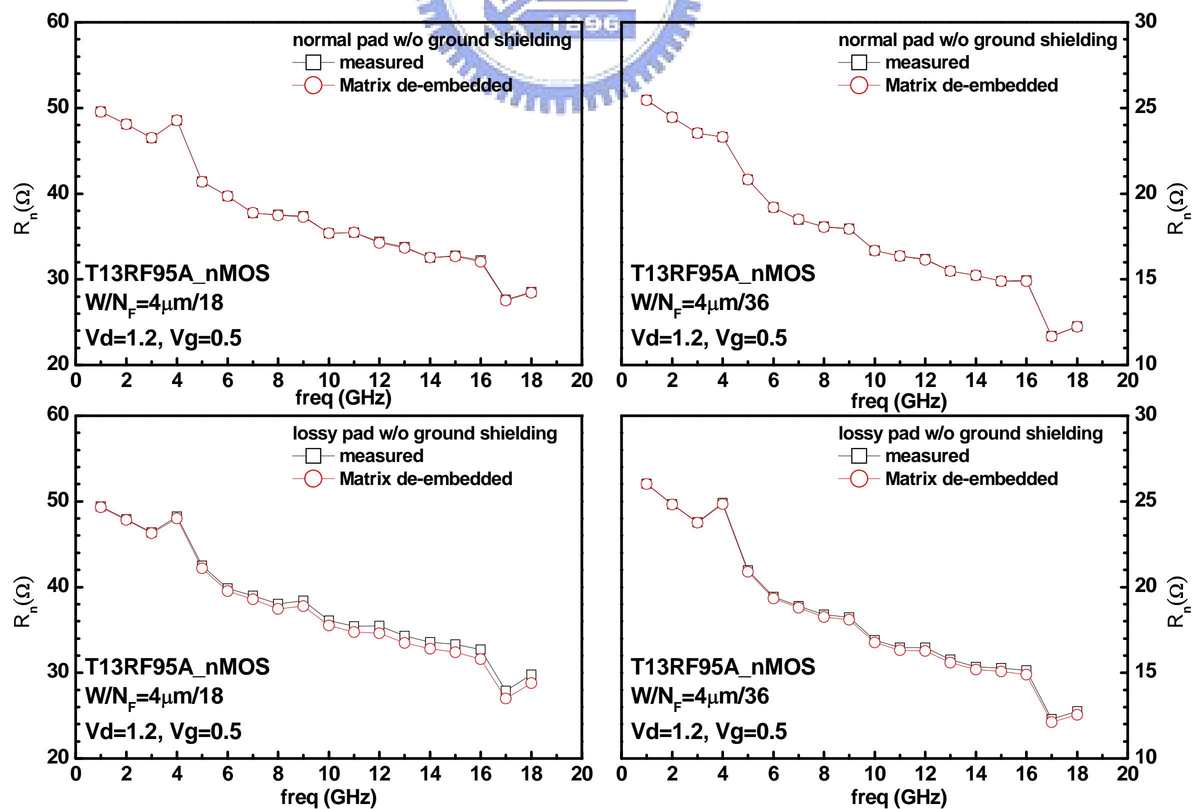


(c)

Fig. 3.5 0.13μm LV tech. 80nm nMOS N_F = 6, 18, 36, 72 biased at Vd = 1V and Vg = 0.7V. Pad layout without metal line and poly-ground shielding under signal pad. Signal pad metal stacking is from M2 to M8. Comparison of noise parameters between as-measured and after correlation matrix de-embedded. (a) NF_{min} (b) R_n (c) Re(Y_{sopt}) and Im(Y_{sopt})



(a)



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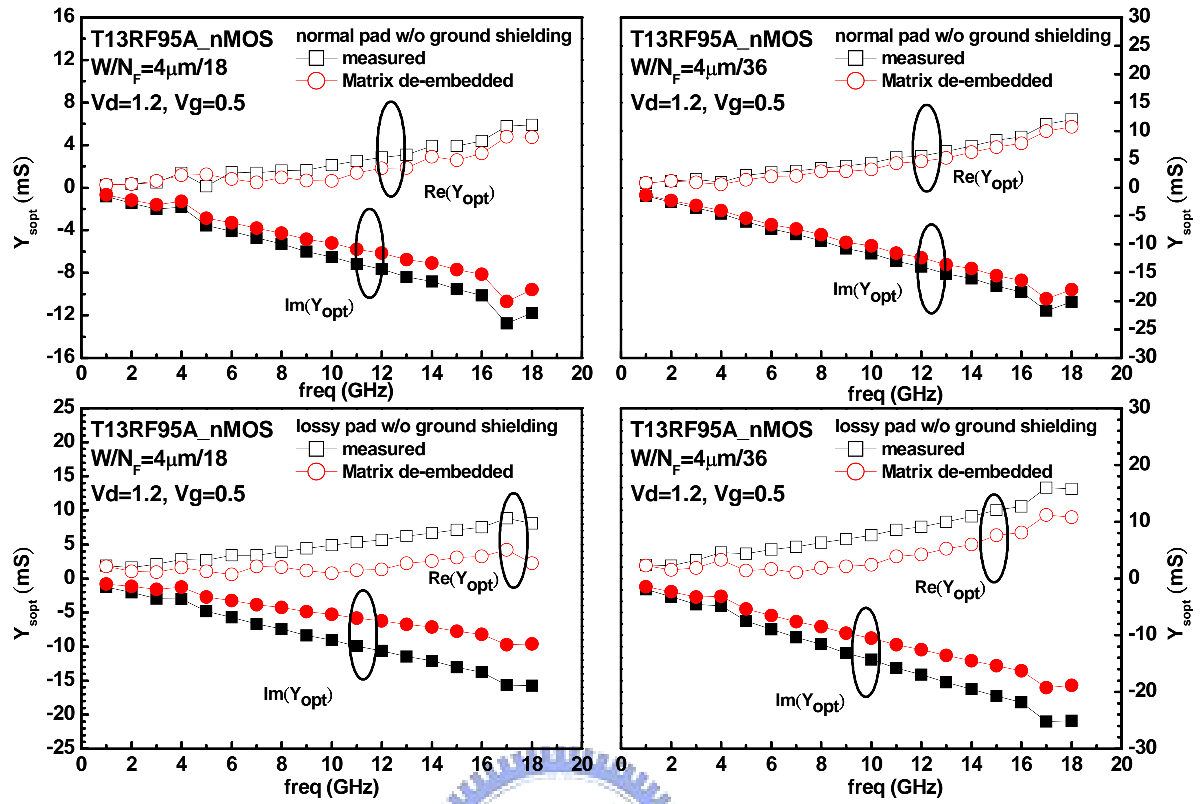
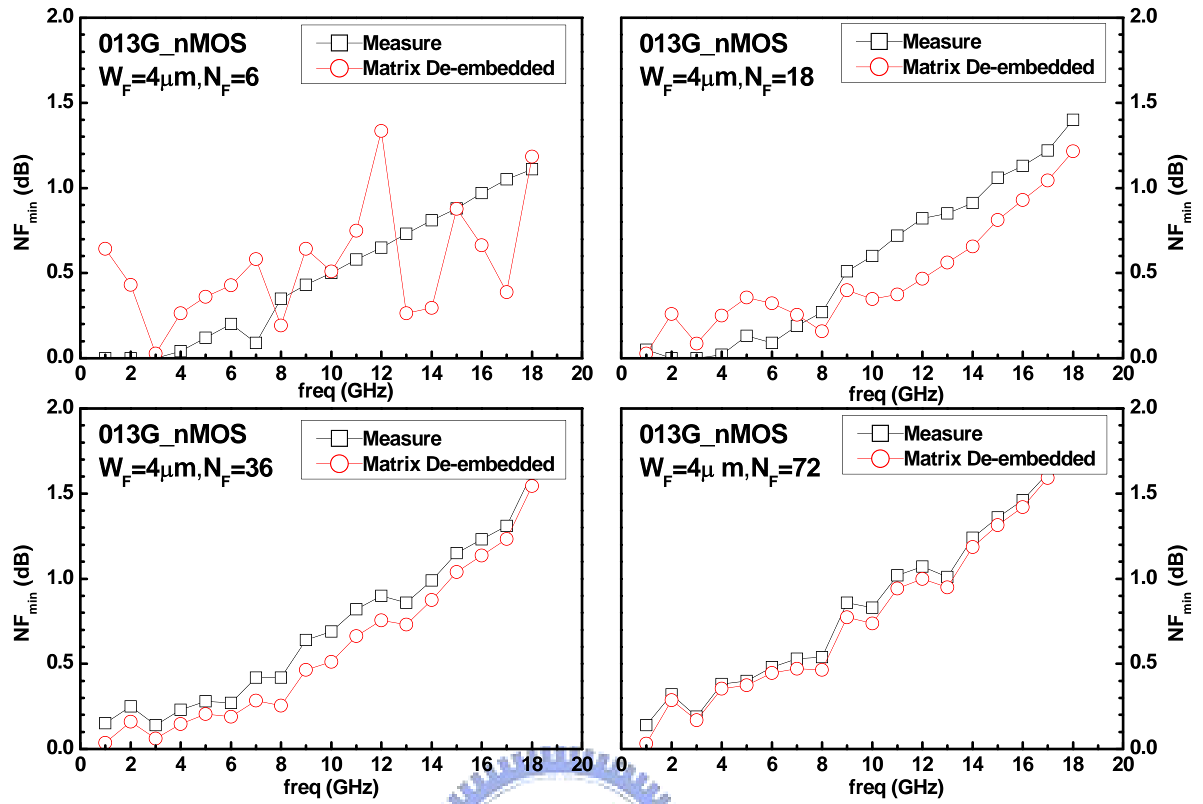


(c)

Fig. 3.6 0.13μm MS/RF tech. nMOS with N_F =18, 36, 72 biased at Vd = 1.2V and Vg = 0.5V. Pad layout without poly-ground shielding under signal pad. Two signal pad metal stacking are from M2 to M8 (called lossy pad) and only top metal M8 (normal pad). Comparison of noise parameters between as-measured and after correlation matrix de-embedded. (a) NF_{min} (b) R_n (c) $Re(Y_{sopt})$ and $Im(Y_{sopt})$



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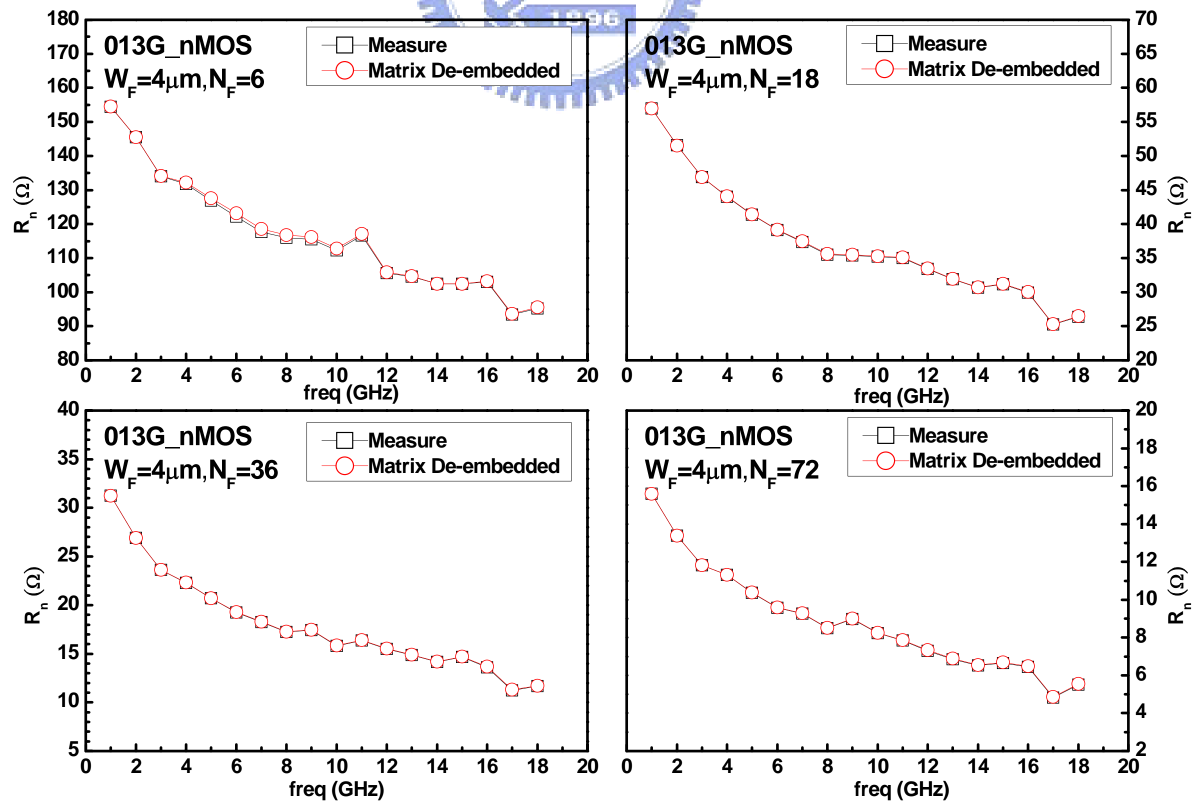

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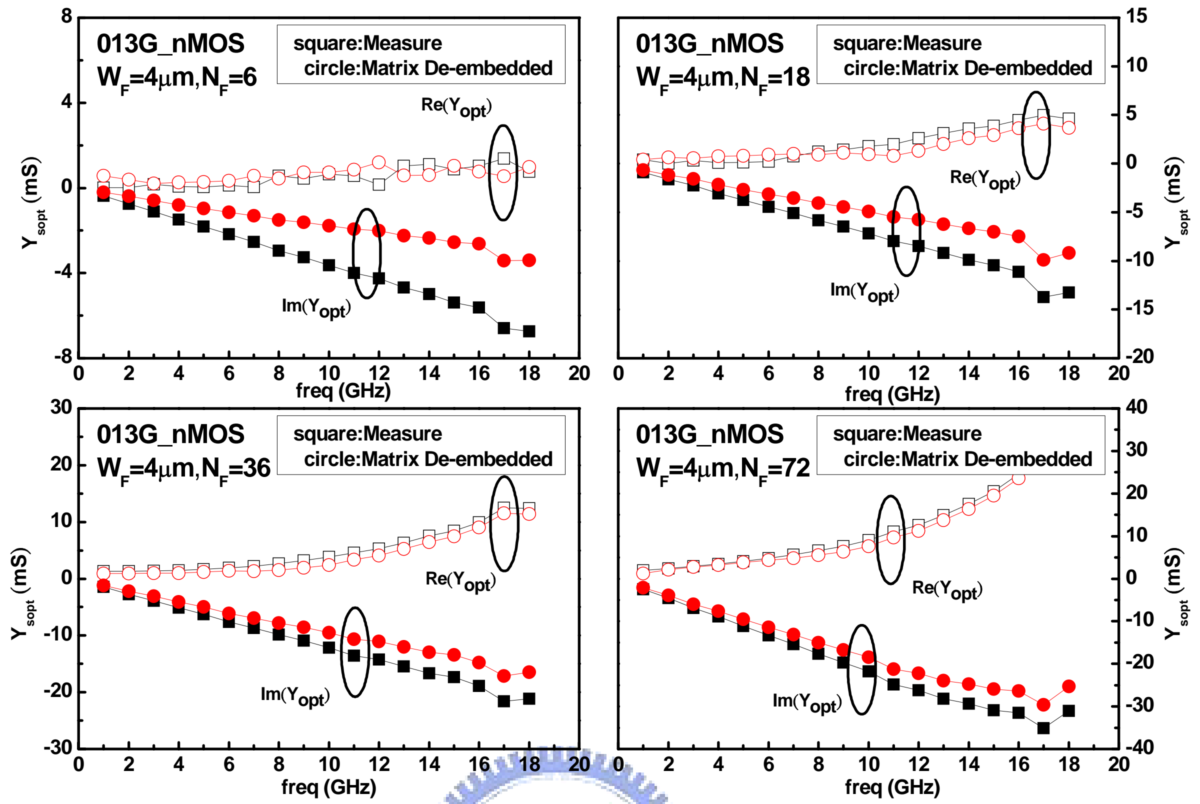


(c)

Fig. 3.7 0.13µm general purpose tech. nMOS with N_F=6, 18, 36, 72 biased at Vd = 1.2V and Vg = 0.6V. Pad layout with poly-ground shielding under signal pad. Signal pad metal stacking consists of M8 only. Comparison of noise parameters between as-measured and after correlation matrix de-embedded. (a) NF_{min} (b) R_n (c) $Re(Y_{sopt})$ and $Im(Y_{sopt})$

Chapter 4

RF MOSFET Intrinsic I-V and C-V Model Calibration

4.1 I-V and C-V Modeling Theory Valid for Sub-100nm MOSFETs

A well calibrated current-voltage (I-V) and capacitance-voltage (C-V) model is pre-requisite to accurate RF MOSFET model development. An elaborated model of I-V characteristic over a wide bias range is important for nowadays circuit design, especially for analog and RF circuit design, where a variety of bias conditions will be used. Also, with the increasing usage of low power circuit in modern IC applications, modeling near subthreshold region is also necessary. Capacitance model, similarly, need to be well calibrated to accurately predict the circuit performance. Altogether, correct I-V and C-V models are essential to provide us trustworthy DC and AC characteristics for further study of high frequency performance.

To ensure free from a non-physical model, before starting the parameter extraction optimization loop, some process related model parameters are specified and fixed at their known values, such as some important geometry or process parameters, L_{int} (channel length offset), W_{int} (channel width offset), T_{ox} (oxide thickness), N_{ch} (channel doping concentration), X_j (junction depth) and so forth.

In this thesis, 80nm and 65nm devices fabricated by C013LV process were adopted for I-V and C-V model calibration and noise de-embedding method development. The calibration work was started by modifying the model released by foundry, TSMC. For C013LV technology, BSIM3v3 model is used and the following important mechanisms are considered [11] (1) short channel and narrow width effects on threshold voltage, (2) mobility reduction due to vertical field, (3) velocity saturation, (4) drain-induced barrier lowering (DIBL), and (5)

Substrate current induced body effect (SCBE). It is assumed that most of the I-V and C-V parameters were fairly modeled in the original model and only minor modification is needed to improve the model accuracy. Unfortunately, the assumption can barely fit 80 nm devices but absolutely is no longer valid for 65 nm devices.

4.2 Intrinsic I-V Model

For RF MOSFET, 3–terminal test structure is usually implemented with common source configuration in which source and body terminals are tied together and grounded. To measure its high frequency characteristic (both S parameter and NF_{min}), two sets of probing pad with G-S-G structures are implemented and connected to the gate and drain terminals. The parasitic resistances associated with MOSFET's terminals such as R_{g_ext}, R_{d_ext}, R_{s_ext}, and R_{b_ext} contributed from the interconnection lines and probing pads will affect I-V characteristic of DUT. Extraction of these parasitic resistances should be done and added to the original intrinsic MOSFET model (BSIM3). The mentioned parasitic resistances can be extracted from the dummy short pads which is designed to de-embed the resistive and inductive parasitics of the interconnect lines and probe pads, etc.

In this study, simulation was done using Agilent Advance Design System (ADS) for model verification and calibration. Based on the original model card, default simulation results of I_d-V_g and I_d-V_d curves were obtained. Through comparison between simulation and measurement in terms of I_d-V_g and g_m-V_g curves in both linear and saturation regions, significant deviation was identified for the threshold voltage (V_{th}), drain current (I_d), gate subthreshold swing (S), etc. As for comparison of I_d-V_d curves, channel length modulation (CLM) and drain induced barrier lowering (DIBL) effects were revealed. Besides, the intrinsic and extrinsic parasitic resistances, R_{d_int} and R_{d_ext} at drain terminal will affect the rising slope between linear and saturation region.

For BSIM3, there are many parameters associated with the threshold voltage model. Since source and body of the DUT are tied together and connected to ground, body bias effect on threshold voltage is not available. Narrow width effect on V_{th} was neglected for sufficient large width of 4μm. Short channel effect related parameters such as *Dvt0* and *Dvt1* were included to account for charge sharing induced threshold voltage lowering. Mobility model parameter *U0* is the zero-filed mobility for I_d-V_g simulation in linear region under small drain bias (V_d = 0.1 or 0.05V). *Ua, Ub* and *Uc* are fitting parameters used to model the mobility degradation subject to normal field under gate bias. Saturation velocity V_{sat} determines the saturation current level. *Eta0*, and *Dsub* control the amount of threshold voltage variation caused by DIBL and I_d-V_g under V_d= V_{dd} is the fitting target. Parameters *A1* and *A2* stands for first and secondary non-saturation effect which occurs in the expression of V_{dsat} also help to improve I_d-V_g and g_m-V_g modeling. Subthreshold current fitting can be improved by V_{off} and *Nfactor* after the previous terms are well modeled. As for I_d-V_d modeling, *Pclm*, *Pdiblc1*, *Pdiblc2* can be used to properly modify the linear and saturation currents as well as output resistance R_{out}. Besides I_d-V_g and I_d-V_d characteristics, first order derivative and even second order derivative also deserve the effort to be well modeled since g_m or g_{ds} at a certain given bias (application bias point) may affect the device performance such as f_T, f_{max} as well as circuit simulation result.

For high frequency measurement, the test devices are configured to be probed through GSG pads. It is not suitable to conduct I-V measurement by using DC probes as conventional DC measurement does. It is due to the fact that only probing on two of the four ground pads will double the parasitic resistance. Even if G-S-G probes are used, horizontal level of the probes should be maintained at an identical horizon. Besides, to compensate for the cable loss, Kelvin connection [22] (with Force and Source lines) was adopted by introducing a bias-T. This configuration can prevent cable loss and small signal interference. Fig. 4.1 (a) and (b)

give the idea of the need of this measurement framework.

Fig. 4.2 ~ Fig. 4.4 present the DC I-V modeling results. Good agreement between measured and simulated results under varying biases and various N_F shows the integrity of the intrinsic BSIM model. The 65nm device was extremely trimmed from 130nm by 65nm, one half of its drawn length. High gate leakage or GIDL may contribute to the high drain current in its off-state. Current degradation for large N_F can be identified from Fig. 4.2 (b). Transconductance g_m per unit width for various N_F is given in Fig. 4.5. About 20% g_m degradation was observed for N_F = 72 compared with N_F = 6 for both two sets of device. Additional IR drop caused by the parasitic source resistance R_{s_ext} is proposed to explain the increasing degradation associated with larger N_F. It is worthy to note that due to the distinct difference in I-V characteristics between these two sets of devices (65nm and 80nm), different I-V model parameters were used to get optimized fitting individually.

4.3 Intrinsic Gate Capacitance (C-V) Model

In this section, capacitance modeling of multi-finger RF MOSFET is presented. Oxide thickness of C013LV nMOS technology is 1.7nm. For this thin oxide, capacitance model flag capMod = 3 was set as default model to take into account of the finite charge thickness determined by quantum effect.

Capacitance in MOSFET is generally divided into three parts, intrinsic, extrinsic and extrinsic parasitic. The intrinsic part is corresponding to the capacitances that are associated with the channel region (region under gate oxide and between metallurgical junction of source and drain). Extrinsic capacitances model considered in BSIM3 are fringing capacitance and overlap capacitance; both consist of bias dependent and bias independent part. Only bias independent outer fringing capacitance is implemented (parameter *CF*) while both bias dependent LDD overlap capacitance (parameter C_{gsl}, C_{gdl}) and bias independent non-LDD

overlap capacitance (parameter *Cgso*, *Cgdo*) are taken into account. However, due to metal routing of DUT and prerequisite of GSG probing pad for RF measurement, extra parasitic capacitances were introduced and these were classified as extrinsic parasitic capacitances (C_{gs_ext}, C_{gd_ext}, C_{ds_ext}, C_{pad}). Fig. 4.6 demonstrates a detailed classification of capacitances in MOSFETs.

Capacitances of RF MOSFET with GSG probing structure are conventionally extracted from the intrinsic Y parameter (Y_{int}) at low frequency. Before the extracting process, parasitic capacitances due to probing pad and interconnection metal should be de-embedded from the measured data. Traditionally, the removal of these parasitics is done through open de-embedding mentioned early. In fact, short de-embedding should also be carried out to get rid of the series impedances. This is essential for accurate capacitance extraction. A broadly accepted de-embedding technique is open/short two step de-embedding for two-port three terminal device (source/bulk tied together) [23]. Due to the fact that the coupling capacitance between two-ports is mainly dominated by the coupling of interconnection metal instead of probing pad, a modified open/short de-embedding approach was proposed to avoid over de-embedding on this coupling capacitance and thus improved C_{gd} model accuracy. Appendix C presents this modified de-embedding. The new de-embedding method is especially efficient when an open pad is designed with all the interconnection metal left.

After the de-embedding, intrinsic gate capacitances can be extracted from the formulas given by [24]:

$$C_{gg} = \mathrm{Im}(Y_{int,11})/\omega \qquad (4\text{-}1)$$

$$C_{gd} = -\mathrm{Im}(Y_{int,12})/\omega \qquad (4\text{-}2)$$

$$C_{gs} = \mathrm{Im}(Y_{int,11}+Y_{int,12})/\omega \qquad (4\text{-}3)$$

$$C_{ds}=\mathrm{Im}(Y_{int,22}+Y_{int,12})/\omega \qquad (4\text{-}4)$$

Intrinsic gate-to-back capacitance C_{gb} is negligible due to its small value in triode and saturation regions. This is because the inversion layer in the channel shields between gate and bulk. It is worthy to mention that how clean the parasitic capacitances can be removed and the intrinsic capacitance can be extracted critically depends on the open dummy structure, i.e., how many coupling terms can be removed from the measured data. A conventional open pad leaving only the GSG pad frame obviously underestimates the coupling capacitances. A modified structure is to remove the DUT cell simply, thus leave the connecting metal between DUT cell and signal metal pad. This modification enables us to extract the capacitances of the DUT cell that is sometimes what a circuit designer need in some cases. As for the open de-embedding structure available for C013LV devices, the metal line is terminated at M3 and the–parasitic coupling between gate to drain, gate to source, drain to source by means of connecting via and metal (from M1 to M3 in 013LV case) will remain in the de-embedded data. These coupling terms greatly depend on the metal routing and lead to the non-scalability of capacitance modeling. This non-scalable property will affect the accuracy of the following parameter extraction for DUT, such as f_T, $\overline{i_d^2}$, $\overline{i_g^2}$ [18][19]. From device modeling point of view, it is better to clearly extract all the parasitics from the DUT to correctly model both capacitances of parasitic and DUT. Also, a pure device model can provide design freedom on metal routing.

In this work, one open dummy pad was shared by all the DUTs. This open dummy is designed so that only the common part of the DUTs was left, i.e. G-S-G pad with interconnection line terminated at M3. As mentioned above, this kind of de-embedding cannot remove the coupling capacitances associated with lower metals (M1~M3). Due to the fact, the capacitance of DUT after de-embedding includes finger-number dependent capacitance, both

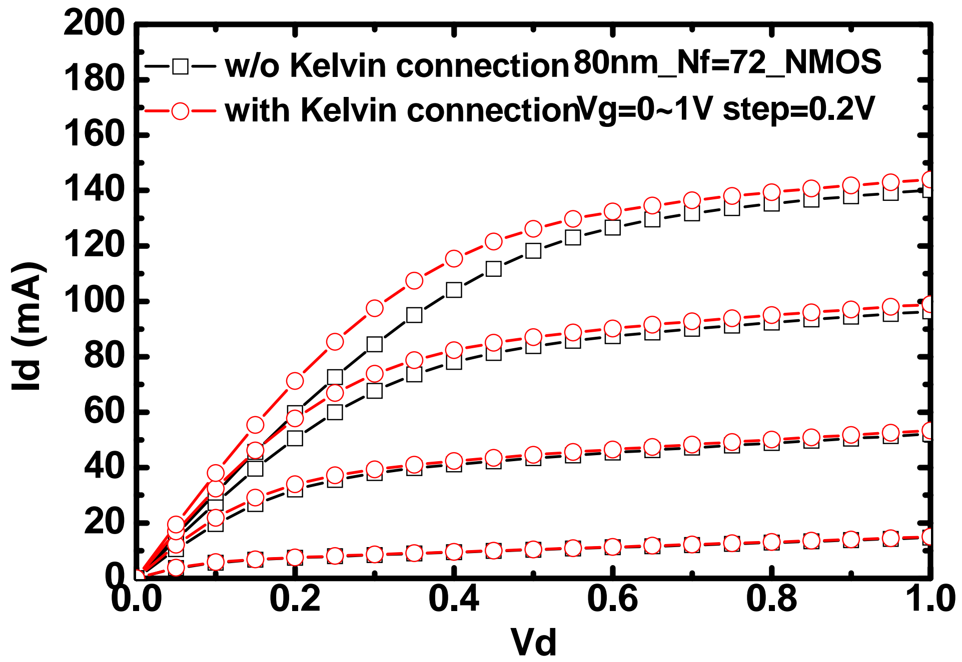
intrinsic and extrinsic portion, and finger-number independent extrinsic parasitic capacitance. Gate capacitance of different finger number is shown in Fig. 4.7. Linear finger-number dependence was demonstrated but the extrapolation of capacitance reveals a non-zero intercept. Linear slope of these capacitances shows C_{gs}/C_{gd} partition of approximately 60%/40% for 65nm device and 65%/35% for 80nm device, respectively. The non-zero intercept indicates a physically finger-number independent common parasitic term for the DUT with different finger numbers.

In the modeling process, extrinsic components C_{gs_ext} and C_{gd_ext} were used to model the common parasitic capacitance and model parameters, C_{gso}, C_{gdo}, C_{gsl}, C_{gdl}, V_{offcv} were used to complete the result. First, adjust C_{gso} and C_{gdo} to a value so that simulation result is close to the measured one. Then, use V_{offcv} to modify its gate bias trend. C_{gsl} and C_{gdl} are employed to modulate the gate bias trend of C_{gs} and C_{gd} individually. Parameter *DLC* may be included to adjust the length offset for C-V model which does not affect the I-V curve modeling. Finalized model parameters are shown in Table 4.1. Fig. 4.8 (a)~(c) present the modeling result of the gate capacitance. C_{gg} is reduced by around 20% for 65nm following the L_{gate} scaling factor while C_{gd} is reduced by only 7~14%. The minor reduction of C_{gd} is due to the drain depletion effect under saturation condition.

Table 4.1

Model parameters for gate capacitance modeling.

W_F=4um	C_{gs_ext}(fF)	C_{gd_ext}(fF)	Cgs0(F/m)	Cgd0(F/m)	Cgsl(F/m)	Cgdl(F/m)	CF(F/m)	Voffcv
65nm	3.488	3.2	10p	370p	60p	60p	0	-0.050
80nm	1.225	4.6	10p	420p	50p	50p	0	-0.038



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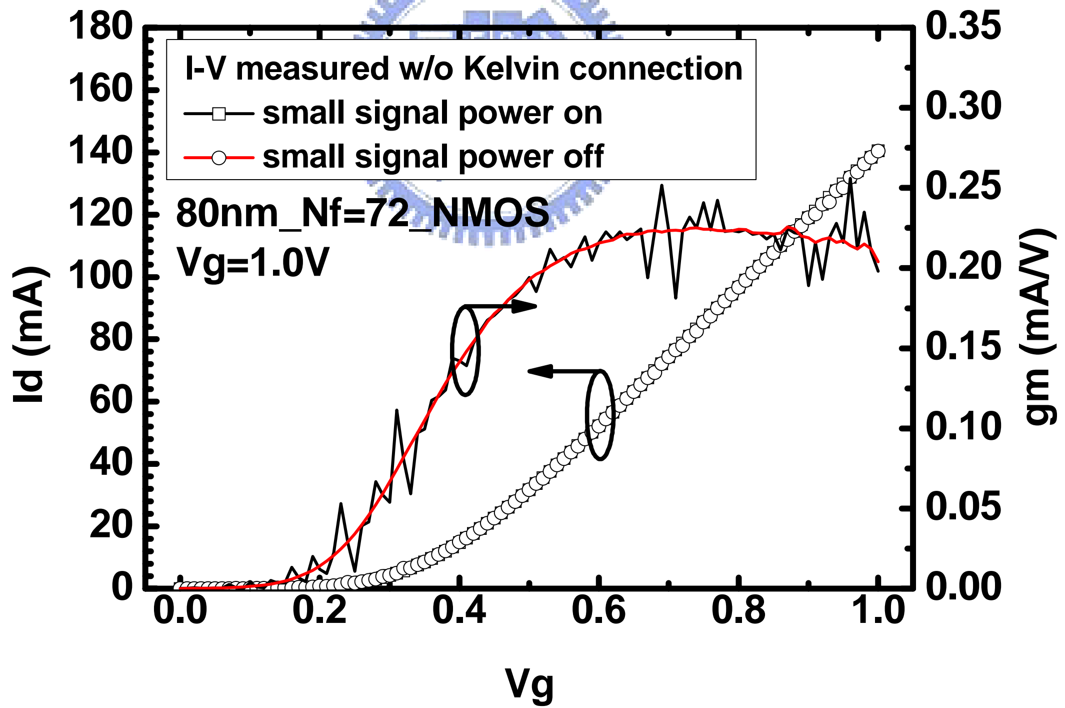
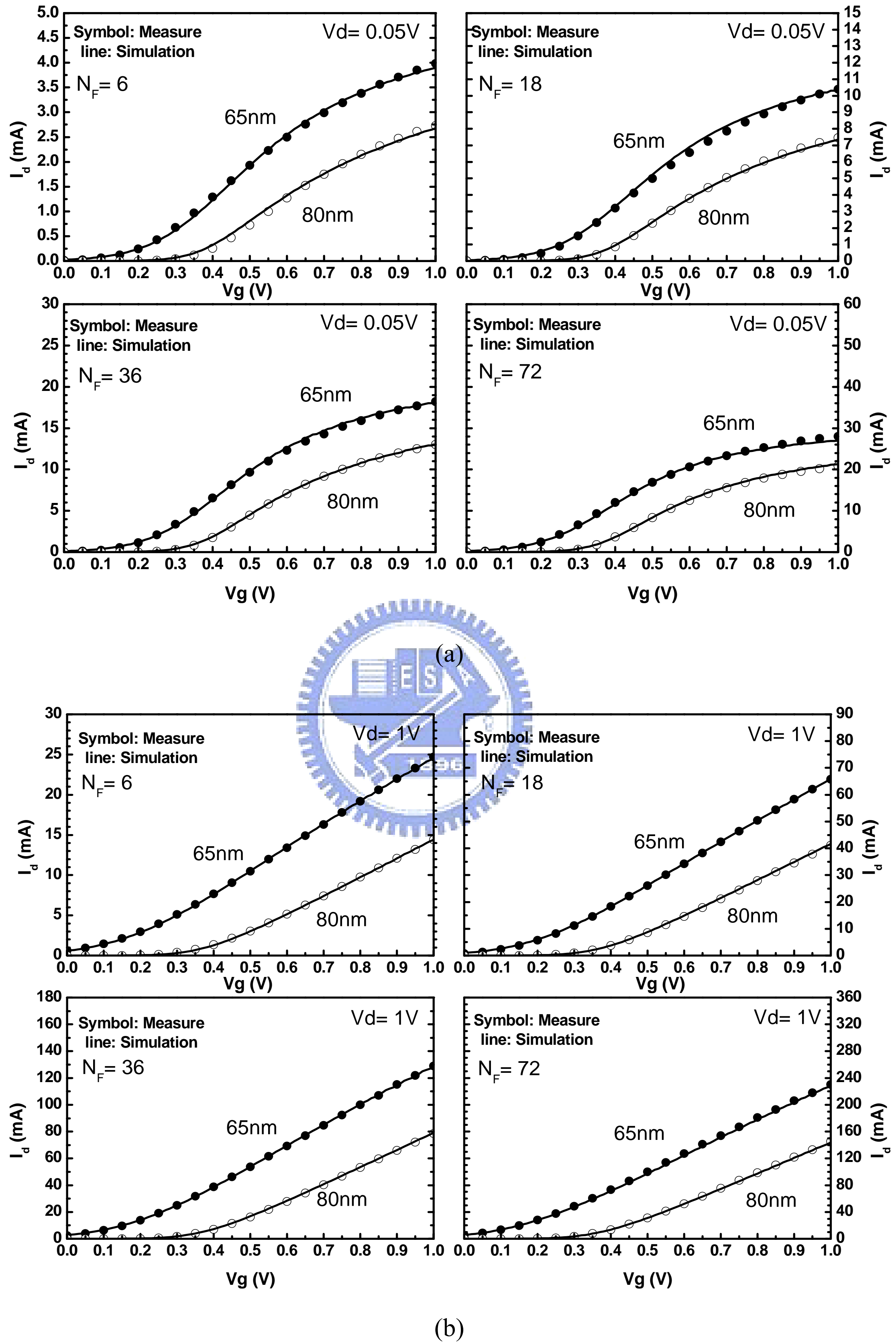


(b)

Fig. 4.1 (a) Id-Vd characteristic measured with and without Kelvin connection.

(b) Id-Vg characteristics measured with and without bias-T network to isolate the small-signal from DC measurement.



(a)

(b)

Fig. 4.2 (a) Linear Id-Vg of 80 and 65nm nMOS when Vd = 0.05V. (N_F = 6, 18, 36, 72)

(b) Saturation Id-Vg of 80 and 65nm nMOS when Vd = 1V. (N_F = 6, 18, 36, 72)

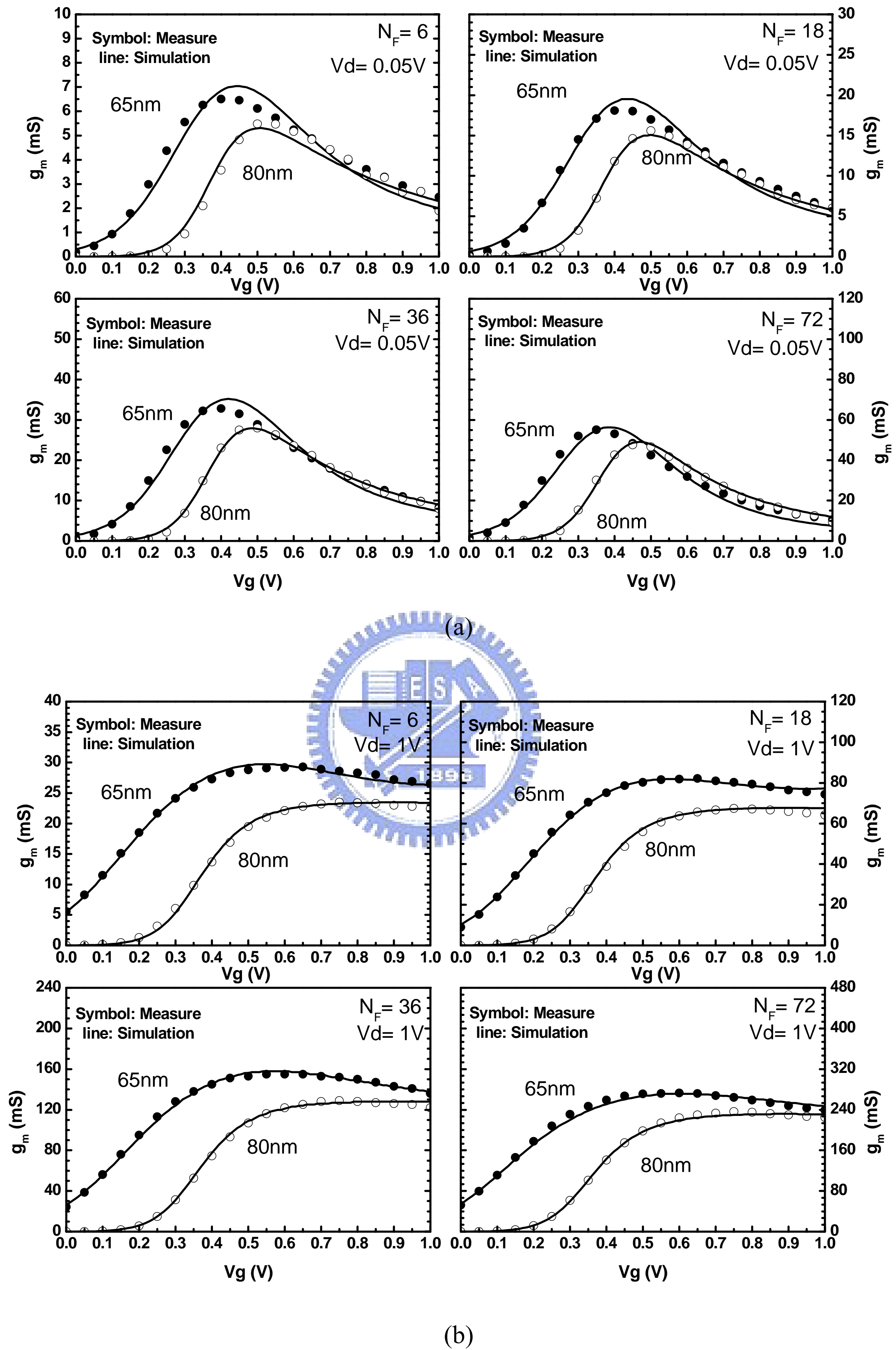
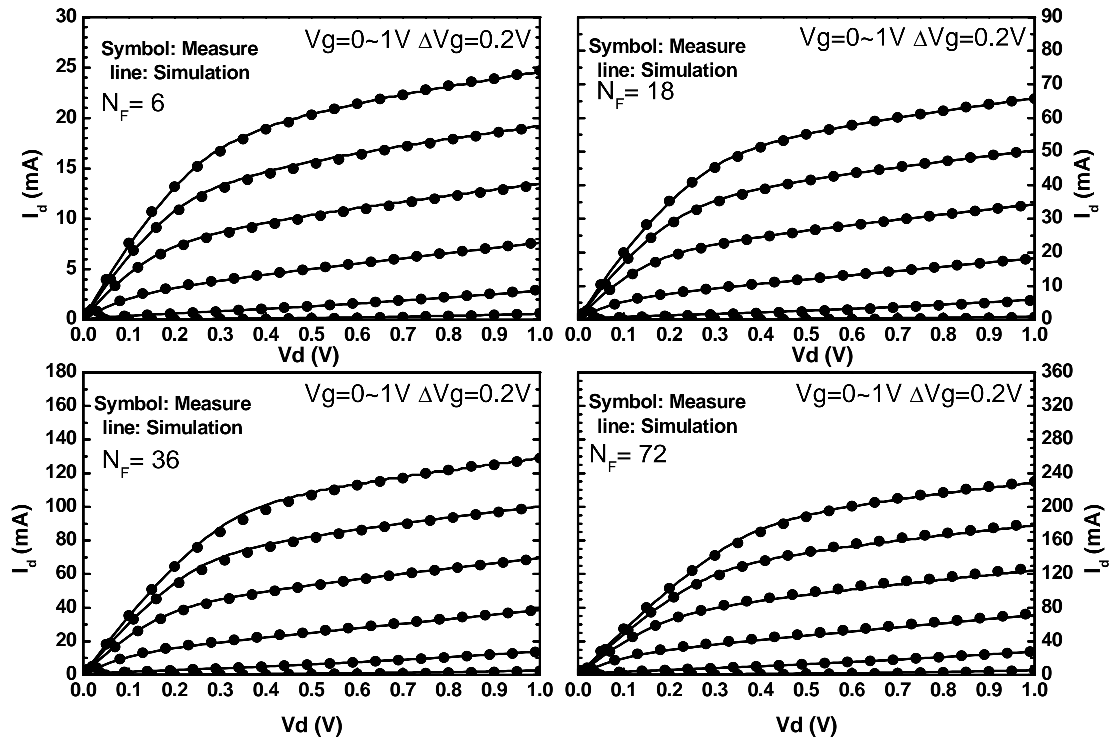


Fig. 4.3 (a) Linear g_m-Vg of 80 and 65nm nMOS when Vd = 0.05V. (N_F = 6, 18, 36, 72)

(b) Saturation g_m-Vg of 80 and 65nm nMOS when Vd = 1V. (N_F = 6, 18, 36, 72)



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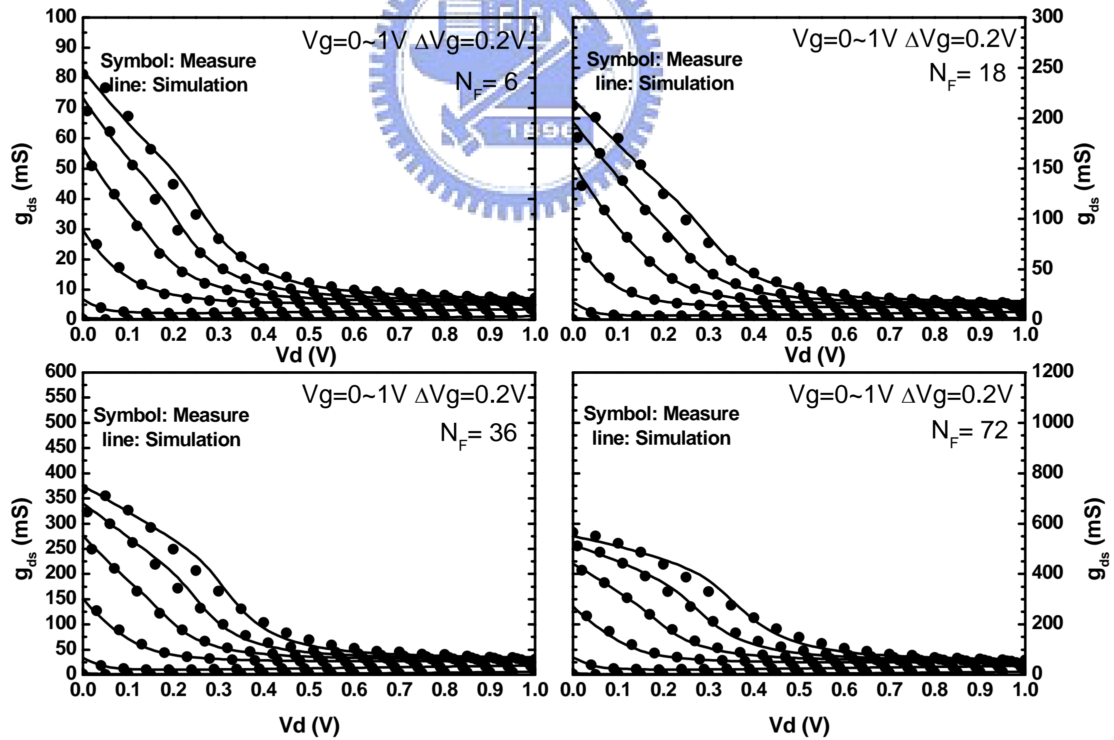
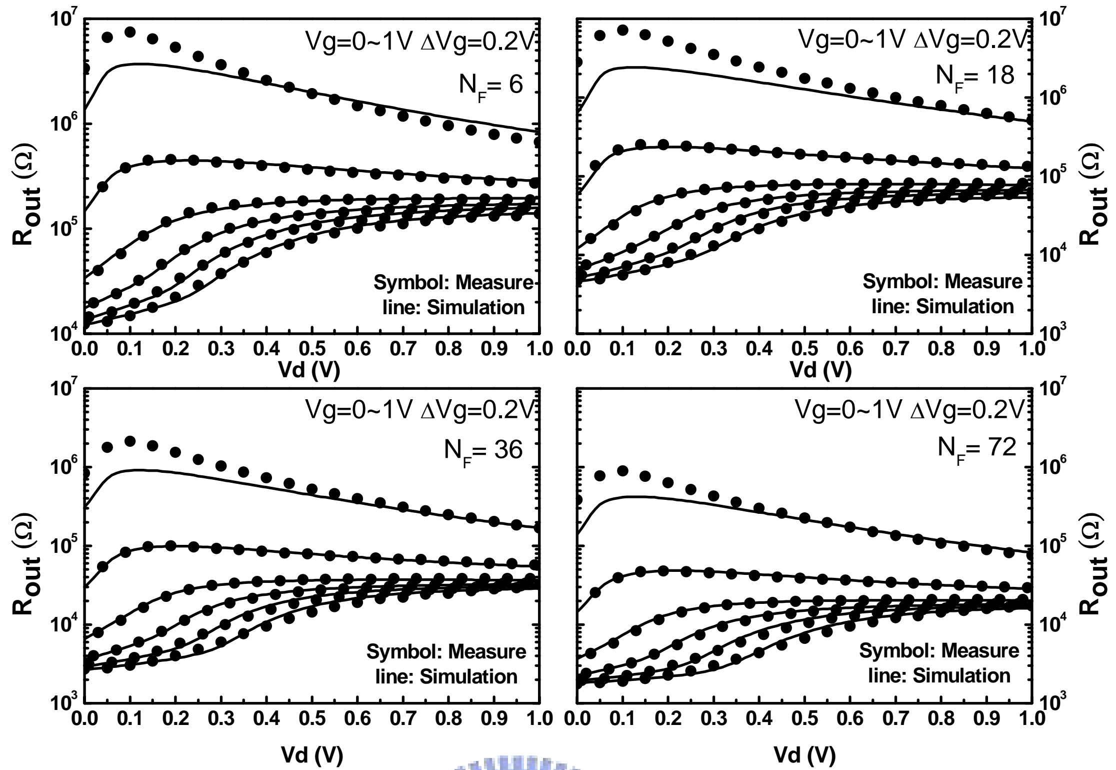


(b)

Fig. 4.4 (a) Id-Vd of 65nm nMOS for Vg = 0~1V with 0.2V Vg step. (N_F = 6, 18, 36, 72)

(b) Conductance g_{ds}-Vd of 65nm nMOS. (N_F = 6, 18, 36, 72)



(c)

Fig. 4.4 (c) Output resistance R_{out}-Vd of 65nm nMOS. (N_F = 6, 18, 36, 72)

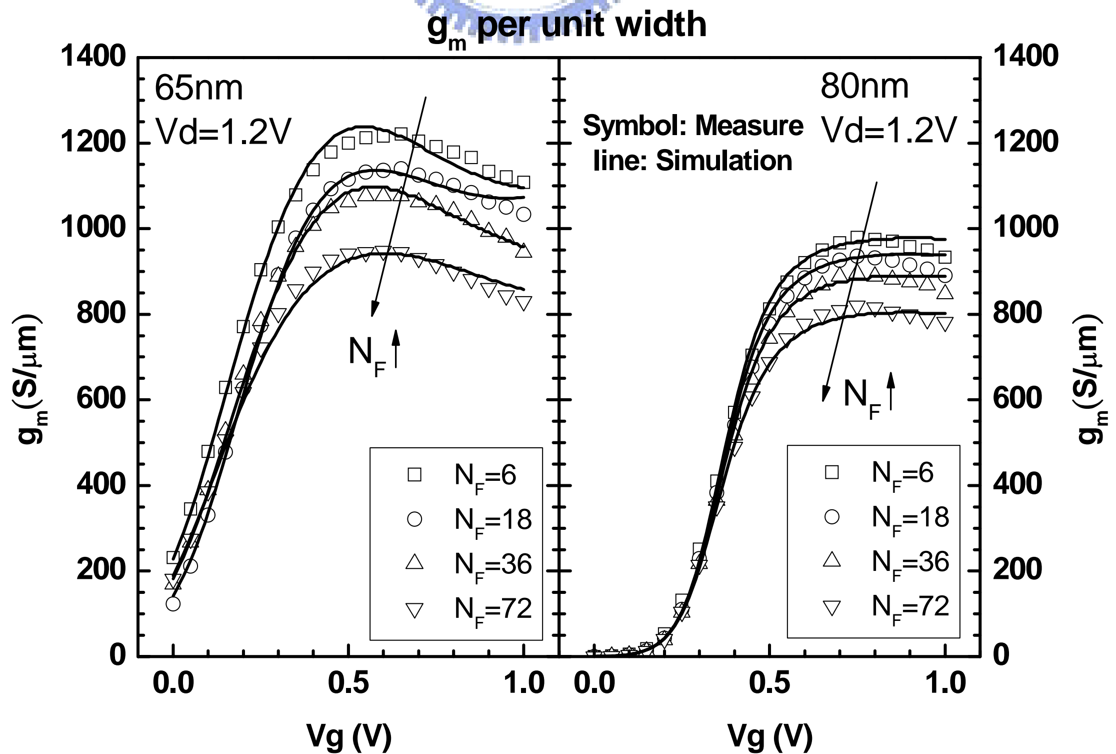


Fig. 4.5 Transconductance g_m for various N_F of 65 and 80nm respectively.

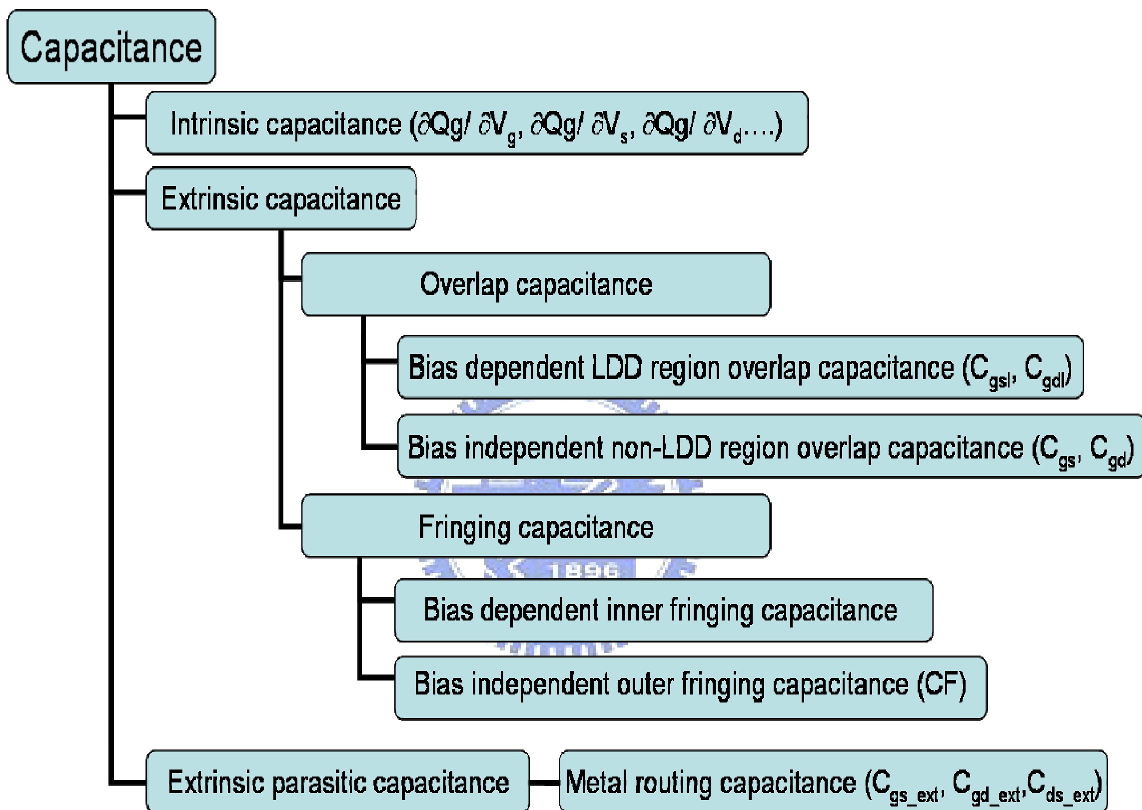
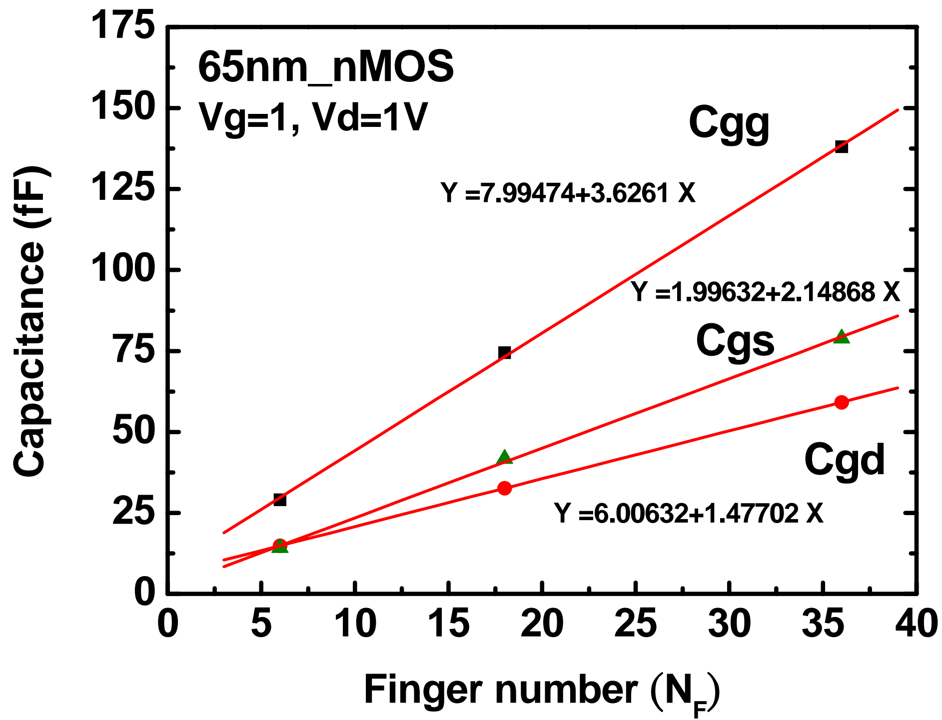
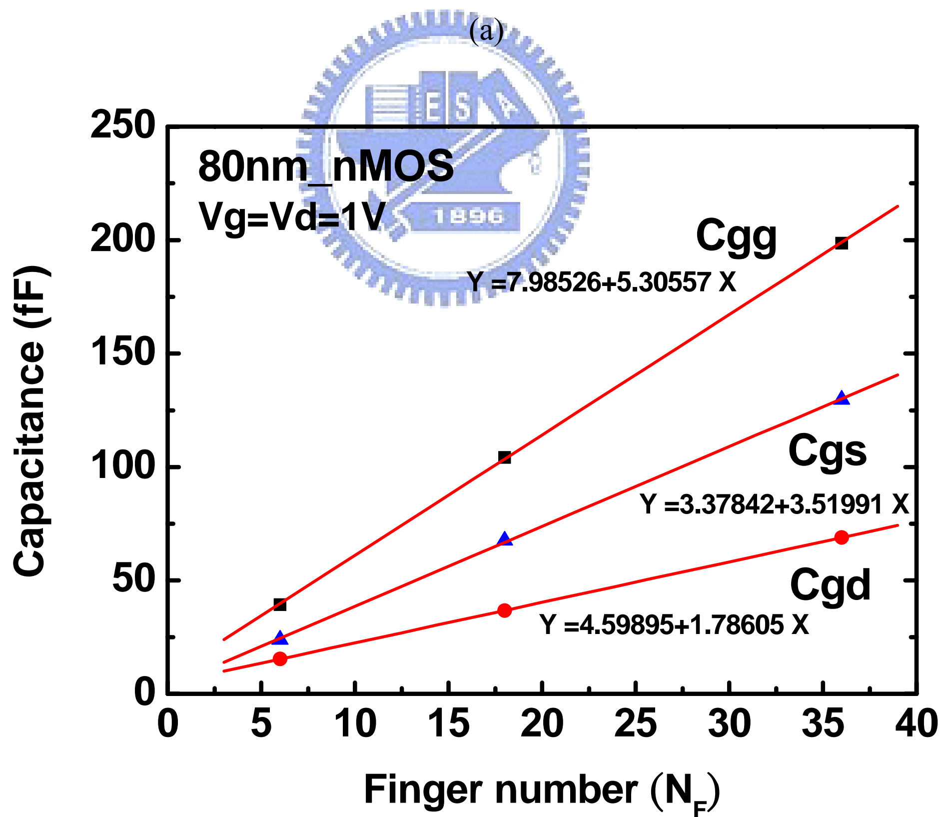


Fig. 4.6 Category diagram of capacitance in MOSFETs.



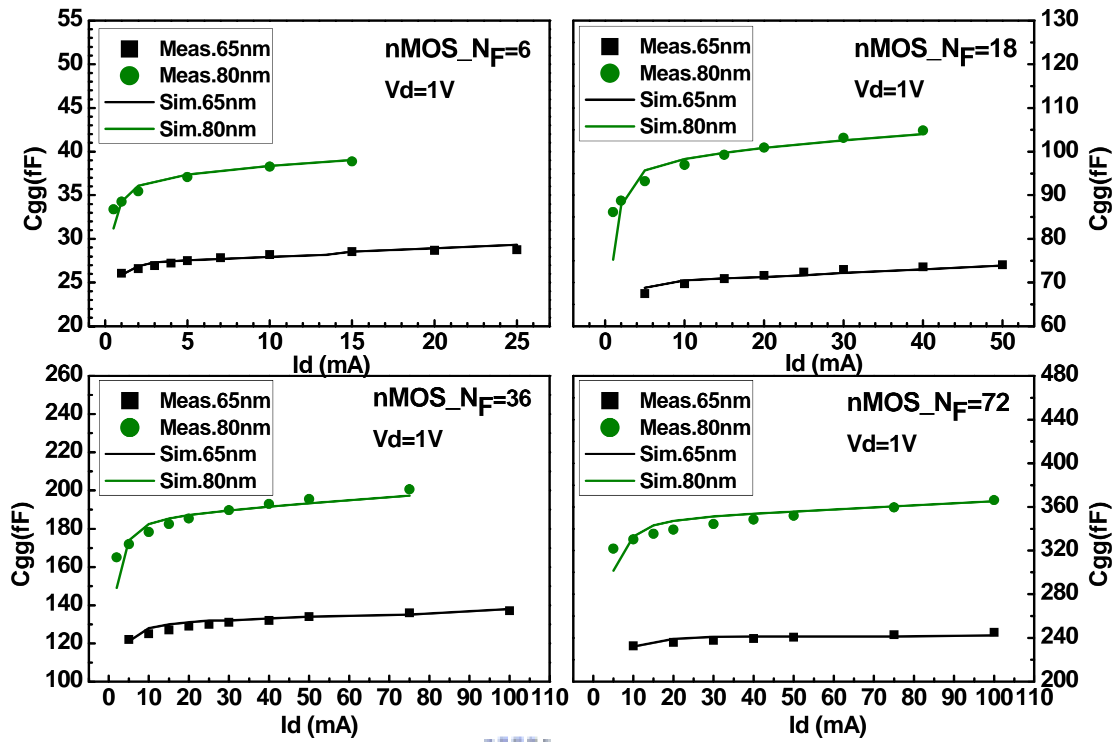
(a)



(b)

Fig. 4.7 (a) 65nm nMOS C_{gg}, C_{gd} and C_{gs} extracted at Vg = Vd = 1V for N_F = 6, 18, 36

(b) 80nm nMOS C_{gg}, C_{gd} and C_{gs} extracted at Vg = Vd = 1V for N_F = 6, 18, 36



(a)

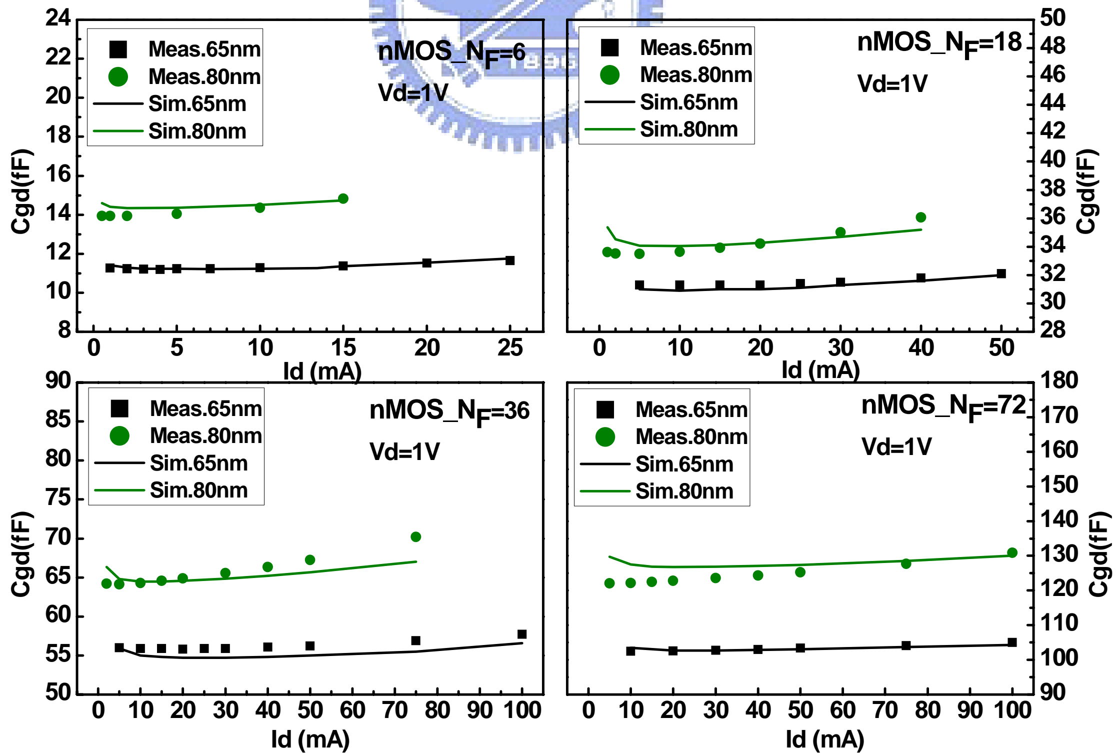
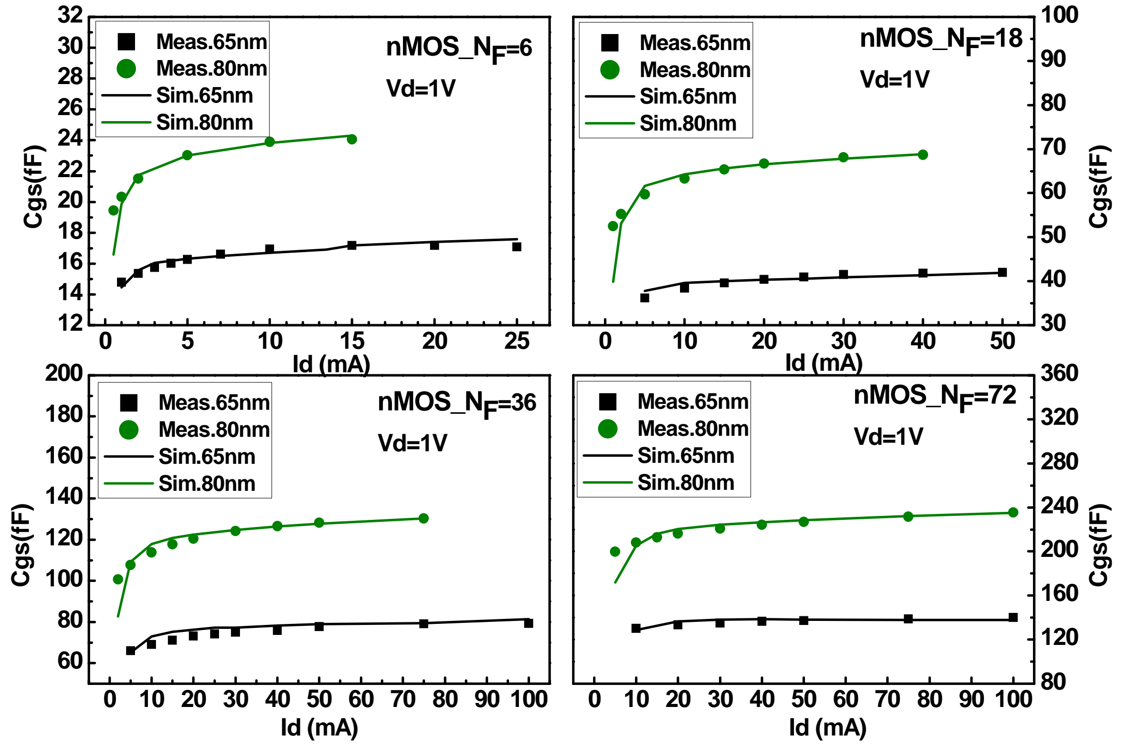


Fig. 4.8 (a) 65 and 80nm nMOS C_{gg} extracted under various Vg for N_F = 6, 18, 36, 72

(b) 65 and 80nm nMOS C_{gd} extracted under various Vg for N_F = 6, 18, 36, 72



(c)

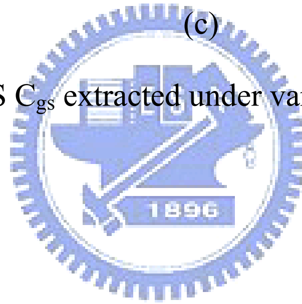


Fig. 4.8 (c) 65 and 80nm nMOS C_{gs} extracted under various Vg for N_F = 6, 18, 36, 72

Chapter 5

RF MOSFET Noise De-embedding

In this study, a new noise de-embedding method has been developed and justified in terms of accuracy over various biases and frequencies. The noise de-embedding was done by removing a lossy substrate model from the original full circuit structure for fitting the measured noise characteristics. This lossy substrate model is composed of parallel and series RLC networks to account for the capacitive coupling and series resistive and inductive impedance originated from the G-S-G pad, interconnection lines, and low resistivity Si substrate.

5.1 Equivalent Circuit Approach

As mentioned previously, noise correlation matrix method is a popular one for noise de-embedding. However, couples of weaknesses existing with this conventional method trigger our motivation of this work. An equivalent circuit method was proposed to model the lossy substrate, lossy pad, and transmission line (TML) effects and their impact on MOSFETs' noise. The proposed equivalent circuit model named as "lossy substrate model" was integrated with a calibrated intrinsic MOSFET model as a full structure for high frequency S-parameter and noise parameter simulation before de-embedding. In this study, BSIM3 model through extensive calibration (Chapter 4) was adopted to simulate the MOSFET characteristics in terms of I-V and C-V. An equivalent circuit composed of series and parallel RLC networks was developed through extensive verification in terms of open pad and full structure S-parameters and noise parameters of a full structure before de-embedding.

For an open pad, two-port measurements were done to achieve input and output reflection coefficient, S_{11} and S_{22}. In general, S_{12} and S_{21} are much smaller than S_{11} and S_{22}

due to extremely small coupling capacitance between port1 and port2. However, depending on the metal layers left in an open pad layout near the DUT, the inter-signal port coupling capacitance can be varied from around 0.5fF to 10fF. A capacitance corresponding to this effect should be added to obtain accurate modeling for S_{12} and S_{21}.

Several pad models were proposed to study the parasitic effect on measured S-parameters and to explain the evolution of model development to an official one named as lossy substrate model. S-parameters are usually expressed in terms of magnitude and phase, while Y-parameters are represent in its real and imaginary part. Model 1 shown in Fig. 5.1 with a shunt capacitance to simulate a purely capacitive coupling is absolutely too ideal. One common idea to simulate lossy silicon substrate using a paralleled RC network was implemented as Model 2 in Fig. 5.2. Nonlinear frequency dependence of admittance Y_{11} (or Y_{22}) can be modeled at frequency below 10GHz (Fig. 5.5), but S_{11} deviates a lot from measured data (Fig. 5.6). Through verification on the RC network using circuit simulation, it was found that S-parameter data could be modeled with a frequency-dependent resistance. This finding resulted in a substrate network with a capacitance in paralleled with a series resistance and capacitance, named as Model 3 in Fig. 5.3. This model can predict S- and Y-parameters below 10GHz quite well, but still lack of accuracy at higher frequency for phase(S_{11}) (or phase(S_{22})) and imaginary part of Y_{11} or Y_{22} (Im(Y_{11}) or Im(Y_{22})). Finally, a new RLC network proposed in this work, named as model 4, composed of a series RLC and then in parallel with a capacitance as shown in Fig. 5.4 can further improve the modeling accuracy up 40GHz and beyond. Fig. 5.5 ~ Fig. 5.7 present the simulated Im(Y_{11}), Mag(S_{11}), and phase (S_{11}) using mentioned different pad models to justify the accuracy improvement through model evolution from the simplest one (model 1) to the final one (model 4) proposed in this work.

The proposed equivalent circuit model for each G-S-G pad consists of two branches of

R-L-C network, incorporating pad capacitance (C_{pad}), lossy substrate (R_{si}, Csi, L_{si}, and C_p), and transmission line (R_{tml}, L_{tml}) used to connect the signal pad to the gate and drain terminals of the intrinsic MOSFET. One of RLC networks, which is near the signal pads (gate or drain) adopted a capacitance named C_{pad} to model the dielectric capacitance under the signal pad. This capacitance is mainly governed by the signal pad area and metal stack underneath. In this work, C_{pad} is implemented as a physical parameter calculated by layout and process parameters rather than form extraction. The pad size of the test structure is 100×100 μm^2. In series with C_{pad}, a RLC network is used to model the signal coupling from the lossy pad through the lossy substrate. Capacitances C_p and C_{si} account for the capacitive coupling while substrate resistance R_{si} and inductance L_{si} were proposed to model the semi-conducting nature of silicon substrate under high frequency operation. Coupling capacitance C_c connecting the two-ports is required to model S_{12} and S_{21} of the open pads and it should be removed from the pad model when a device is attached through the two-ports to simulate S-parameters and noise parameters of a full structure before de-embedding. Regarding the resistance (R_{tml}) and inductance (L_{tml}) associated with transmission line, they can be extracted from Z-parameters of a short pad after modified open de-embedding.

Fig. 5.8(a) presents the equivalent circuit model derivation through circuit analysis. Fig. 5.8(b) indicates the extraction flow of equations derived through circuit analysis. The model parameters can be extracted under approximation valid for relatively low or relatively high frequency. These extracted values serve as initial guess for further optimization. Parameter optimization was supported by Agilent IC-CAP and Agilent Advance Design System (ADS). Optimization target was set to get best fit to S- and Y- parameters simultaneously. Good agreement between simulation and measurement for S_{11}, S_{22}, Y_{11}, and Y_{22} are shown in Fig. 5.9. Table 5.1 lists the optimized open pad model parameters.

Table 5.1 Open pad model parameters

	L_{tml}(pH)	R_{tml}(Ω)	C_{pad}(fF)	C_P(fF)	$C_{Si,1}/C_{Si,2}$ (fF)	L_{Si}(nH)	R_{Si}(Ω)
Gate	30	0.25	190	15.5	47/126.5	0.5	408
Drain	20	0.25	190	15.5	43/143	0.38	368

5.2 Equivalent Circuit Model Verification

Fig. 5.10 illustrates the device characterization and modeling flow. The equivalent circuit of intrinsic MOSFET was shown by the dash block in the full circuit schematic in Fig. 5.11. A core BSIM3 MOSFET model was calibrated in terms of I-V and C-V characteristics. Two junction diodes were implemented to represent the drain-to-body and source-to-body p-n junctions. C'_{ds} and R'_{ds} were adopted to model the source to drain proximity capacitance and the associate resistance apparent at high frequency; they play an important role in accurate modeling of S_{22}. R_g is the gate resistance extracted from real part of Z-parameters which is mainly dominated by poly gate resistance and distributed channel-coupled resistance [25], R_g is a momentous factor in RF MOSFET, it greatly affects the noise figure, f_{max}, and input matching. R_d and R_s are the parasitic drain and source resistances due to lower level metal routing (below M3). Terminal parasitic inductances (L_g, L_d and L_s) are required to model the high frequency characteristic of interconnection lines and device routing metal. These will become very small (smaller than 10pH) and can be neglected from the intrinsic MOSFET model when accurate short de-embedding was performed. R_{bulk} represents the distributed substrate resistance, which generally has significant effect on small-signal output characteristics [26] and noise performance. Though a popular substrate network of three substrate resistance was suggested by some study but we get important observation through careful verification that the resistor in series with a junction diode does not show visible effect in the simulated results. As a result, only one simple resistance attached with the bulk terminal was used in this work. Regarding the source and bulk configuration for the 3-terminal

MOSFET in this study, common short was defined in the circuit schematic for simulation to ensure the common potential of source and bulk.

The gate resistances R_g extracted from Z-parameters are demonstrated in Fig. 5.12(a) and (b) for 80nm and 65nm devices, respectively. Referring to the extraction equations in [24] accurate R_g should be extracted at sufficiently high frequency and a constant R_g achieved at frequency higher than 20GHz as shown in Fig.5.12 justifies the proposed extraction method. R_s and R_d were extracted from short pad but with some minor optimization for I-V fitting. Intrinsic model verification in terms of I-V and C-V has been covered in Chapter 4. Cut-off frequency (f_T) extraction and simulation under various gate biases were also done to further verify the accuracy of intrinsic model. Fig. 5.13 presents good agreement between the measured and simulated f_T for 80nm and 65nm nMOS in which obvious f_T improvement of around 50~60% was realized by gate length scaling from 80nm to 65nm.

Fig. 5.11 depicts the proposed full circuit model which incorporates lossy substrate model with well calibrated intrinsic MOSFET model (dash block). Pad model parameters previously extracted from open pad structure serve as initial value for further optimization to fit S-parameters and noise parameters measured from full circuit. In practice, the substrate coupling effect in a full circuit with DUT and pad does not exactly follow that of a dummy pad which consists of interconnection lines terminated at M3. Base on this concept, minor modification on the original pad model parameters is needed to get better fitting to the measured S-parameters, Y-parameters and noise parameters before de-embedding. Finalized parameters for various N_F are given in Table 5-2. L_{tml} and R_{tml} associated with gate and drain were extracted from Z-parameters of a short pad, which was commonly shared by various N_F. Therefore, L_{tml} and R_{tml} are the same for different N_F. Because source and bulk were tied together, transmission lines of source and bulk terminals were in parallel and expressed as $L_{sb,tml}$. Inductors associated with gate, drain and source/bulk terminal are extracted from

Z-parameters through open and short de-embedding. It is assumed that parasitic resistance and inductors of metal interconnection can be removed after short de-embedding. However, for larger devices of N_F = 36, 72 in which larger area spanned by larger finger number may lead to failure of clean de-embedding of metal lines' parasitics by a common shared short de-embedding structure. As a result, small amount of residual inductance remains with the devices of larger N_F (Table 5.2). As for smaller device of N_F= 6, 18, the remaining parasitic inductances after short de-embedding are extremely small or even go to negative value, which means almost no inductance left or even over-deembedding through the common short de-embedding. To compromise with the mentioned un-reasonable conditions, they were set to zero.

Table 5.2

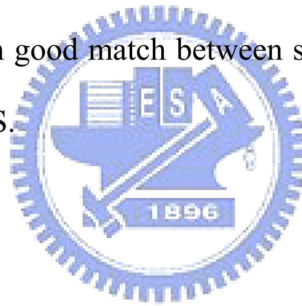
Pad model parameters for various N_F after optimization

Gate Electrode								
N_F	L_{tml}(pH)	R_{tml}(Ω)	C_{pad}(fF)	C_P(fF)	$C_{Si,1}$ (fF)	$C_{Si,2}$ (fF)	L_{Si}(nH)	R_{Si}(Ω)
6	30	0.25	190	18.2	82	122	0.6	390
18	30	0.25	190	29.0	94	185	0.31	280
36	30	0.25	190	55.0	121	202	0.7	250
72	30	0.25	190	60.0	290	240	0.3	200

Drain Electrode								
N_F	L_{tml}(pH)	R_{tml}(Ω)	C_{pad}(fF)	C_P(fF)	$C_{Si,1}$ (fF)	$C_{Si,2}$ (fF)	L_{Si}(nH)	R_{Si}(Ω)
6	20	0.25	190	16.6	105	139	0.40	325
18	20	0.25	190	12.0	300	260	0.38	250
36	20	0.25	190	25.0	364	295	1.00	250
72	20	0.25	190	52.0	710	650	3.00	200

L_g=80nm/W_F=4μm										
N_F	R_g (Ω)	R_S (Ω)	R_d (Ω)	L_g(pH)	L_d(pH)	L_s(pH)	R_{bulk} (Ω)	C_{ds}(fF)	R_{ds} (Ω)	L_{sb_tml} (pH)
6	26.56	1.23	1.26	33.8	18.6	3.5	166.43	6.52	524.43	12.20
18	11.05	0.83	0.42	31.4	16.4	3.9	87.04	39.29	222.46	12.20
36	6.27	0.73	0.21	32.7	17.5	3.3	67.19	88.45	146.97	12.20
72	3.98	0.67	0.10	30.3	15.1	3.8	57.26	186.77	109.23	12.20

The full circuit as shown in Fig. 5.11 was adopted for high frequency and noise simulation to achieve S-parameter and noise parameters before de-embedding Fig. 5.14 (a) ~ (c) demonstrate good match in S_{11} and S_{22} between measurement and simulation for both 80nm and 65nm nMOS with various N_F. Fig. 5.15 and Fig. 5.16 present the same results in Smith chart. Fig. 5.17 (a) and (b) indicate Y_{11} and Y_{22} representing input and output capacitances. In noise simulation, in addition to thermal noise of intrinsic MOSFET and parasitic resistance induced excess noise, pad capacitive coupling and substrate loss are considered as important factors responsible for the abnormal as-measured NF_{min}. Good agreement between the measured and modeled noise parameters NF_{min}, R_n, Re(Y_{sopt}) and Im (Y_{sopt}) over wide range of frequencies up to 18GHz are shown in Fig. 5.18 ~ Fig. 5.23. Fig. 5.24 ~ Fig. 5.26 show the extrinsic NF_{min} under varying I_d (0.5~100mA) and fixed frequency (2.4, 5.8, and 10GHz) in which good match between simulation and measurement is realized for both 65nm and 80nm nMOS.



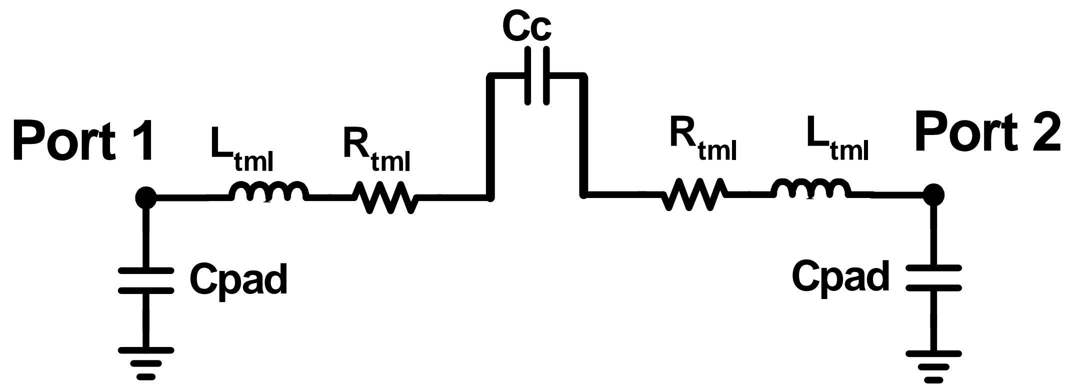


Fig. 5.1 Equivalent circuit of open pad model (Model 1)

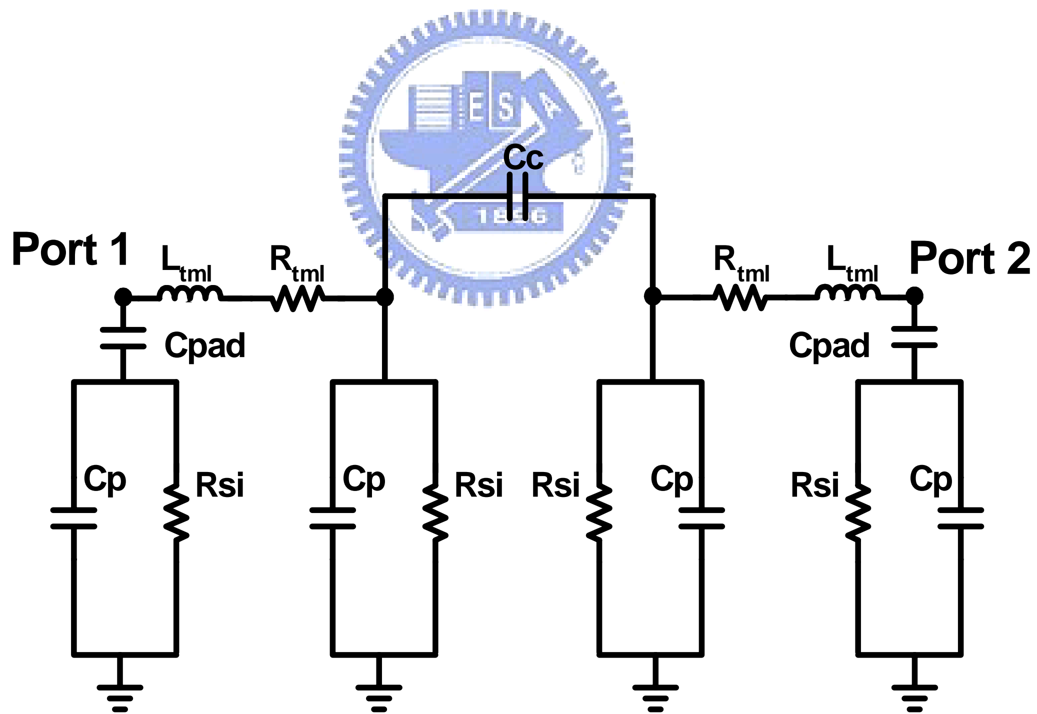


Fig. 5.2 Equivalent circuit of open pad model (Model 2)

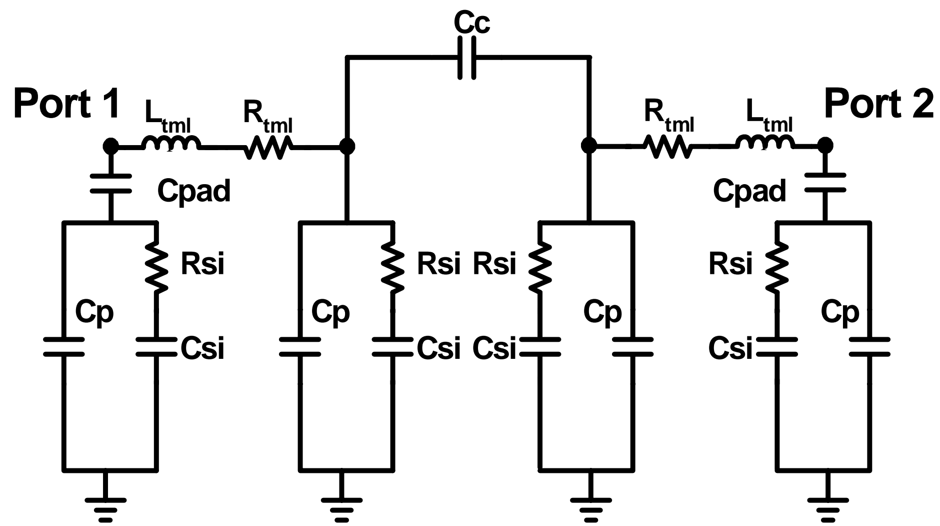


Fig. 5.3 Equivalent circuit of open pad model (Model 3)

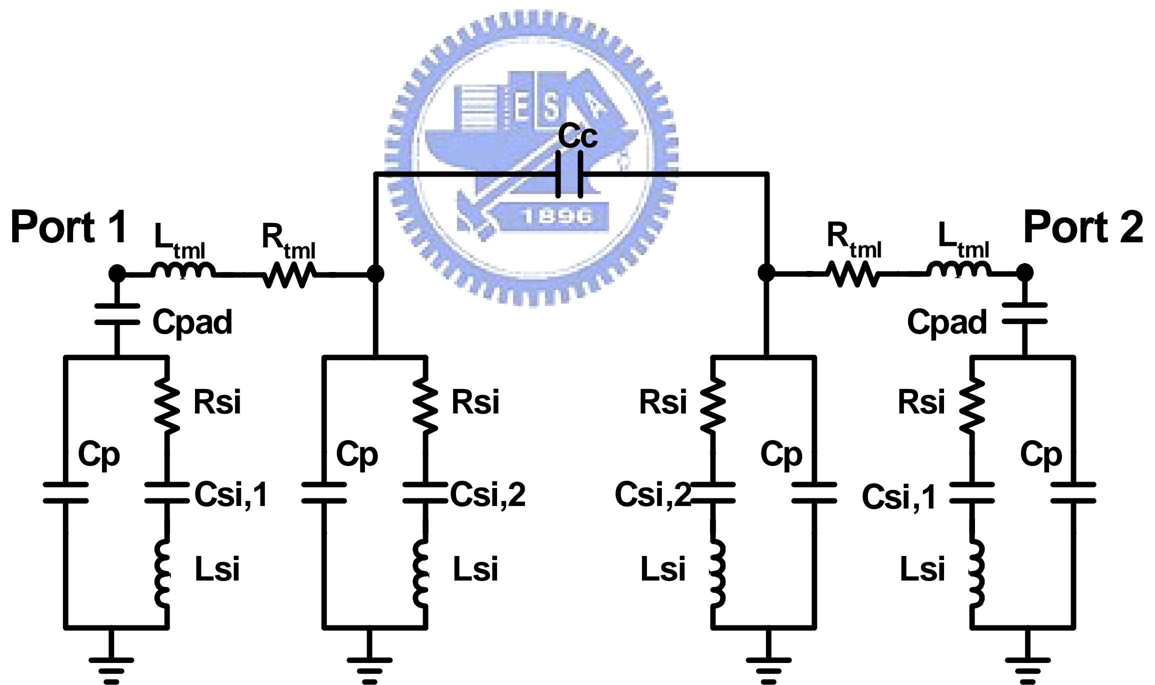


Fig. 5.4 Proposed equivalent circuit of open pad model (Model 4)

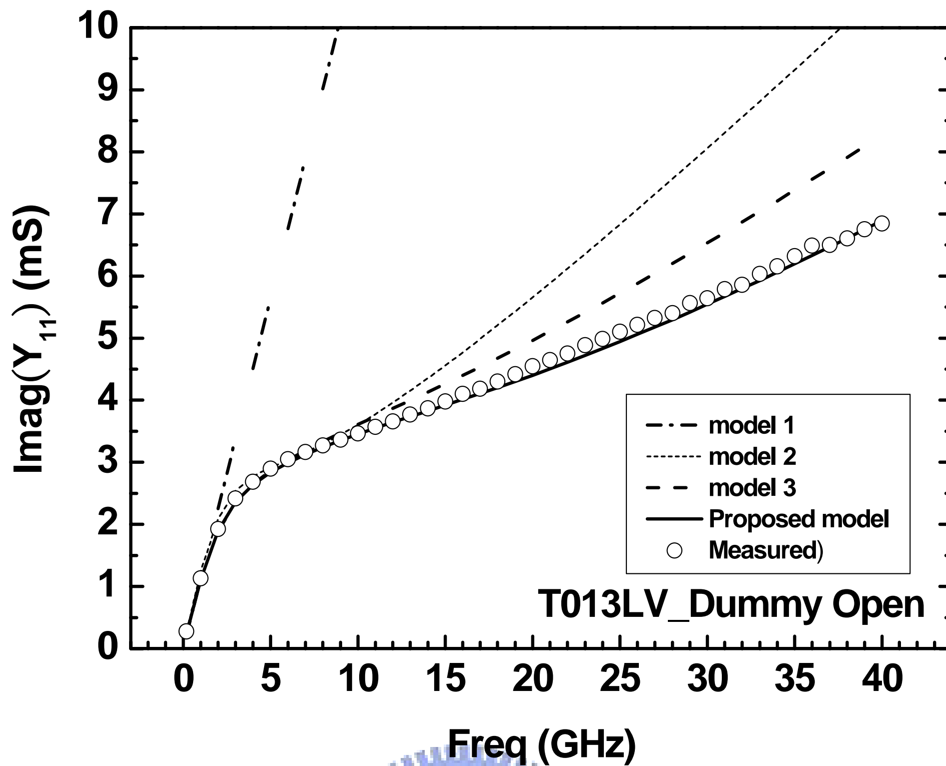


Fig. 5.5 Imaginary part of Y_{11} measured and simulated by different equivalent open pad model.

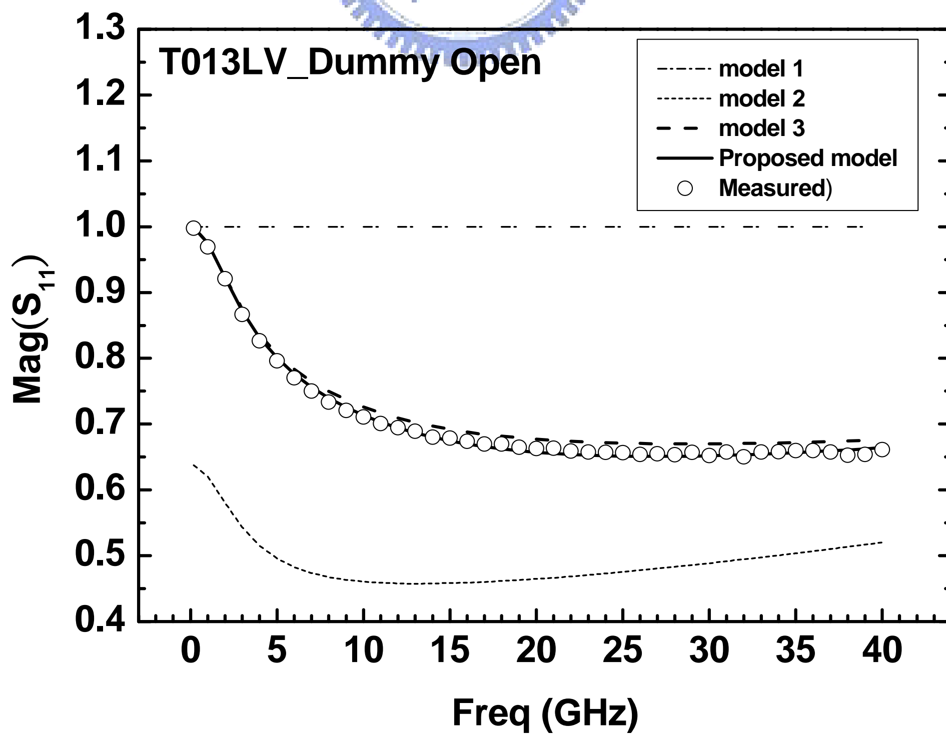


Fig. 5.6 Magnitude of S_{11} measured and simulated by different equivalent open pad model.

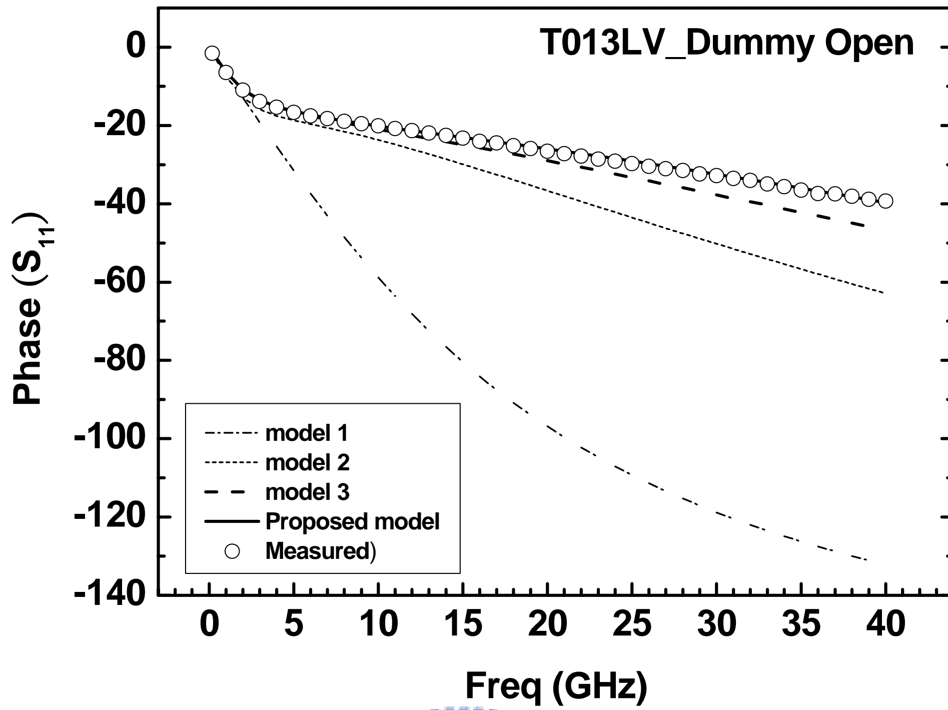


Fig. 5.7 Phase of S_{11} measured and simulated by different equivalent open pad model.

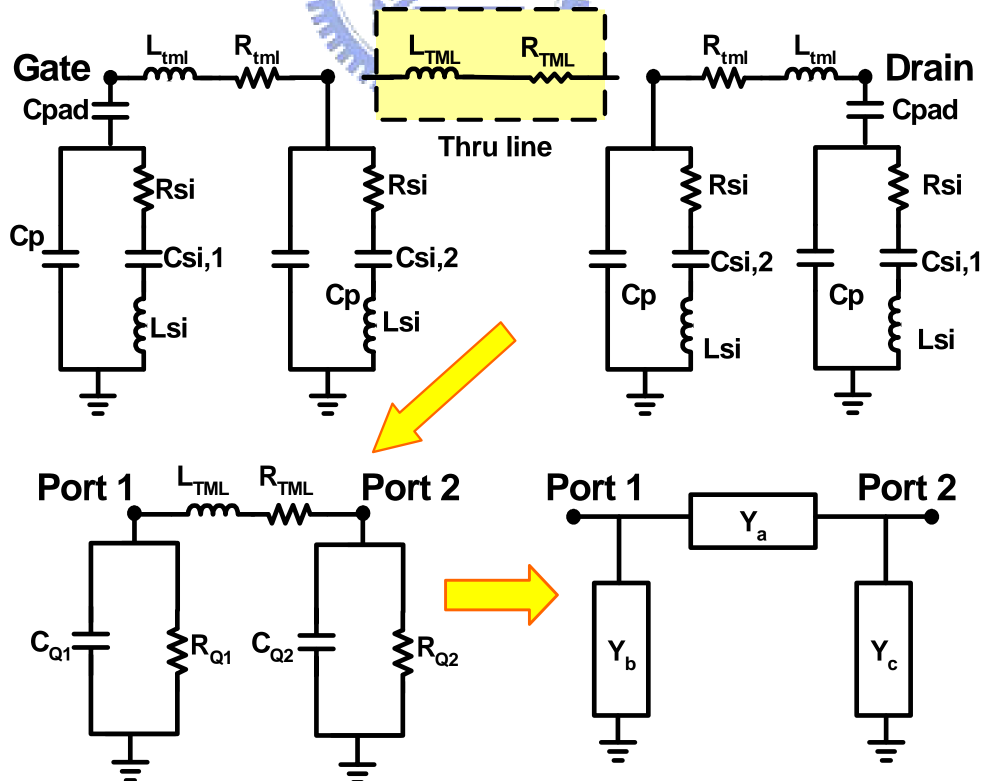


Fig. 5.8 (a) Equivalent circuit model derivation by circuit analysis

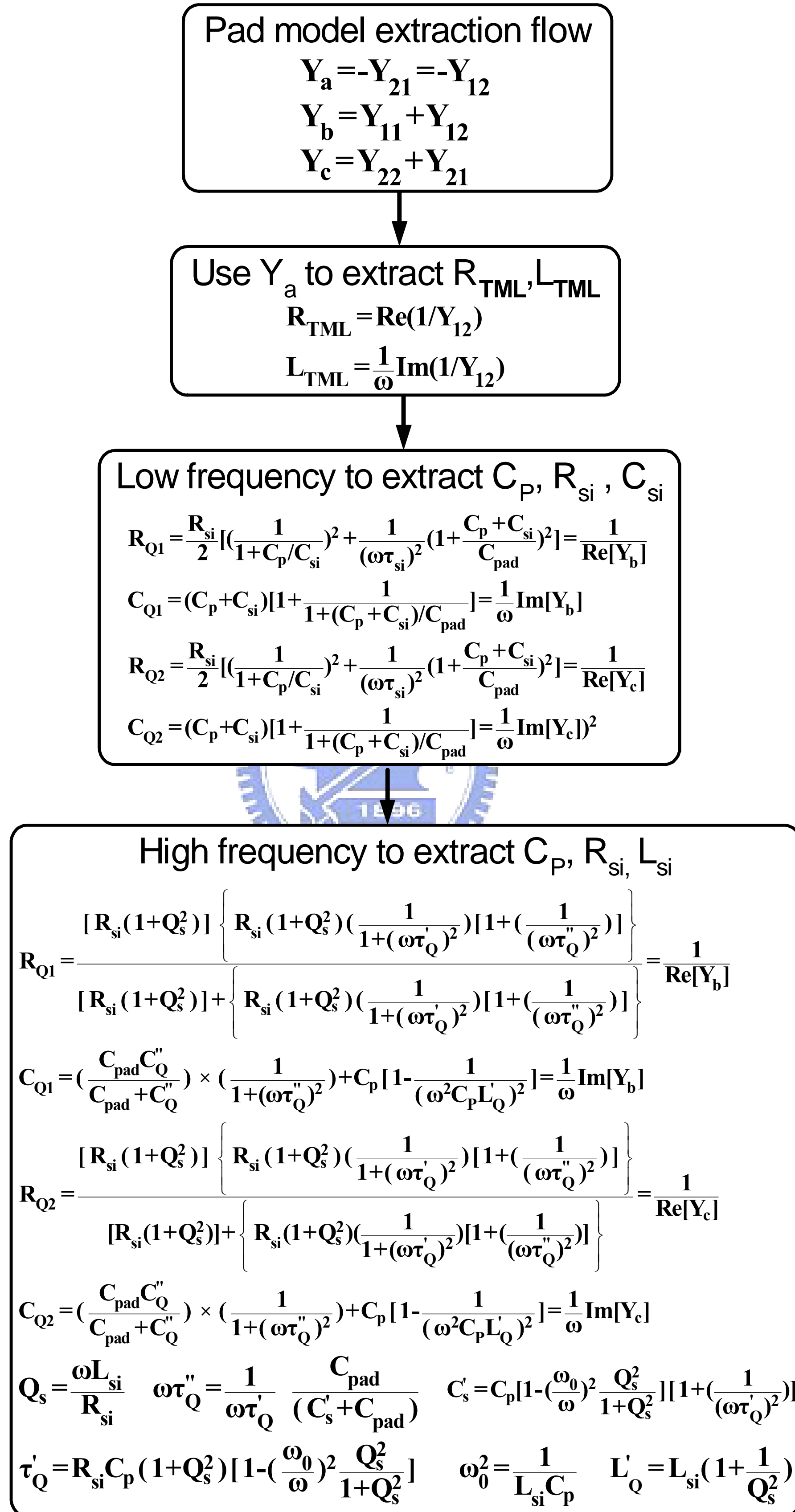


Fig. 5.8(b) Pad model parameter extraction flow.

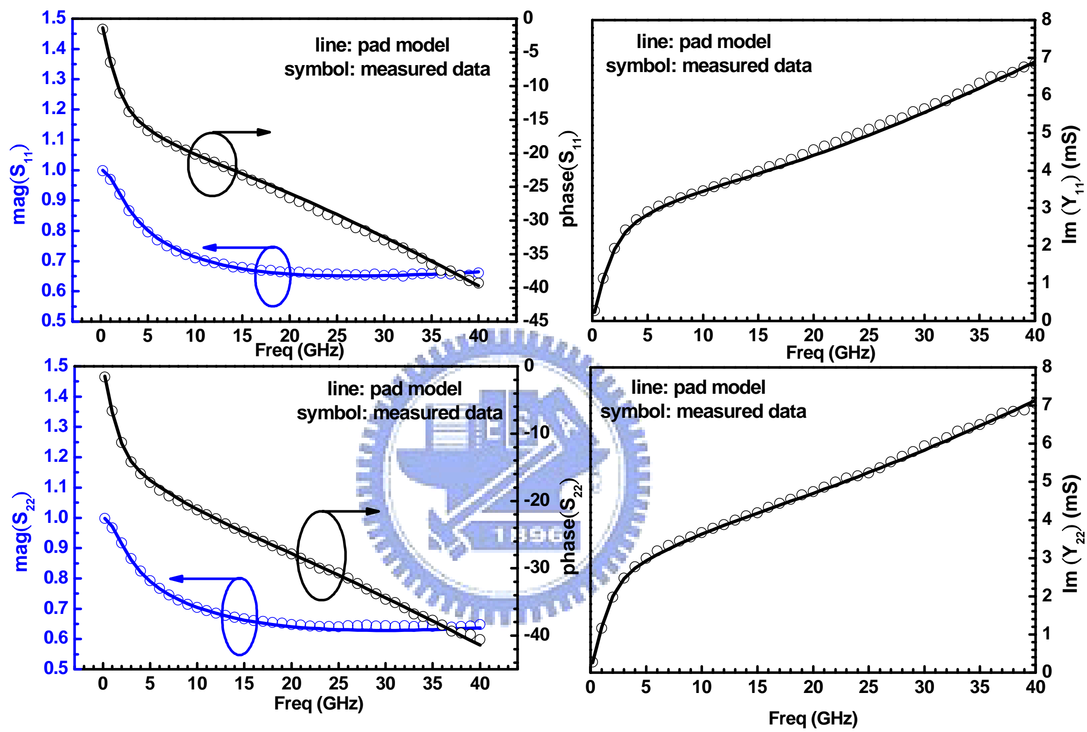


Fig. 5.9 Simulation and measurement of open pad S_{11}, S_{22}, Y_{11}, and Y_{22}.

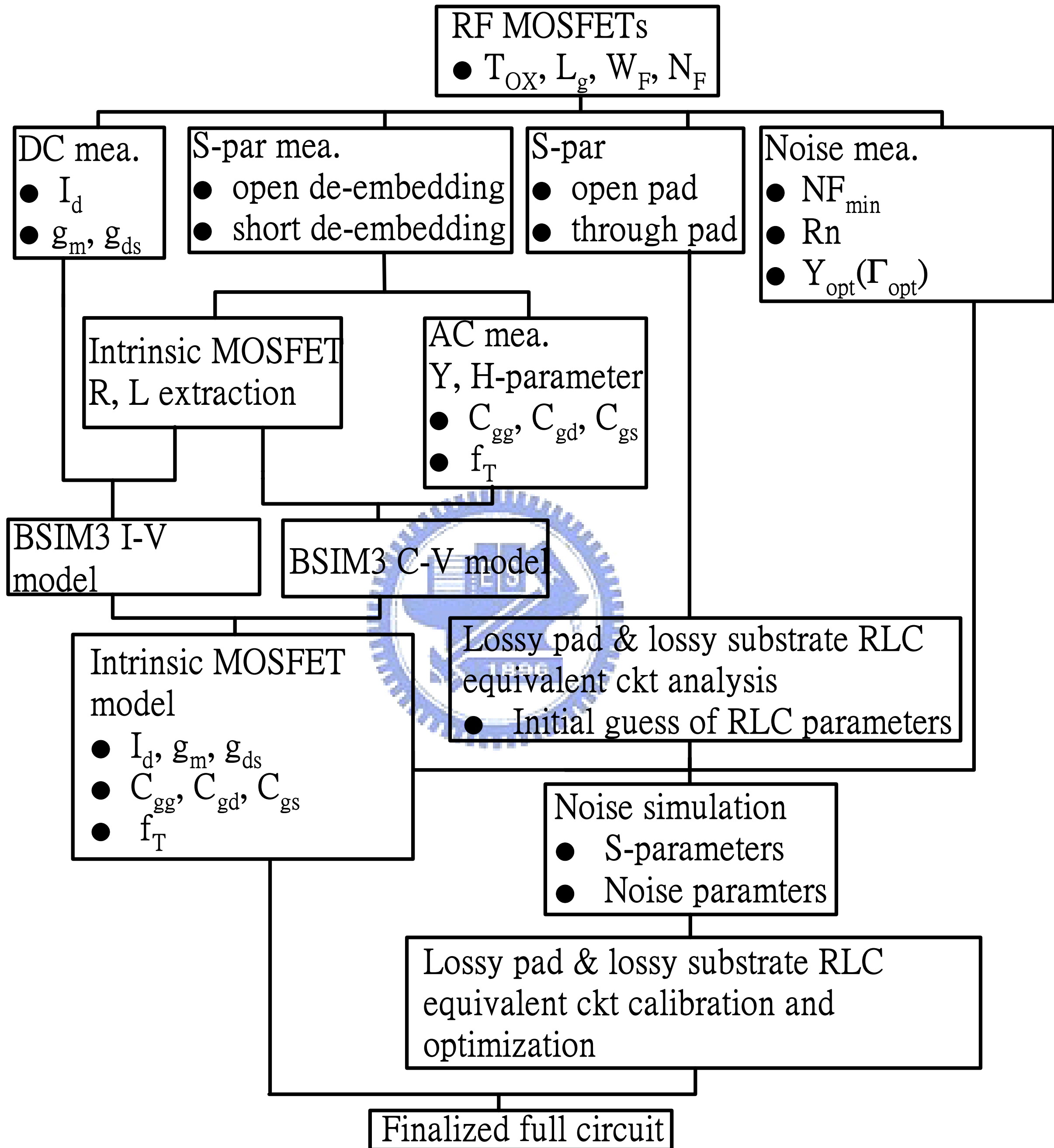


Fig. 5.10 MOSFETs device modeling items and modeling flow.

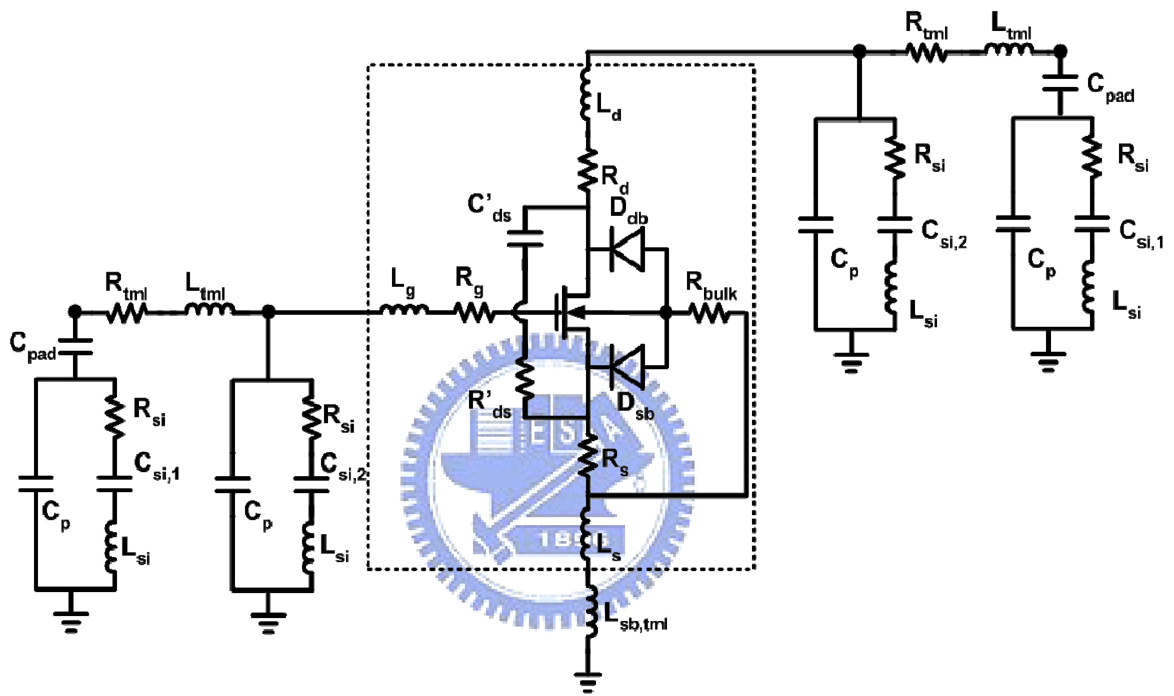


Fig. 5.11 Full circuit model MOSFETs device modeling items and modeling flow.

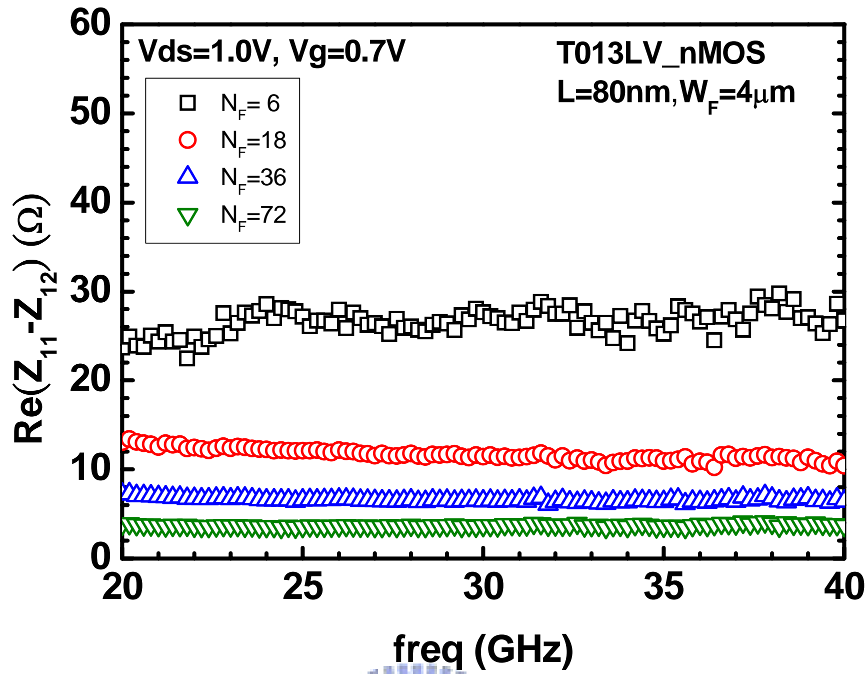


Fig. 5.12(a) R_g extracted from real part of $(Z_{11}-Z_{12})$ for 80nm DUT.

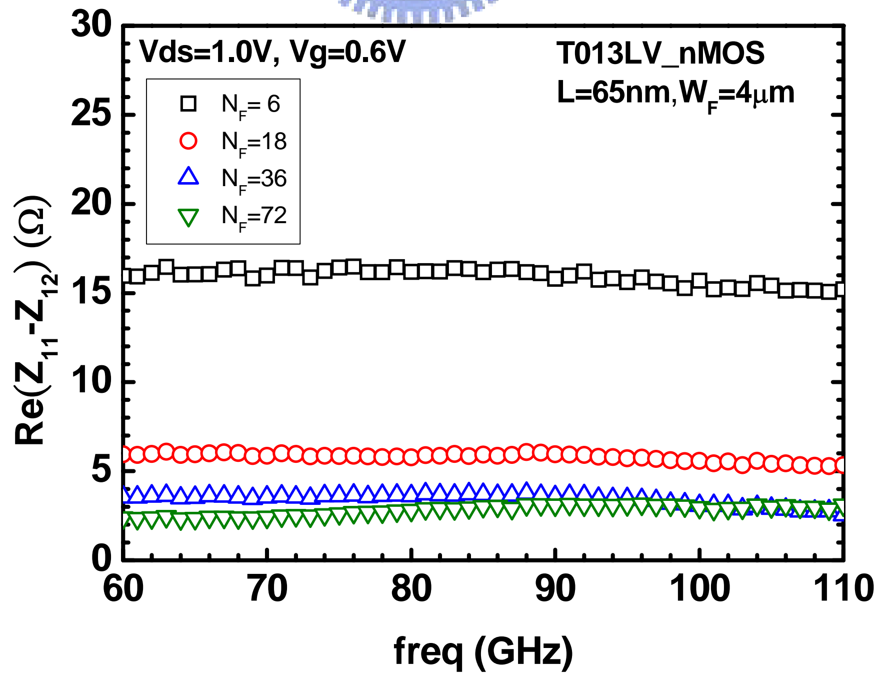


Fig. 5.12(b) R_g extracted from real part of $(Z_{11}-Z_{12})$ for 65nm DUT.

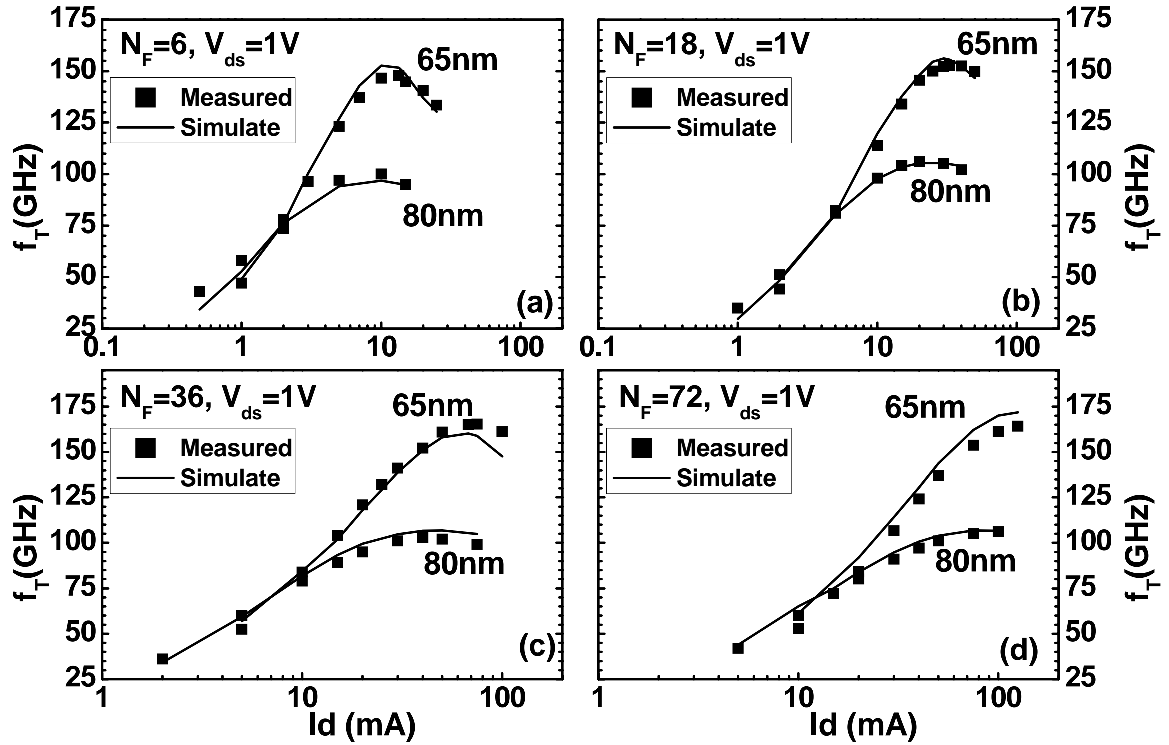


Fig. 5.13 Measured and simulation f_T for 80nm and 65nm DUT.

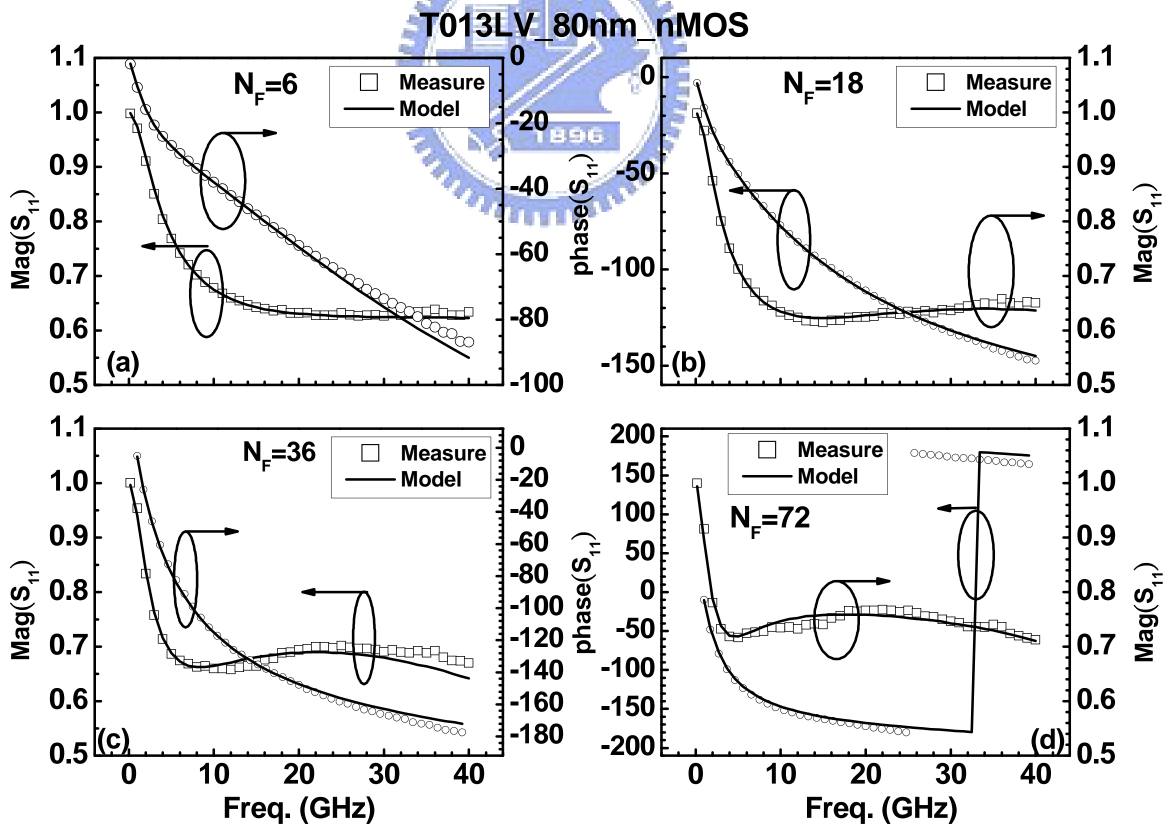


Fig. 5.14 (a) Measured S_{11} for gate terminal and good fit by simulation using the proposed RLC circuit. (80nm nMOS with $N_F = 6, 18, 36, 72$)

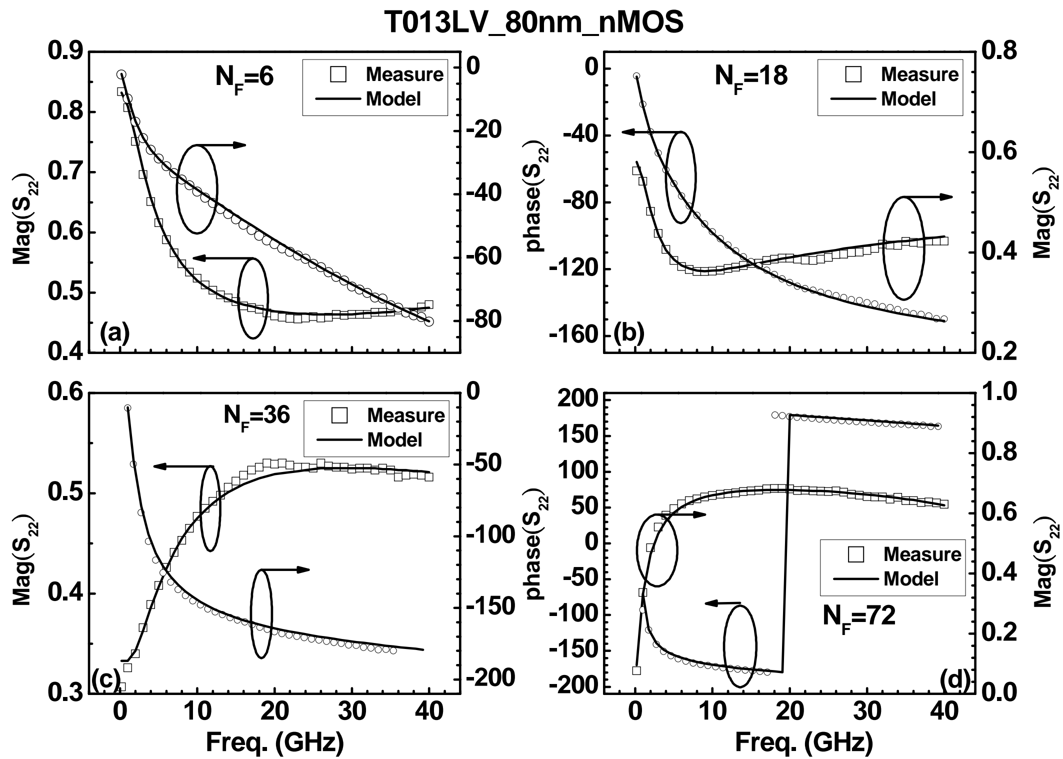


Fig. 5.14 (b) Measured S_{22} for drain terminal and good fit by simulation using the proposed RLC circuit. (80nm nMOS with $N_F = 6, 18, 36, 72$)

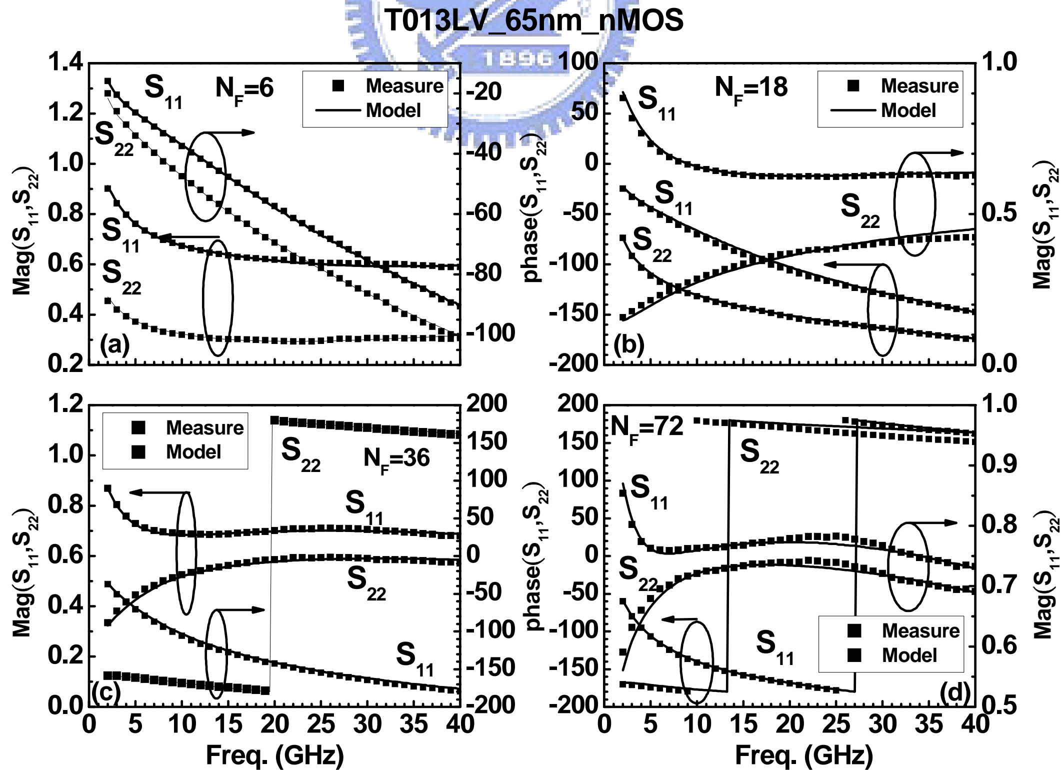


Fig. 5.14 (c) Measured S_{11} and S_{22} for gate and drain terminal and good fit by simulation using the proposed RLC circuit. (65nm nMOS with $N_F = 6, 18, 36, 72$)

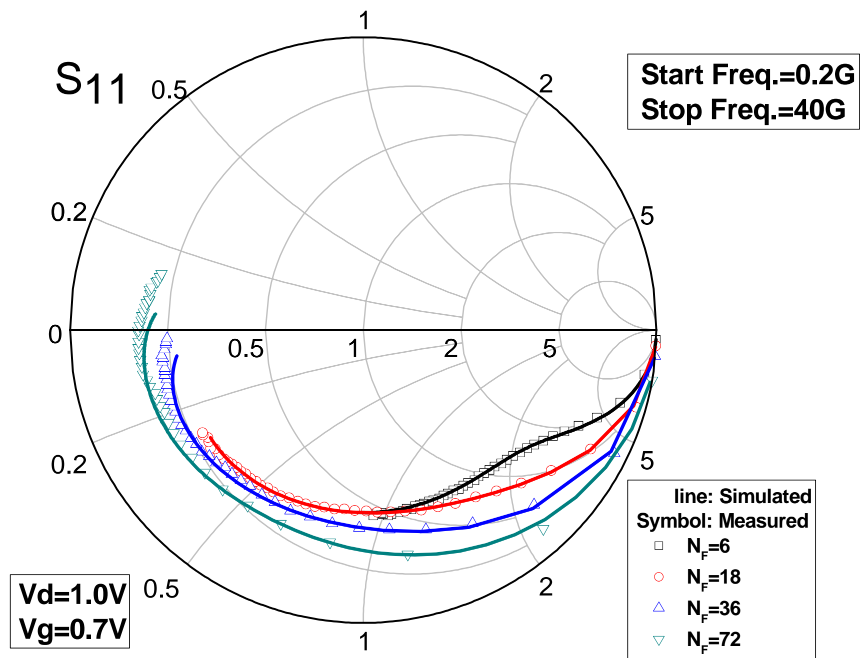


Fig. 5.15(a) Smith chart of measured S_{11} for DUT and good match by simulation using proposed circuit (80nm nMOS with $N_F = 6, 18, 36, 72$)

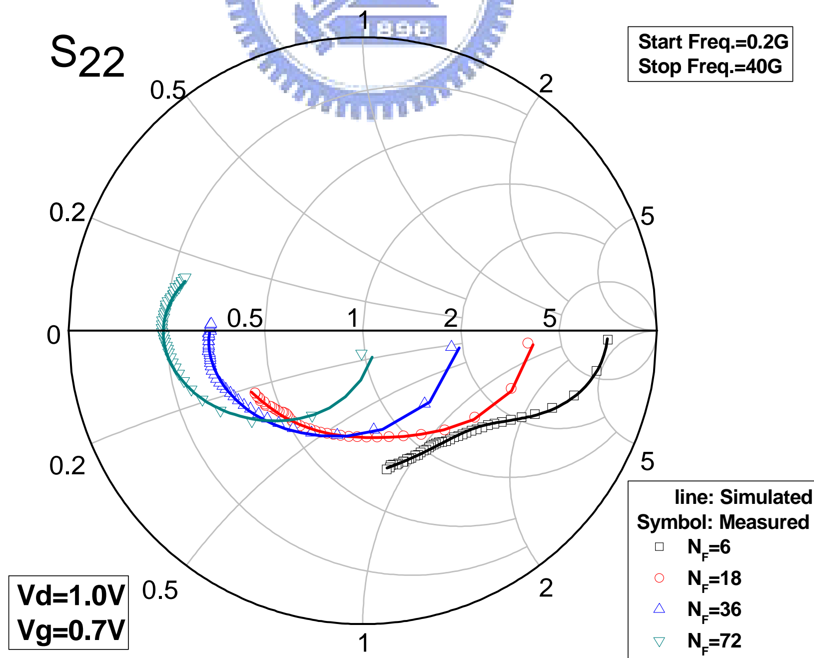


Fig. 5.15(b) Smith chart of measured S_{22} for DUT and good match by simulation using proposed circuit (80nm nMOS with $N_F = 6, 18, 36, 72$)

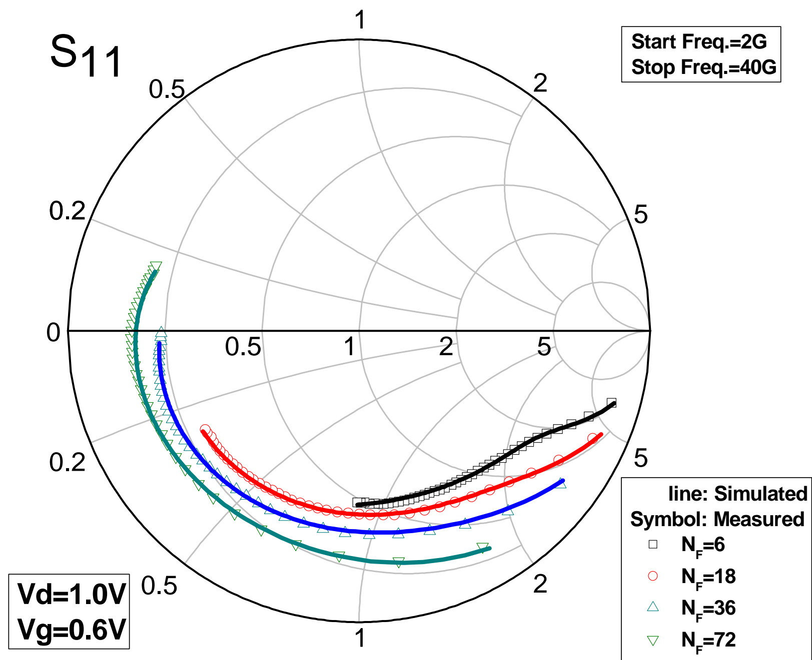


Fig. 5.16(a) Smith chart of measured S_{11} for DUT and good match by simulation using proposed circuit (65nm nMOS with N_F = 6, 18, 36, 72)

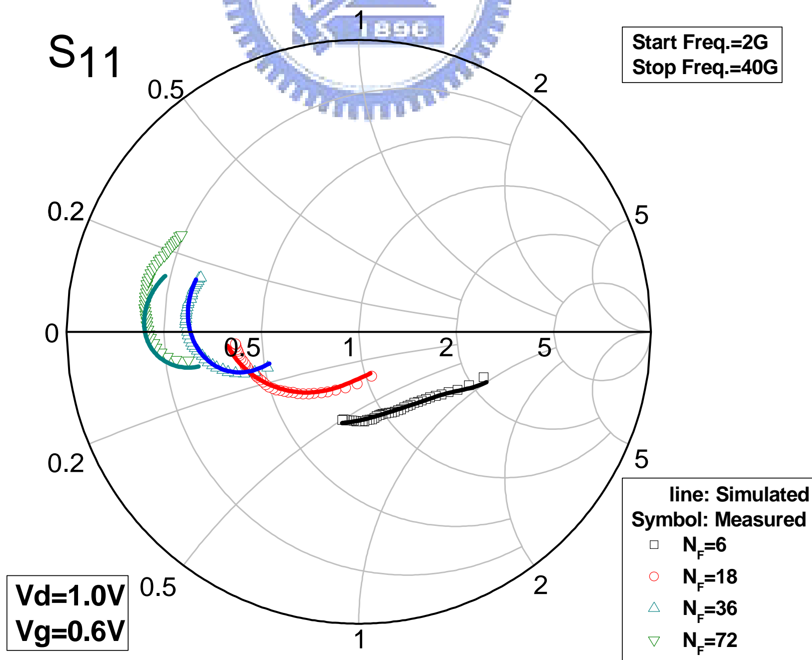


Fig. 5.16(b) Smith chart of measured S_{11} for DUT and good match by simulation using proposed circuit (65nm nMOS with N_F = 6, 18, 36, 72)

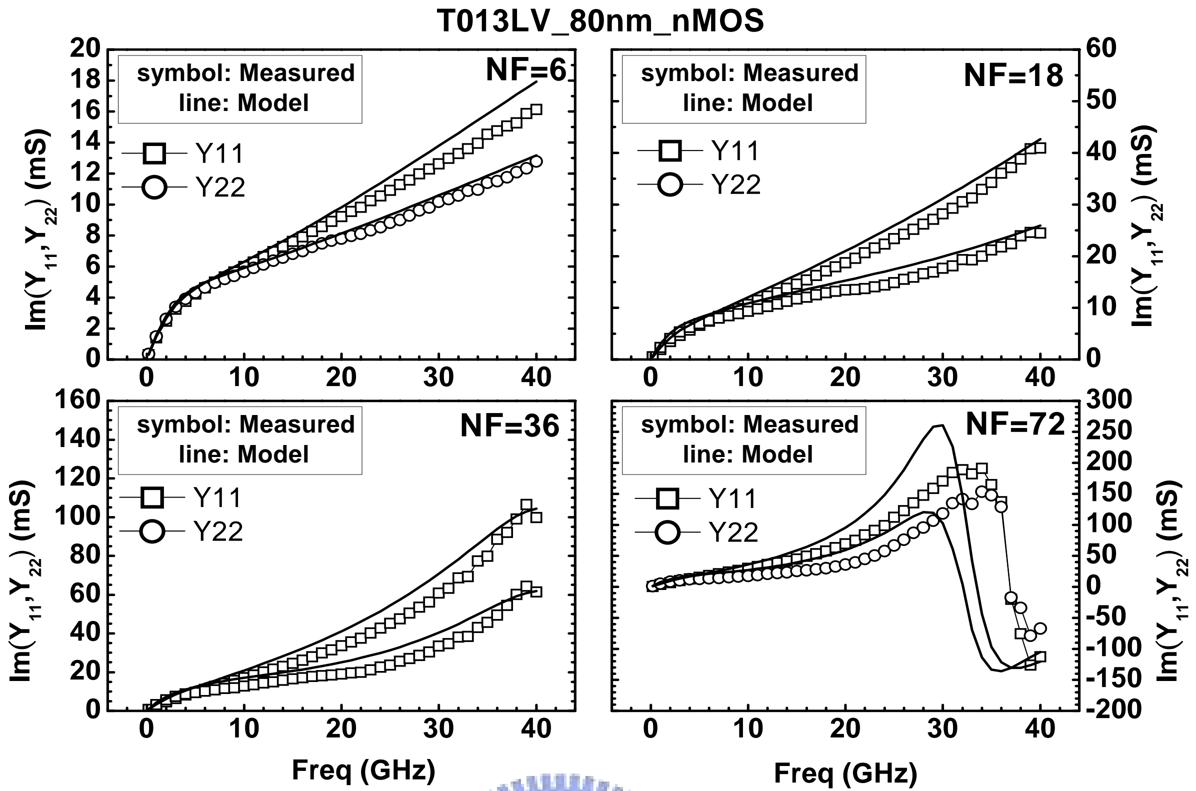


Fig. 5.17(a) Measured Y_{11} and Y_{22} with good fit by simulation of 80nm nMOS

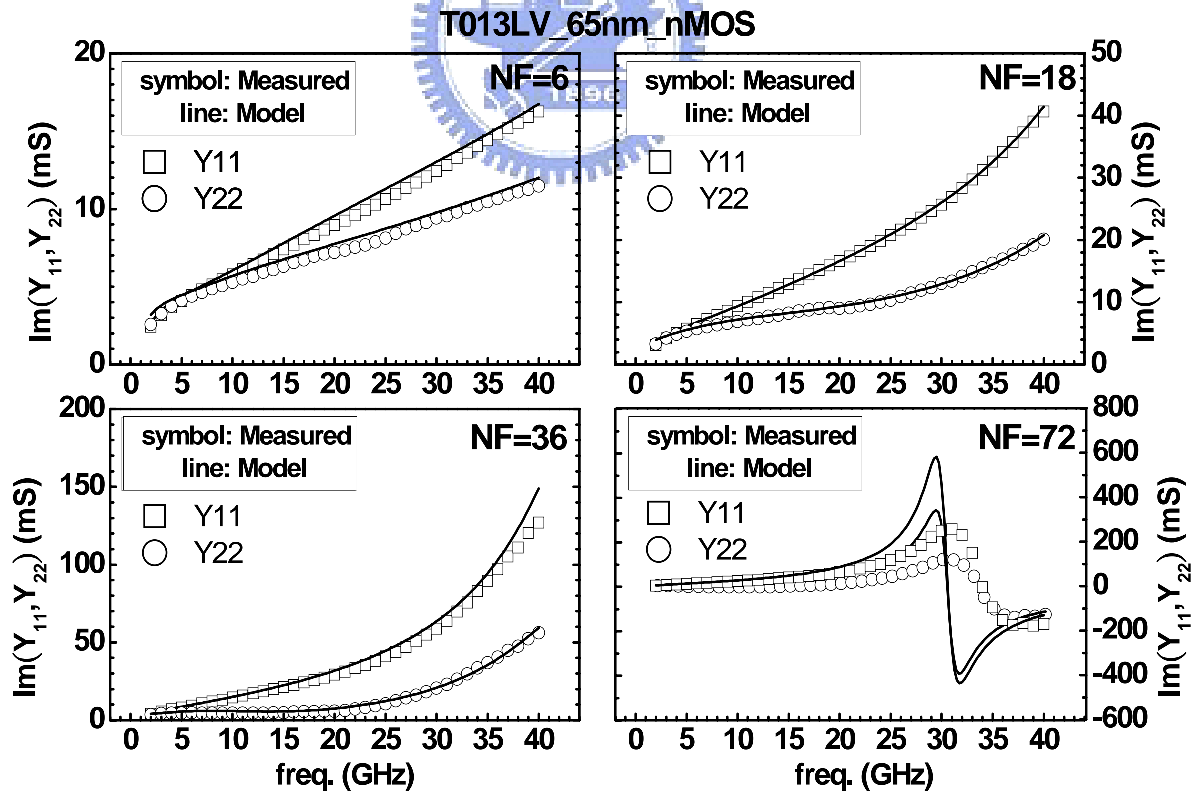


Fig. 5.17(b) Measured Y_{11} and Y_{22} with good fit by simulation of 65nm nMOS

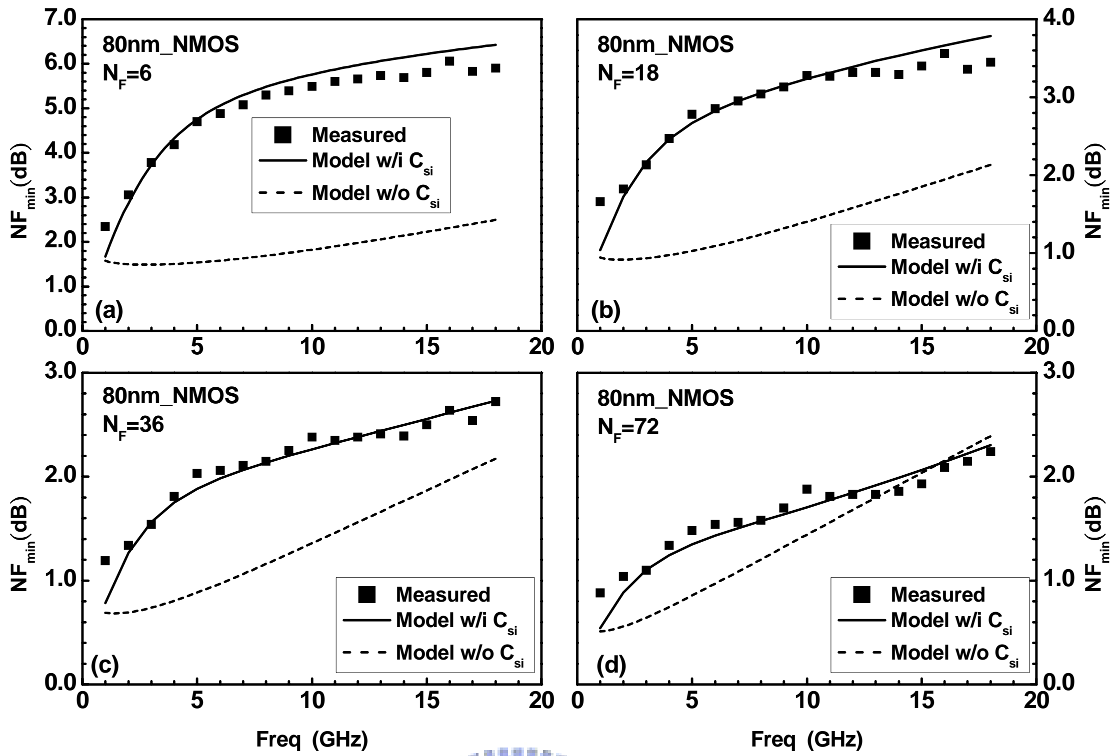


Fig. 5.18 Extrinsic results of measured and simulation NF_{min}, C_{si} effect is demonstrated for 80nm nMOS (N_F = 6, 18, 36, 72).

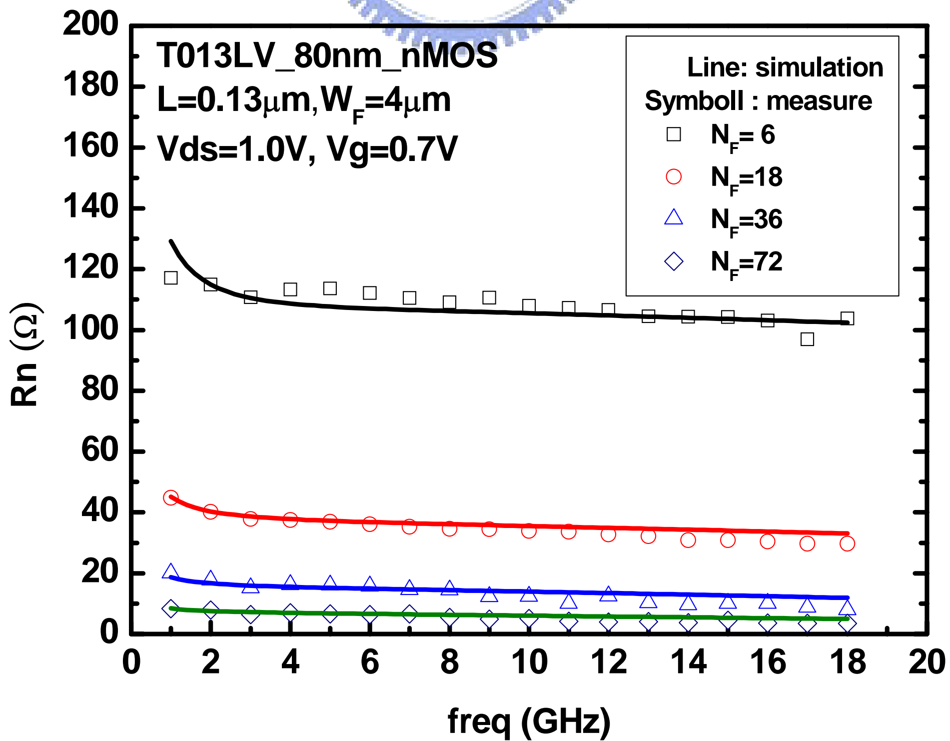


Fig. 5.19 Extrinsic results of measured and simulation R_n for 80nm nMOS (N_F = 6, 18, 36, 72)

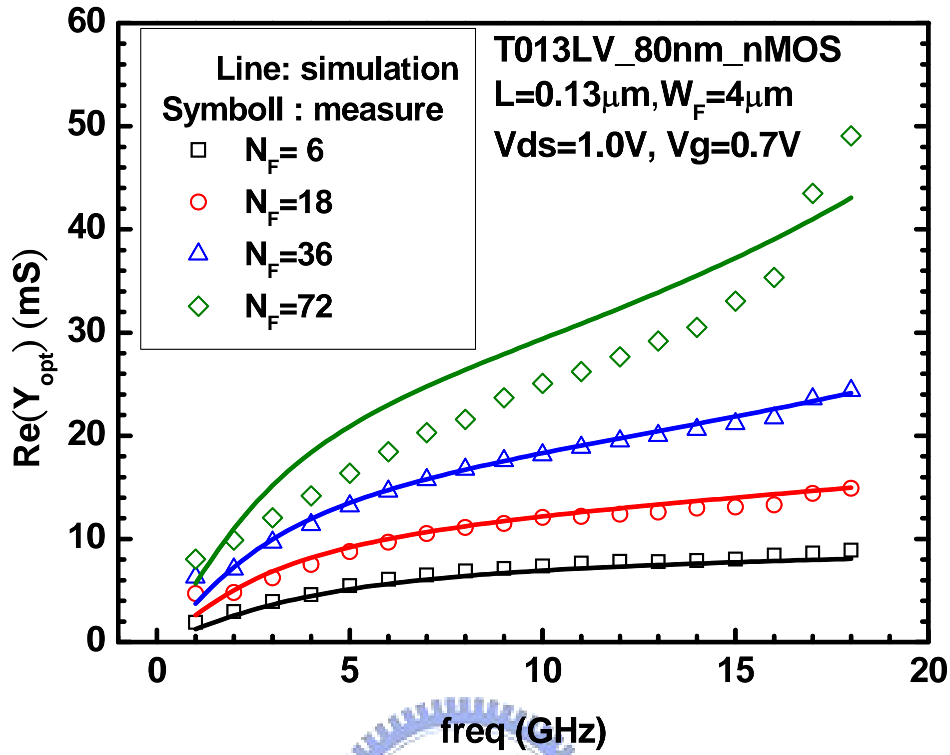


Fig. 5.20(a) Extrinsic results of measured and simulation Re(Y_{sopt}) of for 80nm nMOS

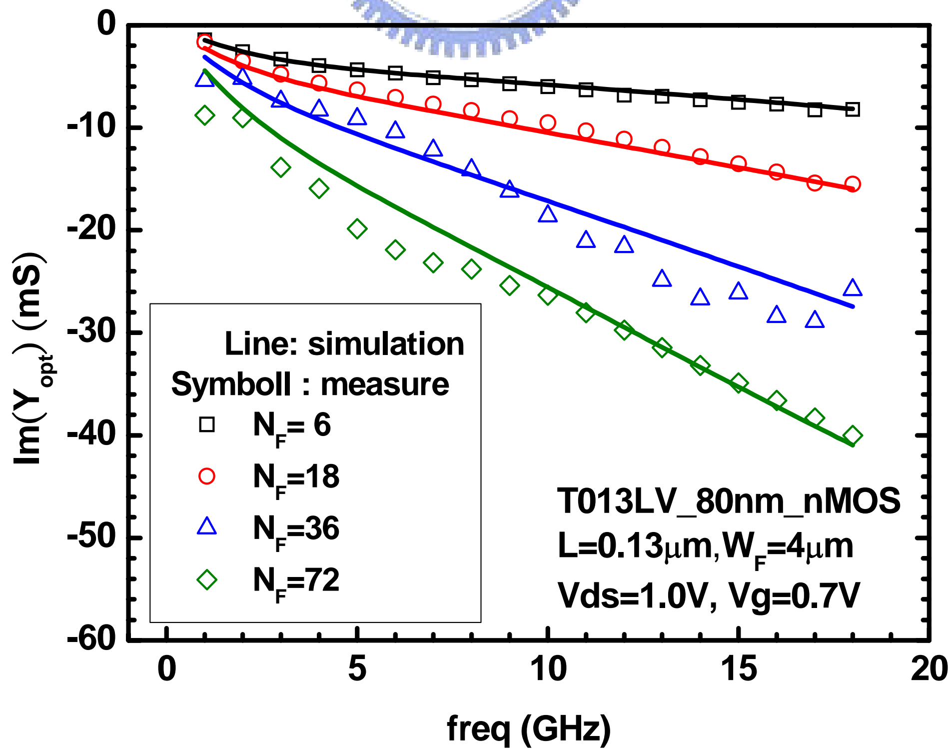


Fig. 5.20(b) Extrinsic results of measured and simulation Im(Y_{sopt}) of for 80nm nMOS

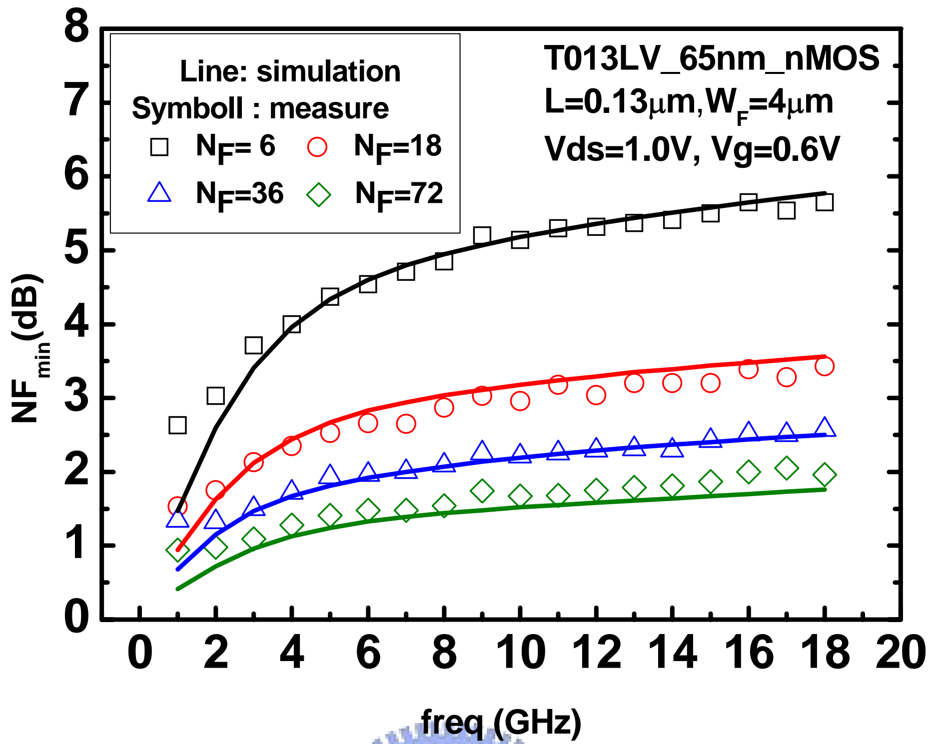


Fig. 5.21 Extrinsic results of measured and simulation NF_{min} for 65nm nMOS

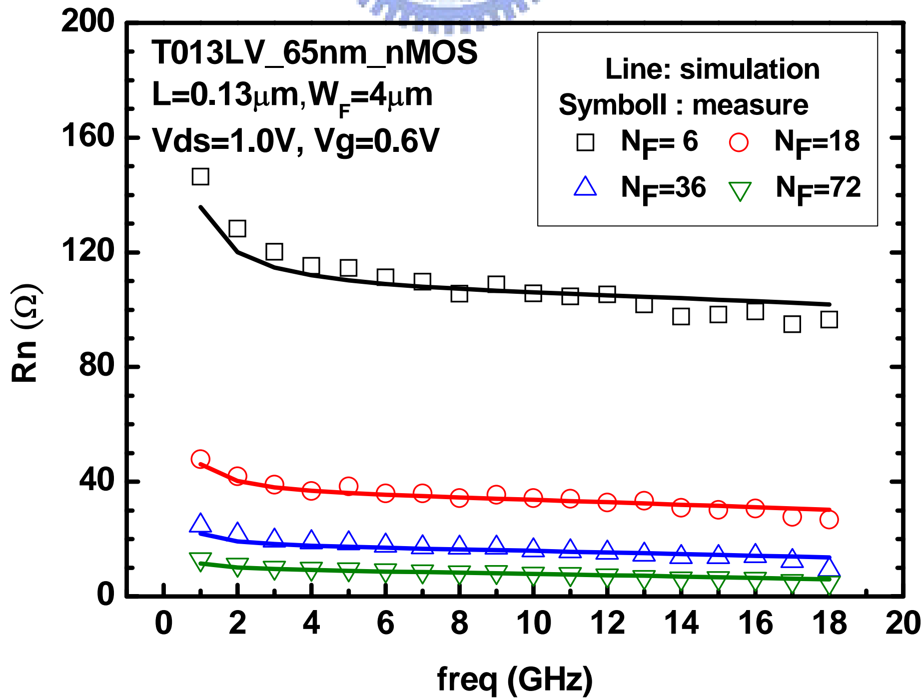


Fig. 5.22 Extrinsic results of measured and simulation R_n for 65nm nMOS

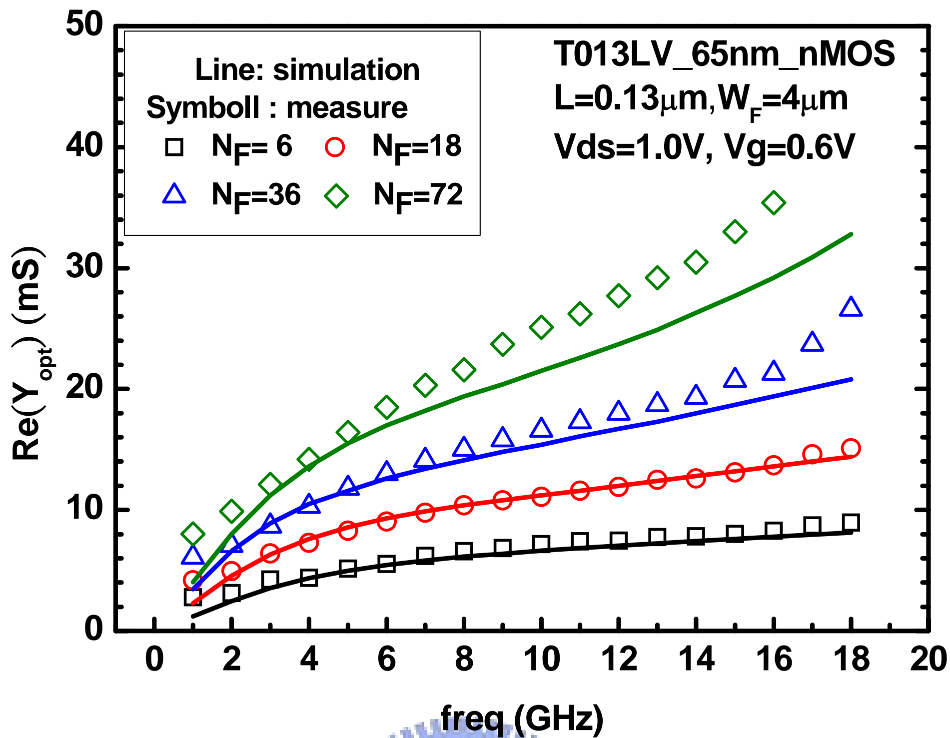


Fig. 5.23(a) Extrinsic results of measured and simulation Re(Y_{sopt}) of for 65nm nMOS

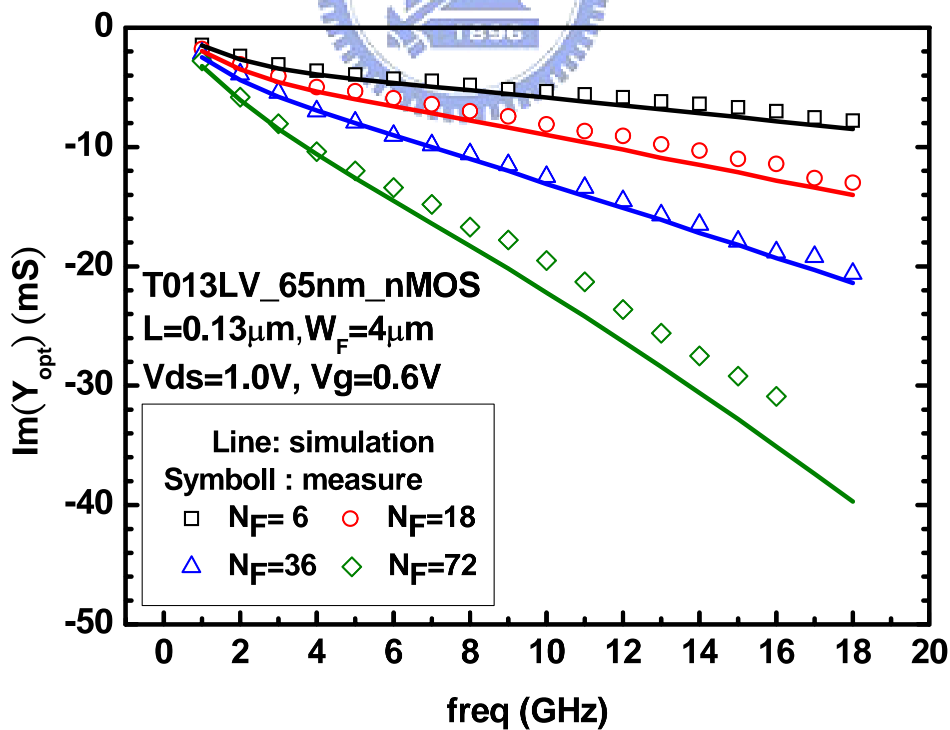


Fig. 5.23(b) Extrinsic results of measured and simulation Im(Y_{sopt}) of for 65nm nMOS

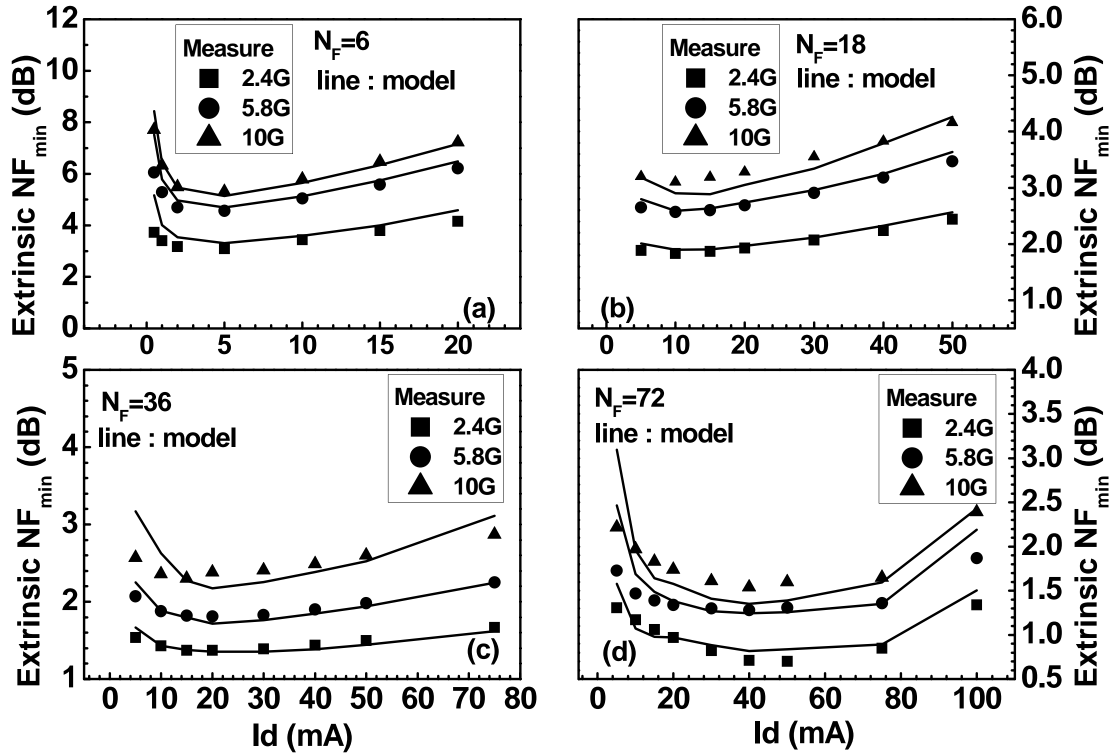


Fig. 5.24(a) Extrinsic results of measured and simulation NF_{min} under various drain current at frequency 2.4GHz, 5.8GHz, and 10GHz for 80nm nMOS.

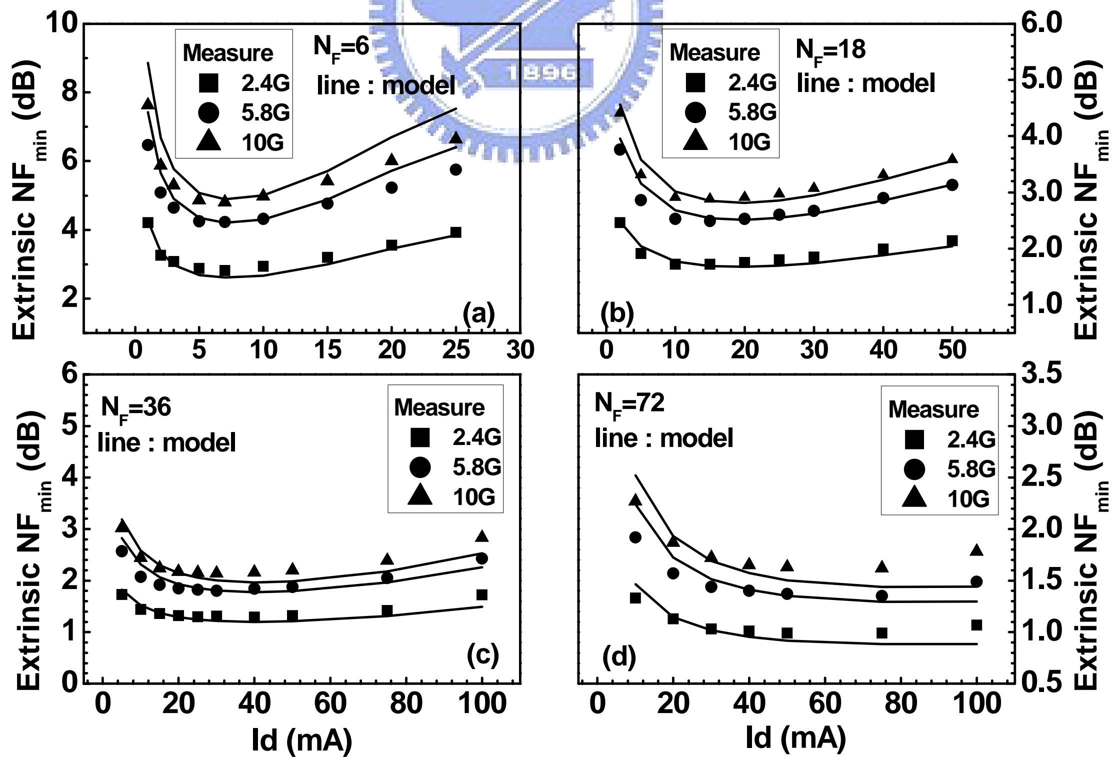


Fig. 5.24(b) Extrinsic results of measured and simulation NF_{min} under various drain current at frequency 2.4GHz, 5.8GHz, and 10GHz for 65nm nMOS.

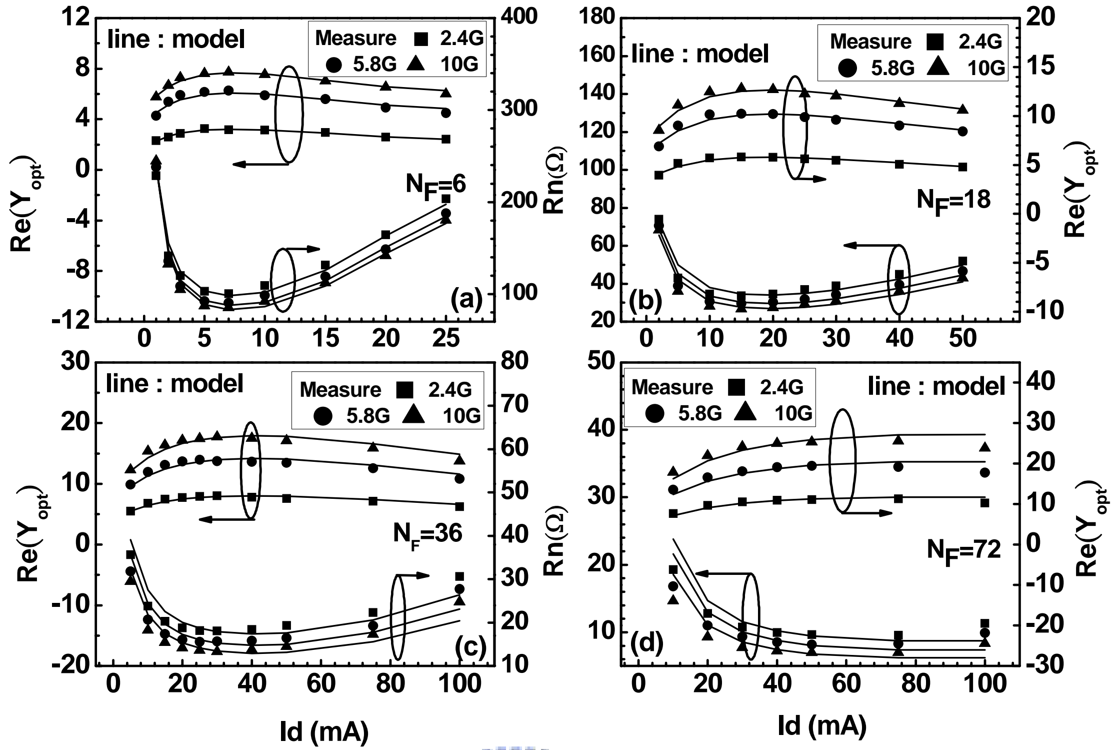


Fig. 5.25 Extrinsic results of measured and simulation Re(Y_{sopt}) and R_n under various I_d at frequency 2.4GHz, 5.8GHz, an 10GHz for 65nm nMOS (N_F = 6, 18, 36, 72).

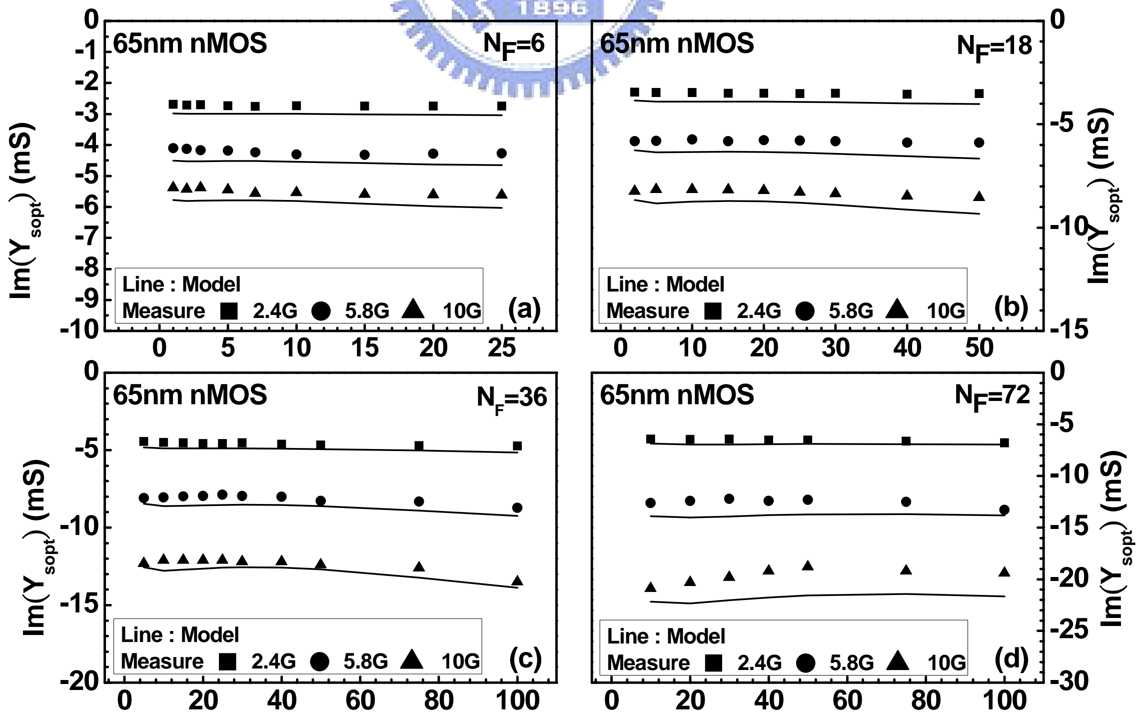


Fig. 5.26 Extrinsic results of measured and simulation Im(Y_{sopt}) under various I_d at frequency 2.4GHz, 5.8GHz, an 10GHz for 65nm nMOS (N_F = 6, 18, 36, 72).

Chapter 6

RF MOSFET Intrinsic Noise Extraction and Simulation

6.1 MOSFET Intrinsic Noise Parameter Analysis

Intrinsic noise extraction and modeling for miniaturized MOSFETs is the main objective of this study. Accurate extraction of intrinsic device performance and parameters is essential to improve device modeling accuracy and help circuit design. The method developed in this work for intrinsic noise extraction is an equivalent circuit approach named as "lossy substrate de-embedding method". In previous chapters, a lossy substrate model has been described and proven with excellent accuracy over varying frequencies and gate biases (drain currents) as well as devices of various gate lengths and finger numbers (N_F = 6, 18, 36, and 72, L_g = 80nm and 65nm). Based on the proven lossy substrate model and calibrated intrinsic MOSFET model, lossy substrate de-embedding can be done simply by removing the elements of the lossy pad and substrate R-L-C networks from the full circuit model in Fig. 5.15. The parasitics resistance R_g, R_d, R_s, and R_{bulk}, which cannot be removed through general de-embedding were left with intrinsic model to account for the excess noise. This "resistance induced excess noise" cannot be eliminated even through conventional noise correlation matrix de-embedding or lossy substrate de-embedding developed in this work.

Fig. 6.1 ~ Fig. 6.4 present intrinsic noise parameters and comparison with measured data for 80nm and 65nm nMOS of various N_F. The intrinsic noise parameters extracted through lossy substrate de-embedding by using circuit simulation will be verified through comparison with the measured ones before de-embedding. Intrinsic R_n has almost the same level as measured ones. For 80nm devices, a little smaller value than measured data was obtained for small N_F and the difference tends to decrease as N_F increases. As for 65nm devices, following similar trend as 80nm devices did at low frequency but the frequency dependence changed a

little at high frequency and even larger than the measured one.

The minor change of R_n after de-embedding suggests that the sensitivity of NF_{min} with respect to the source admittance (Y_s) deviation from its optimum source admittance (Y_{sopt}) target did not make significant difference due to lossy substrate effect. Another feature is that 80nm device has lower R_n compared with 65nm ones no matter whether extrinsic or intrinsic. It means that the noise figure is less sensitive to the mismatch between Y_s and Y_{sopt} for 80nm devices. The extracted intrinsic Re(Y_{sopt}) and Im(Y_{sopt}) were compared with extrinsic Y_{sopt} (measured or simulated) to identify the effect through lossy substrate de-embedding. Both Re(Y_{sopt}) and Im(Y_{sopt}) reveal obvious reduction in magnitude for the intrinsic components as the result of equivalent circuit de-embedding. According to equation (A-13), if correlation admittance (Y_c) is assumed to be purely imaginary under the assumption that correlation coefficient c is a purely imaginary value. The noise factor F can be expressed as

$$F_{min} = 1 + 2R_n G_{sopt} = 1 + 2R_n \cdot \mathrm{Re}\left(Y_{sopt}\right) \qquad (6\text{-}1)$$

The obvious reduction of Re(Y_{opt}) through de-embedding contributes to the significant suppression of NF_{min}. Another important feature is that the nonlinear frequency dependence of Re(Y_{sopt}) before de-embedding was recovered to linear characteristics for intrinsic Re(Y_{sopt}) after lossy substrate de-embedding. This is the main factor that recovers linear frequency dependence for intrinsic NF_{min}. Great difference between extrinsic and intrinsic NF_{min} reflects the need for measured NF_{min} de-embedding. Fig. 6.5 shows the intrinsic noise extracted under two gate bias conditions corresponding to maximum g_m (or f_T) and minimum NF_{min}. Obviously lower NF_{min} was demonstrated for 65nm devices as compared with 80nm ones. The improvement on NF_{min} reflects the gain in f_T from gate length scaling and shows weak dependence on finger number. The NF_{min} at 10GHz can be suppressed to less than 0.8 dB for 80nm and 0.5dB for 65nm nMOS corresponding to an optimized drain current.

Finally, noise parameters corresponding to varying drain current are presented in Fig. 6.6 ~ Fig. 6.9. They manifest two important clues: As N_F increases, it tends to shift the minimum NF_{min} to higher current operation. This makes it impossible to implement a low noise and low power circuit while using large N_F device. Noise suppression due to gate length scaling becomes even more significant in higher current region. Analytical expression related NF_{min} to devices parameters as follows:

$$F_{min} = 1 + K_1 \cdot \frac{f}{f_T}\sqrt{g_m(R_g + R_s)} = 1 + K_2 \cdot f \cdot C_{gs} \cdot \sqrt{\frac{(R_g + R_s)}{g_m}} \quad (6\text{-}2)$$

Larger finger number leads to smaller gate resistance and higher transconductance g_m but pay the penalty of higher gate capacitance C_{gs}. The overall performance of larger N_F device compared with small N_F ones are higher gain and higher f_{max} with almost same level of minimum NF_{min} and f_T but consume more power and area. Information shown above provides useful guidelines for RF CMOS design and optimization in terms of speed, power, and noise.

6.2 MOSFET noise current analysis

Detailed derivation of relation between noise current ($\overline{i_g^2}$, $\overline{i_d^2}$ and $\overline{i_g i_d^*}$) and noise parameters (F_{min}, R_n, G_{opt} and B_{opt}) by using correlation matrix leads to the following expression:

$$\overline{i_g^2} = 4kT\Delta f \cdot R_n \cdot [|Y_{opt}|^2 + |Y_{11}|^2 - 2 \cdot \mathrm{Re}(Y_{11} Y_c^*)] \quad (6\text{-}3)$$

$$\overline{i_d^2} = 4kT\Delta f \cdot R_n \cdot |Y_{21}| \quad (6\text{-}4)$$

$$\overline{i_g i_d^*} = 4kT\Delta f \cdot R_n \cdot (Y_{11} - Y_c) Y_{21}^* \quad (6\text{-}5)$$

where Y_c is given by

$$Y_c = \frac{F_{\min} - 1}{2R_n} - Y_{opt} \tag{6-6}$$

According to equations (6-3) to (6-6), noise currents and their correlation coefficient can be extracted from the noise parameters. In order to extract the noise currents of intrinsic MOSFETs, Y-parameters and four noise parameters used in the above formula should be intrinsic quantity too.

Intrinsic MOSFET model was used to calculate the noise currents to investigate the noise behavior of the sub-100nm devices. In addition to the intrinsic MOSFET noise currents of major concern, gate resistance effect on noise currents and NF_{min} was also an interesting topic. It is well known that gate resistance contributes significant thermal noise to the device. Fig. 6.10~Fig. 6.14 indicate the simulated R_g effect on noise performance in terms of NF_{min}, R_n, S_{id} and S_{ig}. R_g through comparison between the original intrinsic MOSFET model with R_g (Table 5.2a) and that with R_g set to zero. The simulation results suggest that NF_{min} of an intrinsic MOSFET is dominated by R_g and its NF_{min} can be reduced to lower than 0.2dB at 10GHz if R_g can be eliminated. This reduction is associated with the great decline of S_{ig} (Fig. 6.12). Excess S_{ig} due to R_g is introduced by means of gate capacitance in the form of [2]:

$$\Delta S_{ig} = 4kTR_g \omega^2 C_{gg}^2 \tag{6-7}$$

From (6-2), different R_g values of various N_F lead to almost the same NF_{min}, because NF_{min} is associated with $g_m R_g$ product. Drain current noise spectrum density (S_{id}) in Fig. 6.13 reveals almost frequency independent feature and shows smaller R_g effect. Through transconductance g_m, R_g contributes the excess S_{id} by

$$\Delta S_{id} = 4kTR_g g_m^2 \tag{6-8}$$

Validity of (6-7) and (6-8) was verified in Fig. 6.13 and Fig. 6.15. The S_{ig} difference to

$4kTR_g\omega^2 C_{gg}^2$ ratio and S_{id} difference to $4kTR_g g_m^2$ is very close to unity. Little deviation from unity at high frequency may be due to the fact that R_g was given as a frequency-independent constant excluding the non-quasi-static effect [27] or the C_{gg} and g_m were given as constants independent of frequency. S_{ig} and S_{id} are plotted together in Fig. 6.16. As operating frequency increases S_{ig} will eventually exceed S_{id}, but S_{ig} is about two orders smaller than S_{id} up to 18GHz. Though the reduction of NF_{min} and R_n are not only dominated by S_{id} and can be estimated from the relation between noise current and noise parameters [9] :

$$F_{min} \approx 1+\frac{2}{\sqrt{5}}\frac{f}{f_T}\sqrt{\gamma\delta(1-|c|^2)} \quad (6\text{-}9)$$

$$R_n \approx \gamma\frac{g_{do}}{g_m^2} \quad (6\text{-}10)$$

where γ, δ, and c are the coefficient already shown in Chapter two.

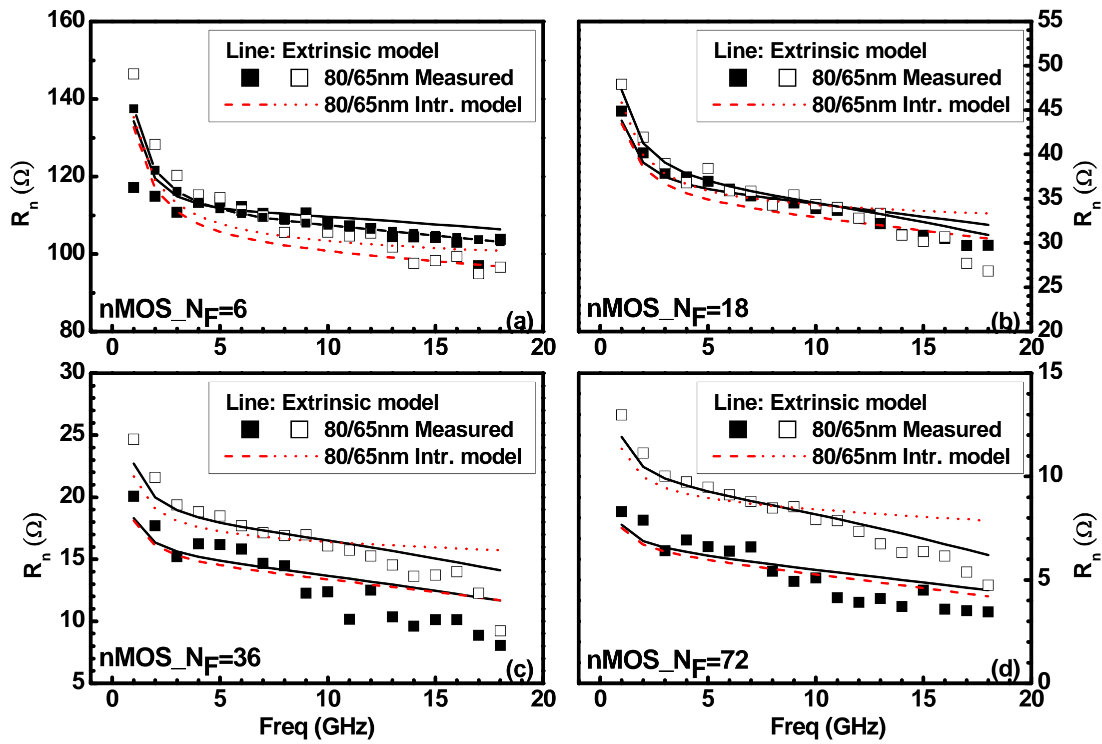


Fig. 6.1 Extrinsic measured and intrinsic simulation R_n for 80 and 65nm nMOS (N_F =6, 18, 36, 72)

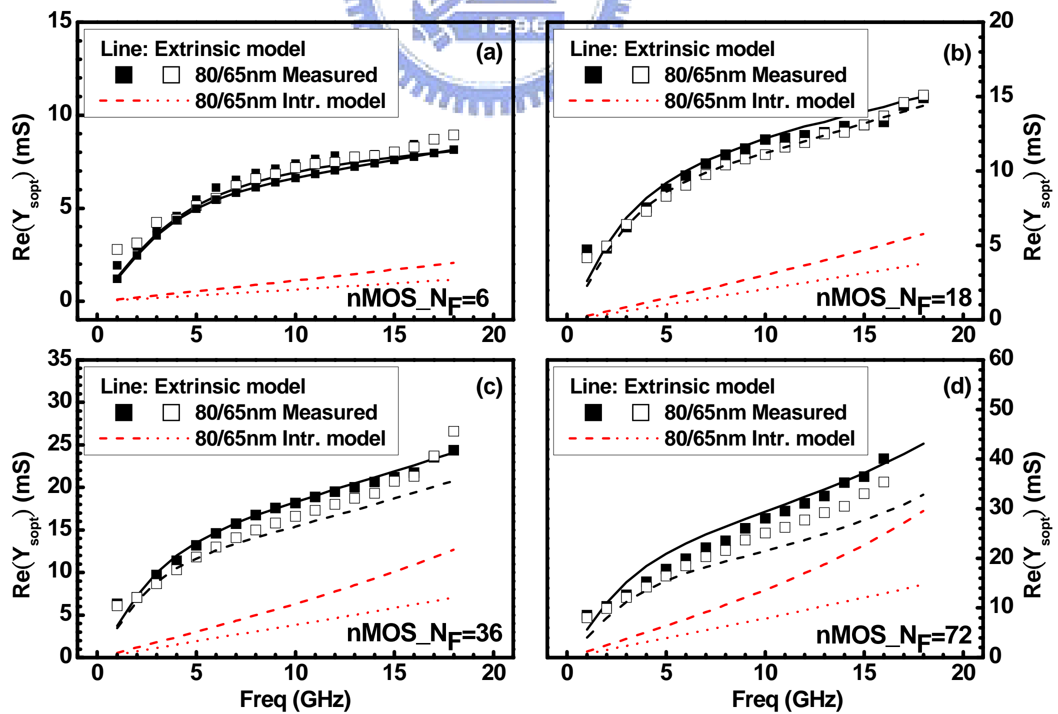


Fig. 6.2 Extrinsic measured and intrinsic simulation $Re(Y_{sopt})$ for 80 and 65nm nMOS (N_F =6, 18, 36, 72)

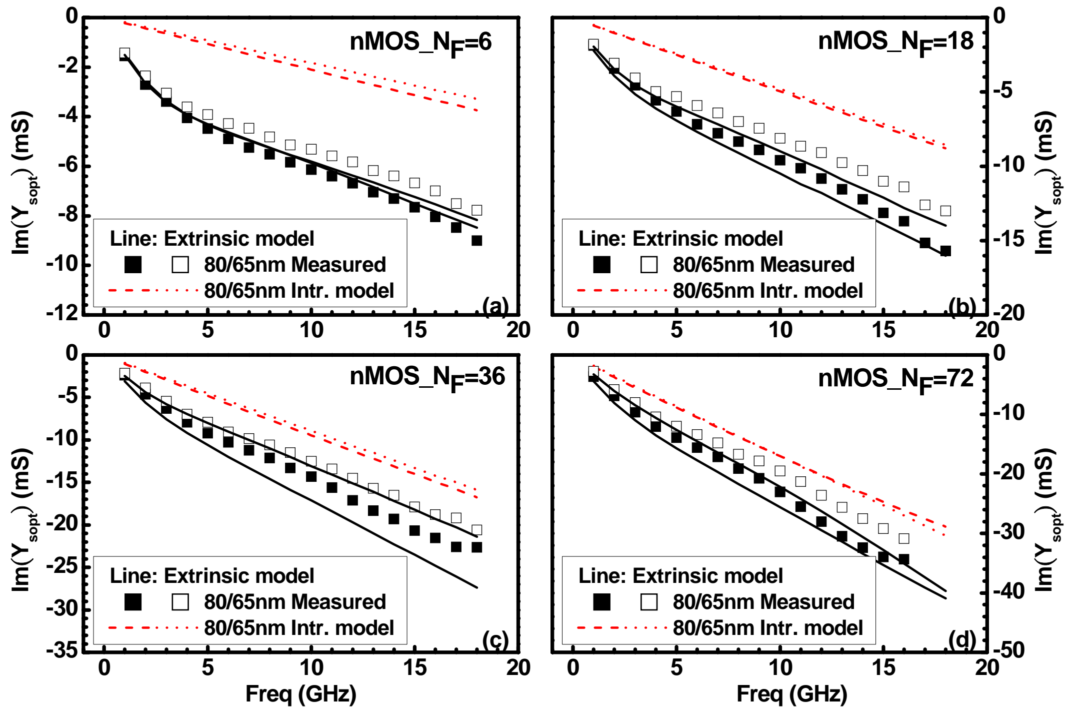


Fig. 6.3 Extrinsic measured and intrinsic simulation $Im(Y_{sopt})$ for 80 and 65nm nMOS (N_F=6, 18, 36, 72)

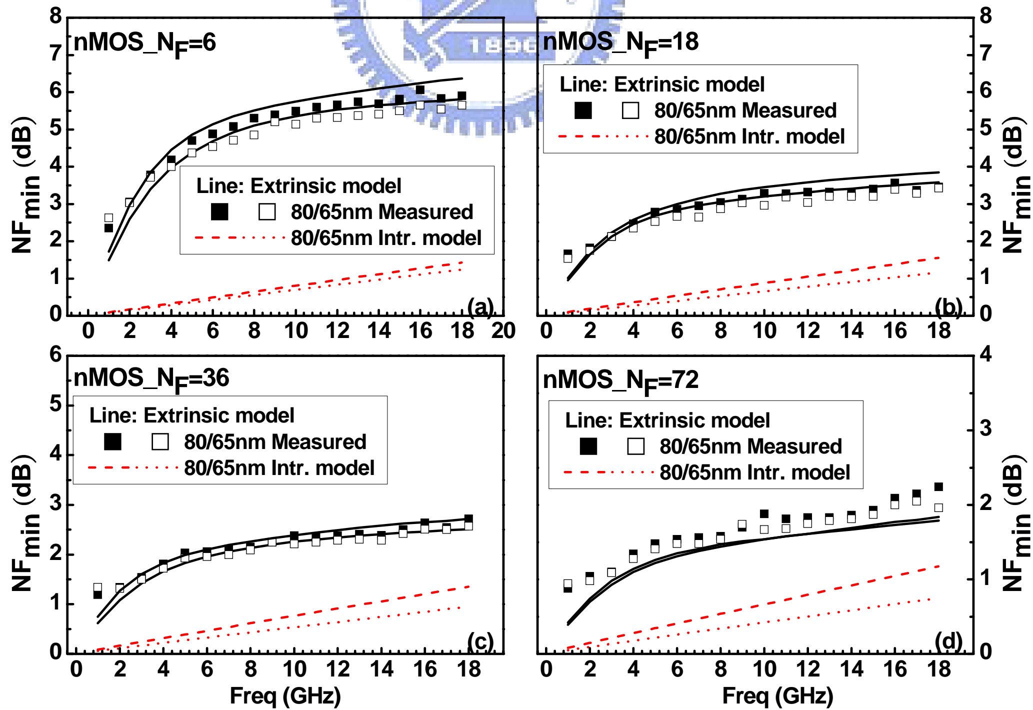


Fig. 6.4 Extrinsic measured and intrinsic simulation NF_{min} for 80 and 65nm nMOS (N_F=6, 18, 36, 72)

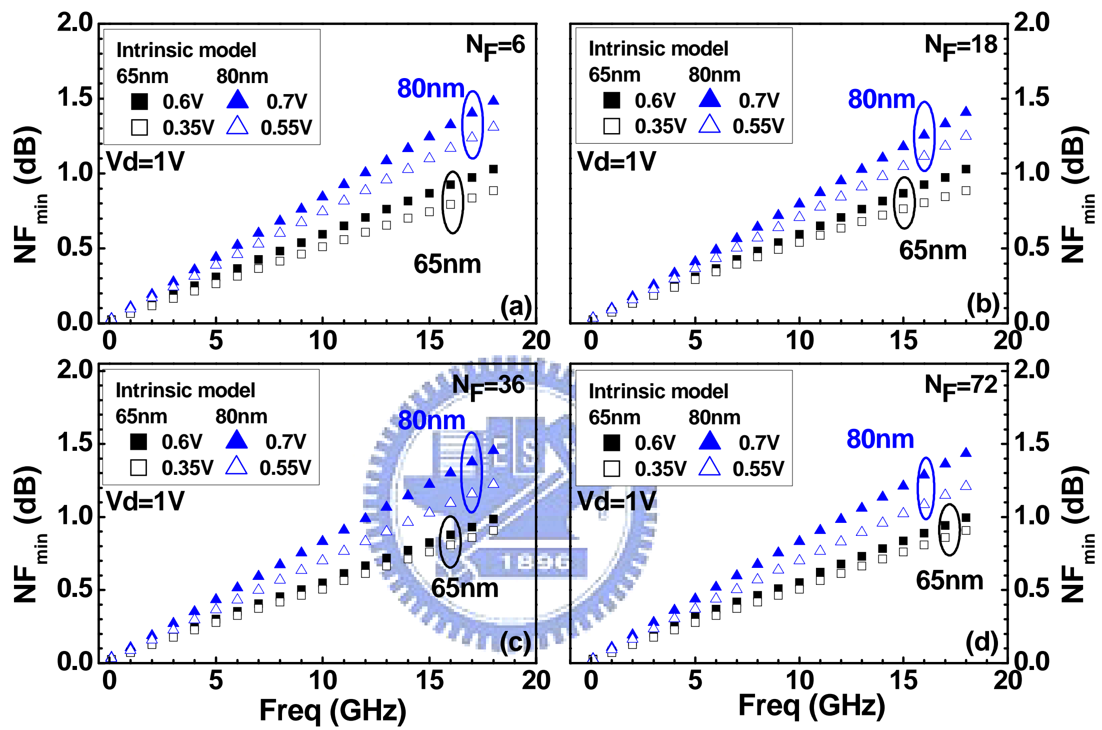


Fig. 6.5 Intrinsic simulation NF_{min} for 80 and 65nm nMOS biased in its maximum g_m and minimum NF_{min} condition. (N_F =6, 18, 36, 72)

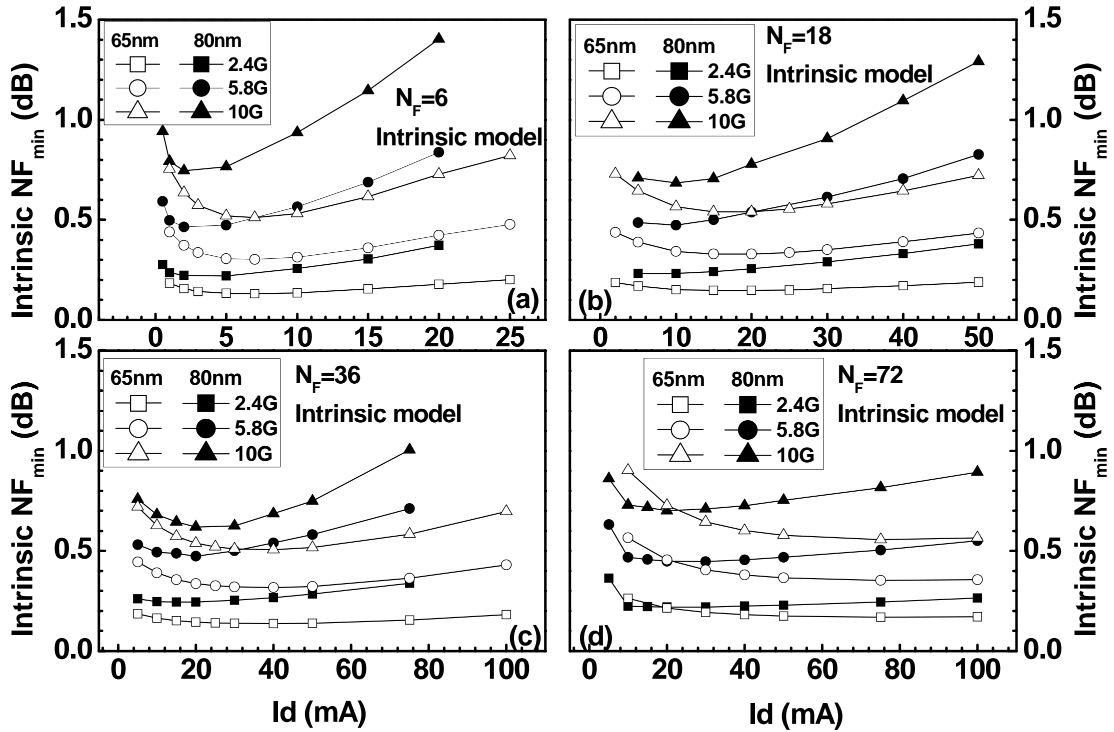


Fig. 6.6 Intrinsic simulation NF_{min} for 80 and 65nm nMOS biased under varying I_d at 2.4GHz, 5.8GHz and 10GHz. (N_F=6, 18, 36, 72)

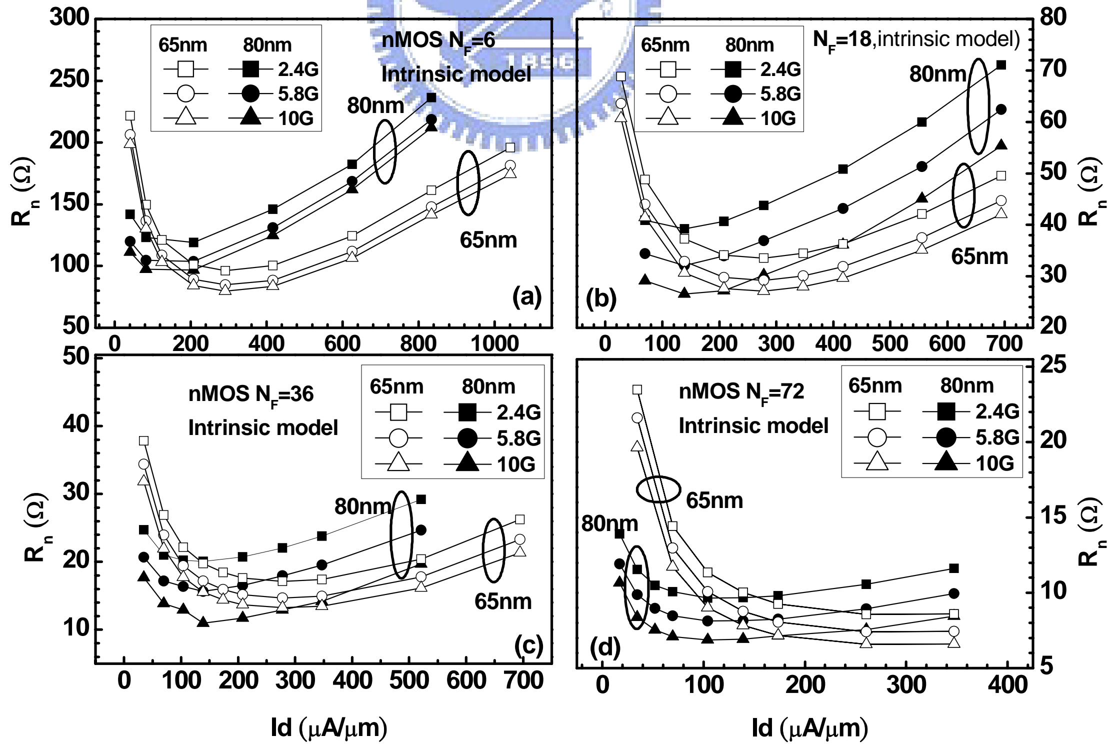


Fig. 6.7 Intrinsic simulation R_n for 80 and 65nm nMOS biased under varying I_d at 2.4GHz, 5.8GHz and 10GHz. (N_F =6, 18, 36, 72)

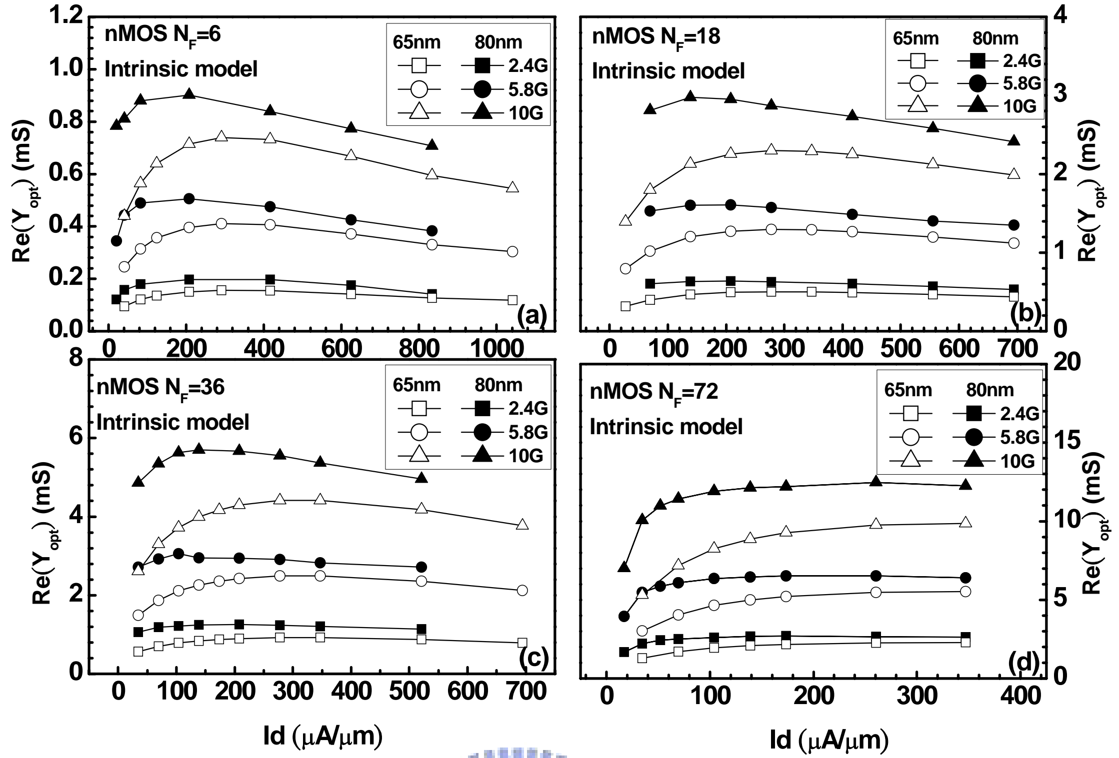


Fig. 6.8 Intrinsic simulation Re(Y_{sopt})for 80 and 65nm nMOS biased under varying Id at 2.4GHz, 5.8GHz and 10GHz. (N_F =6, 18, 36, 72)

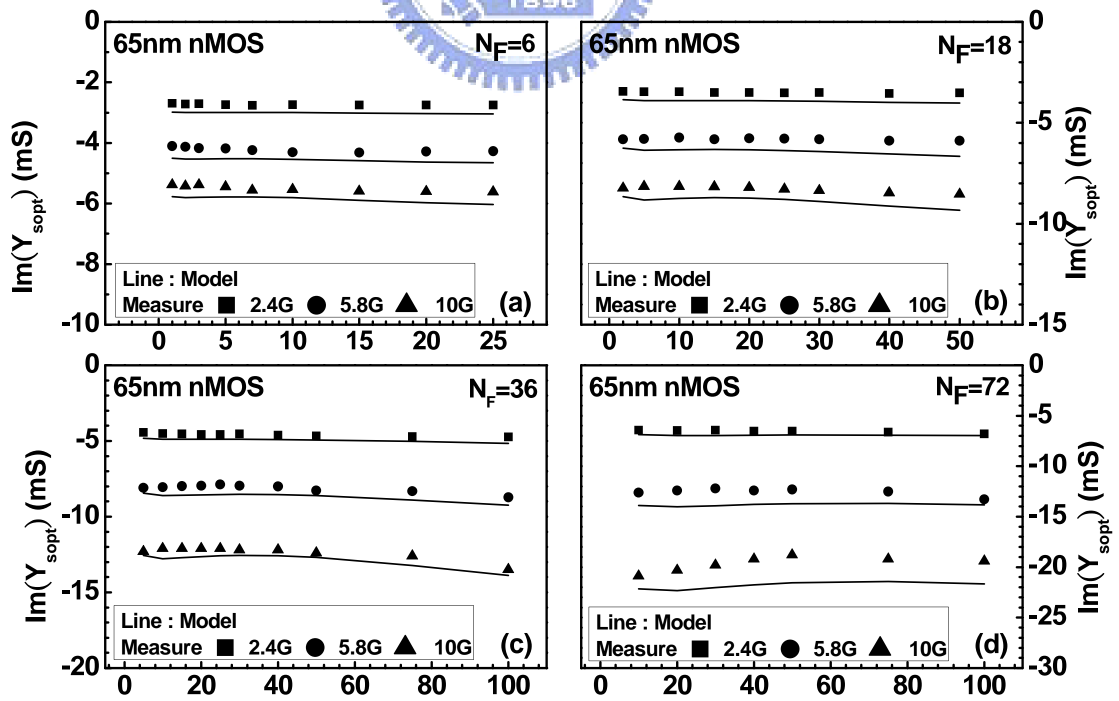


Fig. 6.9 Intrinsic simulation Im(Y_{sopt})for 80 and 65nm nMOS biased under varying Id at 2.4GHz, 5.8GHz and 10GHz. (N_F =6, 18, 36, 72)

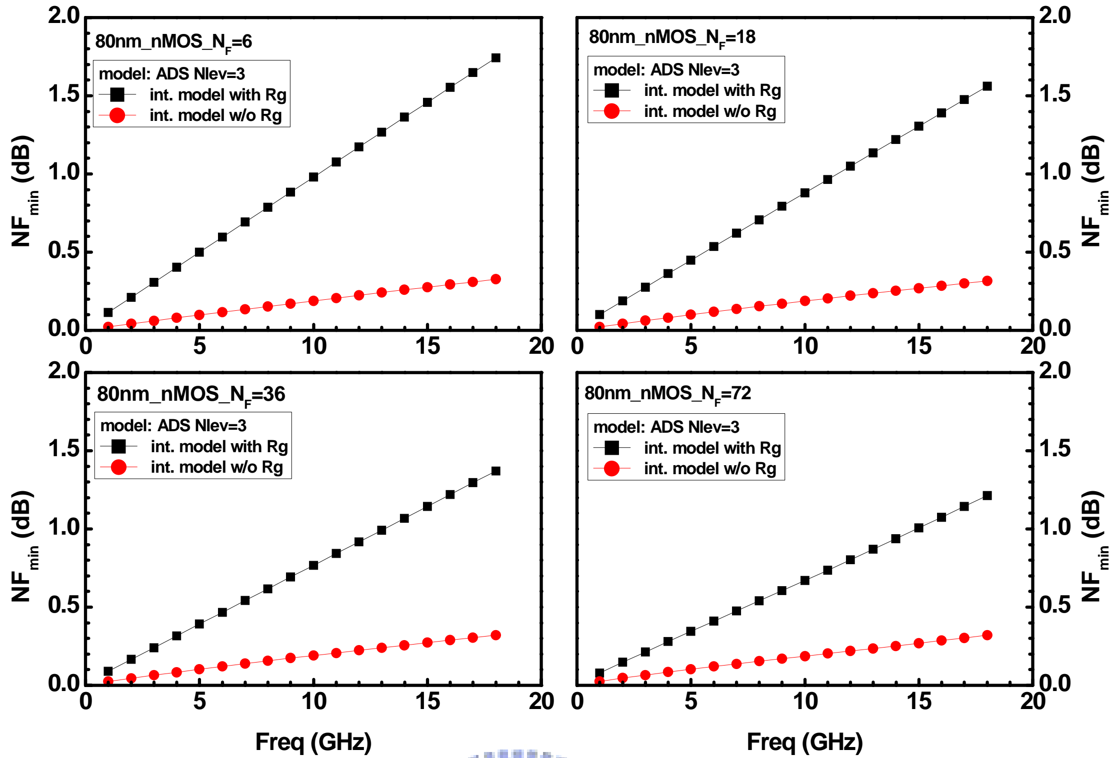


Fig 6.10 R_g effect on NF_{min}. NF_{min} simulated by intrinsic model with and without R_g.

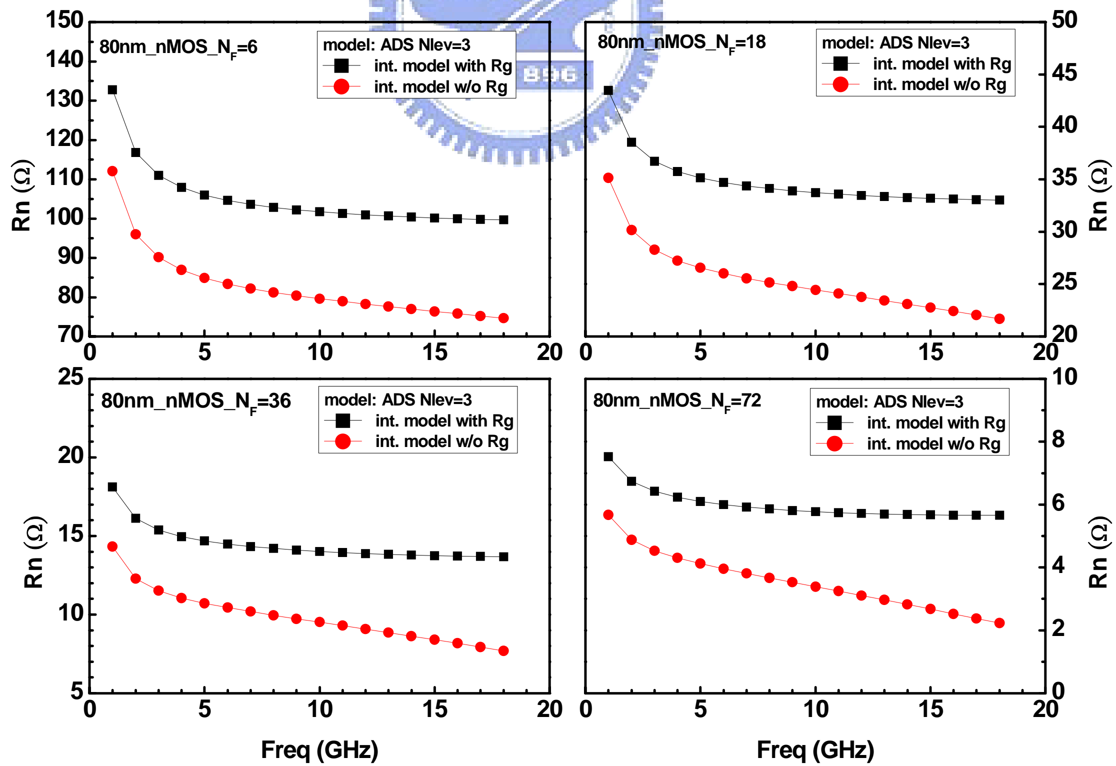


Fig 6.11 R_g effect on R_n. R_n simulated by intrinsic model with and without R_g.

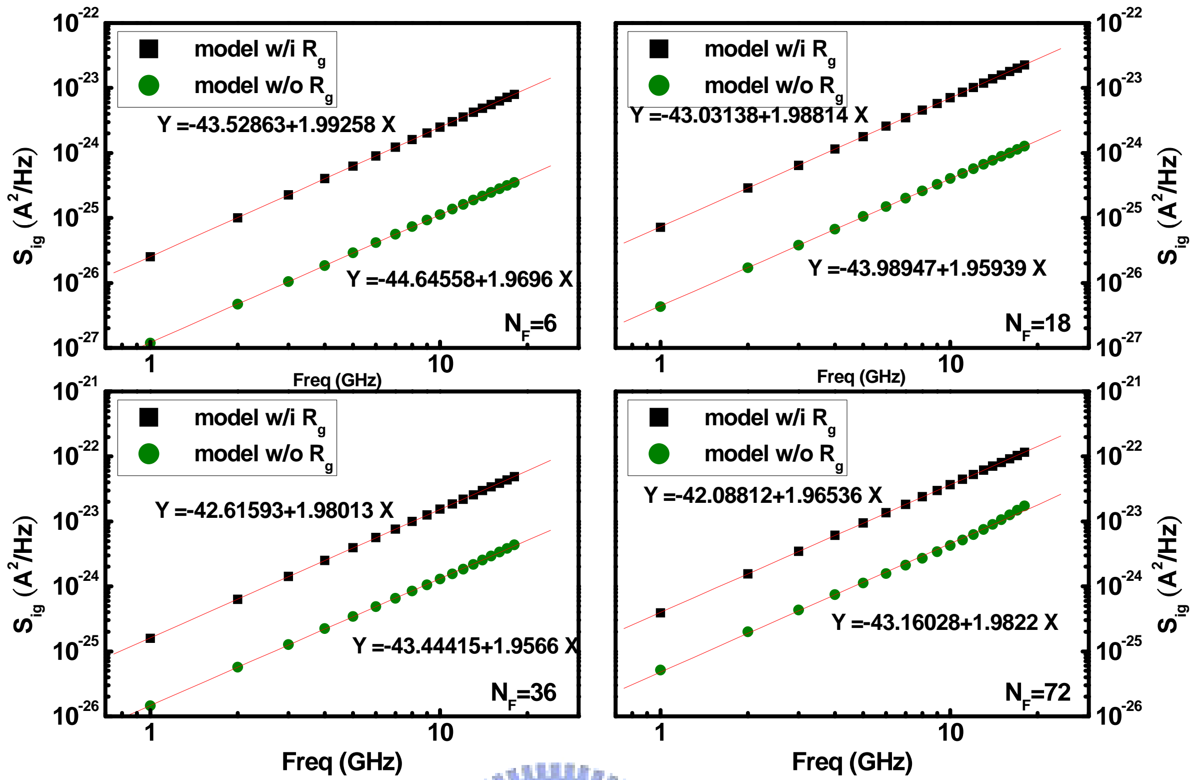


Fig 6.12 R_g effect on S_{ig}. S_{ig} simulated by intrinsic model with and without R_g.

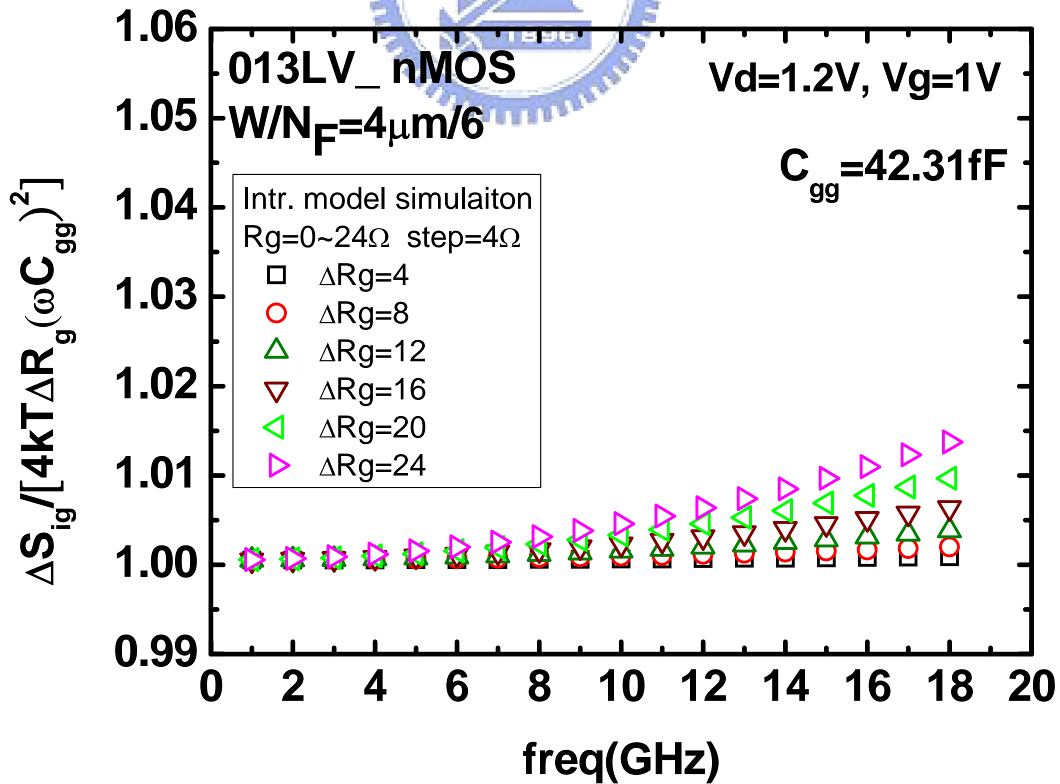


Fig 6.13 Ratio of S_{ig} simulated by intrinsic model w.r.t. S_{ig} calculated by $4k_BT\Delta R_g(\omega C_{gg})^2$

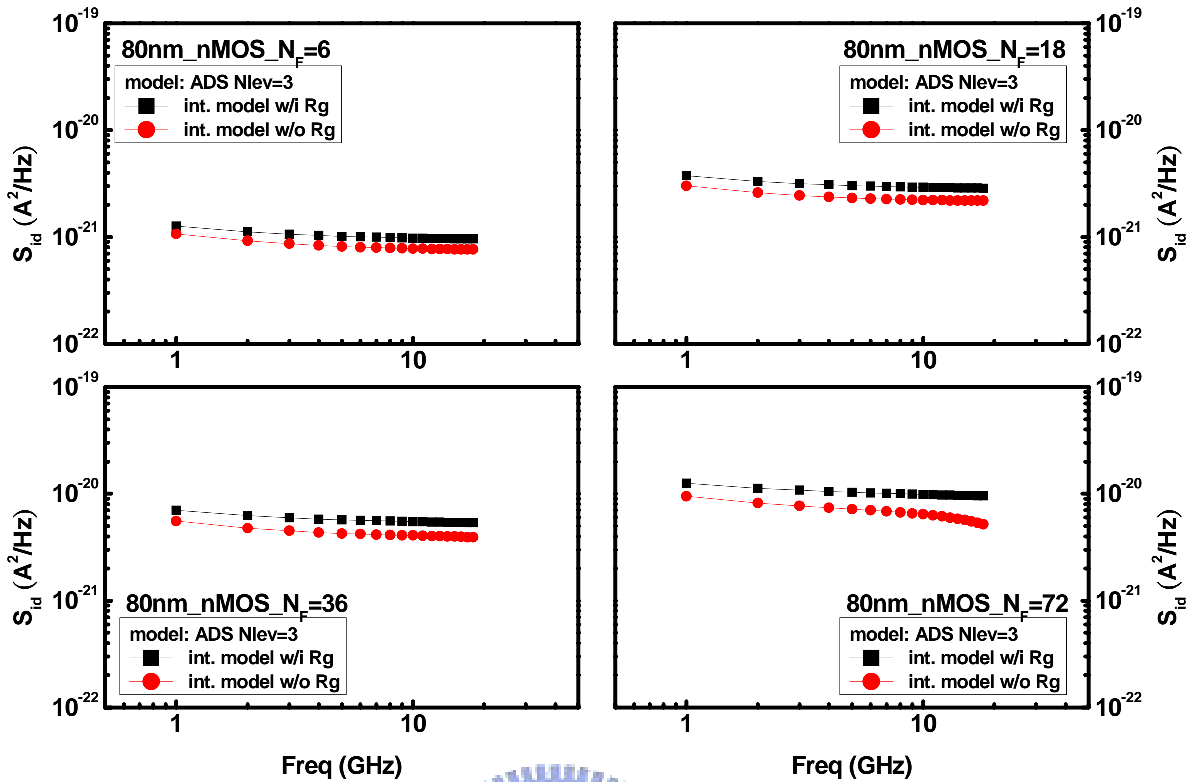


Fig 6.14 R_g effect on S_{id}. S_{id} simulated by intrinsic model with and without R_g.

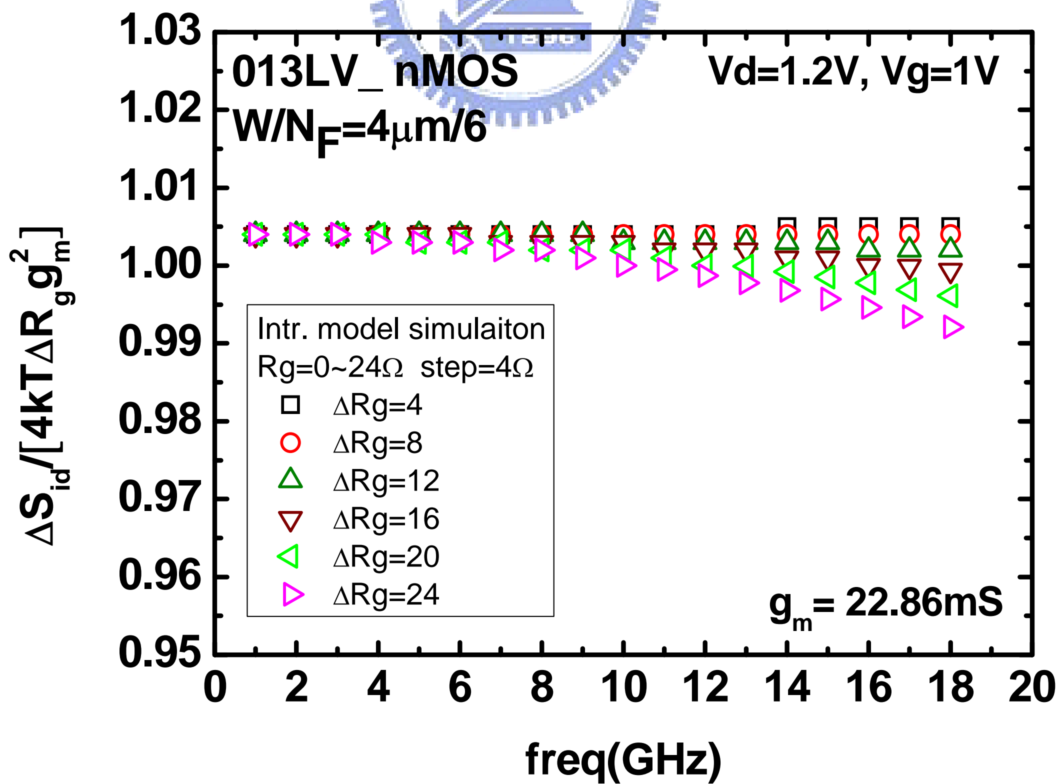
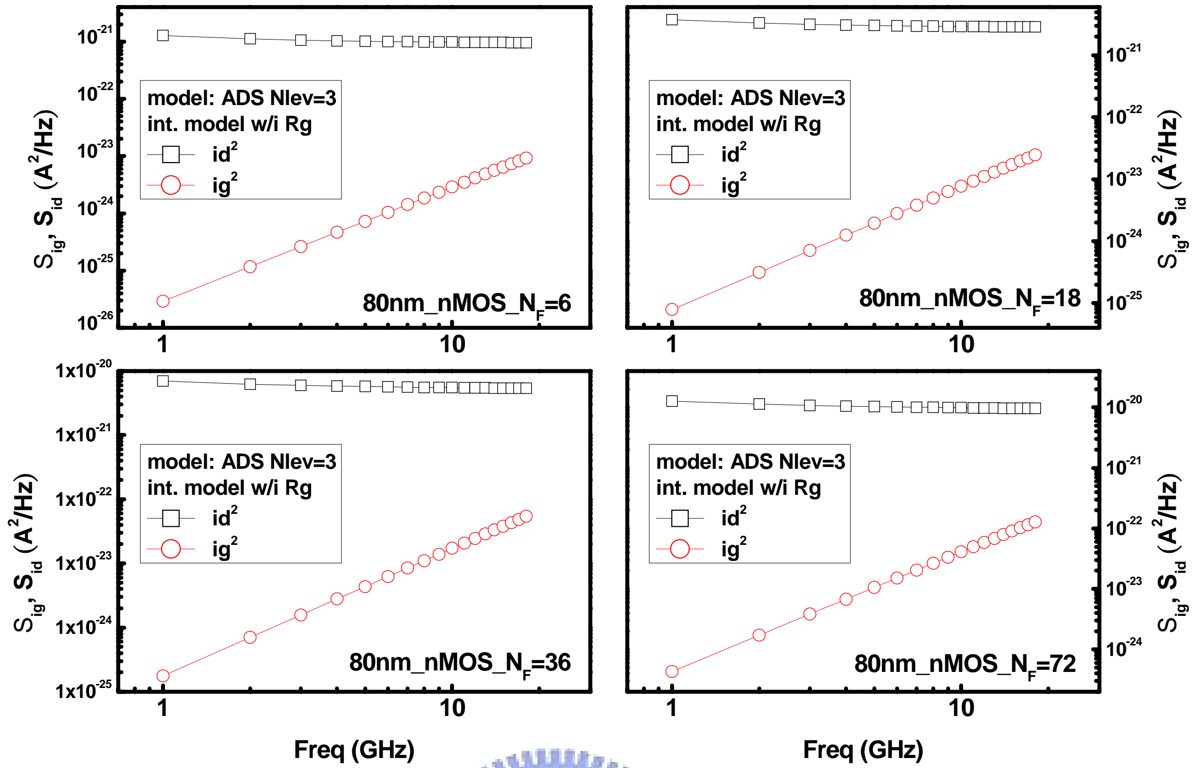


Fig 6.15 Ratio of S_{id} simulated by intrinsic model w.r.t. S_{id} calculated by $4k_BT\Delta R_g g_m^2$



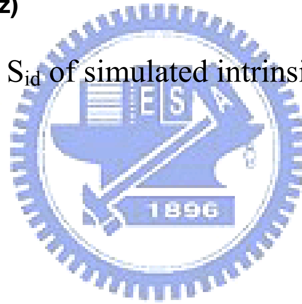


Fig 6.16 Comparison of S_{ig} and S_{id} of simulated intrinsic model.

Chapter 7
Conclusions

In this thesis, the major work have been covered from device test structure design, device characterization and parameter extraction to model construction and finally simulation verification. The primary achievement and contribution realized through this M.S. program is the development of a lossy substrate model for accurate noise simulation and a lossy substrate de-embedding method for intrinsic noise extraction for miniaturized RF MOSFETs.

7.1 Summary

Specified process parameters based on in-line monitor and calibrated I-V model parameters constitutes DC model of the sub-100nm MOSFETs under study. Gate capacitance model calibration was done through extensive verification of the gate capacitances under various gate biases. Gate capacitance was extracted from de-embedded Y-parameters. Proper de-embedding should be conducted for accurate capacitance extraction. A complete de-embedding of major parasitic capacitances depends on delicate open pad layout. Sufficient device geometry splits with various finger numbers (N_F), finger widths (W_F) as well as gate lengths (L_g) are needed to verify and facilitate a scalable model. By incorporating the DC model with key components for RF MOSEFT such as R_g, R_{ds}, C_{ds}, and substrate network, intrinsic RF MOSFET model can be verified through S-parameters, Y-parameters, f_T-I_d etc. Preliminary parameter extraction and further post-extraction parameter optimization were implemented in Agilent-ICCAP environment.

In order to de-embed the extrinsic noise parameters, equivalent circuit de-embedding method was developed. Equivalent circuit for the probing pad consists of pad capacitance as well as lossy substrate RLC components. Various pad structures have been designed to widely

verify its practicability. Extrinsic characteristics such as measured S- and Y- parameters can be predicted by a full circuit model up to 40GHz. The impressive achievement is the good agreement between as-measured noise parameters and simulation results. Finally, intrinsic noise characteristic which is our ultimate interest can be obtained by lossy substrate de-embedding through circuit simulation. Comparisons show the large amount excess noise introduced by lossy pad structure due to the lossy substrate coupling. This makes the proposed de-embedding technique essential. Characteristics over wide range of frequencies, various drain current levels and different geometries were also provided. The encouraging performance extracted in this work consistently matches the RF CMOS scaling trend [17]. The information provided will be especially helpful to improve RF circuit simulation accuracy for low noise RF circuit design.

7.2 Future Work and Recommendation

There remain various interesting and challenging topics worthy of further study through continuous effort. To further improve the high frequency model accuracy, precise extraction of gate resistance as well as substrate network model parameters is essential. Two-port device configuration entails intrinsic drawbacks for RF MOSFET modeling in terms of measurement, de-embedding and parameter extraction, etc. It is because that some parasitic and model parameters cannot be precisely decoupled and extracted for MOSFET of four terminal nature but limited to two-port measurement. Four port measurements theoretically can solve this problem, but new challenges and problems may emerge in respect of de-embedding and parameter extraction. On the other hand, as the pad effect on measured noise can be effectively reduced by improved pad structure design, the research on MOSFET noise would go a further step into the topics of intrinsic noise mechanism and compact model development. In addition to short channel effect and hot carrier effect, gate tunneling current may also introduce more modeling issue. Physical mechanism modeling will take more efforts in

respect of physics understanding, model development and implementation as well as extensive verification.

Through this process of noise characterization and modeling, one of major difficult jobs is the data acquisition of integrity and reliability. On-wafer RF measurement involves many delicate and laboring work. Instrument calibration, probe and cable qualification, and probing technique altogether affect the repeatability and reliability of the measurement. Indeed, repeatable data is a mandatory criterion, especially for device modeling. Appropriate de-embedding technique suitable for specific layout is also important to obtain the truly intrinsic device feature. It is believed that the measurement and modeling difficulty will be tougher for nanoscale devices. More complicated parasitic effects and device physical mechanism will be encountered. However, it also implies that there will be more and more interesting research topics awaiting exploration.

Appendix A [10]

Derivation of Noise Parameters

Base on the noise model with noise source $\overline{i_s^2}$ and source admittance Y_s at the input of the network, a lossy network is presented by a voltage and current noise connected at the input of a lossless network. Refer to Fig. A.1.

From equation 2-18, noise figure can be expresses as follows:

$$F \equiv \frac{\text{total output noise power}}{\text{output noise power due to noise source}} = \frac{\text{Total equivalent input noise power}}{\text{noise power of source impedance}} \qquad \text{(A-1)}$$

$$F = \frac{\overline{i_s^2} + \left|\overline{i_n + Y_s V_n}\right|^2}{\overline{i_s^2}} \qquad \text{(A-2)}$$

Splitting the noise current i_n into an uncorrelated i_u and a correlated noise current i_c, the correlated noise current is related to the noise voltage V_n via a correlation factor Y_c $(Y_c = G_c + jB_c)$

$$\begin{aligned}
F &= \frac{\overline{i_s^2} + \left|\overline{(i_c + i_u) + Y_s V_n}\right|^2}{\overline{i_s^2}} \\
&= \frac{\overline{i_s^2} + \left|\overline{(V_n Y_c + i_u) + Y_s V_n}\right|^2}{\overline{i_s^2}} \\
&= \frac{\overline{i_s^2} + \left|\overline{V_n (Y_c + Y_s) + i_u}\right|^2}{\overline{i_s^2}} \qquad \text{(A-3)} \\
&= 1 + \frac{\overline{i_u^2} + \left|Y_c + Y_s\right|^2 V_n^2}{\overline{i_s^2}} \\
&= 1 + \frac{\overline{i_u^2} + \left|(G_c + G_s)^2 + (B_c + B_s)^2\right| V_n^2}{\overline{i_s^2}}
\end{aligned}$$

Noise sources can be presented by equivalent thermal noise model

$$\overline{i_s^2} = 4kT\Delta f \cdot G_s \quad \text{; noise due to source admittance} \qquad \text{(A-4)}$$

$$\overline{i_u^2} = 4kT\Delta f \cdot G_u \quad \text{; noise due to equivalent noise conductance} \qquad \text{(A-5)}$$

$$\overline{V_n^2} = 4kT\Delta f \cdot R_n \quad \text{; noise due to equivalent noise resistance} \qquad \text{(A-6)}$$

Substituting (A-4) ~ (A-6) into (A-3) leads to

$$\begin{aligned} F &= 1 + \frac{4kT\Delta f \cdot G_u + \left|(G_c + G_s) + (B_c + B_s)\right|^2 (4kT\Delta f \cdot R_n)}{4kT\Delta f \cdot G_s} \\ &= 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s}[(G_c + G_s)^2 + (B_c + B_s)^2] \end{aligned} \qquad \text{(A-7)}$$

Minimum noise figure can be achieved by giving an appropriate admittance Y_s. To find this specific admittance, derivative of (A-7) with respect to G_s and B_s is conducted

$$\begin{aligned} \frac{\partial F}{\partial G_s} &= \frac{-G_u}{G_s^2} + \frac{2R_n(G_c + G_s)G_s - R_n[(G_c + G_s)^2 + (B_c + B_s)^2]}{G_s^2} \\ &= \frac{-G_u - R_n(G_c^2 - G_s^2) - R_n(B_c + B_s)^2}{G_s^2} \end{aligned} \qquad \text{(A-8)}$$

$$\frac{\partial F}{\partial B_s} = \frac{2R_n}{G_s}(B_c + B_s) \qquad \text{(A-9)}$$

Optimum source admittance Y_{sopt} is obtained by setting both $\frac{\partial F}{\partial G_s}$, $\frac{\partial F}{\partial B_s}$ equal to zero,

$$G_{sopt} = \sqrt{G_c^2 + \frac{G_u}{R_n}} \qquad \text{(A-10)}$$

$$B_{sopt} = -B_c \qquad \text{(A-11)}$$

Substituting (A-10) and (A-11) into (A-7) leads to

$$\begin{aligned}
F &= 1 + \frac{R_n(G_{sopt}^2 - G_c^2)}{G_s} + \frac{R_n}{G_s}\left[(G_c + G_s)^2 + (B_s - B_{sopt})^2\right] \\
&= 1 + 2R_nG_c + \frac{R_n(G_{sopt}^2 - G_c^2) + R_n(G_c^2 + G_s^2) + R_n(B_s - B_{sopt})^2}{G_s} \\
&= 1 + 2R_nG_c + \frac{R_n(G_{sopt}^2 + G_s^2) + R_n(B_s - B_{sopt})^2}{G_s} \\
&= 1 + 2R_n(G_{sopt} + G_c) + \frac{R_n(G_s - G_{sopt})^2 + R_n(B_s - B_{sopt})^2}{G_s} \\
&= F_{\min} + \frac{R_n}{G_s}(Y_s - Y_{sopt})^2
\end{aligned} \tag{A-12}$$

where the minimum noise figure is defined as

$$F_{\min} = 1 + 2R_n(G_{sopt} + G_c) \tag{A-13}$$

F_{min} is an intrinsic property related to R_n, G_c, G_u and independent of the input noise source and source admittance.

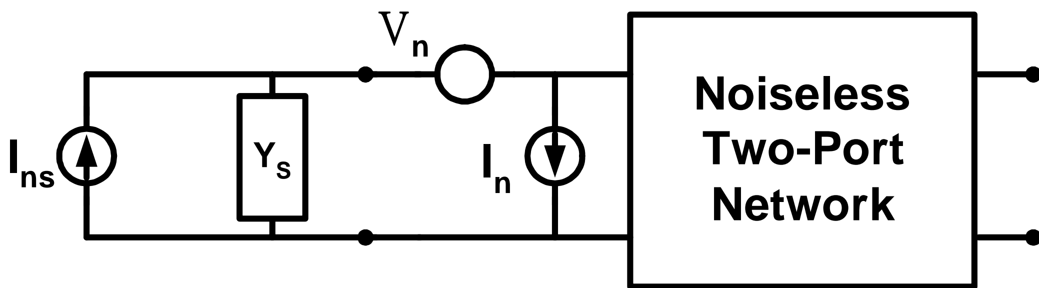


Fig. A.1 Presentation of a noisy two-port network connected to a noise source and source admittance.

Appendix B [28]

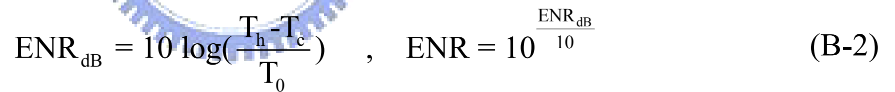
The Y-Factor Method and Noise Figure Correction

In noise figure measurement, total output noise power measured is

$$N_o = N_a + GN_i = N_a + kTBG \tag{B-1}$$

where N_o and N_i represent the noise levels available at the output and input respectively, G is the gain of the DUT, B is the bandwidth, k is Boltzmann's constant, and T is the absolute temperature.

To determine N_a, output noise power corresponding to two source temperatures are needed. Two output noise power and two source temperatures determine the slope kBG and intercept N_a. A diode based noise source in the on-state (hot) generates noise when it is reverse biased into avalanche breakdown. Thus the equivalent noise temperature will be higher than its "off-state" (cold). Temperature difference is expressed by excess noise ratio (ENR)



$$ENR_{dB} = 10\log\left(\frac{T_h - T_c}{T_0}\right) \quad , \quad ENR = 10^{\frac{ENR_{dB}}{10}} \tag{B-2}$$

Y-factor is defined as the output noise ratio

$$Y = \frac{N_1}{N_2} \tag{B-3}$$

Derivation is shown as follows:

$$N_1 = N_a + kT_cBG \quad , \quad N_2 = N_a + kT_hBG$$

$$ENR = 10^{\frac{ENR_{dB}}{10}} = \frac{T_h - T_c}{T_0} \tag{B-4}$$

$$Y = \frac{N_2}{N_1} = \frac{N_a + kT_hBG}{N_a + kT_cBG}$$

In practice, T_c is assumed to be 290K when it is calibrated. This leads to

$$
\begin{aligned}
(Y\text{-}1)N_a &= kBG(T_h\text{-}YT_0) \\
&= kBG(T_0 \cdot ENR+T_0\text{-}Y \cdot T_0) \\
&= kT_0BG(ENR+1\text{-}Y)
\end{aligned}
\tag{B-5}
$$

$$\Rightarrow$$

$$N_a = kT_0BG(\frac{ENR}{Y\text{-}1}\text{-}1)$$

From the derived N_a, the total noise factor measured can be calculated.

$$F_{tot} \equiv \frac{N_a+GN_i}{GN_i} = \frac{kT_0BG(\frac{ENR}{Y\text{-}1}\text{-}1)+GkT_0B}{GkT_0B} = \frac{ENR}{Y\text{-}1} \tag{B-6}$$

Because only the noise factor of the DUT is interested, removal of the noise contributed from the second stage is essential. Based on the noise factor analysis of multi-stage system, total noise factor of a two-stage system is

$$F_{tot} = F_1+\frac{F_2\text{-}1}{G_1} \tag{B-7}$$

where F_1, F_2 and G_1 are noise factor of 1st stage, 2nd stage and gain of 1st stage respectively.

Noise factor of the instrument (F_2) can be characterized while doing system calibration and gain of the DUT (G) will be obtained while measuring S-parameters before noise measurement. Therefore corrected noise factor is obtained

$$F_1 = F_{tot} - \frac{F_2\text{-}1}{G_1} \tag{B-8}$$

then is used to construct the noise equation.

Appendix C [7]

Correlation Matrices Noise De-embedding Method

1.) Measure the scattering parameters of DUT and open pad, $[S]_{mea}$ and $[S]_{open}$, also the noise parameter of the DUT (F_{min}, R_n, Y_{opt}). Then convert those S parameters to Y parameters, $[S]_{mea} \rightarrow [Y]_{mea}$; $[S]_{open} \rightarrow [Y]_{open}$.

2.) Calculate the correlation matrix $[C_A]_{mea}$ from measured noise parameters by the following relation.

$$\begin{aligned}
C_{A,11,mea} &= 2 \cdot K_B T \cdot R_n \\
C_{A,21,mea} &= 2 \cdot K_B T \cdot \left(\frac{F_{\min} - 1}{2} - R_n Y_{opt} \right) \\
C_{A,12,mea} &= 2 \cdot K_B T \cdot \left(\frac{F_{\min} - 1}{2} - R_n Y^*_{opt} \right) \\
C_{A,22,mea} &= 2 \cdot K_B T \cdot \left((F_{\min} - 1) G_{sopt} - \frac{(F_{\min} - 1)^2}{4 R_n} + \left| \frac{C_{A,21mea}}{2 * K_B T} \right|^2 \cdot \frac{1}{R_n} \right)
\end{aligned} \tag{C-1}$$

$$[C_A]_{mea} = 2K_B T \begin{pmatrix} R_n & \frac{F_{\min} - 1}{2} - R_n * Y_{opt} \\ \frac{F_{\min} - 1}{2} - R_n * Y^*_{opt} & (F_{\min} - 1) * G_{sopt} - \frac{(F_{\min} - 1)^2}{4 * R_n} + \left| \frac{C_{A,21mea}}{2 * K_B T} \right|^2 * \frac{1}{R_n} \end{pmatrix} \tag{C-2}$$

3.) Convert matrix $[C_A]_{mea}$ to $[C_Y]_{mea}$ by using $[C_A]_{mea}$ and measured Y parameters $[Y]_{mea}$.

$$\begin{aligned}
[C_Y]_{mea} &= [T]_{mea} [C_A]_{mea} [T]^{\dagger}_{mea} \\
&= \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}_{mea} [C_A]_{mea} \begin{bmatrix} -Y^*_{11} & -Y^*_{21} \\ 1 & 0 \end{bmatrix}_{mea}
\end{aligned} \tag{C-3}$$

4.) Calculate the open pad correlation matrix $[C_Y]_{open}$

$$[C_Y]_{open} = 2 k_B T * \mathrm{Re}[Y]_{open} \tag{C-4}$$

5.) De-embed the parallel parasitics of measured Y parameters $[Y]_{mea}$ and correlation matrix $[C_Y]_{mea}$.

$$[Y]_{DUT} = [Y]_{mea} - [Y]_{open} \tag{C-5}$$

$$[C_Y]_{DUT} = [C_Y]_{mea} - [C_Y]_{open} \tag{C-6}$$

6.) Convert the intrinsic Y parameters $[Y]_{DUT}$ to its chain matrix.

$$[A]_{DUT} = \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}_{DUT}^{-1} \begin{bmatrix} Y_{12} & 0 \\ Y_{22} & 1 \end{bmatrix}_{DUT} = \frac{-1}{Y_{21}} \begin{bmatrix} Y_{22} & 1 \\ (Y_{11}Y_{22} - Y_{12}Y_{21}) & Y_{11} \end{bmatrix}_{DUT} \tag{C-7}$$

7.) Transform the intrinsic correlation matrix $[C_Y]_{DUT}$ to its chain matrix $[C_A]_{DUT}$.

$$\begin{aligned}[C_A]_{DUT} &= [T_A]_{DUT}[C_Y]_{DUT}[T_A]_{DUT}^{\dagger} \\ &= \begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix}_{DUT} [C_Y]_{DUT} \begin{bmatrix} 0 & 1 \\ A_{12}^{*} & A_{22}^{*} \end{bmatrix}_{DUT}\end{aligned} \tag{C-8}$$

8.) De-embedded intrinsic noise parameters $F_{min,\,DUT}$, $R_{n,\,DUT}$, $Y_{opt,\,DUT}$ can be calculated from the chain matrix $[C_A]_{DUT}$.

$$F_{\min,DUT} = 1 + \frac{\mathrm{Re}[C_{A,12,DUT}]}{k_B T} + \frac{\sqrt{C_{A,11,DUT} C_{A,22,DUT} - (\mathrm{Im}[C_{A,12,DUT}])^2}}{k_B T} \tag{C-9}$$

$$R_{n,DUT} = \mathrm{Re}[\frac{C_{A,11,DUT}}{2k_B T}] \tag{C-10}$$

$$Y_{sopt,DUT} = G_{sopt,DUT} + \mathrm{I} * B_{sopt,DUT} = \frac{\sqrt{C_{A,11,DUT} C_{A,22,DUT} - (\mathrm{Im}[C_{A,12,DUT}])^2} + \mathrm{I} * \mathrm{Im}[C_{A,12,DUT}]}{C_{A,11,DUT}} \tag{C-11}$$

$$G_{sopt,DUT} = \mathrm{Re}[\frac{1}{R_{n.DUT}} * (\frac{F_{\min,DUT} - 1}{2} - \frac{\mathrm{Re}[C_{A,12,DUT}]}{2 * k_B T})] \tag{C-12}$$

$$B_{sopt,DUT} = -\frac{1}{2 * k_B T} * \frac{1}{R_{n.DUT}} * \mathrm{Im}[C_{A,21,DUT}] \tag{C-13}$$

Note:

(a) $\text{NFmin(dB)}=10\times\log_{10}(\text{Fmin})$ (C-14)

(b) Noise parameters measured from noise measurement are NF_{min}, R_n, and $\ _{opt}$. Before conducting the noise matrix de-embedding, opt should be transform to Y_{opt}. (In Advance Design System (ADS) simulator, S_{opt} stands for $\ _{opt}$.)

$$Y_{opt}=G_{opt}+I^{*}B_{opt}=\frac{1}{Z_o}\cdot\frac{1-\Gamma_{opt}}{1+\Gamma_{opt}} \tag{C-15}$$

(c) $K_B=8.62\times10^{-5}$ (eV/K), $T=T_C+273$ (K)

(d) Correlation matrices of an passive two-port in impedance and admittance representation are

$$C_Z=2K_BT\cdot\text{Re}[Z] \tag{C-16}$$

$$C_Y=2K_BT\cdot\text{Re}[Y] \tag{C-17}$$

Chain representation of the whole test fixture is estimated from the measured noise parameter (NF_{min}, R_n, Y_{opt}).

$$[C_A]_{mea}=2K_BT\begin{pmatrix} R_n & \frac{F_{min}-1}{2}-R_n*Y_{opt} \\ \frac{F_{min}-1}{2}-R_n*Y^{*}_{opt} & R_n\,|Y_{opt}|^2 \end{pmatrix} \tag{C-18}$$

(e) Interconnections of the two-port networks can be described by the operation of the two matrix:

$$\begin{aligned} &C_Z=C_{Z1}+C_{Z2} && \text{(series)} \\ &C_Y=C_{Y1}+C_{Y2} && \text{(parallel)} \\ &C_A=A_1C_{A2}A_2^{\dagger}+C_{A1} && \text{(cascade)} \end{aligned} \tag{C-19}$$

(f) Transformation of matrices presentation is done by taking the Fourier transform of convolution integral of the noise signal. The transformation formula can be expressed as

$$C'=TCT^{\dagger} \tag{C-20}$$

where C and C' are the original and resulting representation, T is the transformation matrix.

(g) Once the chain matrix of the intrinsic device is obtain, noise parameters after de-embedding can be calculated follow the expression above:

$$[C_A]_{\mathrm{DUT}} = 2K_BT\begin{pmatrix} R_{n,DUT} & \frac{F_{\min,DUT}-1}{2} - R_{n,DUT} * Y_{opt,DUT} \\ \frac{F_{\min,DUT}-1}{2} - R_{n,DUT} * Y^{*}{}_{opt,DUT} & R_{n,DUT}\,|\,Y_{opt,DUT}\,|^2 \end{pmatrix}$$

(C-21)

$$[C_A]_{\mathrm{DUT}} = 2K_BT\begin{pmatrix} R_{n,DUT} & \frac{F_{\min,DUT}-1}{2} - R_{n,DUT} Y_{opt,DUT}{}^{*} \\ \frac{F_{\min,DUT}-1}{2} - R_{n,DUT} Y_{opt,DUT} & R_{n,DUT}\,|\,Y_{opt,DUT}\,|^2 \end{pmatrix}$$

Appendix D

Modified Open-Short De-embedding

Open and short pads were conventionally used to de-embed parallel parasitic admittance and series parasitic impedance respectively. The de-embedding procedure is shown as follows:

$$Y_{m_de_o} = Y_m - Y_o \tag{D-1}$$

$$Y_{s_de_o} = Y_s - Y_o \tag{D-2}$$

$$Z_{int} = (Y_{m_de_o})^{-1} - (Y_{s_de_o})^{-1} = (Y_m - Y_o)^{-1} - (Y_s - Y_o)^{-1} \tag{D-3}$$

$$Y_{int} = (Z_{int})^{-1} \tag{D-4}$$

where

Y_m = measured Y parameter of DUT

Y_o = measured Y parameter of open pad

Y_s = measured Y parameter of short pad

Y_{int} = intrinsic Y parameter after open/short de-embedding

Equivalent circuits of test structure with DUT, open pad and short pad are given in Fig. D.1~Fig. D.3. According to these equivalent circuits, following expression holds

$$Y_o = \begin{pmatrix} Y_{p1} + Y_{p3} & -Y_{p3} \\ -Y_{p3} & Y_{p2} + Y_{p3} \end{pmatrix} \tag{D-5}$$

$$Z_{s_de_o} = (Y_{s_de_o})^{-1} = Y_s - Y_o = \begin{pmatrix} Z_{s1}+Z_{s3} & Z_{s3} \\ Z_{s3} & Z_{s2}+Z_{s3} \end{pmatrix} \quad \text{(D-6)}$$

In this de-embedding process, based on Fig. D.3, short pad does not see a parasitic admittance Y_{p3} because all the interconnection metals are shorted at the same potential. De-embedding procedure (D-2) may introduce an over-de-embedding error because Y_{p3} was deducted from Y_s in which Y_{p3} does not exist. Therefore step (D-2) was modified as given below and keeps the rest of the steps the same.

$$Y_{s_de_o} = Y_s - \begin{pmatrix} Y_{11}+Y_{12} & 0 \\ 0 & Y_{22}+Y_{21} \end{pmatrix} \quad \text{(D-7)}$$

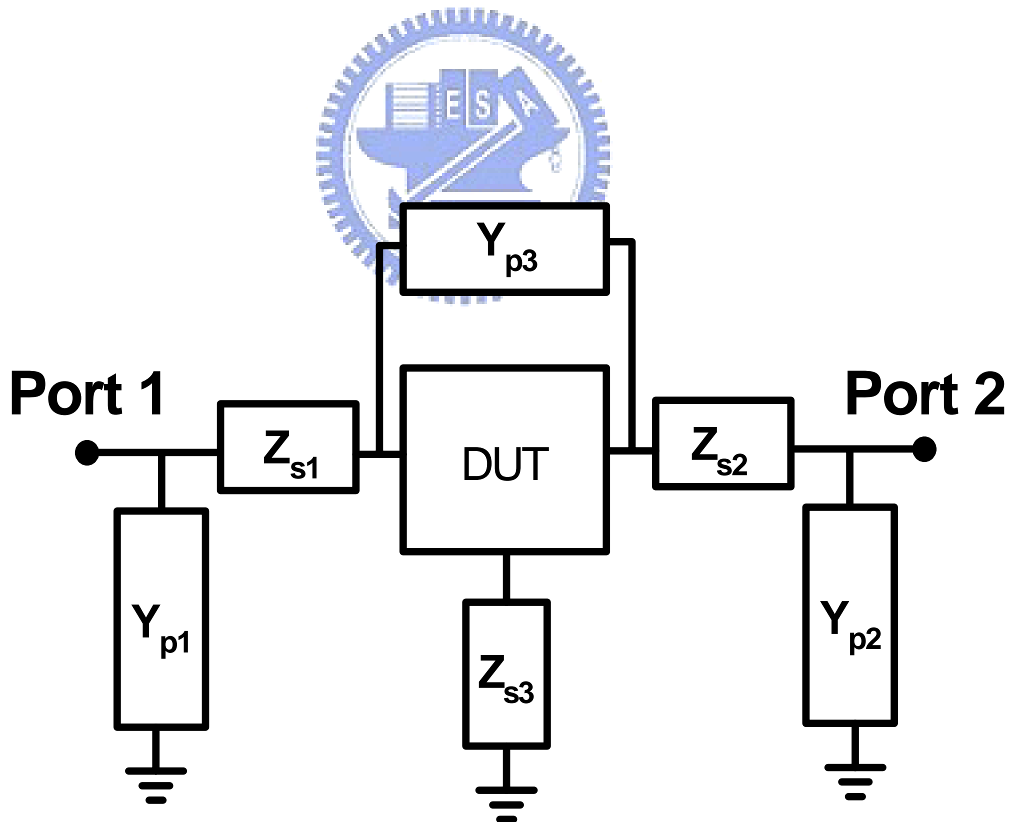


Fig. D.1 Equivalent circuit of test structure with DUT

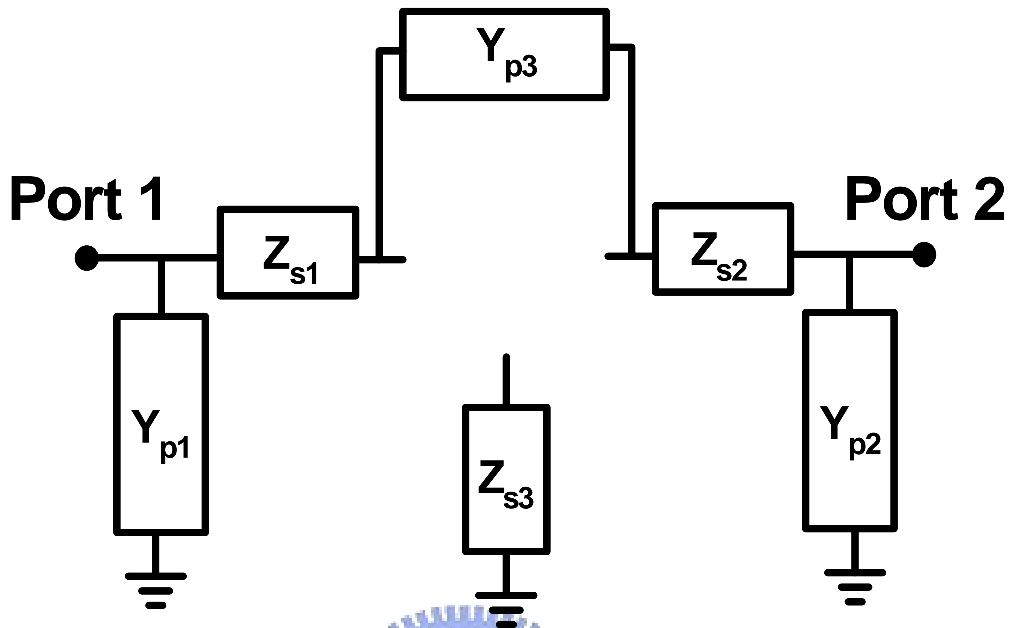


Fig. D.2 Equivalent circuit of open pad

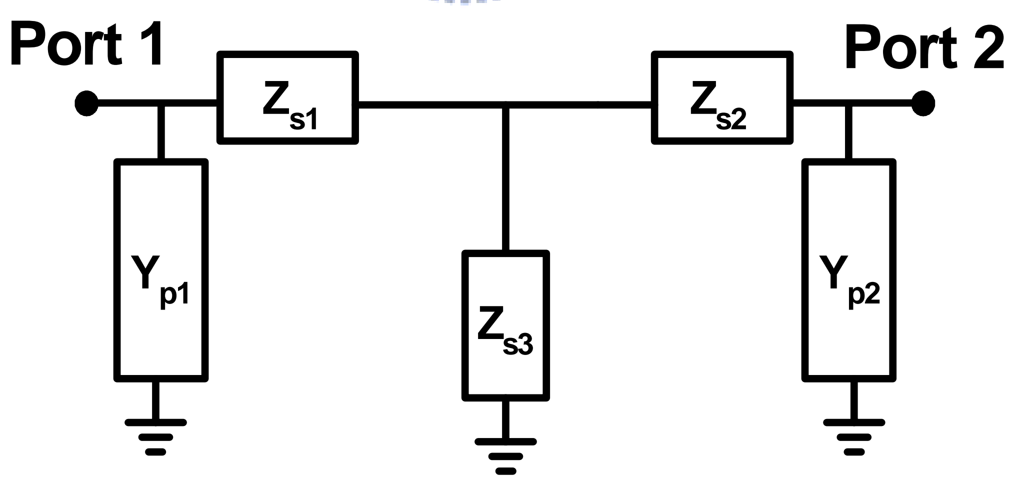


Fig. D.3 Equivalent circuit of short pad

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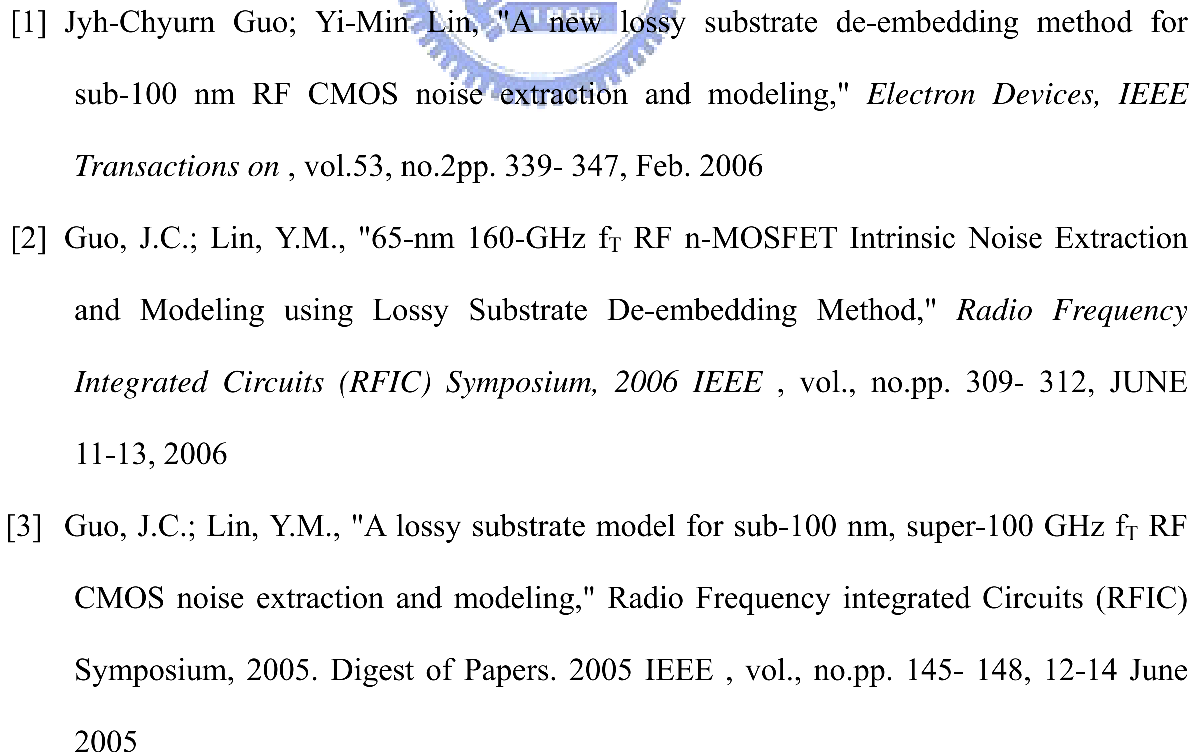

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