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碩 士 論 文

高介電常數材料（$HfAlO_xN_y$）在MOS元件上特性之研究

Characteristic and Investigation of High-k (HfAlOxNy) Dielectric on MOS Devices

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摘 要

根據半導體的微縮定律，隨著半導體製造逐漸的微小化，極薄的二氧化矽介電層將伴隨著極大的直接穿遂漏電流，而這個直接穿遂漏電流將對元件的功率消耗有嚴重的影響。在閘極二氧化矽介電層薄到10 奈米以下的情況之下，為了解決這嚴重的直接穿遂漏電流現象，我們將利用高介電係數材料來替換傳統的二氧化矽。我們利用高介電係數材料在相同的等效二氧化矽厚度之下，能擁有較大的實際物理厚度以抵擋直接穿遂漏電流。

在眾多高介電係數材料之中，二氧化鉿和三氧化二鋁是非常有潛

力的高介電係數材料。二氧化鉿有較高的介電係數，但它的結晶溫度太低<500oC。為了克服二氧化鉿結晶溫度太低的問題，我們加入三氧化二铝去改善這問題及提升載子能障·當高介電數材料直接沈積在矽晶圓表面上時，在介面的地方會有一層二氧化矽的介面層產生·這一層介面層的品質扮演著非常重要的角色對於在元件的特性和可靠度·所以我們想要成長一層像熱二氧化矽一般，有很少的介面缺陷特性的極薄氧化層，來改介面特性和電性·在我們的實驗過程中，在成沈高介電質之前我們利用紫外光及上臭氧去成長一層高品質的極薄氧化層·

本論文首先研究以紫外加上臭氧在室溫成長的薄氧化層的基本特性·從實驗結果，我們發現利用紫外加上臭氧所成長的二氧化矽具有自我限制的飽和成長特性·接下來討論不同的沈積後退火的溫度在沈高介電質之前我們利用紫外光及上臭氧去成長一層高品質的極薄氧化層·介由電性的量得到一個適合的沈積後退火的溫度(900oC 30sec)·在第二章最後比較了有做紫外光臭氧表面、沒有做過任合表面處理及做了紫外光臭氧之後加上 NH3 電漿的氮化的表面處理·從漏電流密度、遲滯現象、ＴＺＢＤ、等效氧化層厚度的電性觀點來看，我們發現在沒有做過任合表面處理不管是從漏電流密度、遲滯現象、ＴＺＢＤ、等效氧化層厚度都不如有做紫外光臭氧的表面處理，而在做了紫外光臭氧之加 NH3 電漿的氮化的效氧化層厚度下表面處理雖然等效氧化層厚度下降，但大量的氮合併造成其它電性的衰退，像是漏電流密度、遲滯現象、ＴＺＢＤ·總合上面的結論來看，我們得到紫外光臭氧的表處理是最佳的化的條件·

在本論文的最後，利用第二章的最佳化的條件去做成 nMOSFETs 同時去把沒有做表面處理條件做成 nMOSFETs 來做比較．經由電性上的結果來看，發現有明顯的改善．最後利用 CVS 去探討可靠度，不管是從表面缺陷密度的增加量和 Bulk 的缺陷密度的增加量都也有明顯的改善．而且從結果得知不管是否有經過表面處理，都是 Bulk 的缺陷密度的增加量為造成臨限電壓偏移的主要原因．

Characteristic and Investigation of High-k ($HfAlO_xN_y$) Dielectric on MOS Devices

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Abstract

According to the scaling rules, aggressive scaling has led to silicon dioxide (SiO_2) gate dielectrics as ultra thin in state-of-the-art CMOS technologies. As a consequence, static leakage power due to direct tunneling through the gate oxide has been increasing at an exponential rate. As technology roadmaps call for sub-10Å gate oxides within the next five years, a variety of alternative high-*k* materials are being investigated as possible replacements for SiO_2. The higher dielectric constants in these materials allow the use of physically thicker films, potentially reducing the tunneling current while maintaining the gate capacitance needed for scaled device operation.

Hafnium oxide (HfO_2) and Alumina oxide (Al_2O_3) are the most potential high-*k*

material. Hafnium oxide has the higher dielectric constant, but it tends to crystallize at a relatively low process temperature (<500^{o}C). In order to overcome this problem, add Al_2O_3 in HfO_2 for improve crystallization temperature and barrier height. There are many interfacial states as high-k materials directly contact silicon. However, the control of SiO_2-like interface between high-κ dielectrics and silicon substrate pays more and more important, since the device performances and reliability characteristics are strongly affected by the interface quality. Therefore we want to grow like thin thermal SiO_2 that have very lower interface state to improve the interfacial layer and electrical characteristics. In this thesis, the basic properties of the ozone oxide were studied first. A saturated oxidation was observed in the growth curves and the resultant self-limiting property. Then different post deposition anneal is studied on $HfAlO_xN_y$ gate dielectric prior UV ozone treatment. PDA can effectively improve gate dielectric quality. Therefore, post deposition anneal must to do but a suitable anneal temperature is very important on electrical characteristics. In this chapter, we find a suitable anneal temperature to improve electrical characteristics. From the hysteresis , leakage density and time zero to breakdown determine the post deposition anneal at 900 ^{o}C and that has excellent electrical characteristics. We compared with UV ozone treatment and without on electrical characteristics. We observe that, no matter on EOT, hystersis, leakage current density and TZBD have excellent electrical characteristics. By different NH_3 plasma treatment's time of UV ozone oxide prior to $HfAlO_xN_y$ gate dielectric deposition were investigated. We find that NH_3 nitridation would degrade device performance such hystersis, leakage current density and TZBD. Though EOT decreasing with the NH3 treatment‘s time increasing but that

improvement on electrical characteristic is little. We determine the optimum condition (UV ozone surface and post deposition anneal 900^{o}C 30s) by above result.

In the thesis final, we used optimum condition on chapter two to fabricate the nMOSFETs and a control sample (without treatment and PDA900^{o}C 30seconds after high k film deposit) was fabricated at the same time. We can observe that improved electrical characteristics on nMOSFET with UV ozone surface treatment.Then we estimate reliability of the $HfAlO_xN_y$ stacks nMOSFETs by constant voltage stress (CVS). We find that UV ozone surface treatment can improved delta interface state density and bulk charge trap density during the constant voltage stress compared with the control sample. We observe that the bulk charge density to dominate the threshold voltage shift charge during the constant voltage stress for with UV ozone treatment and without

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Contents

Table Captions

Chapter 1

Chapter 2

Chapter 3

Figure Captions

Chapter 1

Chapter 2

Chapter 3

CHAPTER 1

Introduction

1.1 Background

Recently, information technology (IT) revolution has progressed dramatically, as can be seen in the rapid spread of Internet and cellular phones. The revolution will change significantly our life and culture, and is expected to improve the quality of life. The progress and spread of the IT technology owe much to the recent remarkable progress of semiconductor technology, especially that of large integrated circuits (LSIs).the development of LSI technology has been made by downsizing its components such as MOSFETs (Metal Oxide Semiconductor Field Effect Transistors). By the scaling, can improve high speed, low cost and low cost and low power of LSIs, It has been realized. From the driving current of MOSFET I_{ds} can be well modeled by following equation:

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_t)^2$$

Form the equation the term (V_{gs}-V_t) is difficult to reduce because operation voltage was gradually decreased approach lower power consumption. To achieve high performance and promote driving current, the gate length and oxide thickness continue scaling down. The barriers of gate length shrinkage are lithography limited and short channel effects. Therefore, gate thickness of MOSFET should be reduced, as shown Figure 1-1. Thermal silicon dioxide has been used for the gate insulator of

MOSFETs. Thermal silicon dioxide is good dielectric for silicon because of that provides low surface trap density and low interface states density. The scaling of SiO_2 based dielectrics is no longer a practical choice when the oxide thickness drops below 13 Å because of the gate leakage current density becomes extremely large due to direct tunneling effect [1]. This is a big problem for low power device, resulting in huge leakage current in an entire LSI chip such as more than 100 A [2]. According to the 2004 ITRS roadmap, oxy-nitride can not meet the limit on gate leakage current density of low standby power logic circuit after 2006[3], shown in Table 1-1. For this reason, replacement of silicon dioxide as a gate insulator in MOSFET devices by materials of higher dielectric permittivity ε_r is motivated by the need of increasing the capacitance density without further reducing the thickness. By using high-k materials we can increase physical gate insulator thickness, basically by maintaining the same electrical characteristics of MIS (Metal Insulator Semiconductor) capacitor. Thus we can suppress the direct tunneling current by high-k materials, as shown in Figure 1-2.

Despite a considerable effort in this direction, the formation of a thin SiO_2 interface layer between silicon substrate and high k material appears to be unavoidable [4]. Most of high k materials are not stable in direct contact with silicon and require a thin SiO_2 layer to stabilize the dielectric film on silicon substrate. Thin SiO_2 layer can improve interface states, surface roughness and electronic characteristic.

Table 1-1 stresses the urgent need for high dielectric constant (ε_r) gate dielectrics for low stand-by power application after the year 2006[5]. For this reason, several alternative materials for silicon dioxide are currently being investigated. High-κ materials, including aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and

zirconium oxide (ZrO_2) etc [6]-[9], shown in Table 1.2**,** are the potential candidates to replace SiO_2. The most benefit for high-κ dielectrics is leakage current reduction by several orders of magnitude at the same EOT compared to SiO_2. However, in device performance point of view, a suitable gate dielectric candidate should also meet the other requirements, including high thermal stability, high carrier mobility, small oxide charges, good stress immunity and silicon process compatible.

1.2 Motivation

In the recent years, the minimum feature size of microelectronic devices has been continuously reduced. As the device scaling continues down to deep submicron scales, fundamental physical limits of device materials are becoming critical barrier. Recently, hafnium oxide had been proved as promising candidates for the gate dielectric due to their higher dielectric constant superior thermal stability, and leakage current by order of magnitude, but hafnium oxide encountered the integrated issues such as charge trapping shifted the flat band and mobility degradation.

From the high k standpoint, Al_2O_3 is inferior to HfO_2 ($\varepsilon_r \doteqdot 25$) but tends to crystallize at a relatively low process temperature ($<500^oC$). However, the crystallization temperature of HfO_2 is quite low, which restricts the thermal budget after the deposition and brings about the high leakage current and non-uniformity associated with grain boundaries. Despite this, the Al_2O_3 dielectric is an extremely promising candidate in terms of its chemical, thermal stability as well as its high barrier offset and band gap (barrier height of electron and hole are 2.9eV and 4.3eV, band gap about 8.3eV). In order to gain higher ε_r by HfO2 and gain superior thermal

stability, we add Al in HfO_2 for improve crystallization temperature and barrier height.

Despite a considerable effort in this direction, the formation of a thin SiO_2 interface layer between silicon substrate and high k material appears to be unavoidable. Most of high k materials are not stable in direct contact with silicon and require a thin SiO_2 layer to stabilize the dielectric film on silicon substrate. However, the control of SiO_2-like interface between high-κ dielectrics and silicon substrate pays more and more important, since the device performances and reliability characteristics are strongly affected by the interface quality. In order to control the interface layer between silicon substrate and high k material, UV ozone is used. We hope to control interface layer and improves that quality.

1.3 Organization of the Dissertation

In this thesis have four chapters in this dissertation. Chapter one shows the background and motivation for the application of the UV ozone oxide and the dielectric properties of high-κ dielectrics.

In chapter 2, the basic properties of the ozone oxide were studied in the first. The effects of UV ozone treatment prior the high k dielectric deposition by different post deposition annealing temperature were investigated in the second. High k dielectric of prior to with and without UV ozone treatment were investigated in the third. By NH3 plasma treatment on the UV ozone oxide of the high k dielectric stacks were investigated in the fourth.

In chapter 3, we used optimum condition on chapter two to fabricate the nMOSFETs and control sample was fabricated at the same time. We measure the basic electrical characteristics compared with control sample.

At the end of this thesis, conclusions are given in chapter 4.

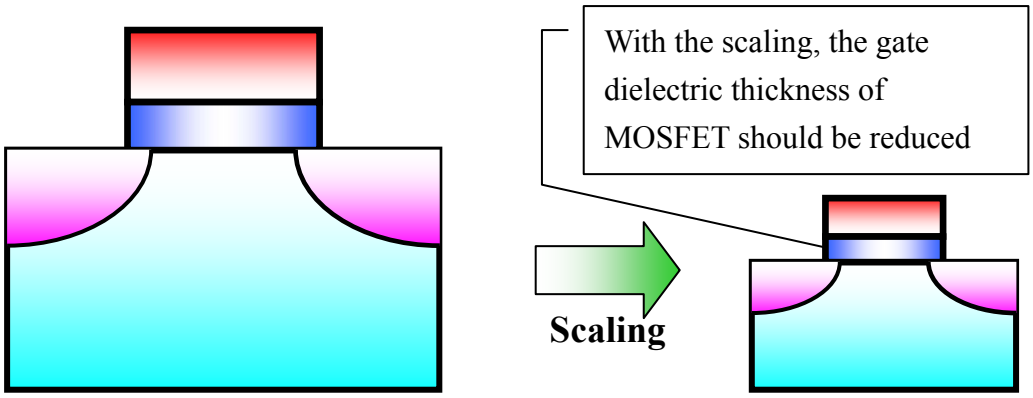


Figure 1-1 Scaling of MOSFETs

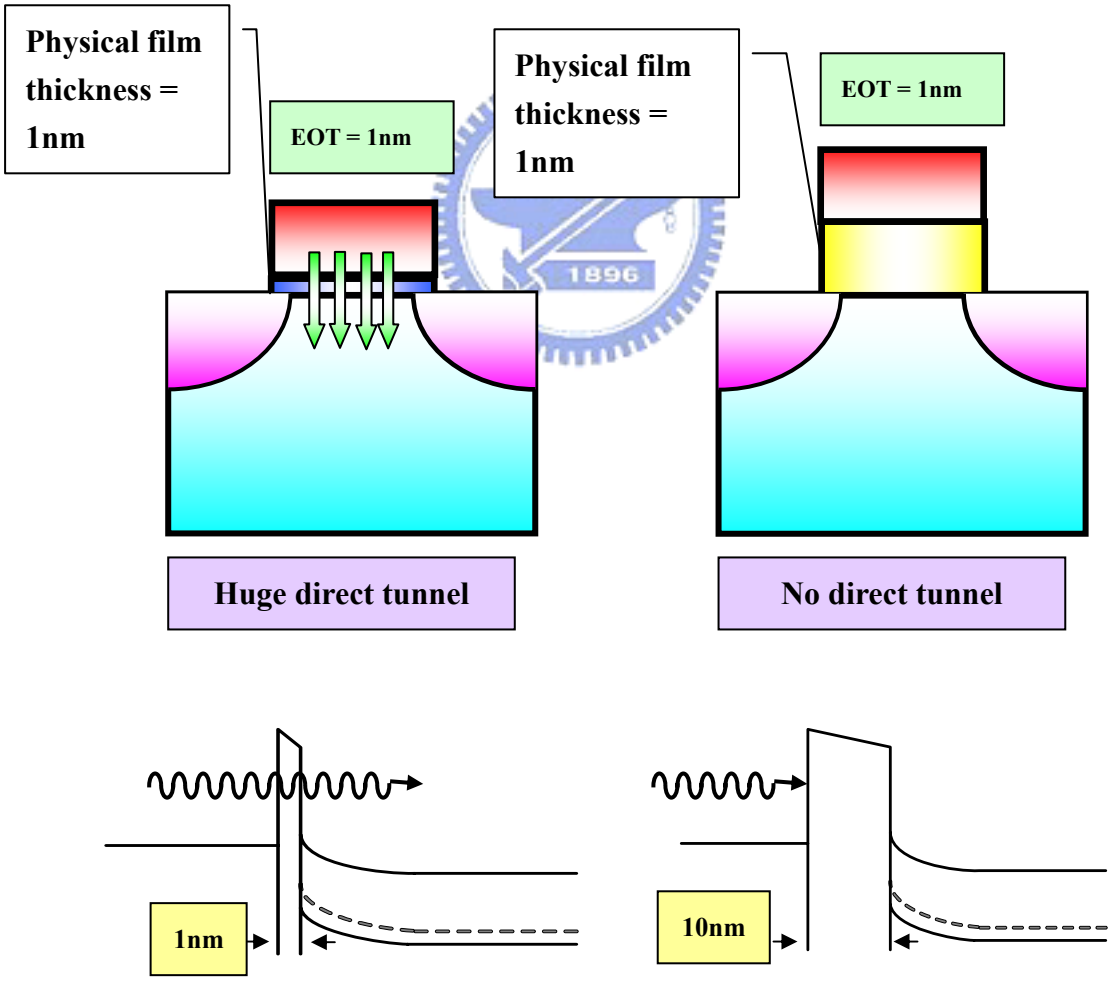
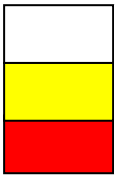


Figure 1-2 High k materials

Year of Production	2004	2005	2006	2007	2008
EOT(physical) for high-performance(nm)	1.2	1.1	1.0	0.9	0.8
Electrical thickness adjustment for gate depletion and inversion layer effects(nm)	0.8	0.7	0.7	0.4	0.4
Nominal gate leakage current desity limit(at 25℃)(A/cm^2)	450	520	600	930	1100



Manufacturable solutions, and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known

Table 1-1 International Technology Roadmap for Semiconductors.

	High-κ Dielectrics		
	HfO_2	ZrO_2	Al_2O_3
Bandgap (eV)	6.02	5.82	8.3
Barrier Height to Si (eV)	1.6	1.5	2.9
Dielectric Constant	~30	~25	9
Heat of Formation (Kcal/mol)	271	261.9	399
ΔG for Reduction ($MO_x + Si \rightarrow M + SiO_x$)	47.6	42.3	64.4
Thermal expansion coefficient (10^{-6} K^{-1})	5.3	7.01	6.7
Lattice Constant (Å) (5.43 Å for Si)	5.11	5.1	4.7 - 5.2
Oxide Diffusivity @ 950°C (cm^2/sec)		$1x10^{-12}$	$5x10^{-25}$

Table 1.2 Materials properties of high-κ dielectrics, Al_2O_3, ZrO_2, and HfO_2.

CHAPTER 2

Comparison of Various Surface Treatment on the $HfAlO_xN_y$ MOS Devics Characteristics

2.1 Introduction

The shrinkage in metal-oxide-semiconductor field effect transistor dimensions is accompanied by a scaling of gate oxide thickness. It is well known that the scaling of conventional SiO_2 is approaching the predicted limit due to large direct tunneling leakage current, thereby presenting a fundamental challenge to continual scaling [5]. Therefore, an alternative gate dielectric material is needed to replace SiO_2. High-κ dielectrics, such as HfO_2, Al_2O_3 are the potential candidates because of thicker film is utilized to reduce the direct tunneling leakage current while maintaining the same gate capacitance[10]-[13]. This is primarily based on the perception that non-uniform distribution of EOT, threshold voltage, and gate leakage will result when device size is comparable to the grain size in high-density integrated circuits. Given the requirement for an amorphous high-k gate dielectric, the ranking of HfO_2 as a desired high-k dielectric drop considerable, because it tends to crystallize at a relatively low process temperature (<500^oC). In order to overcome this problem, add Al in HfO_2 for improve crystallization temperature and barrier height[14]-[18].

However, the control of SiO_2-like interface between high-κ dielectrics and silicon substrate pays more and more important, since the device performances and

reliability characteristics are strongly affected by the interface quality. Nitridation of the Si surface using NH_3 prior to the deposition of high-κ gate dielectrics has been shown to be effective in achieving the low EOT (equivalent oxide thickness) and preventing boron penetration [19], [20]. However this technique results in higher interface charges [21], which leads to higher hysteresis and reduced channel mobility. Ozone-formed oxide (ozone oxide) has superior characteristics. Even when the formation temperature is less then 400°C, ozone oxide has a high film density comparable to that of the device-grade oxide film formed at higher temperature (e.g. 900°C) [22], a low interface trap density ($D_{it} \sim 10^{10}$ cm^2) [23], and a much thinner structural transition layer near the SiO_2/Si interface [24]. The aim of this experiment was to investigate the interfacial issues at $HfAlO_xN_y$/silicon interface. The ozone surface treatment was employed to improve the interface quality between $HfAlO_xN_y$ and silicon substrate.

2.2 Experiment Details

2.2.1 Experiment Details of Ozone Oxide Growth

4 inch p-type (100) silicon wafers were cleaned by standard RCA processes with HF-last for the removal of the particles and native oxides. Figure 2-1 showed the schematic diagram of UV ozone system. The ozone generator (AnserosPAP-2000) decomposed the oxygen molecular to generate ozone gas by high electrical field. The ozone gas was mixed with UV lamp in chamber. By changing the oxygen flow and ozone generation power, the ozone concentration in the chamber could be adjusted. Ozone oxide was grown on Si wafer in the chamber at room temperature. The

relationship between the ozone concentration in the DI water and thickness change of ozone oxide was under investigation. N&K was utilized to measure the ozone oxide thickness.

2.2.2 Different Post Deposition Anneal Characteristics of HfAlOxNy MOS Devices with Ozone Surface Treatments

Field oxide 5000Å isolated MOS capacitors were fabricated on 4 inch p-type (100) silicon wafers. After forming field oxide isolation, wafers were cleaned by standard RCA processes with HF-last. Prior to high-κ dielectrics deposition, the samples were prepared by Ozone oxide. UV ozone was used to grow an ultra-thin ozone oxide about 9~11Å (measured by N&K). After UV ozone surface treatments, a high temperature 900^{o}C 60seconds was used for densify ozone oxide. $HfAlO_xN_y$ was then deposited at room temperature and 7.6E-3 torr by ion sputter system, as shown in Figure 2-2, followed by a different high temperature (as deposition, 500^{o}C, 600^{o}C, 700^{o}C, 800^{o}C,900^{o}C) post deposition annealing (PDA) in the nitrogen ambient for 30 seconds were investigated. Aluminum metal served as the gate electrode was created by a thermal evaporation system. After gate electrodes patterned and backside contact was formed by thermal evaporation. The cross section and the total process flow were shown in Figure. 2-3. Square capacitors of 1×10^{-4} cm^2 areas with field oxide isolation are used to evaluate the gate oxide integrity. The equivalent oxide thickness (EOT) was extracted by fitting the measured high-frequency (100 kHz) capacitance-voltage (*C-V*) data from Hewlett-Packard (HP) 4284 LCR meter under accumulation condition. UCLA CVC simulation program was utilized to obtain the accurate flat band voltage (V_{FB}). The *C-V* hysteresis phenomenon was measured by sweeping the gate voltage from accumulation to inversion then back. The tunneling leakage current

density-electric field (*J-E*) and the reliability characteristics of MOS capacitors were measured by semiconductor parameter analyzer HP 4156C.

2.2.3 UV Ozone Treatment and Without UV Ozone Treatment Characteristics of HfAlOxNy MOS Devices

Field oxide 5000Å isolated MOS capacitors were fabricated on 4 inch p-type (100) silicon wafers. After forming field oxide isolation, wafers were cleaned by standard RCA processes with HF-last. Prior to high-κ dielectrics deposition, either the samples were prepared by ozone oxide or without ozone oxide were investigated. UV ozone was used to grow an ultra-thin ozone oxide about 9~11Å (measured by N&K). After UV ozone surface treatments sample with a high temperature 900^{o}C 60seconds was used for density ozone oxide. $HfAlO_xN_y$ was then deposited at room temperature and 7.6E-3 torr by ion sputter system. Followed by a high temperature 900^{o}C post deposition annealing (PDA) in the nitrogen ambient for 30 seconds. Aluminum metal served as the gate electrode was created by a thermal evaporation system. After gate electrodes patterned and backside contact was formed by thermal evaporation. The cross section and the total process flow were shown in Figure 2-4. Square capacitors of 1×10^{-4} cm^2 areas with field oxide isolation are used to evaluate the gate oxide integrity. The equivalent oxide thickness (EOT) was extracted by fitting the measured high-frequency (100 kHz) capacitance-voltage (*C-V*) data from Hewlett-Packard (HP) 4284 LCR meter under accumulation condition. UCLA CVC simulation program was utilized to obtain the accurate flat band voltage (V_{FB}). The *C-V* hysteresis phenomenon was measured by sweeping the gate voltage from accumulation to inversion then back. The tunneling leakage current density-electric field (*J-E*) and the reliability characteristics of MOS capacitors were measured by semiconductor

parameter analyzer HP 4156C.

2.2.4 NH3 Plasma Treatment on Ozone Surface Treatment Characteristics Of HfAlOxNy MOS Devices

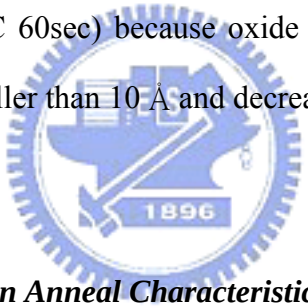
Field oxide 5000Å isolated MOS capacitors were fabricated on 4 inch p-type (100) silicon wafers. After forming field oxide isolation, wafers were cleaned by standard RCA processes with HF-last. Prior to high-κ dielectrics deposition, the samples were prepared by Ozone oxide. UV ozone was used to grow an ultra-thin ozone oxide about 9~11Å (measured by N&K). NH3 plasma treatment (30, 60 90 120 seconds) is prepared of the UV ozone oxide surface. After that a high temperature 900^{o}C 60seconds was used for repair damage at plasma treatment. $HfAlO_xN_y$ was then deposited at room temperature and 7.6E-3 torr by ion sputter system. Followed by a high temperature 900^{o}C post deposition annealing (PDA) in the nitrogen ambient for 30 seconds. Aluminum metal served as the gate electrode was created by a thermal evaporation system. After gate electrodes patterned and backside contact was formed by thermal evaporation. The cross section and the total process flow were shown in Figure 2-5. Square capacitors of 1×10^{-4} cm^2 areas with field oxide isolation are used to evaluate the gate oxide integrity. The equivalent oxide thickness (EOT) was extracted by fitting the measured high-frequency (100 kHz) capacitance-voltage (*C-V*) data from Hewlett-Packard (HP) 4284 LCR meter under accumulation condition. UCLA CVC simulation program was utilized to obtain the accurate flat band voltage (V_{FB}). The *C-V* hysteresis phenomenon was measured by sweeping the gate voltage from accumulation to inversion then back. The tunneling leakage current density-electric field (*J-E*) and the reliability characteristics of MOS capacitors were measured by semiconductor parameter analyzer HP 4156C.

2.3 Results and Discussions

2.3.1 Basic Property Investigation of the Ozone Oxide

The growth curves of UV ozone oxide as a function of time to grow up shown in Figure 2-6. A saturated oxidation was observed in the growth curves and the resultant self-limiting property could improve the thickness uniformity.

Figure 2-7 shown UV ozone oxide growing 5min with annealing 900^{o}C 60sec in the nitrogen ambient and without. We can observe thinner oxide thickness after a high temperature (RTA 900oC 60sec) because oxide become more densify. We can control the interface layer smaller than 10 Å and decrease EOT.



2.3.2 Different Post Deposition Anneal Characteristics of HfAlOxNy MOS Devices with Ozone Surface Treatments Effect

Figure 2-8, Figure 2-9 showed the normalized capacitance-voltage (*C-V*) characteristics and V_{fb} Weibull distribution of $HfAlO_xN_y$ stacked gate dielectrics with various post deposition anneal on UV ozone treatment samples. Post deposition annealing could reduce the interface trap density exhibited by more sharp *C-V* characteristics. The *C-V* curve of Ozone-treated PDA 900^{o}C capacitors was kink free and exhibited good interface properties. From V_{fb} Weibull distribution, |Vfb| decreasing depends on PDA temperature increasing. Speculation on inter face state decreasing with PDA temperature increasing.

The hysteresis of various post deposition anneal on UV ozone treatment

samples was compared in Figure 2-10. The hysteresis voltage was defined as the flat band voltage difference between the forward and backward swept *C-V* curves, which might be contributed from the trapped charges within high-κ bulk or interface. The samples without PDA treatment revealed large hysteresis. *C-V* hysteresis decreasing depends on PDA temperature increasing. Indicate Ozone-treated PDA 900^{o}C sample exhibited almost hysteresis-free characteristics.

Figure 2-11 showed the EOT Weibull distribution of $HfAlO_xN_y$ stacked gate dielectrics with various PDA temperatures on UV ozone treatment samples. We can observe that, PDA(500^{o}C~900^{o}C) treatment sample EOT smaller than without treatment(8~11EOT decrement). Therefore, PDA has to do because PDA can improve the high k quality and decrease EOT.

Leakage current density of $HfAlO_xN_y$ stacked gate dielectrics with various PDA temperatures on UV ozone treatment as a function of effective electric field (E_{eff}):

$E_{eff} = (V_g - V_{fb}) / EOT$

for samples showed in Figure 2-12. Figure 2-13 showed the Leakage current density at V_{fb}-1 distribution. From Figure 2-12 and Figure 2-13, indicate 900^{o}C PDA treatment could lower the leakage current density at V_{fb}-1 at least 1~2 order. From leakage density current revealed that a suitable PDA temperature can further improve the dielectric properties.

Synthesized above mentioned in Figure 2-14, PDA treatment could reduced current density at least 1~ 2 orders of magnitude with smaller than 8~11Å EOT decrement.

The time-zero dielectric breakdown (TZDB) reliability investigation were shown in Figs. 3-15. PDA can promote the reliability. Sample without PDA treatment

was supposed to have poor dielectric quality, which will degrade the dielectric reliability. After PDA treatments, the high k dielectric quality was improved, and the reliability therefore became superior.

2.3.3 Comparison of UV Ozone Treatment and Without UV Ozone Treatment Characteristics of HfAlOxNy MOS Devices

Figure 2-16, Figure 2-17 showed the normalized capacitance-voltage (*C-V*) characteristics and V_{fb} Weibull distribution of $HfAlO_xN_y$ gate dielectric PDA 900°C with ozone surface treatment and without treatment.

The hysteresis of UV ozone treatment samples and without were compared in Figure 2-18. The hysteresis voltage was defined as the flat band voltage difference between the forward and backward swept *C-V* curves, which might be contributed from the trapped charges within high-κ bulk or interface. Fortunately, ozone surface treatment resulted in excellent hysteresis behavior.

Figure 2-19 showed the EOT Weibull distribution of $HfAlO_xN_y$ stacked gate dielectrics with PDA 900°C on UV ozone treatment samples and without zone treatment. We can observe that, ozone treatment sample EOT smaller than without treatment (1~2Å EOT decrement). Maybe ozone treatment prevent interfacial to grow, therefore ozone treatment sample has smaller EOT.

Leakage current density of $HfAlO_xN_y$ stacked gate dielectrics with PDA 900°C on UV ozone treatment samples and without zone treatment were compared. Various surface treatments as a function of effective electric field (E_{eff}):

$$E_{eff} = (V_g - V_{fb}) / EOT$$

for samples showed in Figure 2-20. Figure 2-21 showed the Leakage current density @ V_{fb}-1 distribution. From Figure 2-20 and Figure 2-21, indicate ozone treatment could lower the leakage current density at V_{fb}-1 at least 2.5 times. From leakage density current revealed that ozone surface treatment can further improve the dielectric properties.

The time-zero dielectric breakdown (TZDB) reliability investigation were shown in Figure 2-22. Ozone treatment can promote the reliability. Sample without surface treatment was supposed to have poor interface between $HfAlO_xN_y$ and Silicon substructure which will degrade the dielectric reliability. After ozone surface treatment, the high k dielectric quality was improved, and the reliability therefore became superior.

2.3.4 Comparison of Different NH3 Plasma Treatment on Ozone Surface Characteristics Of HfAlOxNy MOS Devices

Figure 2-23, Figure 2-24 showed the normalized capacitance-voltage (*C-V*) characteristics and V_{fb} Weibull distribution of $HfAlO_xN_y$ gate dielectric PDA 900^oC prior to ozone surface treatment follow various NH_3 plasma treatment's times (30s, 60s, 90s, 120s). From the V_{fb} weibull and C-V curve we can observer negative V_{fb} shift depend on NH_3 plasma treatment's times increase. Indicated NH3 plasma treatment has positive charges accumulation at interface. Apparent C-V deterioration was observed in NH_3 plasma treatment sample due to the excess nitrogen concentration compels more Si bonding constraints at the interface. Indicate nitrogen at interface bring positive charges. The C-V curve of without NH3 plasma treatment capacitors was kink free and exhibited good interface properties.

The hysteresis of various NH_3 plasma treatment's times on prior UV ozone treatment samples were compared in Figure 2-25. The hysteresis voltage was defined as the flat band voltage difference between the forward and backward swept *C-V* curves, which might be contributed from the trapped charges within high-κ bulk or interface. Apparent hysteresis Weibull distribution was observed NH_3 plasma treatment samples exhibited larger hysteresis depend on plasma treatment's time increasing. Perhaps due to excess nitrogen concentration compels more Si bonding constraints at interface.

Figure 2-26 showed the EOT Weibull distribution of $HfAlO_xN_y$ gate dielectric PDA 900°C prior to ozone surface treatment follow various NH_3 plasma treatment's times. We can observe that, EOT decreasing with NH_3 plasma treatment's time increasing. Maybe, the increasing of interface layer's ε_r is caused by the mixing nitrogen. Therefore bring about the EOT decrement.

Leakage current density of $HfAlO_xN_y$ gate dielectric PDA 900°C prior to ozone surface treatment follow various NH_3 plasma treatment's times were compared. Various plasma treatment's time as a function of effective electric field (E_{eff}):

$$E_{eff} = (V_g - V_{fb}) / EOT$$

for samples showed in Figure 2-27. Figure 2-28 showed the Leakage current density @ V_{fb}-1 distribution. From Figure 2-27 and Figure 2-28, indicate NH_3 plasma treatment could higher the leakage current density at V_{fb}-1. From leakage density current revealed that NH_3 plasma treatment maybe damaged the dielectric properties.

The time-zero dielectric breakdown (TZDB) reliability investigation were shown in Figure 2-29. NH_3 plasma treatment has poor reliability. NH_3 plasma treatment samples were supposed to have poor interface between $HfAlO_xN_y$ and

Silicon substructure which will degrade the dielectric reliability. Maybe excess nitrogen concentration compels more Si bonding constraints at interface or plasma damage the interface.

2.4 Summary

In this chapter, the basic properties of the ozone oxide were studied first. A saturated oxidation was observed in the growth curves and the resultant self-limiting property could improve the thickness uniformity. UV ozone oxide after rapid thermal oxidation become more densify and we can control thickness less 10 Å avoid growing thick interface layer.

Then different post deposition anneal is studied on $HfAlO_xN_y$ gate dielectric prior UV ozone treatment. PDA can effectively improve gate dielectric quality. Therefore, post deposition anneal must to do but a suitable anneal temperature is very important on electrical characteristics. In this chapter, we find a suitable anneal temperature to improve electrical characteristics. From the hysteresis , leakage density and time zero to breakdown determine the post deposition anneal at 900 ^oC and that has excellent electrical characteristics.

We compared with UV ozone treatment and without on electrical characteristics. We observe that, lower EOT and leakage density by UV ozone treatment. Therefore, UV ozone can improve the interface quality. At other electrical characteristic such hystersis also were improved.

By different NH_3 plasma treatment's time of UV ozone oxide prior to

$HfAlO_xN_y$ gate dielectric deposition were investigated. Significantly large fixed charges and hysteresis of NH_3 nitridation would degrade device performance. Form other electrical characteristics view, though EOT decreasing with the NH3 treatment‘s time increasing but that improvement on electrical characteristic is little. Leakage current density raises with the time of NH_3 plasma treatment increasing. Indicate NH_3 plasma treatment could higher the leakage current density. From leakage density current revealed that NH_3 plasma treatment maybe damaged the dielectric properties. Time zero to breakdown also shows the bad electrical characteristic on NH_3 plasma treatment.

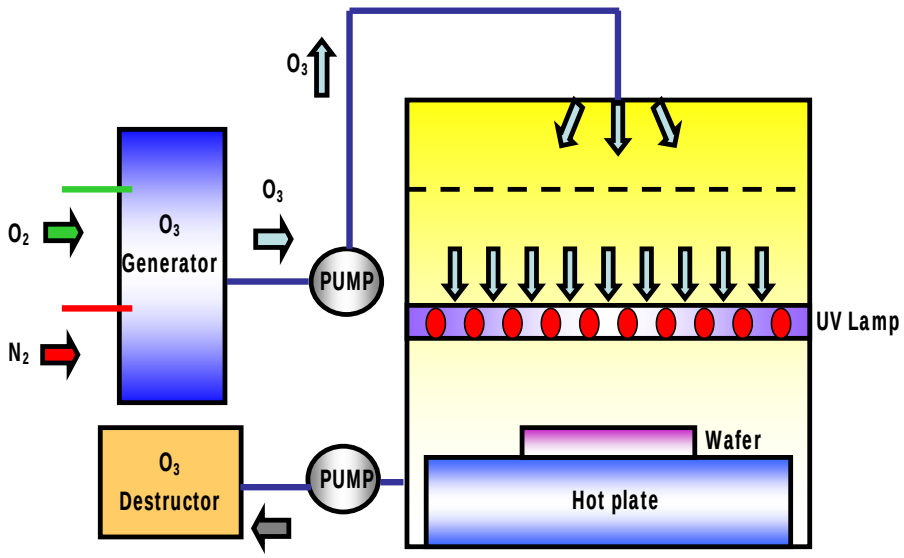


Figure 2-1 UV ozone system schematic diagram

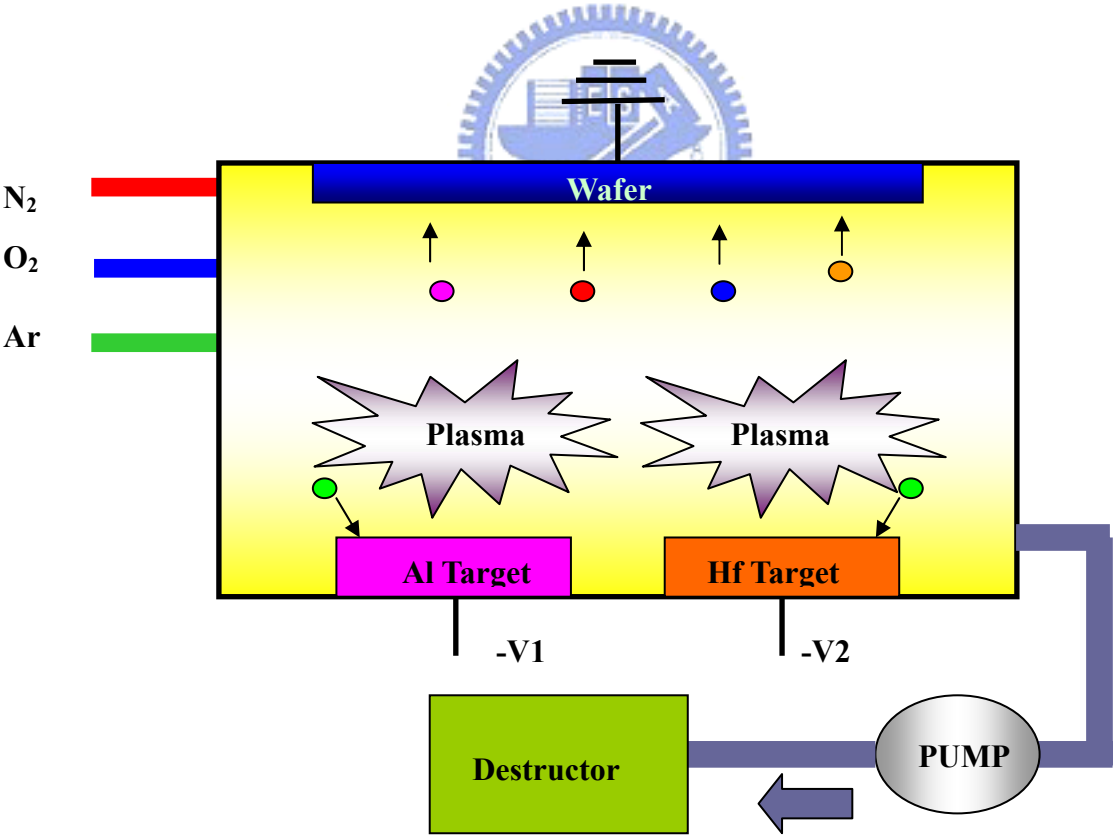


Figure 2-2 Sputter system schematic diagram

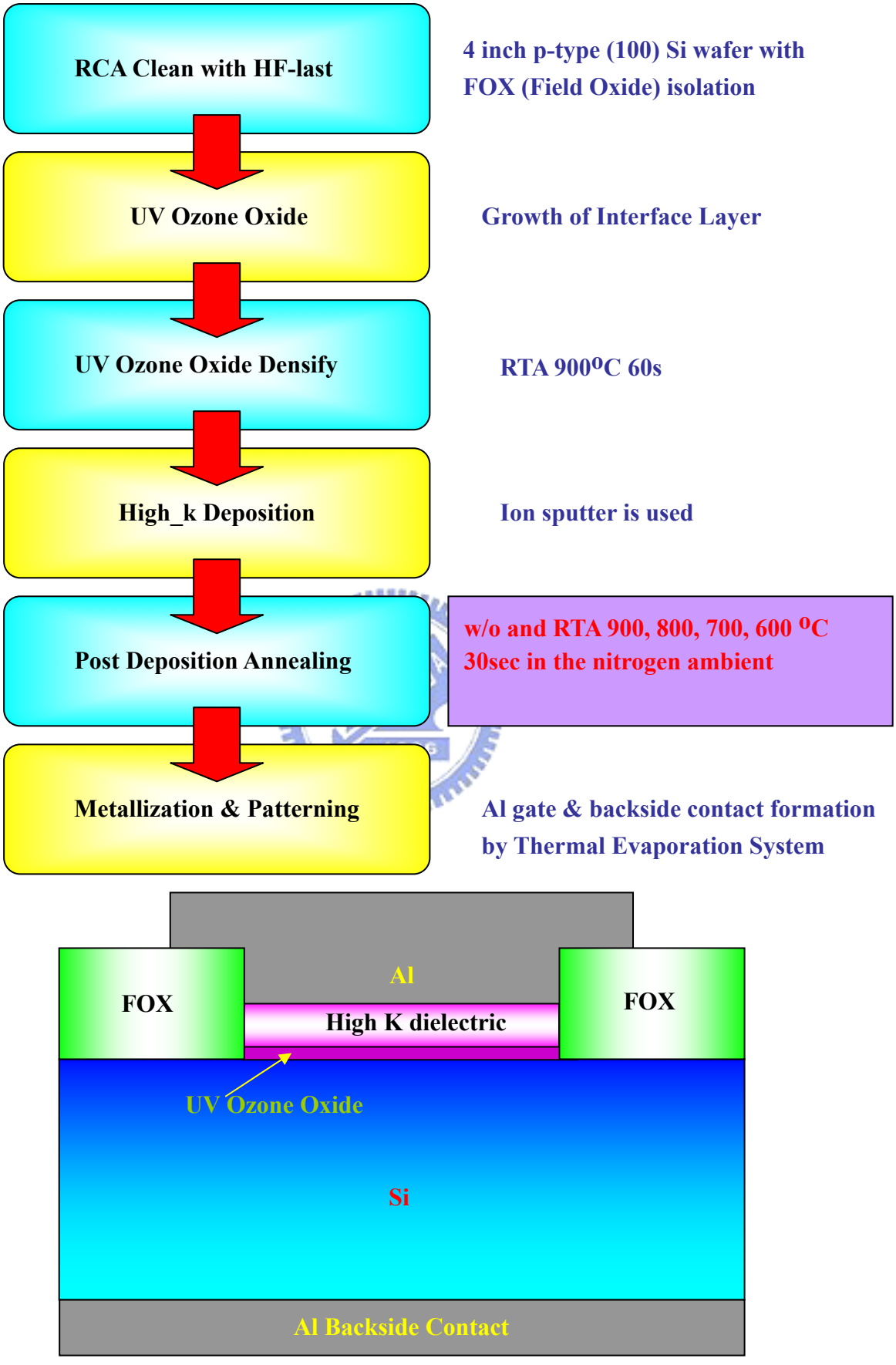


Figure 2-3 Cross section and process flow

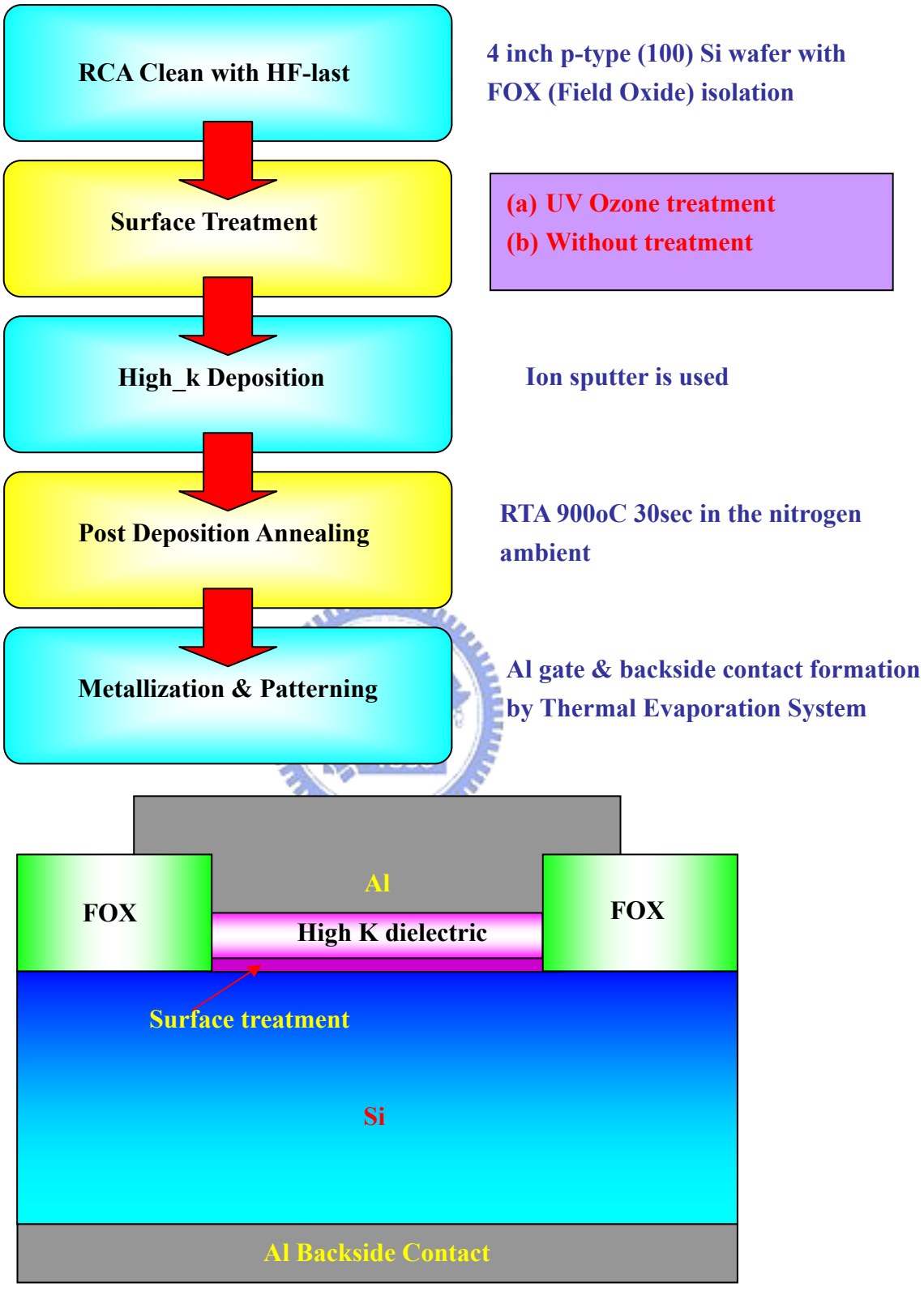


Figure 2-4 Cross section and process flow

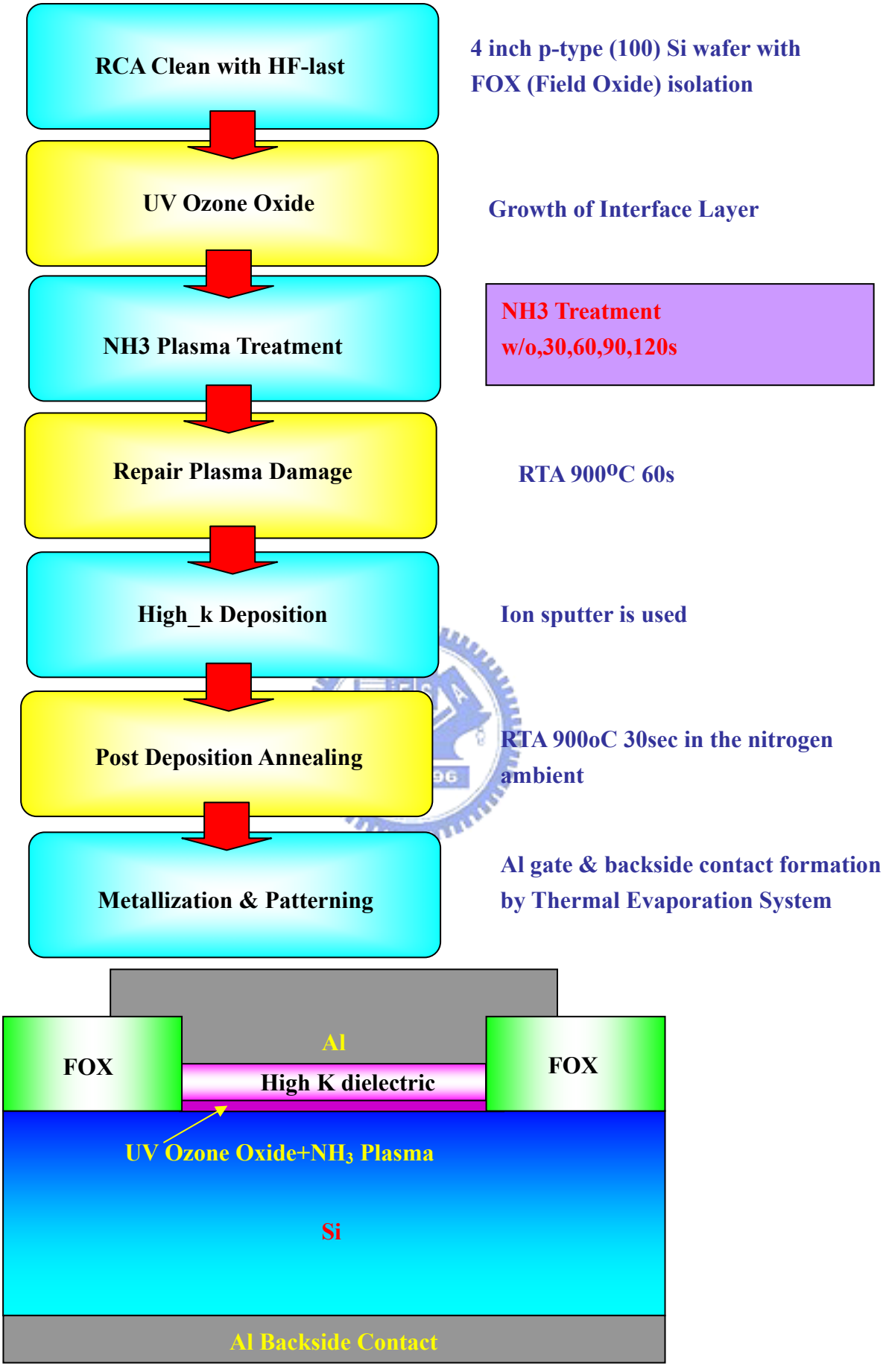


Figure 2-5 Cross section and the process flow

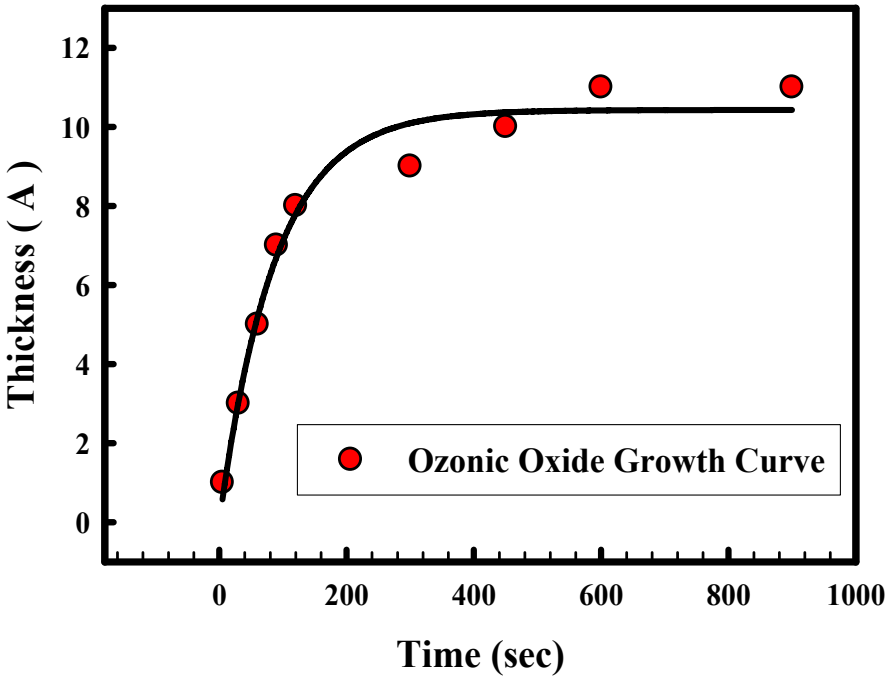


Figure 2-6 Growing curve of UV ozone oxide

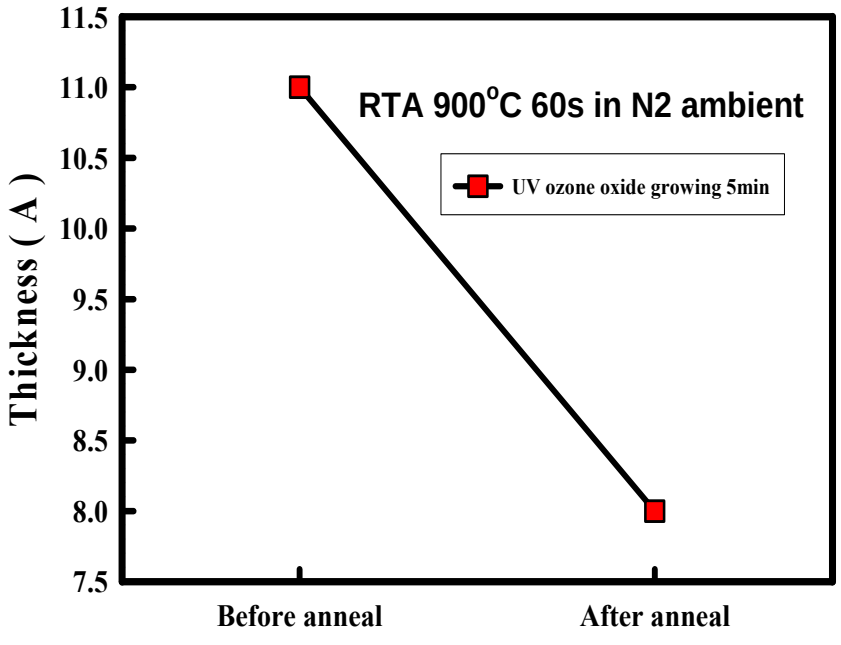


Figure 2-7 UV ozone oxide growing 5min with annealing 900°C 60sec in the nitrogen ambient and without

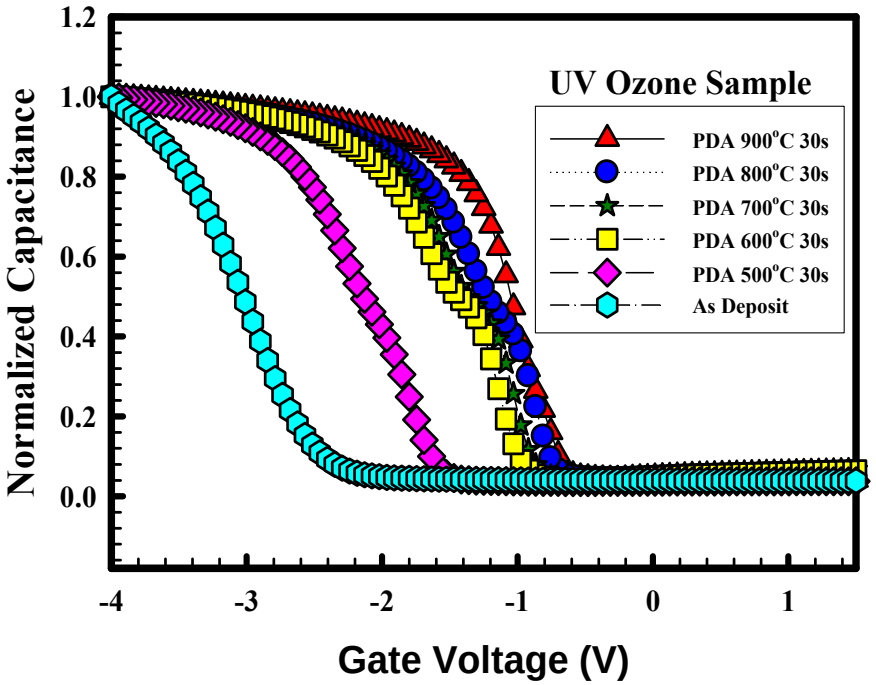


Figure 2-8 Normalized capacitance-voltage (*C-V*) characteristics of $HfAlO_xN_y$ stacked gate dielectrics with various post deposition anneal on UV ozone treatment samples.

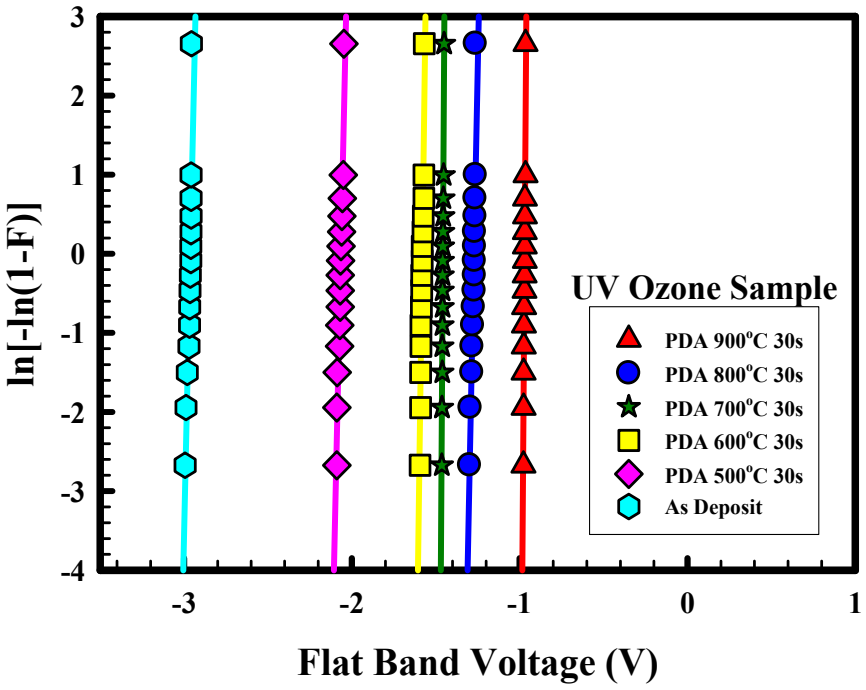


Figure 2-9 Vfb Weibull distribution of $HfAlO_xN_y$ stacked gate dielectrics with various post deposition anneal on UV ozone treatment samples.

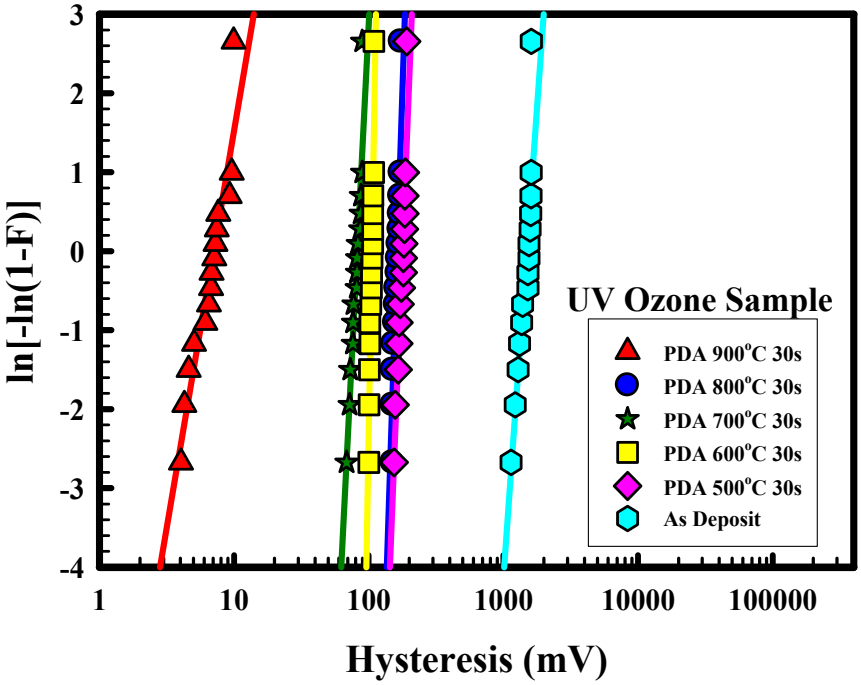


Figure 2-10 The hysteresis of various post deposition anneal on UV ozone treatment

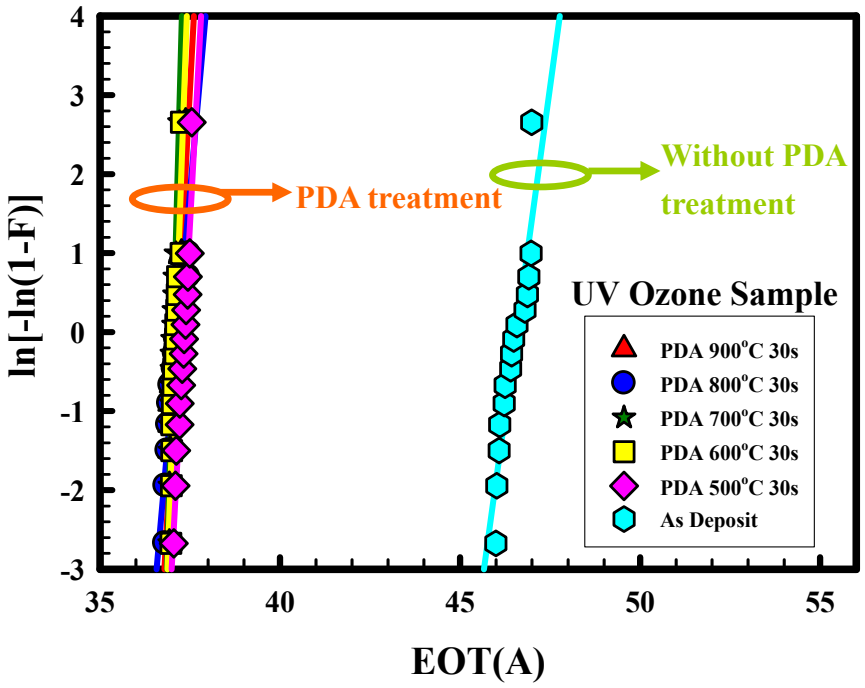


Figure 2-11 EOT Weibull distribution of HfAlOxNy stacked gate dielectrics with various PDA temperatures on UV ozone treatment samples.

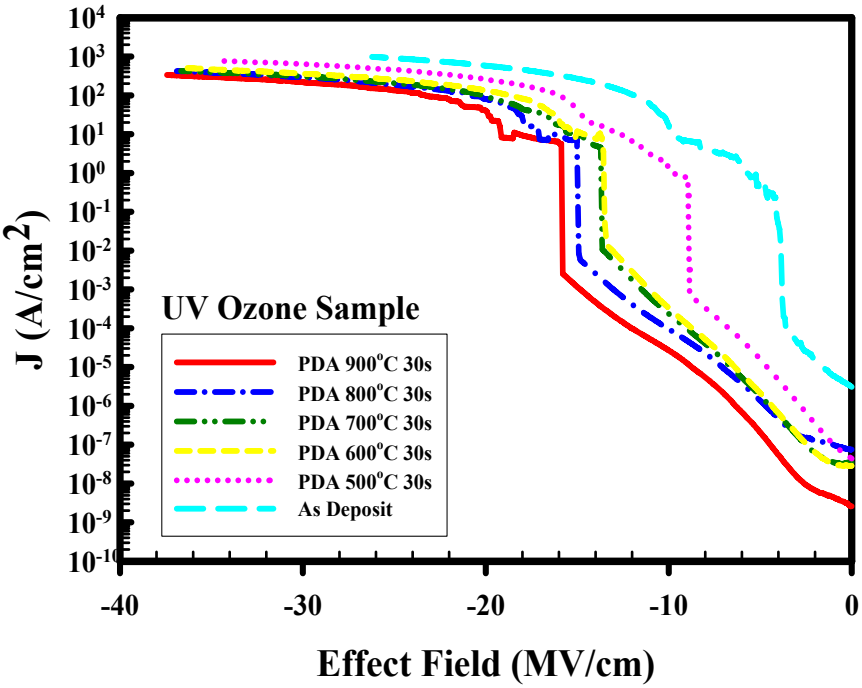


Figure 2-12 Leakage current density of HfAlOxNy stacked gate dielectrics with various PDA temperatures on UV ozone treatment

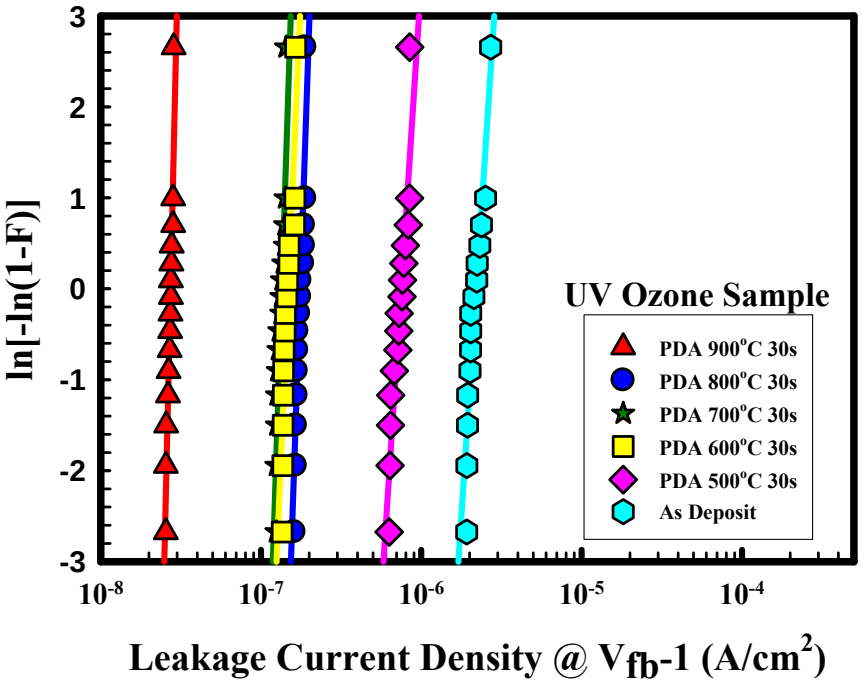


Figure2-13 Leakage current density at V_{fb}-1 distribution of HfAlOxNy stacked gate dielectrics with various PDA temperatures on UV ozone treatment samples.

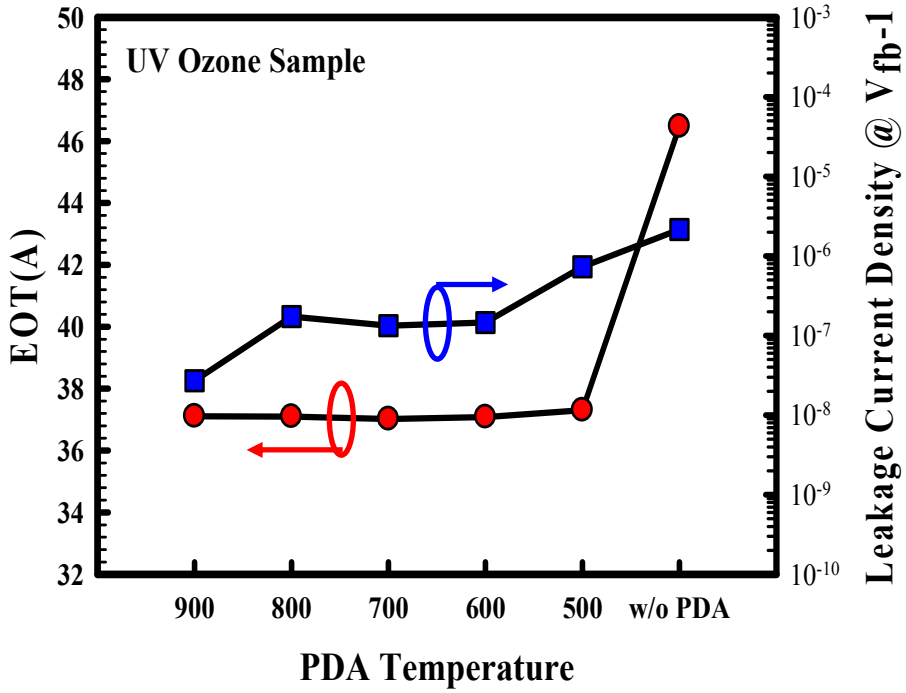


Figure 2-14 Assembled the EOT and leakage current density at V_{fb}-1 of HfAlOxNy stacked gate dielectrics with various PDA temperatures on UV ozone treatment samples.

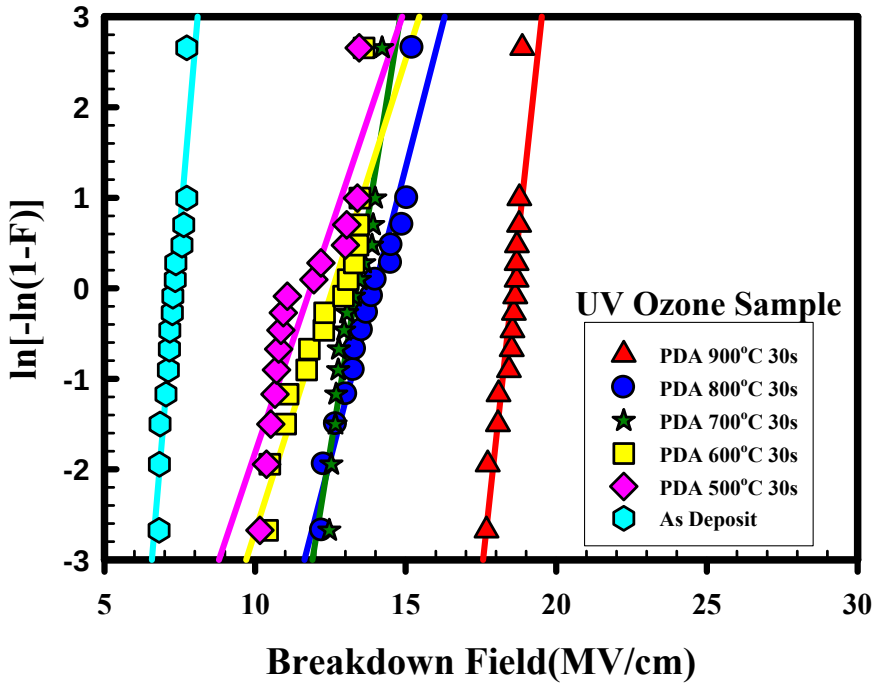


Figure 2-15 TZBD of HfAlOxNy stacked gate dielectrics with various PDA temperatures on UV ozone treatment samples.

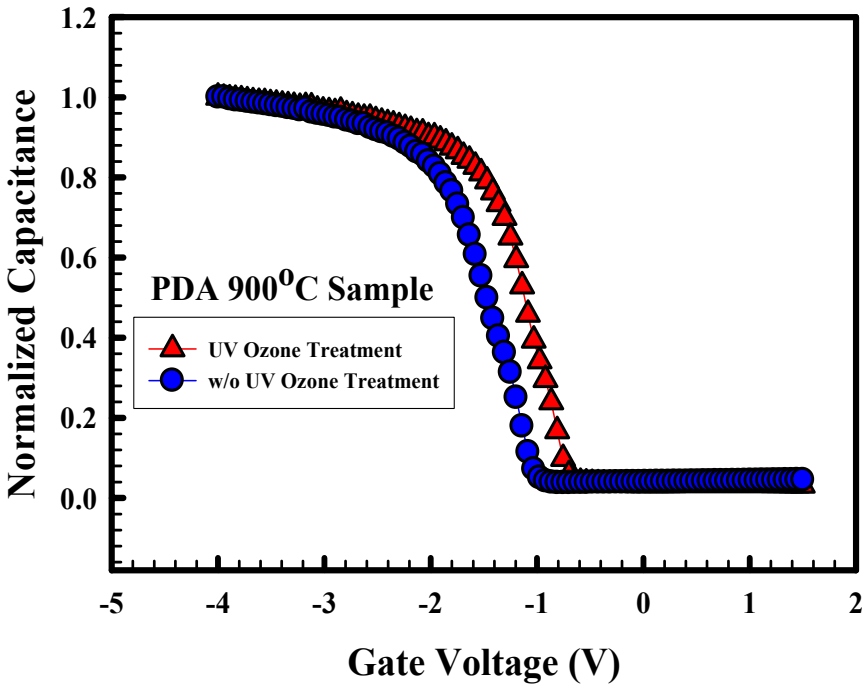


Figure 2-16 Normalized capacitance-voltage (*C-V*) characteristics of $HfAlO_xN_y$ gate dielectric PDA 900°C with ozone surface treatment and without treatment.

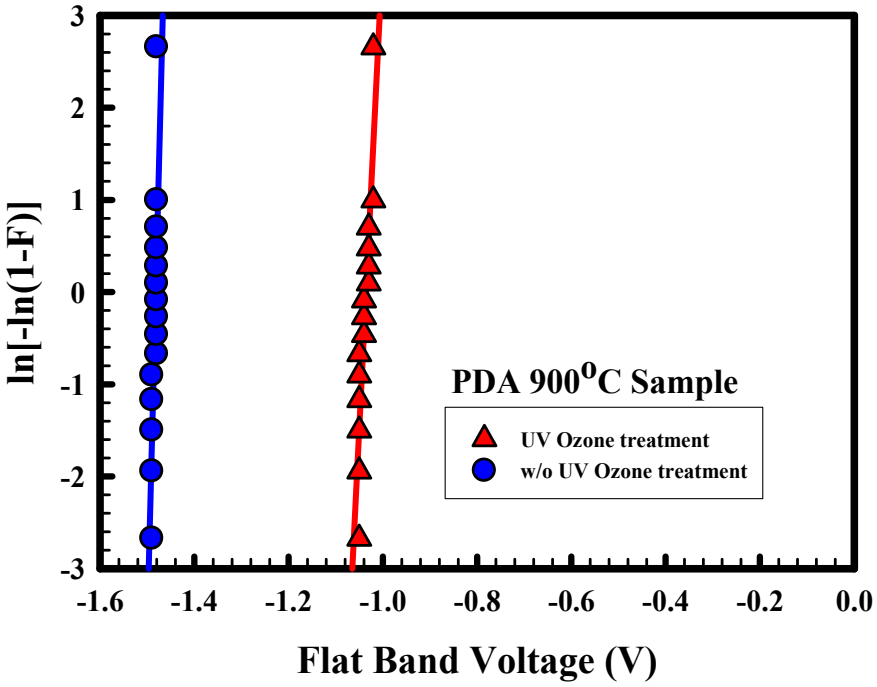


Figure 2-17 Vfb Weibull distribution of $HfAlO_xN_y$ gate dielectric PDA 900°C with ozone surface treatment and without treatment.

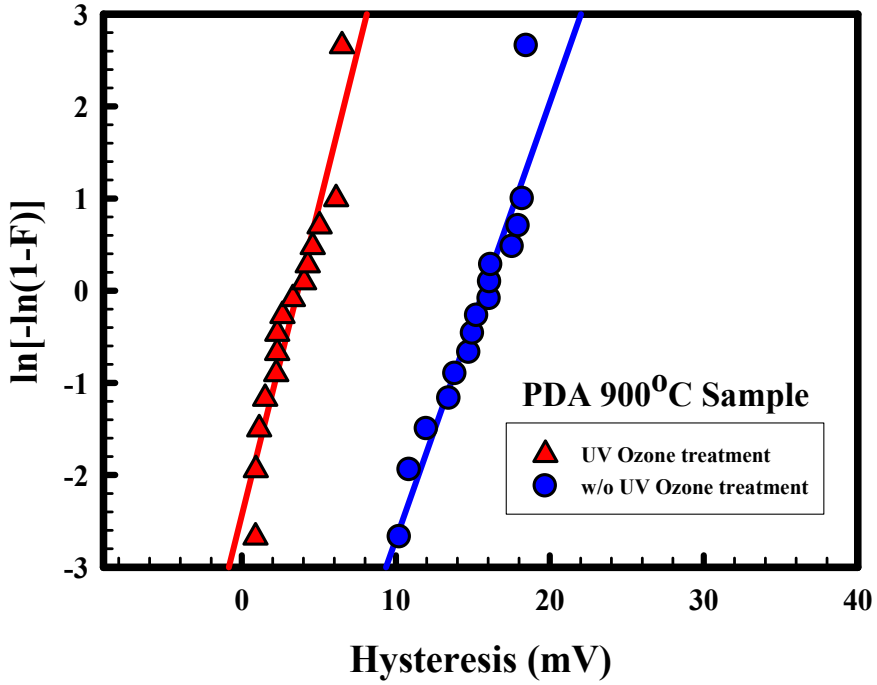


Figure 2-18 The hysteresis of UV ozone treatment samples and without

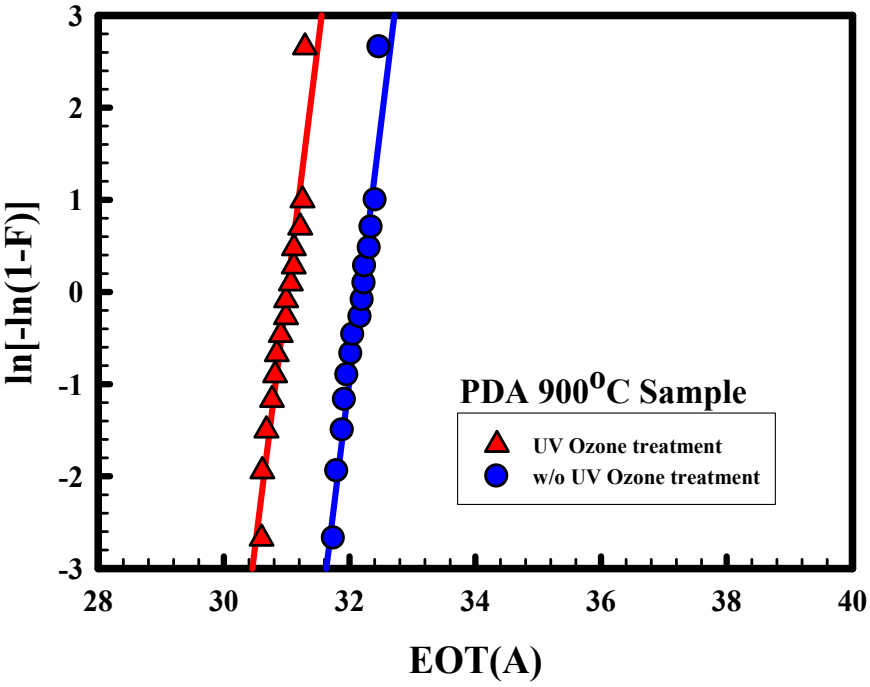


Figure2-19 EOT Weibull distribution of HfAlOxNy stacked gate dielectrics with PDA 900°C on UV ozone treatment samples and without zone treatment.

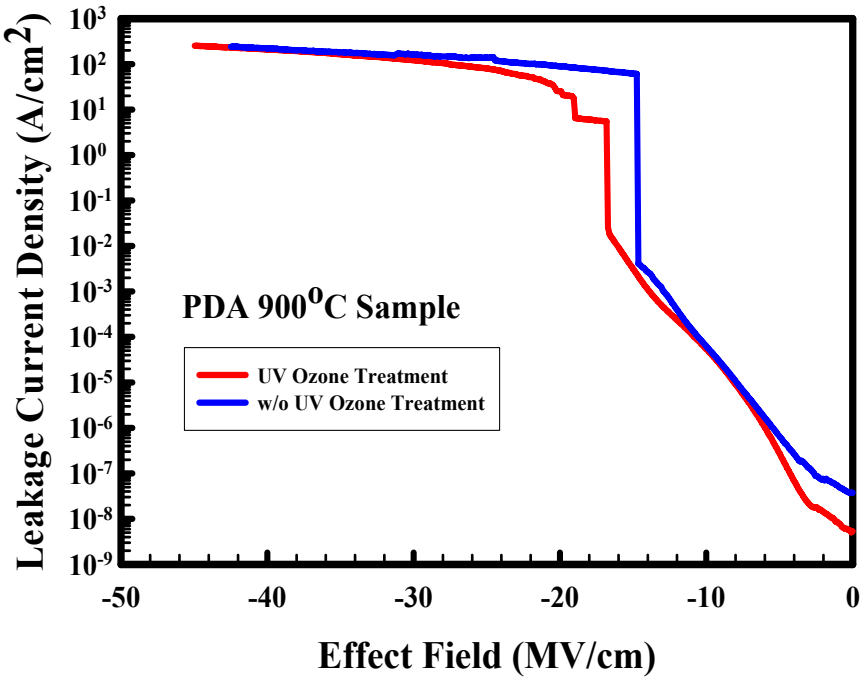


Figure 2-20 Compare with leakage current density of HfAlOxNy stacked gate dielectrics with PDA 900°C on UV ozone treatment samples and without zone treatment.

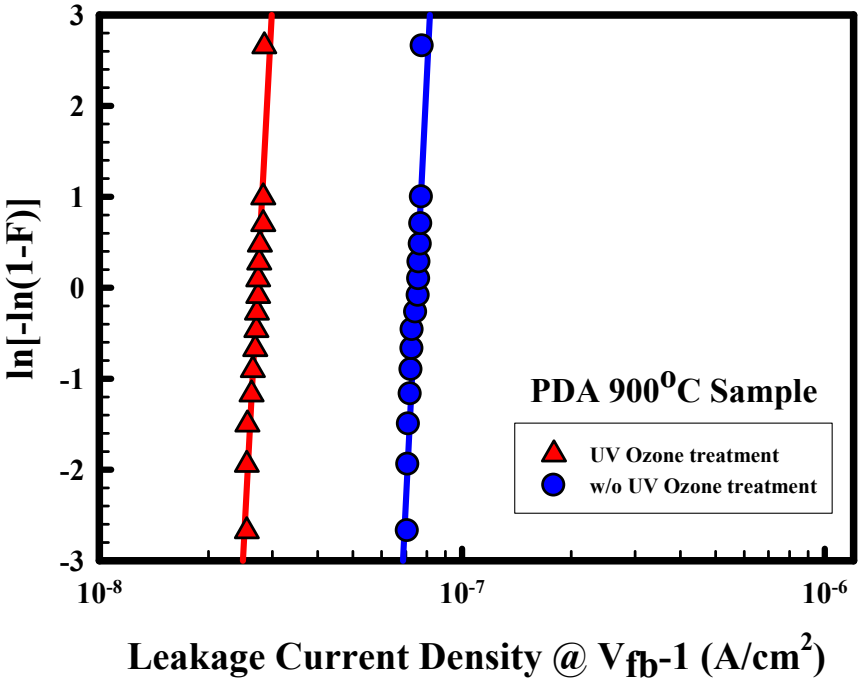


Figure 2-21 Leakage current density @ V_{fb}-1 distribution of HfAlOxNy stacked gate dielectrics with PDA 900°C on UV ozone treatment samples and without zone treatment.

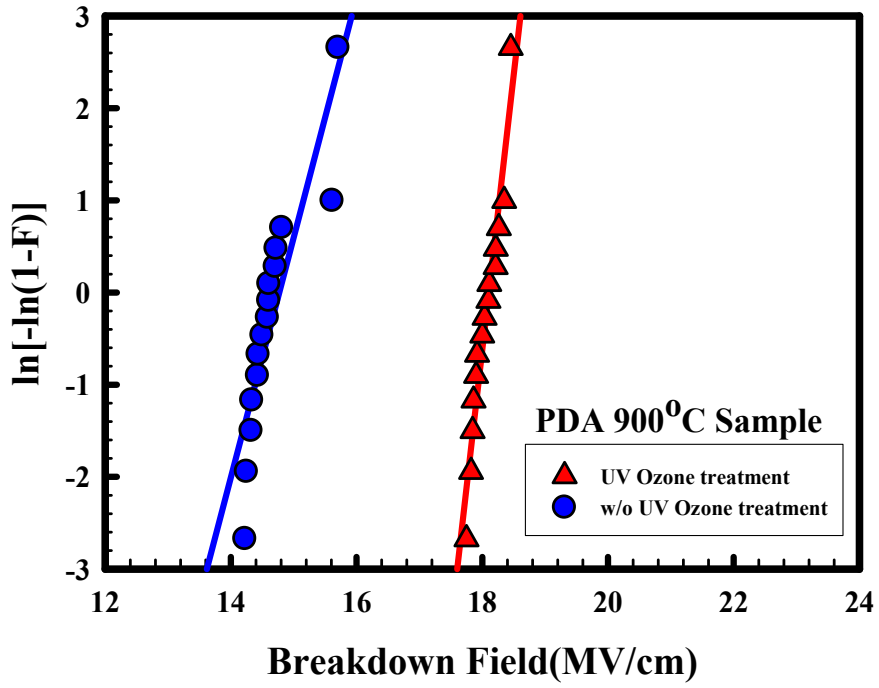


Figure 2-22 The time-zero dielectric breakdown (TZDB) of HfAlOxNy stacked gate dielectrics with PDA 900°C on UV ozone treatment samples and without zone treatment.

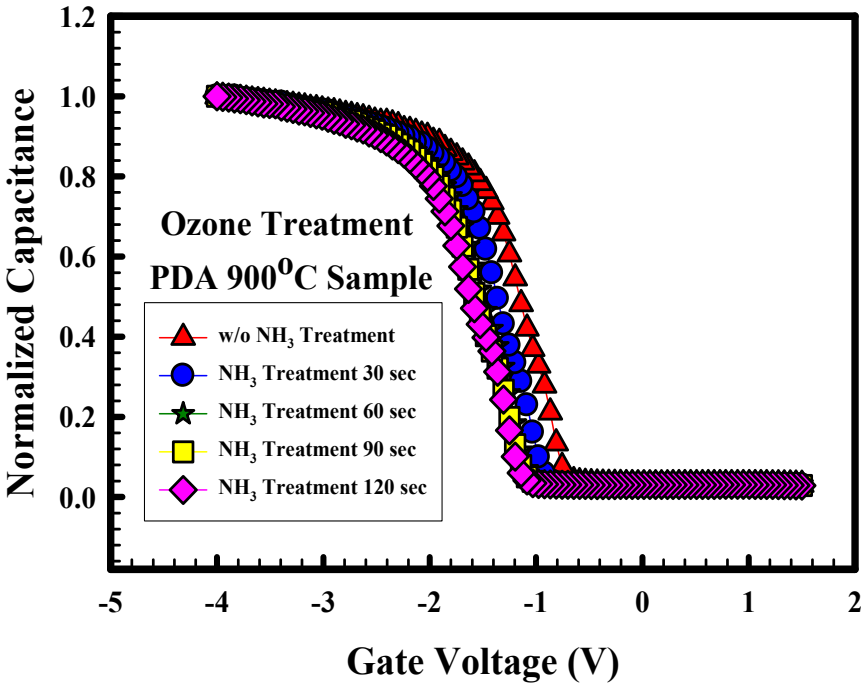


Figure 2-23 Normalized capacitance-voltage (*C-V*) characteristics of $HfAlO_xN_y$ gate dielectric PDA 900°C prior to ozone surface treatment follow various NH_3 plasma treatment's times.

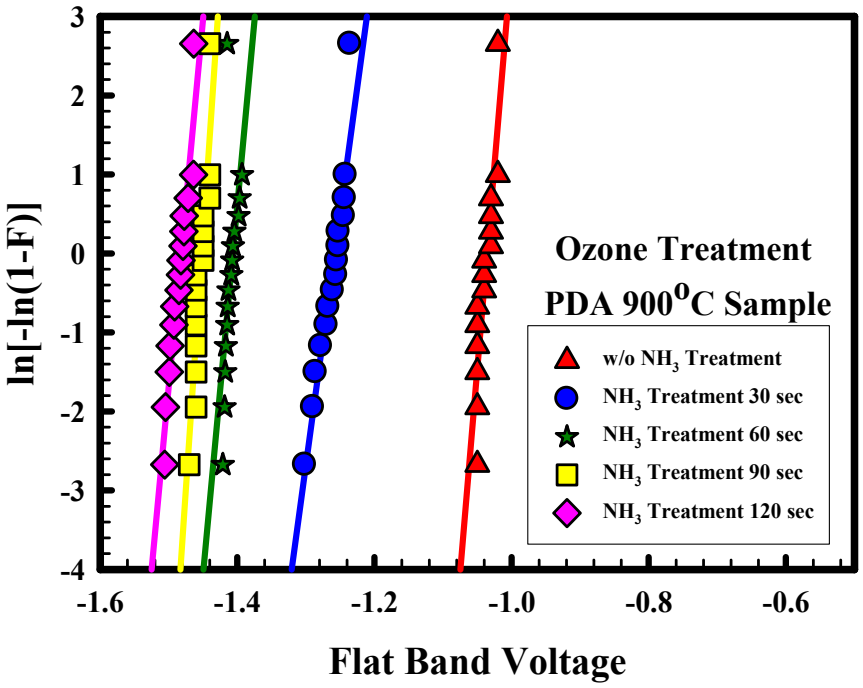


Figure 2-24 V_{fb} Weibull distribution of $HfAlO_xN_y$ gate dielectric PDA 900°C prior to ozone surface treatment follow various NH_3 plasma treatment's times.

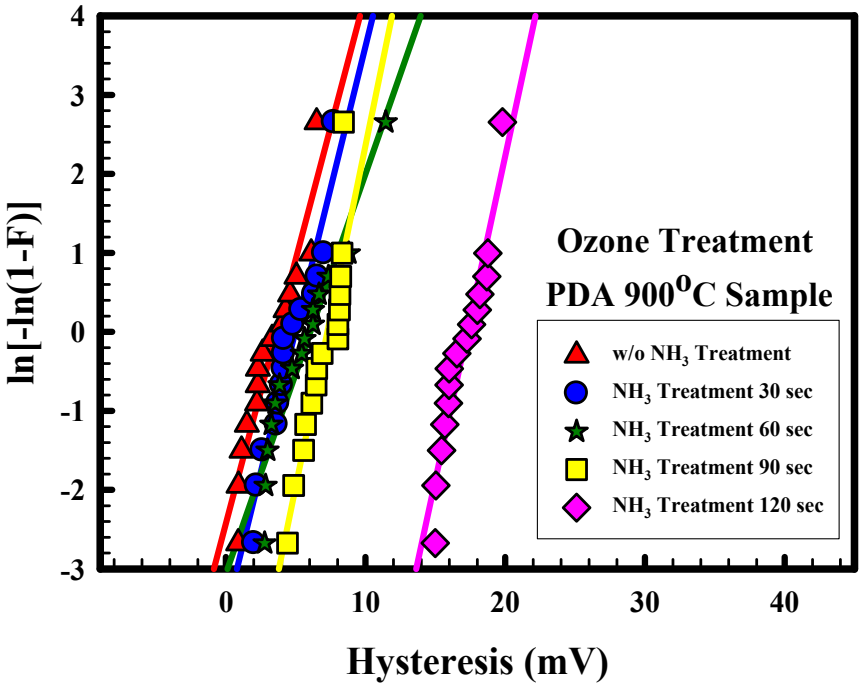


Figure 2-25 The hysteresis of of $HfAlO_xN_y$ gate dielectric PDA 900°C prior to ozone surface treatment follow various NH_3 plasma treatment's times.

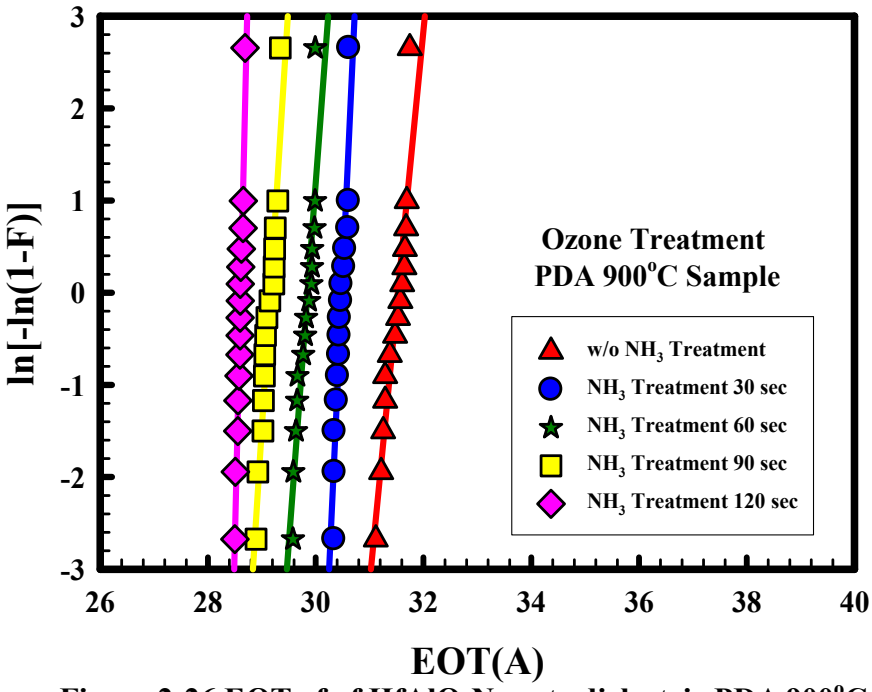


Figure 2-26 EOT of of $HfAlO_xN_y$ gate dielectric PDA 900°C prior to ozone surface treatment follow various NH_3 plasma treatment's times.

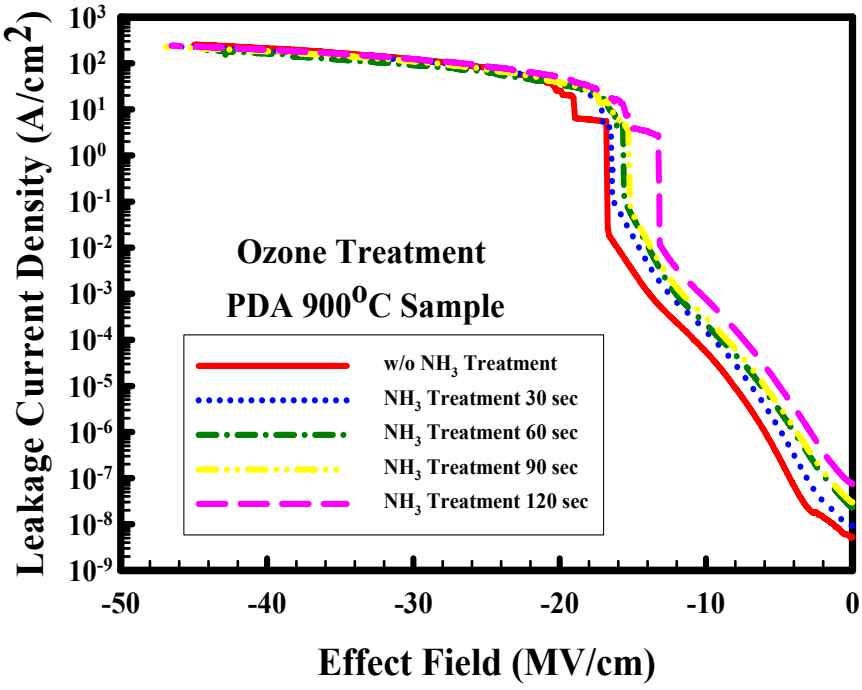


Figure 2-27 Leakage current density of of $HfAlO_xN_y$ gate dielectric PDA 900°C prior to ozone surface treatment follow various NH_3 plasma treatment's times

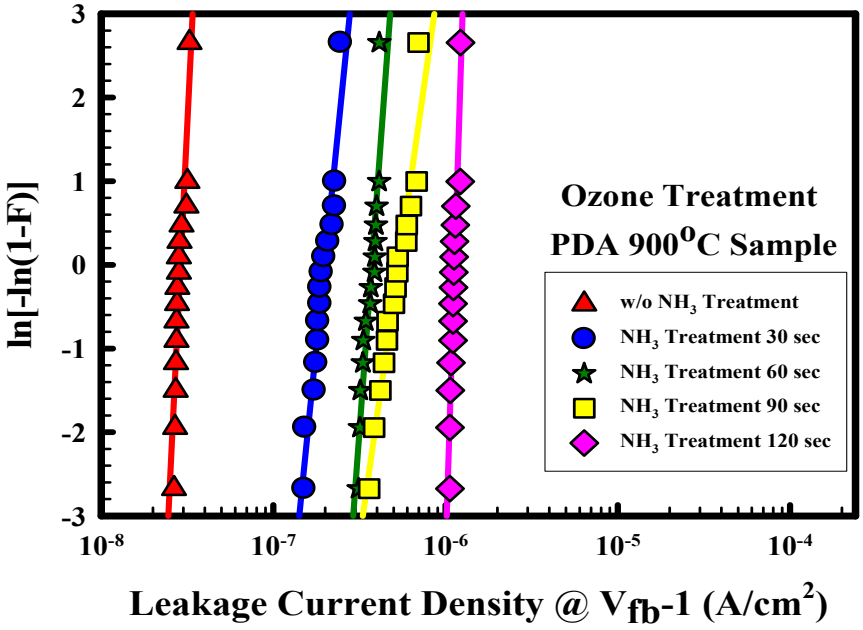


Figure 2-28 Leakage current density @ V_{fb}-1 distribution of of $HfAlO_xN_y$ gate dielectric PDA 900°C prior to ozone surface treatment follow various NH_3 plasma treatment's times.

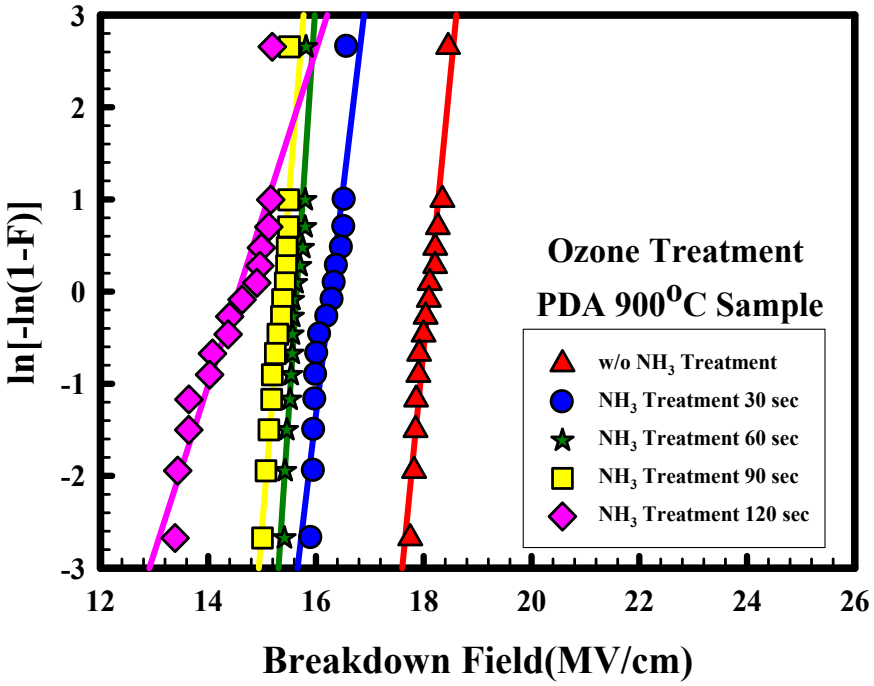


Figure 2-29 The time-zero dielectric breakdown (TZDB) of $HfAlO_xN_y$ gate dielectric PDA 900°C prior to ozone surface treatment follow various NH_3 plasma treatment's times

CHAPTER 3

$HfAlO_xN_y$ MOS FET Devices Characteristics

3.1Introduction

Unlike SiO2 films, high-k films are more susceptible to charge trapping. Charge trapping is arguable one of the most important issue in CMOS devices with high k gate dielectrics, because of the large amount of bulk traps present in the high k films [25]-[28]. The existence of bulk trap unavoidably causes many unwanted problems, such as reliability degradation [29], mobility degradation [30]-[34] and threshold voltage instability [35]-[44]. Charge pumping measurement is widely used to estimate interface state density in MOSFET devices. This measurement is very effective because it allows the exclusion of gate leakage contribution to the calculated interface state density presented in thin gate oxides.

Recently, reliability is an important issue in scaled MOSFET. During positive bias stress defects can be generated in the devices, which in turn cause threshold voltage shifts and device characteristics degradation. The device parameter variation can lead to circuit failures, both for analog and digital application.

In this work, we used optimum condition (UV ozone treatment and PDA 900^{o}C 30 seconds after high k film deposit) on chapter two to fabricate the nMOSFETs. A control sample (without treatment and PDA900^{o}C 30seconds after high k film deposit) was fabricate at the same time. In this chapter we compare to this two samples on electrical characteristic. We found that UV ozone treatment effectively improve the electrical characteristics, such interface state density, electric mobility, transconductance and ect. We investigate energy distribution of the interface traps in a

relatively large part of the forbidden energy gap on both sides of midgap by measuring the charge pumping currents (I_{cp}) with variable fall and rise times.

3.2 Experiment Details

In this thesis, field oxide was used for device isolation. MOS transistors was fabricated on 4-inch p-type Si with (1 0 0) orientation. After removing the native oxide, RCA clean was performed with HF-dip last, and immediately split into two groups. One is UV ozone treatment and the other is without UV ozone treatment. (UV ozone was used to grow an ultra-thin ozone oxide about 9~11Å (measured by N&K). After UV ozone surface treatments sample with a high temperature 900^{o}C 60seconds was used for density ozone oxide. On above step we called UV ozone treatment.) After surface treatment $HfAlO_xN_y$ was deposited at room temperature and 7.6E-3 torr by ion sputter system. Followed by a high temperature 900^{o}C post deposition annealing (PDA) in the nitrogen ambient for 30 seconds in order to improve the film quality. A 200nm undoped polycrystalline silicon (poly-Si) layer was directly deposited by low pressure chemical vapor deposition (LPCVD) on top of $HfAlO_xN_y$ films. After the gate electrode was patterned by lithography and etching processing. Then implant As 20 KeV dose 5E15 #/cm^2 after that activation was done at 950 ^{o}C by rapid thermal annealing (RTA) for 30seconds in the nitrogen ambient. After a 500nm

SiO_2 passivation was done by PECVD. Define the contact hole by the lithography and etching passivation SiO_2 and high k layer in order to silicon contact whit metal. Al was deposited by thermal evaporation system. Metal pad is defined by lithography and etching. Backside contact was formed by thermal evaporation. Figure 3-1 shown The cross section and the key process flow.

Current-voltage (*I-V*) and capacitance-voltage*(C-V*) characteristics were evaluated by an HP4156A precision semiconductor parameter analyzer and HP4284 LCR meter, respectively. The equivalent oxide thickness (EOT) of the gate dielectric was obtained from high frequency (100 KHz) capacitance-voltage (*C-V*) curve at strong inversion without considering quantum effect.

The hysteresis phenomenon was measured by sweeping the gate voltage from accumulation to inversion then back. Determine that by measurement V_t shift difference between forward and reverse.

In this thesis, the interface trap density (N_{it}) was analyzed using the charging pumping technique [3-18]. Square-wave waveforms (f = 1MHz) were applied to the gate by 811110A plus generator, and the base voltage was varied from accumulation to inversion, while keeping the pulse amplitude at 1.5V. Figure 3-2 shows the configuration of measurement setup used in our charge pumping experiment. A MOSFET with area A_G gives the charge pumping current as:

$$I_{cp} = qA_G fN_{it} \tag{3-1}$$

Interface trap density could be extracted from the above equation.

The total trap density increase, ΔN_{tot} which includes the increade of interface trap density and bulk trap density, was calculated from ΔV_{th} bv assuming that the charge was trapped at the interface between the dielectric and substrate.

$$\Delta N_{tot} = \frac{C\Delta V_{th}}{qA_G} \tag{3-2}$$

However, By measuring the charge pumping currents (I_{cp}) with variable fall and rise times, one can obtain the energy distribution of the interface traps in a relatively large part of the forbidden energy gap on both sides of midgap [3-19][3-20]. Therefore, interface traps act is donor-like or acceptor-like which depend on their relative state to the band gap. Relative position depends on its fermi level and an interface trap will be occupied by an electron or empty. Meanwhile, we listed some useful equations for analyzing whether acceptor like interface states or donor like interface states.

$$\frac{I_{cp}}{f} = 2qD_{it}A_G kT\left\{\ln\sqrt{t_r t_f} + \ln\left(\frac{|V_{fb}-V_t|}{|V_a|}V_{th}n_i\sqrt{\sigma_n\sigma_p}\right)\right\} \tag{3-3}$$

$$E_{em,e} - E_i = -kT\ln(V_{th}n_i\sigma_n\frac{|V_{fb}-V_t|}{|V_a|}t_f + e^{\frac{(Ei-Ef,inv)}{kT}}) \tag{3-4}$$

$$E_{em,h} - E_i = +kT\ln(V_{th}n_i\sigma_p\frac{|V_{fb}-V_t|}{|V_a|}t_r + e^{\frac{(-Ei-Ef,acc)}{kT}}) \tag{3-5}$$

$$N_{it}(E_2) = -\frac{t_f}{qA_G Tf}\frac{dI_{cp}}{dt_f} \qquad (t_r \text{ constant}) \tag{3-6}$$

$$N_{it}(E_1) = -\frac{t_r}{qA_G Tf}\frac{dI_{cp}}{dt_r} \qquad (t_f \text{ constant}) \qquad (3\text{-}7)$$

If we got the result that $N_{it}(E_2)$ was a large vibrations and $N_{it}(E_1)$ was almost similar according to equation (3-3), (3-4) and (3-6), We can observe that it existed strong fall time dependence of charge pumping curves for fixed rise time. This results of indicate acceptor like interface states existence because of huge interface state variation near conduction band. If we got the result that $N_{it}(E_1)$ was a large vibrations and $N_{it}(E_2)$ was almost similar according to equation (3-3), (3-5) and (3-7), We can observe that it existed strong rise time dependence of charge pumping curves for fixed fall time. This results of indicate donor like interface states existence because of huge interface state variation near valence band.

We consider an n-channel device of gate length L and width W Evaluate mobility by Spilt-CV technique. The effective mobility was measured at low drain voltage and then gave:

$$\mu_{\text{eff}} = \frac{g_d L}{W Q_n} \qquad (3\text{-}8)$$

where the drain conductance g_d is defined as:

$$g_d = \frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{GS}=constant} \qquad (3\text{-}9)$$

Q_n was measured from capacitance measurements. The capacitance meter was connected between the gate and the source-drain connected together with the substrate grounded. Therefore, Q_n was expressed as follows

$$Q_n = \int_{-\infty}^{V_{GS}} C_{gc} dV_g \tag{3-10}$$

And effective electric field produced by the gate voltage was express as:

$$E_{eff} = \frac{Q_b + \eta Q_n}{K_s \varepsilon_o} \tag{3-11}$$

Q_b was measured from capacitance measurements. The capacitance meter was connected between the gate and the substrate with the source-drain connected together grounded. Therefore

$$Q_b = \int_{Vfb}^{V_{GS}} C_{gb} dV_g \tag{3-12}$$

where Q_b and Q_n were charge density in depletion layer and inversion layer, respectively. The parameter η =1/2 was for electron mobility. And subsequently universal mobility was accomplished by this equation.

$$\mu_{eff} = \frac{638}{1 + \left(\frac{\varepsilon_{eff}}{area} \right)^{1.69}} \tag{3-13}$$

Above all equations, we easily can extract all of the data what we need. Figure 3-3 represents the configuration of split-CV measurement setup.

3.3 Results and Discussion

3.3.1 Basic electrical Properties Of Devices

Figure 3-4 shows the drain current (I_d) versus the drain voltage (V_d)

characteristic for UV ozone surface treatment is solid line and without surface treatment is dotted line. The drain current is larger for the UV ozone surface treatment. Figure 3-5 shows high frequency (100 kHz) C-V characteristic of the $HfAlO_xN_y$ stacks. First, we can see that the EOT value obtained from strong inversion region are around 20Å and 20.2Å for samples with and without UV ozone treatment, respectively. Figure 3-6 shows the cumulative probability of the threshold voltage (V_{th}) for the fabricated devices. Figure 3-7 (a),(b) and Figure 3-8 (a),(b) shows the drain current (I_d) versus the gate voltage (V_g) and hysteresis characteristics of nMOSFETs with and without UV ozone treatment. Samples of UV ozone treatment and without threshold voltage are 0.547V and 1.14V, respectively. We can see that the substhreshold swing (S.S.) can be improved from 114.13 mV/decade to 82.9 mV/decade and hysteresis also be improved from 24.5 mV to 0.763 mV. Whit the UV ozone treatment, EOT is 0.2Å thicker than the control sample, so based on equation (3-14), we redraw transconductance characteristics, shows in Figure 3-9. Form Figure 3-9 observe that normalized transconductance peak value has roughly gained 1.85 times as compared to control sample.

$$G_m = \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{W \mu_n C_{ox}}{L}(V_{gs} - V_t) \qquad (3\text{-}14)$$

We consider an n-channel device of gate length L and width W Evaluate mobility by Spilt-CV technique. Figure 3-10 means electron mobility with UV ozone surface and with treatment measured by split-CV method. Using split-CV wouldn't calculate short channel device because of large disturbance when we measure. Therefore, we only can measure large dimension device. Form the mobility we can find that UV ozone treatment improved mobility about 1.32 times.

Leakage current density of $HfAlO_xN_y$ stacked gate dielectrics with UV ozone treatment and without treatment that is compared shows in Figure 3-11. From leakage density revealed that UV ozone surface treatment can further improve the dielectric properties.

3.3.2 Charge Pumping Measurements Of HfAlOxNy stacks nMOSFETs Devices

Charge pumping measurement is used to further understand nMOSFET characteristics on interface density and distribution of the interface traps. If is well known that the charge pumping measurement is used to quantify the interface density by monitoring the substrate current. Interface state density was measured using the fixed amplitude sweep for the nMOSFETs with and without UV ozone surface treatment as function of the peak voltage.

The results are shown in Figure 3-12(a), (b). It can be seen that the Icp and |Id+Is| reduce on the UV ozone treatment. Indicate that, interface state density reduce at UV ozone treatment. We can see that the interface state density can be improved from $1.23*10^{12}$ /cm^2 to $3.65*10^{11}$ /cm^2. Therefore, we UV ozone surface treatment can improve the interface state.

Besides, understanding interface state is important because it will affect carrier mobility. By measuring the charge pumping currents (I_{cp}) with variable fall and rise times, one can obtain the energy distribution of the interface traps in a relatively large part of the forbidden energy gap on both sides of midgap. Figure 2-13(a)(b) shows the UV ozone treatment result which tells us strong fall-time dependence of charge pumping current for fixed rise time. This also means that acceptor-like interface stats

exist on UV ozone surface treatment for $HfAlO_xN_y$ stacks nMOSFETs. The same result at without UV ozone treatment sample is shown in Figure 2-14 (a),(b). Without treatment result which tells us strong fall-time dependence of charge pumping current for fixed rise time. This also means that acceptor-like interface stats exist on without treatment for $HfAlO_xN_y$ stacks nMOSFETs.

3.3.2 Constant Voltagee Stress

The transistor I_d-V_g curves and charge pumping were measured for monitoring the threshold voltage shift ($\triangle V_{thc}$) and delta interface state density during constant voltage stress intervals. The stress conditions are (V_{CVS}=V_g-V_{thc}) of 0.5~2V for the devices with and without UV ozone treatments. V_{thc} is define as follow:

$$Vthc \equiv \frac{W}{L} \times 5e^{-8} \tag{3-15}$$

Moreover, the total trap density which consists of interface trap density and bulk trap density is calculated from threshold voltage shift before and after stress. It expresses as follow:

$$\Delta N_{total} = \frac{C\Delta V_{thc}}{qA_G} \tag{3-16}$$

And bulk trap density also can be calculated as follows:

$$\Delta N_{bulk} = \Delta N_{total} - \Delta N_{it} \tag{3-17}$$

Figure 3-15 shows basic measurement method for CVS.

Figure 3-16 shows the delta V_{thc} versus stress time for device with and without UV ozone treatment. Indicate that, UV ozone treatment can improve the shift amount of V_{thc}. Figure 3-17 shows the interface state density versus the stress time. Delta

interface state reduce was observed by UV ozone treatment. Therefore, we proved that UV ozone surface treatment can improve interface quality. Figure 3-18 shows the delta total charge density with UV ozone treatment and without by equation (3-16). From the delta N_{total} we can find the N_{bulk} by equation (3-17) as function shows in Figure 3-19. From the Figure 3-18 and Figure 3-19 we see that use the UV ozone treatment effectively reduce the delta N_{total} and N_{bulk}. For this reason we believe that electrical characteristics is improved by UV ozone treatment, so UV ozone surface treatment is good candidate for prior the $HfAlO_xN_y$ deposition.

From the equation (3-17), we know the delta total charge composed of the delta interface charge and delta bulk charge. We also know that total charge is a function with V_{thc} shown in equation (3-16). Therefore, threshold voltage shift is a function and composed of the delta interface charge and delta bulk charge. Figure 3-20 shows the interface charge density, bulk charge density and total charge density versus the stress times with UV ozone treatment. Form we observe that the delta bulk charge density dominate the delta total charge. Therefore, we can say that bulk charge major factor to effect the threshold voltage shift with UV ozone treatment. Figure 3-21 shows the interface charge density, bulk charge density and total charge density versus the stress times without treatment. The same result was observed in here. Therefore, we can say that bulk charge major factor to effect the threshold voltage shift on the control sample.

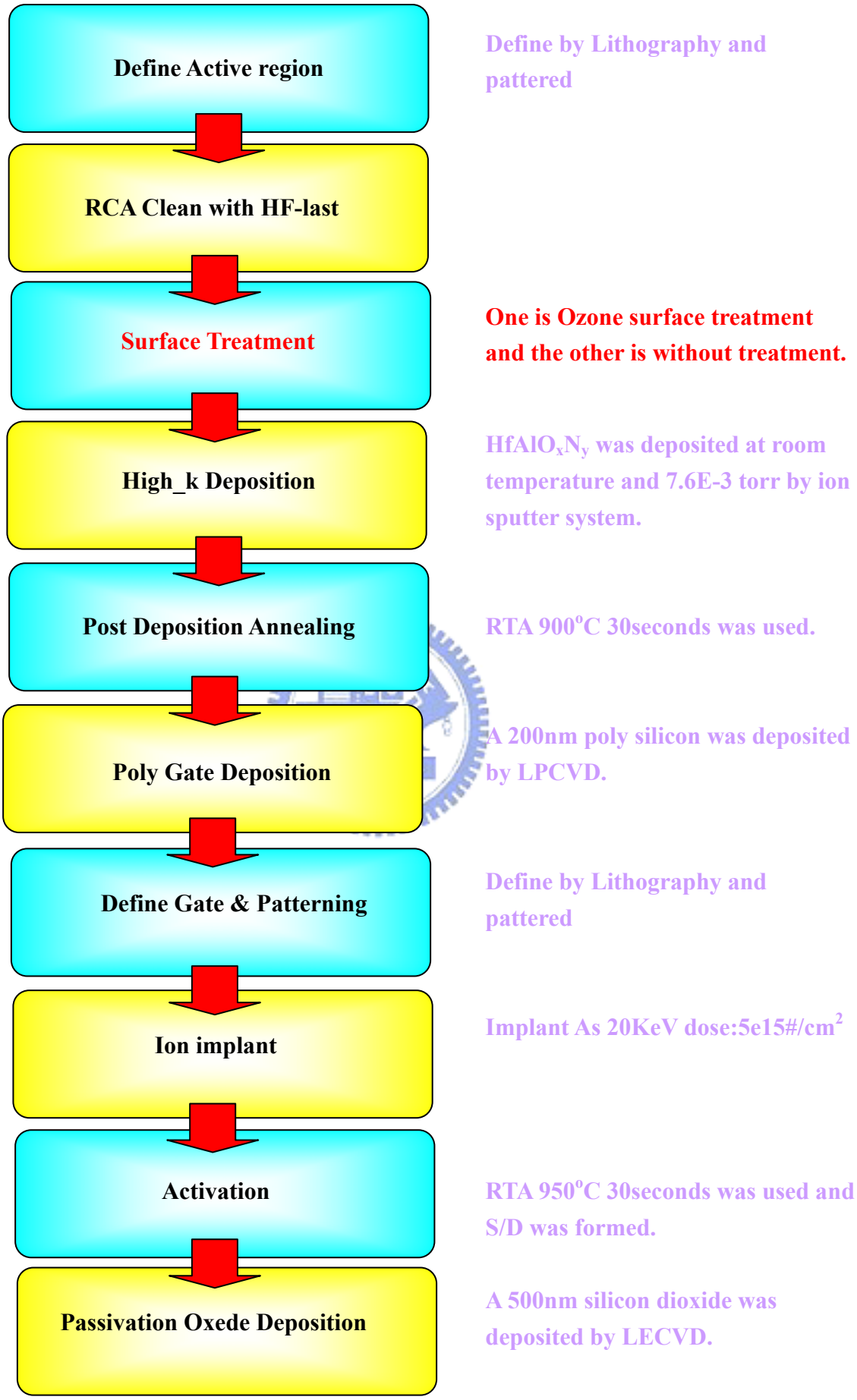
3.4 Summary

In this work, we used optimum condition (UV ozone treatment and PDA 900^{o}C

30 seconds after high k film deposit) on chapter two to fabricate the nMOSFETs and a control sample (without treatment and PDA900^{o}C 30seconds after high k film deposit) was fabricated at the same time. Basic electrical characteristics were compared with UV ozone treatment and without. Form the electrical characteristics, we observe that use UV ozone treatment improve the substhreshold swing (S.S.), hysteresis , Leakage current, mobility, transconductor Gm and interface state density N_{it} shows in table A. From the table A we can observe that improved electrical characteristics on red region in the Table 3-1.

We determine the energy distribution of the interface traps in a relatively large part of the forbidden energy gap on both sides of midgap by measuring the charge pumping currents (I_{cp}) with variable fall and rise times. By the result which tells us strong fall-time dependence of charge pumping current for fixed rise time. This also means that acceptor-like interface stats exist on with UV ozone treatment and treatment for $HfAlO_xN_y$ stacks nMOSFETs.

Then we estimate reliability of the $HfAlO_xN_y$ stacks nMOSFETs by constant voltage stress (CVS). We find that UV ozone surface treatment can improved delta interface state density and bulk charge trap density during the constant voltage stress compared with the control sample. Final, we find the bulk charge density to dominate the threshold voltage shift during the constant voltage stress for with UV ozone treatment and without.


Define Active region
Define by Lithography and pattered
RCA Clean with HF-last
Surface Treatment
One is Ozone surface treatment and the other is without treatment.
High_k Deposition
HfAlO$_x$N$_y$ was deposited at room temperature and 7.6E-3 torr by ion sputter system.
Post Deposition Annealing
RTA 900°C 30seconds was used.
Poly Gate Deposition
A 200nm poly silicon was deposited by LPCVD.
Define Gate & Patterning
Define by Lithography and pattered
Ion implant
Implant As 20KeV dose:5e15#/cm^2
Activation
RTA 950°C 30seconds was used and S/D was formed.
Passivation Oxede Deposition
A 500nm silicon dioxide was deposited by LECVD.

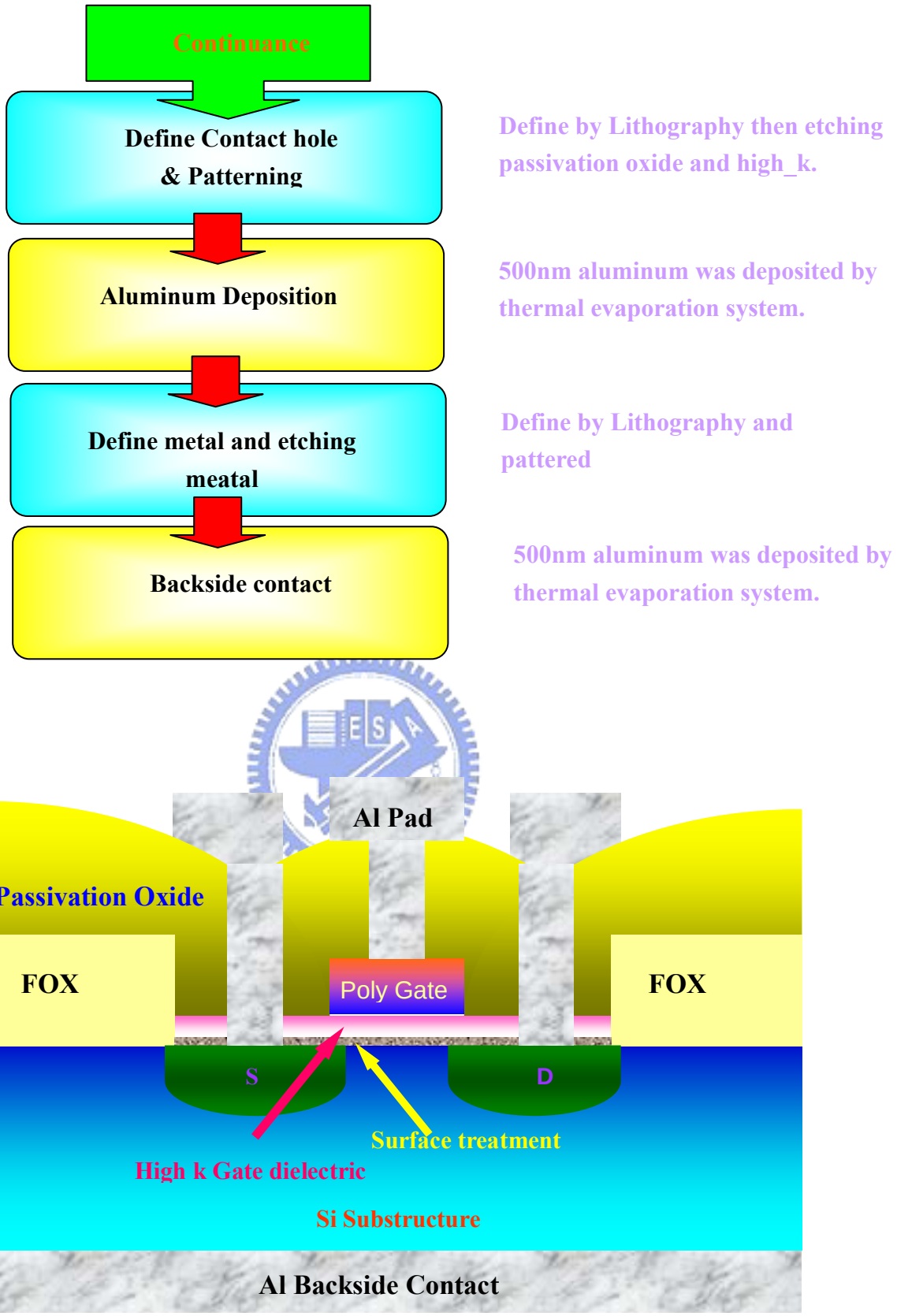


Figure 3-1 The cross section and the key process flow of nMOS transistor.

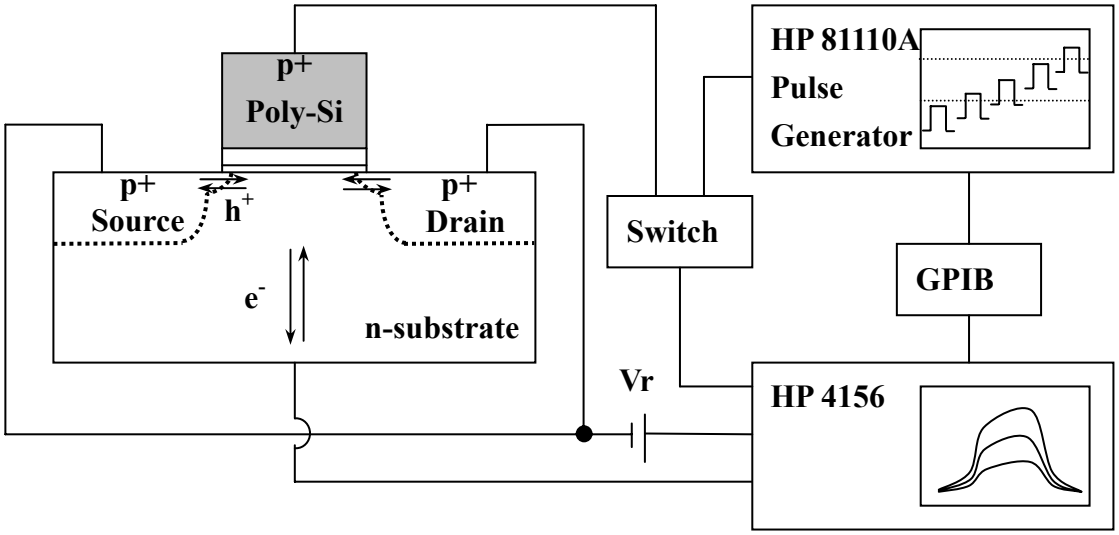
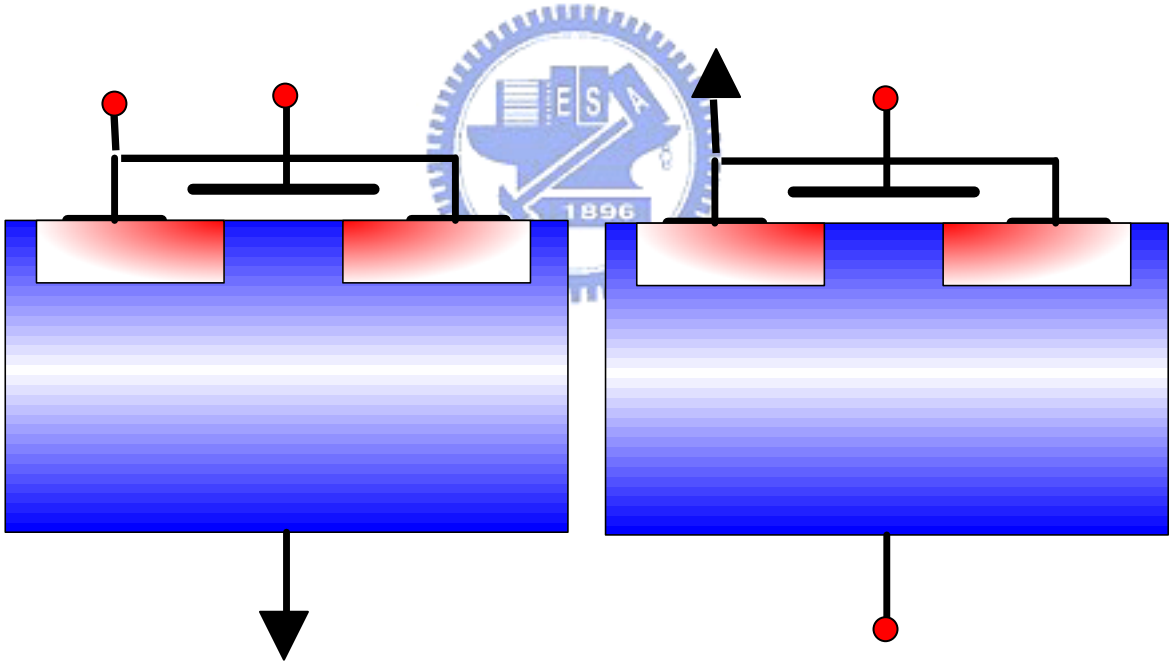


Figure 3-2 Basic experimental setup of charge pumping measurement.



a **b**

Figure 3-3 Configuration for (a) gate-to-channel, (b) gate-to-substrate capacitance measurements.

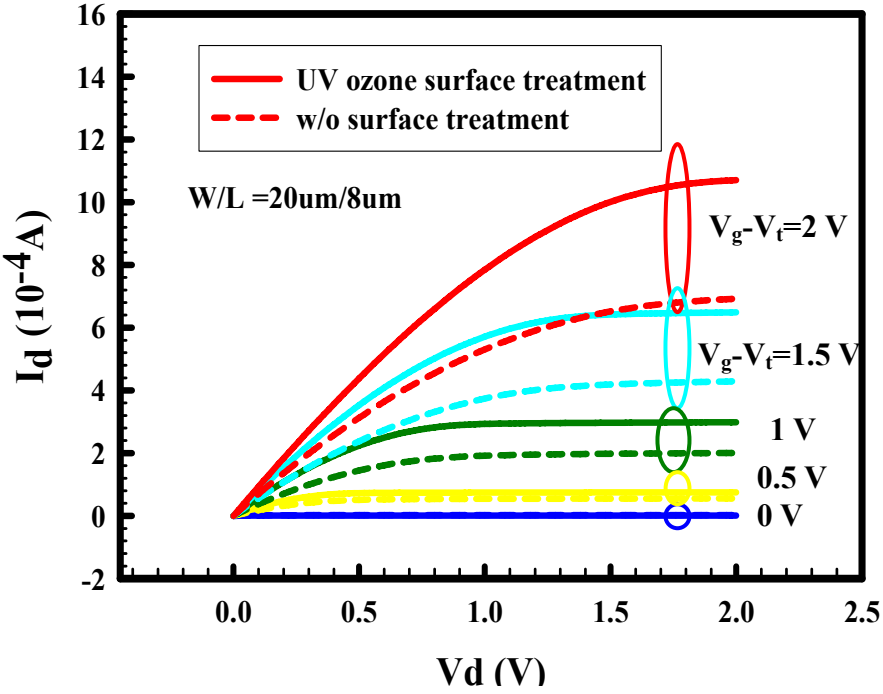


Figure 3-4 I_d vs V_d characteristics of UV ozone surface treatment and without treatment V_G-V_{th}= 0 ~ 2 V, step= 0.5 V, W/L=20 μm/8μm.

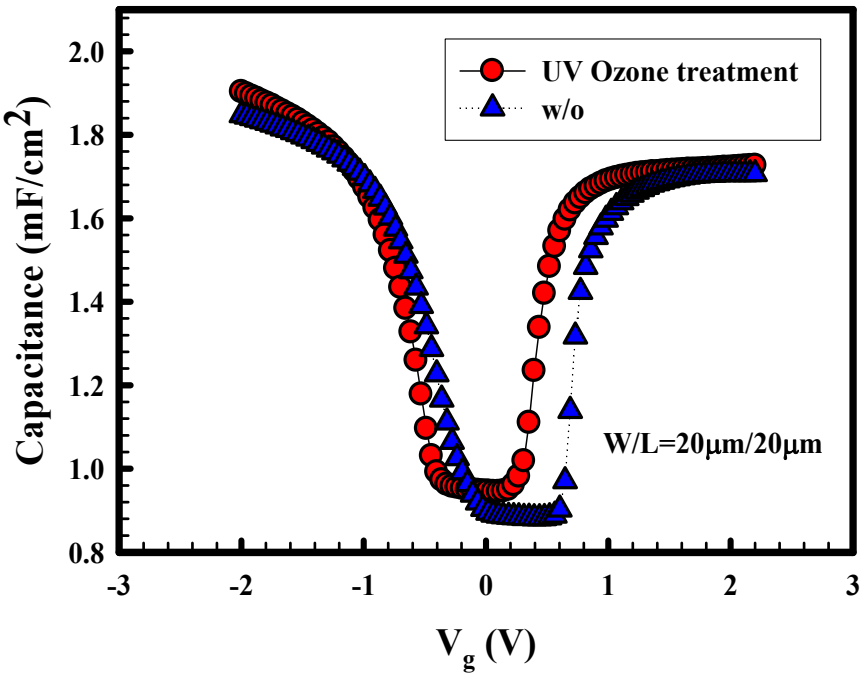


Figure 3-5 High frequency (100 kHz) C-V characteristic of the $HfAlO_xN_y$ stacks. EOT are 20 and 20.2 for with and without UV ozone treatment, respective.

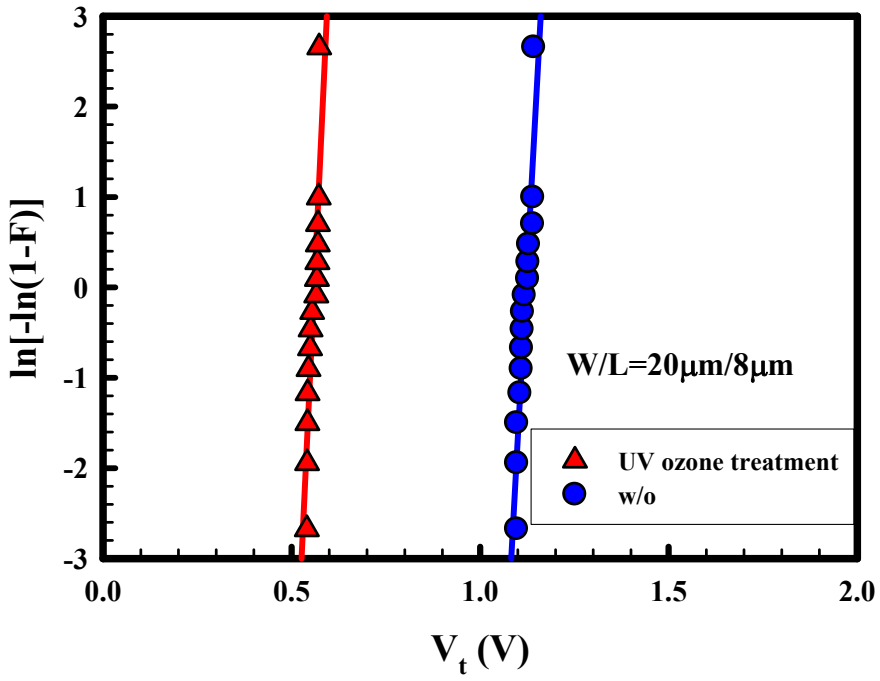
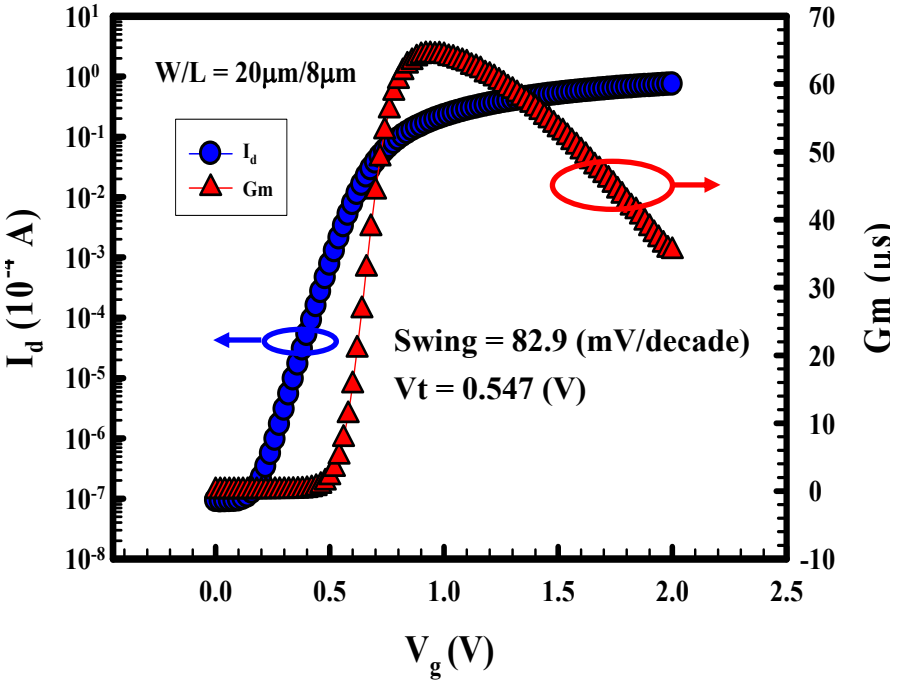
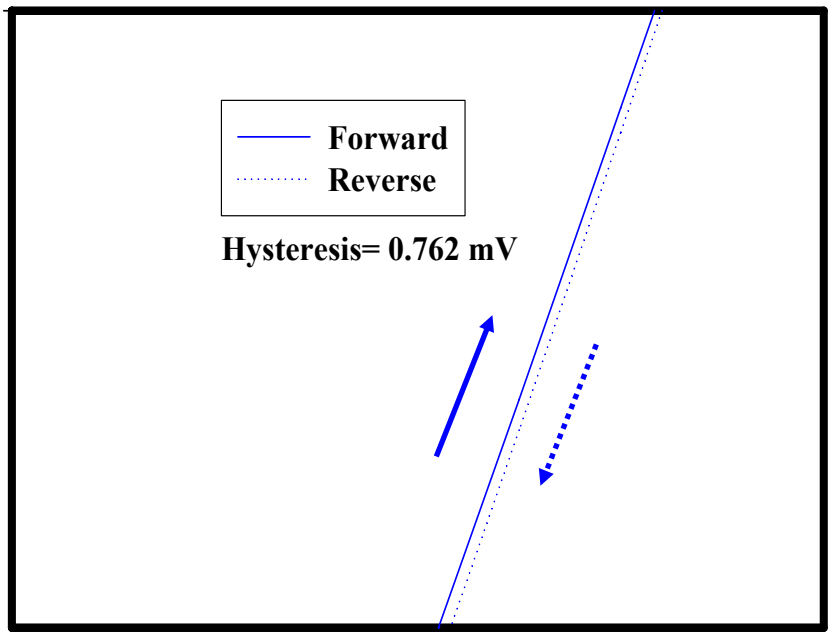


Figure 3-6 Cumulative probability of the threshold (V_{th}) for $HfAlO_xN_y$ stacks nMOSFETs.

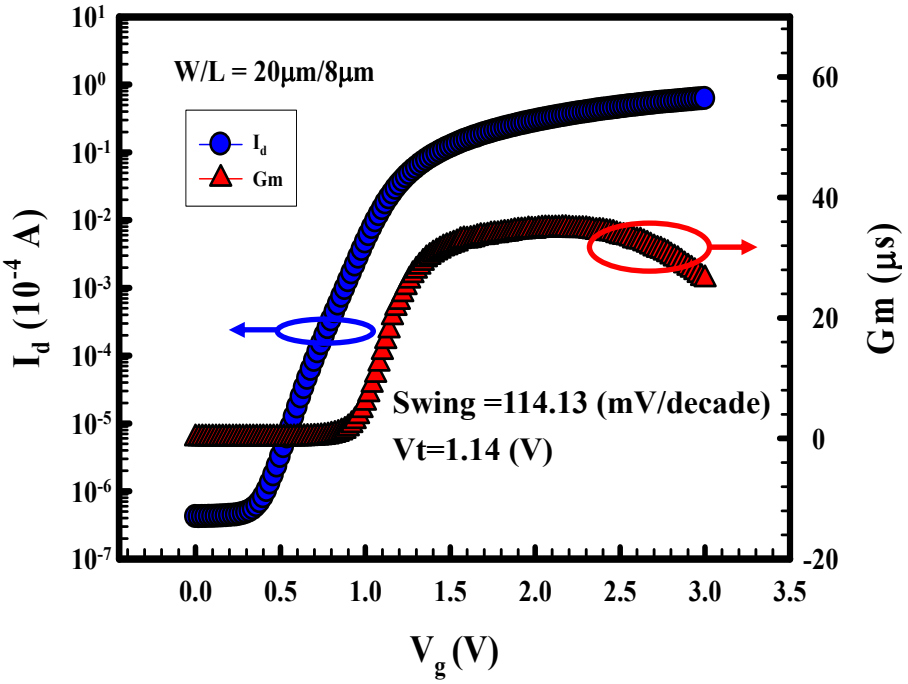


(a)

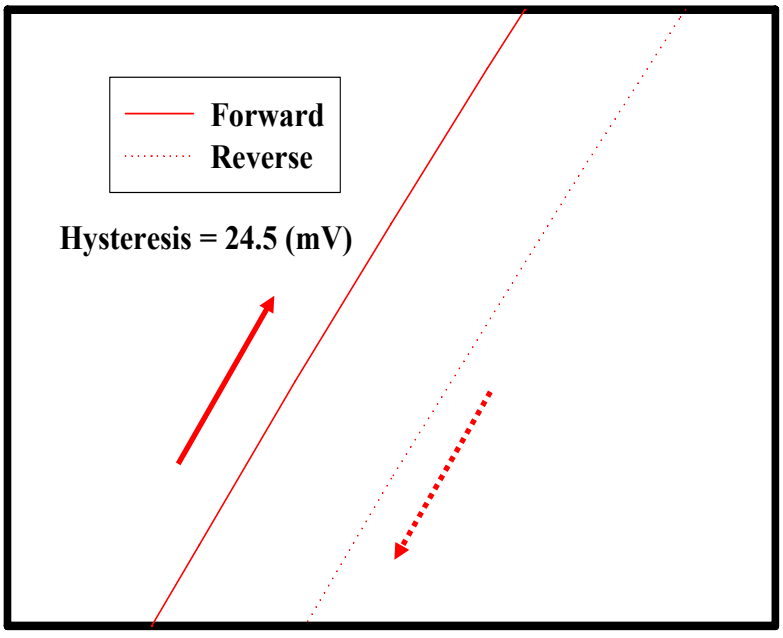


(b)

Figure 3-7 (a) Id vs Vg, (b) Hystersis of nMOSFET characteristics with UV ozone treatment.



(a)



(b)

Figure 3-8 (a) Id vs Vg, (b) Hystersis of nMOSFET characteristics without UV ozone treatment.

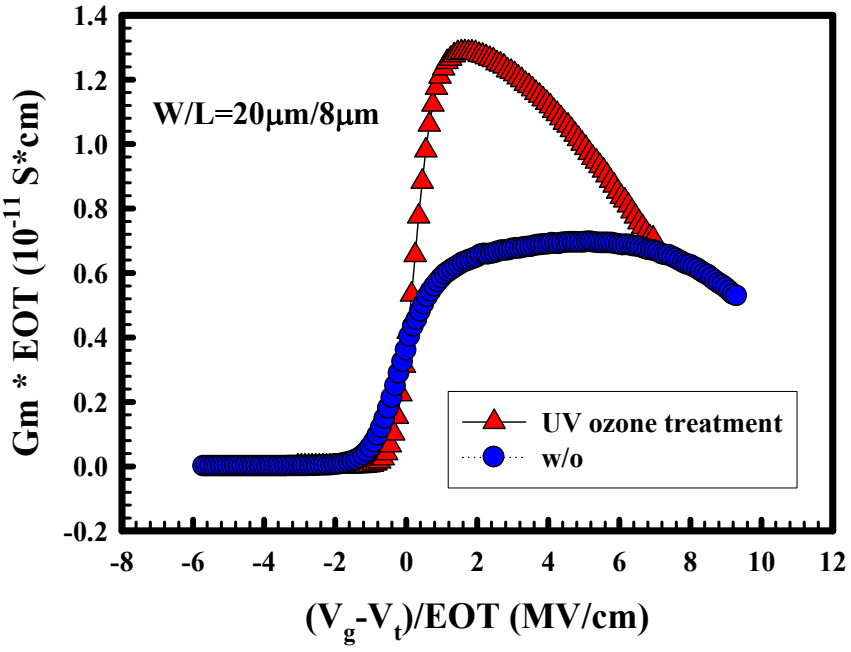


Figure 3-9 Normalized transconductance characteristic of nMOSFET with $HfAlO_xN_y$ stacks.

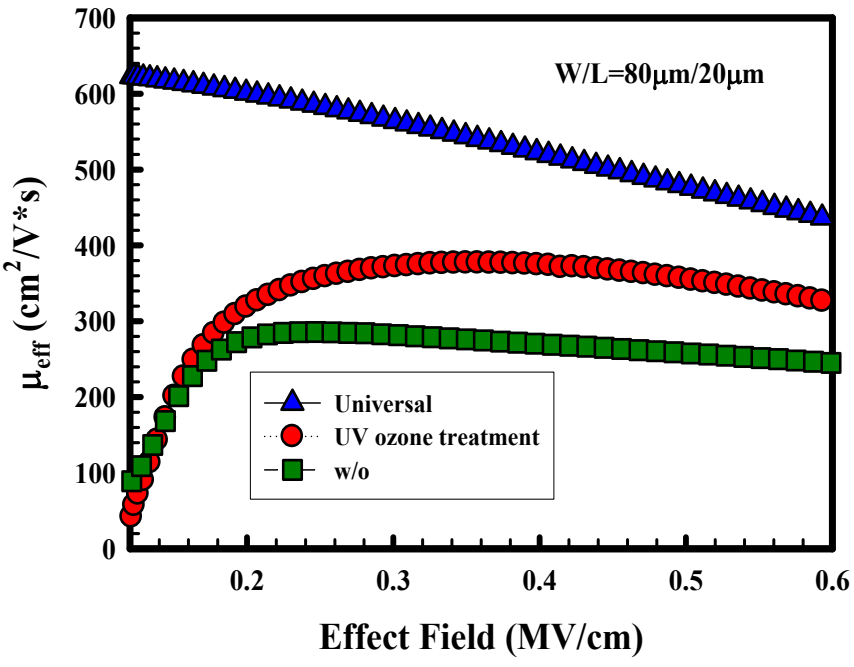


Figure 3-10 Mobility characteristic of nMOSFET with $HfAlO_xN_y$ stacks.

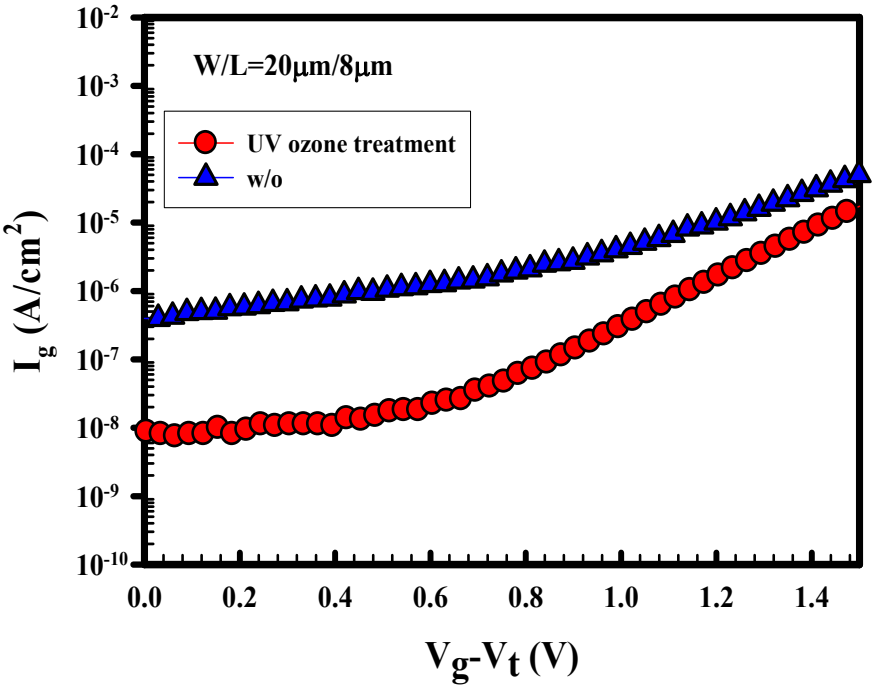
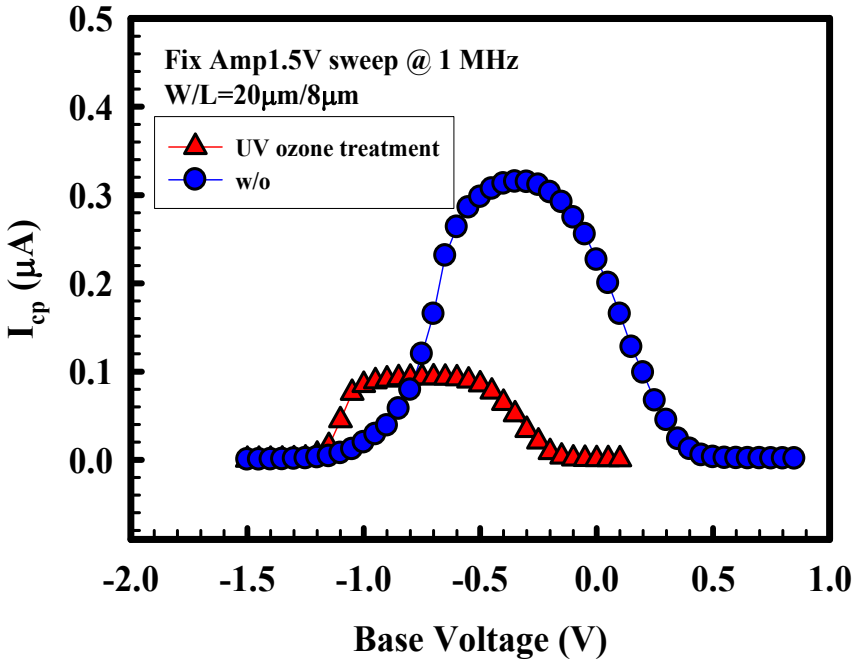
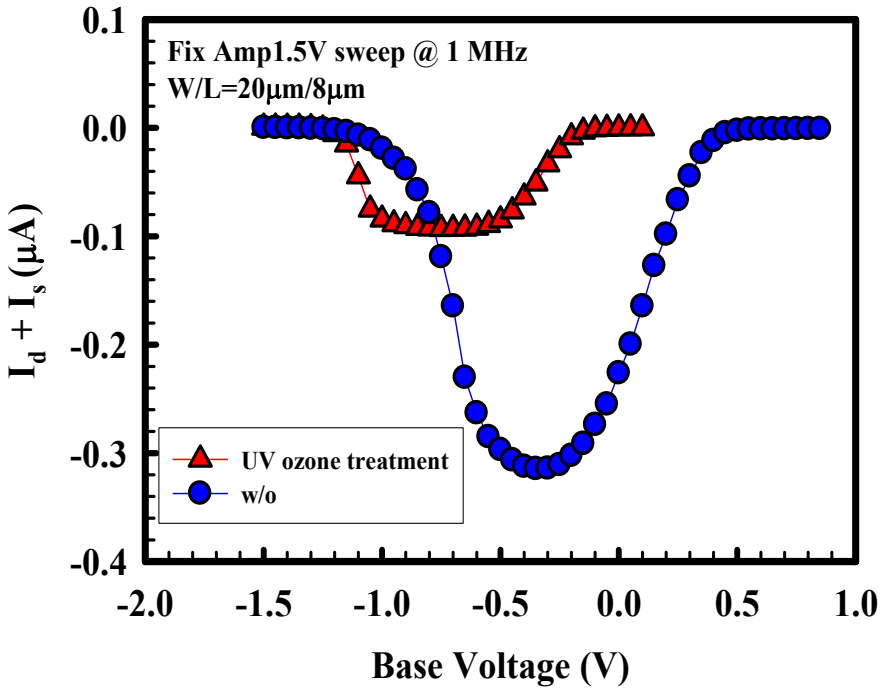


Figure 3-11 Leakage current density of nMOSFET with $HfAlO_xN_y$ stacks.

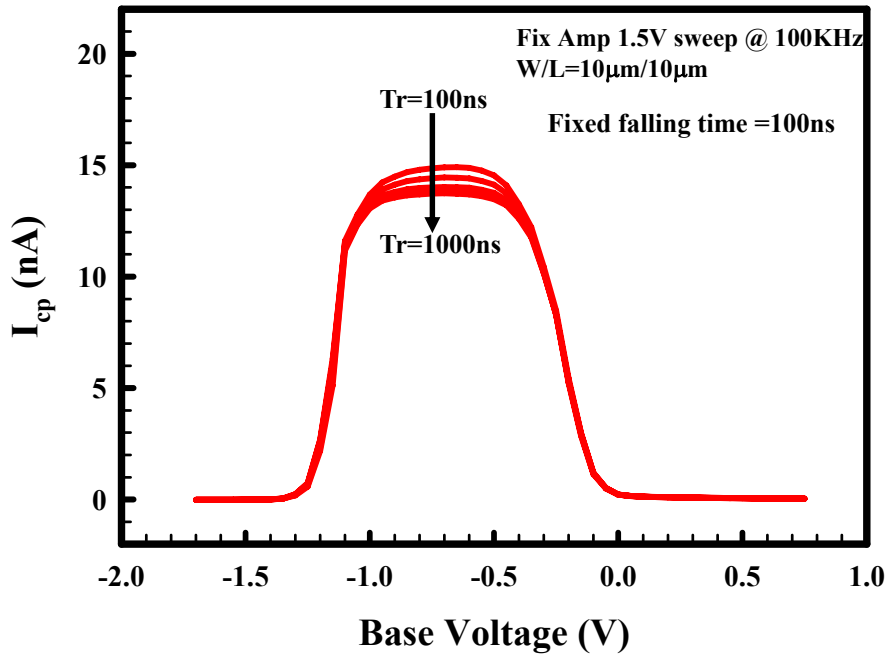


(a)

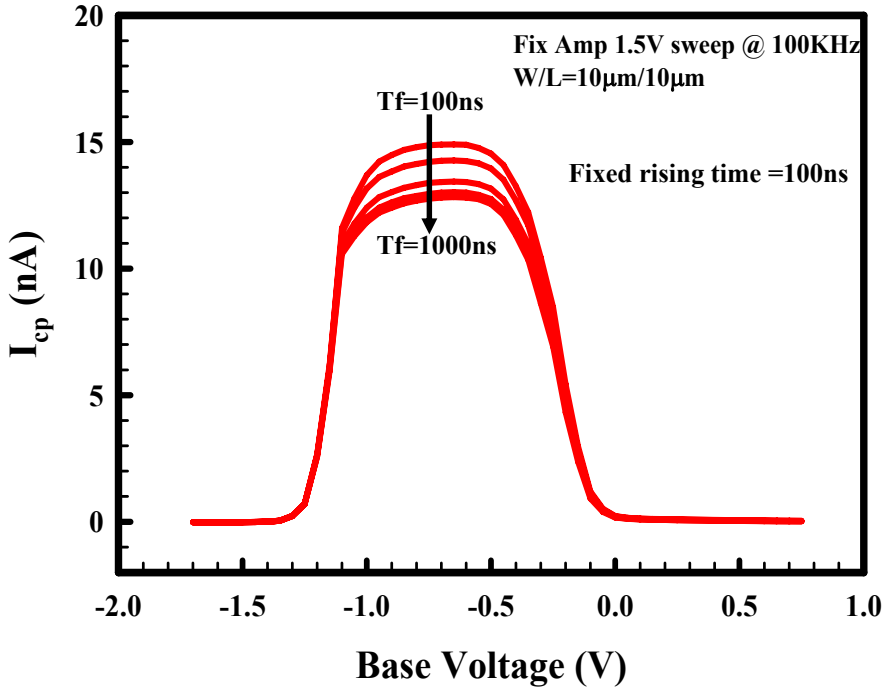


(b)

Figure 3-12 Charge pumping measurement (a)I_{cp} (b)I_d+I_s

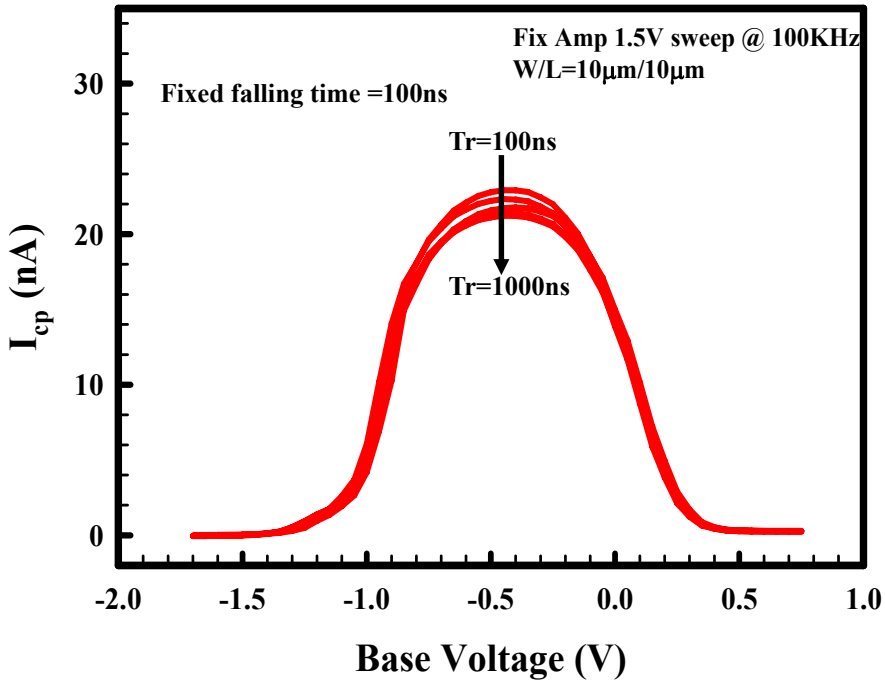


(a)

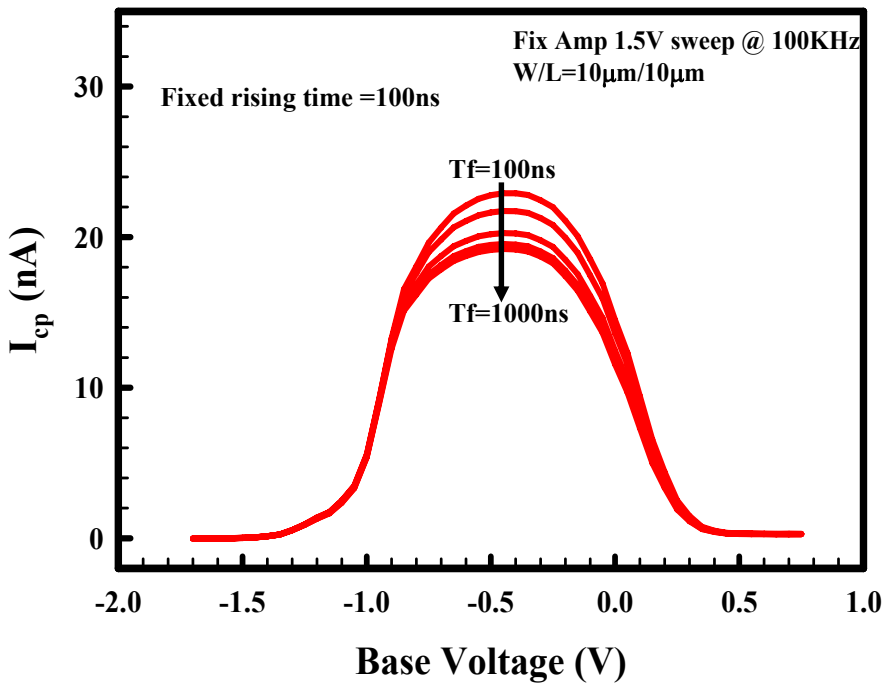


(b)

Figure 3-13 (a)Weak rise-time dependence of charge pumping current for fixed fall time. (b)Strong fall-time dependence of charge pumping current for fixed rise time on UV ozone treatment sample.



(a)



(b)

Figure 3-13 (a)Weak rise-time dependence of charge pumping current for fixed fall time. (b)Strong fall-time dependence of charge pumping current for fixed rise time. On control sample.

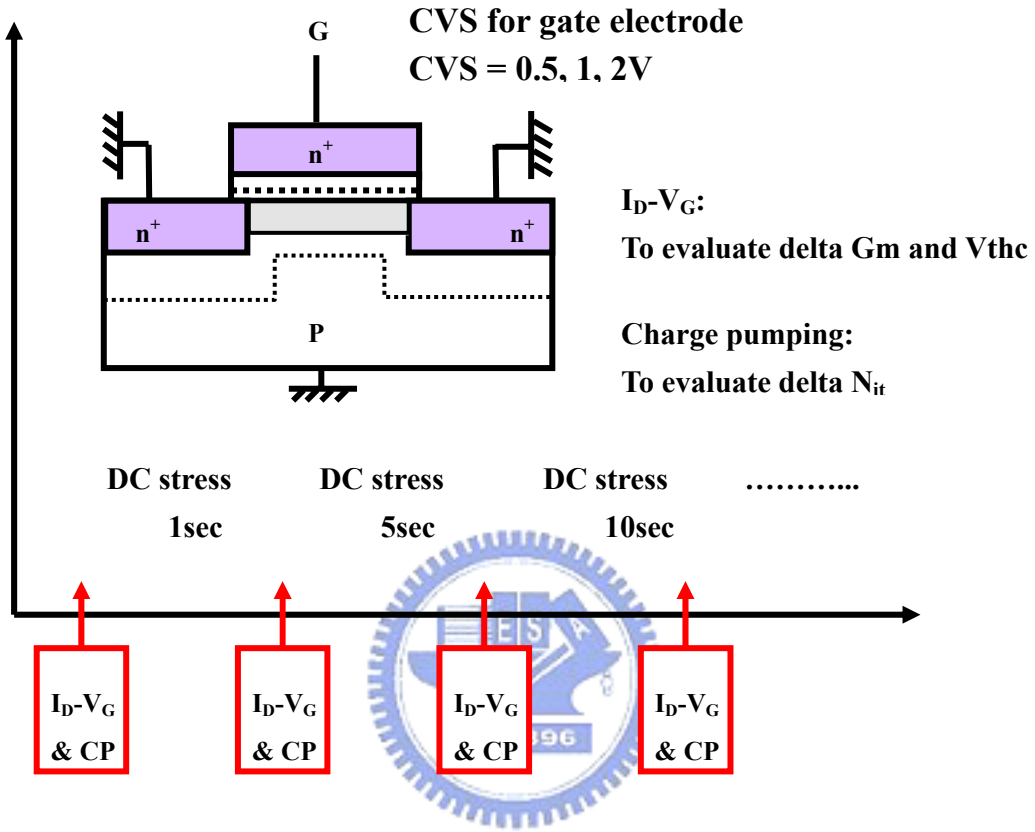


Figure 3-15 Basic measurement method for CVS.

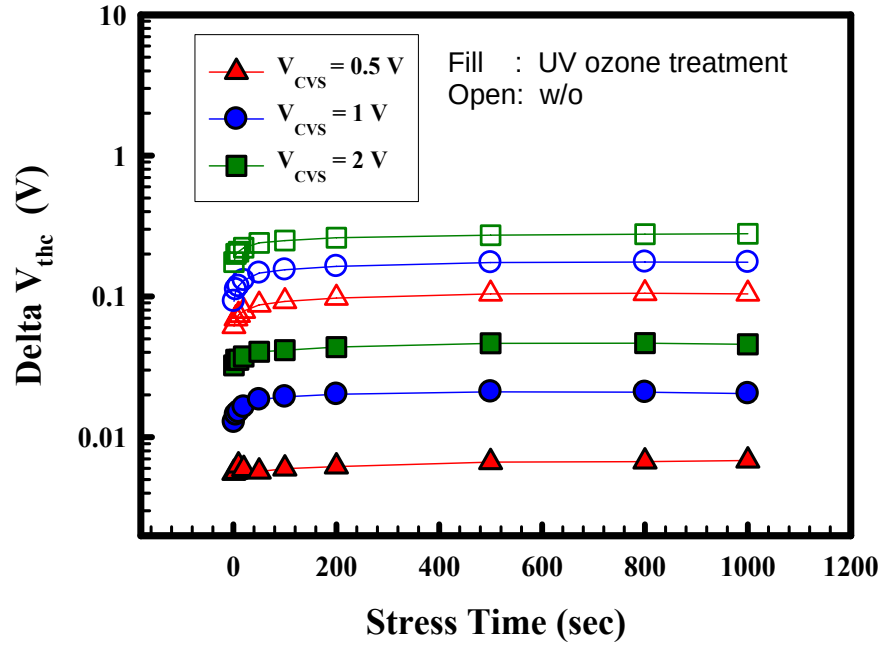


Figure 3-16 Delta V_{thc} versus stress time for device with and without UV ozone treatment.

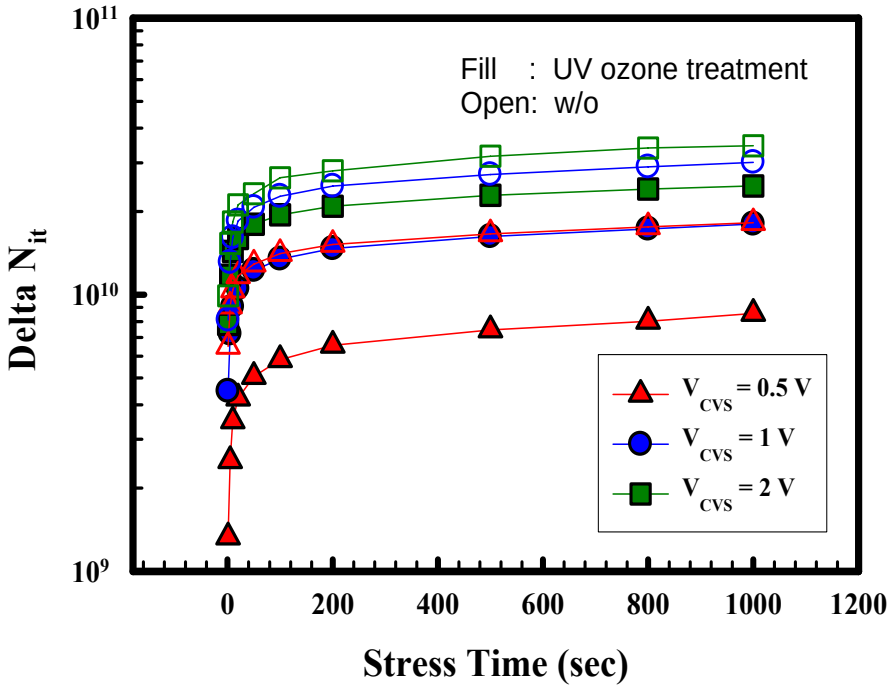


Figure 3-17 Delta N_{it} versus stress time for device with and without UV ozone treatment.

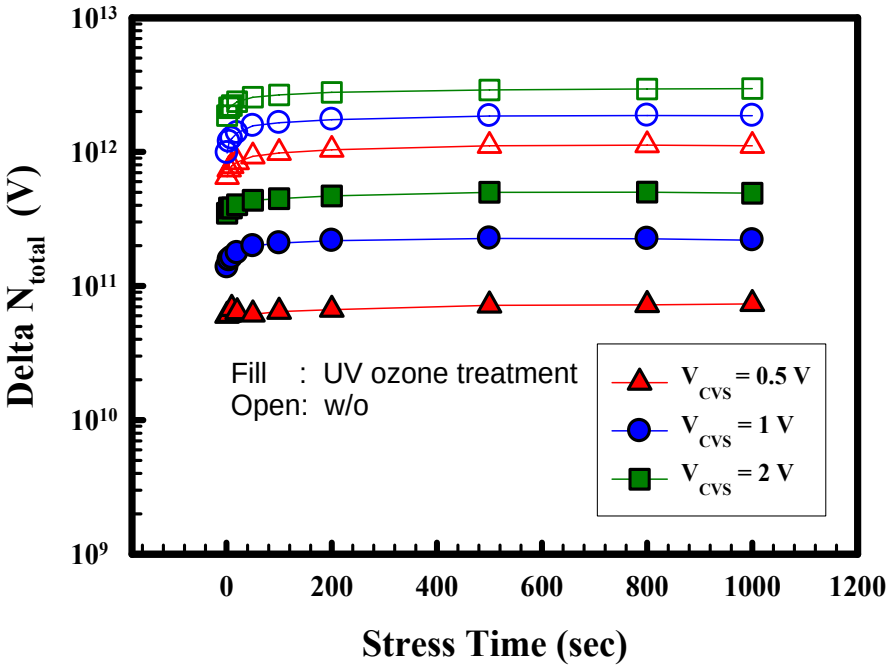


Figure 3-18 Delta N_{total} versus stress time for device with and without UV ozone treatment.

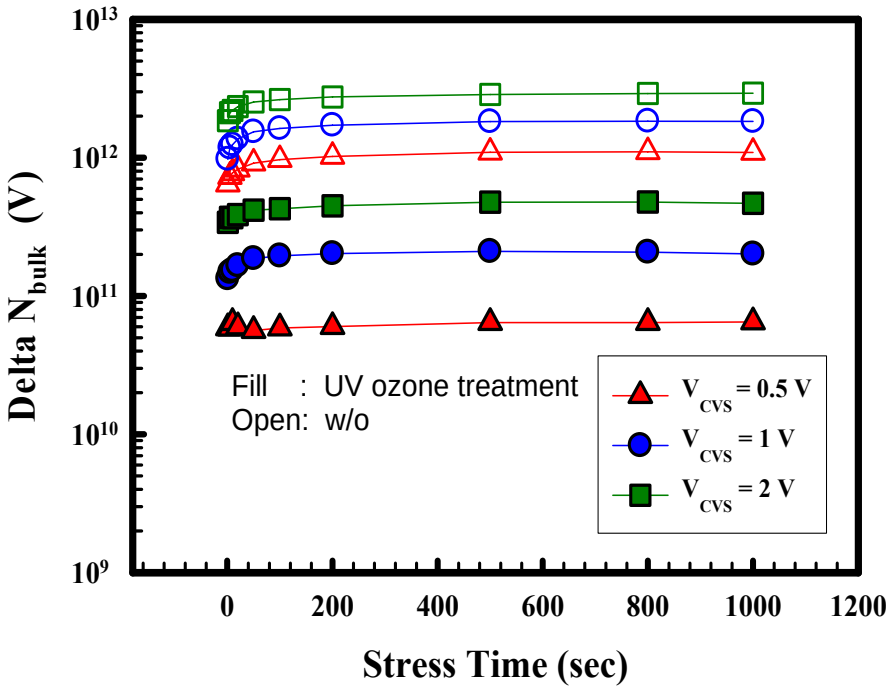


Figure 3-19 Delta N_{bulk} versus stress time for device with and without UV ozone treatment.

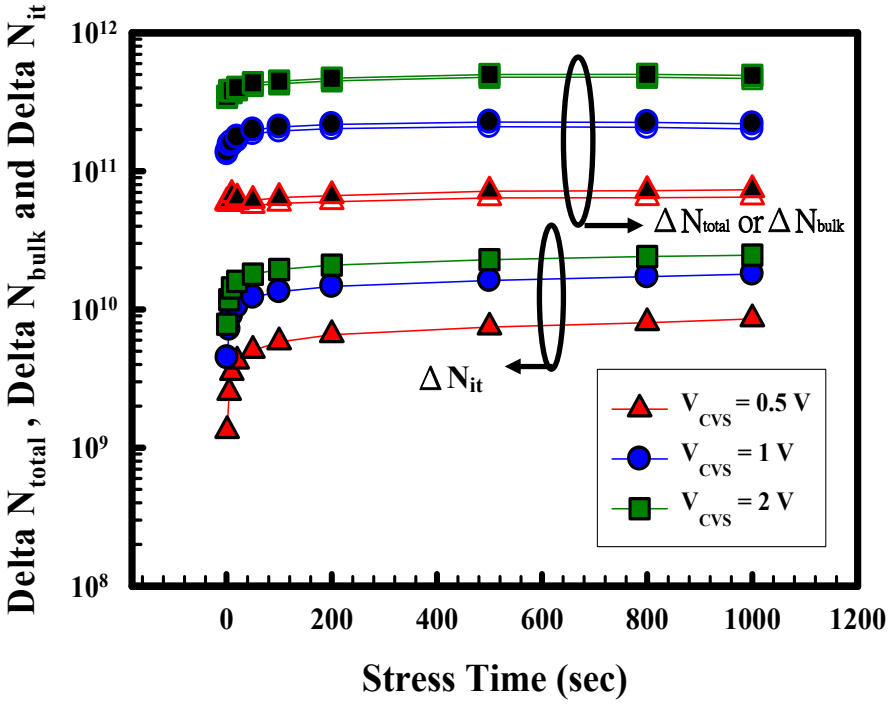


Figure 3-20 Interface charge densities, bulk charge densities and total charge density versus the stress times with UV ozone treatment.

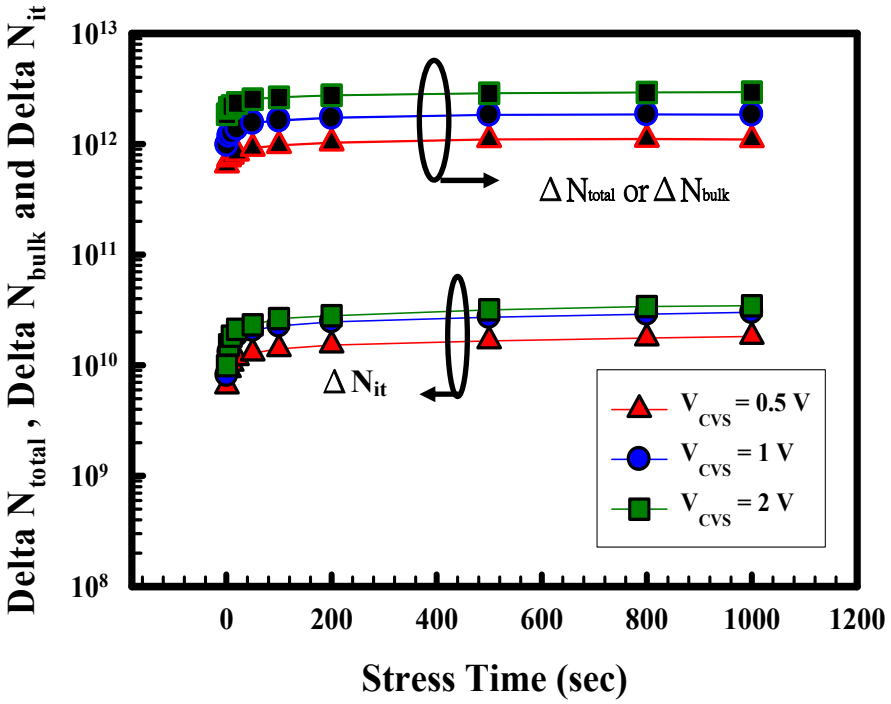


Figure 3-21 Interface charge densities, bulk charge densities and total charge density versus the stress times without UV ozone treatment.

	UV ozone surface treatment sample	Control sample
Threshold Voltage (V)	0.547	1.14
EOT at strong inversion (Å)	20	20.2
Substhreshold swing (mV/decade)	82.9	114.3
Hystersis (mV)	0.762	24.5
Normal transconductance peak value (S*cm)	$1.29*10^{-11}$	$6.96*10^{-12}$
Leakage current density (A/cm^2)@ Vg-Vt=1	$3.81*10^{-7}$	$4.35*10^{-6}$
Mobility peak value ($cm^2/V*s$)	377.05	285.76
Interface state density ($\#/cm^2$)	$3.65*10^{11}$	$1.23*10^{12}$

Table 3-1 Synthesize compared electrical characteristics.

CHAPTER 4

Conclusions and Recommendations for Future Works

4.1 Conclusions

The basic properties of the UV ozone oxide were studied first in chapter 2. A saturated oxidation was observed in the growth curves and the resultant self-limiting property could be used to control the interface layer thickness after a high temperature densify. We find the optimum condition of post deposition anneal with UV ozone treatment. We know that post deposition anneal at 900^{o}C is the optimum condition by the electronic measurement. We compared with UV ozone treatment and without on electrical characteristics. We observe that, lower EOT and leakage density by UV ozone treatment. Therefore, UV ozone can improve the interface quality. At other electrical characteristic such hystersis also were improved.

By different NH_3 plasma treatment's time of UV ozone oxide prior to $HfAlO_xN_y$ gate dielectric deposition were investigated. Significantly large fixed charges and hysteresis of NH_3 nitridation would degrade device performance. Form other electrical characteristics view, though EOT decreasing with the NH3 treatment's time increasing but that improvement on electrical characteristic is little. Leakage current density raises with the time of NH_3 plasma treatment increasing. Indicate NH_3 plasma treatment could higher the leakage current density. From leakage density current revealed that NH_3 plasma treatment maybe damaged the dielectric properties.

Time zero to breakdown also shows the bad electrical characteristic on NH_3 plasma treatment.

We used optimum condition (UV ozone treatment and PDA 900^{o}C 30 seconds after high k film deposit) on chapter two to fabricate the nMOSFETs and a control sample (without treatment and PDA900^{o}C 30seconds after high k film deposit) was fabricated at the same time. Basic electrical characteristics were compared with UV ozone treatment and without. Form the electrical characteristics, we observe that use UV ozone treatment improve the substhreshold swing (S.S.) from 114.3 to 82.9 (mV/decade), hysteresis from 0.762 to 24.5 (mv), Leakage current density@ V_g-V_t=1 from $3.81*10^{-7}$ to $4.35*10^{-6}$A/cm^2,mobility peak value form 377.05 to 288.76 (cm2/V*s), normal transconductor peak value (Gm) from $6.96*10^{-12}$ to $1.29*10^{-11}$ (S*cm) and interface state density N_{it} from $3.65*10^{11}$ to $1.23*10^{12}$ (#/cm2).

We determine the energy distribution of the interface traps in a relatively large part of the forbidden energy gap on both sides of midgap by measuring the charge pumping currents (I_{cp}) with variable fall and rise times. By the result which tells us strong fall-time dependence of charge pumping current for fixed rise time. This also means that acceptor-like interface stats exist on with UV ozone treatment and treatment for $HfAlO_xN_y$ stacks nMOSFETs.

Then we estimate reliability of the $HfAlO_xN_y$ stacks nMOSFETs by constant voltage stress (CVS). We know that UV ozone surface treatment can improved delta interface state density and bulk charge trap density during the constant voltage stress compared with the control sample. Final, we finds the bulk charge density to dominate the threshold voltage shift during the constant voltage stress for with UV ozone treatment and without.

4.2 Recommendations for Future Works

1. More HRTEM images to evidence thickness variation and interfacial layer reaction.
2. More physical analysis to understand the properties of the ozone oxide.
3. Metal gate replace with poly gate to study the device characteristics
4. Various surface treatment to study the device characteristics.
5. Improve the interface between the poly gate and high k dielectric by UV ozone treatment.

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