國立交通大學

電子工程學系 電子研究所

博士論文

高介電係數介電質材料應用於金氧金電容之研究

The Investigation of Metal-Insulator-Metal Capacitor Applying High-κ Dielectrics Material

研究生：黃靖謙
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中華民國九十八年六月

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摘要

根據國際半導體技術藍圖制定會(ITRS)，元件尺寸必須不斷的縮微，為了配合現今類比、射頻通訊和記憶體元件的發展，金氧金電容(MIM Capacitor)的研發是刻不容緩的。在各種不同的被動元件中，金氧金電容經常被廣泛的應用在射頻電路裡的阻抗匹配與直流濾波器中；然而，它們通常卻占據了很大的電路面積。此外，金氧金電容也是發展高密度動態記憶體中所面臨的重要挑戰之一。因此，為了有效降低晶片的面積與節省成本，提高單位面積的電容值是極為需要的。為了達到未來記憶體元件的高電容密度要求，高介電係數介電質材料的開發似乎是唯一的選擇。當使用高介電質材料時，在增加材料的介電常數和減少元件厚度所伴隨而來的高漏電，更是目前主要的研究議題之一。

目前高介電材料應用於金氧金電容從氮氧化矽(κ~4-7)、氧化鋁(κ~10)、氧化鉿(κ~22)、氧化鉭(κ~25)，一直發展到氧化鈮(κ~40)。但是目前在這些材料中還無法同時達到在高電容密度下金氧金電容所需要的特性，例如：低漏電、低電壓和低電容變化係數。因此，我們發展出新的製程和高介電係數的材料來改進金氧金電容，例如氧化鎳(κ~30-40)、氧化鐠(κ~26-32)和鈦酸鍶(κ>50)。為了進一步改

善介電質低能隙的缺點，我們利用較高功函數金屬鉑或鈹當作上電極，可以得到較佳的元件特性。

雖然，鈦酸鍶具有高介電係數，但較低的導帶不連續(conduction band discontinuity)和能帶寬度(bandgap)，會造成較大的電流。鈦酸鍶必須要形成結晶相才能具有較高的介電係數(κ~150-170)，而要形成奈米結晶(nano-crystal)的鈦酸鍶，則需要較高的製程溫度(>450^{o}C)，這不適用於後段製程。此外，鈦酸鍶具有電壓電容係數(Voltage coefficient of capacitance)較高的缺點。因此，我們利用氧化鉭具有降低漏電流以及改善電壓電容係數的特性，將氧化鉭以一定比例摻入鈦酸鍶中，可有效降低整體元件的漏電流和電壓電容係數。此外，我們也成功發展出一種電漿處理(Plasma treatment)介電質的方法，不但在漏電流上有明顯的改善，也同時改良了電壓電容係數和溫度電容係數(Temperature coefficient of capacitance)。

除了基本的漏電流與低頻量測以外，我們也量測了射頻電容的高頻散射參數。並利用模擬軟體，淬取出元件在不同頻率所具有的電容大小。除此，我們還深入探討電容的傳導機制與電容變化跟電壓和溫度相關的成因，相信本篇論文對未來發展高效能金氧金電容會有很大的助益。

The Investigation of Metal-Insulator-Metal Capacitor Applying High-κ Dielectrics Material

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Abstract

According to International Technology Roadmap for Semiconductor (ITRS), continuous increasing the capacitance density ($\varepsilon_0\kappa/t_\kappa$) is required to scale down the device size and the cost of Metal-Insulator-Metal (MIM) capacitors which are widely for Analog, RF and DRAM functions. However, they often occupy a large fraction of circuit area. To meet these requirements, high dielectric constant (κ) materials provide the only solution since decreasing the dielectric thickness (t_κ) degrades both the leakage current and $\Delta C/C$ performance. To achieve this goal, the only choice is to increase the κ value of the dielectrics, which have evolved from SiON (κ~4-7), Al_2O_3 (κ=10), HfO_2 (κ~22), Ta_2O_5 (κ~25) to Nb_2O_5 (κ~40).

To further achieve the properties of MIM such as low leakage current, low voltage coefficient of capacitance and low temperature coefficient of capacitance. Thus, we have developed novel process and high-κ dielectric materials, such as TiNiO (κ~30-40), TiPO (κ~26-32) and $SrTiO_3$ (κ>50) to achieve this technology. To further improve the small bandgap (E_G) of these dielectrics, we apply the higher

work-function (ϕ_B) Pt (5.7 eV) and Ir (5.3 eV) top electrode are used to give better device performance.

Although $SrTiO_3$ has large dielectric (κ~50-200), the small conduction band offset (ΔEc) and bandgap leading to larger leakage current is a larger drawback. Besides, $SrTiO_3$ shows its higher κ values by forming nano-crystals, which is only practicable at a higher process temperature > 450°C. Furthermore, the high voltage coefficient of capacitance of $SrTiO_3$ is also an important issue. Because Ta_2O_5 has very low voltage coefficient of capacitance and can considerably suppressed the leakage current, the overall electrical characteristics of MIM device could be improved by doping Ta_2O_5 into $SrTiO_3$ MIM capacitor. Otherwise, we have developed a plasma treatment on dielectric to repair the defect of the dielectric to improve leakage current, voltage coefficient of capacitance and temperature coefficient of capacitance at the same time. Therefore, not only high capacitance and low leakage current, but also small voltage/temperature dependence of capacitance are obtained under limited thermal budget for back-end-integration.

In addition to the measurement of capacitance at low frequency and the leakage current, the measurement of the S-parameters to investigated the characteristics of the MIM capacitors at RF regime are also demonstrated. By using the simulation software, the capacitance density of MIM capacitors at different frequencies was extracted.

Besides, the related factors such as understandings of the mechanism of conductivity, the voltage/temperature dependence of capacitances, barrier height, and interfacial layer were investigated, and these are also useful in the development of advanced MIM capacitors.

Acknowledgement

That I exist is a perpetual surprise which is life.
- Rabindranath Tagore

我的博士求學過程－現在回想起來感覺像是一場冒險旅程。旅程中充滿各種的關卡。每個關卡都需要一把鑰匙，而通過之後是絕無僅有的寶物與更多的抉擇。冒險中的鑰匙是我的老師、朋友、以及家人、甚至一些從未見過的朋友。寶物是我從錯誤中學習的人生經驗。而抉擇是我充滿未知的人生。

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Chapter 1

Introduction

1.1 Motivation to study High-κ Dielectric Materials

In the scaling down of CMOS, reducing the thickness of gate stack while maintaining lower leakage current plays an important role. The leakage current of devices with the same gate dielectric reduces with the scaling down of gate length and width; however, the leakage current density increases with the scaling gate dielectrics exponentially. In other word, the gate leakage current increases as the device size degreases. The larger leakage current will lead to the degrading effect of devices' reliability and higher power consumption of the devices. Therefore, reducing the leakage current with scaling down the device size will be a crucial issue in the development of advanced electrical devices.

Because the leakage current is strongly related to the physical thickness of dielectric layer, increasing the thickness of dielectric layer can considerably suppress the leakage current of the devices. By using the dielectric material with high dielectric constant (high-κ), the physical thickness of the dielectric layer in the devices could be increased without reducing the capacitance density. High-κ dielectric material often exhibits poorer material properties than SiO_2, such as smaller bandgap, weaker bond, and higher defect density; however, the high-k dielectrics with the same effective oxide thickness (EOT) with SiO_2 still demonstrate lower leakage current than SiO_2 by several orders. This is the reason why high-κ dielectric material plays an important role in the future advanced technology.

According to the ITRS (International Technology Roadmap for Semiconductor) [1] of SIA showing in Figure 1-1, the thickness of gate oxide is required to be below 10 Å after 2009. In addition, the gate length and bias voltage reduce by 11% every year while maintaining the drive current of device is needed. Thus, it is inevitable to continually scale down the gate dielectric in the proceeding CMOS technology. On the other hand, the operation frequency of the device below the generation of 100 nm will be above GIGA Hz and the electrical characteristics of high-κ dielectrics at that frequency play a crucial position for the using of high-speed electrical devices. Although several high-κ dielectrics exhibit good electrical characteristics at low frequency, their performance would possibly degrade at RF regime. Therefore, it is imperative to find out the high-κ dielectric exhibiting practicable characteristics at both high and low frequency region.

In the recent, there are some high-κ dielectrics have been widely investigated and the issues and characteristics of these dielectric material have also been reported.

Unfortunately, high-κ dielectrics showing good performances are often accompanied by some drawbacks. Searching for the most practicable high-κ dielectrics for the use of advanced electrical device and altering the suitable device structure or process to meet the requirement of high-speed device is the most imperative mission to apply high-κ dielectrics to the next VLSI generation.

1.2 Motivation to study MIM capacitors using high-κ dielectrics

For electrical devices, especially for mobile applications, it is imperative to reduce the capacitor area since the area percentage of capacitor significantly increases with the scaling down of logic parts. In RF applications, a high degree of linearity is required for capacitors to minimize harmonic generation and improve balancing. Integration of high-quality and high-density MIM capacitors is a challenge for the RF transceiver roadmap. The need to integrate new materials in a cost-effective manner to realize high-density MIM capacitors follows the guideline published in the ITRS roadmap. Potential solutions for MIM capacitors include the introduction of high-κ dielectrics now being developed for future use for gate dielectrics [2-16]. Therefore the high-κ dielectrics used in MIM capacitors have evolved from SiON (κ~4-7) [3-5], Al_2O_3 (κ=10) [13], HfO_2 (κ~22) [7]-[11], Ta_2O_5 (κ~25) [12], [15] to Nb_2O_5 (κ~40) [16]. Unfortunately, the demonstration of MIM with these films is not practicable to achieve properties, such as non-dispersive, good linearity and high breakdown with low leakage concomitantly, at high unit capacitance. To achieve this goal, some novel high-κ dielectrics have been studied, which have progress from TiO_2 (κ~50-80) [17], TiHfO (κ~40-50) [18], TiTaO (κ~40-50) [19]-[21] to $SrTiO_3$ (STO, κ~50-200) [21]-[23].

It has been studied that titanium oxide (TiO_2) exhibits several better properties than other dielectrics. In addition to its higher dielectric constant, TiO_2 has good thermal stability while it was integrated with TiN electrode. It allows TiO_2 shows the dielectric characteristic after high temperature process for silicide formation. Moreover, the heat conduction rate of TiO_2 is higher than that of SiO_2. Although TiO_2 has the above merits, there are still some major drawbacks that should be overcome, such as larger leakage current than that of other dielectrics with the same effective oxide thickness, lower breakdown voltage, and interfacial oxide layer forming after post implant RTA. However, it has been reported that thickness of the interface oxide layer could be reduced by using NH_3 plasma treatment [23], but the flat-band voltage shift and the degradation of channel mobility still occurred.

$SrTiO_3$ (STO) is a potential candidate to increase the κ value beyond a value of 45, It has the well-known perovskite-type structure and has a para-electric phase above 105K, and high-κ value of ~300 at room temperature. This makes it an attractive candidate for DRAM [24]-[27] due to the high charge storage capacity and para-electricity (no fatigue or aging problems). To achieve the high κ value, the STO requires a heat treatment at 450~500°C under an oxygen ambient for crystallization [24]-[26]. Therefore, it also requires a Pt or RuO_2 lower electrode [25] to withstand the high temperature oxidation, but the high cost and availability of noble metals pose concerns for mass production.

The continuous scaling down of the design rule for DRAM lead to some difficulties needed to overcome. In the G-bit DRAM generation, the memory cell density is too high that the dielectrics couldn't fill the cell space, while its thickness is larger than 20 nm. This limitation of dielectric thickness makes it impossible to use the quaternary metal oxide, such as $SrTiO_3$ or $BaSrTiO_3$ as the dielectric layer. Due to the difficulties of conformal CVD for these quaternary metal oxides, the high aspect ratio of trench for DRAM is an inevitable challenge to solve.

Because of the high dielectric constant, minimum thickness limit and good ability of step coverage, simple metal oxide such as Ta_2O_5, Al_2O_3, ZrO_2, HfO_2 and Pr_2O_3 are thought as the promising dielectric materials in the development of advanced DRAM technology. Among these dielectrics, ZrO_2, HfO_2 and Pr_2O_3 exhibit larger conduction band offset (ΔEc ~0.5 eV), bandgap (~4-6 eV), dielectric constant (κ~ 15-25) and bond enthalpy to prevent from larger leakage current and obviously degradation after high temperature process. Similar to high- κ /Si CMOSFET, the larger conduction band offset is the better choice for MIM capacitor. Due to their moderate permittivity, it is difficult to meet dielectric layer with an EOT well below 1.0 nm. One solution to raise the permittivity is combining them with very high-κ dielectric, such as TiO_2 with high permittivity value of 50-80 contributing from the soft phonons. From above discussion, we know TiO_2-based dielectric material combined with moderate high-κ and large bandgap and conduction band offset materials will be a suitable approach for logic devices (metal gate/high-κ) or DRAM technology beyond 45 nm.

On the other hand, in order to fabricate monolithic microwave integrated circuits successfully, it is required to meet reliable, repeatable, and predictable performance for both active and passive components. Among them, the capacitor used in filtering, decoupling and network matching plays a significant role in front end or mixed signal circuits. Therefore, capacitors with high capacitance density, low voltage coefficient, good capacitor matching, precision control of values and low parasitic effects are required. By using thin dielectric film with high dielectric constant, the capacitance density could be considerably increased. Recently, some kinds of dielectrics and methods have been reported to meet the goal of high capacitance density and good characteristics.

Moreover, it is also essential to investigate the interface between the electrode and high-κ dielectric layer, especially the bottom electrode which is being exposed to the precursors during the deposition. During the post annealing process, there will be interfacial layer form between bottom electrode and dielectric layer. There will be traps and defects in the interfacial layer. Since it is know that leakage can be interface or bulk dominated. If the thickness of interfacial layer is thicker, the leakage current would be higher due to more traps formation. In addition, it has been reported the traps present in the dielectric also resulted in the dispersive capacitor behavior. It is thus, useful and needed to investigate how to reduce the interfacial layer formation during process.

1.3 The Background of Metal Electrodes

The Metal-Insulator-Metal (MIM) structure can reduce the contact resistance and increase the storage charge with comparison to Metal-Insulator-Semiconductor (MIS) structure. MIM capacitors are often integrated in the back end part of process flow. In the back end process, the maximum process temperature is restricted by the thermal budget.

As DRAM density increasing, devices shrinkage and higher charge storage is inevitable. It is difficult for conventional MIS structure to achieve the requirements, so MIM structure is expected to apply in the trench DRAM process. Therefore, the interaction between high-κ dielectric layer and metal electrode is not been anticipated. If high-κ material interacts with the metal electrode, there will be an interfacial layer forming between high-κ material and metal electrode. The interfacial layer will change the properties of whole dielectric film, such as interface roughness, interface stress, electron barrier height, thermal stability, etc.

The demand for advanced materials in the DRAM trench capacitor is delayed compared to the stacked capacitor by only a few years. Several high-κ materials are currently used in the Silicon-Insulator-Silicon (SIS) structure for DRAM trench capacitors, but a metal-top electrode will be needed in 2007 and a full MIM structure with high-κ material may be needed until 2009.

The electrodes of MIM capacitors are fabricated using metals such as TaN, TiN, etc., which are often deposited using CVD (chemical vapor deposition), ALD (atomic layer deposition) or MOCVD (metal organic chemical vapor deposition) methods. Low-temperature electrode deposition process (< 450^{o}C) is required for MIM capacitors used for logic-friendly embedded DRAM features.

1.4 The Deposition method of High-κ Dielectrics

Several methods to deposit thin high-κ dielectrics have been proposed in recent years and these various methods each exhibit the merits while there are some issues needed to overcome.

Recently, atomic layer chemical vapor deposition (ALCVD) has attracted much attention due to its self-limit and mono-layer deposition properties. ALCVD is the method using MCL_4 (M: Hf, Ti, Zr….) and H_2O as sources to deposit high-κ dielectrics. The precursors are introduced into the heated chamber and substrates. The reaction only occurs in the substrate surface instead of the deposited layer and each layer is deposited at a time. Therefore, the thickness of dielectrics could be controlled precisely and is dependent on the process cycle linearly. Although the excellent uniformity of deposition can be achieved on SiO_2 and Si_3N_4, the directly deposition on H-terminated Si substrate would lead to rough surface. Unfortunately, H-terminated Si substrate is inevitable after HF dipping. Therefore, the improvement of process precursor is the key point to overcome the issues of ALCVD deposition.

Metalorganic chemical vapor deposition (MOCVD) is the other dispositive method wildly used in VLSI fabrication. The dielectrics are deposited by using metal organic precursor vapor. During the deposition process, the precursors are introduced into low-pressure chamber and the substrate is heated to some suitable process temperature. The uniform and conformal deposition of dielectrics can be obtained by using MOCVD. This is why MOCVD process is integrated into fabrication process flow extensively. Although MOCVD have many merits, it still has some issues, such as carbon contamination and the impact of precursors to the environment and health.

Using PVD method to deposit the metal or metal oxide directly on the substrate followed by thermal oxidation and annealing is the other method to deposit dielectrics. In the past five years, there are many reports about this technology. In the beginning of the deposition process, the pre-clean Si substrate is loaded into high vacuum chamber immediately to prevent from native oxide formation. Following, the metal layer is deposited using reactive dc magnetron sputtering with oxygen modulation technique. Or, the metal oxide layer is sputtering directly followed by annealing. This method could be compatible with the modern VLSI process; however, the formation of interfacial oxide and crystallization are the crucial issues required to be solved. By combining the nitridation and dielectrics doping techniques, the above problems could be minimized. Thus, this dispositive method is still practicable due to the merits.

In our studies, the PVD method is used to deposit the high-κ dielectrics layer. Before high-κ dielectric layer deposition, we utilized NH_3 plasma treatment on the bottom electrode. Then, the pre-cleaned Si wafer was loaded into E-beam evaporator under high vacuum condition. After depositing the dielectric film, it was subsequently oxidized in O_2 ambient followed by annealing. The devices using TiNiO, TiPrO, $SrTiO_3$, and $SrTiO_3$ doped Ta_2O_5 are fabricated and measured at high and low frequencies.

1.5 The evaluation of high-κ value

First, we consider our MIM capacitor:

$$C = \frac{\kappa \varepsilon_0 \mathrm{A}}{t} \tag{1.1}$$

where κ is the dielectric constant (also referred to as the relative permittivity in this article) of the material, ε_0 is the permittivity of free space (8.85×10^{-3} fF/μm), *A* is the area of the capacitor, and *t* is the thickness of the dielectric. This expression for *C* can be rewritten in terms of t_{eq} and κ_{ox} (=3.9, dielectric constant of SiO_2) of the capacitor. The term t_{eq} represents the theoretical thickness of SiO_2 that would be required to achieve the same capacitance density as the dielectric:

$$t_{eq} = \frac{3.9 \times \varepsilon_0}{C_{high-k}} = \frac{3.9 \times 8.85 \times 10^{-3} (\mathrm{fA/\mu m})}{C_{high-k}\,(\mathrm{fA/\mu m^2})} = \frac{3.9 \times 8.85}{C_{high-k}} \ (\mathrm{unit}: nm) \tag{1.2}$$

Thus, the high-κ value of an alternative dielectric employed to achieve the equivalent capacitance density of t_{eq} can be obtained from the expression:

$$\kappa_{high-k} = \frac{3.9 \times t_{high-k}}{t_{eq}} \tag{1.3}$$

1.6 The measurement of the Devices

To investigate the electrical characteristics of our devices, we measured the leakage current using HP 4156A semiconductor parameter analyzer. Besides, HP4284A precision LCR meter was used to evaluate the capacitance density and the conductance ranging from 100 kHz to 1 MHz. Furthermore, to investigate the characteristics of our devices at the frequency above 1 MHz, we measured the scattering parameter using HP8510C network analyzer and the test set. The measurement set-up for S-parameter is shown in Figure 1-2. Network analyzer generates a calibrated RF signal and has three input measuring channels. These are commonly called the R, the A, and the B channels. The R channel is used to measure the incident voltage, and the A and B channels measure reflected and transmitted voltages. Then, we can obtain S_{11} and S_{21} by calculating A/R and B/R in polar form, respectively. The S_{12} and S_{22} can also be obtained using the same way except changing the input voltage channel. The noise figure and associated gain were measured by HP85122A and ATN-NP5B noise parameter extraction system (shown in Figure 1-3) up to 6 GHz. There are three major categories of measurement type that the system can supply: DC, S-parameters, and noise parameters. The first two categories mainly support the noise parameter measurement.

1.7 Innovation and Contribution

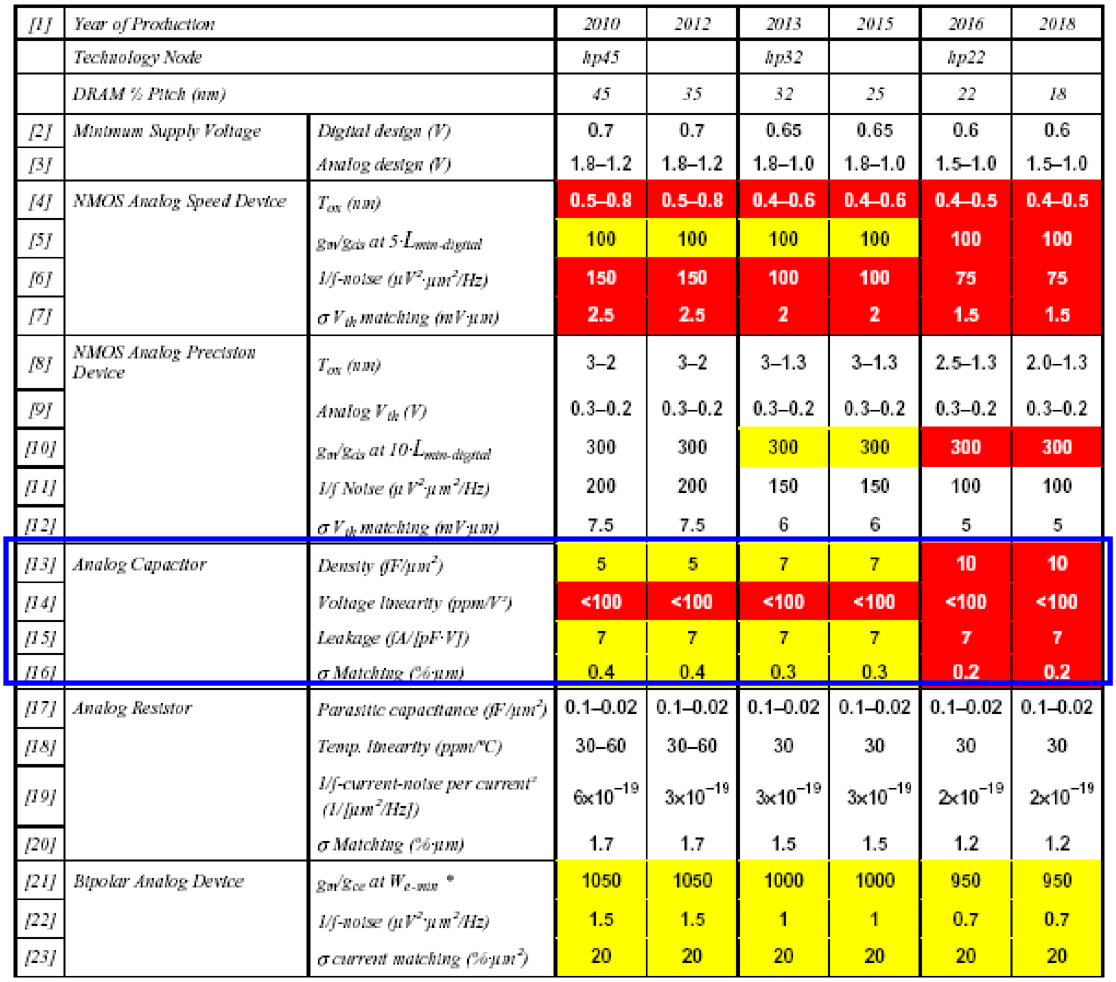
The overall objective of this thesis is to achieve a fundamental understanding of the working principles and the implementation issues of the Metal-Insulator-Metal capacitor and to demonstrate the novel high-κ dielectric material, electrode gate and treatment approaches for our device. The innovation of this thesis and the major topics it addresses are as follows.

First, we have investigated the effects of N^+ plasma treatment and oxygen annealing on Ni/TiNiO/TaN capacitors. The novel high-κ TiNiO dielectric material is first studied in this work and the Ni top electrode is used instead of the other high work function metal electrode, such as Pt or Ir. The post deposition annealing of TiNiO under oxygen ambient increases the capacitance density but trades off the increased leakage current. This leakage current could be considerably reduced by applying an optimized N^+ plasma treatment on the dielectric film. At high capacitance density of 17.1 fF/μm^2, a low leakage current of 7.7×10^{-6} A/cm^2 at 1 V is obtained.

Second, we demonstrate high quality material TiPrO and high density $Ti_xPr_{1-x}O$ (x~0.67) metal-insulator-metal (MIM) capacitors using high work function (~5.3 eV) Ir top electrode. Pr_2O_3 is one of attractive rare earth metal oxides with many merits such as large conduction band offset (ΔE_C~ 1 eV), moderate dielectric constant (κ~15) and large bandgap (E_G ~4 eV). Furthermore, significantly large Gibbs free energy of Pr_2O_3 (+106 kcal/mol) in contact with silicon can avoid metal/oxide inter-diffusion or chemical reaction caused by oxygen exchange, which not only reduce the interfacial layer between dielectric layer and bottom electrode but also performs excellent thermal stability. Combining above advantages of high-κ Pr_2O_3 with the high dielectric constant of TiO_2 (~50), mixed TiPrO dielectric overcomes the issue of leakage current without scarifying capacitance density. Very low leakage current of 7×10^{-9} A/cm^2 at -1 V and high 16 fF/μm^2 capacitance density are achieved for 400 ^{o}C anneal TiPrO, which also meets the ITRS goals (at year 2018) of 10 fF/μm^2 density and $J/(C\cdot V) < 7\ \mathrm{fA}/(\mathrm{pF}\cdot V)$. Furthermore, the improved high 20 fF/μm^2 capacitance density TiPrO MIM is obtained at higher annealing temperature, where low leakage current 1.2×10^{-7} A/cm^2 is measured at -1 V. These good performances indicate TiPrO MIM is suitable for analog/RF ICs Applications.

Third, the impact of Ta_2O_5 doping on electrical characteristics of $SrTiO_3$ MIM capacitors was studied for the first time. Using high-κ Ta_2O_5 doped STO dielectric (PDA temperature:420^{o}C), an absolute value of quadratic voltage coefficient of capacitance (VCC-α) of 420 ppm/V^2 and high capacitance density of ~20 fF/μm^2 are achieved in this work. This is approximately one order of magnitude better than the same device using a pure STO, with added advantages of improved voltage and temperature coefficients of capacitance. Besides, the degradation of electrical properties (the capacitance variation versus voltage, VCC-α, and the long-term reliability) after stress are all reduced, in contrast with using a pure STO. Therefore, this doping method has merit for achieving both low VCC and maintaining high capacitance density beyond previous STO MIM studies. Moreover, although nano-crystallized STO shows higher κ values and good device characteristics, the nano-crystallized STO requires a heat treatment at 450~500°C under an oxygen ambient. This activation maximum temperature (>450°C) cannot permit for the backend integration. In this study, the improvement on VCC by using amorphous Ta_2O_5 doped STO MIM capacitors with low thermal budget (420°C) could be achieved.

Finally, in this thesis, we achieved high-κ value to 169 and capacitance density to 35 fF/μm^2, or capacitance-equivalent-thickness (CET) of 0.99 nm for unified multi-functional SoC. Such large capacitance density with low leakage current was achieved by using very high-κ $SrTiO_3$ (STO) with formed nano-crystals (4.3 nm). This small poly grain size is also important to reduce variation among devices. In addition, a plasma nitridation was applied to bottom TaN that prevents CET degradation by forming interfacial TaON during STO post-deposition anneal (PDA) or using expensive conductive noble electrodes, such as Pt, Ru, and Ir. Moreover, we have studied STO MIM capacitor for RF application. Very high capacitance density of 35 fF/μm^2, high κ value of 169 and small capacitance variation with frequency and voltage are obtained at the same time that demonstrates the excellent device performance for RF application. These high performance capacitors can drastically reduce the RF capacitor area, yet can be fabricated with full compatibility with current VLSI process lines. Although this work could achieve high capacitance density and low leakage current at the same time, but its higher PDA temperature (>450°C) to form nano-crystal is an important issue in the back-end process flow.



			2010	2012	2013	2015	2016	2018
[1]	Year of Production		2010	2012	2013	2015	2016	2018
	Technology Node		hp45		hp32		hp22	
	DRAM ½ Pitch (nm)		45	35	32	25	22	18
[2]	Minimum Supply Voltage	Digital design (V)	0.7	0.7	0.65	0.65	0.6	0.6
[3]		Analog design (V)	1.8–1.2	1.8–1.2	1.8–1.0	1.8–1.0	1.5–1.0	1.5–1.0
[4]	NMOS Analog Speed Device	T_{ox} (nm)	0.5–0.8	0.5–0.8	0.4–0.6	0.4–0.6	0.4–0.5	0.4–0.5
[5]		g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$	100	100	100	100	100	100
[6]		1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	150	150	100	100	75	75
[7]		σV_{th} matching ($mV \cdot \mu m$)	2.5	2.5	2	2	1.5	1.5
[8]	NMOS Analog Precision Device	T_{ox} (nm)	3–2	3–2	3–1.3	3–1.3	2.5–1.3	2.0–1.3
[9]		Analog V_{th} (V)	0.3–0.2	0.3–0.2	0.3–0.2	0.3–0.2	0.3–0.2	0.3–0.2
[10]		g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$	300	300	300	300	300	300
[11]		1/f Noise ($\mu V^2 \cdot \mu m^2/Hz$)	200	200	150	150	100	100
[12]		σV_{th} matching ($mV \cdot \mu m$)	7.5	7.5	6	6	5	5
[13]	Analog Capacitor	Density ($fF/\mu m^2$)	5	5	7	7	10	10
[14]		Voltage linearity (ppm/V^2)	<100	<100	<100	<100	<100	<100
[15]		Leakage ($fA/[pF \cdot V]$)	7	7	7	7	7	7
[16]		σ Matching (%·µm)	0.4	0.4	0.3	0.3	0.2	0.2
[17]	Analog Resistor	Parasitic capacitance ($fF/\mu m^2$)	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02
[18]		Temp. linearity (ppm/°C)	30–60	30–60	30	30	30	30
[19]		1/f-current-noise per current² ($1/[\mu m^2/Hz]$)	6×10^{-19}	3×10^{-19}	3×10^{-19}	3×10^{-19}	2×10^{-19}	2×10^{-19}
[20]		σ Matching (%·µm)	1.7	1.7	1.5	1.5	1.2	1.2
[21]	Bipolar Analog Device	g_m/g_{ce} at $W_{e\text{-}min}$ *	1050	1050	1000	1000	950	950
[22]		1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	1.5	1.5	1	1	0.7	0.7
[23]		σ current matching ($\% \cdot \mu m^2$)	20	20	20	20	20	20

Figure 1-1 The International Technology Roadmap of analog and mixed-signal capacitors.

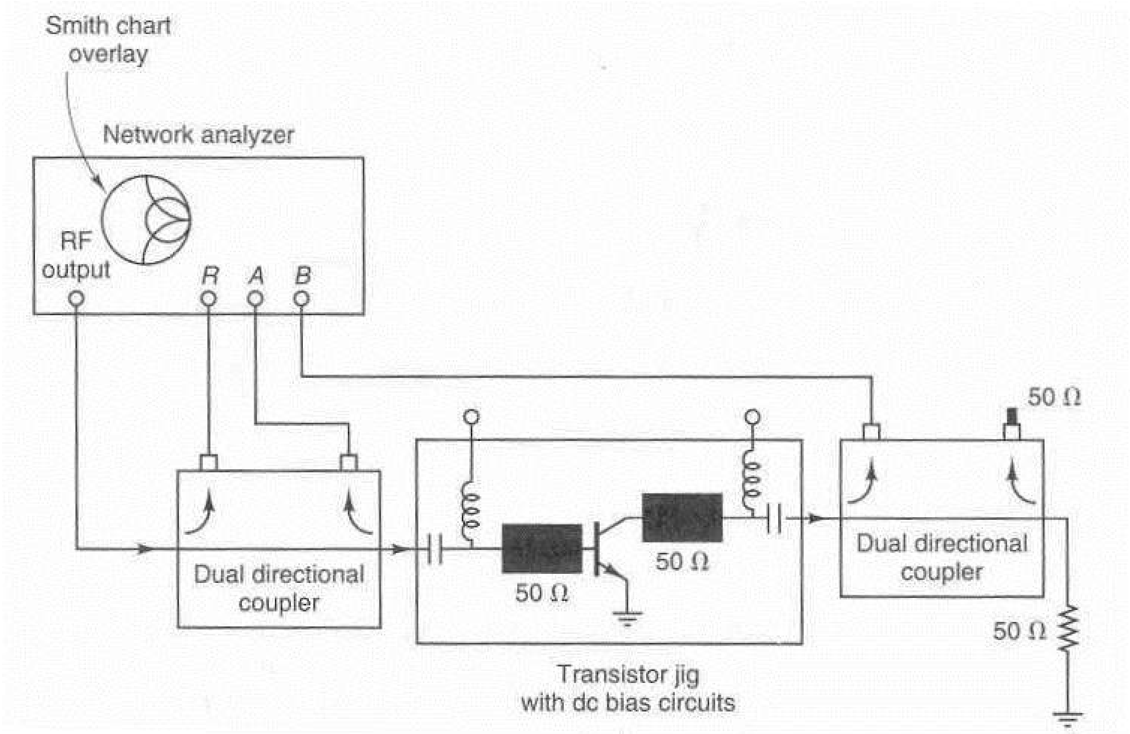


Figure 1-2 The measurement set-up for S-parameter.

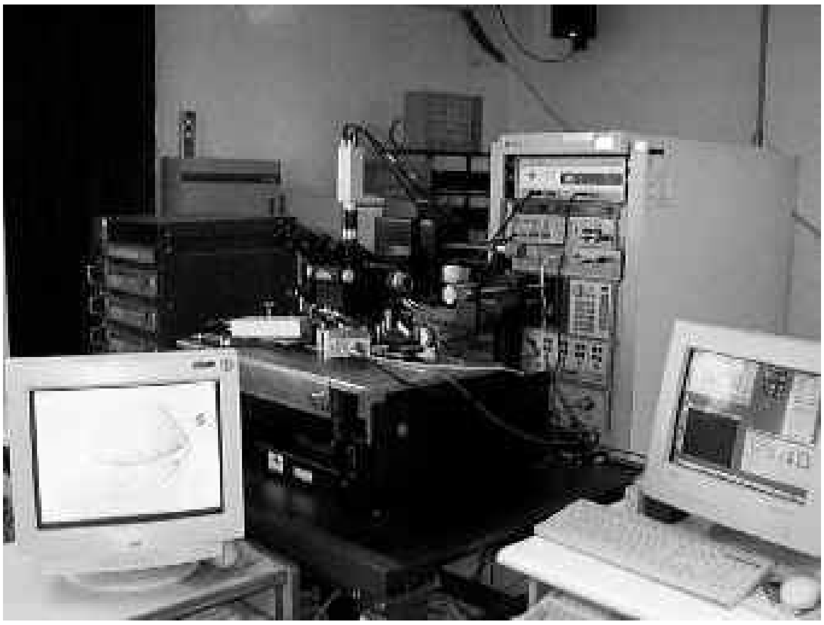


Figure 1-3 The illustration of HP85122A and ATN-NP5B noise measurement system.

Chapter 2

Leakage Current Improvement of Ni/TiNiO/TaN Metal-Insulator-Metal Capacitors using Optimized N^+ Plasma Treatment and Oxygen Annealing

2.1 Motivation

Metal-insulator-metal (MIM) capacitors are widely used in integrated circuits (ICs) for analog, radio frequency and dynamic random access memory applications. The performance requirements of MIM capacitors are the high capacitance density, low leakage current, small voltage dependence of the capacitance ($\Delta C/C$) and low process temperature $\leq 400°C$ for back-end integration. To meet these goals, both high-κ dielectric TiNiO and high work function electrode Ni are demonstrated. It is important to note that TiNiO is the low cost dielectric deposited by plasma vapor deposition (PVD) rather than the absolute high cost needed for atomic layer deposition which is usually used for some recent works like ZrO_2 with distinct low-κ value comparing to our TiNiO case.

The TiNiO is another potential dielectric material with a value of 30–40 that was obtained under an O_2 postdeposition annealing (PDA) at 420–460°C. However, it also requires a Pt or RuO_2 bottom electrode [25] to withstand such high temperature oxidation, but the high cost noble metals pose concerns for mass production. To address this issue in this paper we have fabricated TiNiO MIM capacitors on conventional bottom electrode TaN, where a NH_3 plasma treatment on TaN has been used to improve electrode stability, so the capacitance density degradation by forming interfacial TaO_x during PDA will obviously decrease. Besides, Binding energy between Nickel and Oxygen (855 eV~861 eV) [41] is significantly larger than the binding energy between Tantalum and Oxygen (~530 eV) [42] and Titanium and Oxygen (~457eV) [65], which causes strong binding between Nickel and Oxygen atoms. This indicates the more complete oxidation of the dielectric film which leads to its better dielectric properties than that of other dielectrics, such as TiTaO and TiO_2 [66].

To improve the leakage current, additional N^+ plasma treatment on TiNiO and high work-function Ni (5.1 eV) top electrode are applied during device processing. Based on these process methods, high 17.1 fF/μm^2 density and low 7.7×10^{-6} A/cm^2 leakage current at 1 V are simultaneously measured, which shows near two orders lower leakage improvement than previous TiNiO data. Such good device integrity indicates the good potential for TiNiO dielectric and high work-function Ni electrode for MIM capacitor application..

2.2 Experimental

The MIM capacitors were fabricated on 4 μm SiO_2 which had been deposited on a Si wafer. The lower capacitor electrodes were formed by depositing 0.05 μm TaN on a 1 μm Ta layer, where the thick Ta was chosen to reduce the parasitic resistance of the electrode and the TaN served as a barrier layer for the TiNiO. After patterning the lower electrode, the TaN was treated by NH_3 plasma nitridation at 100 W, to improve the lower interface. Then the $Ti_xNi_{1-x}O$ ($x\sim0.65$) dielectric with 19 nm was deposited by PVD dielectric layers were then deposited using RF magnetron sputtering. This was followed by 20W and 40W N^+ plasma treatment on the dielectric for 5 min and then 420°C to 460°C furnace annealing for 30 min under oxygen ambient subsequently to reduce the leakage current. Finally, Ni was deposited and patterned to form the top capacitor electrode. The fabricated MIM capacitors were characterized by current-voltage (*J-V*) and capacitance-voltage (*C-V*) measurements using an HP4156C curve tracer and HP4284A precision LCR meter, respectively.

4.3 Results and discussion

A. The effect of O_2 PDA temperature

Figures 2-1(a) and 1(b) show the *C-V* and *J-V* characteristics of $Ni/Ti_{0.35}Ni_{0.65}O/TaN$ MIM capacitors under 420 and 460°C annealing, respectively. Capacitance density increases from 12.8 to 17.7 fF/μm^2 with increasing O_2 PDA temperature. It is important to notice that the higher annealing temperature results in higher capacitor density, which may be due to more complete oxidation of the dielectric. From the measured capacitance density, a high-κ value of 27 was obtained for 420°C annealed TiNiO that becomes higher to 39 after increasing O_2 annealing temperature to 460°C. The low leakage current of 5×10^{-5} A/cm^2 (−1V) is measured at 17.7 fF/μm^2 capacitance density using Ni electrode that is significantly better than the previous TiNiO data of > 10^{-4} A/cm^2 (1V) at lower 14.3 fF/μm^2 density with Al top electrode [30]. Such improvement may be due to the discriminative work function between Ni (5.1 eV) and Al (4.25 eV) and higher TiO composition. In addition, the higher anneal temperature does not cause the underlying TaN film to oxidize apparently because of the improved TaN electrode stability after NH_3 plasma treatment.

Figure 2-2(a) shows $\Delta C/C$-V characteristics of Ni/TiNiO/TaN capacitors annealed at 420 and 460°C, respectively. The lines in the figure are fits to the data using the expression in the following expression:

$$\frac{\Delta C}{C}\times10^{6}=\left[\frac{C(V)-C(0)}{C(0)}\right]_{ppm}=\alpha V^{2}+\beta V \qquad (2.1)$$

The α and β are quadratic and linear voltage coefficient of capacitance, respectively. Since β can be compensated by appropriate circuit design [31], α is the dominant factor for the undesired $\Delta C(V)/C/C$. The α for 460°C annealed TiNiO device is larger than that annealed at 420°C, which is related to the higher capacitance density and larger leakage current at higher 460°C temperature. Figure 2-2(b) shows the temperature coefficient on capacitance (*TCC*) obtained from normalized capacitance of Ni/TiNiO/TaN MIM capacitor at frequency of 1 MHz. Again the *TCC* is higher for 460°C annealed sample than that of 420°C. Thus, a trade-off the capacitance density with α and *TCC* is needed based on device requirement.

B. N^+ plasma effect

To further improve the device performance with 460°C O_2 PDA, a N^+ plasma treatment on $Ti_xNi_{1-x}O$ dielectric is applied. Figure 2-3(a) shows the *J-V* characteristics of Ni/TiNiO/TaN capacitors processed at different N^+ conditions and 460°C O_2 PDA, where the capacitance density and leakage current are summarized in Figure 2-3(b). The capacitor with 20 W N^+ plasma treatment shows significant improvement on leakage current to 7.7×10^{-6} A/cm^2 at 17.1 fF/μm^2 capacitance density. This improvement of leakage current may arise from the nitrogen atom assists to passivate oxygen vacancies in the TiNiO dielectric and eliminate the electron leakage path mediated by the oxygen vacancies [32]-[34]. However, increasing N^+ plasma to 40 W, the leakage current is even worse than the untreated one, which may be due to the plasma damage at larger energy. The higher oxidation temperature and moderate N^+ plasma treatment largely improve the device performance.

Figures 2-4(a)~4(c) show the $\Delta C/C$-*V*, *TCC*, and summarized α, *TCC*, and capacitance equivalent thickness (CET) results of the Ni/TiNiO/TaN capacitors under different N^+ treatment conditions. The capacitors with 20 W N^+ plasma treatment not only reduce the leakage current but also improve the α and *TCC*, which may be due to the better TiNiO dielectric property by atomic N passivation to defects.

C. Performance comparison

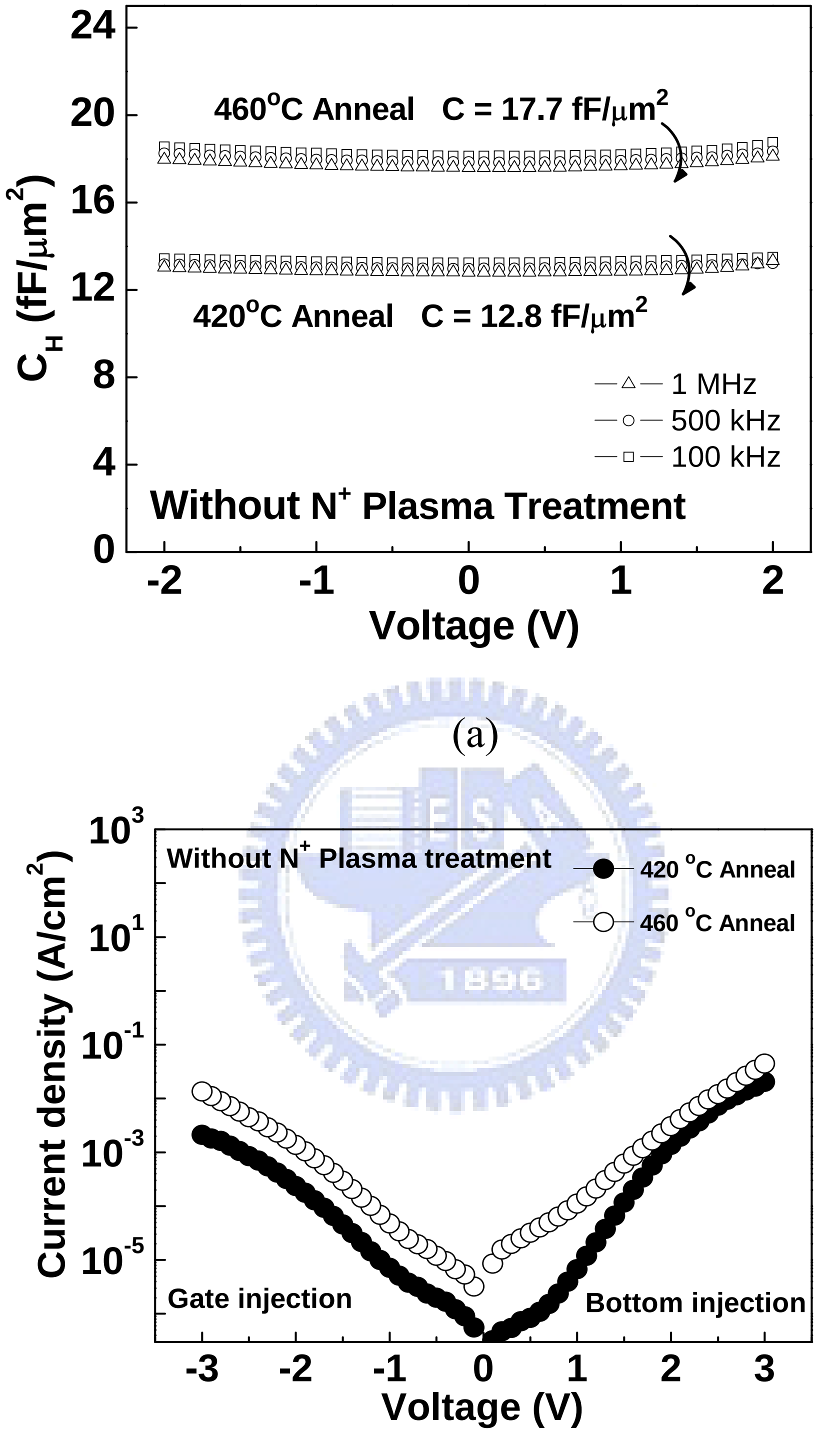
The important device parameters for the MIM capacitors are summarized in Table 2-1. Among the various high-κ capacitors, the Ni/TiNiO/TaN MIM capacitor, made using a high work-function Ni electrode and high-κ TiNiO dielectric, shows high capacitance density and low leakage current that are comparable with or better than the best reported data in the literature.

2.4 Conclusion

In this work, the different O_2 PDA temperature, N^+ plasma treatment, high work function Ni electrode were applied to TiNiO MIM capacitors. High capacitance density of 17.1 fF/μm^2 and low leakage current of 7.7×10^{-6} A/cm^2 at 1 V are obtained in Ni/TiNiO/TaN MIM capacitors. Such good capacitor device performance suggests a potential use of the Ni/TiNiO/TaN capacitor for IC applications.

Table 2-1. Comparison of MIM capacitors with various dielectrics and metal electrode.

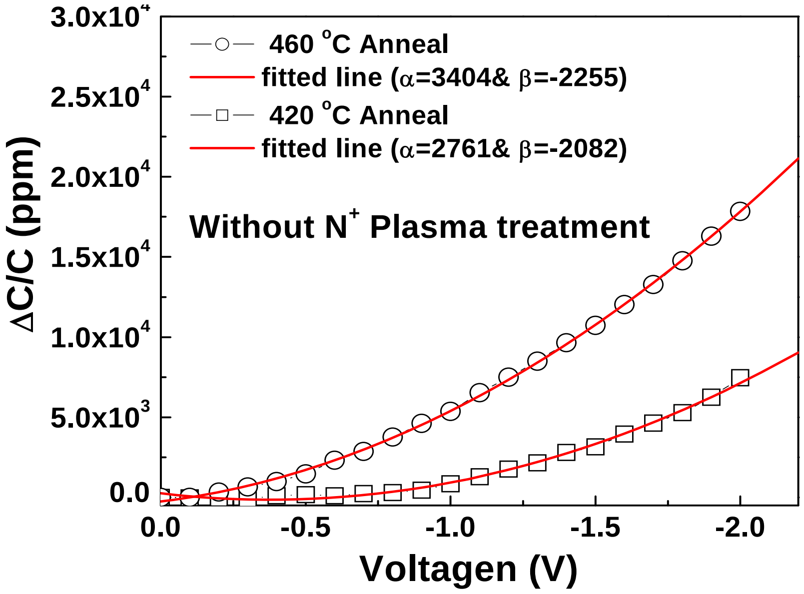
	HfO_2 [29]	Tb-HfO_2 [8]	Al_2O_3-HfO_2 [10]	Nb_2O_5 [16]	Previous paper for TiNiO [30]	This Work
Top metal	Ta	Ta	TaN	Ta	Al	Ni
Lower metal	TaN	TaN	TaN	Ta	TaN	TaN
C Density (fF/μm^2)	13	13.3	12.8	17.6	14.3	17.1
J (A/cm^2) @25 °C	6×10^{-7} (2V)	1×10^{-7} (2V)	8×10^{-9} (2V)	7×10^{-7} (1V) 8×10^{-6} (2V)	$> 1\times10^{-4}$ (1V) $> 1\times10^{-3}$ (2V)	7.7×10^{-6} (1V) 5.6×10^{-5} (2V)
α (ppm/V^2)	831	2667	1990	—	—	3220
κ	~ 15	~ 20	~ 18	~ 30	—	~ 39
PDA Temperature	—	—	—	—	550°C	460°C



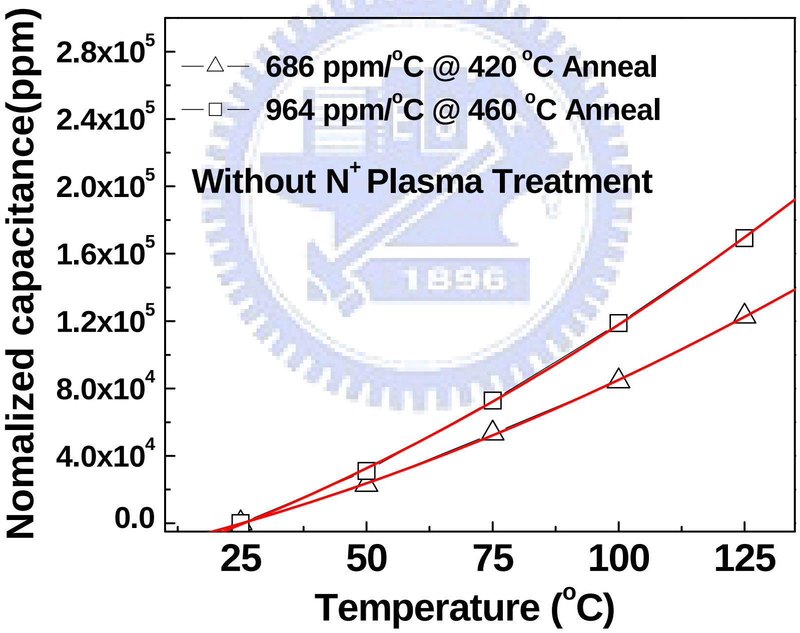
(a)

(b)

Figure 2-1(a) *C*-*V* and (b) *J*-*V* characteristics of Ni/TiNiO/TaN MIM capacitors processed at respective 420 and 460°C O_2 PDA.

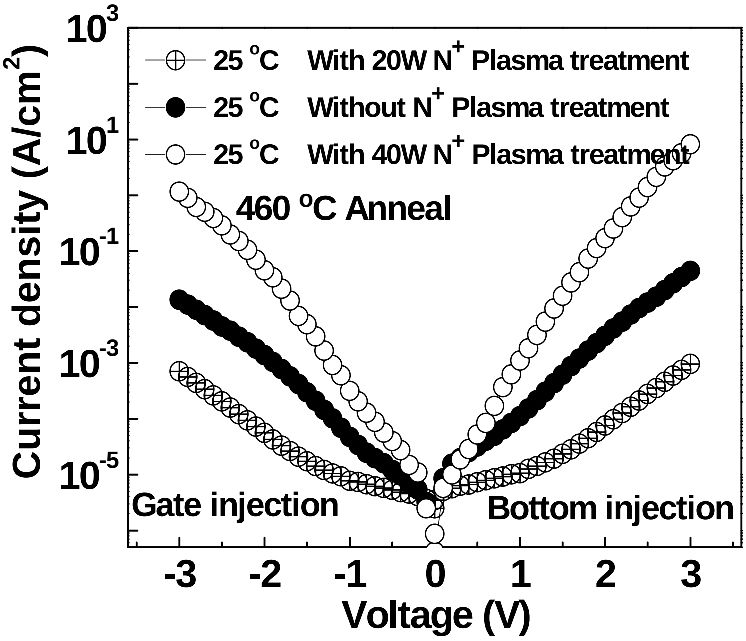


(a)

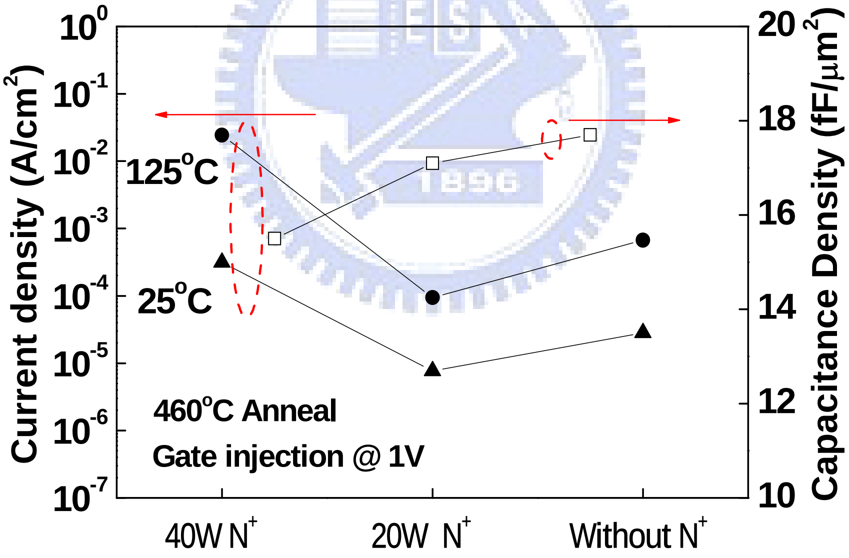


(b)

Figure 2-2 (a) $\Delta C(V)/C$-V and (b) *TCC* of Ni/TiNiO/TaN capacitors annealed at 420 and 460°C O_2 PDA.

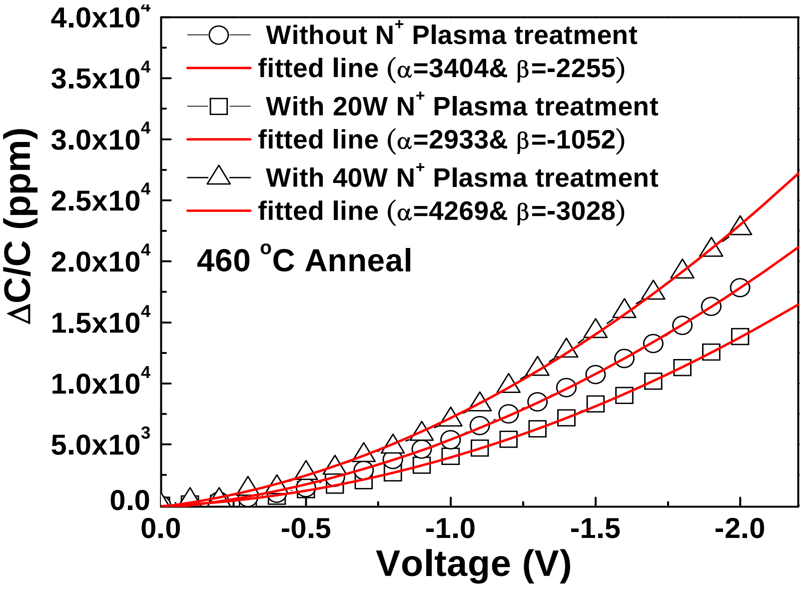


(a)

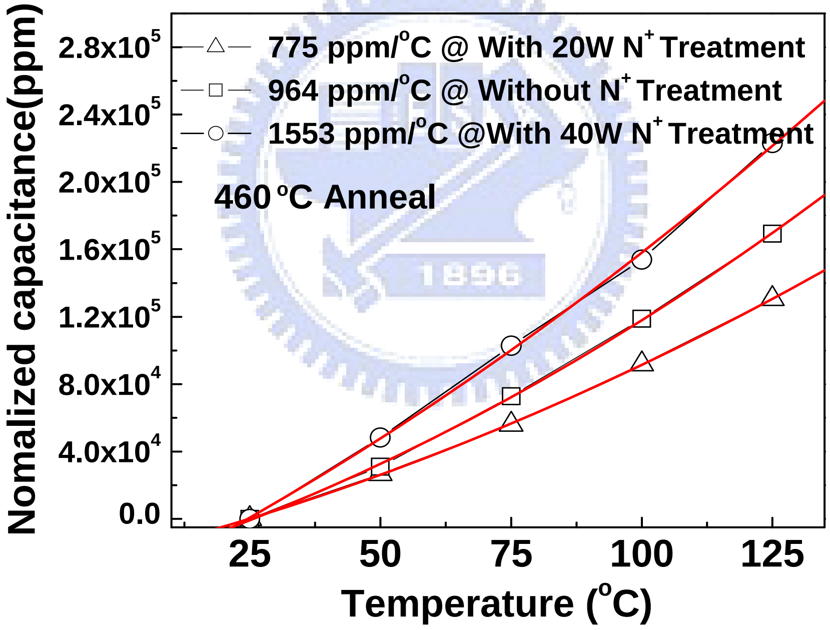


(b)

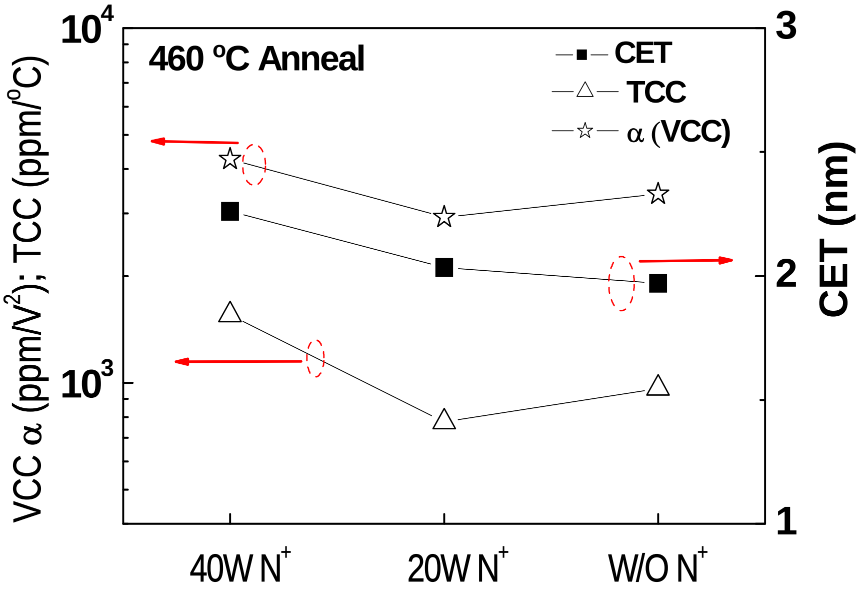
Figure 2-3 (a) *J*-*V* characteristics and (b) summarized *C*-*V* and *J*-*V* data of 460°C-PDA Ni/TiNiO/TaN MIM capacitors processed under different N$^+$ plasma treatment.


4.0x10^4
3.5x10^4
3.0x10^4
2.5x10^4
2.0x10^4
1.5x10^4
1.0x10^4
5.0x10^3
0.0
ΔC/C (ppm)
Without N$^+$ Plasma treatment
fitted line (α=3404& β=-2255)
With 20W N$^+$ Plasma treatment
fitted line (α=2933& β=-1052)
With 40W N$^+$ Plasma treatment
fitted line (α=4269& β=-3028)
460 °C Anneal
0.0
-0.5
-1.0
-1.5
-2.0
Voltage (V)

(a)


2.8x10^5
2.4x10^5
2.0x10^5
1.6x10^5
1.2x10^5
8.0x10^4
4.0x10^4
0.0
Nomalized capacitance(ppm)
775 ppm/°C @ With 20W N$^+$ Treatment
964 ppm/°C @ Without N$^+$ Treatment
1553 ppm/°C @With 40W N$^+$ Treatment
460 °C Anneal
25
50
75
100
125
Temperature (°C)

(b)



(c)

Figure 2-4 (a) Δ*C*(*V*)/*C*-*V*, (b) *TCC*, and (c) summarized α, *TCC*, and CET of Ni/TiNiO/TaN capacitors under different N^+ plasma treatment and 460°C O_2 PDA.

Chapter 3

High Performance Ir/TiPrO/TaN MIM Capacitors for Analog ICs Application

3.1 Motivation

The technology evolution for Metal-Insulator-Metal (MIM) capacitors [5-23] requires higher capacitance density with low leakage current at evaluating temperature [1]. Besides, the MIM capacitors are also used for Analog/RF ICs and DRAM technology. Since the capacitance density equals $\varepsilon_0\kappa/t_\kappa$, the only method for higher density, without increasing unwanted leakage current by decreasing dielectric thickness (t_κ), is to use higher dielectric constant dielectric (κ) materials. One major drawback for higher-κ MIM device is the large leakage current due to low conduction band offset (ΔE_C) at evaluated temperature that leaks out the stored charge in capacitor ($Q=C\cdot V$). However, increasing dielectric constant (κ) usually leads to decreasing of ΔE_C with respect to the electrode. This is also the challenge of flash memory but unavoidable during IC operation due to large circuit density and high DC power dissipation due to leakage current. The possible solution is using high bandgap (E_G) dielectric to form the laminate [8] or multi-layer structure [10], but the overall κ value and voltage coefficient of capacitance (*VCC*) are largely degraded. Pr_2O_3 is one of attractive rare earth metal oxides with many merits such as large conduction band offset (ΔE_C~ 1 eV) [36], moderate dielectric constant (κ~15) and large bandgap (E_G ~4 eV) [36]. Furthermore, significantly larger Gibbs free energy of Pr_2O_3 (+106 kcal/mol) [37]-[39] in contact with silicon than that of TiO_2 (+7.5 kcal/mol), Ta_2O_5 (-52 kcal/mol), HfO_2 (+47 kcal/mol) and NiO (-51.4 kcal/mol) can avoid metal/oxide inter-diffusion or chemical reaction caused by oxygen exchange, which not only reduce the interfacial layer between dielectric layer and bottom electrode but also performs excellent thermal stability. Combining above advantages of high-κ Pr_2O_3 with the high dielectric constant of TiO_2 (~50), mixed TiPrO dielectric overcomes the issue of leakage current without scarifying capacitance density.

In this paper, we report Ir/TiPrO/TaN capacitors with capacitance density of 16 fF/μm^2 and further improved capacitance density of 20 fF/μm^2 using higher annealing temperature. High-κ values 26-32 were obtained in this work by using mixed $Ti_xPr_{1-x}O$(x~0.67). By using high-κ TiPrO with the ratio of Ti to Pr 2:1 and high work function electrode Ir, we can achieve high capacitance density of 16-20 fF/μm^2, and low leakage current of 7×10^{-9} A/cm^2 to 1.2×10^{-7} A/cm^2 at 25 ^oC at -1 V, small quadratic *VCC* (α) of 1720~2174 ppm/V^2, and small *TCC* of 532~758 ppm/^oC. The lower leakage shows improved quadratic *VCC* (α) and *TCC*, which are important for analog/RF functions. It would be important to note that the device shows large orders of magnitude lower thermal leakage at 25 ^oC and 125 ^oC at -1V than our previous work on TiTaO [19] and TiNiO [35], at comparable capacitance density. Such good device integrity is due to the mixed high-κ TiPrO (κ~26-32) with larger bandgap (E_G~4 eV), larger high-κ/Si conduction band offset (ΔE_C~1 eV) and larger Gibbs free energy (+106 kcal/mol) of Pr_2O_3.

3.2 Experimental

After depositing 2 μm SiO_2 on a Si wafer, the lower capacitor electrode was formed using PVD-deposited TaN/Ta bi-layers. The Ta was used to reduce the series resistance and the TaN served as a barrier layer between the high-κ TiPrO and the Ta electrode. The TaN was treated by NH_3 plasma nitridation at 100W to improve the bottom interface. The TaN layer with NH_3 surface nitridation [22]-[23] can improve electrode stability and prevent CET (capacitance equivalent thickness) degradation by forming interfacial TaON during post-deposition anneal (PDA). Then 14 nm thick $Ti_xPr_{1-x}O$ (x~0.67) dielectric layer were deposited on the TaN/Ta electrode by PVD respectively followed by 400 ^{o}C and 430 ^{o}C oxidation and annealing step to reduce the leakage current. Finally, Ir was deposited and patterned to form the top capacitor electrode. The fabricated devices were characterized by *C-V* and *J-V* measurements using an HP4155B semiconductor parameter analyzer and an HP4284A precision LCR meter.

3.3 Results and discussion

Figure 3-1 shows the *C–V* characteristics of Ir/TiPrO/TaN capacitors, which were processed differently. The capacitance density increased from 16 to 20 fF/μm^2 with increasing O_2 PDA temperature from 400 ^{o}C to 430 ^{o}C. In Figure 3-2(a) and 3-2(b), we perform the *J–V* characteristics of the TiPrO MIM capacitors with capacitance density of 16 fF/μm^2 and 20 fF/μm^2 respectively, measured at 25 and 125 °C. The good *J-V* and *C-V* characteristics are obtained with the use of high work function top electrode Ir (~5.27 eV) and nitrogen plasma (N^+) treatment on bottom electrode TaN. The nitrogen plasma (N^+) treatment reduces the interfacial layer growing between the bottom electrode TaN and TiPrO layer during oxygen annealing [22]-[23]. It is very important to note that the TiPrO MIM with capacitance density of 16 fF/μm^2 achieves the ITRS goals (at year 2018) [1] of 10 fF/μm^2 density and $J/(C\cdot V) < 7\ \mathrm{fA}/(\mathrm{pF}\cdot V)$. This excellent result indicates TiPrO is a potential material candidate for future electrical device application.

To further evaluate the device performance, Figure 3-3(a) and 3-3(b) show the temperature-dependent *J-V* characteristics of TiPrO MIM capacitors at capacitance density of 16 and 20 fF/μm^2, respectively. The leakage current increases rapidly with increasing temperature; however, the high temperature operation is unavoidable for modern high performance IC due to the increasing power consumption. In addition, the unwanted interfacial layer between bottom electrode and high-κ dielectric layer would lead to surface roughness between them. The interface layer make the thermal leakage current of the electron bottom injection (voltage= 0~3 V) slightly larger than the leakage of the electron gate injection (voltage= 0~-3 V), which can be observed in Figure 3-2. Thus, we only perform the *J-V* characteristics under reverse bias in Figure 3-3.

The examination of device performance with comparable capacitance density at 25 ^{o}C is performed in Figure 3-4. We can see the leakage current of TiPrO MIM is significantly lower than TiO_2 MIM and our previous work TiTaO MIM and TiNiO MIM, at a comparable capacitance density. The lower leakage current of TiPrO MIM is due to the higher ΔE_C between metal and high-κ TiPrO interface, higher bandgap of high-κ TiPrO and larger Gibbs free energy of Pr_2O_3, which reduce the leakage current exponentially. We also plot $ln(J)$ versus $E^{1/2}$ relation in Figure 3-5. The temperature-dependent leakage current in MIM is typically governed by Schottky emission (*SE*) or Frenkel-Poole (*FP*) as:

$$J \propto \exp\left(\frac{\gamma E^{1/2} - V_b}{kT}\right) \qquad (3\text{-}1)$$

$$\gamma = \left(\frac{q^3}{\eta \pi \varepsilon_0 K_\infty}\right)^{1/2} \qquad (3\text{-}2)$$

The η is equal to 1 or 4 for FP or SE case and K_∞ is the high-frequency dielectric constant (=n^2). The refractive index n =2.3 for $Ti_xPr_{1-x}O$ (x~0.67) is reasonable by linear interpolation of the reported 2.57 for TiO_2 and 1.75 for Pr_2O_3. From Figure 3-5, the leakage at 25 °C from Ir top electrode on TiPrO/TaN is ruled by *SE* at low field and *FP* at high field by trap-conduction. Besides, the leakage at 125 °C is also dominated by SE at low field and FP at high field. This result would be due to the large ΔE_C of TiPrO and the larger energy barrier ϕ_b of Ir electrode. The different slopes γ, for the *SE* and *FP* cases arise from the different energy barriers ϕ_b, corresponding to the work function of the metal-electrode/dielectric in the *SE* case or the trap energy level in the dielectric for the *FP* case.

Since the conduction mechanism at high electric field for Ir electrode on TiPrO is governed by Frenkel-Poole Emission, we plotted the *ln(J/E)-1/KT* relation of TiPrO in Figure 3-6(a) to extract the trapping level. The larger Gibbs free energy of Pr_2O_3 (+106 kcal/mol) contacted with silicon avoids metal/oxide inter-diffusion. Above reason indicates the interfacial trap density of TiPrO (between dielectric and electrode) would be smaller than that of other dielectrics, such as TiTaO and TiNiO. Thus, the trapping energy in the TiPrO dielectric will be larger than TiTaO (~0.3 eV) [19] and TiNiO [35]. Besides, the binding energy between Praseodymium and Oxygen (928 eV~970 eV) [40] is significantly larger than the binding energy between Nickel and Oxygen (855 eV~861 eV) [41] and that between Tantalum and Oxygen (~530 eV) [42], which causes stronger binding between Praseodymium and Oxygen atoms [66]. This indicates the more complete oxidation of the dielectric film which leads to its better dielectric properties than that of other dielectrics, such as TiNiO, TiTaO and TiO_2.

For illustration, we also plot this relation of our previous work TiNiO MIM in Figure 3-6(b). The trapping energy of dielectric was extracted using *FP* conduction theory [64]. During *FP* conduction, trapped charge carriers hop between potential wells (from a discrete trap level to the conduction band) that define the trap states, and an applied electric field enhances the hopping rate because of the barrier-lowering effect. From the slope of the ln(J/E) vs $1/kT$ plot, the trapping energy under a specific electric field can be obtained. Compared with Figure 3-6(a) and 3-6(b), the trapping energy of TiPrO about 0.43 eV is significantly larger than the trapping level of TiNiO by about 0.17 eV. This result also explains why TiPrO MIM can achieve near 2.5 orders of magnitude lower leakage current at -1V at 125 °C than TiNiO MIM, which is shown in Figure 3-6(c). On the other hand, the current flow which increases exponentially with the square root of the applied voltage for electric fields is usually ascribed to Schottky emission [64]. To determine schottky barrier height, it is common to make a $\ln(J/T^2)$ vs $E^{1/2}$ plot. This curve will be a straight line, whose extrapolated intercept with $ln(J/T^2)$ axis at E=0 gives value "x" (the zero electric field intercept). From the x value, the schottky barrier height can be calculated as followed:

$$\phi_b = x(kT/q) \tag{3-3}$$

In Figure 3-7, the *SE* barrier height (ϕ_b) at 125 °C was extracted from $ln(J/T^2)$-$E^{1/2}$ plot. The value for ϕ_b is 1.53 eV for TiPrO device at 125 °C with Ir top electrode.

VCCs are important parameters for MIM capacitor applications, and can be obtained by fitting the measured data with a second order polynomial equation of $C(V) = C(\alpha V^2 + \beta V+1)$, where C is the zero-biased capacitance, α and β represent the quadratic and linear voltage coefficients of capacitance, respectively. Figure 3-8(a) shows $\Delta C/C$-V characteristics of Ir/TiPrO/TaN capacitors fitted by the above mentioned equation. The lower leakage using high ϕ_m (Ir) also improves ΔC/C, and VCC-α due to the trap-related mechanism [7], [13], [14]-[15]. It should be noted that since linear VCC-β can be cancelled by circuit design [31], α is important for Analog/RF functions and it is strongly dependent on electric filed and dielectric physical thickness. To the best of our knowledge, the MIM capacitor with combined higher ϕ_m and higher κ dielectric is the only method to achieve lower thermal leakage and better VCC-α simultaneously without sacrificing capacitance density in multi-layer or laminate structure. Figure 3-8(b) shows the normalized capacitance versus measured temperature (*TCC*) of MIM capacitor for capacitance density 16 fF/μm^2 and 20 fF/μm^2, respectively. We can find the *TCC* showed increase with the increase of the measured temperature [20].

Amorphous dielectrics like TiPrO have some advantages over crystalline materials including low processing thermal budget, conventional electrode, high uniformity and scalability to very thin layers, which is suitable for BEOL and manufacture. Table 3-1 summarizes important device data for MIM capacitors with various high-κ dielectrics and work-function metals. The thermal leakage decreases largely with increasing ϕ_m of metal electrode from TaN to Ir. High 16~20 fF/μm^2 density, reasonable quadratic VCC-α of 1702~2174 ppm/V^2 and low 7×10^{-9}~1.2×10^{-7} A/cm^2 leakage current at 25 ^{o}C at -1 V are simultaneously measured in Ir/TiPrO/TaN devices, which are comparable with or better than the best reported data in literature [1]. In summary, amorphous dielectric TiPrO shows good thermal stability, leakage current, and scalability to very thin layers issue. Besides, TiPrO is also the better amorphous dielectric material than TiO_2, TiTaO and TiNiO.

3.4 Conclusion

Due to large conduction band offset (~1 eV), large bandgap (~4 eV), large Gibbs free energy (~106 kcal/mol) of Pr_2O_3, large binding energy of Pr-O (928 eV~970 eV) and high dielectric constant (~50) of TiO_2, the mixed high-κ TiPrO is a potential material candidate for electronic devices. Dielectric material TiPrO shows its excellent amorphous material properties and gives enough high κ value (κ~26-32). By applying the good properties to our MIM device, the device not only shows apparently lower thermal leakage than other dielectric MIM at comparable capacitance density but also meets the ITRS requirement. Such good device integrity indicates TiPrO dielectric is attractive as a very promising dielectric material for Analog/DRAM applications.

Table 3-1. Comparison of important device data for MIM Ir/TiPrO/TaN capacitor with various high-κ dielectrics and work-function metals.

	ITRS @2018	Tb-HfO_2 [8]	Al_2O_3-HfO_2 [10]	Nb_2O_5 [16]	TiTaO [19]	TiNiO [35]	**This work**	
Process Temp. (^{o}C)	—	420	420	420	400	400	400	430
Top metal	—	Ta	TaN	Ta	Ir (5.3 eV)	Ni (5.1 eV)	Ir*(5.3 eV)	Ir*(5.3 eV)
Lower metal	—	TaN	TaN	Ta	TaN	TaN	TaN	TaN
C Density ($fF/\mu m^2$)	10	13.3	12.8	17.6	23	17.1	**16**	**20**
J (A/cm^2) @25 ^{o}C	1×10^{-8} (1V)	1×10^{-7} (2 V)	8×10^{-9} (2 V)	7×10^{-7} (1 V) 8×10^{-6} (2 V)	2×10^{-6} (1 V) 2×10^{-5} (2 V)	7.7×10^{-6} (1 V) 5.6×10^{-5} (2 V)	7×10^{-9} (1 V) 1.1×10^{-7} (2 V)	1.2×10^{-7} (1 V) 7.4×10^{-6} (2 V)
J (A/cm^2) @125 ^{o}C	—	2×10^{-7} (2 V)	6×10^{-9} (1 V) 5×10^{-8} (2 V)	4×10^{-7} (1 V) 1×10^{-5} (2 V)	—	—	3.6×10^{-7} (1 V) 7.2×10^{-6} (2 V)	5.8×10^{-7} (1 V) 3.8×10^{-4} (2 V)
J/(C•V) (fA/[pF•V])	< 7	37.9 @2 V	3.1 @2 V	14.5 @1.5 V	870 @1 V	4530 @1 V	3.45 @1 V	45 @1 V

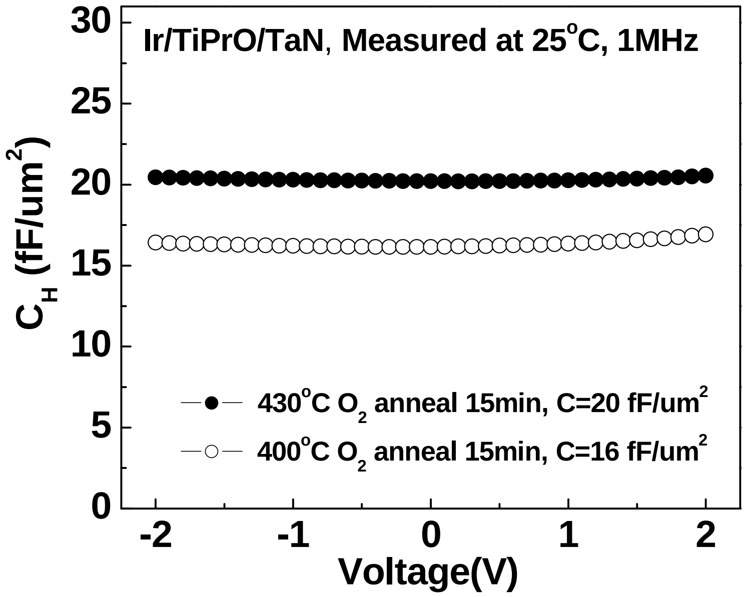
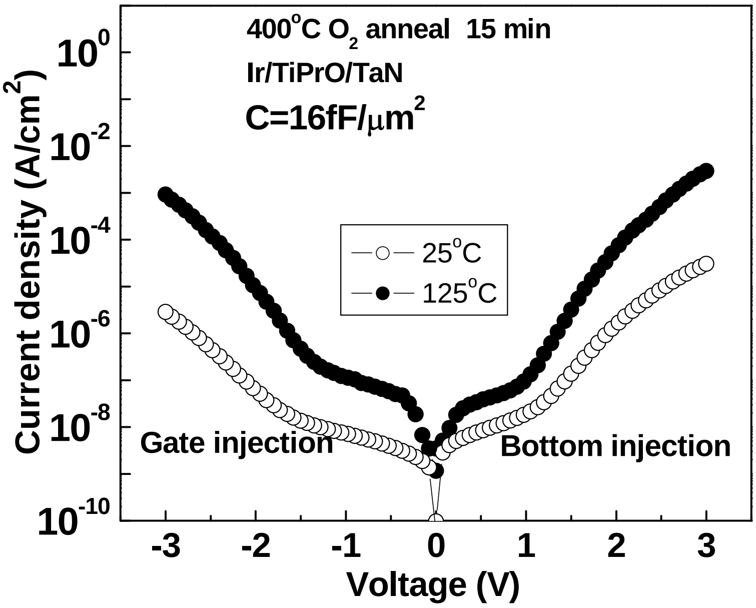
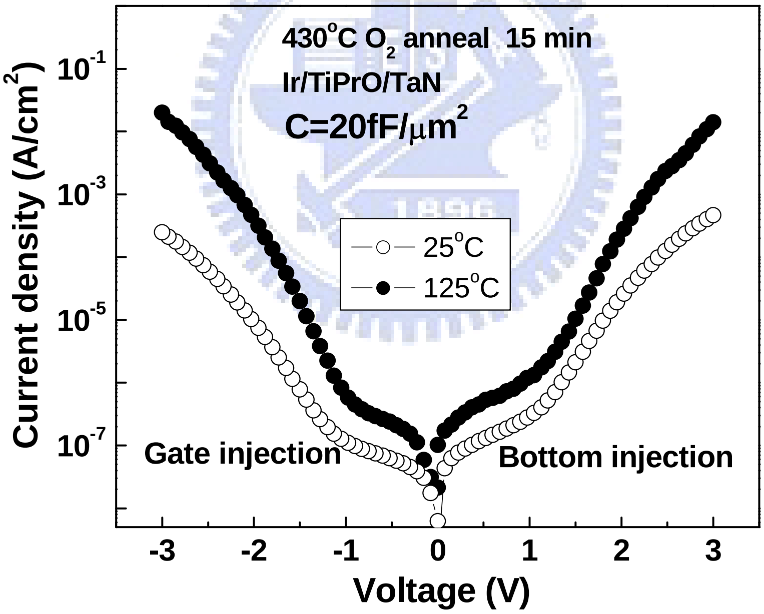


Figure 3-1 *C-V* characteristics of Ir/TiPrO/TaN capacitors with different annealing temperature measured at 1 MHz.

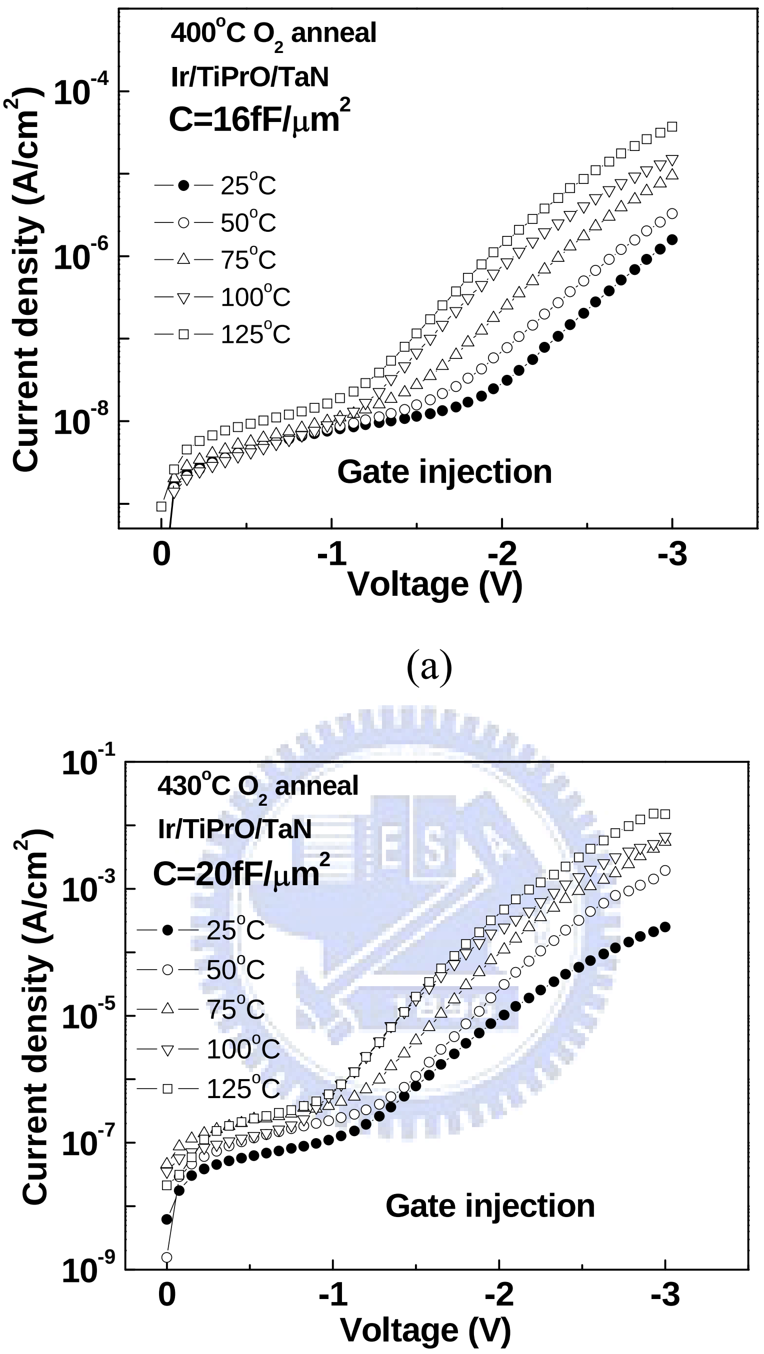


(a)



(b)

Figure 3-2 *J-V* characteristics of Ir/TiPrO/TaN capacitors with different capacitance density (16 fF/μm^2 and 20 fF/μm^2) measured at (a) 25 °C and (b) 125 °C, respectively.



(a)

(b)

Figure 3-3 *J-V* characteristics of Ir/TiPrO/TaN capacitors for capacitance density with (a) 16 fF/μm^2 and (b) 20 fF/μm^2 measured from 25 ^{o}C to 125 ^{o}C, respectively.

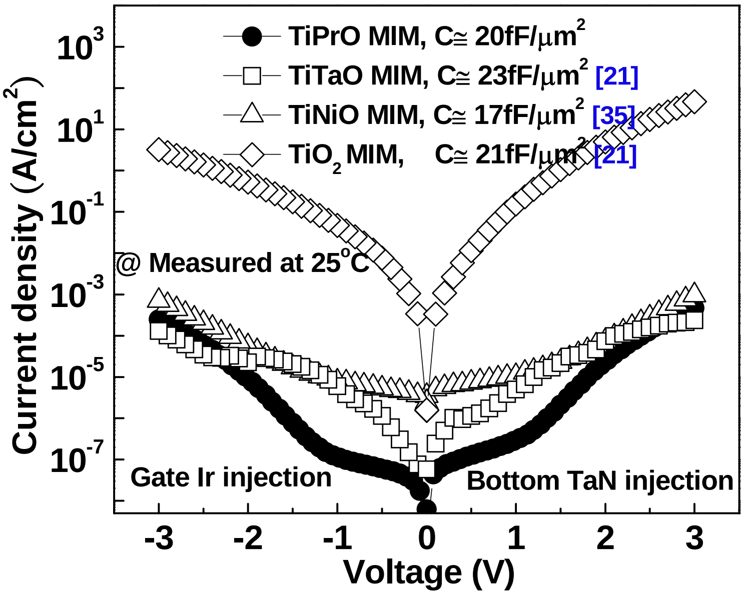


Figure 3-4 The comparisons of *J-V* for different high-κ material capacitors, at comparable capacitance density. The leakage current of TiPrO MIM is significantly lower than TiO_2 and previous work TiTaO and TiNiO MIM.

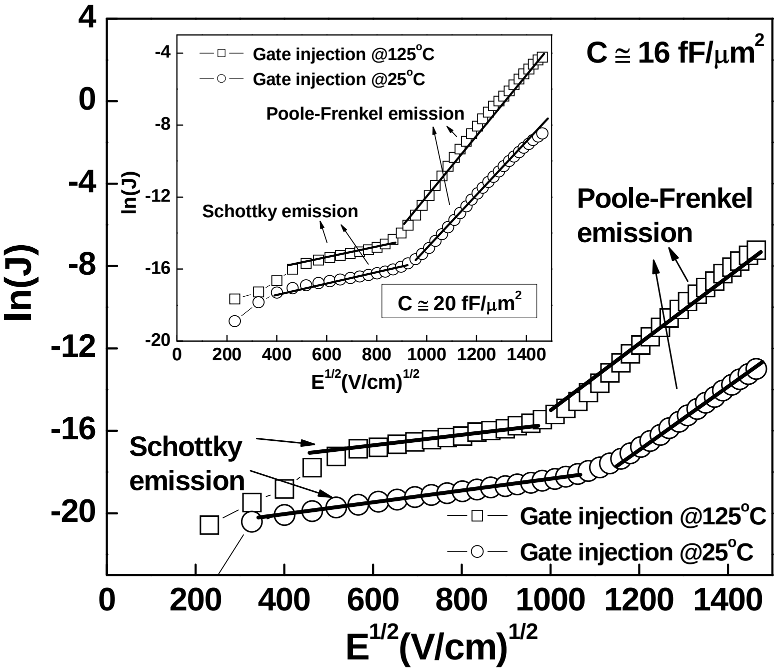
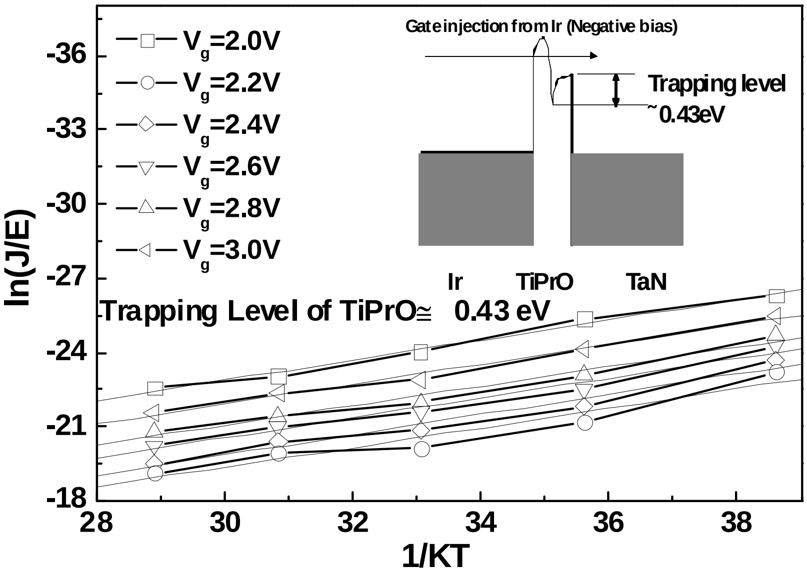
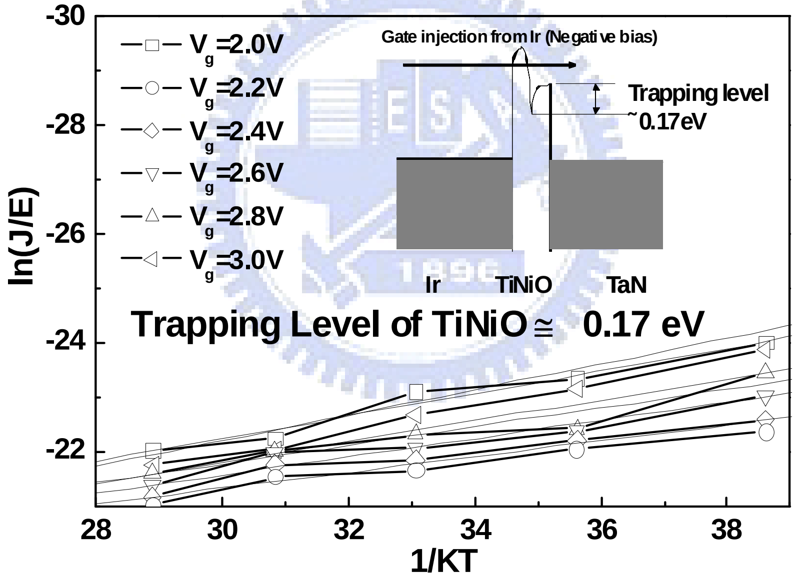


Figure 3-5 Plot of *ln(J)* versus $E^{1/2}$ under electron injection from top electrode for Ir/TiPrO/TaN capacitors with capacitance density of 16 fF/μm² and capacitance density of 20 fF/μm² is shown in the inserted figure. The SE emission fitting at low electric field and the FP emission fitting at high electric field are measured at 25 °C and 125 °C, respectively.



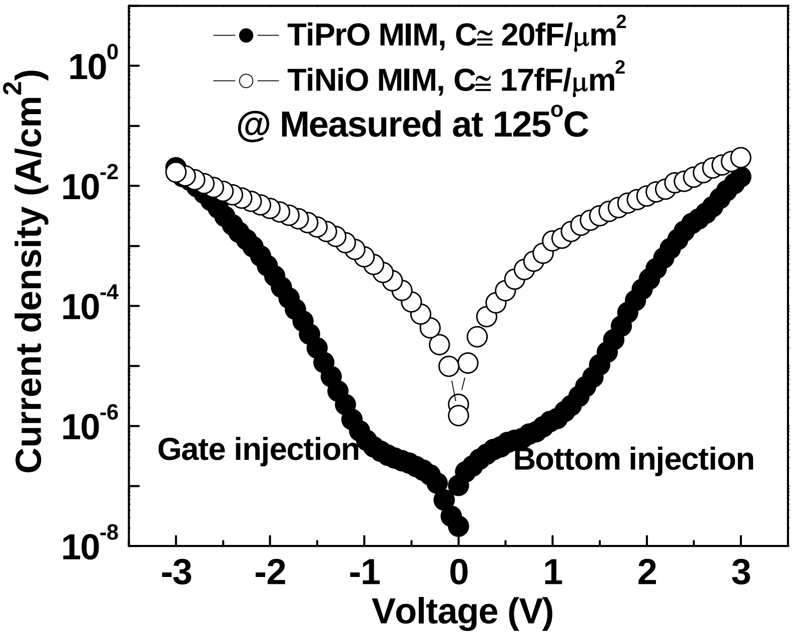
Vg=2.0V
Vg=2.2V
Vg=2.4V
Vg=2.6V
Vg=2.8V
Vg=3.0V
Gate injection from Ir (Negative bias)
Trapping level
~0.43eV
Ir
TiPrO
TaN
Trapping Level of TiPrO≅ 0.43 eV
ln(J/E)
-36
-33
-30
-27
-24
-21
-18
28
30
32
34
36
38
1/KT

(a)



Vg=2.0V
Vg=2.2V
Vg=2.4V
Vg=2.6V
Vg=2.8V
Vg=3.0V
Gate injection from Ir (Negative bias)
Trapping level
~0.17eV
Ir
TiNiO
TaN
Trapping Level of TiNiO≅ 0.17 eV
ln(J/E)
-30
-28
-26
-24
-22
28
30
32
34
36
38
1/KT

(b)



(c)

Figure 3-6 The FP conduction fitting at high field for (a) Ir/TiPrO/TaN capacitor and (b) Ir/TiPrO/TaN capacitor are shown. The leakage current measured at 125 °C for Ir/TiPrO/TaN and Ir/TiNiO/TaN MIM are also shown in (c).

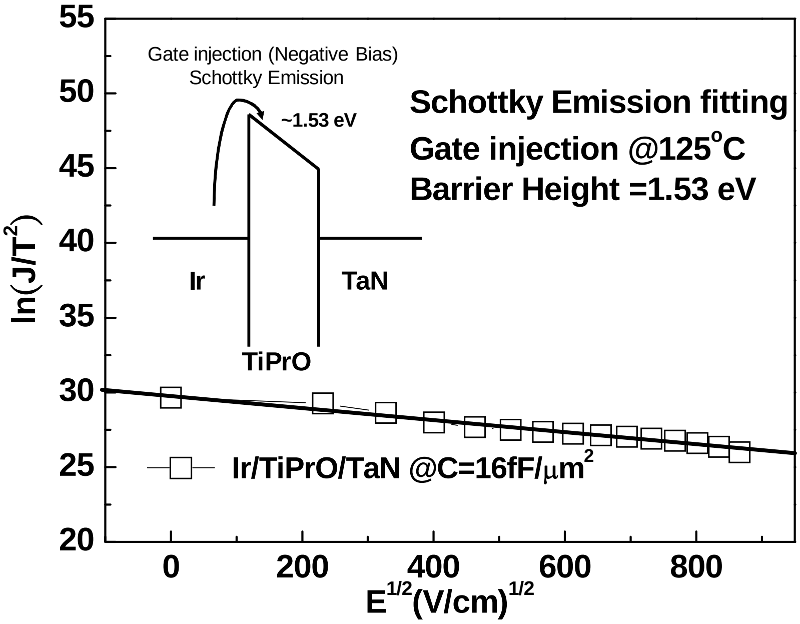
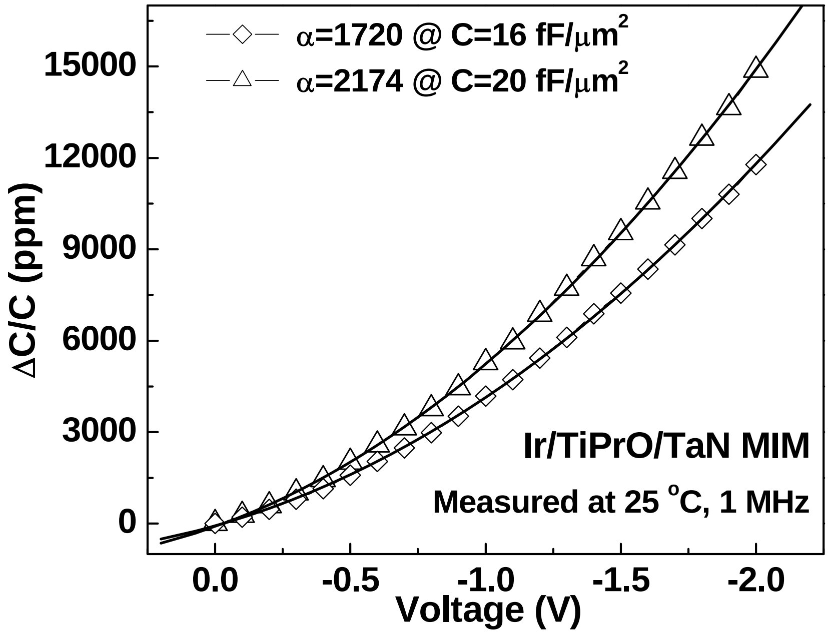
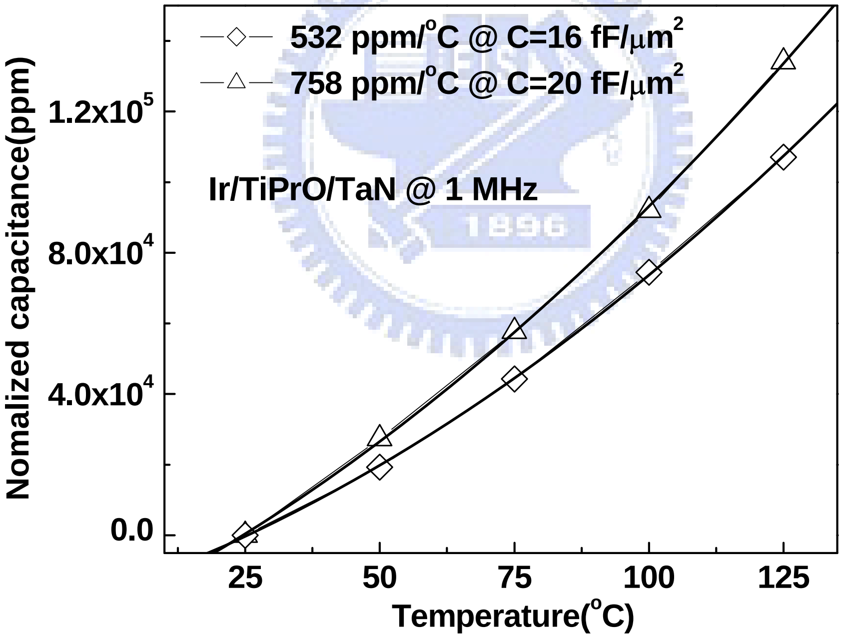


Figure 3-7 The SE emission fitting of Ir/TiPrO/TaN capacitors at low electric field.



(a)



(b)

Figure 3-8 (a) *ΔC/C -V* characteristics of Ir/TiPrO/TaN capacitors for different capacitance density. (b)The temperature-dependent normalized capacitance for Ir/TiPrO/TaN capacitors for different capacitance density.

Chapter 4

Impact of Ta_2O_5 doping on Electrical Characteristics of $SrTiO_3$ Metal-Insulator-Metal Capacitors

4.1 Motivation

High performance MIM capacitors which are essential for Microwave and RF circuit applications have become strong requirements in RF and Analog/Mixed-signal devices. For the requirement of RF application, the voltage coefficient of capacitance (VCC) is important for MIM capacitors. In addition, for the purpose of reducing IC chip size, greater capacitance densities for capacitors are necessary. Thus, the applications of high-κ dielectric materials into MIM capacitors are highly anticipated in the near future. To meet these requirements, many high-κ dielectrics used in MIM capacitors have been investigated (SiON (κ~4-7) [3]-[5], Al_2O_3 (κ=10) [13], HfO_2 (κ~22) [7]-[11], Ta_2O_5 (κ~25) [5], [12], [15] to Nb_2O_5 (κ~40) [16] or TaTiO (κ~45) [19]-[21]). $SrTiO_3$ (STO) is another potential candidate to achieve higher dielectric constant. It has the well-known perovskite-type structure, a nano-crystal phase and high κ value above 100 at 450°C O_2 annealing [22]. These merits make it an attractive candidate for DRAM [25]-[28], [46] application. Unfortunately, STO in amorphous structure has problems in MIM capacitors that the conduction band offset (ΔEc) can even be slightly negative [47] (~-0.1eV), the bandgap is narrower (~3.3 eV), and the VCC is not good enough. A low ΔEc and narrow bandgap lead to an unwanted leakage current for MIM devices at high temperature. On the other hand, although crystallized STO shows higher κ values and good device characteristics, the crystallized STO requires a heat treatment at 450~500^{o}C under an oxygen ambient [22], [25]-[28], [46]. This activation maximum temperature (>450^{o}C) cannot be permitted in backend integration. In this study, we first demonstrated the doping of Ta_2O_5 into STO can improve the analog characteristics of STO MIM capacitor effectively.

In the previous literatures, there have been rarely solutions to achieve high capacitance density larger than 10 fF/μm^2, while maintaining low VCC-α value [9], [20], [43]-[45], [48]-[50]. Recently, bi-layer structure SiO_2/HfO_2 MIM [9] can obtain very low VCC-α (VCC-α~ 14 ppm/V^2 at C <6 fF/μm^2); however, the capacitance density of SiO_2/HfO_2 MIM is strictly limited by the low-κ value of SiO_2. Besides, M. Kahn et al. proposed a solution to VCC-α improvement for STO capacitor by inserting an Y_2O_3 layer between STO/bottom electrode [45]. Although this STO-Y_2O_3 stack MIM improves the VCC-α of STO, the best results (VCC-α~ -750 ppm/V^2 at C ~10 fF/μm^2) still cannot meet our exception for RF application due to poor VCC-α. Reported from previous studies, Ta_2O_5 [5], [51] can achieve very low VCC-α (VCC-$\alpha \sim -9.9$ ppm/V^2), while preserving its desirable dielectric constant (κ~25). In this study, we first demonstrated the doping of Ta_2O_5 into STO can improve the analog characteristics effectively. We find that the VCC-α, capacitance density, leakage current, and stress stability could be improved after Ta_2O_5 doped into STO. For ITRS 2018 requirement, the MIM dielectric material must achieve a high capacitance density value (10 fF/μm^2) with good VCC-α (< 100) and low leakage currents density (6×10^{-7} A/cm^2). The VCC-α (~420 ppm/V^2) and high capacitance density (~20 fF/μm^2) were obtained in our work. It is important to note that *VCC* increases linearly with $1/t^2_{ox}$ [7], [9]. When we increase the thickness of the dielectric, the requirements for capacitance density value and VCC-α of ITRS 2018 could be easily achieved. And the major drawback (leakage current) of our work could also be improved considerably at the same time. The Ta_2O_5 doped STO MIM capacitor allows us to overcomes this drawback of conventional STO MIM capacitor [52] without sacrificing overall capacitance density and dielectric constant value. From the view of reliability, the MIM samples with Ta_2O_5 doped also show a durable stress behavior in our study.

In this study, the improvement on VCC in MIM capacitor by using amorphous Ta_2O_5 doped STO formed with low thermal budget (420^oC) is found. Besides, the leakage current and the stress behavior of the capacitance variation ($\Delta C/C$) under the constant voltage stress (CVS) are also improved. These all attribute to the combination of larger ΔE_C (~0.5 eV) [47], wider bandgap (4.5 eV) [47] and low VCC-α of Ta_2O_5 [5], [51].

4.2 Experimental

After depositing 2 μm SiO_2 on a Si wafer, the lower capacitor electrode was formed using PVD-deposited TaN (50nm)/Ta (200nm) bi-layers. Then, the TaN was treated by NH_3 plasma nitridation to improve the bottom interface. The lower TaN with NH_3 surface nitridation [20], [53] can improve electrode stability and prevent capacitance-effective-thickness (CET) increase by forming interfacial TaON during post-deposition anneal (PDA). The 15 nm thick $SrTiO_3$ doped with Ta_2O_5 dielectric layer were deposited by RF Sputter, in a mixed oxygen and argon (O_2/Ar = 1:4). And the deposition rate of RF sputter is 3: 1 ($SrTiO_3$: Ta_2O_5) from $SrTiO_3$ and Ta_2O_5 dielectric target, respectively. In the deposition process, the approach with co-sputter was used. By tuning the deposition rate, a simultaneously control of dielectric content ($SrTiO_3$: Ta_2O_5= 3: 1) can be achieved. The deposited rate was controlled by individual power supplies for the STO and Ta_2O_5 targets. A thermal budget of 420°C for 30 min was followed to repair the dielectric defects and reduce the leakage current. Finally, Pt deposited and patterned to form the top capacitor electrode. The fabricated devices were characterized by *C-V* and *J-V* measurements using the HP4284A precision LCR meter and the HP4155 semiconductor parameter analyzer.

4.3 Results and discussion

The *C–V* characteristics of pure STO MIM and Ta_2O_5 doped STO MIM are described in Figure 4-1, respectively. From Figure 4-1, we extract the corresponding high frequency (1 MHz) dielectric constant of 45 and 38. The capacitance densities are about 24.6 and 20 fF/μm^2, respectively. Figure 4-2 shows the free carrier injection model, which attributes the capacitance density variation to the injected carriers. The charge pass through the dielectric will follow the alternating signal (gate voltage) with a relaxation time that depends on the mobility of carrier, carrier density, and the defect in the dielectric. A longer relaxation time means that the carriers are more difficult to follow the alternating signal and to pass through the dielectric layer. When the bandgap and ΔEc of dielectric are smaller, the carrier injection will be higher and the charge relaxation time will be shorter, which leads to a larger capacitance variation. In Figure 4-3(a), compared with pure STO MIM capacitor, although the addition of Ta_2O_5 decrease the capacitance density and dielectric constant, a lower degree of capacitance density dispersion was observed in 0.01~1 MHz frequency range for the Ta_2O_5 doped STO MIM capacitor. This may be for the reason that the Ta_2O_5 doping improves the properties of the pure STO dielectric due to its higher ΔE_C (~0.5 eV) [47] and larger band gap (~4.5 eV) [47]. Besides, the interfacial states density and charge trapping of the overall dielectric film could be decreased considerably after the Ta_2O_5 addition [54].

Because of Ta_2O_5 characteristics, the relaxation time may be longer. Thus, we could assume that smaller capacitance variation in Figure 4-3(a) is explained by the model in Figure 4-2. The corresponding dielectric constant in 0.01 - 1 MHz frequency range is also shown in Figure 4-3(a). In Figure 4-3(b), Ta_2O_5 doped STO MIM capacitor also exhibits lower tanδ and smaller frequency dispersion than that of pure STO MIM. The *J-V* characteristics of control sample and Ta_2O_5 doped sample are shown in Figure 4-4. In comparison with pure STO MIM, the reduction of leakage current of Ta_2O_5 doped STO MIM capacitor has almost one order of magnitude. This improved leakage current might be due to the fewer defects in the Ta_2O_5 doped STO and the higher ΔE_C between metal and high-κ interface, which lower the leakage current exponentially.

VCCs are important parameters for MIM capacitors. These parameters can be obtained by fitting the measured data with a second order polynomial equation of $C(V) = C(\alpha V^2 + \beta V+1)$, where C is the zero-biased capacitance. The parameters of α and β represent the quadratic and linear voltage coefficient of capacitance, respectively. Linear VCC-β can be cancelled by circuit design [31]; however, VCC-α is strongly dependent on electric field and dielectric physical thickness. Figure 4-5 shows *ΔC/C-V* characteristics of MIM capacitors and the VCC-α extracted from the above mention equation. In Figure 4-5(b), the VCC-α of 420 ppm/V^2 was extracted for Ta_2O_5 doped STO MIM from -2V to 2V, which is also obviously smaller than that of pure STO MIM.

The improvement of VCC-α for STO doped Ta_2O_5 MIM capacitor attributes the addition of Ta_2O_5. It is need to note that deep traps will be formed after the subsequently annealing processes after Ta_2O_5 added. The deep traps would cause the *C-V* characteristic does not show perfect quadratic dependence when Ta_2O_5 doped. This problem could be solved while using advanced equipments to deposit the dielectric film. Figure 4-6 shows the normalized capacitance versus measured temperature (*TCC*) for pure STO and Ta_2O_5 doped STO MIM capacitors, respectively. *TCC* for Ta_2O_5 doped STO MIM capacitor also performs considerably better than that of pure STO MIM. We assume this thermal stability improvement is due to the larger bandgap of the dielectric and fewer defects in the dielectric after Ta_2O_5 doped.

To further evaluate the device performance for long-term use, the *C-V* and $\Delta C/C$-*V* characteristics of pure STO capacitors after CVS at 25°C are shown in Figure 4-7(a) and 4-7(b). We can observe the capacitance density decreases with the stress-voltage increasing. It is observed that an approximately reduction of 17.5% on capacitance density under CVS of -4V for the pure STO MIM. Therefore, a large degradation on $\Delta C/C$ after CVS seems to be suggested. Based on the free carrier injection model [55-56], these degrading effects of stress may be due to the shorter charge relaxation time caused by the more defects in the STO dielectric. The shorter charge relaxation time would lead to dielectric constant (ε) decreases. While the dielectric constant decreases, the capacitance density and $\Delta C/C$ will also degrade. On the other hand, compared with pure STO, Ta_2O_5 doped STO has fewer defects and certainly longer charge relaxation time. This is because Ta_2O_5 could considerably reduce the defect of overall dielectric [54]. The C-V and $\Delta C/C$-V characteristics of Ta_2O_5 doped STO capacitors after CVS at 25^{o}C are in Figure 4-8. After doping Ta_2O_5 into STO, a smaller reduction of 9% on capacitance density under CVS and less degradation of $\Delta C/C$ were achieved.

In Figure 4-9, a smaller degradation on *TCC* under CVS was also observed in Ta_2O_5 doped STO MIM capacitor. Since the *TCC* is also believed to relate with the free carrier injection model, less carrier injection leads to smaller overall capacitance variation for Ta_2O_5 doped STO MIM could be expected. The device reliability for 10 years operational span is also important. The operational condition is less than the breakdown voltage and investigated by the time-to-breakdown (t_{BD}) study. In Figure 3-10, a larger 2.5 V operation voltage for 10 years is achieved in Ta_2O_5 doped STO MIM capacitor, which was obtained from the t_{BD} plot by extrapolating to that time. Indeed, for a dielectric material, it is important to know its voltage stress stability, VCC-α and *TCC* and the operation reliability. The four parameters are closely linked and also been improved in our work. From above discussions, we certainly know the Ta_2O_5 with low VCC-α characteristic, wider bandgap and conduction band offset, in turn, improve the important electrical properties and strengthen the operational reliability of STO MIM capacitor.

Table 4-1 summarizes the important device data for MIM capacitors with various high-κ dielectrics. Compared with the previous studies, the approach first provided in this paper is the promising and effectively solution to improve VCC-α, while maintaining favorite capacitance density. The good device integrity of high capacitance density, low VCC-α, simple single dielectric process, and multi-functions are the strong merits using this novel high-κTa_2O_5 doped STO material.

4.4 Conclusion

A method on VCC-α improvement by Ta_2O_5 doping into higher permittivity STO dielectric has been developed successfully. Because Ta_2O_5 could considerably reduce the defect of overall dielectric, the leakage current is also obviously reduced. Compared with pure STO MIM capacitor, the experimental results for Ta_2O_5 doped STO MIM clearly demonstrated the benefits of Ta_2O_5 doping for the overall performance. For the consideration of long-term reliability, the Ta_2O_5 doped STO MIM capacitors also exhibits better stress degradation on the $\Delta C/C$ and *TCC* properties. Besides, a 10-years extrapolated reliability also pointed out the merits by using a large bandgap Ta_2O_5 doping dielectric. To sum up, Ta_2O_5 doped STO MIM capacitor in our study may be a promising material for RF and DRAM applications.

Table 4-1. Comparison of important device data for MIM capacitor with various high-κ dielectrics.

	HfO_2 [5]	SiO_2/HfO_2 Stack [9]	TiTaO [21]	TiLaO [43]	TiHfO [44]	$STO\text{-}Y_2O_3$ Stack [45]	**This work**	
Process Temp. (°C)	400	400	400	400	400	**500**	**420**	
C Density ($fF/\mu m^2$)	13	6	23	23	14.3	10	Pure STO **24.6**	STO doped Ta_2O_5 **20**
$\lvert\alpha\rvert$ (ppm/V^2)	607	14	3600	>3000	3392	**750**	**2130**	**510**
Dielectric Thickness (nm)	10	16	17	15	30	25	15	15

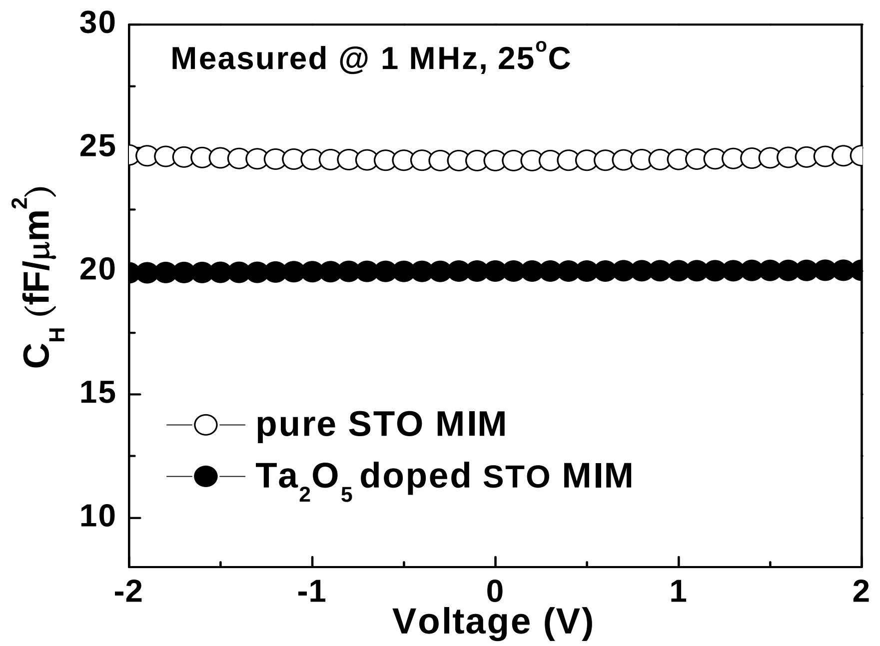


Figure 4-1 *C-V* characteristics of pure STO and STO doped Ta_2O_5 devices, measured at 1MHz.

$$\varepsilon^* = \varepsilon' - j\varepsilon'' = \varepsilon \frac{1 + j\omega\tau}{j\omega\tau + \frac{\tanh(A)}{A}}$$

$$A = \sqrt{\frac{1 + j\omega\tau}{D\tau}}$$

$$D = \frac{\mu k t}{q}$$

$$\tau \propto \frac{\varepsilon}{\mu n}$$

$$\tau = \frac{\varepsilon}{\sigma}$$

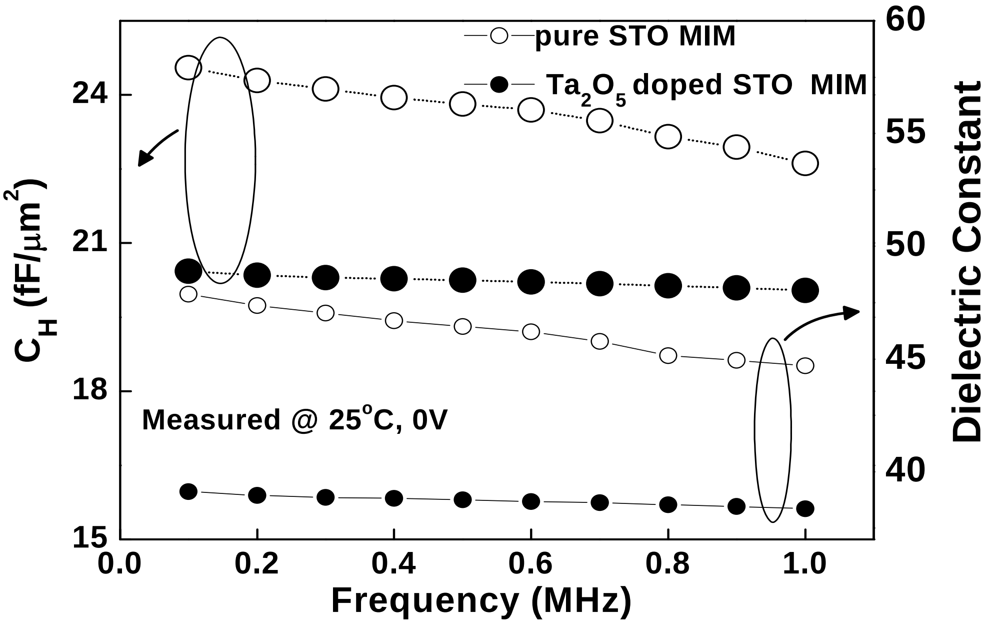
$$n = n_0 \exp\left(\frac{q\varphi_b}{kT}\right) \exp\left(\frac{\beta_S \sqrt{E}}{2kT}\right)$$

$$n_0 = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2} \left[\frac{-(E_C - E_F)}{kT}\right]$$

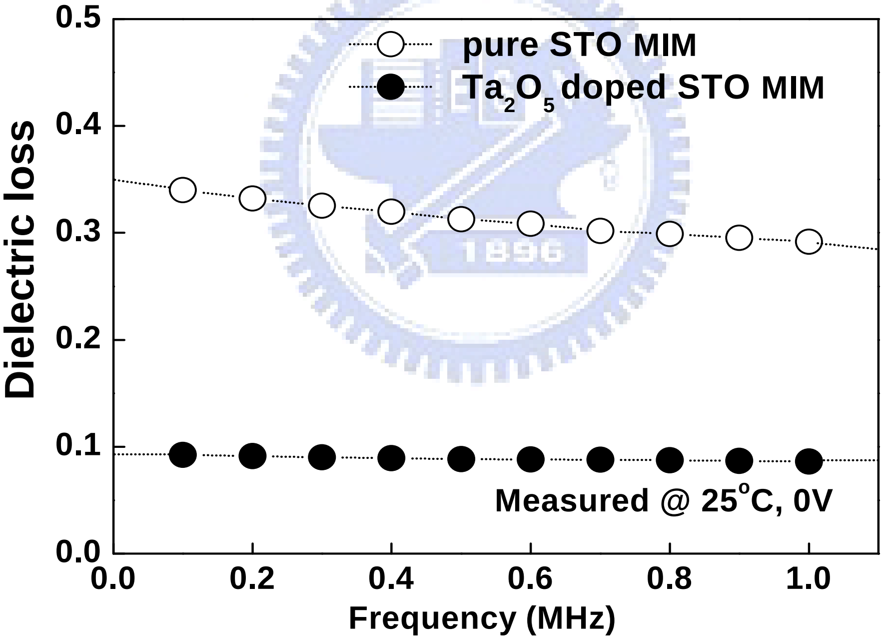
$$= N_c \left[\frac{-(E_C - E_F)}{kT}\right]$$

C: capacitance density
τ: relaxation time
μ: carrier mobility in insulator
σ: conductivity
T: temperature
t: thickness of insulator
n: carrier concentration
w: angular frequency
ε^*: the complex permittivity
ε': the real part of the complex permittivity
ε'': the imaginary part of the complex permittivity
ε: the dielectric constant
q: magnitude of electronic charge
ϕ_b: Schottky barrier height
β_S: β factor in Schottky emission

Figure 4-2 Free carrier injection model.



(a)



(b)

Figure 4-3 (a) Capacitance density at zero bias (0V) and corresponding dielectric constant. (b) tanδ at 0.01 - 1 MHz frequency range for pure STO and STO doped Ta_2O_5 devices.

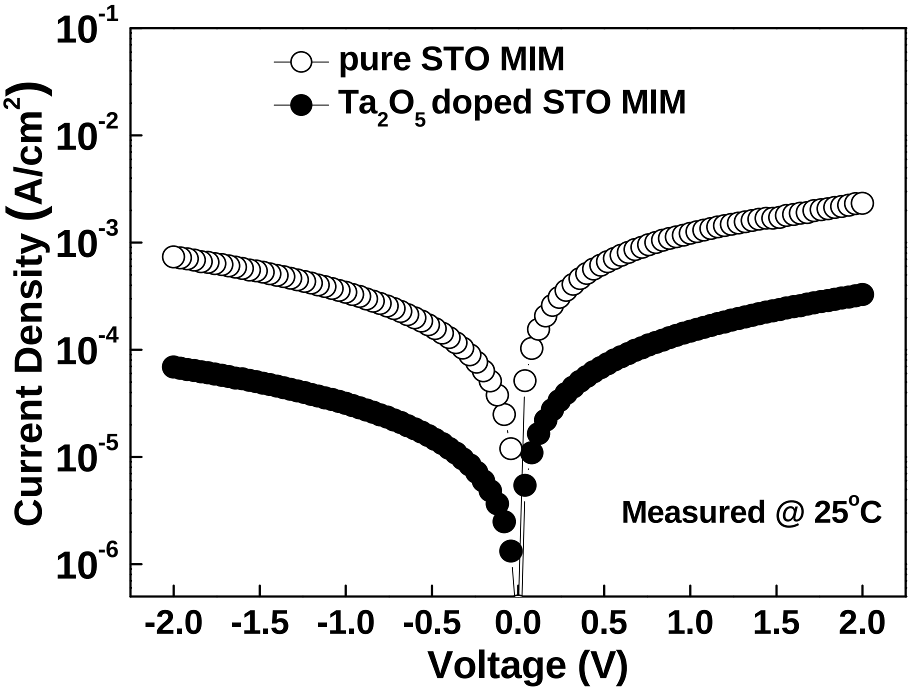


Figure 4-4 *J-V* characteristics for pure STO and STO doped Ta_2O_5 devices measured at 25°C.

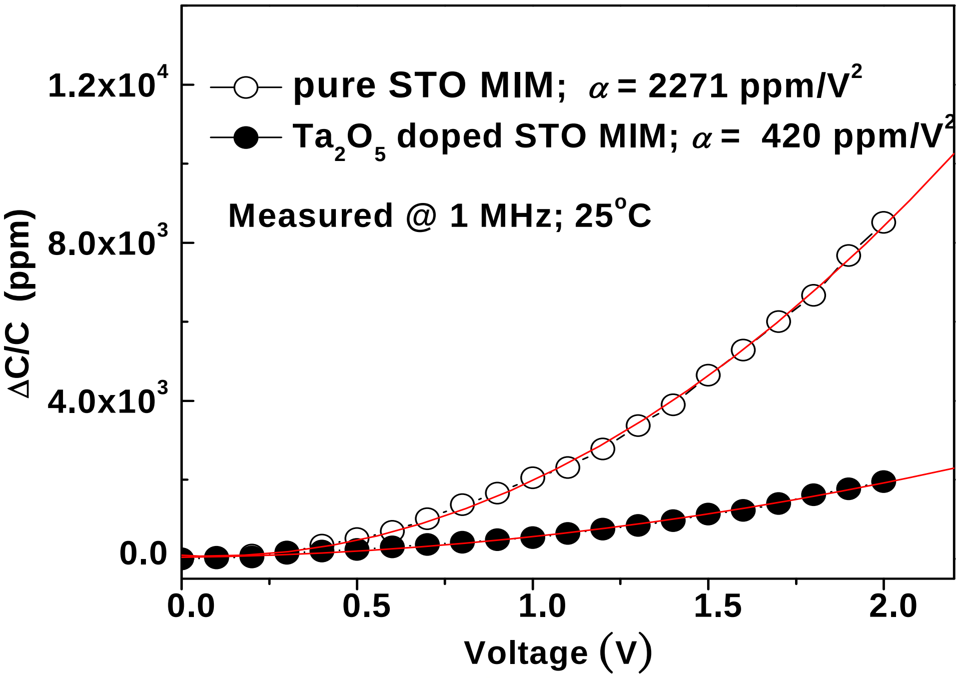


Figure 4-5 *ΔC/C -V* characteristics of pure STO and STO doped Ta_2O_5 devices.

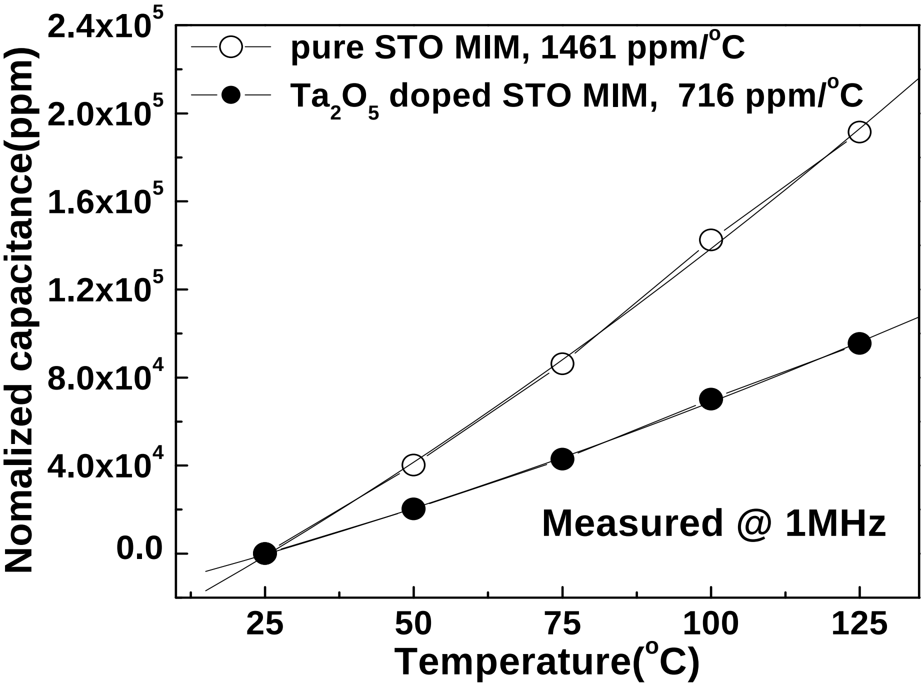
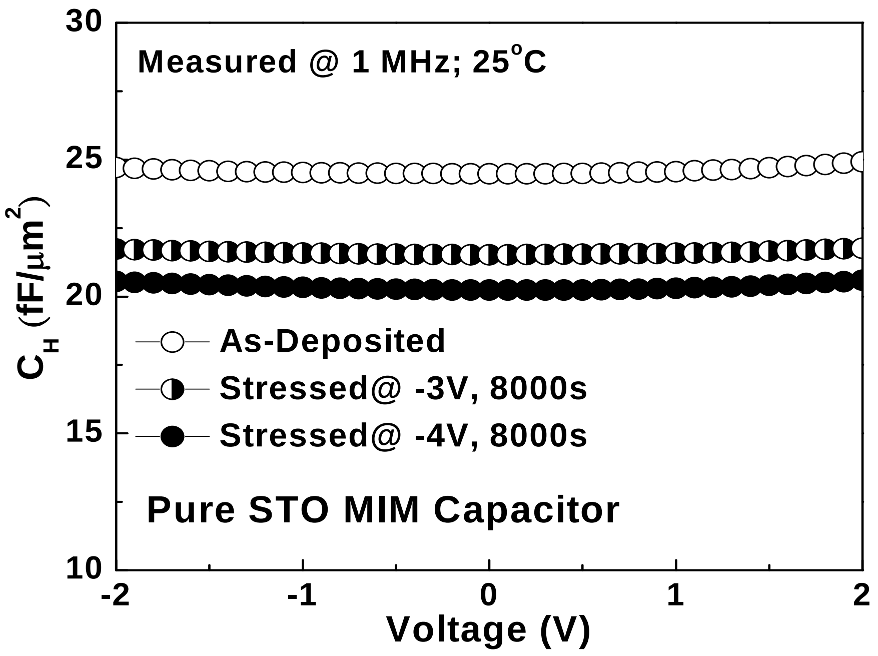
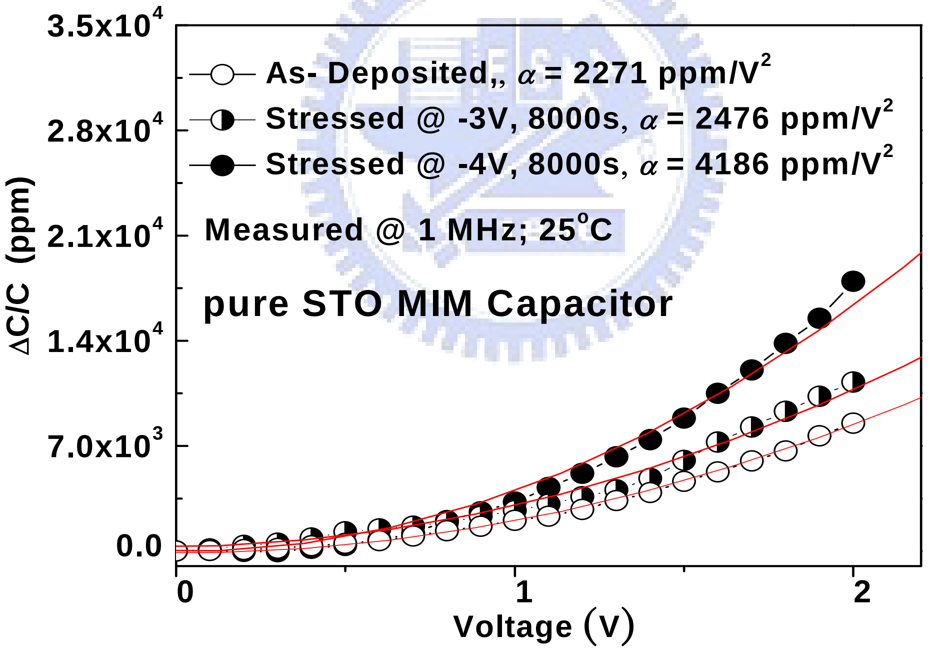


Figure 4-6 *TCC* characteristics of pure STO and STO doped Ta_2O_5 devices.

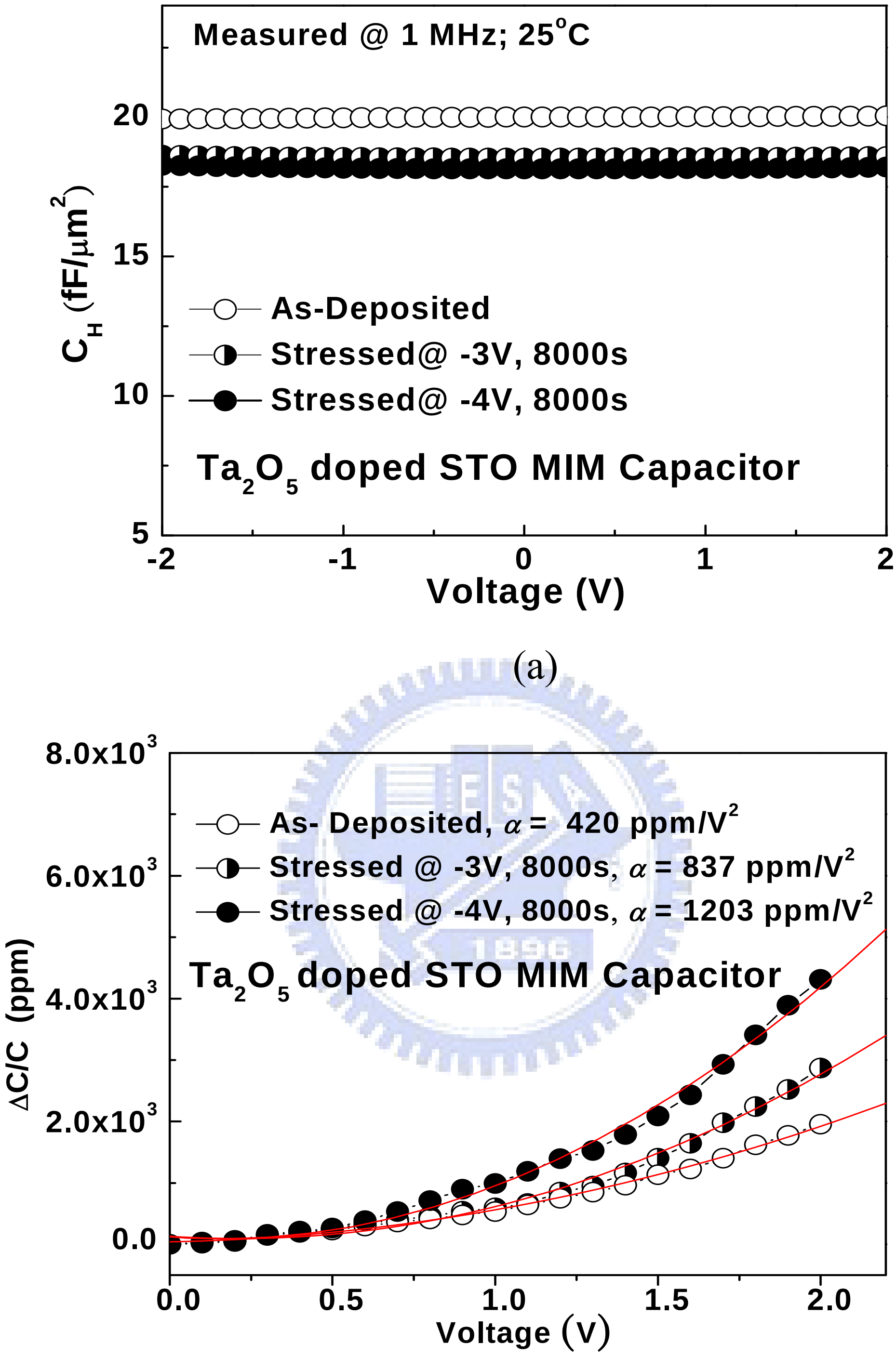


(a)



(b)

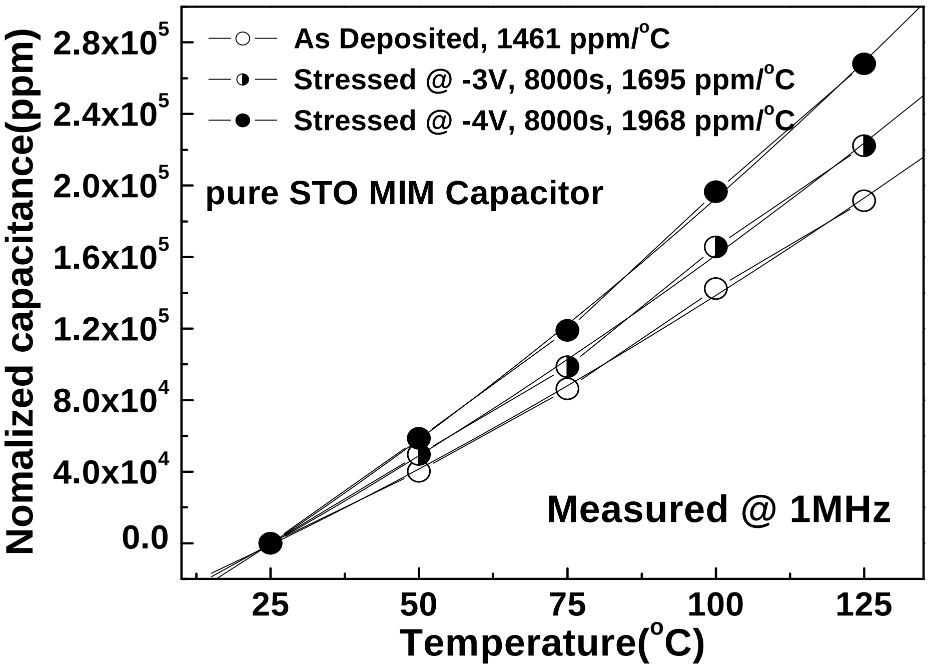
Figure 4-7 (a) *C-V* and (b) Δ*C/C-V* characteristics after CVS at 25°C for pure STO MIM capacitor, respectively.



(a)

(b)

Figure 4-8 (a) *C-V* and (b) Δ*C/C-V* characteristics after CVS at 25°C for STO doped Ta_2O_5 MIM capacitor, respectively.



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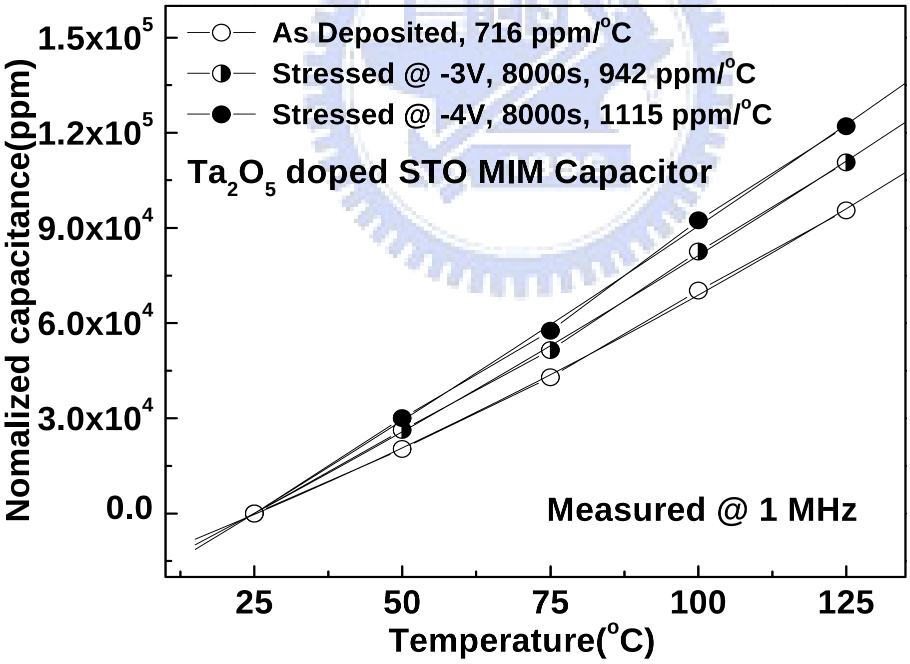


(b)

Figure 4-9 *TCC* characteristic of (a) pure STO and (b) STO doped Ta_2O_5 MIM capacitors, respectively.

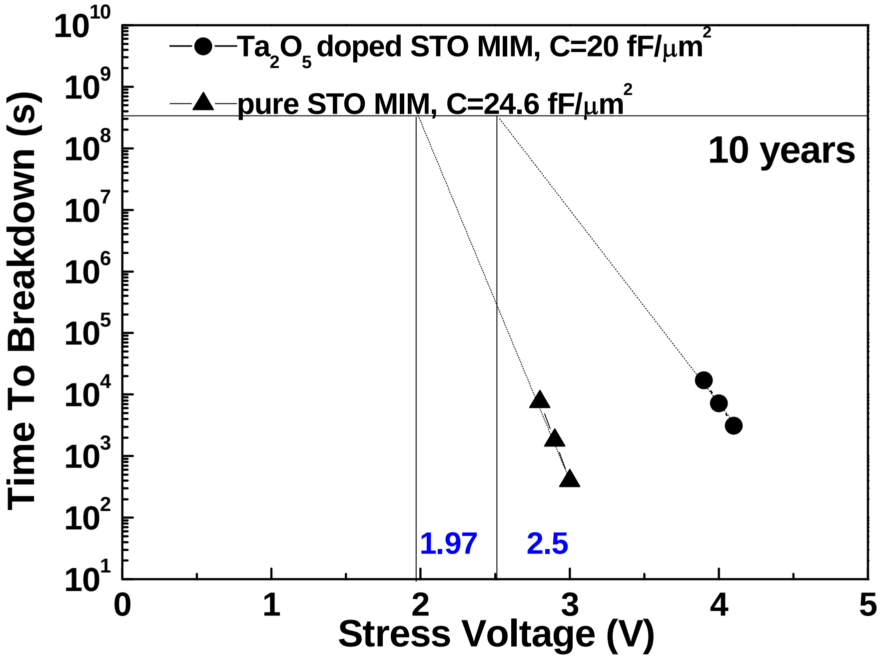


Figure 4-10 A comparison on the extrapolated operation voltage of 10-years life time for STO and STO doped Ta_2O_5 MIM capacitor.

Chapter 5

RF TaN/$SrTiO_3$/TaN MIM Capacitors with 35fF/μm^2 Capacitance Density

5.1 Motivation

Continuous down-scaling of component size is the technology trend for VLSI, which is important to reduce the die size and chip cost. For RF ICs, the active MOSFETs scale down by 70% in length every 2 years and also give higher RF gain and lower noise. However, the passive RF metal-insulator-metal (MIM) capacitor scales down at a much slower rate and consumes a large portion of the whole die area. Therefore, it is necessary to increase the capacitance density ($\varepsilon_0\kappa/t_d$) for smaller device area of RF capacitors that are widely used for impedance matching, DC blocking and filtering in RF ICs. To achieve this goal, high dielectric constant (κ) material is required since the decreasing dielectric thickness (t_d) will exponentially increase the undesired leakage current. Therefore, high-κ dielectric has been continuously evolving from SiON (κ~4-7) [2], [6], [55], Al_2O_3 (κ=10) [13], [56]-[57] and HfO_2 (κ~20) [7] or Ta_2O_5 (κ~24) [12], [14], [58] according to International Technology Roadmap for Semiconductors (ITRS) [1]. For κ value larger than 25, ternary dielectric is needed and we have previously shown good RF characteristics of MIM capacitors using TaTiO (κ~45) [19]-[21]. In this study, we have further developed high performance RF MIM capacitors with the very high-κ Strontium Titanate oxide ($SrTiO_3$). The $SrTiO_3$ (STO) is also listed in future DRAM manufacturing roadmap due to its high κ value of ~300 and paraelectricity (no fatigue or aging problem) [59]. We report the very high density of $35fF/\mu m^2$, small capacitance reduction of 4% from 100 KHz to 10 GHz and small leakage current of 1×10^{-7} A/cm^2 for TaN/STO/TaN MIM capacitors. Such excellent results are due to the very high κ value of 169. Such large capacitance density can drastically reduce the area of current foundry-provided RF capacitor by ~35 times with additional advantages of full process compatibility to current VLSI line and capable to integrate with DRAM for multi-functional system-on-chip (SoC)..

5.2 Experimental

After depositing thick isolation SiO_2 on standard Si wafers using VLSI back-end process, the TaN/Ta bi-layer was deposited on SiO_2/Si-substrate by sputtering and patterned to form the bottom capacitor electrode. Such bi-layer structure with thick Ta is needed to reduce the RF ohmic loss. To further improve the diffusion barrier property, the TaN was treated by NH_3 plasma nitridation. Such nitrogen-plasma (N^+) nitridation is important to reduce the leakage current and improve the capacitance density. Then 43 nm thick STO dielectric layer was deposited by RF sputtering with ceramic target in a gas mixture of O_2/Ar, followed by subsequent 450^{o}C post-deposition anneal (PDA) for 30 min ~ 1 hour under oxygen (O_2) ambient. It is important to notice that the device performance improvements with N^+ nitridation are due to the reduced interfacial TaON formation on TaN during PDA under O_2, as measured by secondary ion-mass spectroscopy (SIMS). However, such O_2 PDA is needed to reduce the oxygen deficiency in STO and improve the trap-assisted tunneling leakage current via defects in TaON. Finally, the TaN/Al metal was deposited and patterned to form both top capacitor electrode and RF transmission line. The fabricated RF MIM capacitors were characterized using HP4284A precision LCR meter to 1 MHz, and the HP8510C network analyzer for S-parameters measurement to 10 GHz. The measured S-parameters were followed by standard de-embedding procedure using a dummy open device [57], [60]-[62]. The series parasitic impedances in RF transmission lines are also de-embedded using a through dummy device [21], [60]-[62]. The RF frequency capacitance value was extracted from measured S-parameters using an equivalent circuit model [57], [60].

5.3 De-embedding Theory

When circuits or devices work at high frequencies, many parasitic effects will happen. For example, a signal applied on one metal line, the potential of this metal line at any point is equal if the wavelength of signal is long enough, compared with the metal line. However, the potential of the metal line at any point will be different when the wavelength of signal can compare with the metal line or shorter, i.e. high frequency signal. Hence, at low frequency, a metal line was regarded as a resistor. On the other hand, a metal line was regarded as resistor plus parasitic inductance and capacitance parameters at high frequency in an equivalent circuit model.

In order to measure this MIM capacitance, we must layout additional pads and signal lines for measurement. However, these added potions will generate additional parasitic effects. So we must de-embed these parasitic parameters to get the intrinsic high frequency capacitance.

As devices were measured approach microwave frequency, we cannot directly measure the lump circuit components, like RLC (resistance, inductance, and capacitance), because of parasitic effects. Scattering-parameters (S-parameters) were obtained in general [63]. According to microwave theorem [63], we can transform the S-parameters into an equivalent circuit model to extract the component that we want.

Among added portions for measurement, the parasitic capacitance effects dominate in probe pads. We can transform both of the measured S-parameters of MIM capacitors and “OPEN” dummy device into admittance parameters (Y-parameters). Then we de-embed the parasitic capacitance effects from the MIM capacitor by Y_{MIM}-Y_{OPEN}. So, we can obtain the de-embedded S-parameters from the transformation of de-embedded Y-parameters (the simulated S-parameters shown in Figure 5-4(a)). Thus, we have de-embedded the parasitic capacitance effects due to the probe pads of MIM capacitor.

Then, we use an equivalent circuit method to simulate the de-embedded S-parameter to extract each components of the equivalent circuit model shown in Figure 5-4(b). From this, we can obtain the RF capacitance of MIM capacitor.

The capacitance values were measured directly using LCR meter from 10 KHz to 1 MHz and calculated from the de-embedded S-parameters up to 20 GHz using the following equation [14]:

$$\frac{\Delta C}{C} = \frac{Z_0(2+Z(C)/Z_0)^2}{2R_P^2} j\omega C^2 (R_P + 1/j\omega C)^2 \Delta(S_{21}) \qquad (5.1)$$

$$Z(C) = R_S + j\omega(L_{S1} + L_{S2}) + \frac{R_P / j\omega C}{R_P + 1/\omega C} \qquad (5.2)$$

$$S_{21} = \frac{2}{2+Z(C)/Z_0} \qquad (5.3)$$

We can use the equation (5.1) to derive the capacitance densities at different frequencies: Z(*C*) in equation (5.2) is the total impedance in the equivalent circuit model of Figure 5-4(b) and Z_0 is the characteristic impedance of transmission line. The RF frequency $\Delta C / C$ in equation (5.1) is obtained by differentiating the measured S_{21} in equation (5.3), where shows the relation between the S_{21} and total impedance Z(*C*). Figure 5-5(a) shows that the derived $\Delta C / C$ decreases rapidly with the increasing frequency, which is advantageous for high frequency analog/RF circuits.

5.4 Results and discussion

A. C-V ,I-V, Δ*C/C*, and *TCC characteristics*

Figure 5-1 shows the *C-V* characteristics for TaN/STO/TaN MIM capacitors. A very high capacitance density of 35 fF/μm^2 or 0.99 nm capacitance-equivalent-thickness (CET) is measured at 1 MHz. Such high capacitance density provides a 35 times area reduction than the ~1 fF/μm^2 value provided by foundry [55]. In addition, a near constant capacitance value with little voltage and frequency dependence is obtained for the STO MIM capacitor, which is important for RF IC under large voltage swing condition. Such high capacitance density is due to the very high κ value of 169 in STO dielectric that is significantly larger than the κ~20 of HfO_2 used in current DRAM manufacture and also higher than the κ~45 in TaTiO MIM capacitors [21], [60]. Since the STO is also shown in the future DRAM technology roadmap [59], it is highly possible to integrate the RF capacitor with DRAM for multi-functional SoC application.

Figure 5-2 shows the *J-V* characteristics of STO MIM capacitors. Small leakage current of only 1×10^{-7} A/cm^2 (7×10^{-7} A/cm^2) is obtained at 1V (2V) with high capacitance density of 35 fF/μm^2. The small leakage current under positive bias voltage (electron injection from bottom electrode) indicates the good bottom STO/TaN interface, where the higher leakage current under negative bias is attributed to the surface roughness originated from STO crystallization. However, such crystallization is needed for STO to give a much higher κ value than amorphous HfO_2 and TaTiO. For a typical large 1 pF capacitor used in RF IC, a very small leakage current of only 29 fA is obtained due to the very high κ value, which is much smaller than the off-state current of a MOSFET with deep sub-100nm gate length [61]-[62].

For analog capacitors a low capacitance voltage linearity is important. Figure 5-3(a) shows a *ΔC/C-V* plot for TaN /STO/TaN MIM capacitors with 35 fF/μm^2 density. We obtained quadratic voltage linearity (α) of 542 ppm/V^2 for the capacitance. Figure 5-3(b) shows the temperature dependence of normalized capacitance of STO MIM capacitor. The *TCC* showed an increase trend with increasing measured temperature.

B. High frequencies characteristics

Figure 5-4(a) shows the measured S-parameters for the 35 fF/μm^2 density TaN/STO/TaN capacitors. The capacitance values at RF frequency were extracted using the equivalent circuit model in Figure 5-4(b): the MIM capacitor is modeled by R_p and C, where the R_p originates from the high-κ dielectric loss. In addition, the R_s, L_{s1}, and L_{s2} represent the parasitic impedances in the coplanar transmission line used for RF measurements. Good agreement between measured and simulated data are obtained over entire frequency range from 200 MHz to 10 GHz indicating the equivalent circuit model suitable and reliable for the TaN/STO/TaN modeling and capacitance value extraction.

Figure 5-5(a) shows the dependence of capacitance density as a function of frequency, where the data at RF frequency region is extracted from the circuit model with well matched S-parameters and the data at intermediate frequency (IF) are obtained from the measured C-V characteristics. A small capacitance reduction of only 4.1% from 100 kHz to 10 GHz is obtained indicating the good quality of device performance over the IF to RF range [21], [60]. However, such extracted capacitance density at RF regime is not sensitive enough to calculate the small $\Delta C/C$ variation- important for precision capacitors operated under large signal swing. We have used the previous circuit-theory-derived equation to calculate the $\Delta C/C$-V from measured S-parameters and the results are also shown in Figure 5-5(a) and 5-5(b). The measured $\Delta C/C$-V can be fitted with a second order polynomial equation, where linear (β) and quadratic (α) voltage coefficients of ΔC/C were obtained. Since the β effect can be canceled by circuit design using differential method, α is the key parameter to cause the unwanted voltage-dependent $\Delta C/C$. The obtained $\Delta C/C$ and α have been plotted in Figure 5-5(a). Fortunately, the $\Delta C/C$ decrease with increasing frequency into RF region, which is attributed to the trapped carriers being unable to follow the high frequency signal with typical carrier lifetimes in the range ms to μs [14]-[15], [19]-[20]. The device quality (Q) factor is shown in Figure 5-6, which was extracted from measured S-parameters using a circuit model [57], [60] at RF frequencies. A capacitance value of 14 pf was obtained and consistent to the 35 fF/μm^2 density measured by C-V. A good Q-factor >50 is obtained for RF application before resonant frequency (f_r) of ~13 GHz, where the relative low f_r is due to the large capacitance.

The important device parameters for the analog capacitors are summarized in Table 5-1. Among the previous high-κ capacitors, the TaN/STO/TaN capacitor provides a promising and effectively solution to improve VCC-α, while maintaining very high capacitance density.

5.5 Conclusion

Very high 35 fF/μm^2 capacitance density, low capacitance reduction of 4% from 100 kHz to 10 GHz and small leakage of 1×10^{-7} A/cm^2 at 1 V were simultaneously achieved in very high-κ TaN/STO/TaN MIM capacitors. This high density MIM capacitor is important for largely down-scaling the capacitance size and integration with DRAM.

Table 5-1. Comparison of important device data for MIM capacitor with various high-κ dielectrics.

	Tb-HfO_2 [11]	HfO_2 [10]	Ta_2O_5 [12]	TiTaO [19]	ITRS 2018	TiHfO	**STO**
C (fF/mm^2)	13.3	12.8	9.2	10.3	10	13.5	35
J (A/cm^2)	1×10^{-7} (2V)	8×10^{-9} (2V)	2×10^{-8} (1.5V)	1.2×10^{-8} (2V)	—	4×10^{-7} (2V)	9×10^{-8} (1V) 7×10^{-7} (2V)
J/(C×V) (fA/[pF×V])	38 @2V	2.9 @2V	14.5 @1.5V	5.8 @2V	<7	—	—
a (ppm/V^2)	2667	1990	3580	89	<100	825	529

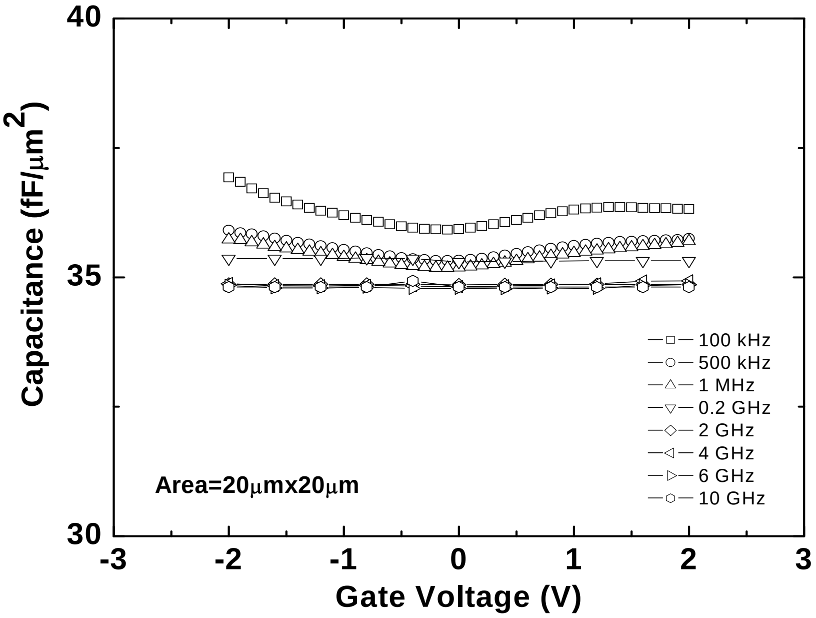


Figure 5-1 The *C*-*V* characteristics of TaN/STO/TaN MIM capacitors. Very high capacitance density of 35 fF/μm^2 is measured at 1 MHz with small capacitance variation. The *C*-*V* results from 100 kHz to 1 MHz are measured from LCR meter and the data from 0.2 GHz to 10 GHz are obtained from the S-parameters.

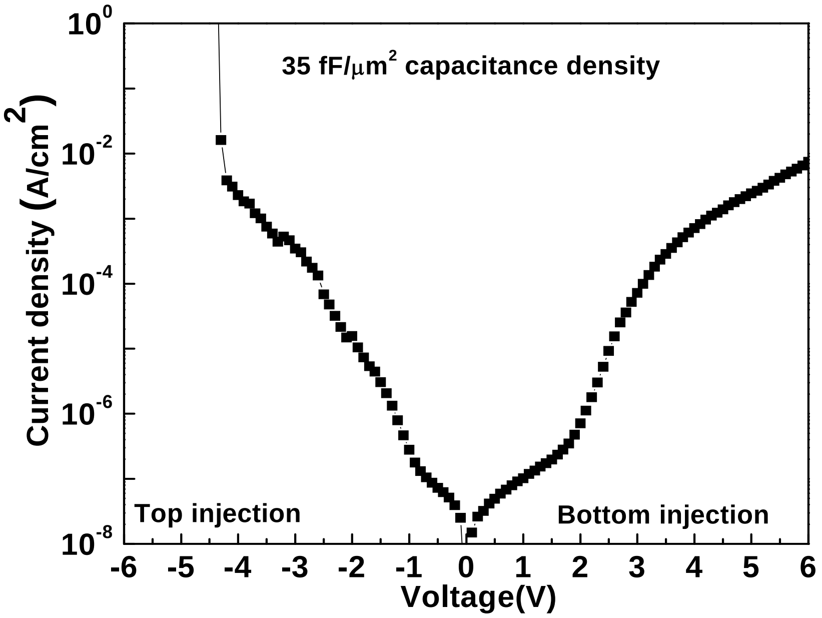
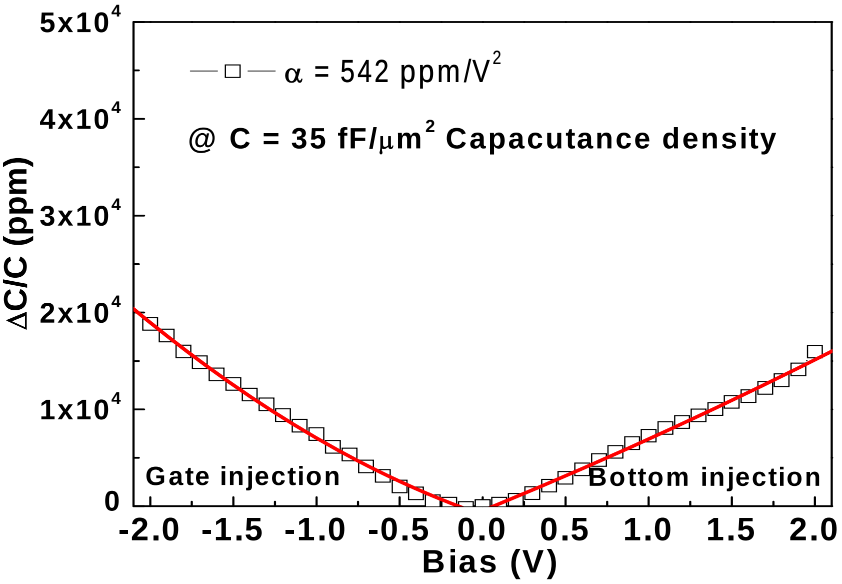


Figure 5-2 The measured *J-V* characteristics of TaN/STO/TaN MIM capacitors with large 35 fF/μm^2 density.



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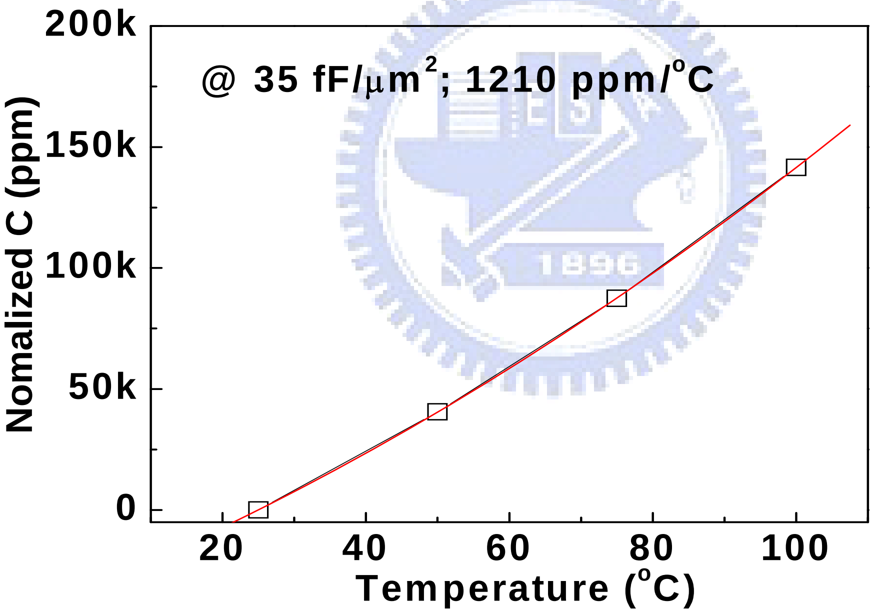
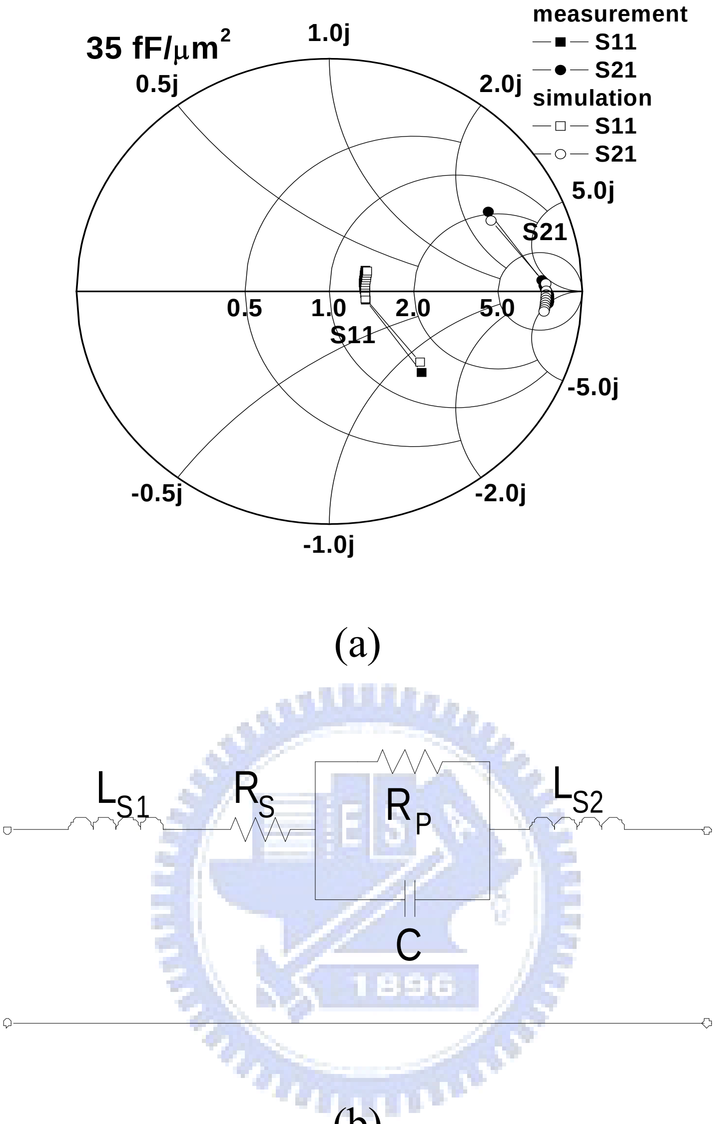


(b)

Figure 5-3 (a) Δ*C/C-V* plot for TaN /STO/TaN MIM capacitors (b) Temperature-dependent normalized capacitance for TaN /STO/TaN MIM capacitors.



(a)

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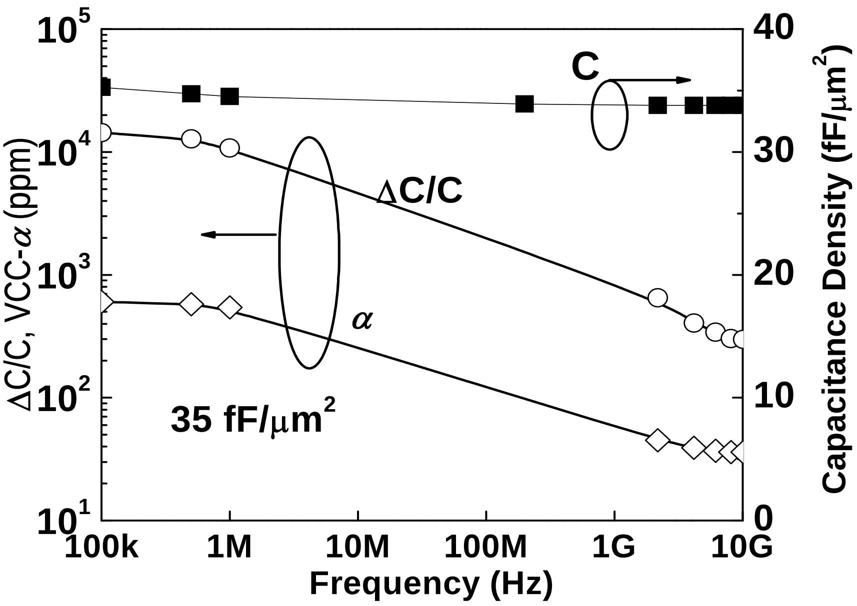
Figure 5-4 (a) The measured and simulated two-port S-parameters for STO MIM capacitors, from 200 MHZ to 10 GHz. (b) The equivalent circuit model for capacitor value extraction from measured S-parameters.



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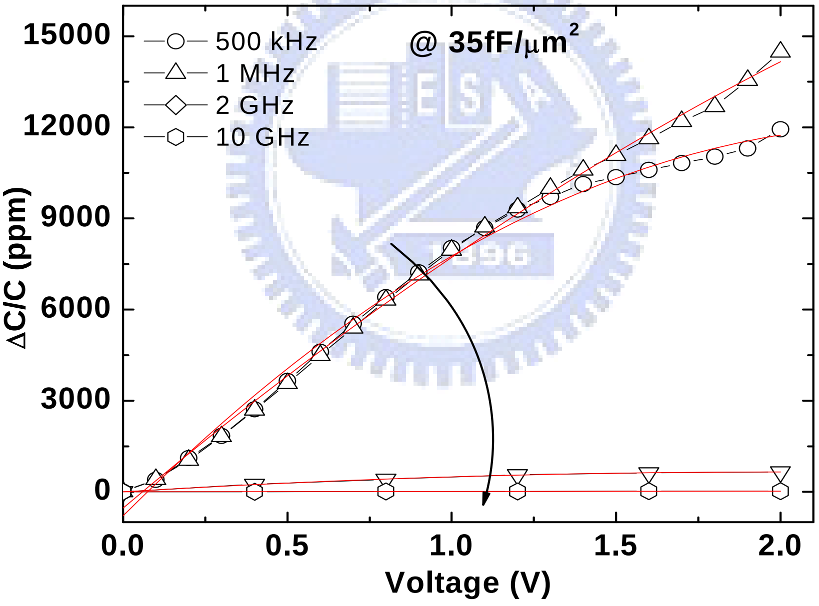
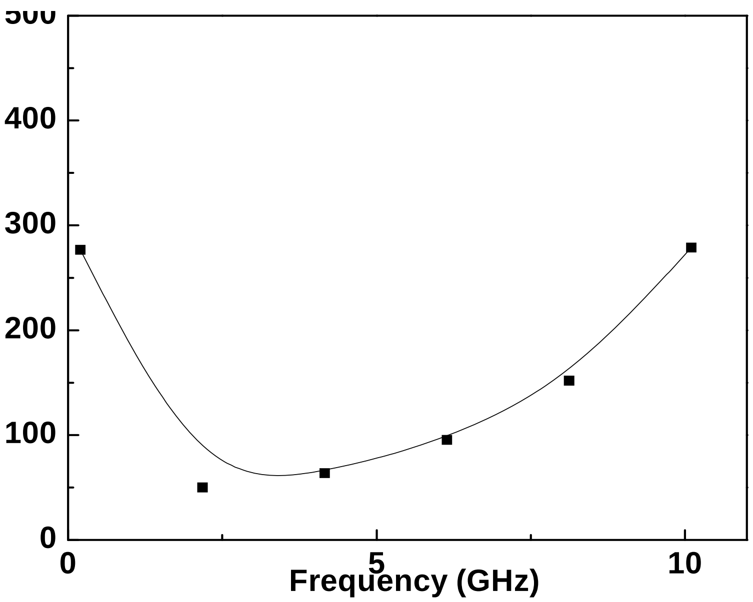


(b)

Figure 5-5 (a) Frequency dependent capacitance density, Δ*C/C* and α for a STO MIM capacitor biased at 1.5V. The data for frequency > 1 MHz were obtained from the S-parameters. (b) The Δ*C/C* characteristics of a STO MIM capacitor at RF regime.



(b)

Figure 5-6 Q-factor of TaN/STO/TaN MIM capacitors biased at 2V.

Chapter 6

Conclusion

Using micro-crystallized high-κ $SrTiO_3$ on NH_3 treated TaN bottom electrode,a very high density of 35 fF/μm^2 is measured in a radio frequency (RF) metal-insulator-metal (MIM) capacitor using high-κ (κ = 169) $SrTiO_3$. A very small capacitance reduction of 4.1% from 100 kHz to 10 GHz, low leakage current of 1×10^{-7} A/cm^2 at 1 V is simultaneously measured. The small voltage dependence of a capacitance ΔC/C of 637 ppm is also obtained at 2 GHz, which ensures this MIM capacitor useful for high precision circuits operated at a RF regime. Although this work could achieve high capacitance density and low leakage current at the same time, but its higher PDA temperature (>450°C) to form nano-crystal is an important issue in the back-end process flow.

Second, in order to further study the characteristics of $SrTiO_3$, the impact of Ta_2O_5 doping on electrical characteristics of $SrTiO_3$ MIM capacitors was studied for the first time. Using high-κ Ta_2O_5 doped STO dielectric (PDA temperature:420°C), an absolute value of quadratic voltage coefficient of capacitance (VCC-α) of 420 ppm/V^2 and high capacitance density of ~20 fF/μm^2 are achieved in this work. This is approximately one order of magnitude better than the same device using a pure STO, with added advantages of improved voltage and temperature coefficients of capacitance. Besides, the degradation of electrical properties after stress is all reduced, in contrast with using a pure STO. In our previous work of STO MIM, although nano-crystallized STO shows higher κ values and good device characteristics, the nano-crystallized STO requires a heat treatment at 450~500^{o}C under an oxygen ambient. This activation maximum temperature (>450^{o}C) cannot permit for the backend integration.

In addition, we have also developed successfully a novel plasma treatment on dielectric film to improve the electrical properties of MIM capacitors. This improvement may arise from the nitrogen atom assists to passivate oxygen vacancies in the TiNiO dielectric and eliminate the electron leakage path mediated by the oxygen vacancies.

Moreover, high 16 fF/μm^2 density and very low 7×10^{-9} A/cm^2 A/cm^2 leakage current are all measured in novel high-κ TiPrO (κ=26) MIM capacitor with high work-function Ir, which meet well the ITRS roadmap requirement for analog IC at year 2018.

Recommendation

The possible influences on voltage dependence of capacitance are summarized as the following section:

(A). Interfacial layer:

The interfacial layer is responsible for higher leakage current, degraded *VCC* and *TCC*, as discussed above, and which may be due to the higher trap density from the oxygen deficiency. For this reason, lower fabricated temperature or NH_3 plasma treated TaN should be used to suppress interfacial layer growth from inter-diffusion and reaction between dielectric and electrode.

(B). Surface roughness:

The surface roughness could induce higher leakage and $\Delta C/C$ due to local electric field enhancement. It is interesting that the amorphous dielectric, such as TiPrO and TiNiO exhibit the bottom injection is the worse case due to poly-crystallized lower electrode. However, the crystallized material, such as $SrTiO_3$ shows the gate injection is the worse case from degraded top interface, which is significant with increasing dielectric thickness. Consequently, using amorphous dielectric and electrode may be a good method for this concern.

(C). Dielectric thickness:

The VCC-α is strongly dependent on the capacitance density and electric field across on dielectric: an exponential decrease of α with increasing capacitance effective thickness (CET), or $1/C$, was observed for all the capacitors. In other words, for the same CET or capacitance density value, the higher-κ dielectric has the lower VCC-α due to lager thickness and decreased electric field. The $\alpha-1/C$ dependence is important to choosing the required C density and also meeting the analog specifications of a low α.

In conclusion, MIM capacitors incorporating a higher ϕ_m top electrode and a higher κ dielectric provide a practical approach to achieve low thermal leakage and good VCC simultaneously, without reducing the capacitance density - as in a multi-layer or laminate structure.

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Publication List

(A) International Journal:

[1] **C. C. Huang**, C. H. Cheng, B. H. Liu, and A. Chin, "Impact of Ta_2O_5 doping on Electrical Characteristics of $SrTiO_3$ Metal-Insulator-Metal Capacitors", *Jpn. J. of Applied Physics,* **(accepted).**

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(B) International Letter :

[1] **C. C. Huang**, C. H. Cheng, Albert Chin, and C. P. Chou, "Leakage Current Improvement of Ni/TiNiO/TaN Metal-Insulator-Metal Capacitors using Optimized N^+ Plasma Treatment and Oxygen Annealing", *Electrochem. Solid-State Lett.*, vol. 10, no. 10. pp. 289-290, 2007.

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