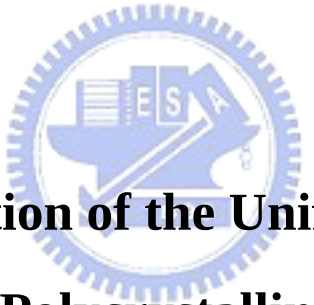
國立交通大學

電子工程學系電子研究所

碩士論文

低溫複晶矽薄膜電晶體元件均勻性及類比緩衝電路設計之研究



Investigation of the Uniformity of Low-Temperature Polycrystalline Silicon Thin Film Transistors in the Devices and Analog Buffer Circuits

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摘要

在本篇論文中，我們以低溫複晶矽薄膜電晶體為基礎，從元件結構以及類比緩衝電路設計兩方面來探討元件均勻性之問題。在此研究中，我們將藉由簡單地調整元件結構來提升低溫複晶矽薄膜電晶體之均勻性，並且提出一個對元件變異性具有補償能力之新式源極隨耦器形式的類比緩衝電路。

首先，我們針對元件結構之觀點來探討低溫複晶矽薄膜電晶體之元件均勻性。希望在不需要額外之光罩也無須改變傳統製程之前提下，藉由元件結構上之簡單調整來提升元件均勻性。在此研究之中，我們採取了多通道之元件架構。根據實驗之結果，我們發現多通道結構可以提升低溫複晶矽薄膜電晶體之截止電壓(threshold voltage)及次臨界擺幅(subthreshold swing)之均勻性，然而對於載子移動率(mobility)及漏電流(leakage)之變異性並無改善。針對此結果，我們也進一步進行機制之探討，認為機率是造成多通道結構均勻性提升最主要之原因。此外，我們將多通道結構引入傳統源極隨耦器形式的類比緩衝電路之驅動電晶體中，藉由觀察類比緩衝電路之輸出特性來驗證多通道結構對薄膜電晶體均勻性提升之能力。由量測結果可以看到具有多通道結構之源極隨耦器形式的類比緩衝電路，其輸出電壓之變異性大約只有傳統源極隨耦器形

式之類比緩衝電路之一半，證實多通道結構的確對元件之非均勻性具有改善作用。

在類比緩衝電路設計之研究中，我們將設計一個新式源極隨耦器形式之類比緩衝電路以消除因元件變異性造成之電路輸出電壓變異的問題。我們先從不同形式之類比緩衝進行比較、評估。雖然運算放大器形式之緩衝電路被廣泛應用於傳統單晶矽之類比積體電路，但礙於複雜之電路架構，較嚴重之輸出電壓之變異性以及較高的功率消耗，以低溫複晶矽薄膜電晶體為基礎之運算放大器形式的緩衝電路並不適合於系統面板(system-on-panel)之應用。相較之下，源極隨耦器形式之類比緩衝電路具有電路架構簡單，對元件變異性有較高之免疫力，以及功率消耗較低等優點，對未來系統面板之應用提供了較佳的選擇。

在設計源極隨耦器形式之類比緩衝電路方面，首先我們針對傳統架構之源極隨耦器進行電路模擬之探討。根據模擬的結果，我們發現傳統的源極隨耦器具有輸出不飽和以及嚴重的輸出變異之問題。因此我們提出了一個新式的源極隨耦器形式之類比緩衝電路來解決這些問題。我們所提出的補償電路由兩個 N 型薄膜電晶體，一個儲存電容及四各開關所組成。在此類比緩衝電路之中，我們藉由加入一個主動負載來抑制傳統源極隨耦器中，因為低溫複晶矽薄膜電晶體較大的次臨界電流所引起輸出不飽和的現象。並且藉由儲存電容以及適當的驅動過程來進行元件變異性之補償。經由模擬以及實際量測結果證實，我們所提出的電路架構確實可以有效地補償元件變異性之問題。此外，在設計類比緩衝電路的過程之中，我們也發現主動負載之閘極偏壓對電路輸出偏差具有顯著的影響。因此在此部份之研究中，我們也對主動負載之偏壓效應做了詳盡的探討。從偏壓效應的探討之中可以得知，我們所提出來的源極隨耦器形式之類比緩衝電路，可藉由適當的偏壓設計達到具良好輸出特性以及低功率消耗之類比緩衝電路。

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ABSTRACT

In this thesis, based on the low-temperature polycrystalline silicon thin film transistors (LTPS TFTs), the device uniformity issues of LTPS TFTs were investigated from the aspects of device structure and buffer circuits design. Simply modified device architecture is used to improve the uniformity of LTPS TFTs and a new source-follower type analog buffer with the capability of device variations compensating is proposed in this work.

First, the device uniformity of LTPS TFTs is studied from the view point of device architecture. We purpose to improve the device non-uniformity of LTPS-TFTs by means of simply modifying the device architecture but without the use of additional masks and have no need to modify the standard process of TFT fabrication. The multi-channel structure with slicing layout method is used in this work. According to the experimental results, it is observed that the multi-channel structure can improve the non-uniformity of threshold

voltage and subthreshold swing of LTPS TFTs, while has no effect on the transconductance and leakage current. The mechanism of the improving uniformity of multi-channel structure is discussed and it is considered that probability effect is the most possible cause. In this part of research, in order to verity the capability of improving uniformity of multi-channel structure, the output variations of the conventional source follower with multi-channel structure are also studied. It can be seen that the output variations are reduced to about half of that of conventional source follower. It is evident that the device non-uniformity indeed can be improved by multi-channel structure.

In the study of analog buffer circuits design, we intend to develop a new analog buffer with compensating configuration to eliminate the output variations resulting from device non-uniformity. First, differential types of analog buffers were compared and evaluated. Although op-amp type is most commonly used as the output buffer in single crystal silicon integrated circuits, the complicated circuit configuration, huge output voltage variation, and high power consumption of op-amp-type analog buffer using LTPS TFT make it not suitable for system-on-panel application. Source-follower-type analog buffer is considered a best candidate because of its simplicity, higher immunity to the device variations of LTPS TFTs and low power consumption.

For designing the analog buffer with source-follower configuration, the output characteristics of conventional source follower is first studied by HSPICE circuit simulator. It is observed that output unsaturated phenomenon and severe output variation exist in the conventional source follower. In order to enhance the output performance of analog buffers, a new source-follower type analog buffer for is proposed to solve the problems of output unsaturated and variations. The proposed analog buffer is composed of two n-type thin film transistors, one storage capacitor and four switches. The active load is employed to suppress the unsaturated phenomenon of output voltage arisen from the significant subthreshold current of driving TFTs. The device variations compensating is performed by the storage

capacitor and compensated operation of the proposed buffer. According to the simulated and measured results, it confirms that the output variation resulting from the variation of poly-Si TFT characteristics is successfully compensated in the proposed analog buffer. Furthermore, it is observed the bias voltage of the active load has significant influence on the output deviation of the proposed analog buffer. The bias effect is also discussed in this study. It is concluded that an optimum value of the bias voltage can be designed to achieve high output performance and keep low power dissipation of the proposed analog buffer.

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Contents

Table Lists

Chapter 2

Chapter 4

Figure Captions

Chapter 2

Chapter 3

Chapter 4

Chapter 1

Introduction

1.1 Overview of the Applications of Thin Film Transistors (TFTs)

Thin-film transistors (TFTs) have been widely used in the electronic system applications in the past ten years. Depending on the different materials of active layer, thin-film transistors (TFTs) can be mainly categorized to three types: amorphous silicon thin film transistors (a-Si:H TFTs), polycrystalline silicon thin film transistors (poly-Si TFTs), and organic thin film transistors (OTFTs). Amorphous silicon thin film transistors (a-Si:H TFTs) were introduced in the 1970's, which have been used in many applications such as solar cells [1.1], image sensors, printing heads, electronic copiers [1.2]-[1.4], especially in the applications of active matrix liquid crystal displays (AMLCDs) [1.5]-[1.7] and newly developed active matrix organic light emitting displays (AMOLEDs) [1.8]-[1.10]. In the AMLCDs, a-Si:H TFTs is used as the pixel switch placed at each pixel for addressing. While in the AMOLEDs applications, a-Si TFTs is used as the active device to provide driving current for illumination. Although a-Si TFTs has the advantage of low processing temperature (<350^{o}C) to allow the use of cheap, mass-produced glass substrate. However, the low carrier mobility of a-Si TFTs which is generally below 1cm^{2}/V-s makes the

difficulty in realizing high resolution definition displays.

On the other hand, polycrystalline silicon (poly-Si) was used to be the active material of TFT for achieving higher performance in the 1980s. Poly-Si TFTs can be divided into two types according to the process temperature, which are high-temperature polycrystalline silicon TFT (HTPS TFT) and low-temperature polycrystalline silicon TFT (LTPS TFT). High- temperature poly-Si TFTs is fabricated by chemical vapor deposition (CVD) with processing temperature above 650^{o}C. This approach requires an endured high-temperature substrate such as quartz, and this demand restricts to the small panel display such as projection display system which is inexpensive. Therefore, a low temperature process was investigated and progressed rapidly to be compatible with glass substrates for increasing economic benefits. Poly-Si TFTs fabricated with a maximum temperature below 600^{o}C is so called low-temperature polycrystalline silicon thin film transistors (LTPS TFTs). In the fabrication of LTPS TFTs, the crystallization of a-Si thin film is considered to be the most important process. Among various low temperature crystallization methods, the excimer laser crystallization (ELC) is considered to be the most promising approach to get high performance of the transistors compared with solid phase crystallization (SPC), metal induced crystallization (MIC) [1.11]-[1.12]. Low temperature poly-Si TFTs can be applied to image sensors [1.13], solar cells [1.14], 3-dimension ICs' [1.15], and the most conspicuous application is the pixel element [1.16]-[1.17] and integrated peripheral circuits of active matrix liquid displays (AMLCDs) [1.18]-[1.20]and active matrix organic light emitting displays (AMOLEDs) [1.21]-[1.22]. Because of the higher carrier mobility and better reliability, LTPS TFTs offer the possibility for integrating the peripheral circuits with the pixel array on a single glass substrate to realize the final target of system-on-panel (SOP) which integrating the driver circuits, controller circuits, memory, central process unit (CPU), etc., and achieve the compact, highly reliable, and low cost display system.

In the recent years, organic thin film transistors (OTFTs) has attracted much interest

due to the advantages of very low process temperature (<200^{o}C) and easily fabricated, therefore OTFTs can be fabricated on the flexible plastic substrate for low cost electronics applications. OTFTs can be applied to the switching devices for active matrix flat panel displays (AMFPDs) based on liquid crystal pixels(AMLCDs), organic light emitting diodes(AMOLEDs), or “electronic paper” displays [1.23]-[1.24], additionally, sensors [1.25], low-end smart cards, and radio-frequency identification tags (RFIDs) consisting of organic integrated circuits. Although OTFT can be applied to large area, low-temperature processing, structural flexible, and low cost applications, this technology is not mature yet [1.26]. Many issues limit the applications of OTFT such as device stability and lifetime, and the most critical issue of OTFTs is the extremely low field effect mobility (typically <<1cm^{2}V^{-1}s^{-1}) compared to the a-Si TFTs and LTPS TFTs.

1.2 Comparison between Amorphous Silicon Thin Film Transistors (A-Si TFTs) and Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

In this section, we will compare the difference between the a-Si TFT and LTPS TFT from two aspects. First is the manufacturing aspect in terms of process steps, commercial cost, and yield and second is the electrical performance including the driving capability and stability.

- **Manufacturing aspect**

- Process Steps and Commercial Cost

Less process steps, usually four to five mask processes are necessary for the fabrication of a-Si TFT which is usually employed by bottom gate structure. These mask processes include gate electrode, a-Si active layer, source/drain electrode, passivation layer, and ITO. Compared to a-Si TFT, top gate structure is usually adopted for LTPS TFTs, and more process steps, nine to ten mask process are needed. They are poly-Si active layer, channel and source/drain implant (N^+, N^-, P^+), gate electrode, inter layer dielectric, source/drain electrode, passivation layer, and ITO.

In addition to more process steps, extra equipment is required to fabricate the LTPS TFTs. These include excimer laser annealing for poly-Si film crystallization, ion implanter or ion shower for implantation to form the source/drain, rapid thermal annealing or excimer laser annealing for doping activation. Consequently, higher equipment cost than a-Si TFT is required to fabricate LTPS TFT. More process steps and higher equipment investment make LTPS TFT more costly than a-Si TFT [1.28]

Electrical Performance

- Driving Capability

Due to the smaller grain sizes and higher gate/source and gate/drain overlap capacitances of hydrogenated amorphous silicon TFT, the mobility of a-Si TFTs is generally below 1.0 cm^2/V-s, and such low carrier mobility limits the driving capability of a-Si TFT. In order to meet sufficient driving capability, large W/L ratio must be designed in the a-Si TFT based circuits which limit the resolution of display. Besides, with the intrinsic properties of a-Si, only n-type TFT is available when a-Si is employed which greatly

reduces the flexibility of TFT applications and causes some difficulties in designing. On the other hand, the carrier mobility of LTPS TFT is one or two orders higher than that of a-Si TFT. The higher driving ability makes it a good candidate for high resolution displays, even provides the possibility of integrating driver circuits for AMLCDs and AMOLEDs to realize completely system on panel (SOP). Besides, both n-type and p-type LTPS are available, therefore CMOS drivers can be integrated on the substrate.

- Stability

A-Si TFT suffers from large threshold voltage shift and conductance current lowering after long term operation. These device performance degradations are commonly explained by two mechanisms which include the dangling-bond states creation in the amorphous silicon layer and charge trapping in the gate insulator [1.29]-[1.30]. On the other hand, LTPS TFT is quite stable relatively after a prolonged period of biasing time.

Although low temperature polycrystalline silicon thin-film transistors (LTPS TFTs) require higher manufacturing cost than that of a-Si TFT, the higher driving capability and better long term reliability of the LTPS TFT are more suitable for the flat panel display applications. At present, LTPS TFT has attract much attention for integrating driver circuits of active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diodes (AMOLEDs) [1.31]-[1.32]. However, there are still some issues of LTPS TFTs for system-on-panel (SOP) application. The more detailed concepts and issues of system-on-panel (SOP) are discussed in the next section.

1.3 The Concepts and Issues of System-On-Panel (SOP)

At present, application of thin film transistors (TFTs) for active matrix display is mainly in the pixel element, the driving circuits and other controlling circuits of active matrix display are employed with single crystalline VLS IC design on printed circuit board (PCB). It requires large numbers of interconnections between the panel and the peripheral circuits. Since off-panel connections have considered to be the most frequent cause of LCD failure, the system-on-panel (SOP) technology which omitting the usage of ICs and interconnections promise the LTPS-based products to be more reliable. Moreover, reducing the number of external components and the connections to display enable to lower the cost of panel and a compact, light weight system can be achieved for better economic benefits. Thus, several researches have been proceeded to integrate the analogue and digital display driver circuits , controller circuits, random access memory (RAM), and more complicated part such as central processing unit (CPU) or digital signal processing (DSP) on the active matrix substrate [1.33]-[1.34]. In 2004, the first full-functional system panel was proposed by Sharp Corporation and Semiconductor Energy Laboratory Co., where a CPU, a graphic controller, an audio circuit, a program ROM, an audio ROM, various types of RAMs, a voltage generator, a clock generator, and the large-scale logic circuits comprising approximately 120,000 TFTs are monolithically formed on a glass substrate forming an LCD by using CG-Silicon technology [1.35].

Although the system display has been successfully demonstrated, the technology is not matured for mass production. In additional, the advantages of lower system cost and lower power consumption are not apparent nowadays. The properties of poly-Si TFTs are considered to be the key factors for the goal of system-on-panel, thus the disadvantages of electrical properties and the fabrication techniques of poly-Si TFTs must be improved to

satisfy the requests for system on panel. Here, several critical issues and the research opportunities for developing system on panel are discussed in the following sections.

• Issues of System-On-Panel

- Electrical Properties

At present, the performance of poly-Si TFTs is still much poor in comparison with conventional single-crystal MOSFETs such as lower carrier mobility, higher threshold voltage, larger subthreshold current and larger leakage current, etc. In order to achieve high speed and high driving capability of poly-Si TFTs, significant advances in carrier mobility are needed. As the carrier mobility is improved, the scale of the transistors can be reduced without sacrificing the driving current, thus high integrated density of transistors can be obtained for high resolution and more functions integrated display system. For the demand of low power consumption, low and centered (between n-tpe TFT and p-type TFT) threshold voltage of poly-Si TFTs is needed. The high threshold voltage will result in relatively high voltage supply required to drive the circuits and dissipate high power.

The kink effect and hot carrier effect of poly-Si TFTs are also the critical problems in system display progressing. Kink effect of poly-Si TFTs causes the high value of output conductance and a strong dependence on bias condition [1.36] that will raise the difficulty in circuit design. For example, in analogue applications that will lead to a considerable reduction of the maximum attainable gain and reduces the common mode rejection ratio (CMRR), and result in increasing of power dissipation and slightly degrades the switching characteristics in digital circuits. Besides, the unsaturated I-V curve causes the problem in saturation voltage defined. The standard definition of saturation voltage is not applicable because a well-defined saturation does not exist. Hot carrier effect will cause the shift of

threshold voltage, subthreshold swing, and mobility of poly-Si TFTs due to the carrier trapped in the Si/SiO_2 interface or carrier injection to the gate oxide. This will degrade the reliability of poly-Si TFTs. Moreover, in order to reduce the kink effect and hot carrier effect, device with drain-engineering architecture or some circuit configurations (e.g. cascode, normally used to reduce the consequences of the kink on circuits) must be introduced. Thus the added steps of device process and excessive number of stacked devices are required which result in an increase in fabricated cost and power dissipation.

The device electrical properties play a key role in the performance of display, therefore, electrical characteristics of poly-Si TFTs must be further improved for meet the requirements of next system-on-panel (SOP) generation.

- Uniformity

Over the past ten years, laser-based crystallization has been intensely studied and developed for poly-Si TFTs [1.37]-[1.40], and have been verified to be the excellent technology with the ability to produce high quality poly-Si films [1.41]. Excimer laser crystallization (ELC) is the most commonly used method for mass production of LTPS TFTs. However, the narrow process window of laser energy density for producing poly-Si thin film is a critical issue for ELC LTPS TFTs. In order to crystallize large-grain poly-Si, the laser energy density must be controlled in the super lateral growth (SLG) region. Nevertheless, the pulse-to-pulse variation of excimer laser energy density and non-uniform laser beam profile cause the laser energy density not to be uniformly controlled in the SLG region across the large area. That result in random grain boundaries distributed in the channel region of LTPS TFTs between devices. As the channel dimensions continue to shrink, the uniformity behavior becomes more severe. The larger device-to-device variation will lead to many problems in real product applications.

- Design Rule Consideration

The performance of poly-Si TFTs is inferior to that of conventional single crystallization Si MOSFETs at present. In order to keep compatible with large-area processing, relatively coarse design rules must been used in designing the poly-Si TFTs based circuits [1.41]. There are three reasons for this phenomenon. First of all, the restriction of photolithographic and processing for fabricating TFTs on the large-area substrate is severe. It is more challenging to scale down the device into the submicron dimension because of limitations in the resolution of lithography equipment. Second, the short-channel effects are relatively severe in poly-Si TFTs. As the dimension scaled down, the short-channel effects will intensely affect the device performance and make more difficulty in designing. Third, an AMLCD pixel typically requires a total voltage swing of about 10 V to encompass both the positive and negative driving polarities, and about 15 V supply voltage is needed by using poly-Si TFTs drivers. Therefore, the broader line width is required.

In order to enhance the device performance, the dimension of poly-Si TFTs must be scaled down. For the development of more advanced panels systems, the dimension of channel must be shrunk to submicron dimension (<0.8um) to achieve high performance TFTs [1.42]. However, there are many challenges to scale down the device into the submicron dimension domain by current mass production technologies. Thus it requires the development and introduction of new technologies of process and device.

- Power Consumption

Because of the higher threshold voltage, lower mobility, and loose design rule of

poly-Si TFTs compared to single crystal Si MOSEFTs. It require higher supply voltage for sufficient driving capability of poly-Si TFTs, thus the power consumption of integrated driver circuits tends to be higher than that of single crystal silicon ICs. This tendency will increase as circuit-integration progresses. For example, in the case of QVGA (Quarter Video Graphics Array) LCDs, the power consumption of conventional TFT-LCD with external driver ICs ranges from 10 to 13 mW, while that of typical SOP-LCDs with integrated driver circuits ranges from 20 mW upwards, which is more than twice of the power consumption of conventional TFT-LCDs [1.43].

Therefore, power reduction is one of the major challenges in further advanced SOP-LCDs application. From the viewpoint of device electrical characteristics, low and centered (between nMOS and pMOS device types) threshold voltage with extremely small distribution is needed for meeting the requirement of low power consumption. Designing the driver circuits with simple configuration and less control signals is also a solution from the designing aspect. Furthermore, modified driver architecture and lowered the line resistance and parasitic capacitance are also the efficient methods to reduce the power consumption.

- Yield

At present, the fabrication cost of low-temperature poly-Si TFTs is higher than that of amorphous silicon TFTs because of more process steps and more expensive equipments. The reduction of external component cost has been offset by the higher fabrication cost in many commercial applications, resulting in higher display prices. Besides, the narrow process window of laser crystallization technology, and additional steps or more complex texture employed to achieve high performance poly-Si TFTs (ex. drain engineering for reducing the kink effect and hot carrier effect, additional steps or equipments for

crystallization to get high carrier mobility) will also reduce the production yield rate. Therefore, how to get high manufacturing yield is really important for real production applications.

- **Research Opportunities for Realizing System-On-Panel**

To achieve the goal of system-on-panel, the improvements at various levels are required to solve several issues as discussed above. This can be achieved from three aspects: materials and process technology, device structure, and circuit design.

- Materials and Process Technology

New elemental process technology is needed for the formation of high quality critical layers, such as the active and the gate-insulator layers of poly-Si TFTs. In the area of active layer, high quality poly-Si microstructure is needed to increase device performance. The crystallization process is a very critical step of the fabrication process for TFTs, because it needs to satisfy the requirements on trade-off considerations including material quality, fabrication cost and thermal-budget constraints imposed by the display substrate. The key points for further improved poly-Si crystallization technology are high electrical performance and good uniformity which can be achieved through enlarging grain size, reducing the defect densities, getting good grain orientation and location control. Several advanced crystallization technology has been proposed to achieve large grain size or location controlled poy-Si film such as the “Continuous Grain Silicon (CG Silicon)” technology by Shrap Corporation [1.44]-[1.45], “Selectively enlarging laser crystallization (SELAX)” technology by Hitachi, Ltd. [1.46]-[1.47], or “comb-shaped excimer laser annealing” technology by NEC Corporation [1.48]-[1.50].

In terms of gate insulator layer, there are requirements in thickness and film quality - i.e. fixed and interface trap density, reliability against electrical stress. GI thickness reduction is necessary to get a TFT gate length in the submicron range. As GI thickness decreases, issues of step coverage become increasingly more severe. Current gate insulator technology is based on PECVD TEOS-SiO2, but this technology seems incapable of overcoming the challenge with the gate insulator thickness gradually decreasing to 50 nm and beyond. In order to maintain high quality for increasingly thinner gate insulator layer, new technology must be introduced.

- Device Architecture

Modified device architectures must complement and customize device performance according to required function. Improvements in the device architecture are vital in two aspects: (1) enable the fabrication of submicron channel dimensions with technology compatible with LCD manufacturing and (2) provide an additional way to complement material quality and compensate the variation of material properties in the critical layer for supplying additional controls for system optimization. But it must conform to the requirement of low cost, thus without extra process step (ex. additional steps for drain engineering or integration of low-voltage and high-voltage TFTs) is also taken into consideration.

- Circuit Design

In additional to improved process technology and device structure, improvements from the circuits design concept offer another solution to realize the goal of system-on-panel. For example, analog buffer which is indispensable to driving large load capacitance of the panel

will suffer from large offset voltage and huge output variation due to the high threshold voltage and large device-to-device variation of poly-Si TFTs. Precise circuit design is employed to deal with the output offset voltage and eliminate the output variation of the buffer circuits through the appropriate circuit architecture and driving scheme. To ensure designing accurately of circuits, suitable device model and exact device parameters are required. It is important to develop accurate models of poly-Si TFTs for circuit simulation and design.

1.4 Motivation

The “system-on-panel (SOP)” technology by low-temperature poly-Si thin-film transistors (LTPS TFTs) is considered to be the most promising solution for realizing the compact, highly reliable, fully functionally, and low system cost display because of the higher carrier mobility of LTPS TFTs which allow the integration of the driver circuit with pixel circuits on a single glass substrate. However, the severe device-to-device variation of LTPS TFTs due to the inevitable process such as pulse-to-pulse variation of laser energy density and random distribution of grain boundaries greatly restrict the progress of system-on-panel (SOP) technology. Thus, in this thesis, the electrical non-uniformity of LTPS TFTs is studied from two viewpoints: device structure and circuit design.

- **The Effect of Multi-channel Structure on the Uniformity of LTPS TFTs**

In this part, we purpose to improve the device non-uniformity of LTPS-TFTs from the aspect of device architecture by means of simply modifying the device architecture while without the use of additional masks and no need to modify the normal process of TFT

fabricating. The multi-channel structure with slicing layout method is used in this work. The electrical characteristics and uniformity of multi-channel devices are studied and compared to conventional single-channel devices. The mechanisms of improving uniformity by the multi-channel structure are found out according to the experimental results.

- **Electrical Uniformity Compensation by Circuit Design**

For the development of integrated data driver employing LTPS TFTs, output buffers are indispensable to drive the large load capacitance of data lines. However, the LTPS TFTs suffer from huge device-to-device variations that cause the bad uniformity of output voltage of analog buffers across the panel. Therefore, many researches on LTPS TFTs analog buffer have been tried to realize a buffer with high immunity to the device variations, and source-follower type analog buffer shows the superiority among these efforts. In additional to the large variations of electrical properties, LTPS TFTs have much larger subthreshold current compared with single crystal Si transistors, and this poor electrical characteristic will results to large output offset and cause the output voltage not to be constant with time. Thus in this thesis, we intend to design a new source-follower type analog buffer which can not only eliminate the output variations but suppress the output unsaturated phenomenon of conventional source-follower type analog buffer. The proposed analog buffer is composed of two n-type thin film transistors, one storage capacitor and four switches. The output voltage variation decreases greatly by the storage capacitor and compensated operation of the proposed buffer. Furthermore, the unsaturated phenomenon of output voltage arisen from the significant subthreshold current of driving TFTs is also eliminated by adding an active load. According to the simulated and measured results, it is obvious that the output voltage is very closely to the real input voltage and the output variations are successfully compensated in the proposed analog buffer.

1.5 Thesis Organization

In chapter two, two types of analog buffers employing low-temperature polycrystalline silicon thin film transistors are introduced and compared. These are operational amplifier type and source-follower type analog buffers. First, the circuit configuration and operation principle of both the simple structure op-amp buffers and modified op-amp circuits with compensated configuration are described. Next, the conventional source-follower type analog buffer and various compensated source follower circuits are introduced. The advantages and disadvantages of op-amp type and source-follower type analog buffers are compared in the end of this chapter.

In chapter three, the effects of the multi-channel structure on the device uniformity of LTPS TFTs are investigated and discussed. The possible mechanisms of improving uniformity of multi-channel structure are proposed and analyzed according to the experimental results. At last, the multi-channel structure is also introduced to the driving TFT of conventional source-follower type analog buffer to study its influence on circuit performance.

In chapter four, a novel source-follower type analog buffer composed of two n-type thin film transistors, a storage capacitor and four switches is proposed for improving the image quality of displays. An active load is employed to the buffer circuit to suppress the unsaturated phenomenon of output voltage arisen from the significant subthreshold current of driving TFTs. The threshold voltage compensation capability and the elimination of unsaturated output voltage phenomenon of the proposed analog buffer are verified by both the SPICE simulation results and experimental results. The measurement results of offset voltage and output variation of proposed analog buffer are also compared to the

conventional analog buffer circuits. Besides, the effect of bias voltage of active load on the performance of proposed buffer circuits is also discussed in this chapter.

Finally, summary and conclusions is given in chapter five.

Chapter 2

Overview of the Analog Buffer Circuits Using Low-Temperature Polycrystalline Thin Film Transistors

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2.1 Introduction

Researches on “system-on-panel” technology have been attracted much attention at present because it provides a chance to realize a compact, light weight, high reliability, and low cost display system [2.1]-[2.3]. Low-temperature polycrystalline silicon thin film transistor is considered to be the best candidate for carrying out system display due to the low temperature process, high carrier mobility and the compatibility to CMOS technology, which allow the integration of the driver circuit and even more complicated parts such as controller circuits, random access memory (RAM), and central processing unit (CPU) with pixel circuits on a single glass substrate. However, LTPS TFTs suffer from huge device-to-device variation due to the pulse-to-pulse variation of laser energy density and random distribution of grain boundaries, such poor uniformity makes the difficulty to fully integrate driving circuit using LTPS TFTs.

To realize integrating driving circuits using LTPS TFTs, output buffers are indispensable for the data driver to drive the large load capacitance of data lines. However, the poor uniformity of LTPS TFTs leads to the non-uniformity of buffer output voltage

across the panel which results in the wrong image displaying. Therefore, many researches employing LTPS TFTs have been tried to carry out analog buffers with high immunity of the device variations [2.4]-[2.17].

Analog buffer circuits using LTPS TFTs are classified into operational amplifier type (op-amp type) analog buffer and source-follower-type analog buffers according to their circuit architecture. Operational amplifier is most commonly used as the output buffer in single crystal silicon integrated circuits. However, the complicated circuit configuration and the huge output voltage variation of op-amp-type analog buffer using LTPS TFT make it not suitable for system-on-panel application. Source-follower-type analog buffer is considered a better candidate because of its simplicity and higher immunity to the device variations of LTPS TFT.

In this chapter, the circuit configuration, operating sequence, advantages and disadvantages of these two types of LTPS TFT analog buffers circuits are introduced. Those analog buffer circuits are simply classified into various types as shown in Fig. 2.1 based on the compensated methods [2.4]-[2.19]. The compensation principles of different types with configuration will be described in detail in this chapter. Furthermore, the output characteristics of the op-amp type analog buffer circuits and source-follower type analog buffer circuits are also discussed in this chapter.

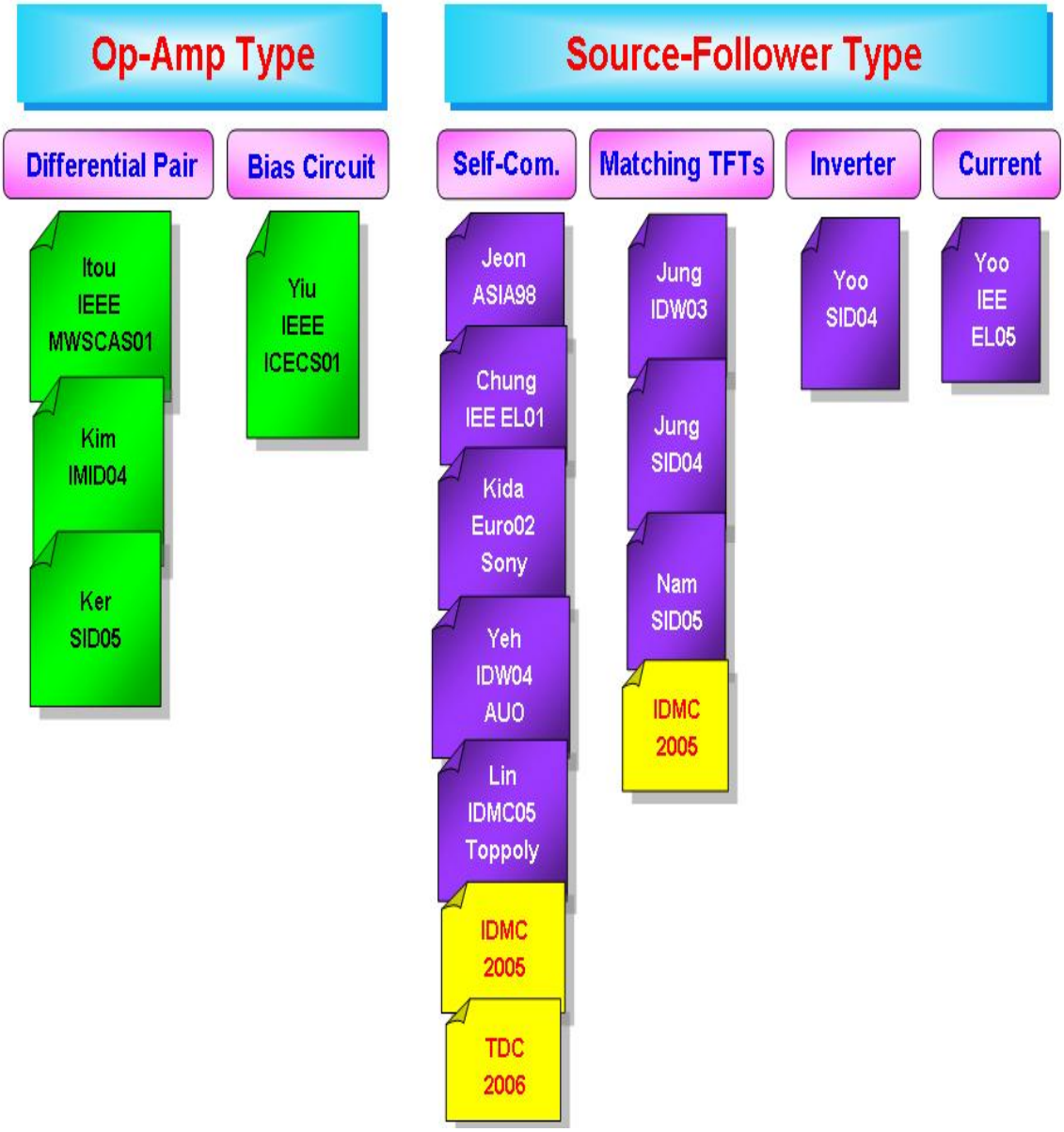

Fig. 2.1. Classification of compensation method for LTPS TFT analog buffer.

2.1.1 Architecture of AMLCD Driver

The block diagram of AMLCD display panel is shown in Fig. 2.2. The periphery circuits blocks of LCD panel are composed of scan driver, data driver, timing controller, DC/DC converter, gamma reference voltage driver, common voltage driver (Vcom driver). The timing controller decodes the output waveform to generate control signals at corresponding time, which is responsible for controlling the behavior of scan driver and transmitting the RGB (red, green, and blue) signals to the data driver. A DC-DC converter steps up a single externally supplied voltage to various higher level voltages (ex. VDD to 2VDD, 3VDD positive output voltage, and -2VDD, -3VDD negative output voltage) which provide the power supply voltage to the timing controller, interface circuit, source driver, gate driver, reference voltage driver and common voltage driver [2.20]-[2.21]. The gamma reference voltage driver is used to provide the various gamma reference voltages to the digital-to-analog converter (DAC) circuits. The common voltage driver is used to provide the common electrode voltage for the panel. Besides, the scan driver and data driver will be further discussed in the following.

- **Scan Driver**

The scan drivers generate the scan pattern and turn on each scan line sequentially. The architecture of source driver is shown in Fig. 2.3. It consists of shifter register, level shifter, and output buffer. The shift register is used to store digital input signal and transit them to the next stage, which generates sequential scan pulse for scan line according to the timing clock. The function of the level shifter is to translate the digital signal to a higher level voltage because the higher voltage is needed to turn on the switch element of the active pixel. Since the scan lines can be modeled as RC (resister and capacitor) ladder, the output

buffer is indispensable to drive the RC loading.

- **Data driver**

Fig. 2.4 shows the architecture of data driver which mainly contains shifter register, data register, level shifter, digital to analog converter (DAC) and output buffer. The first three stages are categorized as digital part, and the other two stages are belonged to analog part. The shift register generates pulse signal for video signal sampling according to the clock signal and transmit the pulse digital RBG signals to the next stage [2.22]. The data register receives the serial data signal and transmits them in parallel. The function of the level shifter is the same as the one used in the scan driver. It is applied to converter the digital RGB signal to a higher level voltage for data driver [2.23]. Because the data signal is transmitted in the digital interface, the digital to analog converter (DAC) is needed to convert the digital RGB video data into analog data signal for displaying the gray level [2.24]-[2.25]. Finally, the selected video data is transmitted to the data line after changing impedance in the output buffer. The purpose of output buffer is to assure the active pixels can be driven into a desired gray level. When the digital to analog converter is insufficient for driving the large loading of data line, the output buffer is used to enhance its driving capability. As the output buffer is applied, the DAC will charge a smaller loading of output buffer instead of a larger loading of data line. Thus, the desired data signal can be transmitted to the active area accurately. Because the LCD panel usually has large loading, especially in larger panel or higher resolution display, the analog buffer is indispensable to drive the large loading of the data lines.

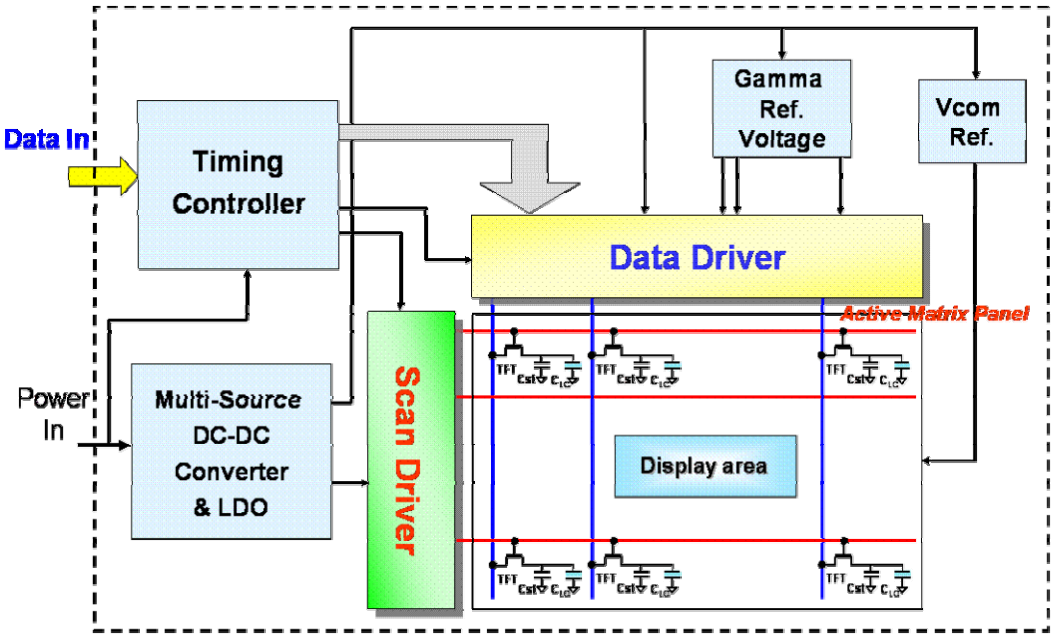

Fig. 2.2. Block diagram of display panel.

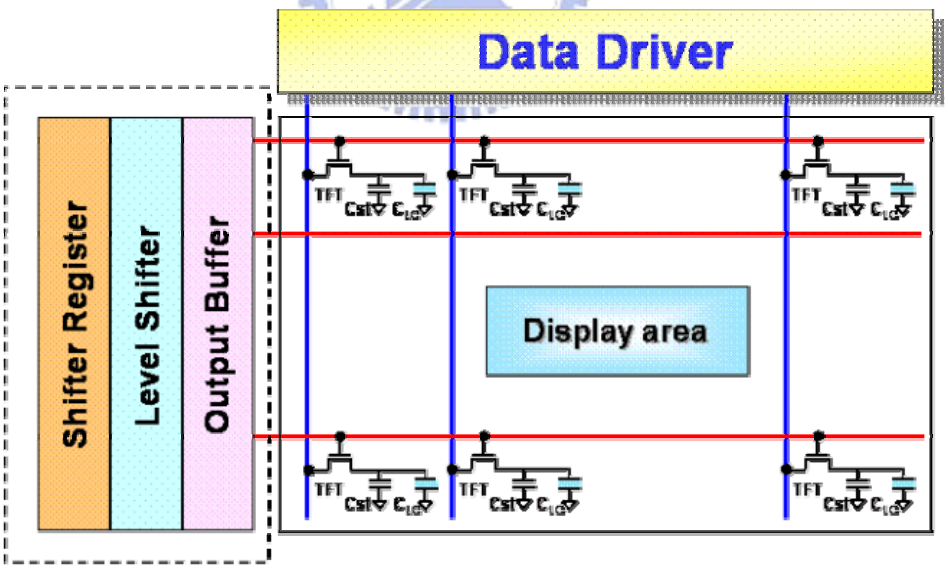

Fig. 2.3. Architecture of the scan driver.

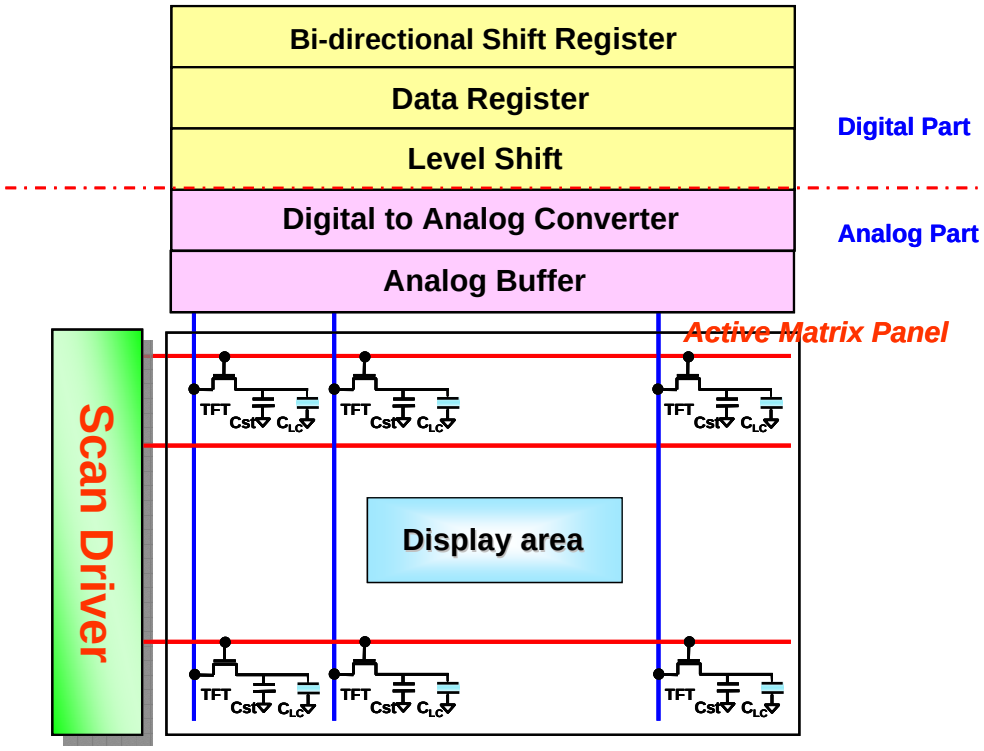

Fig. 2.4. Architecture of the data driver.

2.1.2 Design Considerations for LTPS-TFTs Analog Buffer

To design the output buffer for the data driver of flat pane display, there are several critical issues to be considered. These include output voltage accuracy, driving capability, layout area, and power consumption.

(1) Output voltage accuracy: Analog buffer is applied to the data driver for ensuring that the data signal outputted from DAC can be transmitted exactly to the active pixel. Thus, the high output voltage accuracy of analog buffer circuits is required to display the desired gray level correctly.

(2) Driving capability: The output settling time for the data drivers must be fast enough to quickly transfer the data signals into the pixels within a line time. Therefore, the analog buffers in the end of data driver must quickly charge or discharge the load capacitance of data bus. Especially in the larger panel area and higher resolution display, the line time becomes shorter while the loading of data line is large. High driving capability of the output buffer is needed to achieve fast transition time and to get sufficient capability for driving large loading of data lines.

(3) Layout area: For the LAAT (line at a time) driving architecture, one analog buffer is needed for each column line. Thus, several hundreds of analog buffers are needed in active matrix display. As the resolution is higher and higher in the future, the amount of analog buffers is increasing and larger area will be occupied. Moreover, a data driver should fit in one pixel pitch, and circuit layout area is limited. Therefore, the simple configuration and less transistors are pursued for high-resolution display.

(4) Power consumption: The power consumption of poly-Si TFT integrated circuits tends to be higher than that of single-crystalline silicon ICs because of inferior electrical characteristics of poly-Si TFT such as higher threshold voltage, lower carrier mobility. For the expanding market of mobile and portable production, the demand of power dissipation is increasing. Since several hundreds of analog buffers are needed in the LAAT (line at a time) driving architecture, large static power is dissipated of analog buffers. Therefore, it needs to design an analog buffer with low power consumption.

2.2 Op-amp-type Analog Buffer

2.2.1 Typical Op-amp-type Analog Buffer

Operational amplifier (op-amp) is generally connected as an unit-gain buffer to act as the output buffer in the single crystal silicon LSIs. A typical two-stage operational amplifier (op-amp) is composed of a differential amplifier and an output stage as shown in Fig. 2.5.

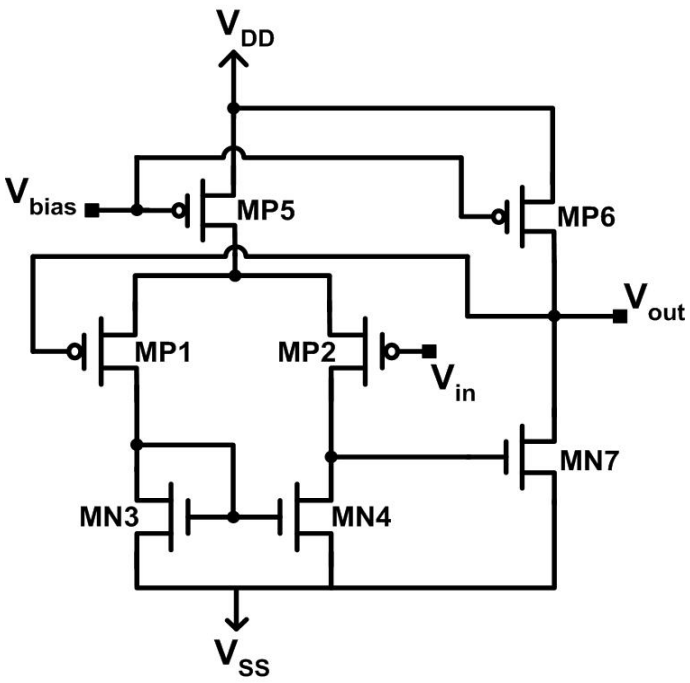

Fig. 2.5. Simple two-stage op-amp unit gain buffer.

The output voltage versus input voltage characteristic and output offset voltage of a typical two-stage op-amp unit-gain buffer employing LTPS TFTs are shown in Fig. 2.6, where the offset voltage is defined as the difference between the input voltage and output

voltage, (i.e. Voffset=Vinput -Voutput). The simulation result shows the good linearity of the op-amp unit-gain buffer. The output offset voltage is average under 30 mV expect when the input voltage is in low level where the offset voltage may exceed 150mV.

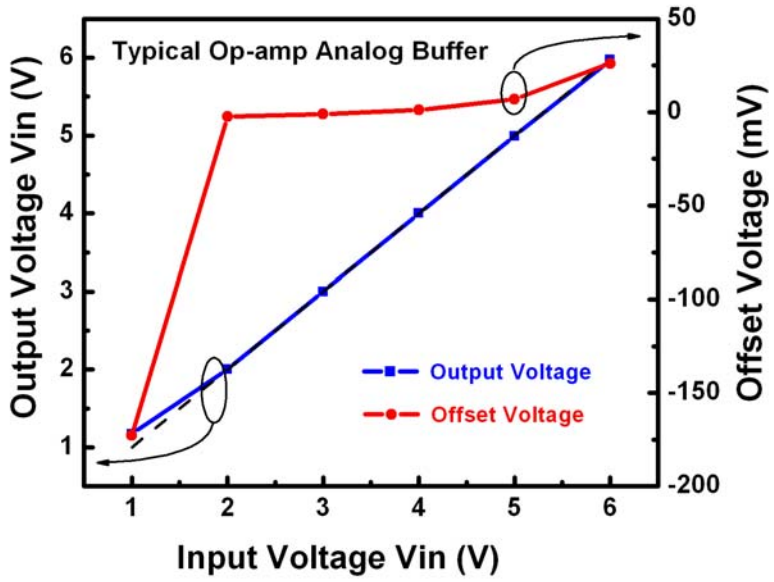

Fig. 2.6. Simulation result of the offset and output voltage versus input data voltage for typical two-stage op-amp type analog buffer circuit.

Although the output error of the typical op-amp type analog buffer is small, huge output voltage variation may exist in this circuit because of the inevitable non-uniformity of the poly-Si TFTs electrical characteristics, such as threshold voltage and mobility variations. In order to study the effect of device non-uniformity on the circuit performance, Monte Carlo simulation with an assumption of normal distribution is introduced where the mean value and deviation of the threshold voltage and the mobility are 1.45V, 0.5V and 65.69 cm^2/V-sec, 15 cm^2/V-sec, respectively. Each poly-Si TFTs are assumed to vary independently when the Monte Carlo simulation is executed. Fig. 2.7 shows the Monte Carlo simulation results of the two-stage op-amp unit gain buffer. It is obvious that the

output voltage has huge variations, where the variation of output offset voltage may get up to 1450mV. This serious output variation makes it difficult to design a high performance output buffer with the typical op-amp-type analog buffer. Therefore, some compensating methods have been proposed to solve this problem. These compensating methods for op-amp type analog buffer will be discussed in the next section.

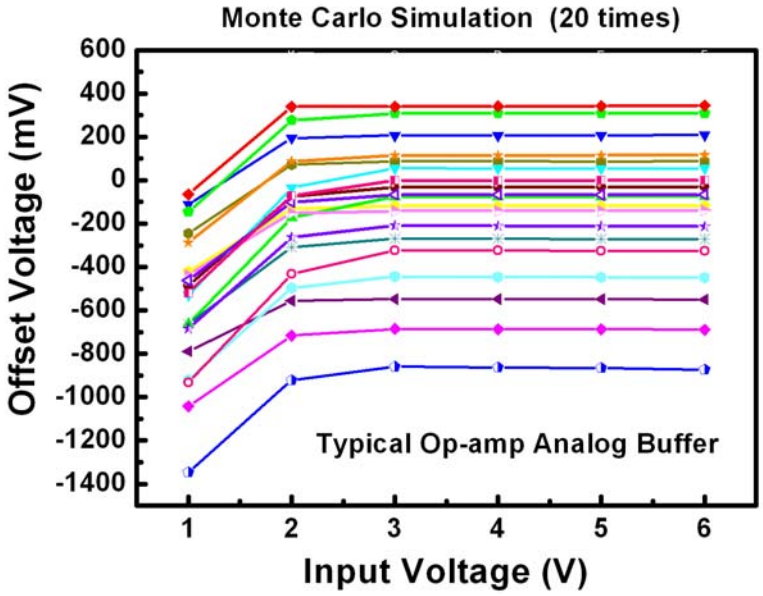

Fig. 2.7. Monte Carlo Simulation result of the typical op-amp-type analog buffer with input voltage varying from 1V to 6V.

2.2.2 Op-amp-type Analog Buffer with Compensated Architecture

The compensating methods for device-to-device variation of LTPS-TFTS op-amp-type analog buffer can be mainly classified into two kinds including differential pair compensated method and bias circuit compensated method. The concepts and operating method of these two kinds of compensating circuits will be discussed in detail.

2.2.2.1 Differential Pair Compensated Method

For the differential pair compensated method, an additional capacitor is used to compensate the device mismatch of the differential pair stage. The operating period usually includes two stages. First is the period to calibrate the electrical properties mismatch of the differential pair and the second stage is the signal data voltage programming period. Fig. 2.8 shows an example of this type of compensating method. The op-amp-type unit gain buffer with threshold voltage and mobility deviation-free differential amplifier was reported by Itou [2.4]. Comparing to the typical two-stage op-amp type analog buffer, one capacitor and three switches are added to the differential pair stage. The operating period including two stages: first is the calibration mode, and second is the operation mode.

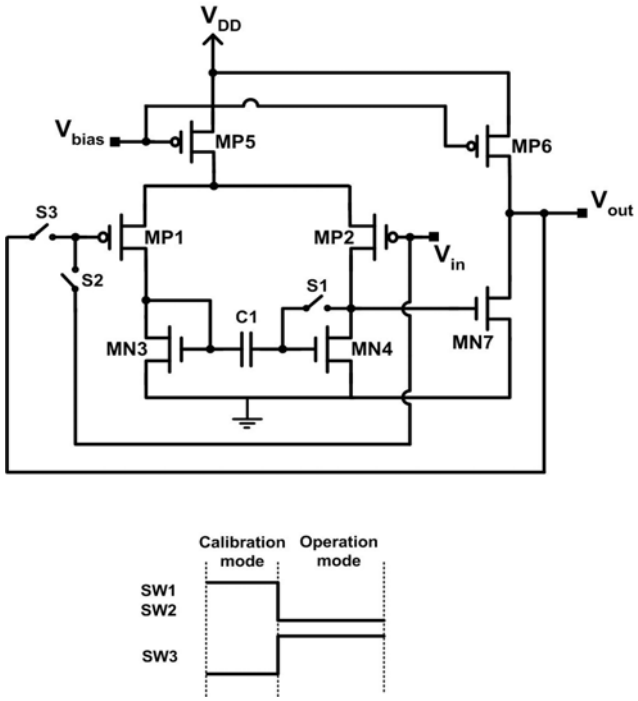

Fig. 2.8. Circuit configuration and timing diagram of Itou's differential amplifier compensated op-amp-type unit gain buffer.

In the calibration mode, switches S1 and S2 are on, and S3 is off. At this time, the two input voltages of the differential pair (MP1, MP2) are the same, and the difference of gate to source voltages between the active load pair (MN3, MN4) is stored in the capacitance C1. The gate voltage of the active load is corresponding with the threshold voltage of the differential pair and the active load. Therefore, the differential pair mismatch and the load pair mismatch are stored in the capacitance C1. When the switches S1 and S2 are off, and S3 is on, the circuit is in the operation mode. In this mode, the input data is transmitted to the output stage. Since the differential pair mismatch and the load pair mismatch have been recorded in the first stage, the input offset resulting from device mismatches can be fully canceled in the operation mode. Thus, the final output voltage will be close to the input data signal in this buffer circuits.

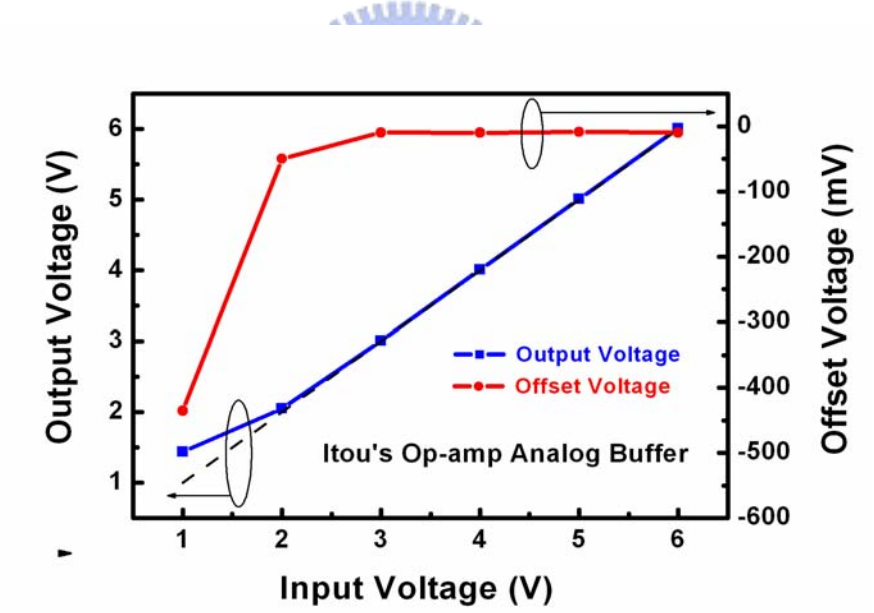

Fig. 2.9. Simulation result of the offset and output voltage versus input data voltage for Itou's differential pair compensated op-amp-type analog buffer circuit.

The output performance of Itou's op-amp analog buffer has been studied by simulation results. Fig. 2.9 shows the output voltage-input voltage characteristic and the output offset of the buffer. The output deviation is small except in low input data signal. The Monte Carlo

simulation result is also shown in Fig. 2.10. It is obvious that the output offset variation of this buffer circuits is much smaller than that of the typical two-stage op-amp-type analog buffer. However, the output variation still remains large (~550mV) in low input data level. It is because that when the input data is in low level, the two transistors of the differential pair (MP1, MP2) operate in the linear region. Thus, the transconductance (gm) of two transistors of the differential pair are not kept in constant which result to the differential pair mismatch and the load pair mismatch cannot be recorded accurately in the capacitance C1 and result in the output performance sensitive to the device variation. Besides, the mismatch of the output stage of the analog buffer also contributes to the output variation of the Itou's op-amp-type analog buffer.

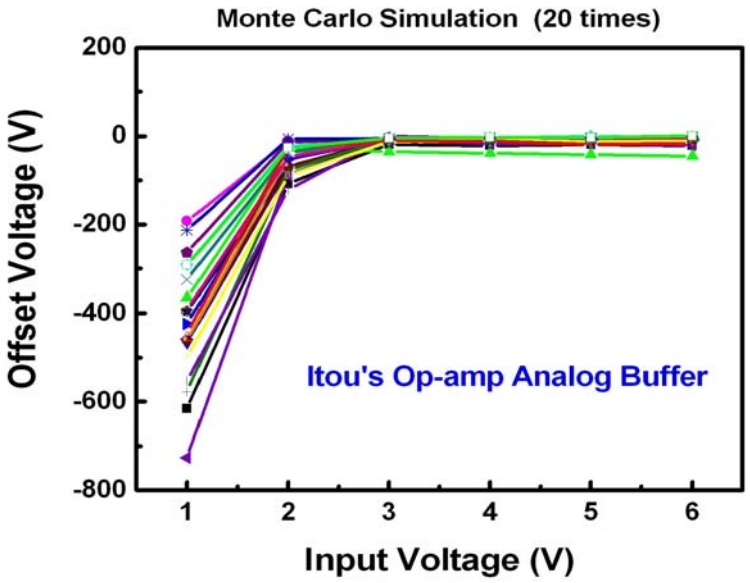

Fig. 2.10. Monte Carlo Simulation result of the Itou's op-amp-type analog buffer with input voltage varying from1V to 6V.

2.2.2.2 Bias Circuit Compensated Method

In the bias circuit compensated method, a threshold voltage insensitive gate bias

voltage generating circuit is applied to eliminate the influence of threshold voltage variation on the bias current. Fig. 2.11 shows an example of op-amp-type analog buffer using this compensating method [2.7]. This buffer circuit is composed of a typical two-stage op-amp unit gain buffer and the threshold voltage insensitive gate bias generating voltage.

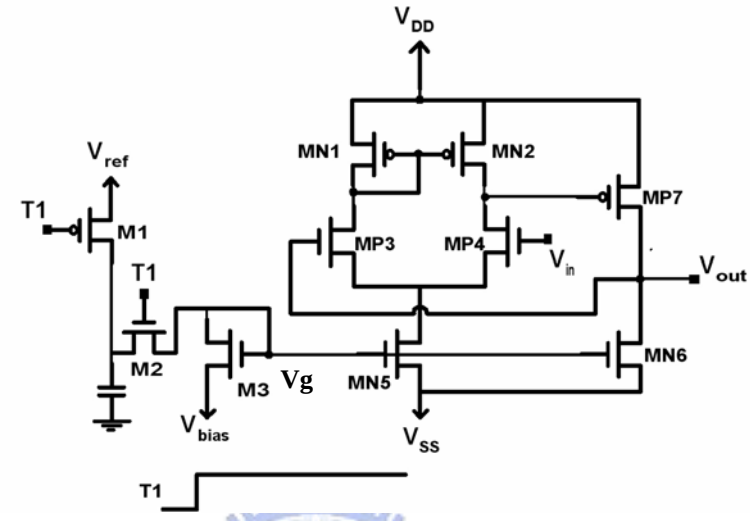

Fig. 2.11. Circuit configuration and timing diagram of Yiu's bias circuit compensated op-amp-type unit gain buffer.

The bias current of this op-amp can be expressed as :

$$I_d = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{MN5}\left(V_{gs\_MN5} - V_{th\_MN5}\right)^2 \qquad (2.1)$$

When there is large variation in threshold voltage that will causes bias current variation, thus the variation of g_m (transconductance). This in turn causes the non-uniformity of the buffer circuit characteristics across the panel. Therefore, eliminating the effect of threshold voltage variation on bias current may maintain the output characteristics of the op-amp unit-gain buffer. Thus, Yiu propose a gate voltage biasing circuit to provide an insensitive bias gate voltage Vg, (refer to Figure. 2.10) for biasing the transistors. The operation of this

compensating circuit is described in the following. In the first stage, the transistor M1 turns on, and the capacitor will be charged up to Vref. Then transistor M1 turns off and transistor M2 turns on to connect the capacitor to transistor M3. Since transistor M3 is connected like a diode, it will discharge the capacitor until the gate voltage of the transistor M3 is equal to $V_{bias} + V_{th}$. Then this voltage is applied to the gate of MN5, MN6 to provide the bias current:

$$I_d = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{MN5}\left(V_{bias} + \cancel{V_{th\_MN3}} - \cancel{V_{th\_MN5}}\right)^2 \quad (2.2)$$

and

$$I_d = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_{MN6}\left(V_{bias} + \cancel{V_{th\_MN3}} - \cancel{V_{th\_MN6}}\right)^2 \quad (2.3)$$

The bias current will be independent of the threshold voltage of the transistor if the transistor MN3, MN5 and MN6 are matched. Therefore, the output non-uniformity of the op-amp type analog buffer resulting from the bias current fluctuation can be eliminated in this compensating circuit architecture.

Fig. 2.12 and Fig. 2.13 show the simulation results of the output offset voltage and the output variation versus input data voltage, respectively. It is clear that large output variation still remains in this compensating circuit. It means that the electrical performance variations can not be calibrated out in this compensating architecture. It is because that the compensating method is performed in the bias circuits but not the differential pair. Even if the bias current mismatch has been compensated, the device mismatch of the differential pair and the active load pair which are the mainly causes of output variation for op-amp-type unit gain buffer still remain. Besides, the compensating configuration will

work effectively only when the electrical characteristic MN3, MN5 and MN6 are matched, but it is very difficult to achieve completely device matched between transistors. In addition to large output variation, extra setup time is also required for the application of this buffer circuit to generate the threshold voltage insensitive bias voltage. Furthermore, op-amp-type analog buffer needs many transistors which not only occupy large area but cause high power dissipation. Therefore, the op-amp-type analog buffer is not suitable for the driver integration applications.

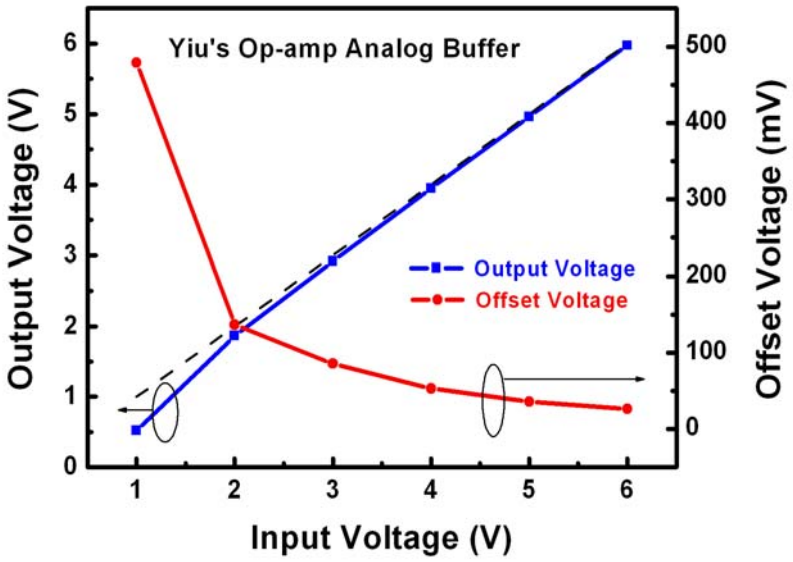

Fig. 2.12. Simulation result of the offset and output voltage versus input data voltage for Yiu's bias circuit compensated op-amp-type analog buffer circuit.

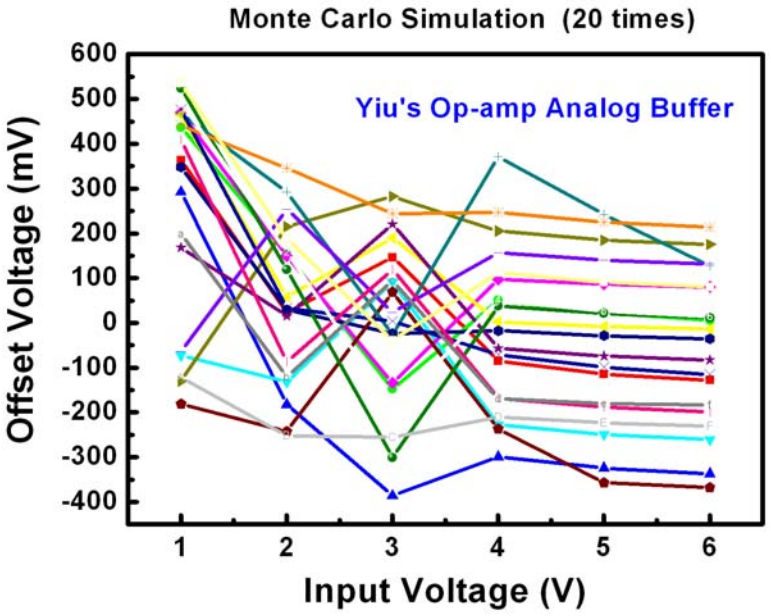

Fig. 2.13. Monte Carlo simulation result of theYiu's op-amp-type analog buffer with input voltage varying from1V to 6V.

2.3 Source-Follower Type Analog Buffer

2.3.1 Conventional Source-Follower Type Analog Buffer

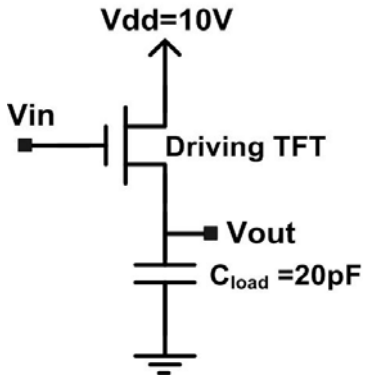

Fig. 2.14. Conventional source-follower type analog buffer.

Conventional source-follower type analog buffer is a very simple configuration as shown in Fig. 2.14. In order to realize the output characteristic of this circuit, HSPICE simulator is used. The simulation result of the output offset versus input voltage is shown in Fig. 2.15. Due to the intrinsic turn on characteristic of the transistor, an offset voltage about the same value to the threshold voltage will exist in the conventional source-follower type analog buffer. As shown in Fig. 2.15, the offset voltage is about 1400mV that is close to the threshold voltage of the LTPS TFTs model we used in this work. Twenty times Monte Carlo simulation is also executed to understand the effect of device variation on the output performance of the conventional source-follower type analog buffer. As shown in Fig.2.16, it is clear that the output offset variation of the conventional source-follower type analog buffer is smaller than that of the typical two-stage op-amp type analog buffer, but huge output variations still exist since the LTPS TFTs device variations. Therefore, the compensating circuit is required to eliminate the device variations for achieving high accurate output performance of source-follower type analog buffer circuits.

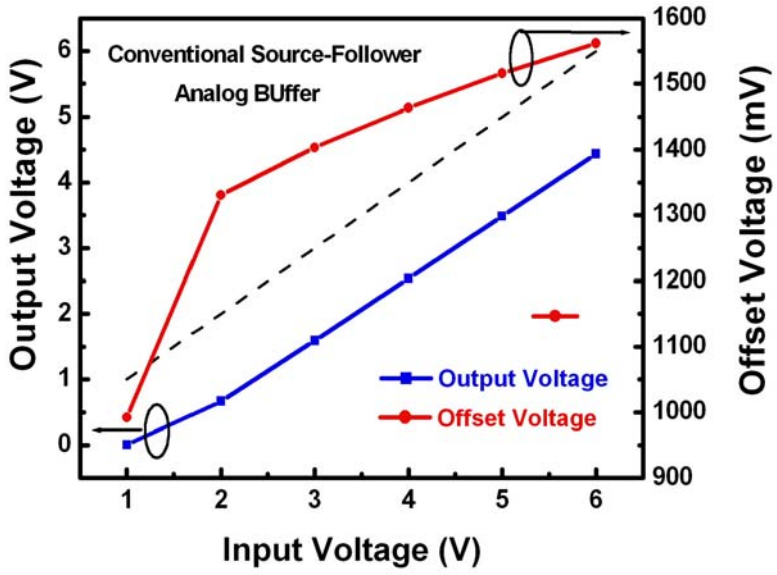

Fig. 2.15. Simulation result of the output voltage and output offset voltage versus input voltage of conventional source-follower type analog buffer.

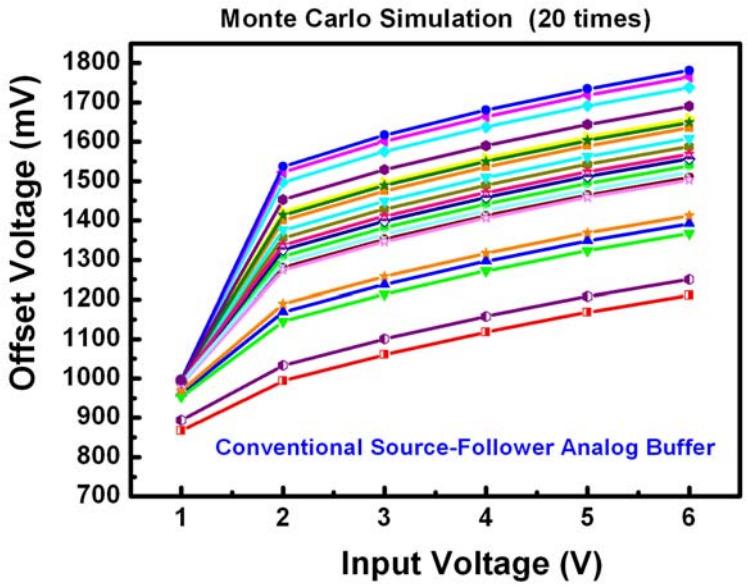

Fig. 2.16. Monte Carlo simulation result of the output offset voltage of conventional source-follower type analog buffer.

2.3.2 Source-Follower Type Analog Buffer with Compensation Architecture

2.3.2.1 Self-Compensation Method

The so-called self-compensation method is to compensate the own threshold voltage variation of the driving TFT. It is usually carried out by an additional capacitance. There are usually two main operating stages in this compensating method. First is the so-called calibration period. The threshold voltage of the driving TFT is stored in the additional capacitance in this stage. Then comes the data input period to transmit the data signal, and the threshold voltage of the driving TFT that has been recorded in the first stage will be canceled out in the second operating stage. Thus, the threshold voltage insensitive source-follower type analog buffer can be obtained with this compensating method. Here

are tow examples of this kind of compensating method, one is the “Push-Pull” analog buffer reported by Chung in 2001 [2.9] and the other is the “Double Offset Canceling” analog buffer proposed by Kida in 2002 [2.10].

- **Chung’s Push-Pull Analog Buffer**

The circuit configuration and the timing diagram of Chung’s push-pull analog buffer are shown in Fig. 2.17. It is composed of a complementary source follower output stage, three switches, and a capacitance. The NTFT pushes up current to the output load and the PTFT pulls down current from the load; thus, it is called “push-pull” analogue buffer. The operation sequence and the compensating concept of this analog buffer will be described in the following.

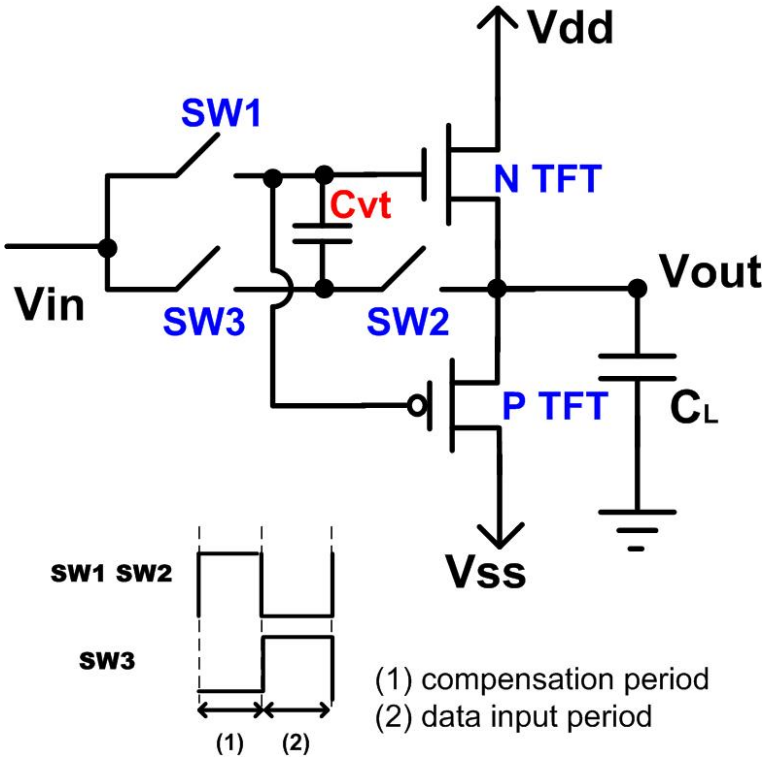

Fig. 2.17. Circuit configuration and timing diagrams of Chung’s push-pull analog buffer.

There are two operating stages for this buffer circuit: first is the compensation period, and second is the data input period. During the first compensation period, switches SW1 and SW2 are turned on and SW3 is turned off. An analog signal (Vin) is applied to the gate of the driving transistors. Then the buffer output voltage will reaches Vin-V_{TN}. Thus,the threshold voltage of NTFT will be stored in the additional capacitance Cvt. Then switches SW3 is turned on, and SW1 and SW2 are turned off. The buffer circuit is in the data input period at this time. The gate voltage will become the input voltage added to V_{TN}, Vgate = Vin + V_{TN}, because the threshold voltage of the NTFT has been stored in first compensation period. Thus, the output voltage of this circuit will reach to Vin, $Vout = Vgate - V_{TN} = Vin - V_{TN} = Vin$. In a similar way, the negative analog voltage signal is buffered by the P-type driving transistor after compensating the threshold voltage of the PTFT. In this way, the output voltage will be independent of the threshold voltage of the driving TFT. Therefore, wide threshold voltage variations of poly-Si TFTs can be compensated by this method.

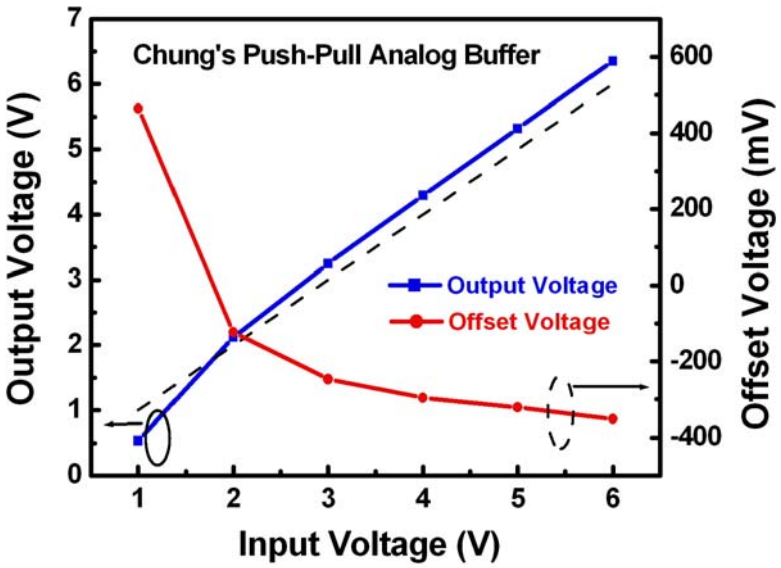

Fig. 2.18. Simulation result of the output voltage and output offset voltage versus input voltage of Chung's push-pull analog buffer.

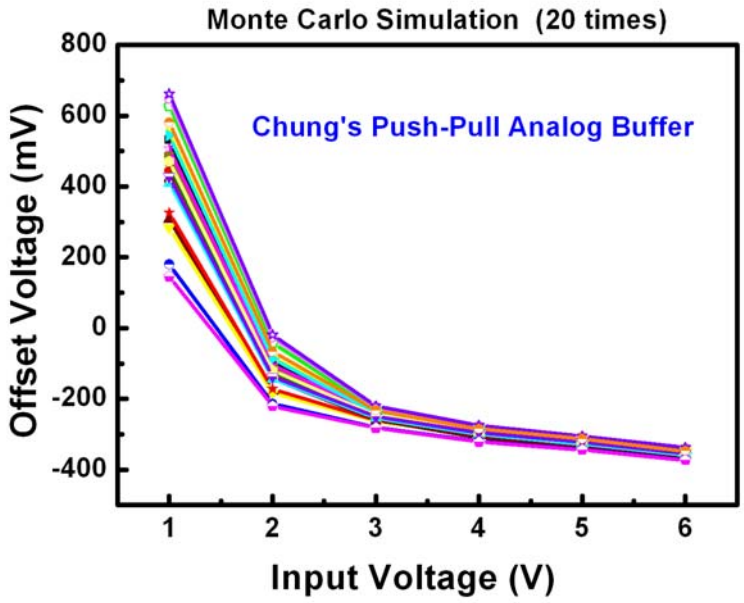

Fig. 2.19. Monte Carlo simulation result of the output offset voltage of Chung's push-pull analog buffer.

Fig. 2.18 and Fig. 2.19 show the simulation results of the output offset voltage versus input voltage and the output variation versus input voltage, respectively. It is obvious that the offset voltage and the output variation are much smaller than that of conventional source-follower type analog buffer due to threshold voltage variation compensated through capacitor Cvt. However, the output error and output variation of this circuit are still large for real product applications. That can be attributed to several causes. The first is the charge loss of the threshold holding capacitor (Cvt); the second is the poor subthreshold characteristic of LTPS TFTs that causes an exact threshold voltage of driving TFT cannot to be stored in the capacitor Cvt. The last cause is that the driving TFT may not be biased at the same gate-to-source voltage during two operating stage. The offset voltage stored in the capacitor Cvt during the first stage is not equal to the actual offset of this circuit. Thus the offset can not be fully canceled by this compensating method. Therefore, Kida et al. of Sony Cop. proposed a modified compensating method named "Double offset canceling" in 2002 which

will be introduced in the following.

- **Sony's Double-Offset-Canceling Analog Buffer**

The compensating concept of the Sony's double-offset-canceling analog buffer is the same with the Chung's push-pull analog buffer. It uses the capacitors to compensate the own threshold voltage variation of the driving TFT. The only difference between these two analog buffers is that the offset calibrating is executed two times in Sony's double-offset-canceling analog buffer. Fig. 2.20 shows the circuit configuration and the timing diagram of double-offset-canceling analog buffer. The analog buffer is the source follower circuit which is composed of one N-type TFT, seven switches, two capacitors, and a constant current source.

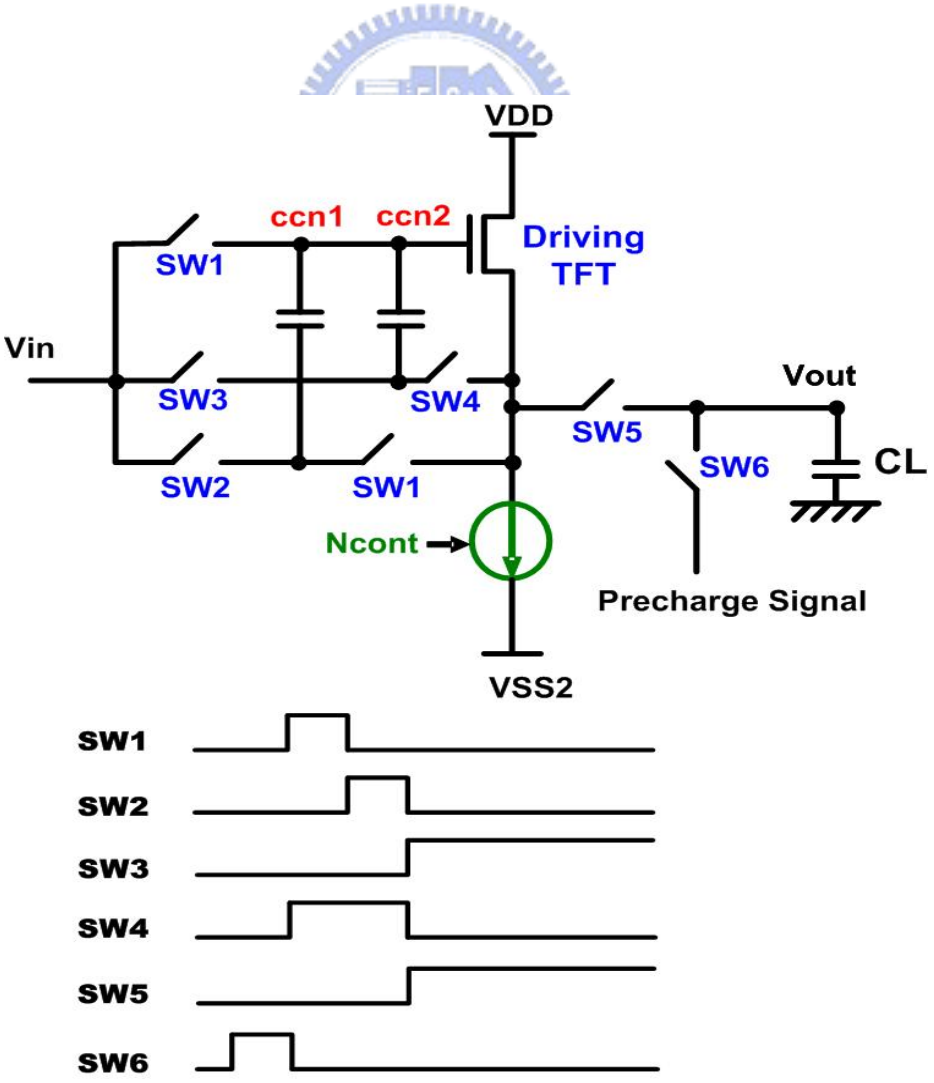

Fig. 2.20. Circuit configuration and timing diagrams of Sony's double-offset-canceling analog buffer.

The operation of this analog buffer is as follows. When Ncont is active, this buffer circuit goes active. The switch SW6 turns on first to discharge the C_L voltage level. Then the switches SW1 and SW4 turn on to supply analog data level from DAC to stored the first offset voltage of the source follower in the capacitor ccn1. Next, SW1 turns off, and SW2 turns on. The gate of the driving TFT becomes Vg=Vin+Vgs(1) at the time. Thus the second offset voltage is produced and stored in the capacitor ccn2. Then both SW2 and SW4 turn off, and SW3 and SW5 turns on to sampling the data to the output terminate. When the first offset cancellation is executed, the operating point reaches nearly to the output signal level that makes the stored voltage in the ccn2 come very close to the actual offset voltage. Therefore, highly accurate output voltage can be achieved by precisely canceling the offset voltage of the source follower.

Fig. 2.21 and Fig. 2.22 show the simulating results of the output offset voltage and the output variation of this buffer circuit. It is obvious that the output offset voltage is very small by twice calibrating the offset of the buffer circuit. Besides, the output voltage of this buffer is almost independent to the threshold voltage variations of the driving TFT because the output voltage is nearly irrelative to the threshold voltage of the driving TFT by applying the double-offset-canceling method. Although highly precise offset canceling can be achieved in this compensating circuit, it requires many transistors, many control signals, two capacitors, and a stable current source. Consequently, it must occupy large area and need complicated operation. Furthermore, the variations of the constant current source employed by the LTPS TFTs will influence the output performance of the circuit that cannot be ignored.

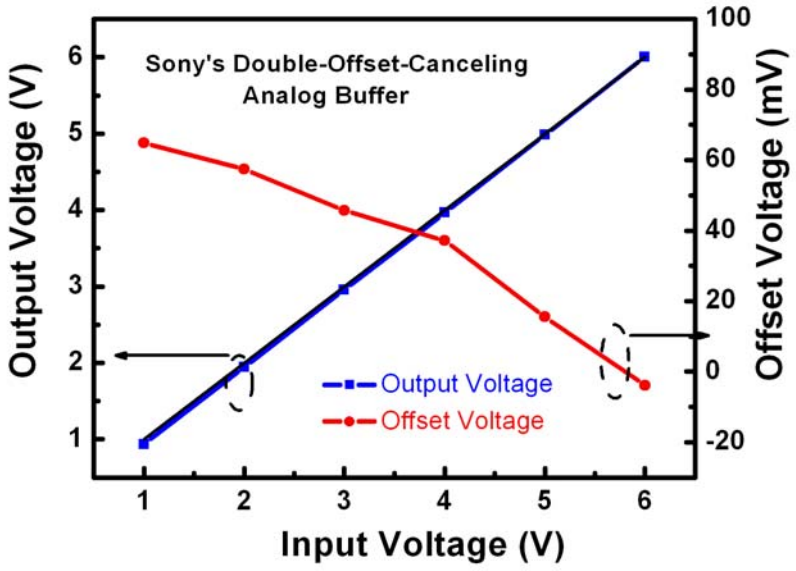

Fig. 2.21. Simulation result of the output voltage and output offset voltage versus input voltage of Sony's double-offset-canceling analog buffer.

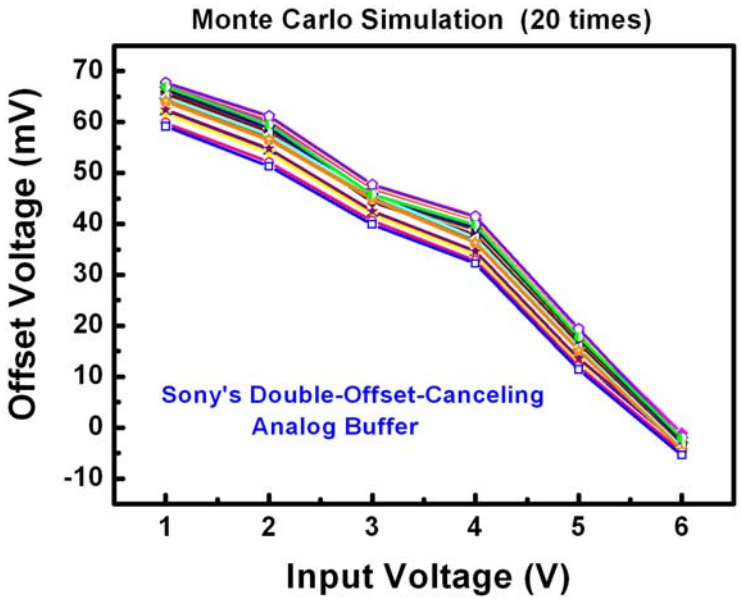

Fig. 2.22. Monte Carlo simulation result of the output offset voltage of Sony's double-offset-canceling analog buffer.

2.3.2.2 Matching TFTs

For the analog buffer employed the concept of matching TFTs, the function of driving TFT is to output the analog voltage, an additional diode connected transistor is used to provided a threshold voltage of the transistor for canceling out the influence of threshold voltage on the circuit output characteristics.

Jung's analog buffer as show in Fig. 2.23 is an example of the compensating circuit with the concept of matching TFTs [2.13]. The operating sequence is described as follows. First, reset signal is high to reset the previous data voltage in the load capacitor. Then the data signal is applied. As the voltage of node A is higher than that of node B, N1 turns on and N2 turns off. The gate of the driving TFT N3 becomes about $Vin-Vth\_{N1}$ by diode connected of N1 and N3 turns on. Then N4 is turned on when "active" signal is high. Since the gate node of N3 is floating, the gate of N3 will be charged up by the bootstrapping effect through power supplied line until $Vdata+Vth\_{N2}$ is reached and then the transistor N2 is turned on while N1 is turned off. The gate of N3 is no longer floating as this time, so the action of bootstrapping is stopped. Finally, the output voltage will reach to $Vdata+Vth\_{N2}-Vth\_{N3}$. If the transistors N2 and N3 are matched, the output voltage will be equal to Vdata, and the offset voltage of source follower can be eliminated. However, the device characteristic of one transistor is impossible to match another completely in reality. Fig. 2.24 and Fig. 2.25 show the simulating results of this analog buffer, in which the mismatch of driving TFT (N3) and the compensating TFT (N2) is taken into consideration. It is obvious that the output offset voltage and the output variations due to threshold voltage variations of driving TFT are still large. It means that the threshold voltage variations of the driving TFT cannot be compensated efficiently using matching-TFTs compensating method.

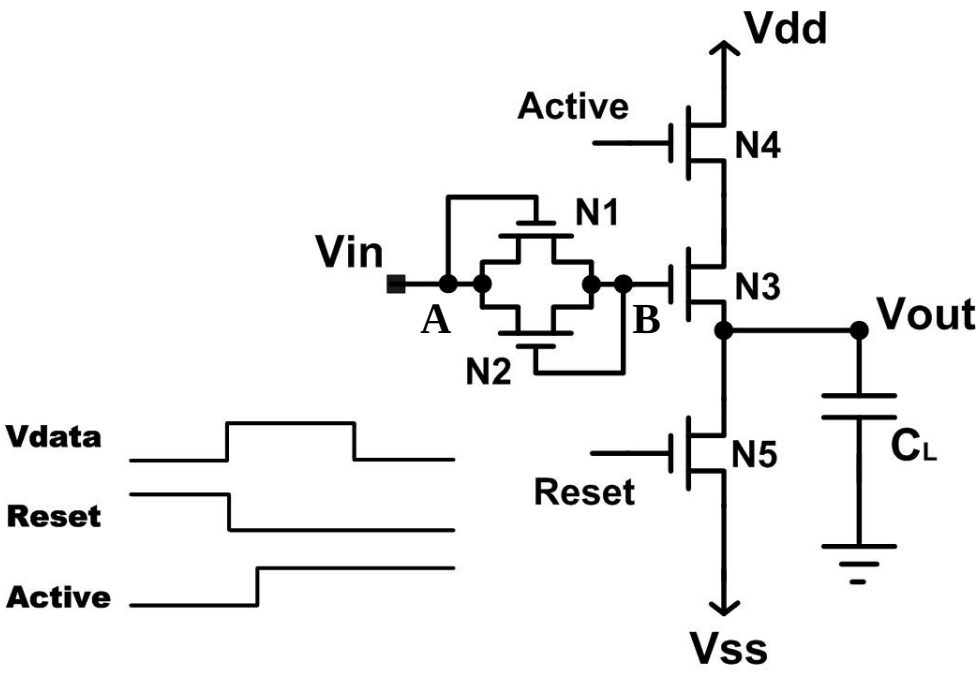

Fig. 2.23. Circuit configuration and timing diagrams of Jung's analog buffer.

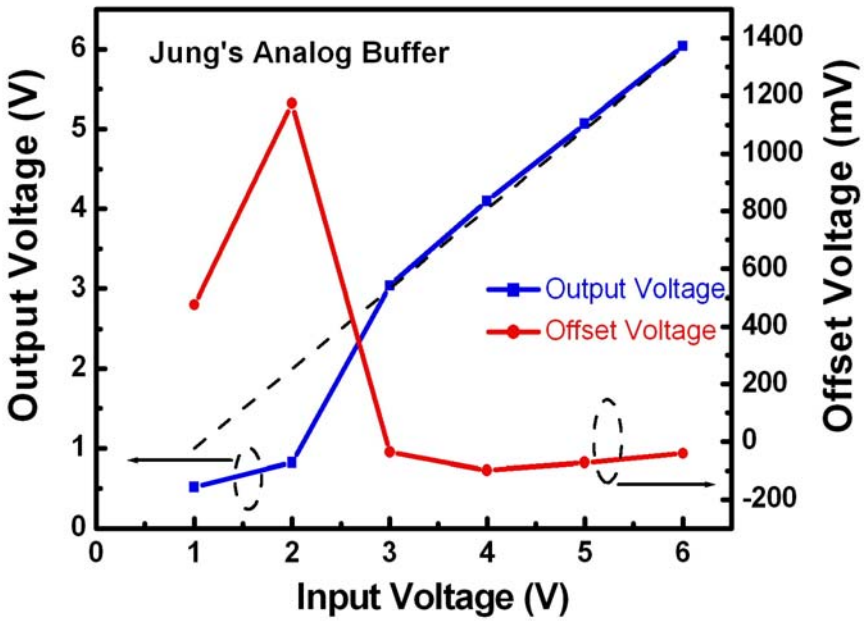

Fig. 2.24. Simulation result of the output voltage and output offset voltage versus input voltage of Jung's analog buffer.

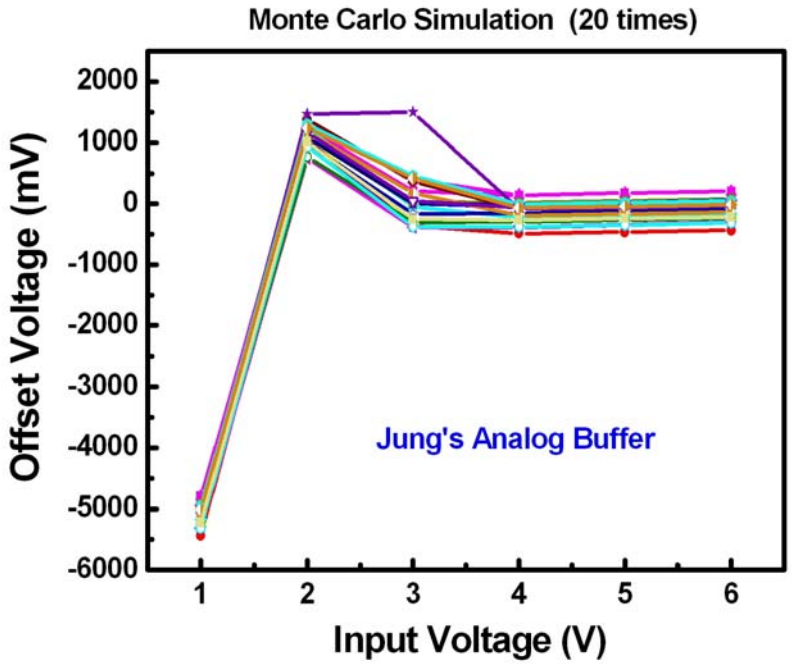

Fig. 2.25. Monte Carlo simulation result of the output offset voltage of Jung's analog buffer.

2.3.2.3 Inverter Type

The purpose of this compensating method is to calibrate out the influence of parasitic capacitances of driving transistor. In the self-compensation method, a compensating capacitor is used to store the threshold voltage of driving TFT in first operating period. Thus in the data input stage, the gate voltage of the driving TFT becomes Vin+Vth. However, the capacitance coupling by parasitic capacitances of Cgd and Cgs in the driving TFT will make the gate voltage of driving TFT not equal to this target voltage. As shown in Fig. 2.26, the real gate voltage of the driving TFT can be represented as equation (2.4).

$$V_{GATE} = V_{INPUT} + \frac{C_{COMPENSATION}}{C_{COMPENSATION} + C_{PARASITIC}} \times V_{TH} \quad (2.4)$$

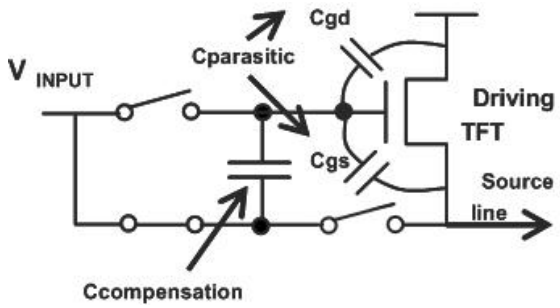

Fig. 2.26. Structure of source follower with compensating capacitance.

In order to solve this problem, Yong-Su Yoo has proposed an inverter type compensating circuit in 2004 [2.16]. The circuit configuration and timing diagrams of Yoo's inverter type analog buffer is shown in Fig. 2.27. It consists of one p-type driving TFT two inverters, four capacitors and eight switches. The operating principle of this buffer circuit is very complicated. In brief, the output voltage will final keep in the value of input voltage times a γ factor and plus a DC voltage level V_{COM_LOW} by the operation of these two inverters, and the coupling of four additional capacitors and the parasitic capacitances. In which, the γ factor is related to the capacitors C1, C2, C3, C4 and Cparasitic. Thus, the output voltage of this buffer circuit is independent of the threshold voltage of driving TFT. Furthermore, the influence of capacitor coupling by the parasitic capacitors of Cgd and Cgs of driving TFT will be eliminated by carefully adjusting the dimension of additional four capacitors.

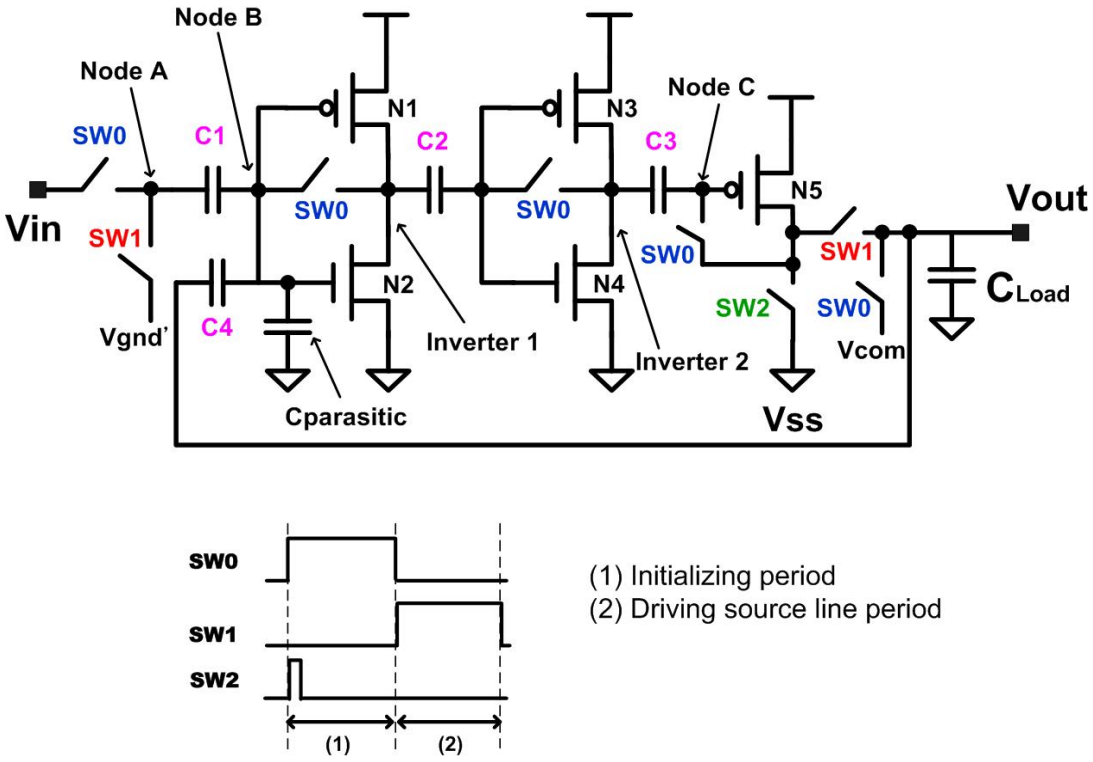

Fig. 2.27. Circuit configuration and timing diagrams of Yoo's inverter type analog buffer.

This type of compensating method needs too many transistors and four additional capacitors. Such complicated circuit configuration may occupy large area and cause high power consumption. In conclusion, it is not practical for real product application. Therefore, the output characteristic of this compensating circuit wouldn't be discussed in this section.

2.3.2.4 Current Type

Fig. 2.28 shows the circuit configuration and the timing diagram of one example of current type compensating buffer circuit, which is proposed by C. Yoo in 2005 [2.17]. It consists of a pair of nMOS and pMOS TFTs, four control switches and a storing capacitor. The operating concept of this buffer circuit is as follows. During the input signal sampling period, the switches S1 and S3 are turned on while the others are open. Since the drain

currents of M1 and M2 are equal. The gate to source voltage of M2 is established and stored on the capacitor as the gate voltage of M1 is equal to Vin. The switches S1 and S3 are then open, and switches S2 and S4 are turned on to enter the driving period. The drain current of M1 and M2 are the same during this period. Because the gate to source voltage of M2 is determined and stored in the storage capacitor at the input signal sampling period, the drain current of M2 during the driving period is the same as that during the input signal sampling period and so dose the drain currents of M1. It means that the gate to source voltage of M1 should also be equal during both periods. Therefore, the output voltage is the same as the input voltage regardless of the threshold voltage and mobility of the N-type and P-type TFTs.

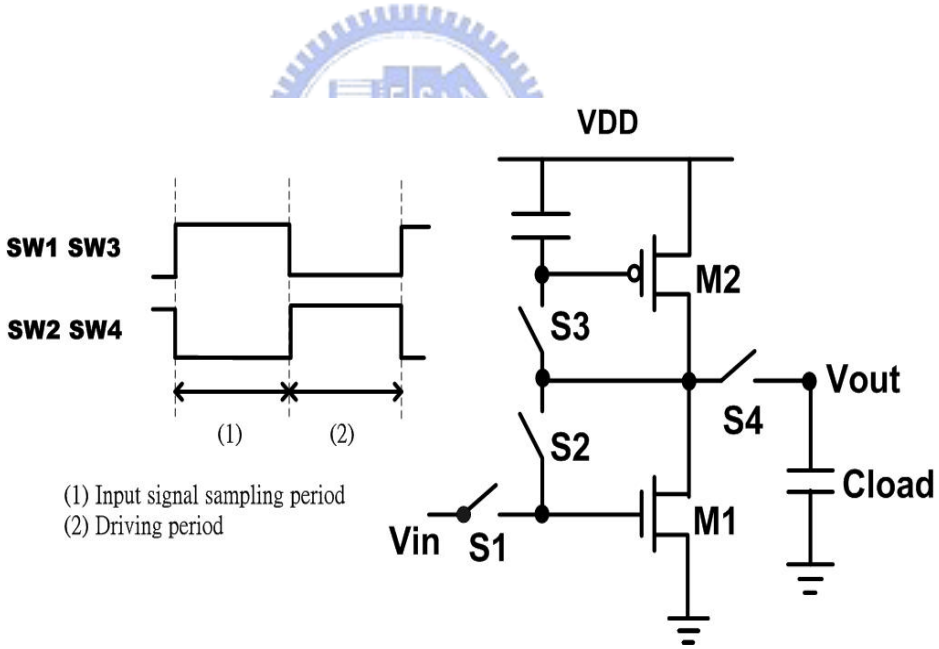

Fig. 2.28. Circuit configuration and timing diagrams of Yoo's current type analog buffer.

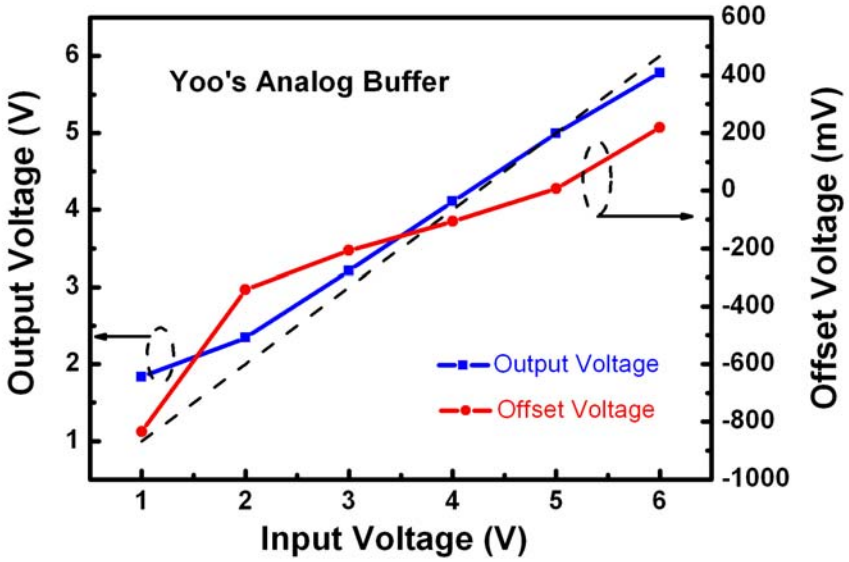

Fig. 2.29. Simulation result of the output voltage and output offset voltage versus input voltage of Yoo's analog buffer.

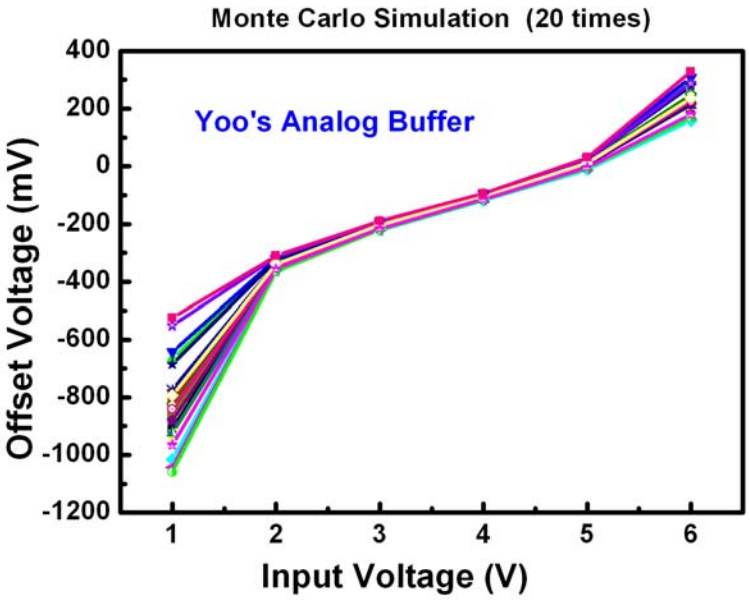

Fig. 2.30. Monte Carlo simulation result of the output offset voltage of Jung's analog buffer.

Fig. 2.29 and Fig. 2.30 show the output characteristics including the output offset voltage and the output variations of this analog buffer circuit. It shows the output offset

voltage still large in this compensating circuit. The main source of the error in the output voltage is the small output resistance of the transistors. The output resistance in the saturation region of the poly-Si TFT is much smaller than that of the single-crystalline Si MOSFETs. Owing to the small output resistance of poly-Si TFTs, the current levels during the sampling and driving periods may be different which results in the invalidity of this compensating method.

2.4 Comparisons of Several Op-amp-type and Source-follower Type Analog Buffer Circuits

In this section, the comparisons between several op-amp-type analog buffers and source-follower type analog buffers including the output performance, circuit configuration, and power dissipation are discussed. These data are shown in Table 2.1.

- From the aspect of output performance

Table 2.1 shows the output offset deviation and output offset variation of three op-amp type analog buffers and three source-follower type analog buffers. The output offset deviation is defined as the difference between the average value and the extreme value of output offset voltage with input signal varying from 1V to 5V. The output offset variation is referred to the maximum value minus the minimum value of the offset voltage in a given input voltage. The simulation results show that op-amp-type analog buffers have better linearity of input-output characteristics while suffering from serious output variations due to device-to-device variations of LTPS TFTs. Effective compensation can be achieved by the differential-pair compensated method while compensation in bias circuit seems less

efficiency. This is because that the differential-pair mismatch is the primary source of output variations in op-amp-type analog buffers. On the contrary, source-follower type analog buffers show higher immunity to the device variation. The output variation can be reduced effectively with self-compensation method through the storage capacitor. However, large variations still exist in the compensating circuit with the concept of matching TFTs. Because the assumption that device characteristic of one transistor matches another completely on the same glass substrate is very difficult to achieve. Therefore, it is considered that self-compensation method by a storage capacitor is the best compensating method for source-follower-type analog buffers.

- From the aspect of circuit configuration

Form Table 2.1, it is clear that op-amp-type analog buffer needs many transistors which will occupy large area. On the contrary, because of the simple configuration, source-follower-type analog buffers need fewer transistors than op-amp-type analog buffers. The advantage of simple configuration makes source-follower type analog buffer more suitable for high resolution display application.

- From the aspect of power dissipation

It is obvious that the power dissipation of source-follower type analog buffers is much smaller than that of op-amp type analog buffers. Depending on the simulation results, the power dissipation of op-amp-type analog buffer is ten times or even larger than that of source-follower-type analog buffer when input voltage is 4V. Since several hundreds of analog buffers are needed in the LAAT (line-at a-time) driving architecture, vast power will be dissipated by analog buffers employing op-amp. Therefore, source-follower type analog

buffer is the better choice for SOP application in consideration of low power consumption.

✦ input voltage : 1~6 V		Offset Voltage Deviation (mV)	Offset Variation at Vin=4V (mV)	The Number of Transistors	The Number of Capacitors	Additional Number of Control Signals	Power Dissipation at Vin=4V (μW)
Op-Amp Type	Typical Two-Stage	199	1434	7	0	0	78.4
	Itou's Differential Pair Com.	427	35	7 (13 including switches)	1	2	69.2
	Yiu's Bias Circuit Com.	452	546	10	0	1	184.5
Source-Follower Type	Conventional	570	562	1	0	0	4.4
	Chung's Push-Pull	816	46	2 (8 including switches)	1	2	6.7
	Sony's Double Offset	40	9	1 (15 including switches)	2	6 & additional current source	12.4
	Jung's Matching TFT	1272	634	5	0	2	6.6

Table 2.1 Comparison of several op-amp-type and source-follower type analog buffers.

2.5 Summary and Conclusion

Several kinds of analog buffer circuits using LTPS TFTs are introduced with the circuit configuration and the compensation concepts. These analog buffer circuits are classified into operational amplifier type (op-amp-type) analog buffer and source-follower type analog buffers according to their circuit architecture and divided into six major compensating methods. These compensating architectures of analog buffer circuits are necessary owing to the electrical characteristic variation of the transistors resulting from the pulse-to-pulse variations of laser energy density and random distribution of grain boundaries. Each kind of circuit compensating method has its own advantages and disadvantages as discussed in section 2.4. In conclusion, the source-follower type analog buffer with simple configuration,

better immunity to the LTPS TFTs device variation, and lower power dissipation is considered to be the best candidate for system-on-panel applications.

Chapter 3

The Effect of Multi-channel Structure on Low-Temperature Polycrystalline Silicon Thin Film Transistors

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3.1 Introduction

Recently, fast growing market of system-on-panel (SOP) for flat-panel display has pressed the development of Low-temperature poly-Si TFT to higher performance, higher uniformity, and higher reliability. It is well known that the key to obtain high performance poly-Si TFT is the crystallization of a-Si thin films. Large grain size and less grain boundaries and trap states of the poly-Si film are the main requirement in the poly-Si crystallization process. Among the many researches of the crystalline methods, the excimer laser crystallization (ELC) is considered to be the most promising approach to get high performance of the transistors at present [3.1]-[3.2]. However, due to the narrow process window of the laser energy density for producing large grain of poly-Si thin film in SLG regime, the laser energy density must be precisely controlled. Unfortunately, laser energy density varies randomly in space, and differs from pulse to pulse, which will cause the non-uniform grain size distribution and thus the non-uniform trap states across the substrate. Thus, when the devices were fabricated on the substrate, large difference of trap states densities may exist between transistors. Trap states of the poly-Si thin film exert a profound

influence on device characteristics. It is well understood that the threshold voltage and subthreshold swing are strongly influenced by the density of dangling-bond midgap states which are thought to originate mainly from dangling bonds in grain boundaries, while the field-effect mobility and leakage current are related to the strain-bond tail states which may mainly come from the intragranular defects [3.3]-[3.5]. Hence, there are large device characteristics variations of LTPS TFTs between transistors. It is very undesirable for device applications.

To achieve the goal of system-on-panel, the improvements are required to solve this problem of device-to-device variations. This can be achieved from three aspects: materials and process technology, device structure, and circuit design. From the aspect of materials and process technology, the key point is the poly-Si crystallization technology. Highly uniform poly-Si thin film is required to achieve good uniformity of LTPS TFTs. The best resolution is to obtain the single grain crystallization. However, it is difficult to carry out at present. From the aspect of device architecture, novel or modified device architectures for better device quality and better tolerance of device variation is needed. But it must fit in with the requirement of low cost. Therefore, without extra process step is must taken into consideration as well. In additional to the improvements from process technology and device structure, the compensation from the circuit design offers another path to solve the output variation of LTPS-TFTs analog circuits resulting from the large device-to-device variation of poly-Si TFTs. It can be achieved by optimizing circuit design with the effective compensating configuration and appropriate driving scheme.

In this thesis, we purpose to compensate the device non-uniformity of LTPS-TFTs by means of modified device architecture and circuit design. For the part of device architecture we want to improve the non-uniformity of LTPS TFTs by simply modifying the device architecture while without the use of additional masks and no need to modify the normal process of TFT fabricating. The multi-channel structure with slicing layout method is used in

this work. Recently, several researches on multi-channel structure revel that high performance and high reliability poly-Si thin film transistors can be achieved with multi-cahnnel structure resulting from the reduction of grain boundary defects and the superior gate control ability [3.6]-[3.10]. However, the improvement of poly-Si TFTs uniformity by multi-channel structure is rare discussed. The multi-channel structure of LTPS-TFT was supposed to possess better uniformity compared with conventional structure. In this chapter, the uniformity of LTPS TFTs with multi-channel structure are investigated and discussed. The mechanism of improving uniformity of multi-channel structure will be detailed expounded.

3.2 Experimental Procedure

Fig.3.1 shows the top view of the layout images of conventional single channel TFTs and the TFTs with multi-channel structure. In the multi-channel TFTs, the channel was divided into five stripes and ten stripes respectively for study the effect of stripe numbers on the device uniformity. The conventional single channel TFTs and multi-channel TFTs were fabricated on the same oxidized silicon wafers by the identical process technology. A schematic graph of key processes is illustrated in Fig.3.2. First, 500Å-thick a-Si thin films were deposited on oxidized silicon wafers by low-pressure chemical vapor deposition (LPCVD) at 550°C using SiH_4 as gaseous source. Then, the a-Si thin films were crystallized by KrF excimer laser annealing in a vacuum ambient, in which the substrate temperature was controlled at room temperature. After defining the device active layer, 500/1000Å-thick tetraethyl orthosilicate (TEOS) gate oxides were deposited by low-pressure chemical vapor deposition (LPCVD). A 2000Å-thick a-Si thin film was then deposited by LPCVD for forming gate electrode. Then, the a-Si thin film was etched by transformer-coupled plasma reactive ion etching (TCP-RIE) to form gate electrodes. After removing the gate oxides,

self-aligned implantations of phosphorous with dose of 5×10^{15} cm^{-2} were carried out to form the source and drain regions of n-channel TFTs. Then a 3000Å-thick passivation TEOS oxides were deposited by low-pressure chemical vapor deposition (LPCVD), following by dopant activation for the source/drain and gate regions by annealing at 300°C in the horizontal furnace. The process was completed after conventional contact opening and 5000 Å-thick Al metallization. After that, a 20-min sintering process was executed at 400°C for reducing the contact series resistance of the source/drain electrodes.

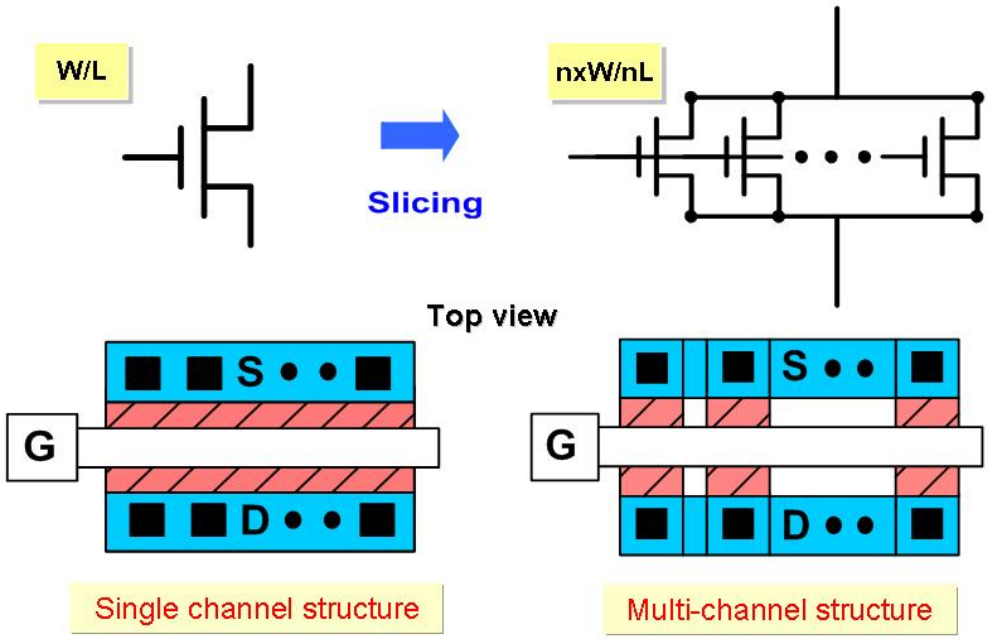


Fig.3.1 Layout image of conventional single channel TFTs and TFTs with multi-channel structure.

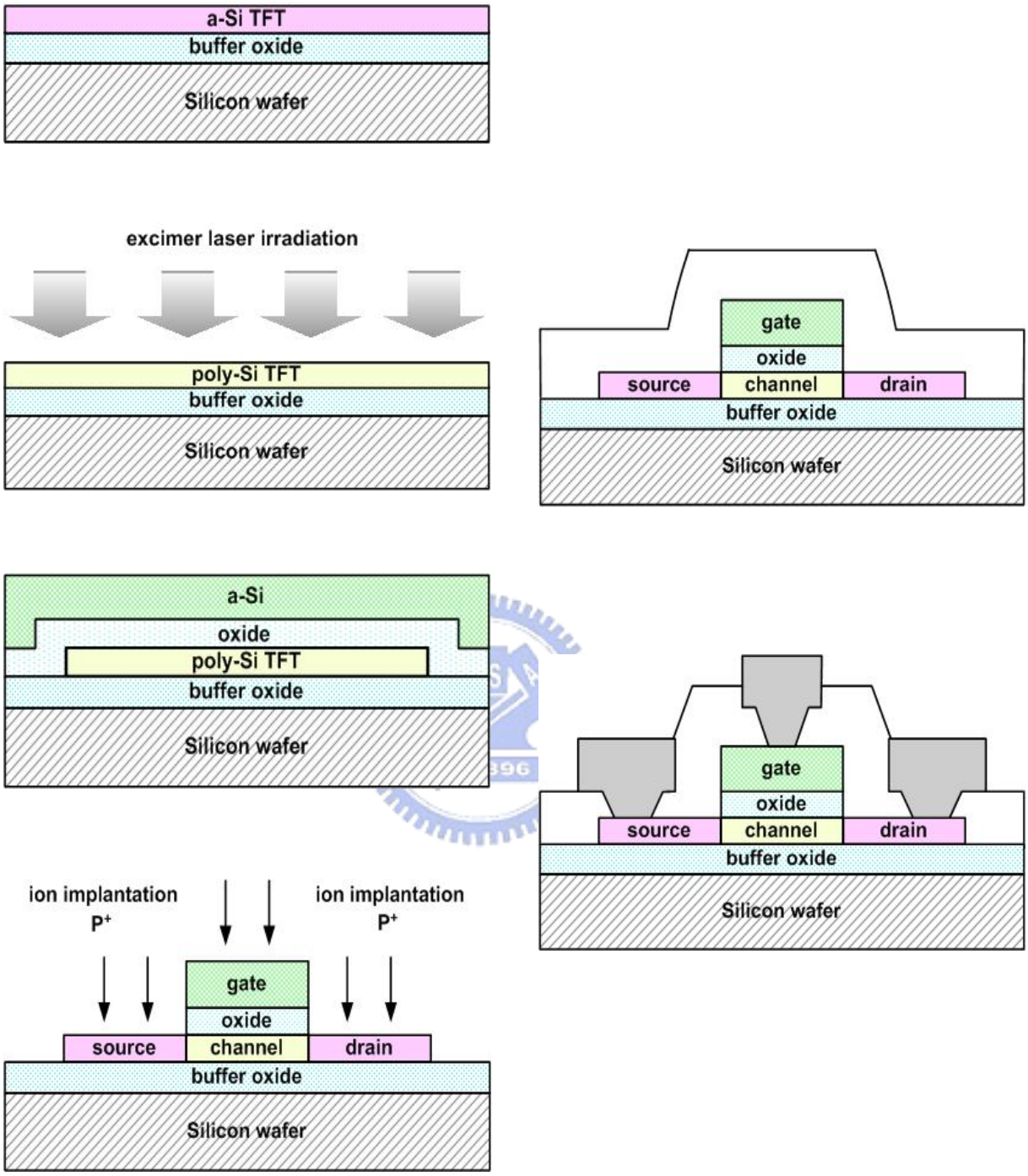


Fig.3.2 The process procedure of fabricating ELC LTPS TFTs.

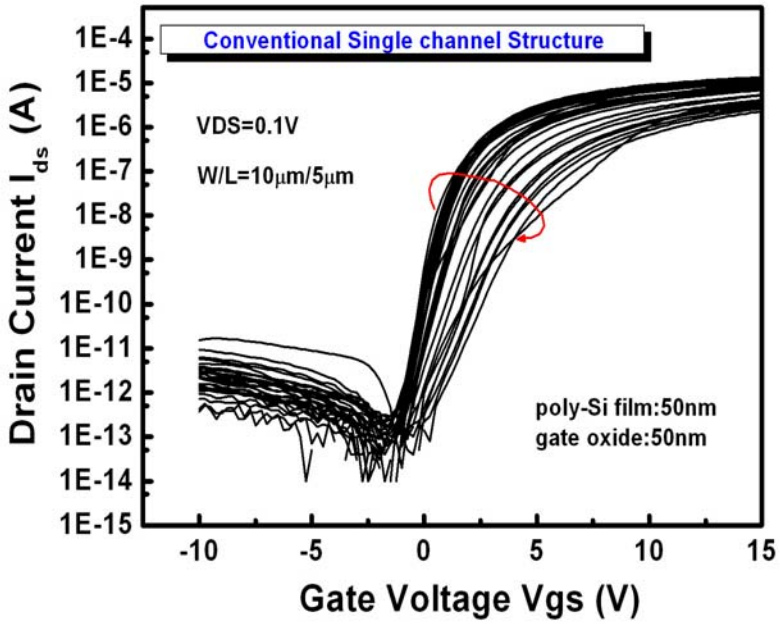
3.3 Results and Discussion

3.3.1 Electrical Characteristics of Conventional Single-channel and Multi-Channel LTPS TFTs

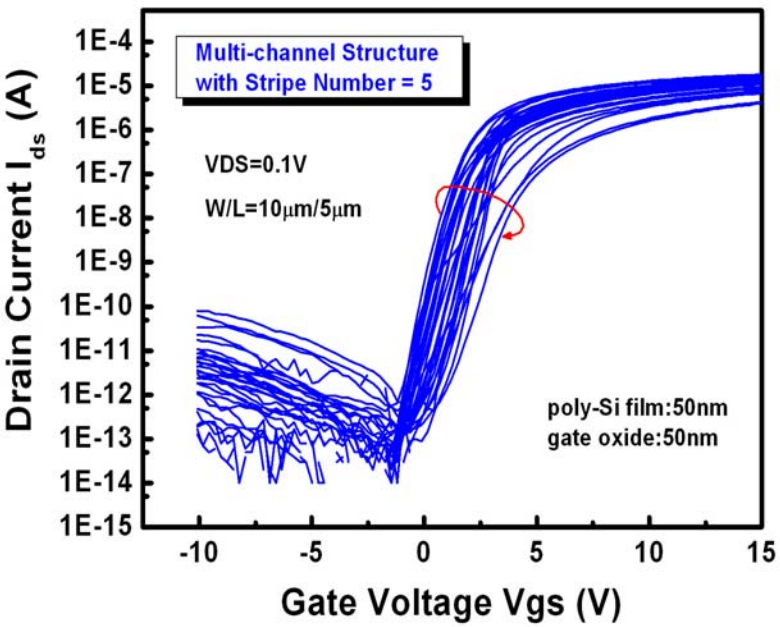
Fig.3.3(a)~3.3(c) show the typical transfer characteristics I-V curves of thirty n-channel LTPS TFTs (W/L=10μm/5μm) of single channel structure, multi-channel structure with five stripe numbers, and multi-channel structure with ten stripe numbers, respectively. It is clear that the performance of the thirty transistors in the subthreshold region becomes more uniform as channel stripe numbers increasing. It revels that the variation of electrical characteristics include threshold voltage and subthreshold swing are reduced by channel slicing. However, the leakage current of thirty transistors still has large distribution regardless of channel stripe numbers. Besides, it can be seen that the scale and variations of on current of single channel and multi-channel structure are almost the same from our measured results. In order to study the multi-channel effect on the on current performance more detailed, the output characteristics are also measured. The Id-Vd curves of these thirty transistors of single channel structure, multi-channel structure with five stripe numbers, and multi-channel structure with ten stripe numbers are shown in Fig.3.4(a)~3.4(c), respectively. It can be seen that the on current of multi-channel devices are slightly larger than single channel devices and the highest on current is existed in the devices with ten channel stripes, while the variations of on current between thirty transistors are still very large in the multi-channel devices. It tells that the non-uniformity of on current can not be improved in our multi-channel devices.

In additional to the Id-Vg and Id-Vd curve, the cumulative probability of twenty-five devices are shown in Fig.3.5 and Fig.3.6 to more clearly find out the device characteristics distribution of single-channel devices and multi-channel devices. Fig.3.5(a)~3.5(c) show the

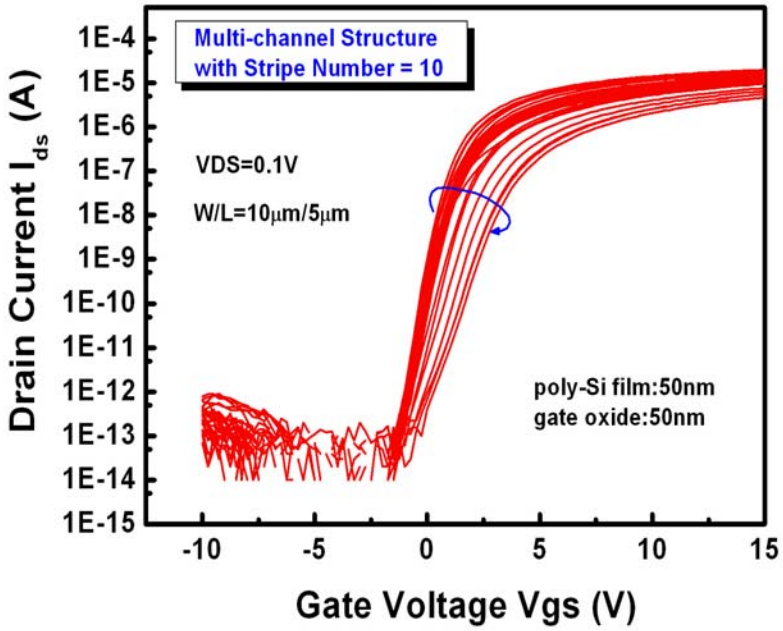
cumulative distributions of critical characteristic of single channel structure and multi-channel structure including threshold voltage (Vth), subthreshold swing (SS), and transconductace (gm), respectively. The W/L of these devices is 10μm/5μm. It is obvious that large variations exist in the conventional single-channel devices. However, the variations of the threshold voltage and subthreshold swing are much smaller in the multi-channel devices and decreasing with the channel stripe numbers increasing. Nevertheless, there are still large variations of the transconductance even the multi-channel structure is employed to the devices. Fig.3.6(a)~3.6(c) also show the cumulative distributions of the third critical characteristics in the devices with large W/L ratio (W/L=200μm/5μm). Similar to the results seen in the devices with smaller W/L ratio (W/L=10μm/5μm), it is observed that the device characteristic variation of Vth and SS are reduced as channel stripes increasing. However, the non-uniformity of transconductance remains poor in multi-channel devices. In addition, it is noticed that the device variations of the transistors with large channel width is commonly smaller then that ones with smaller channel width. The devices with 200μm channel width and ten channel stripes suffer from the smallest device-to-device variations in our experiment.


Conventional Single channel Structure
VDS=0.1V
W/L=10μm/5μm
poly-Si film:50nm
gate oxide:50nm
Drain Current I_{ds} (A)
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
1E-12
1E-13
1E-14
1E-15
-10
-5
0
5
10
15
Gate Voltage Vgs (V)

(a)

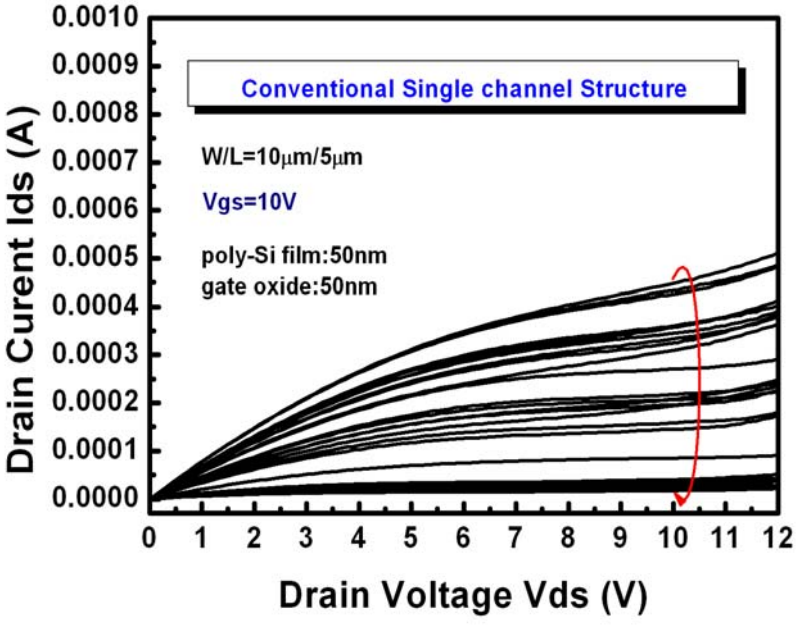

Multi-channel Structure
with Stripe Number = 5
VDS=0.1V
W/L=10μm/5μm
poly-Si film:50nm
gate oxide:50nm
Drain Current I_{ds} (A)
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
1E-12
1E-13
1E-14
1E-15
-10
-5
0
5
10
15
Gate Voltage Vgs (V)

(b)

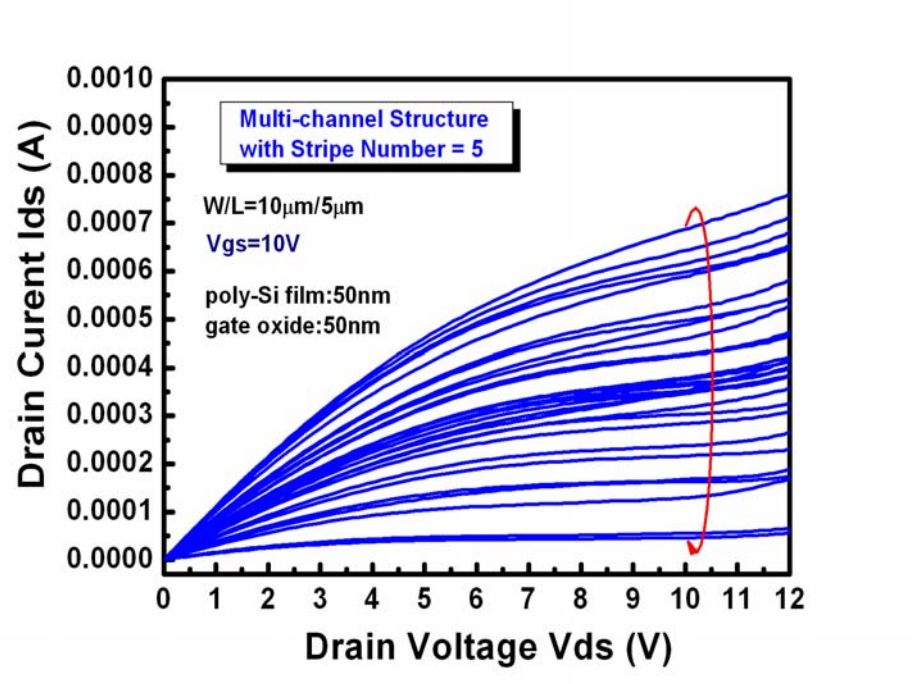


(c)

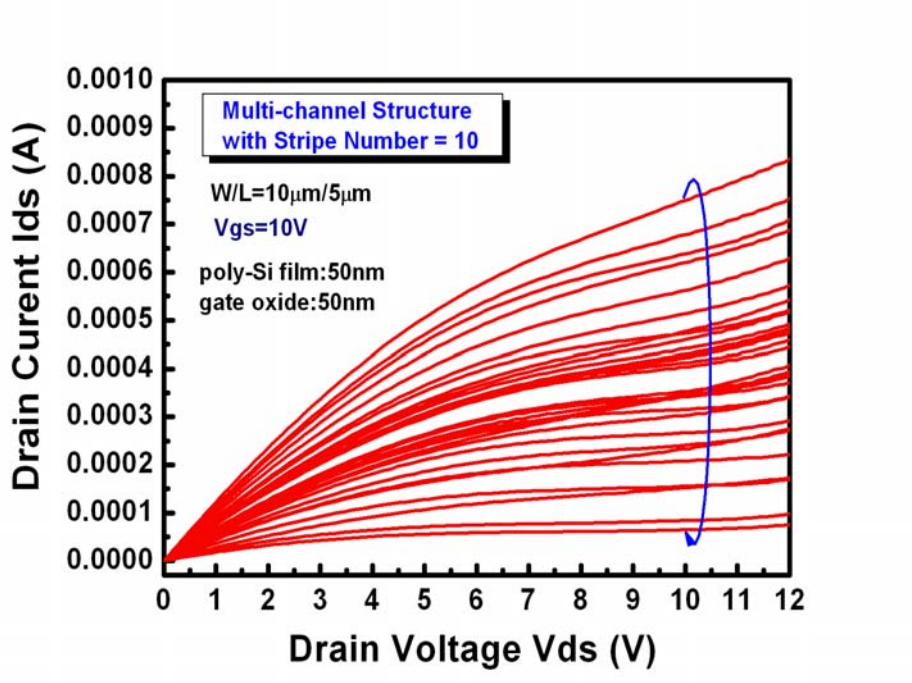
Fig.3.3. Transfer characteristics of thirty LTPS TFTs at V_{ds} = 0.1 V of (a) single channel devices, (b) multi-channel device with stripe number =5, and (c) multi-channel device with stripe number =10.



(a)

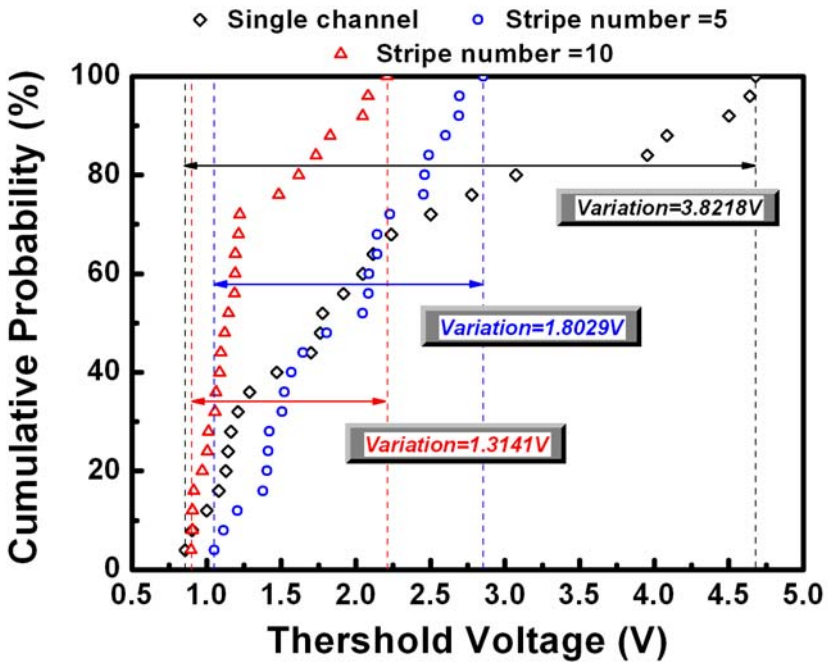


(b)

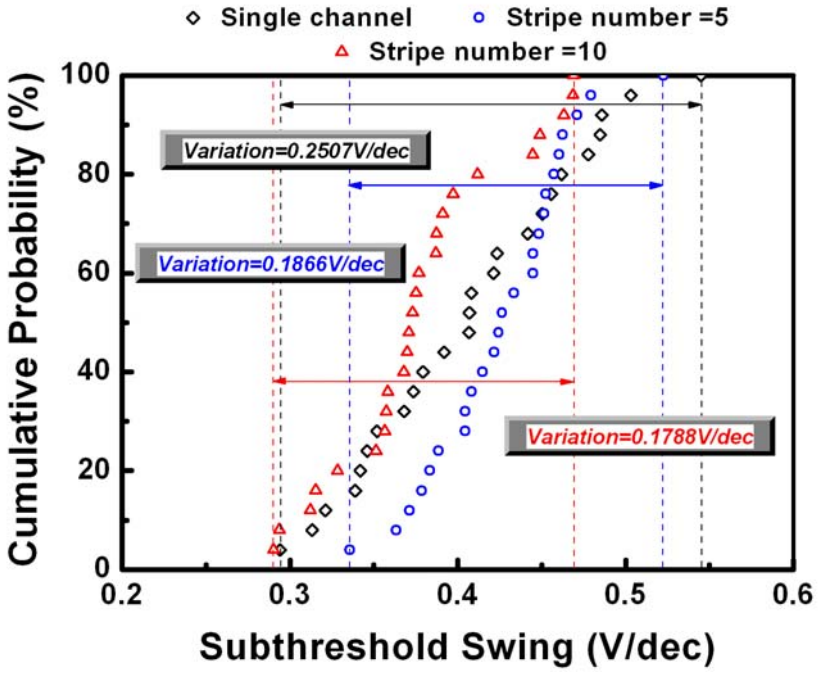


(c)

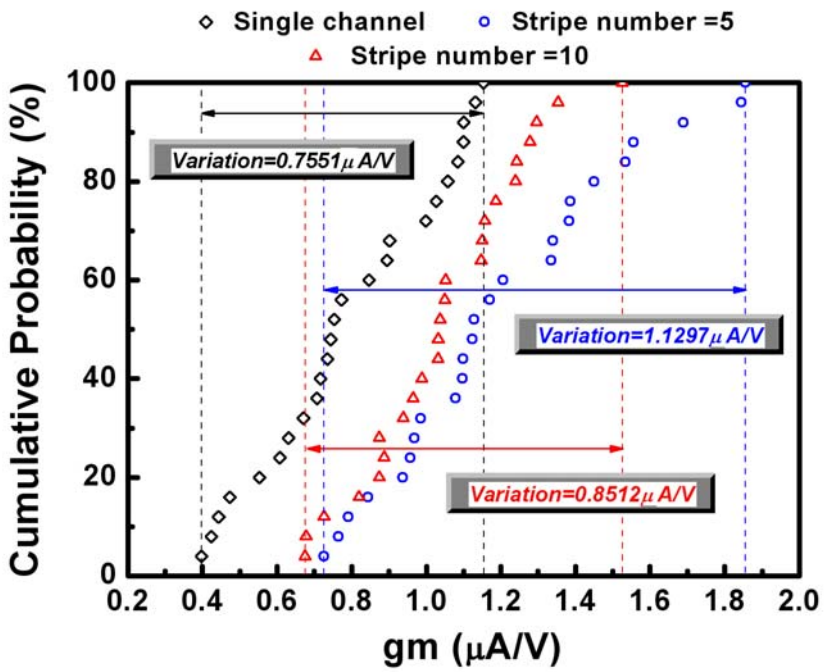
Fig.3.4. Output characteristics of thirty LTPS TFTs at Vg=10V of (a) single channel devices. (b) multi-channel device with stripe number =5, and (c) multi-channel device with stripe number =10.


Single channel
Stripe number =5
Stripe number =10
Cumulative Probability (%)
Thershold Voltage (V)
Variation=3.8218V
Variation=1.8029V
Variation=1.3141V

(a)

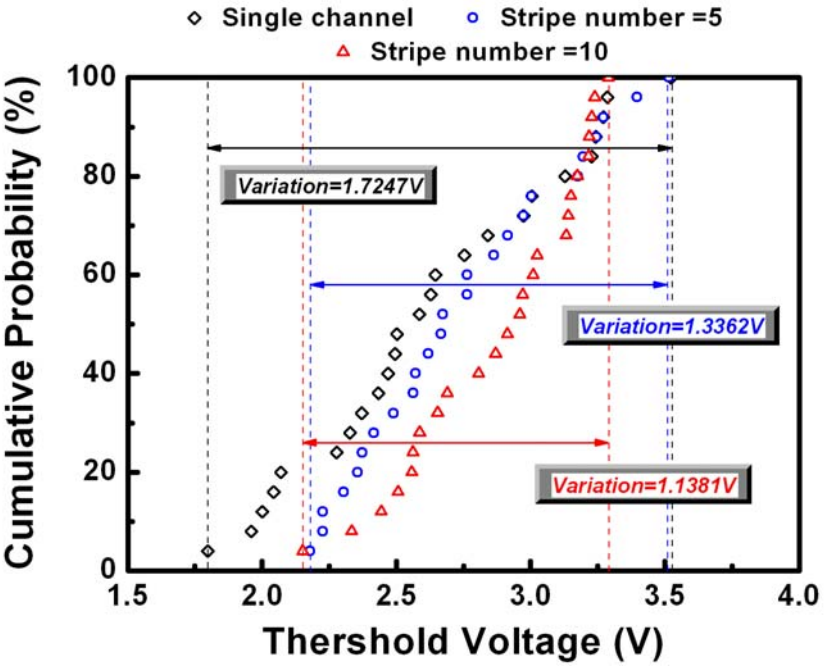

Single channel
Stripe number =5
Stripe number =10
Cumulative Probability (%)
Subthreshold Swing (V/dec)
Variation=0.2507V/dec
Variation=0.1866V/dec
Variation=0.1788V/dec

(b)

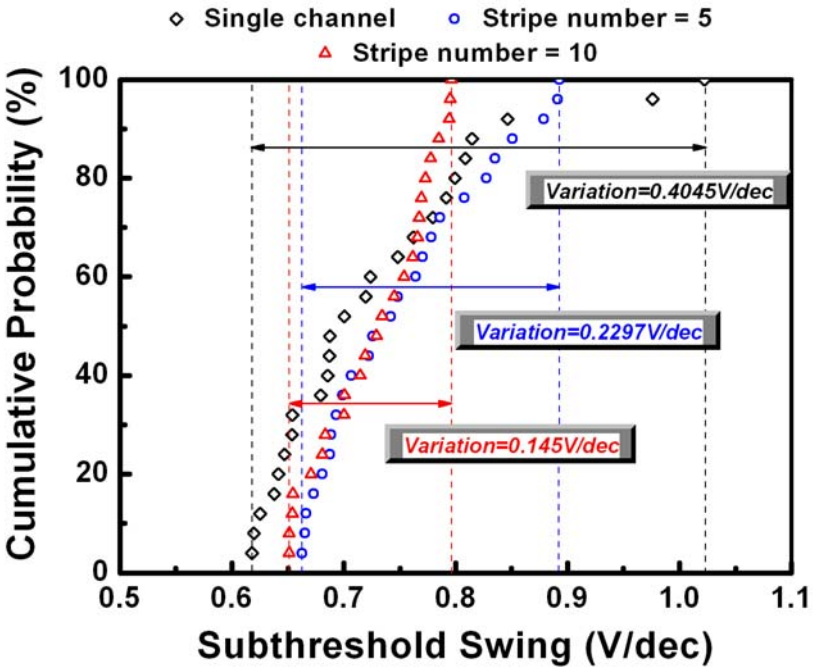


(c)

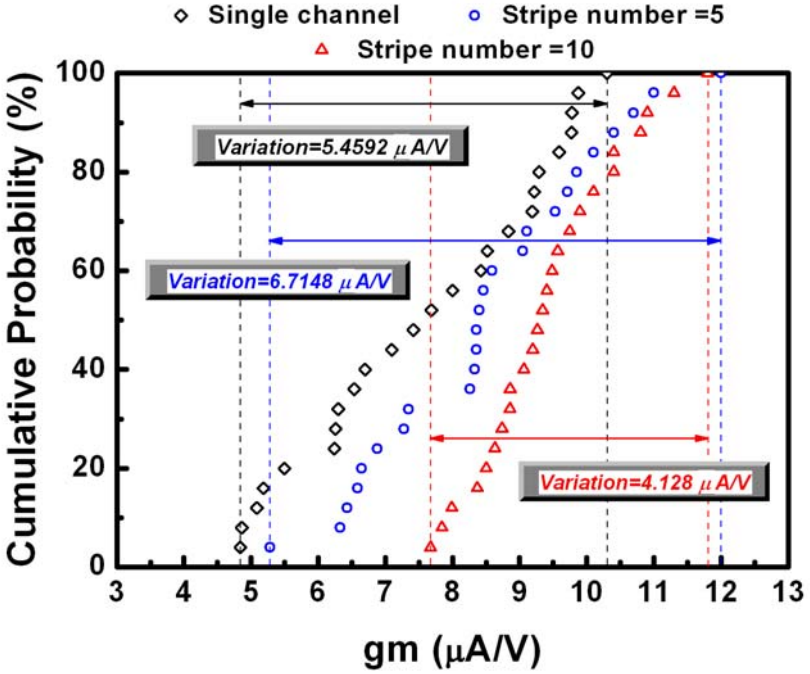
Fig.3.5. Cumulative distributions of (a) threshold voltage, (b) subthreshold swing, and (c) transconductace the device parameters from 25 n-channel LTPS TFTS (W/L=10μm/5μm) of single channel structure and multi-channel structure.



(a)



(b)



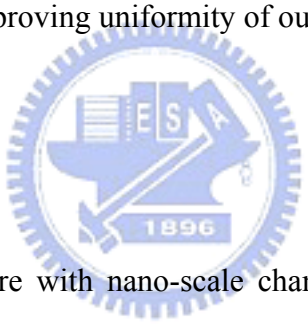
(c)

Fig.3.6. Cumulative distributions of (a) threshold voltage, (b) subthreshold swing, and (c) transconductace the device parameters from 25 n-channel LTPS TFTS (W/L=200μm/5μm) of single channel structure and multi-channel structure.

3.3.2 Mechanisms of the Effect of Multi-channel Structure

From the experimental results discussed in the previous section, it seems that multi-channel structure can only improve the uniformity of Vth and SS, but on effect on improving the uniformity of transconductance. In this section, we will propose the mechanisms of the multi-channel effect on device uniformity of LTPS TFTs according to our measurement results.

At first, we suppose that there are three possible mechanisms of improving uniformity of LTPS TFTs by multi-channel structure. They are side-wall effect, passivation effect, and probability effect. These three effects are discussed and analyzed in the following to make out the most important factor in improving uniformity of our multi-channel devices.



- **Side-wall effect**

The multi-channel structure with nano-scale channels has been verified to effectively enhance the electrical performance and reliability of poly-Si TFTs [3.8]-[3.9]. It is referred to induce side-wall channels on both sides of each channel due to the tri-gate structure. It results in the increasing of effective channel width and excellent gate control. As a result, LTPS TFTs with the multiple nano-scale channels structure can obtain higher electrical performance. Therefore, the standard deviation of the device characteristics is reduced due to the increasing of the average value. However, the smallest channel width of each stripe in the multi-channel devices we fabricated is 1μm, which is impossible to form the tri-gate structure. Moreover, the50nm-thick poly-Si thin film and 50/100nm-thick gate oxide were used in our devices. The side-wall gate control capability is very weak in these devices because of the thick gate oxide. Consequently, the effect of side-wall channel can be almost neglected in our multi-channel devices. The side-wall effect is considered not to be the factor

in improving uniformity of our multi-channel devices.

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- **Passivation effect**

The passivation of defects in the channel region has been proved to be the effective method for reducing grain boundary traps [3.11]-[3.16]. Trap states in the poly-Si active region have pronounced influence on device characteristics. The threshold voltage and subthreshold swing are strongly influenced by the density of dangling-bond deep states which are thought to mainly originate from dangling bonds in grain boundaries, while the field-effect mobility and leakage current are related to the strain-bond tail states which may mainly come from the intra-grain defects. The multi-channel structure has been reported to get high performance devices due to increase the efficiency of passivation resulting from the expanded passivation path [3.17]-[3.20]. Moreover, it has been verified that the passivation treatment can improves the uniformity of TFT characteristics significantly due to the reduction of localized defect density in the poly-Si film [3.21]. Therefore, it can be sure that the transistors with multi-channel structure which enhance the passivation efficiency can greatly reduce the device variation. Nevertheless, there is no passivation treatment in our devices fabricating process. As a result, the passivation effect is not the cause of improving uniformity in our multi-channel devices.

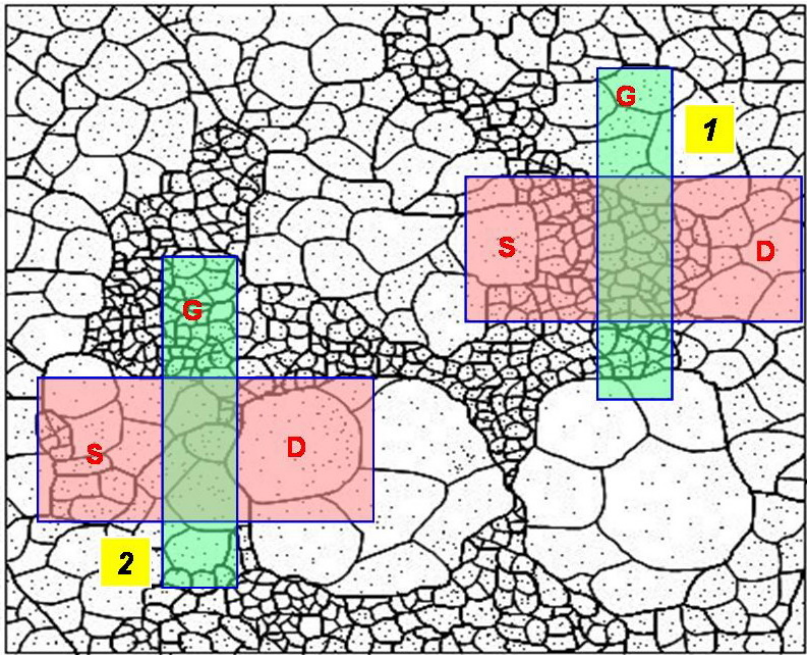
- **Probability effect**

For the LTPS TFTs using excimer laser crystallization, due to the non-uniform beam profile and pulse-to-pulse variation of laser energy density, a very non-uniform grain size distribution is always obtained across the whole substrate. The random grain distributions will result to huge variations of electrical characteristic between transistors. As shown in

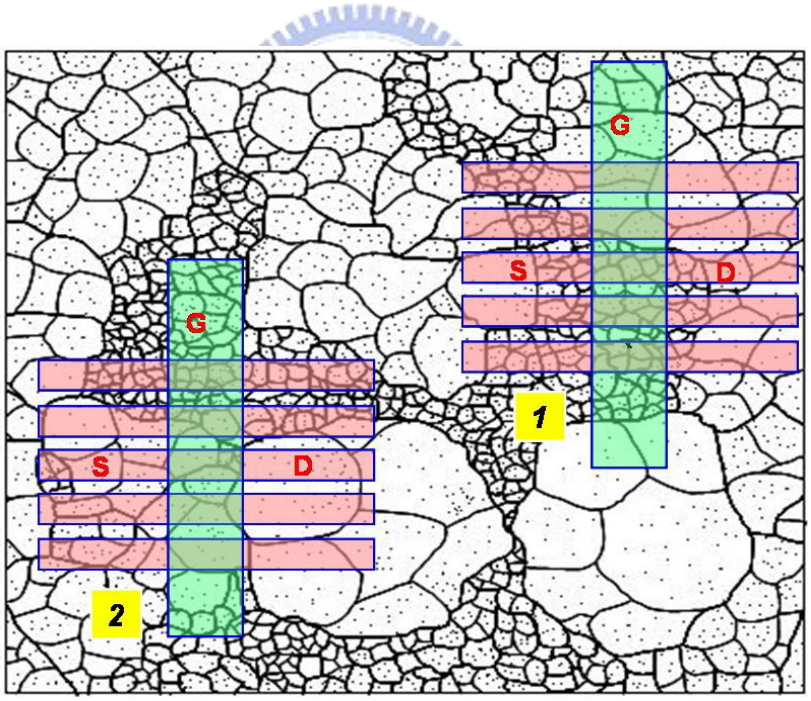
Fig.3.7(a), when the transistors were fabricated on the substrates, it may located in the small grain region like device 1 or in the large grain region such as device 2. Large trap states densities difference will exist between these two devices and cause the device variations. When the transistors with multi-channel structure is performed, as shown in Fig.3.7(b), for device 1, several of the divided channels may shift to the large grain region but some still in the small grain region. In comparison with single channel device shown in Fig.3.7(a), the grain boundaries are reduced in the multi-channel device and hence the performance is improved. In the case of device 2, when the channel is divided, some divided channels may encounter the small grain but some still located in the large grain region. Therefore, the numbers of grain boundaries are about the same between device 1 and device 2 on the substrate by employing the multi-channel structure. Owing to the dangling bonds in grain boundaries are the main source of deep states which strongly affect the threshold voltage and subthreshold swing of poly-Si TFTs, the variations of the Vth and SS in the multi-channel devices are much reduced resulting from the more uniform grain boundaries densities between transistors. It is consonant with our measurement results discussed previously. However, according to the mechanism of probability, only the grain boundaries non-uniformity can be improved by multi-channel structure, the intra-grain defects of unit area is nearly the same with single-channel devices even after channel divided. Large variations of tail states still remain between the transistors with multi-channel structure. Therefore, the field-effect mobility and leakage current which governed by the strain-bond tail states in active region nonetheless suffer from large variations in the multi-channel devices which also coincide with the measurement result shown in section 3.3.1. It can be concluded that the multi-channel structure is evident of reducing the deep states densities effectively, while is inefficient for reducing the tail states variations.

In order to investigate the correlation between the grain size and the stripe numbers in out multi-channel devices, scanning electron microscopy (SEM) analysis was executed. The

samples were processed by Secco-etch before analysis. Fig.3.8 shows the SEM image of 500-Å poly-Si thin film crystallized by ELA with the laser energy density of 340 mJ/cm^2. The average grain size is about 0.3 μm; the maximum and minimum grain size is about 0.9 μm and 0.1 μm, respectively. It is clear that severe variations of grain size exist in the laser crystallized poly-Si thin films which contribute to the electrical characteristic variations of LTPS TFTs. Based on the measured results and the mechanism of probability effect, it reveals that good uniformity will be achieved in the multi-channel devices with nano-scale channels. Therefore, the devices with more channel stripes get the better uniformity. However, the more channel stripes, the larger the layout area. Restricting to the design rule and the consideration of layout spaces, the numbers of channel stripes must be limited to an optimum value in the multi-channel devices. In addition, the influence of side-etching gets noticeable when the width of each channel stripe is in the nano-scale. The process variation resulting from side-etching will also contribute to variations of electrical characteristics in the multi-channel devices with tiny channel stripes. In conclusion, the optimum design is obtained when the channel width of each stripe close to but slightly larger than the grain size.



(a)



(b)

Fig.3.7. Probable distributions of the relative location between grain structures and the devices. (a) single channel devices, and (b) multi-channel devices.

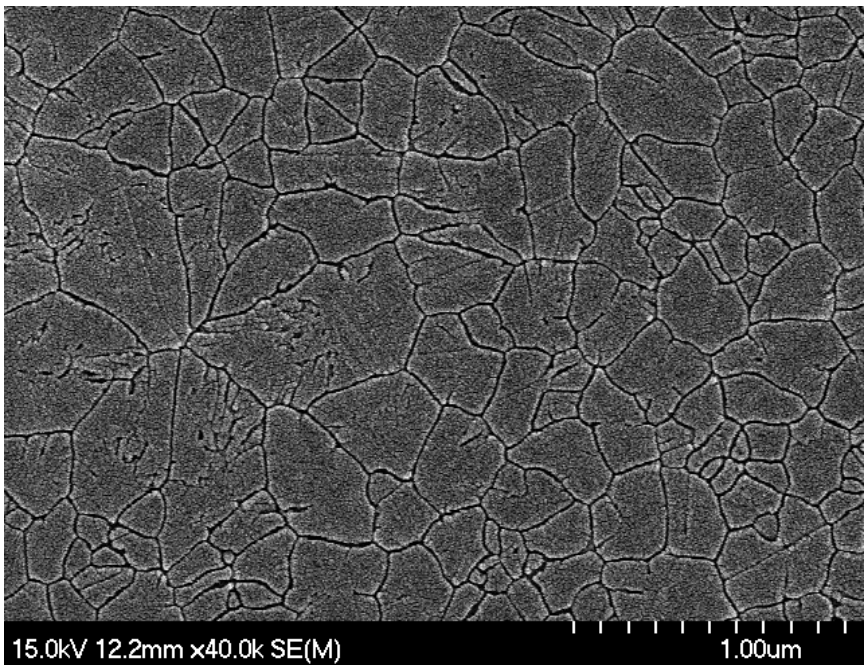


Fig.3.8. SEM image of poly-Si thin films crystallized by ELA.

3.4 Conventional Source-follower Analog Buffer with Multi-channel Structure

In this section, the multi-channel structure is applied to the driving TFT of the conventional source follower buffer circuit to study its effect on the buffer output performance. The circuit configuration of conventional source follower and conventional source follower with multi-channel structure are shown in Fig.3.9. The W/L ratio of the driving TFT is 100μm/8μm of both the conventional source follower and source follower with multi-channel structure. The channel of the driving TFT in the source follower buffer circuits which have multi-channel structure is divided into ten stripes in this design. The buffer circuits were fabricated by the same process flow as described in section 3.2. The measurement system is consist of the Agilent 4156C including probe station and parameter analyzer and Agilent MSO6034A mixed signal oscilloscope to display the output signal through the coaxial cable

and BNC connection.

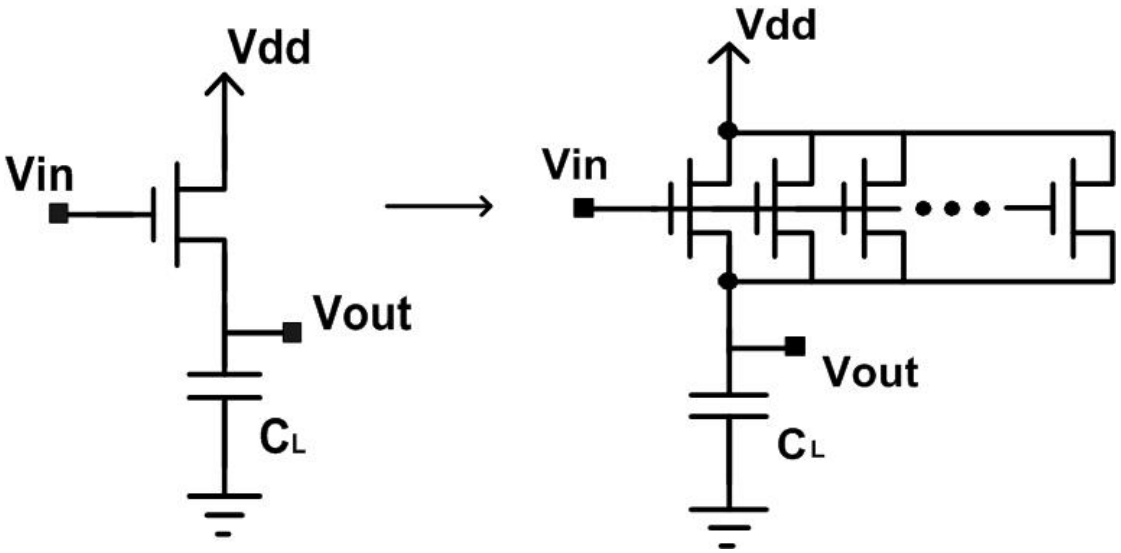


Fig.3.9. Conventional source follower and conventional source follower with multi-channel structure in the driving TFT.

The measurement results of output offset voltage variations in ten sets of conventional source follower buffer circuits are shown in Fig.3.10. It shows that large output offset voltage variation may exceed 1000 mV exist in the conventional source follower. In comparison, the output offset voltage variations of the source follower with multi-channel structure are below 900 mV as shown in Fig.3.11 when input data is in the range of 1V~6V. In order to clearly see the influence of multi-channel structure on the output variation of buffer circuits, the measured results of conventional source follower and conventional source follower with multi-channel structure are compared as shown in Fig.3.12. It is obvious that the output offset variation of the source follower with multi-channel structure is smaller. The output offset voltage is reduced to about half of that in the conventional source follower by the multi-channel structure of the driving TFT. It confirms that the multi-channel structures indeed can improve the uniformity of LTPS TFTs.

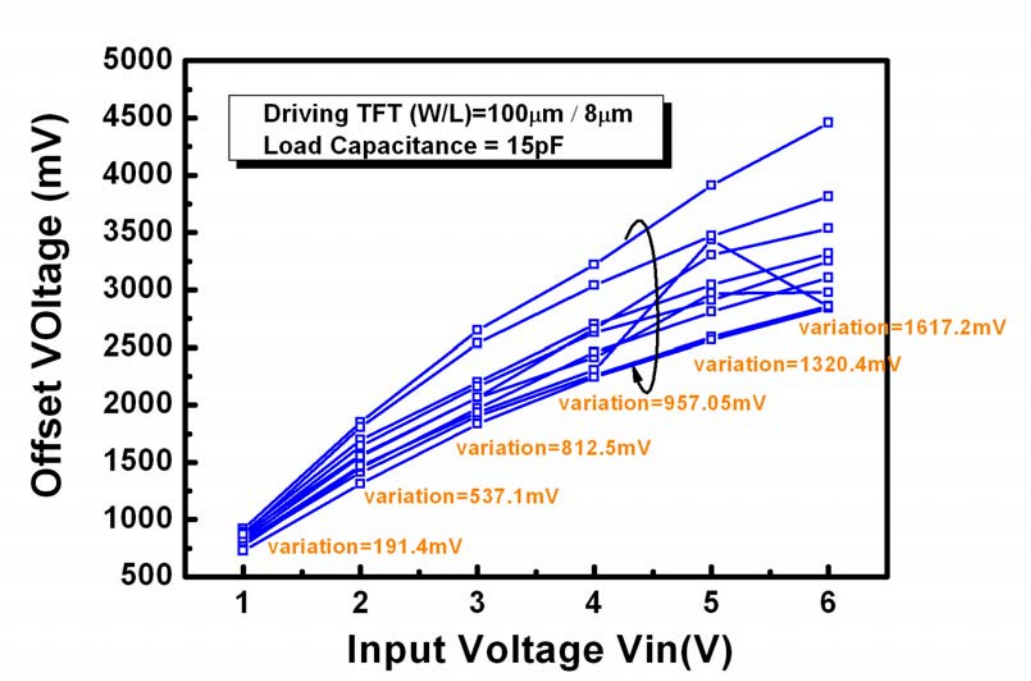


Fig.3.10. Measured results of the output offset voltage variations in ten sets of conventional source follower buffer circuits.

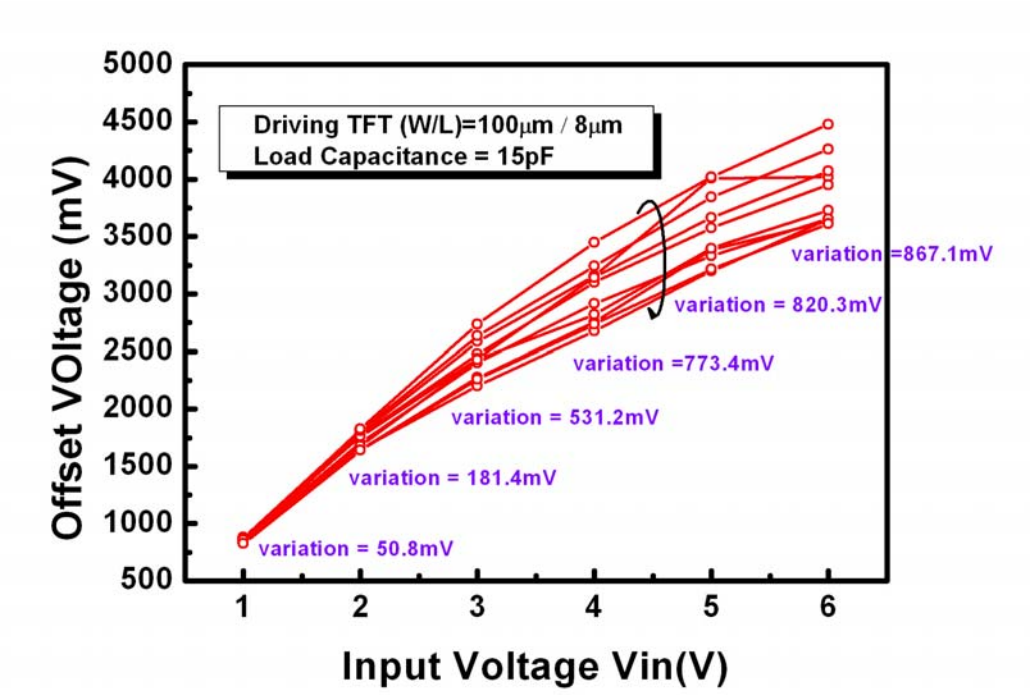


Fig.3.11. Measured results of the output offset voltage variations in ten sets of conventional source follower buffers with multi-channel structure of the driving TFTs.

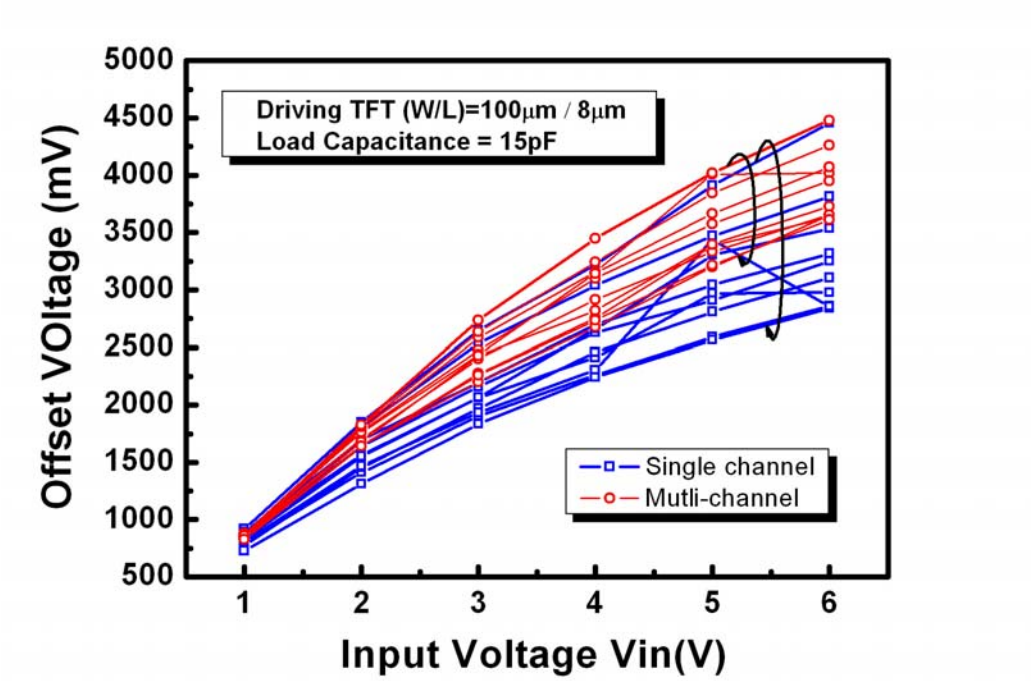


Fig.3.12. Comparison of the measured output offset voltage variations between the conventional source follower and conventional source follower with multi-channel structure.

3.5 Summary

The effects of multi-channel structure on the device uniformity of LTPS TFTs and the output performance of source follower analog buffer are investigated in this chapter. It is clear that variations of the threshold voltage and subthreshold swing are reduced as channel stripes increasing, while no such tendency can be seen in the transconductance and leakage current. The mechanism of the improving uniformity of multi-channel structure is studied in this chapter. It is proposed that probability effect is the most possible cause of improving uniformity of multi-channel structure. In conclusion, better uniformity of threshold voltage and the subthreshold swing of poly-Si TFTs can be obtained with channel slicing due to the more uniform grain boundaries densities between transistors according to the probability distribution. While the variations of the mobility and leakage current can not be reduced due

to the remained tail states variations of multi-channel devices. At last, the multi-channel structure is also employed to the conventional source follower to study the multi-channel effect on the output performance of buffer circuits. It is obvious that the output offset voltage variations of source follower with multi-channel structure in the driving TFT are reduced to about half of that in conventional source follower. It proves that the variations of poly-Si TFTs surely can be reduced by the multi-channel structure.

Chapter 4

Proposed Source-Follower Type Analog Buffer Circuits

4.1 Introduction

Low-temperature poly-Si thin-film transistors (LTPS TFTs) have attracted a considerable attention for integrating driver circuits of TFT-based flat panel displays such as AMLCD and AMOLED [4.1]-[4.4]. In a poly-Si TFT-LCD, poly-Si TFT is used to implement the driving circuits with the pixel array on a single glass substrate. Such integration reduces the number of external components and the connections to display which allows us to reduce system cost and make compact, high reliable displays.

For the integrated data driver employing LTPS TFTs, output buffers are indispensable to drive the large load capacitance of data lines. When the digital to analog converter is insufficient for driving the large loading of data line, the output buffer is applied to enhance its driving capability. The main requirements of an output buffer for the data driver of flat pane display including high output voltage accuracy, high driving capability, small layout area, and low power consumption.

Analog buffer can be simply employed by a typical two-stage operational amplifier (op-amp) or a simple source follower. However, large output variations will exist in these simplest circuits due to the electrical characteristic variations of LTPS-TFTs such as threshold

voltage variation, carrier mobility variation, and subthreshold swing variations. That is mainly caused by the random grain boundaries distributed in the channel region of LTPS TFTs between devices across the glass substrate resulting from pulse-to-pulse variation of excimer laser energy density and non-uniform laser beam profile. Moreover, LTPS-TFTs have much poor subthreshold characteristic compared with single crystal Si transistor. Such poor electrical characteristics and non-uniformity of LTPS-TFTs will results to large output offset of the analog buffer employing LTPS-TFTs and lead to the wrong gray scale. Since thousands of output buffers are necessary for a poly-Si TFT-LCD, it is necessary to design an analog buffer with high immunity to the non-uniformity of LTPS-TFTs to eliminate the output deviation as possible. Several researches on LTPS TFTs analog buffer have been tried to carry out a buffer with high immunity to the device variations [4.5]-[4.18]. These compensating circuits can be classified into operational amplifier type (op-amp type) analog buffer [4.5]-[4.8] and source-follower type analog buffers [4.9]-[4.18] according to their circuit architecture. Operational amplifier is usually used as the output buffer in single crystal silicon integrated circuits. However, the complicated circuit configuration, high power dissipation and the huge output voltage variation of op-amp type analog buffer using LTPS TFT make it not suitable for system-on-panel application. Source-follower type analog buffer with simple configuration, low power consumption and higher immunity to the device variation of LTPS TFT is considered an excellent candidate for system-on-panel application.

In this chapter, a new simple source-follower type analog buffer using low-temperature polycrystalline silicon thin-film transistors (LTPS-TFTs) for the integrated data driver circuits of AMLCD and AMOLED is proposed. In additional to the electrical properties variations of driving TFT, LTPS TFTs have much larger subthreshold current compared with single crystal Si transistors, and this poor electrical characteristic will results to large output offset and cause the output voltage not to be constant with time. This output voltage unsaturated phenomenon will also make more difficulty in buffer circuit design. In order to overcome

these problems, a new compensated analog buffer composed of two n-type thin film transistors, one storage capacitor and four switches is proposed. An active load is added to the buffer circuit to suppress the unsaturated phenomenon of output voltage. The output characteristic of conventional source-follower analog buffer circuit is discussed at the first in this chapter. Next, the circuit configuration and detail operation principle of the proposed buffer circuit are shown and discussed. In order to study the performance of the proposed analog buffer, simulation and measurement results are shown and compared with the conventional one. Both the simulated and measured results exhibit that the proposed buffer circuit is capable of minimizing the variation from both the signal timing and the device characteristics.

4.2 Output Voltage Unsaturated and Distribution Phenomenon of Source-Follower Type Analog Buffer

In order to investigate the output performance of the source-follower type analog buffer, HSPICE circuit simulator was introduced. In this work, the typical model of the poly-Si TFTs for simulation is expressed by the PRI parameters. The device parameters such as threshold voltage and mobility are 1.45V and 65.69cm^2/V-sec for n-type TFTs, and -0.99V and 61.51cm^2/V-sec for p-type TFTs. The load capacitance of data line is assumed 20pF which corresponds to a 2-inch QVGA LCD.

4.2.1 Output Voltage Unsaturated Phenomenon of Conventional Source-Follower Type Analog Buffer

A conventional source follower and its output waveform are shown in Fig. 4.1 and Fig. 4.2, respectively. In theory, the output voltage of a source follower will reach to input voltage minus the threshold voltage of the transistor (Vout=Vin-Vth) according to the turn-on characteristic of transistors. However, from the output waveform shown in Fig 4.2, it is clear that the final output voltage of the source follower is not kept constant, but exceeds the target voltage of Vin-Vth with time. This is mainly caused by the large subthreshold current of poly-Si TFTs. As model used in this work, the sub-threshold swing of LTPS TFTs is about 0.3V/dec that is much larger than MOSFETs' (0.06V/dec). When the output voltage approach the target voltage, the source follower will operate in the subthreshold region and large subthreshold current will keep charging the load capacitance. Consequently, the output voltage will be sensitive to the charging time. This problem makes the difficulty in buffer circuits designing for various product specifications with a source follower structure.

In order to eliminate this output unsaturated phenomenon, an active load is added to the source follower. The source follower with an active load and its output waveform simulating result are shown in Fig. 4.3. It is obvious that the unsaturated phenomenon of the output voltage is suppressed and the final output voltage nearly kept constant. In this circuit, the active load plays the role of a constant current source which provides a leaking path for subthreshold current of the driving TFT. Therefore, the output voltage will not be charged up by the subthreshold current and then keeps constant with charging time. The offset voltage (i.e. offset voltage=Vin-Vout) versus input voltage (Vin) of conventional source follower and source follower with active load with different charging time are shown in Fig. 4.4. It is clear that the offset voltage of the conventional source follower varies with different charging time. On the contrary, the offset voltage of the source follower with an active load is almost the same in different charging time. It means that adding the active load can solve the unsaturated phenomenon of the output voltage successfully. Although the output offset voltage of source follower with active load is larger than that of conventional source follower, it can be

eliminated by gamma correction [4.19]. According to the results, the structure of source follower with active load has high charging time variation-tolerant and is suitable for LTPS-TFTs buffer circuit design with source-follower-type configuration.

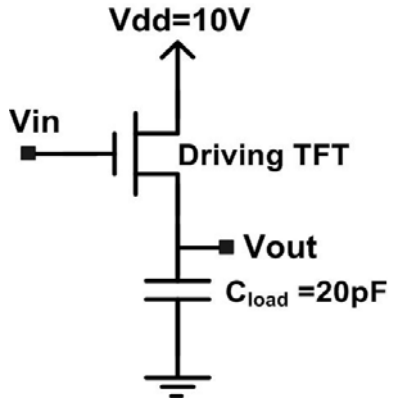


Fig. 4.1. Conventional source-follower type analog buffer.

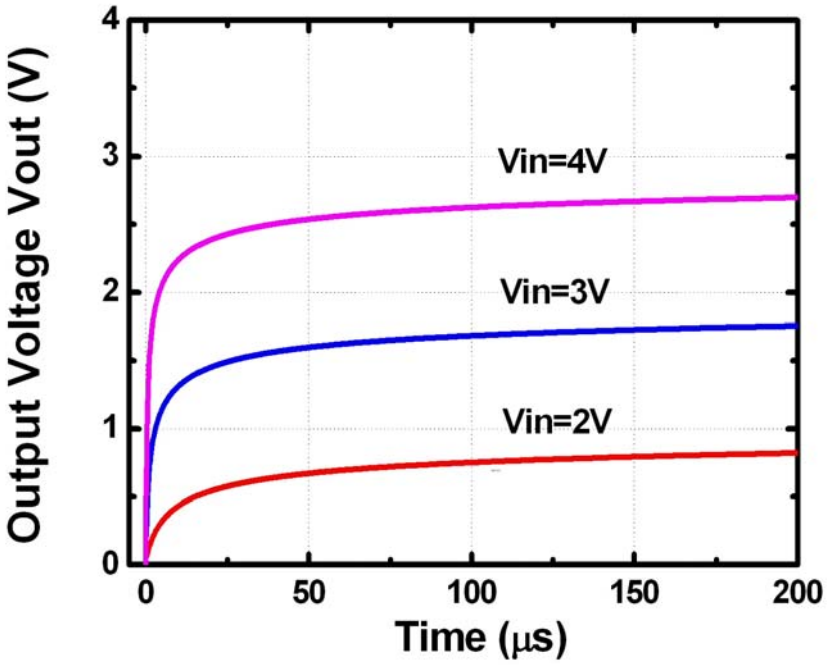


Fig. 4.2. Simulating output waveform of conventional source-follower type analog buffer.

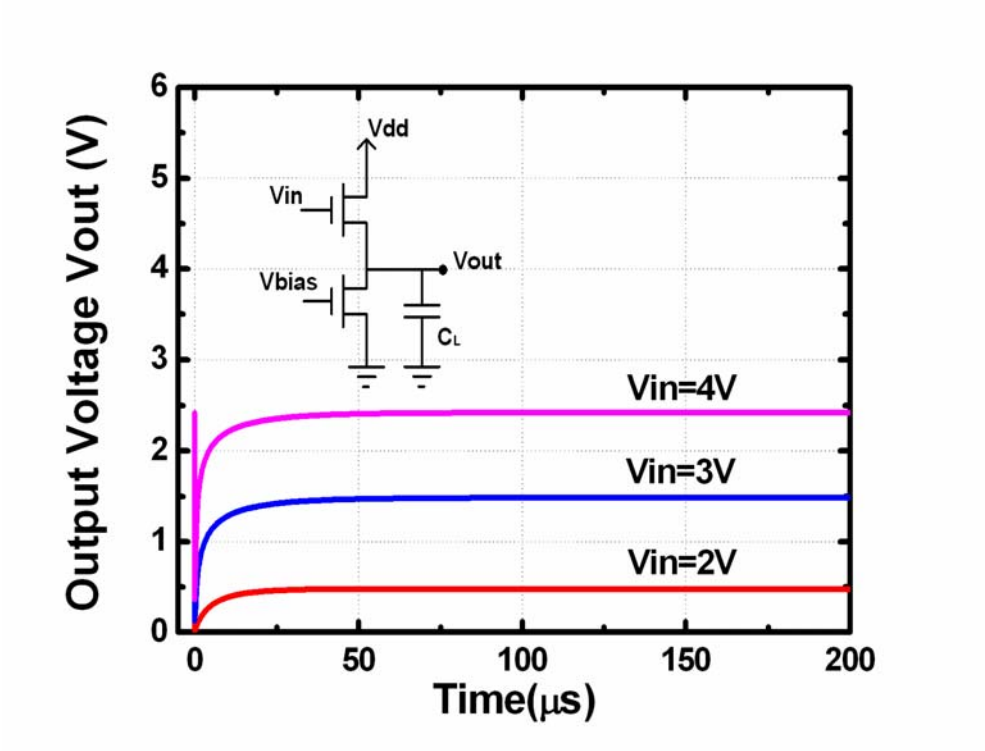


Fig. 4.3. Schematic of conventional source follower with an active load and its output waveform simulating results.

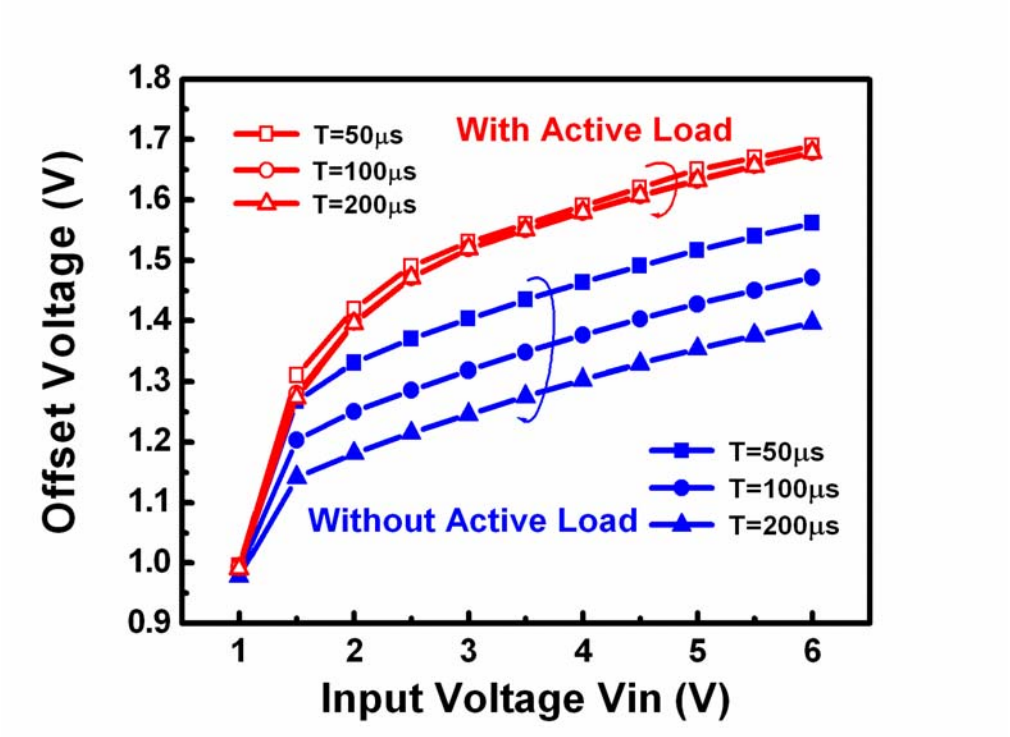


Fig. 4.4. Offset voltage comparison of conventional source follower and source follower with an active load in various charging time.

4.2.2 Output Voltage Distributed Phenomenon of Source-Follower Type Analog Buffer

In additional to the output unsaturated phenomenon of conventional source follower, the large output voltage variation resulting from the electrical characteristic variations of LTPS-TFTs such as threshold voltage variation, carrier mobility variation, and subthreshold swing variations is another serious problem needed to be solved in LTPS-TFTs analog buffer circuits. Fig. 4.5 shows the cumulative distributions of the device parameters from 30 n-channel LTPS TFTs fabricated on the same glass substrate. It is obvious that there is a large variation in the electrical characteristics of LTPS TFTs between transistors over the substrate glass. Such huge device-to-device variation will cause the output voltage distributed phenomenon of the source follower and lead to the wrong gray scale.

To study the effect of the device variation on the circuit performance, Monte Carlo simulation with an assumption of normal distribution as shown in Fig. 4.6 is executed, where the mean value and the deviation of the threshold voltage and mobility are 1.45V, 0.5V and 65.69cm^2/V-sec, 15cm2/v.s, respectively. Fig. 4.7 shows the twenty times Monte Carlo simulation results of the conventional source follower with active load when input voltage are 2V, 3V, and 4V. It can be seen obviously that huge output voltage variations resulting from the LTPS TFTs device variation still exist in this circuit. Therefore, an effective compensating configuration is required to develop an analog buffer with high immunity to the device variation in TFTs.

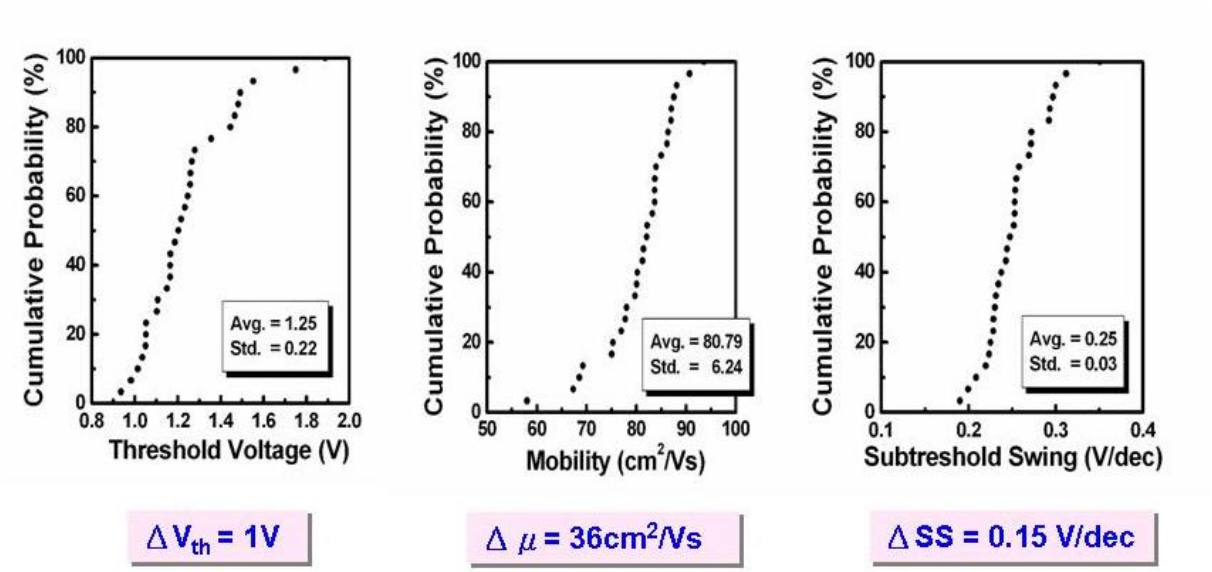


Fig. 4.5. Cumulative distributions of the device parameters from 30 n-channel LTPS TFTS fabricated on the same glass substrate.

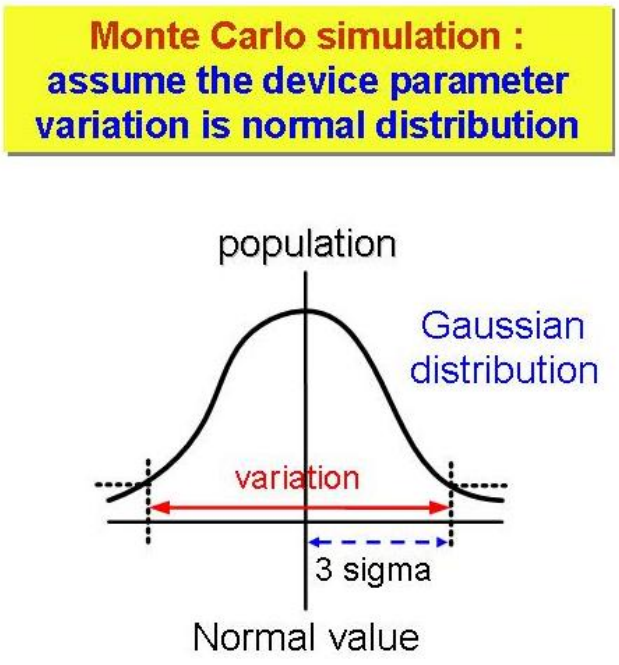


Fig. 4.6. The diagram of the assumption for Monte Carlo Simulation.

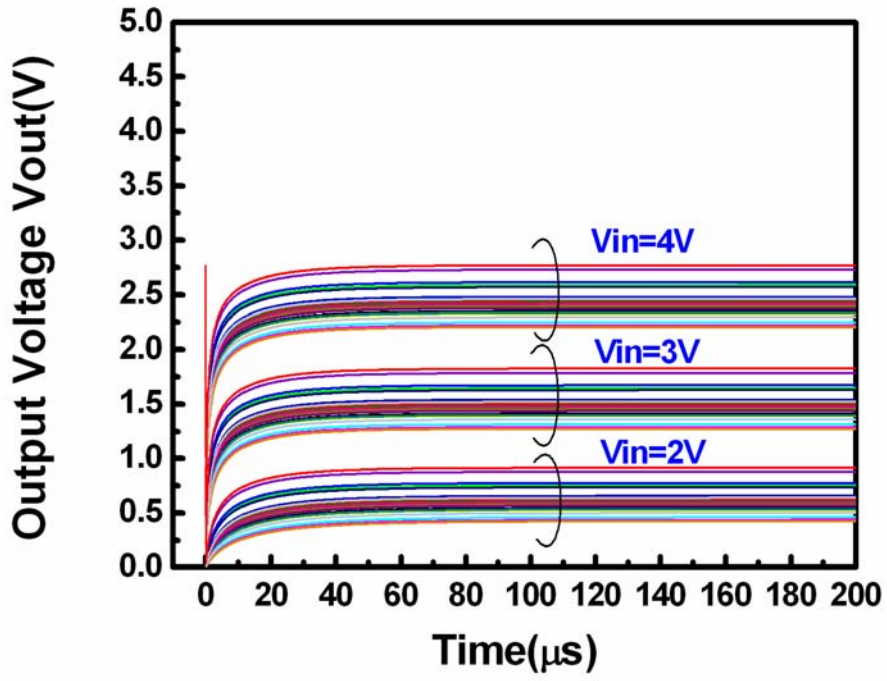


Fig. 4.7. Twenty times of Monte Carlo simulation results of the conventional source follower with an active load when input voltage 2V to 4V

4.3 Proposed Source-follower Type Analog Buffer

Since the conventional source-follower-type analog buffer suffers from large output voltage variation due to the inevitable non-uniformity of the poly-Si TFTs electrical characteristics as discussed previously. A new source-follower-type analog buffer is proposed in this article for compensating the device variations in LTPS TFTs.

Table 4.1 shows the schematic of the proposed analog buffer which is composed of two n-type thin film transistors, one storage capacitor and four switches. The design parameters of the proposed analog buffer are also shown in Fig. 4.9. The roles of these two NTFT are the driving TFT and the active load, respectively. The driving TFT is to provide the data voltage to charging the data line loading. Thus the large W/L ratio is designed for high driving capability consideration. The active load is used to as a constant current source to eliminate

the output unsaturated phenomenon of source follower and thus large channel length is chosen to minimize the kink effect. The gate terminal of the active load is bias with a constant voltage Vbias. The capacitor is supplied to compensate the device variation of driving TFT through the concept of self-compensation method which has been described in chapter 2. And in this work, the load capacitance of data line is assumed to be 20pF which corresponds to a 2-inch QVGA LCD.

The operation scheme and compensation principle of the compensating buffer circuit are described as follows.

(1) Compensation period:

During the first operating period, SW1 and SW2 are closed, and SW3 and SW4 are opened. Thus, the compensation is executed from the constant voltage source Vdd, and a voltage drop ΔV corresponding to the threshold voltage of driving TFT, the threshold voltage of the active load, and the bias voltage is stored in the capacitance Cvt.

(2) Data input period:

After the compensation period was executed, SW1 and SW2 are opened, and SW3 and SW4 are closed. The input data is then applied to one terminal of the storage capacitor to enter the data input period. Because of the gate to source voltage (V_{GS}) of the driving TFT is hold in the value of ΔV, the gate voltage of the driving TFT becomes the input voltage added to ΔV. Thereby, the output voltage will be equal to input data voltage, $V_{out}=V_{in}+\Delta V-\Delta V=V_{in}$. Consequently, the output voltage will be independent of the threshold voltage and the carrier mobility of the driving TFT and the device variation can be compensated through the capacitor and the operating sequence.

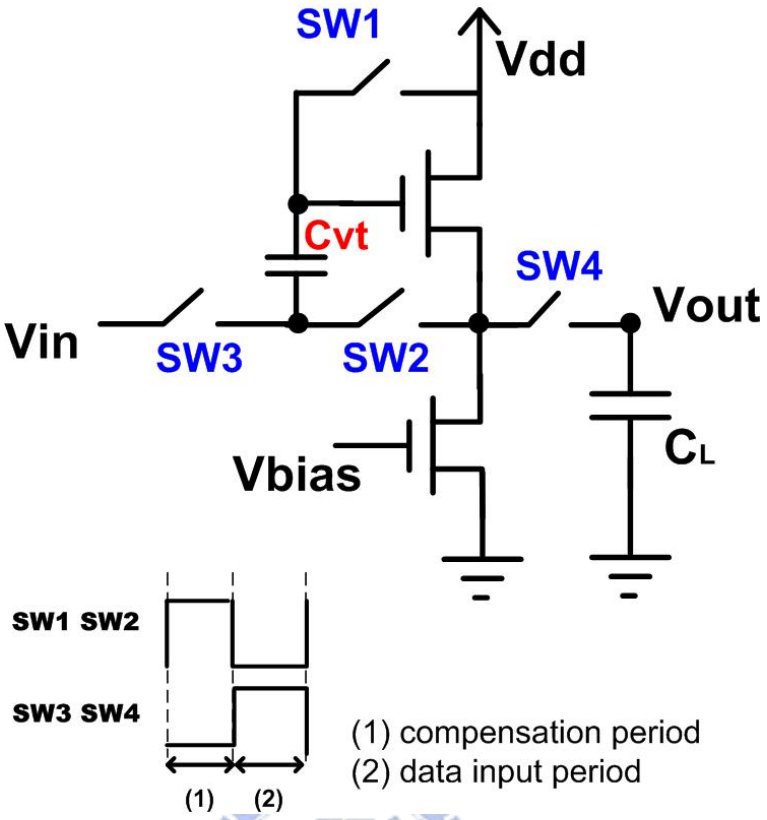


Fig.4.8. Schematic and the timing diagram of the proposed source-follower-type analog buffer.

Devices				
W/L (switching TFT)	W/L (driving TFT)	W/L (active load)	Cvt	C_L
8 μ m/8 μ m	100 μ m/8 μ m	8 μ m/50 μ m	2pF	20pF
Signal Lines				
Vdd	SW1~SW4	Bias voltage for the active load		
10V	0~10V	2~2.5V		

Tab 4.1. Design parameters of the proposed source-follower-type analog buffer.

4.4 Simulation and Measurement Results of the Proposed Analog Buffer

In this section, the output performance of the proposed analog buffer is studied and verified through both the circuit simulation and experiment. In the circuit simulation, HSPICE circuit simulator was performed. The typical model of the poly-Si TFTs for simulation is expressed by the PRI parameters. The device parameters such as threshold voltage and mobility are 1.45V and 65.69cm^2/V-sec for n-type TFTs, and -0.99V and 61.51cm^2/V-sec for p-type TFTs. The load capacitance of data line is assumed 20pF which corresponds to a 2-inch QVGA LCD.

4.4.1 Simulation Results and Discussion

In this work, Monte Carlo simulation is executed to study the effect of the device variation on the proposed circuit design, where the simulation condition is the same as that used in section 4.2.2. Fig. 4.9 shows the twenty times Monte Carlo simulation result of the output waveform of the proposed analog buffer when input voltage is 2V, 3V, and 4V. Compared to the simulating result of the source follower with active load shown in Fig. 4.7, it is clear that the output variation decrease drastically. The output voltage variation of the conventional source follower with active load is larger than 500mV, while that of the proposed analog buffer is commonly smaller than 25mV regardless of the large variation of LTPS-TFTs characteristics. It verifies that the device variation of LTPS TFTs can be compensated successfully by the proposed analog buffer.

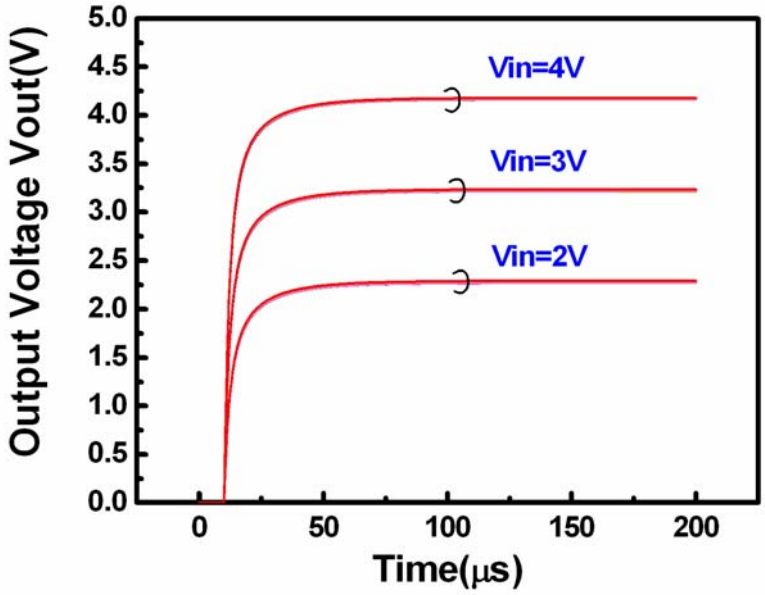


Fig.4.9. Monte Carlo Simulation output waveform of the proposed analog buffer when input voltage is 2V, 3V, 4V.

4.4.2 Fabrication Process and Measurement Result of the Proposed Analog Buffer

In addition to circuit simulation, the proposed analog buffer is also fabricated and measured to study its output performance after buffer circuit design finished. The testing buffer circuits were fabricated using a LTPS CMOS process. The fabrication process is described as follows. A buffer oxide and 500Å-thick a-Si was first deposited on the glass substrate sequentially. Then the amorphous silicon thin film was crystallized to poly-crystalline silicon film by KrF excimer laser annealing at room temperature. After the active region was defined, the channel doping was carried out for adjusting the threshold voltage of n-type TFT. Then, high dose ion implantation was executed to source/drain regions of n-type TFT. Next, 1000 Å-thick gate oxide was deposited by plasma enhanced chemical

vapor deposition (PECVD). A 3000Å-thick Cr film was deposited next. Then, the gate oxide and the Cr film were etched to form the gate electrode. Next, a high dose self-aligned ion implantation was executed to form source/drain regions of p-type TFT. Then a 4000Å-thick SiNx was deposited by PECVD as interlayer. Finally, the test circuits for the proposed analog buffer were accomplished after the contact holes formation and the 4000Å-thick Cr metallization. The image of optical micrograph of the proposed analog buffer circuit is shown in Fig. 4.10.

The measurement system for these testing buffer circuits is shown in Fig. 4.11. It includes four units: (1) Agilent 4156C including probe station and parameter analyzer, (2) HP 41501A pulse generator for providing control signal pulse, (3) Keithley 617 programmable electrometer for supplying one DC signal voltage through an additional probe, (4) Agilent MSO6034A mixed signal oscilloscope to display the output signal through the coaxial cable and BNC connection.

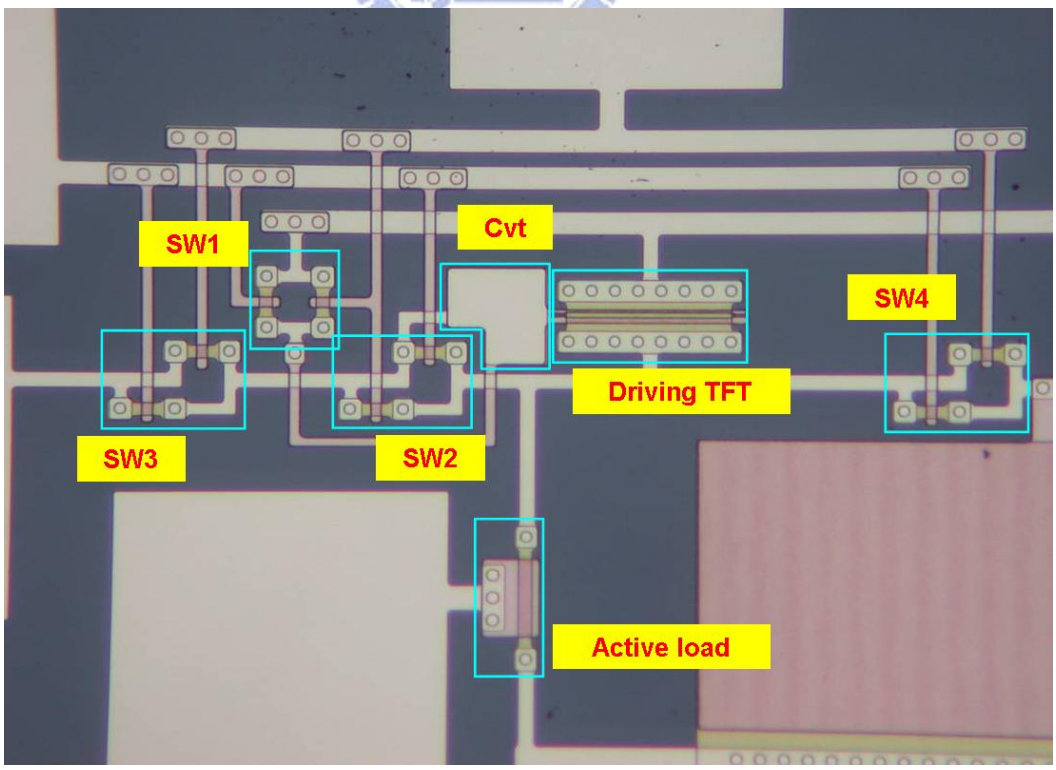


Fig. 4.10. Optical micrograph of the proposed analog buffer circuit.

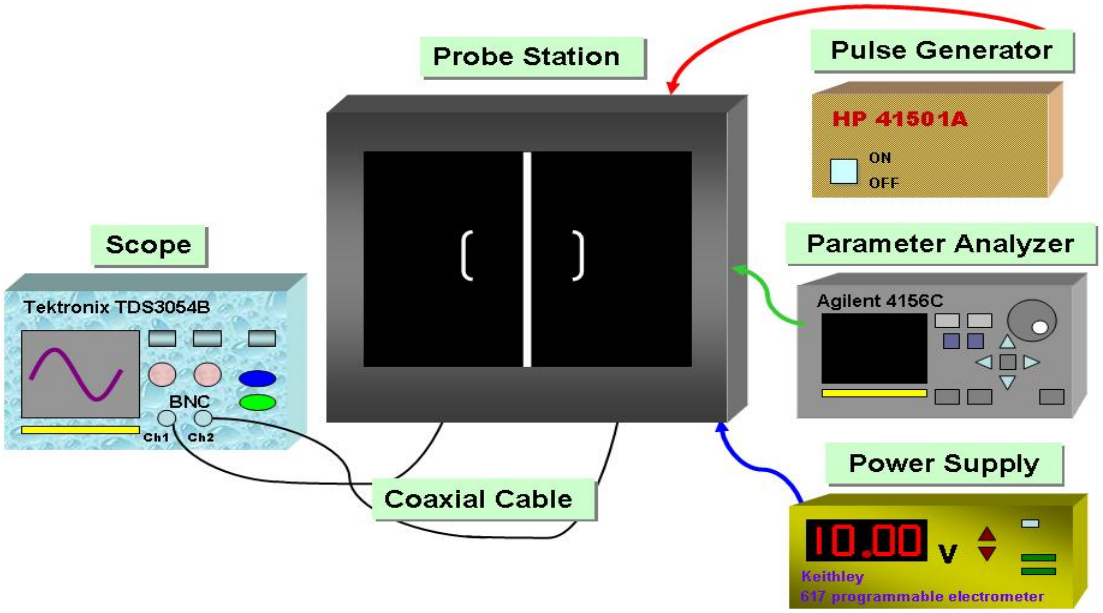


Fig. 4.11. Measurement system for the testing buffer circuits.

After measurement system is ready for measuring, several testing buffer circuits of the proposed analog buffer and conventional source follower were measured. Fig.4.12 shows the measurement result of the offset voltage compared between the proposed analog buffer and the conventional analog buffer with input voltage varying from 1V to 6V. It is observed that output voltage of the proposed analog buffer is very closely to the actual input voltage. The maximum offset voltage of the proposed buffer is about 160mV which is much less than the large offset voltage (>1V) of the conventional analog buffer. In order to study the variation toleration of the proposed buffer, eight set of the buffer circuits are measured to gather statistics. The measured result shows that the conventional analog buffer suffers from large output offset variation as shown in Fig.4.13. On the other hand, the output offset variation of the proposed analog buffer is much smaller than that of the conventional analog buffer. It is evident that the proposed analog buffer can compensate the device-to-device variations of LTPS TFTs successfully.

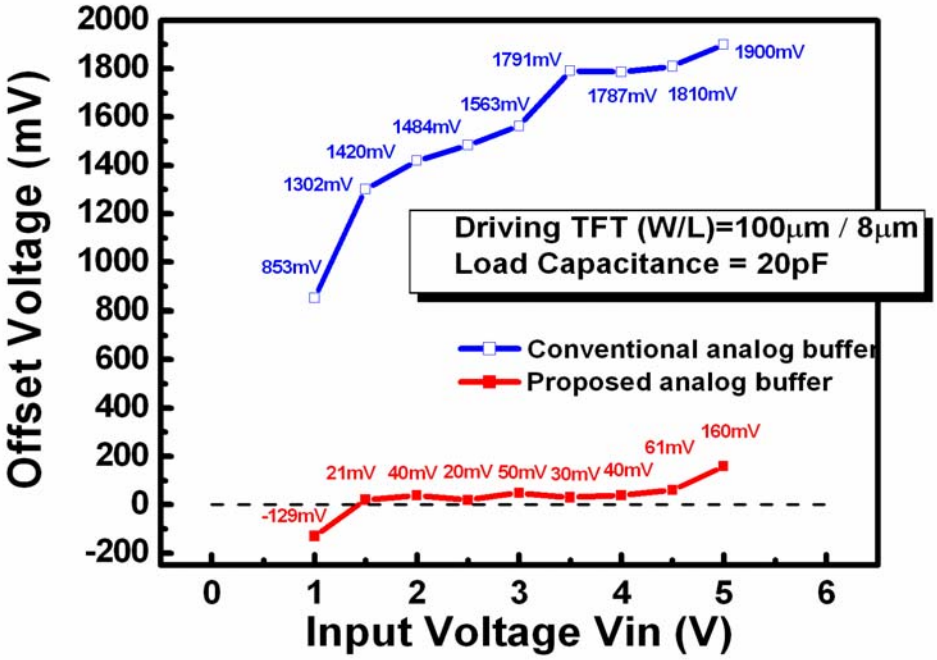


Fig.4.12. Measurement result of the offset voltage compared between the proposed analog buffer and the conventional analog buffer.

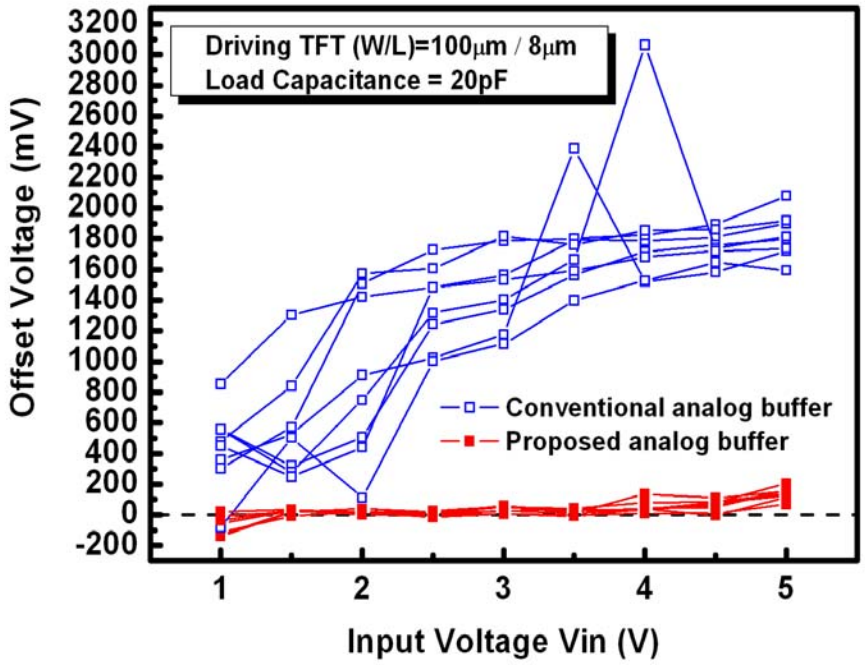


Fig.4.13. Offset voltage variation of 8 set of the analog buffer circuits are compared between the proposed analog buffer and the conventional analog buffer.

4.5 Bias Voltage Effect Discussion

The bias voltage of the active load is considered to be a factor that may affect the performance of the proposed analog buffer. The value of the bias voltage will determine the operation region of the active load, and the operation mode of the driving TFT and the active load in two operating period will affect the output characteristic due to the different output resistance of transistor in these two operation mode. Thus, in this section we will discuss the bias effect of the proposed analog buffer in detail.

First, the circuit simulation is executed to investigate how the bias voltage affects the output performance. Fig.4.14. shows the simulation result of the offset voltage and the power dissipation for the proposed analog buffer with bias voltage varying from 1.5V to 9.5V when input data voltage is 3V. It shows that the offset voltage defined as Vin minis Vout turns from positive to negative value as bias voltage increasing, and a minimum value of the offset voltage exists as the bias voltage is in the range between 2V to 2.5V. The tendency can be understood by the detailed discussion on the operation of driving TFT and the active load. During the first compensation period, the driving TFT is in the saturation region because of the diode connected configuration and the active load is also operated in the saturation region. However, during the data input period, the active load may operate in the saturation or the linear region depending on the bias voltage while the driving TFT still work in the saturation region.

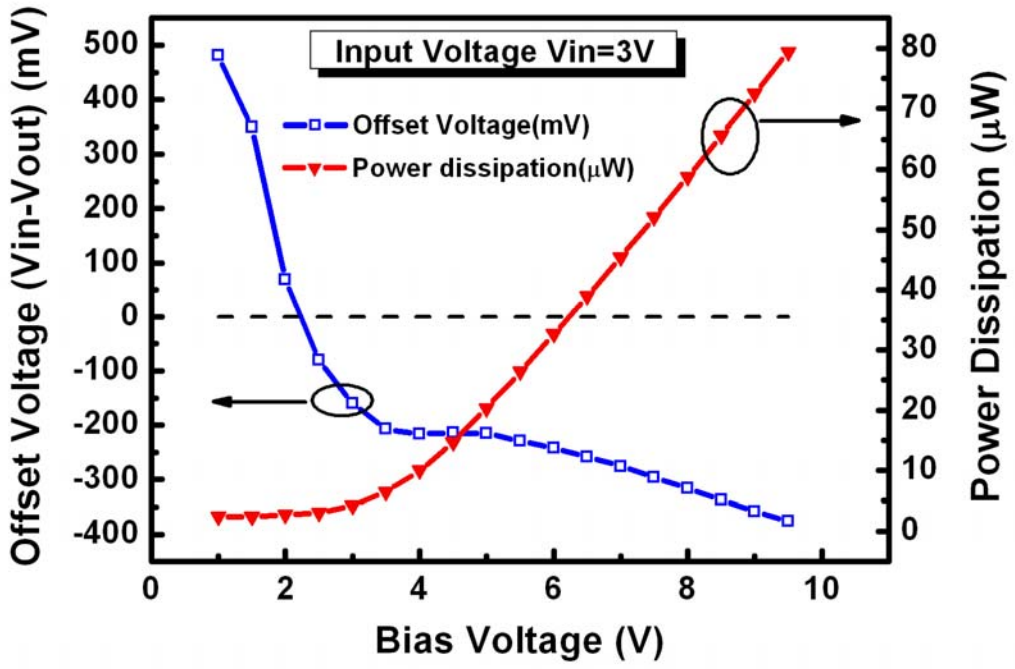


Fig.4.14. Simulation result of the output offset voltage and the power dissipation for the proposed analog buffer with different bias voltage.

These can be divided into two conditions for discussing. In the following, we will discuss these two conditions in detail by the mathematical analysis. Here the driving TFT is assumed to TFT1 and active load is TFT2 for convenience.

A. Driving TFT in saturation region, active load in saturation region at the data input period

(1)Compensation period:

$$I_D = K_1(V_{GS1} - V_{TH1})^2 = K_2(V_{GS2} - V_{TH2})^2 \tag{4.1}$$

, here K1=1/2μ$_1$CoxW$_1$/L$_1$; K2=1/2μ$_2$CoxW$_2$/L$_2$

$$\rightarrow K_1(V_{DD} - V_{out} - V_{TH1})^2 = K_2(V_{bias} - V_{TH2})^2 \tag{4.2}$$

$$\rightarrow a = \sqrt{K_1 / K_2} = \frac{V_{bias} - V_{TH2}}{V_{DD} - V_{out} - V_{TH1}} \tag{4.3}$$

$$aV_{DD} - aV_{out} - aV_{TH1} = V_{bias} - V_{TH2} \tag{4.4}$$

$$V_{out} = V_{DD} - V_{TH1} + \frac{1}{a}V_{TH2} - \frac{1}{a}V_{bias} \tag{4.5}$$

$$\therefore Cvt\_storage\_\Delta V = V_{DD} - V_{out} = V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias} \tag{4.6}$$

(2)Data input period:

$$I_D = K_1(V_{in} + \Delta V - V_{out} - V_{TH1})^2 = K_2(V_{bias} - V_{TH2})^2 \tag{4.7}$$

$$\rightarrow a = \sqrt{K_1 / K_2} = \frac{V_{bias} - V_{TH2}}{V_{in} + (V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias}) - V_{out} - V_{TH1}} \tag{4.8}$$

$$\rightarrow aV_{in} - V_{TH2} + V_{bias} - aV_{out} = V_{bias} - V_{TH2} \tag{4.9}$$

$$\Rightarrow V_{out} = V_{in} \tag{4.10}$$

From equation (4.6), it is observed that the threshold voltage and carrier mobility variations of driving TFT and the active load both can be stored in the capacitor for the compensation during the compensation period. Therefore, the output voltage will be in theoretically equal to the input voltage independent of the threshold voltage and the carrier mobility of the driving TFT and active load as shows in equation (4.10).

B. Driving TFT in saturation region, active load in linear region at the data input period

(1)Compensation period:

During the first operation period, the driving TFT and the active load will always work in the saturation region as the bias voltage is smaller than Vdd. Therefore, the situation in this condition during the compensation period is the same as described previously. In which the voltage stored in the capacitor is corresponding to the threshold voltage of driving TFT and active load, bias voltage and the K1/K2 ratio.

(2)Data input period:

$$I_D = K_1(V_{in} + \Delta V - V_{out} - V_{TH1})^2 = K_2[(V_{bias} - V_{TH2})V_{out} - \frac{1}{2}V_{out}{}^2] \tag{4.11}$$

$$\rightarrow a^2[V_{in} + \Delta V - V_{out} - V_{TH1})^2 = (V_{bias} - V_{TH2})V_{out} - \frac{1}{2}V_{out}{}^2 \tag{4.12}$$

from equation (4.3) :

$$\Delta V = V_{DD} - V_{out} = V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias} \tag{4.13}$$

$$\rightarrow a^2[V_{in} + (V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias}) - V_{out} - V_{TH1}]^2 \tag{4.14}$$

$$= (V_{bias} - V_{TH2})V_{out} - \frac{1}{2}V_{out}{}^2 \tag{4.15}$$

$$\Rightarrow V_{out} = \underbrace{\frac{2(V_{bias} - V_{TH2}) + 4a(V_{bias} - V_{TH2}) + 4a^2V_{in}}{2(1+2a^2)}}_{\text{(A)}} + \underbrace{\frac{\sqrt{[(4a+2)(V_{bias} - V_{TH2}) + 4aV_{in}]^2 - 4(2a^2+1)[2(V_b{}^2 + V_t{}^2)] + 4aV_{in}(V_{bias} - V_{TH2}) + 2a^2V_{in}{}^2 - 4V_{bias}V_{TH2}}}{2(2a^2+1)}}_{\text{(B)}} \tag{4.16}$$

assume that $2a^2 >> 1$, $4a >> 2$

(A) term can be simplified to: $V_{in} + \frac{(V_{bias} - V_{TH2})}{a} + \frac{(V_{bias} - V_{TH2})}{2a^2}$ (4.17)

(B) term :

$$\frac{\sqrt{[(4a+2)(V_{bias} - V_{TH2}) + 4aV_{in}]^2 - 4(2a^2+1)[2(V_b{}^2 + V_t{}^2)] + 4aV_{in}(V_{bias} - V_{TH2}) + 2a^2V_{in}{}^2 - 4V_{bias}V_{TH2}}}{2(2a^2+1)}$$

$$\approx \frac{\sqrt{[(4a)(V_{bias}-V_{TH2})+4aV_{in}]^2 - 4(2a^2)[2(V_b^2+V_t^2)]+4aV_{in}(V_{bias}-V_{TH2})+2a^2V_{in}^2 - 4V_{bias}V_{TH2}}}{4a^2}$$

(4.18)

$$\rightarrow \frac{\sqrt{[16a^2(V_{bias}^2+V_{TH2}^2)-32a^2V_{bias}V_{TH2}]+32a^3V_{in}(V_{bias}-V_{TH2})+16a^4V_{in}^2-[16a^2(V_{bias}^2+V_{TH2}^2)-32a^2V_{bias}V_{TH2}]-32a^3V_{in}(V_{bias}-V_{TH2})-16a^4V_{in}^2}}{4a^2}$$

(419)

$$\rightarrow \frac{\sqrt{0}}{4a^2}$$

(4.20)

Therefore, the output voltage can be simplified as

$$V_{out} = V_{in} + \frac{(V_{bias}-V_{TH2})}{a} + \frac{(V_{bias}-V_{TH2})}{a^2}$$

(4.21)

Equation (4.21) indicates that the output voltage will larger than the input voltage because that the bias voltage must be higher than the threshold voltage of the active load to turn on the active load. Therefore, we know that if the active load works in the linear region at the data input period, the output voltage will exceed the input data and thus a negative offset voltage is obtained. This situation will happen when the bias voltage is higher than the input voltage. Corresponding to the simulation result shown in Fig.4.14, it is obvious that the output offset voltage is the negative value as the bias voltage larger than the input voltage because the active load is in the linear region. Nevertheless, as the bias voltage is lower than the input voltage, the active load will operate in the saturation region and the output voltage is very closely to the input data voltage as expressed in equation (4.10).

In addition, an important information can be obtained from equation (4.21). It tells us that the output voltage can be almost equal to the input voltage when the Vbias is chosen to a lower value but just slightly above V_{TH2} and the large factor “a” is designed. The factor “a” is

related to the mobility and the W/L ratio of the driving TFT and the active load as represented in equation (4.3). Because of the mobility of the driving TFT and the active load are almost the same. Larger W/L ratio of the driving TFT and smaller W/L ratio of the active load were designed to possess large “a” factor which coincides with previously design in section 4.3. The output voltage is accurate as the factor “a” is larger. However, the optimum value in designing is required to meet the specifications of display.

Furthermore, from the mathematical analysis of bias voltage effect, we can see that the proposed analog buffer circuit can compensate not only the variations of the driving TFT but also the variations of the active load. In additional to the electrical characteristic variations, the issue of TFTs reliability is also taken into consideration in this discussion. In comparison with a-Si TFTs, LTPS TFTs have better long term reliability. For example, after 1000sec DC stress with Vg=7V and Vd=14V, the threshold voltage variation is about 0.5V and the degradation of carrier mobility is about 4% [4.20]. Moreover, the gate voltage of the active load is designed to be 2V in our proposed analog buffer which is in the very low voltage level. Therefore, it is almost no degradation of the active load in this bias condition and no apparent influence on the output performance will be seen in the proposed analog buffer circuit.

In additional to simulation result, the analog buffer circuits were also measured to study the bias effect. The measurement result is compared to the simulation result when input voltage 3V as shown in Fig.4.15. It is clear that the relationship between the offset voltage and the bias voltage of measurement result shows the same tendency with the simulation result. The simulation and measured result when input voltage 2V is also shown in Fig.4.16, and the same trend exhibited. According to the simulation and measured results, an optimum value of the bias voltage can be chosen to get the minimum output offset voltage. Furthermore, the power dissipation related to the bias voltage shown in Fig.4.14 exhibit that the power dissipation is small when the bias voltage is in the range corresponding to the minimum output offset voltage. It is clouded that an appropriate design of the bias voltage is required to

achieve high output performance and keep low power dissipation.

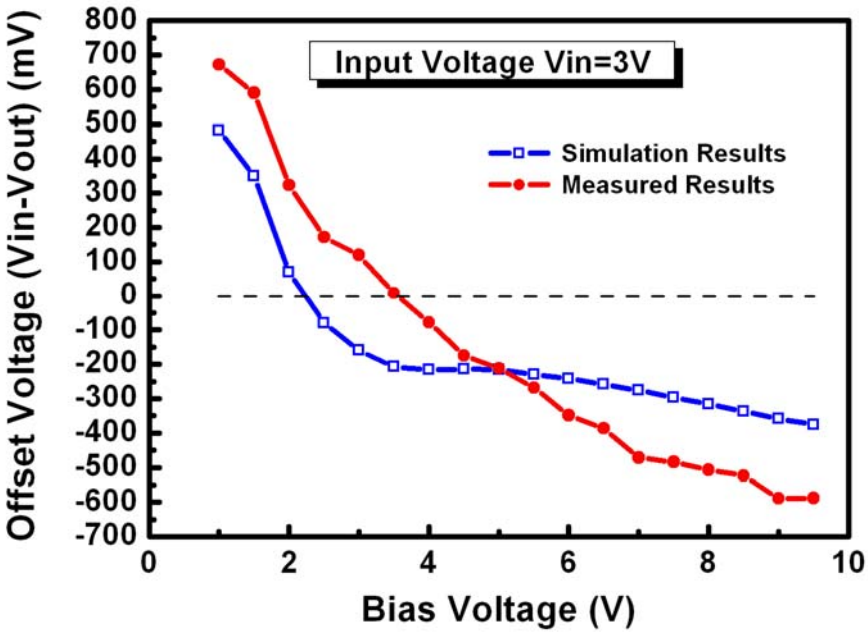


Fig.4.15. Output offset voltage versus bias voltage of the measurement result in comparison with the simulation result at input voltage Vin=3V.

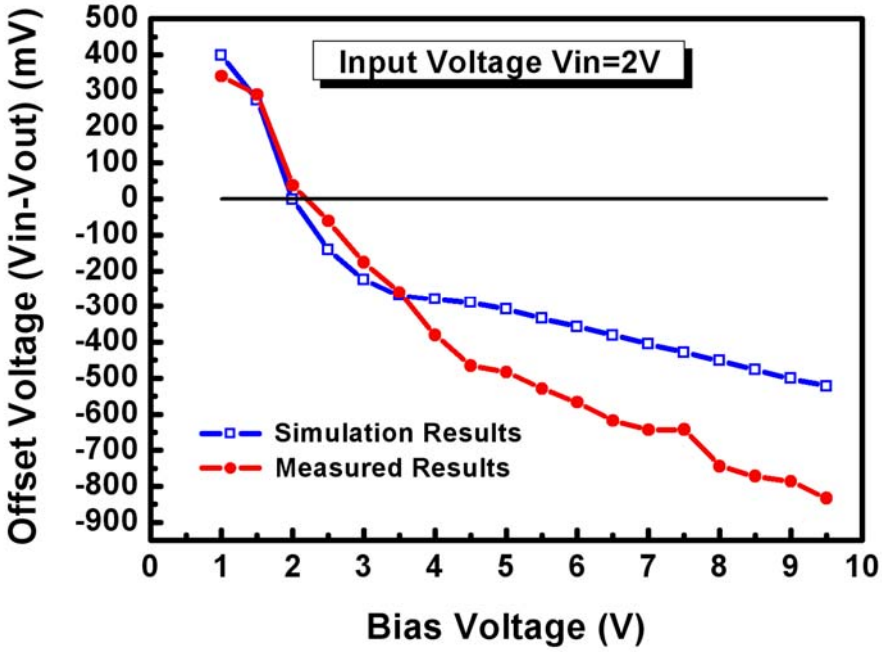


Fig.4.16. Output offset voltage versus bias voltage of the measurement result in comparison with the simulation result at input voltage Vin=2V.

4.6 Comparisons between the Proposed Analog Buffer Circuit and Others Analog Buffer Circuits

The comparisons of the proposed analog buffer and others analog buffer including op-amp type analog buffers and source-follower type analog buffers are given in the output performance, circuit configuration, and power consumption in this section. As shown in Taable 4.2, the output offset voltage deviation and the output offset voltage variations are both smaller than that of others buffer circuits expect sony's double-offset-canceling buffer. The output performance is superior to the Chung's push-pull analog buffer due to the compensation from the power supply line (Vdd) instead of the input signal line in Chung's buffer. Although the output performance of the sony's double-offset-canceling analog buffer is greater, the requirements of many transistors and extra applied signals which occupies large area and cause much higher power consumption in comparison with our proposed analog buffer. The circuits configuration and power dissipation of the proposed analog buffer are also superior to others buffer circuits.

Circuit Types \ Characteristics		Offset Voltage Deviation (mV) Vin=1~6	Offset Variation at Vin=4V (mV)	The Number of Transistors	The Number of Capacitors	Additional Number of Control Signals	Power Dissipation at Vin=4V (μW)	Output Resistance (kΩ)
Op-Amp Type	Typical Two-Stage	199	1434	7	0	0	78.4	339.7
	Itou's Differential Pair Com.	427	35	7 (Additional 6 TFTs needed for switches)	1	2	69.2	802.8
	Yiu's Bias Circuit Com.	452	546	10	0	1	184.5	35.7
Source-Follower Type	Conventional	570	562	1	0	0	4.4	15.1
	Chung's Push-Pull	816	46	2 (Additional 6 TFTs needed for switches)	1	2	6.7	15.3
	Sony's Double Offset	40	9	1 (Additional 14 TFTs needed for switches)	2	6 & additional current Source	12.4	99.9
	Jung's Matching TFT	1272	634	5	0	2	6.6	43.1
	Proposed Analog Buffer	165	20	2 (Additional 8 TFTs needed for switches)	1	2	5.8	99

Table 4.2 Comparison of the proposed analog buffer and others buffer circuits.

4.7 Summary

A novel source follower type analog buffer using low-temperature polycrystalline silicon thin film transistors (LTPS-TFTs) for the integrated data driver circuits of active matrix liquid crystal displays (AMLCD) and active matrix light emitting diodes (AMOLED) has been proposed. It is composed of two n-type thin film transistors, one storage capacitor and four switches. Besides the data line and DC power supply lines, two additional control signals were used. However, the sign of these two control signal are completely inverse, and thus only one control signal line is needed by adding an inverter. Therefore, an analog buffer with simple circuit configuration is achieved.

The proposed buffer circuit compensates the device variation of transistors by a

capacitor and the simple operation scheme. Both the simulation and measurement results exhibit that the output variation resulting from the variation of poly-Si TFT characteristics is successfully compensated in the proposed analog buffer. The output offset voltage is also eliminated through the compensation operation. Furthermore, the unsaturated of output voltage arisen from the significant subthreshold current is solved by adding an active load. The effect of the bias voltage applied to the active load is also discussed in this study. An optimum parameter of the bias voltage can be designed to achieve high output performance and keep low power dissipation of the proposed analog buffer. Consequently, the proposed analog buffer has high immunity to device variation, simple configuration, and low power consumption which is suitable for integrated system application.

Chapter 5

Summary and Conclusions

The uniformity issues of low-temperature polycrystalline silicon thin film transistors (LTPS TFTs) in devices and analog buffer circuits were investigated in this thesis. The multi-channel structure is employed to improve the uniformity of LTPS TFTs and the mechanism of improving device uniformity is proposed. In addition, the design of LTPS TFTs analog buffers has been studied. A new simple source-follower type analog buffer with compensating configuration has been proposed. The improvement of output variation is achieved by compensating the device variations through a capacitor and the appropriate operation schemes.

In chapter two, several kinds of analog buffer circuits using LTPS TFTs are introduced and discussed. These analog buffer circuits are classified into operational amplifier type (op-amp-type) analog buffer and source-follower type analog buffers according to their circuit architecture and divided into six major compensating methods. These compensating architectures of analog buffer circuits are necessary owing to the electrical characteristic variation of the transistors resulting from the random distribution of grain boundaries. The advantages and disadvantages of each kind of circuit compensating method have also been discussed and compared. In conclusion, the source-follower type analog buffer with simple configuration, better immunity to the LTPS TFTs device variation, and lower power dissipation is considered to be the best candidate for system-on-panel applications.

In chapter three, the effects of multi-channel structure on the device uniformity of LTPS

TFTs and the output performance of source follower analog buffer are investigated. It is clear that variations of the threshold voltage and subthreshold swing are reduced as channel stripes increasing, while no such tendency can be seen in the transconductance and leakage current. The mechanism of the improving uniformity of multi-channel structure is discussed and it is considered that probability effect is the most possible cause. According to the probability distribution, better uniformity of threshold voltage and the subthreshold swing of poly-Si TFTs can be obtained with channel slicing due to the more uniform grain boundaries densities between transistors. While the variations of the mobility and leakage current can not be reduced due to the remained tail states variations of multi-channel devices. At last, the conventional source follower with multi-channel structure is also studied. It is clear that the output offset voltage variations of source follower with multi-channel structure in the driving TFT are reduced to about half of that in conventional source follower. It confirms that the variations of poly-Si TFTs indeed can be reduced by the multi-channel structure.

In chapter four, a novel simple source follower type analog buffer using low-temperature polycrystalline silicon thin film transistors (LTPS-TFTs) for the integrated data driver circuits of AMLCD and AMOLED has been proposed. It consists of two n-type thin film transistors, one storage capacitor and four switches. Both the simulation and measurement results exhibit that the output variation resulting from the variation of poly-Si TFT characteristics is successfully compensated in the proposed analog buffer. The output offset voltage is also eliminated through the compensation operation. Furthermore, the unsaturated of output voltage arisen from the significant subthreshold current is solved by adding an active load. The effect of the bias voltage applied to the active load is also discussed in this study. An optimum parameter of the bias voltage can be designed to achieve high output performance and keep low power dissipation of the proposed analog buffer. Consequently, the proposed analog buffer has high immunity to device variation, simple configuration, and low power consumption which is suitable for integrated system application.

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論文題目：低溫複晶矽薄膜電晶體元件均勻性及類比緩衝電路之研究

Investigation of the Uniformity of Low-Temperature Polycrystalline Silicon Thin Film Transistors in the Devices and Analog Buffer Circuits