國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

高壓元件 LDMOS 可靠度分析
與 SPICE 模型建立

Investigation of Spice Modeling and Reliability Issues in High Voltage LDMOS

研 究 生 ：杜冠潔

指導教授 ：汪大暉 博士

中華民國 九十五 年 六 月

高壓元件 LDMOS 之特性分析與 SPICE 模型建立

Investigation of Spice Modeling and Reliability Issues in High Voltage LDMOS

研 究 生 ：杜冠潔　　Student : Kuan-Chieh Tu

指導教授 ：汪大暉 博士　　Advisor : Dr. Tahui Wang

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master

in

Electronic Engineering

June 2006

Hsinchu, Taiwan, Republic of China.

中華民國 九十五 年 六 月

高壓元件 LDMOS 可靠度分析與 SPICE 模型建立

學生：杜冠潔　　指導教授：汪大暉 博士

國立交通大學　電子工程學系　電子研究所

摘要

隨著半導體產業的發展，高功率元件經常被應用在許多電力電子方面。LDMOS(平面二次擴散之金氧半場效電晶體)通常在高壓積體電路中作為驅動元件。本論文內容探討 LDMOS 的基本特性，並建立 SPICE 模型，最後作可靠性分析。

由於結構與傳統 MOSFET 有所不同，故在應用上缺少內建的高壓元件模型，本論文中，利用子電路（sub-circuit）的模擬方法來建立 LDMOS 電流-電壓 SPICE 模型。此子電路中主要部分包含了一個傳統 MOSFET 與一個受閘極與汲極控制的可變電阻。首先，先以一個 MOS 模型描述邊際效應(Fringe effect)所產生的邊際電流(fringe current)；再利用 LDMOS 在低閘極電壓與高閘極電壓有著不同特性的現象，從低閘極電壓區域萃取出 MOS 模型，再藉由此 MOS 模型反算出外掛電阻模型，最後以自我熱效應公式修正模擬值，即完成一單一尺寸 LDMOS 模型。並考慮不同尺寸與操作環境的應用，將四個邊界尺寸模型做箱化，以期最後可適用於各種尺寸與操作模式的元件。

在 LDMOS 可靠性研究上，我們使用電荷幫浦的實驗方法(Charge Pumping Technique)探討不同的加壓條件下，不同的區域各有何不同的損害產生。

根據我們的研究，可以歸納出以下結果：可以從 LDMOS 本身萃取出 SPICE

模型，而不需要 MESDRIFT 結構(多了一個接觸點佈值); 並可以對尺寸做模型箱化，成功的使模型可以準確模擬不同尺寸與環境的 LDMOS。而在可靠度的研究上也發現，在有最大閘極漏電流的加壓條件下，LDMOS 的熱載子退化現象最為明顯。

Investigation of Spice Modeling and Reliability Issues in High Voltage LDMOS

Student: Kuan-Chieh Tu Advisor: Dr. Tahui Wang

Department of Electronics Engineering &

Institute of Electronics

National Chiao Tung University

Abstract.

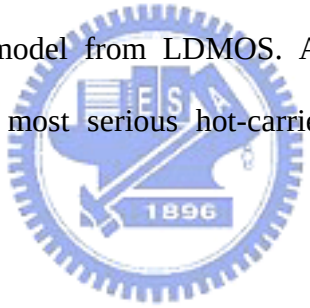
Power metal-oxide-semiconductor field-effect transistors (MOSFETs) have been widely applied to power electronics owing to great semiconductor industry. LDMOS (lateral Double-Diffused MOSFET) is usually the driver component in high voltage integrated circuits. In our study, we will engage in the characteristics of LDMOS including of SPICE macro model and the reliability issues.

Because the architecture of a LDMOS is different from it of a MOSFET, there is still a lack of SPICE model for LDMOS. In our study, we use the sub-circuit method to model a LDMOS device. The method mainly consists of an intrinsic MOS model and a gate and drain voltage controlled resistance. In addition, we model the extra fringe currents by giving a fringe MOS model. After deducing the influence of the fringe effect, we extract the MOS

model from I-V measured data in low-Vg stage region and reverse calculate the external resistance in high-Vg stage region using the MOS model. Finally, the model is amended by correcting function of self-heating. Not only achieving a single size device, we also consider the application of LDMOS scaling problems and various operation modes. Therefore, we used the binning technique to bin the models from four corner size models to generate a universal SPICE macro model suitable for various devices of different sizes and operation conditions.

Another part of our study is the investigation of the reliability issue of various hot-carrier degradation modes. We identify the properties of trap types and locations of oxide damage under different hot-carrier stress modes by using a novel three-region charge pumping technique.

According to our study, we can conclude that: We don’t need MESDRIFT devices and can extract a SPICE macro model from LDMOS. And the research about reliability of LDMOS shows that there is most serious hot-carrier degradation under max. Ig stress condition.



致謝

謝謝曾經協助我論文的每個人。這段旅程的完結開啟了下一段冒險的序幕。

Contents

Figure & Table Captions

\