Chapter 1

Introduction

From a historical perspective, power semiconductor devices have played an increasingly important role in the development of power electronic systems over the last 50 years. From the beginning with the invention of the bipolar transistor in the late 1940's to the power MOSFET first introduced commercially in the 1970's which is redesigned to LDMOS (lateral double-diffused MOS) for increasing voltage blocking capability, year by year, we can see the application and operation range are expanding [1]. The applications for power semiconductor devices are quite diverse as shown in Fig. 1.1 and Fig. 1.2 [2].

However, an ideal power device is capable of handling high currents and voltages and switching at a high speed at the same time, but it can't be satisfied all three requirements simultaneously. The LDMOS, the main object of this study, is classified as requiring relatively low breakdown voltage (less than 100volts) but high current handling capability and high speed and usually used in automotive electronics, switch mode power supplies, and etc. Because of these advantages plus process compatibility to CMOS technologies [3],[4] , LDMOS transistors is one of the widely used power MOSFETs in high-voltage (HV) applications now.

Although power devices are getting more popular, the problem of lacking a simple accurate SPICE HV MOS model for HV IC simulation is more serious. The most crucial ways of modeling HV MOS are to combine either a nonlinear resistance [5],[6],[7],[8] or a JFET [9] with a MOSFET. However, most of sub-circuit methods don't consider the width/length effects and different temperature and bulk bias conditions. In our work, we choose a SPICE sub-circuit method consisting of a

MOSFET and a non-linear resistance for the simulation of LDMOS. Our method not only combines specific physical-based phenomena, such as quasi saturation and the fringe effect but also takes account of the width/length effect and different temperature and bulk bias conditions. .

Another important topic is the hot carrier reliability. LDMOS used as a driver is usually biased at high drain voltage, so the hot-carrier degradation is needed to be concerned about. The hot-carrier effect not only causes the reduction of the Safe Operating Area (SOA) but also lets the life time of devices decrease [11]. In our report, we identify the location of oxide damage and trap types induced after hot-carrier stress by using three-region charge pumping technique.

This thesis is organized as follows: Chapter1 is introduction. Chapter2 indicates the structure of the LDMOS used throughout this work and analyzes some characteristics of it. Chapter3 shows the extraction flow of SPICE LDMOS model. A novel two stages extraction method of LDMOS is proposed. Several physical-based parameters are also discussed. Then, the hot-carrier degradation issue is introduced in Chapter4. Finally, we will make a brief conclusion.

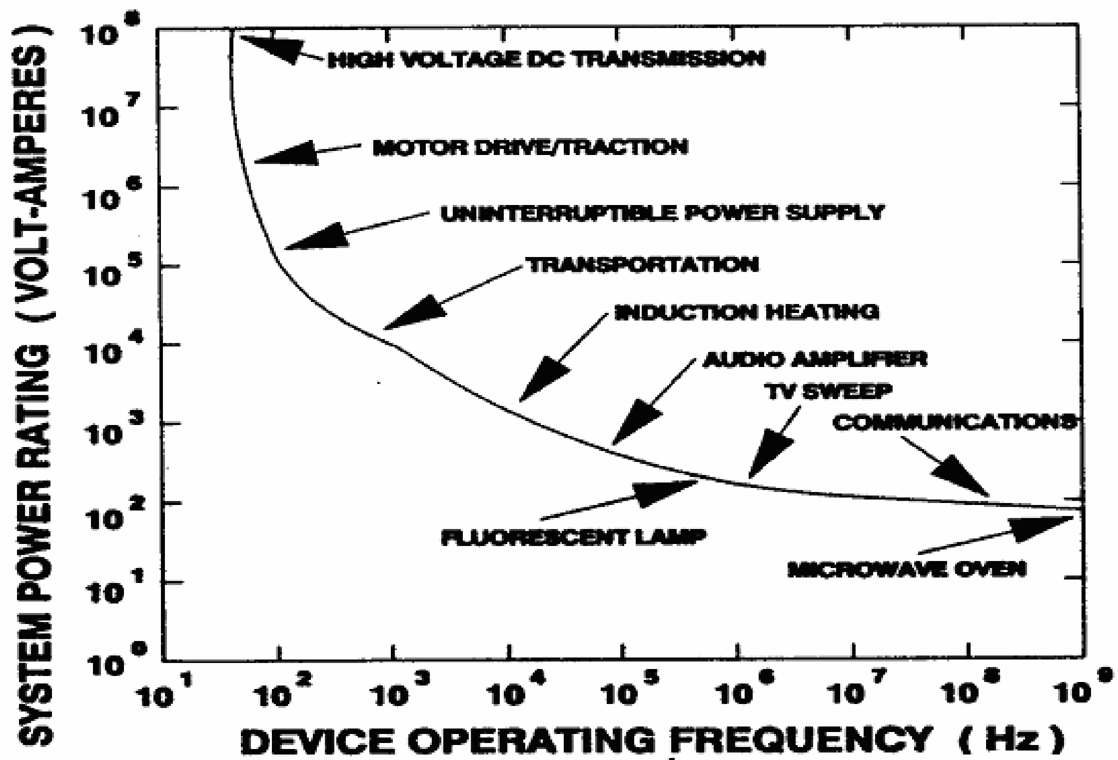


Fig. 1.1 Applications for power semiconductor devices provided as a function of system operating frequency and power handling capability.

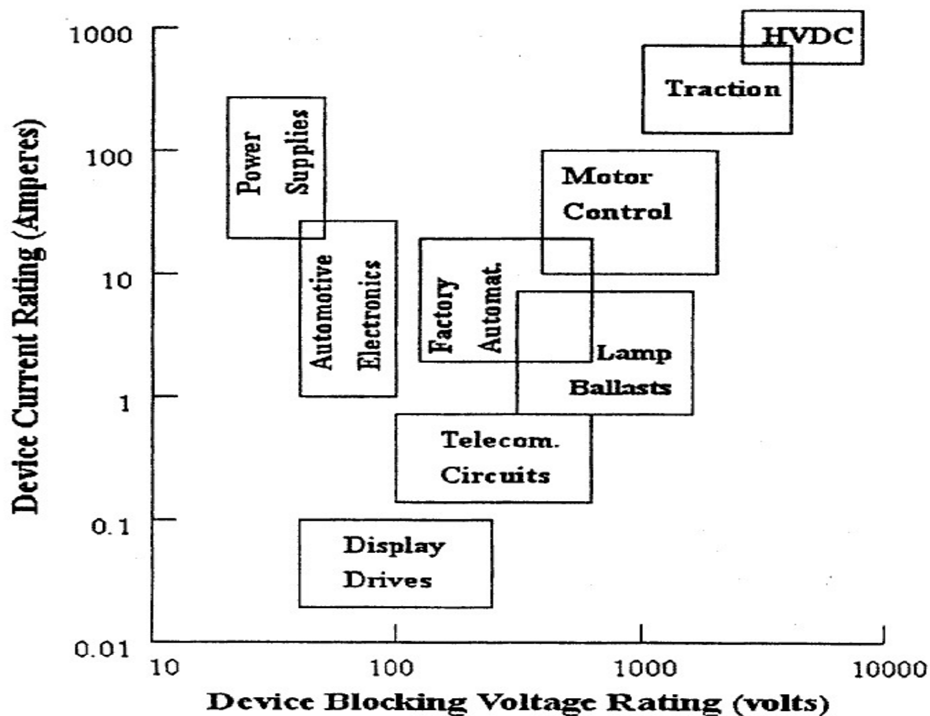


Fig. 1.2 Applications for power devices in relation to their voltage and current ratings.

Chapter 2
Analysis of LDMOS Characteristics

2.1 Introduction

In this chapter, the characteristics of LDMOS including the I-V curve, the quasi-saturation effect, and the reliability issues are analyzed. First, a schematic view of LDMOS is provided. Then, the basic I-V curves and the quasi-saturation effect are illustrated. Finally, the three crucial special issues are investigated. The self-heating effect and the fringe effect mechanism are discussed and this discussion of phenomena help us provide an accurate model next in Chapter 3; the hot carrier induced degradation is also explained and will be examined it in Chapter 4.

2.2 Basic Structure and I-V Curve Discussion of LDMOS

2.2.1 LDMOS Basic Structure and I-V Curve Discussion

The cross section of N-LDMOS studied in our work is shown in Fig. 2.1. The whole device is inside a lightly epitaxial layer. The double diffused n^+/P-Body region forms source and channel, and a threshold voltage adjustment layer should be used to avoid a laterally varying doping concentration in the channel region. The n^- drift region extends primarily from the PBODY into drain leading to a voltage drop between the heavily n^+ doped drain contact region and the channel of the device. Higher breakdown voltages are achieved due to the n^- drift region. For reliability analysis, source and substrate contacts are separated, but substrate contact is close to source contact. The oxide region with verified thickness and covers two regions: the first one is the thin gate oxide above the channel region and a part of the drift region; the second is thick field oxide above the drift region. The degree of current spread out

across the whole body of the drift region and the gate controlling ability depend on the thickness of the thick field oxide [12]. The field plates (the portions of the poly-gate that cross over the drift region) can increase the breakdown voltage because of reducing field crowding at the edge of depletion layer under the poly-gate.

Some important features of LDMOS transistor are outlined, which are the effective channel length L_{chan}, the accumulation length L_{acc}, the field oxide length L_{fox}, and the drift region length L_d. The P-Body concentration and n^- drift concentration are also important parameters for deciding V_{th} and the operation voltage.

The LDMOS devices used in our work were processed in a 0.18 μm CMOS technology with a gate oxide thickness of 100nm and a field oxide thickness of 500nm. The lengths of LDMOS devices vary from 1.7 μm to 20 μm; the widths of them vary from 3 μm to 20 μm. The operation voltages are Vg=40V and Vd=40V. Threshold voltages of LDMOS devices are around 1.5V. The measured I-V curves including IdVg curve at linear region (Vd=0.1V) and IdVd curve at Vg=2, 9.5, 17, 24.5, 32V are shown in Fig. 2.2(a) and Fig. 2.2(b).

2.2.2 Quasi -Saturation Effect

In this section, we discuss a crucial phenomenon in LDMOS called "quasi-saturation effect". The quasi saturation effect does not occur in traditional MOS transistors but appears in power MOSFET devices like LDMOS obviously. When the gate voltage is sufficiently high, comparing to traditional MOSFETs, the increase of saturation currents is relatively small[13]. By measuring the DC characteristics in our LDMOS transistors, it is clearly shown that the drain current is limited at high gate voltage in Fig. 2.2(b). The reason for the occurrence of quasi-saturation effect at high gate voltages is that the conductivity of the channel region is high, whereas that of the drift region is low due to depletion in it. For further

increasing drain voltage, the depletion layer widens and the drain current through the drift region becomes crowded, which leads to velocity saturation in the drift region [14]. Unlike traditional MOSFET devices, the drain current tends to enter saturation region because of the pinch-off of the channel at the drain side.

The quasi-saturation effect has been solved by two main approaches. One is by developing physically based compact models which are efficient and relatively simple but lack flexibility [14],[15],[16]. The other is by using sub-circuit models. The sub-circuit model combines external components, such as JFET[9] or variable resistance [5],[6],[7],[8], with a MOSFET together to form an equivalent circuit of a true LDMOS. In our study, we use nonlinear resistance controlled by drain and gate to model the drift region and the macro model extraction method will be demonstrated in Chapter 3.

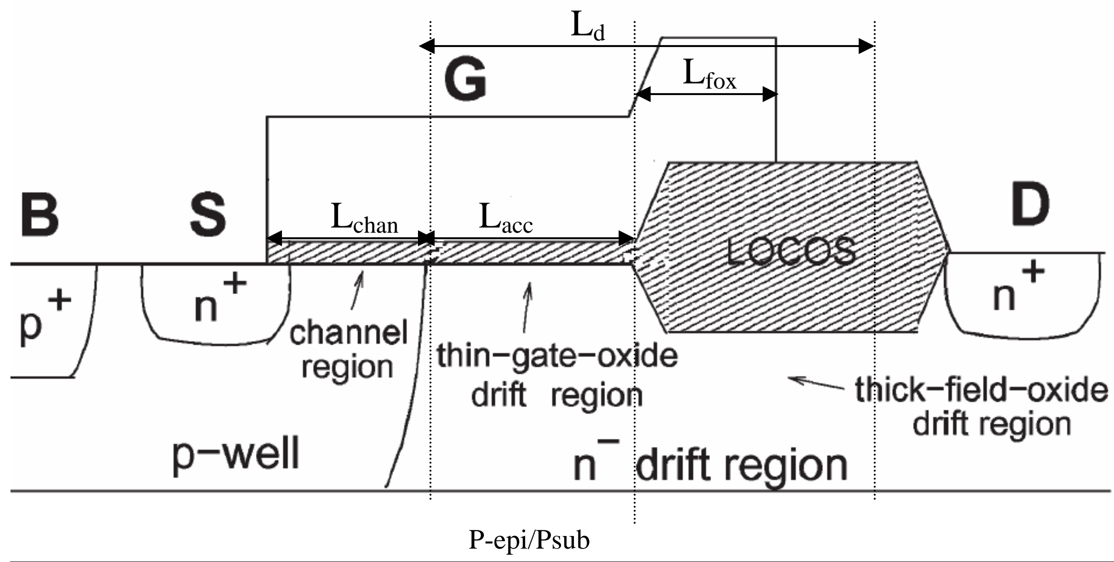


Fig. 2.1 Schematic cross section of NLDMOS device used in our study.

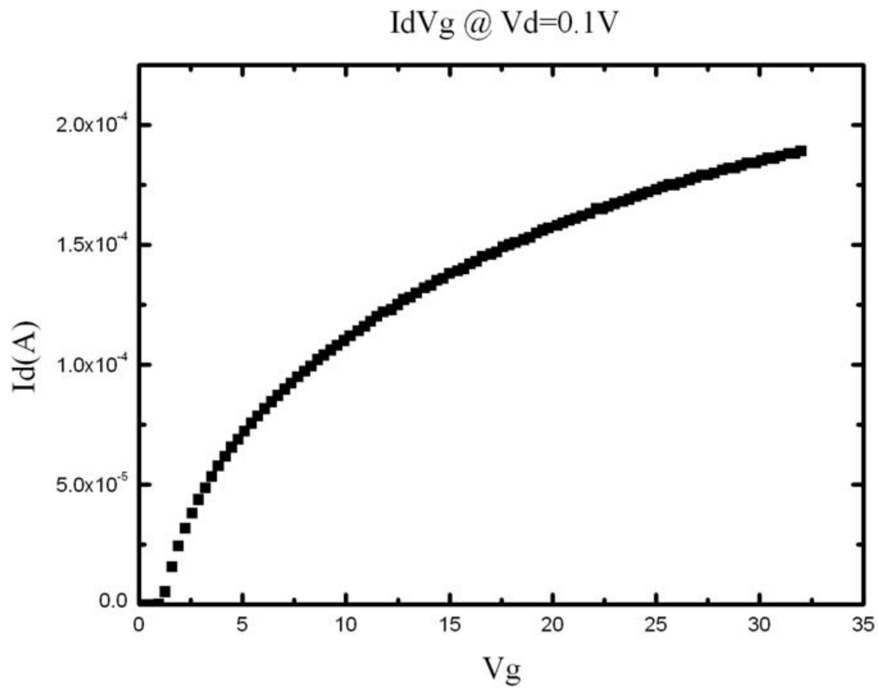


Fig. 2.2(a) Measured Id-Vg characteristics at Vd=0.1 of NLDMOS (W=20 μm, L=1.7 μm).

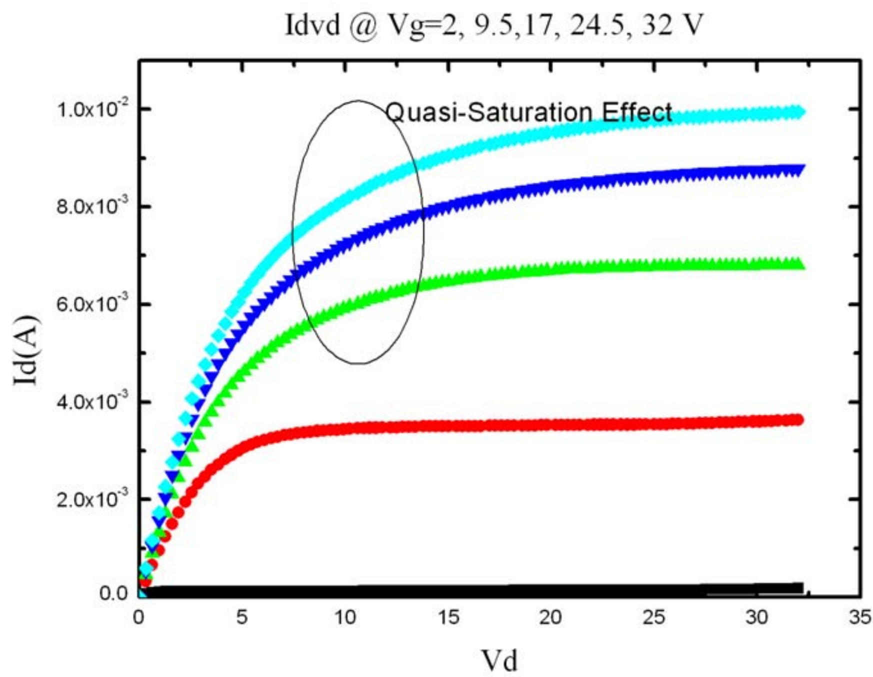


Fig. 2.2(b) Measured Id-Vd characteristics at Vg=2, 9.5, 17, 24.5, 32V of NLDMOS (W=20 μm, L=1.7 μm).

2.3 Special Issues of LDMOS

2.3.1 Fringe Effect

The fringe effect can be illustrated in Fig. 2.3. In Fig. 2.3, we can see that the gate area exceeds the channel region, so there are some extra currents which go through this extension area and make the total drain current increase. This extension area leads the side effect which can be shown clearly in Fig. 2.4. We find out that there is an abnormal “two-stage turning on effect” shown in IdVg data and the drain currents increase by different trends in different range of Vg. As shown in the figure, current is normalized by width ate the same length. In IdVg curve at Vd=0.1V, the normalized Id by W=5 μm is larger than the normalized Id by W=20 μm. Besides the examination of various widths, we also compare the data of different lengths with the same width in Fig. 2.5. It demonstrates that the device with short length is influenced by the fringe effect more seriously than the longer length. Because the fringe effect occurs more seriously in small devices, we will model the fringe effect by using small devices later in Chapter 3.

2.3.2 Self-Heating Effect

The current tendency in microelectronic industry is to the down scaling of electronic components leading to power increase. This means that thermal effects must be taken into account in the design. It is known that the temperature under the operation of devices has a considerable influence on reliability and performances, which can modify and degrade transistor behavior [17],[18].

In Fig. 2.6, we can clearly see the self-heating effect on our LDMOS devices. It causes a reduction in the mobility of the carriers in the device and hence increases the on-resistance. This leads to a decrease in current levels of the device and negative output conductance effect [19]. Moreover, self-heating would induce thermal

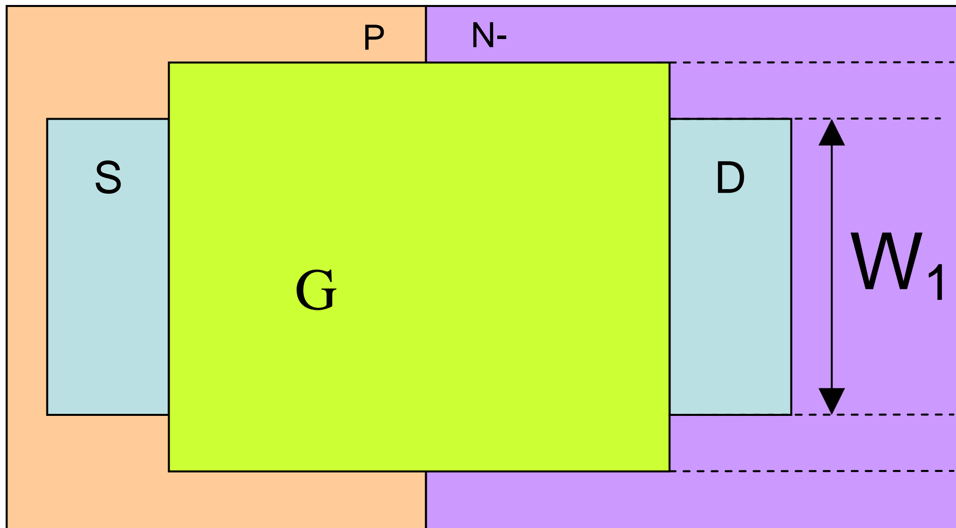
instability which causes thermal runaway finally. The thermal SOA boundary is defined by the device being thermal runaway [11].

The characterization of the interaction between electrical and thermal effects is needed to understand and precisely explore the Safe-Operating-Limits (SOA). There are many reports which estimate of channel and junction temperature to help identify the self-heating effect and give an accurate model. The most popular approach now is to model the degradation performance of device by using a voltage pulse system [20],[21],[22]. The system includes thermal resistance and thermal capacitance to form a thermal parasitic network of the LDMOS. In our study, we will examine the self-heating effect at room temperature and model it by giving an appropriate function for describing the degree of degradation in Chapter 3.

2.3.3 Hot-Carrier Effect

Hot-carrier effect is one of the foremost reliability problems in submicron MOSFET transistor [23]. Since LDMOS transistors are the devices of a choice to combine standard CMOS process for smaller sizes and lower cost, they face this reliability issue too. Under the influence of the high lateral fields, electrons or holes in the channel and pinch-off region can gain sufficient energy such that their energy distribution becomes much greater than would be expected if they were in equilibrium with the lattice. The generation of these hot carriers called hot-carrier effect can be the cause of several reliability problems. The hot carriers can lose their energy via impact ionization, which results in substrate currents. These substrate currents may initiate latch-up problem. Besides, if the hot carriers acquire sufficient energy to surmount the energy barriers or tunnel into the oxide, their passing through the Si-SiO2 interface can lead to the generation of interface traps and to electron and/or hole trapping in the oxide. These phenomena will then induce threshold voltage shifts and

transconductance degradation. In Chapter 4, we will examine the hot-carrier degradation under non-uniform hot-carrier injection conditions by three-region charge pumping technique.



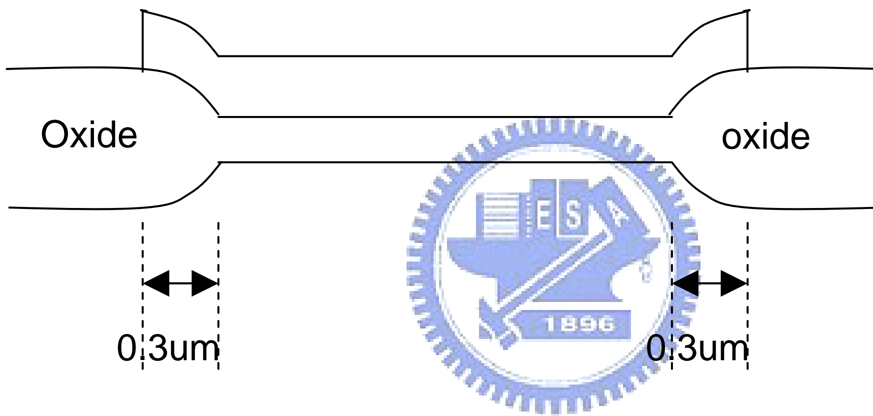


Fig. 2.3 The schematic top view and side view pictures of LDMOS.

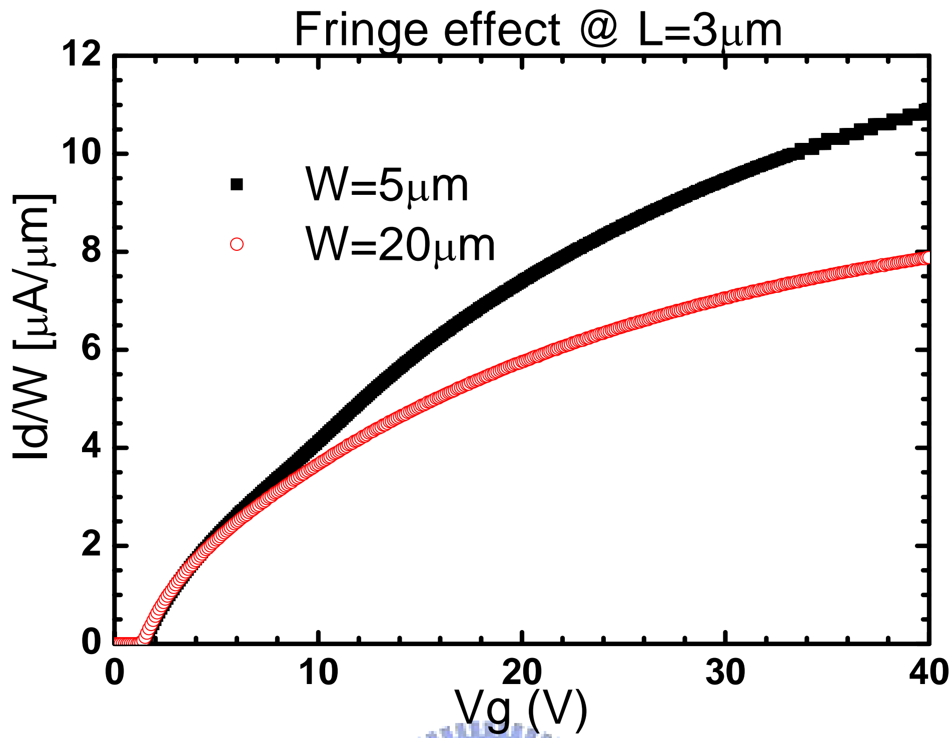


Fig. 2.4 Measured normalized Id (by width)-Vg of NLDMOS.

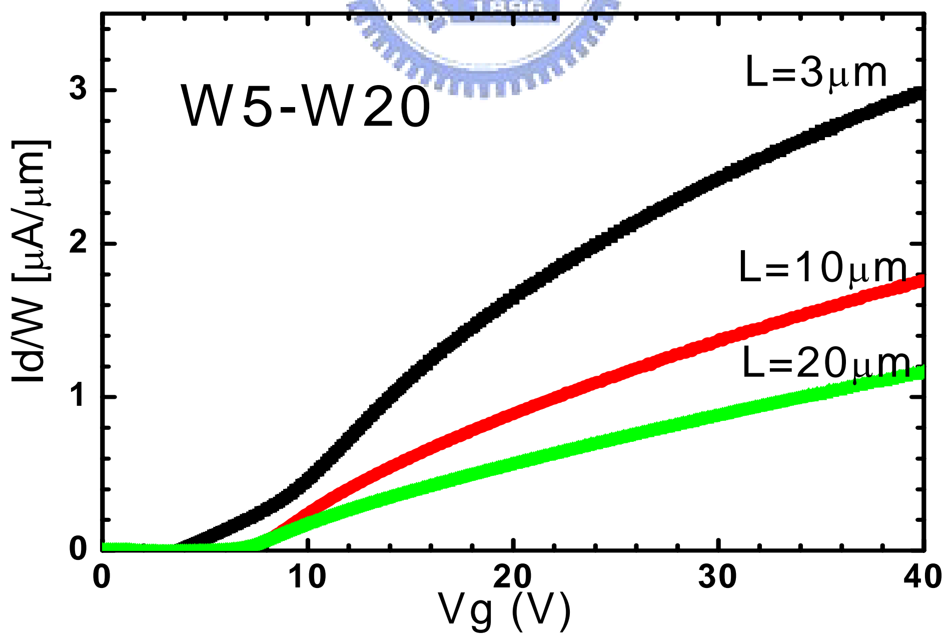


Fig. 2.5 ΔI of measured normalized Id (by W=5 μm) subtracting Normalized Id (by W= 20 μm)-Vg of NLDMOS

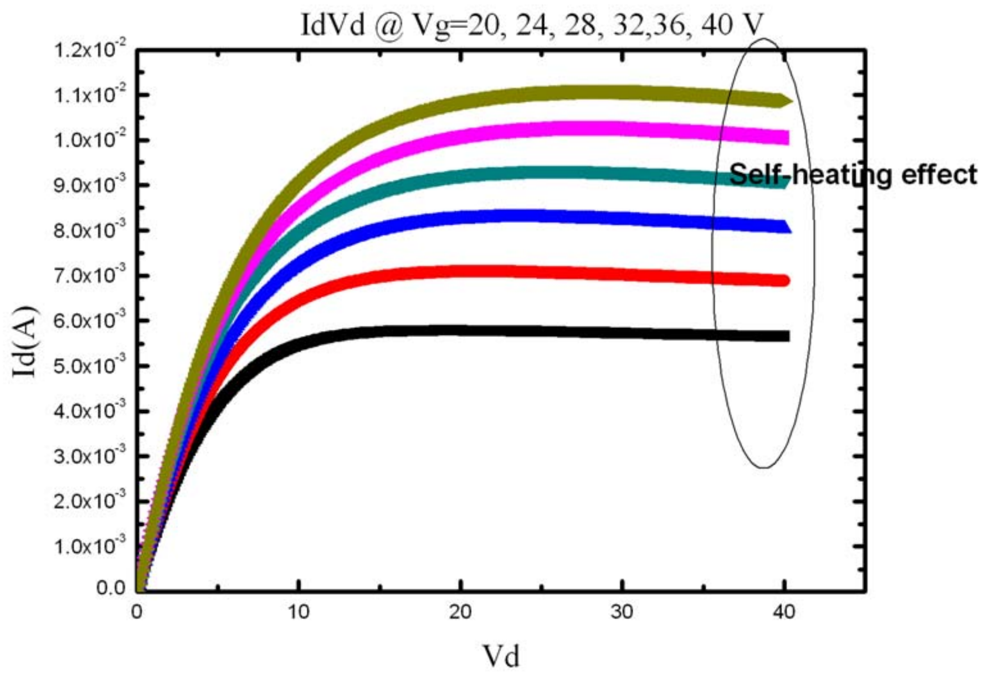


Fig. 2.6 Measured I-V characteristics of NLDMOS (W=3 μm, L=20 μm)with self-heating effect.

Chapter 3
Spice Model of LDMOS

3.1 Introduction

An overall spice model extraction flow of LDMOS is illustrated step by step in this chapter. Our strategy shown in Fig. 3.1 considers the characteristics of quasi-saturation effect, the fringe effect and the self-heating effect and models LDMOS transistors by sub-circuit method depicted in Fig. 3.2. First, we take account of the fringe effect and separate drain currents into pure LDMOS drain currents (Id) and fringe MOS drain currents (If), thus we can model these two MOS currents respectively and solve the “two stage turning on effect”. Then, a LDMOS without influence of the fringe effect is modeled by a MOSFET model and a bias-dependent series resistance described by an analytic expression to represent the characteristic of I-V data in a LDMOS. This approach is called “two stages model” because it uses the characteristic of a LDMOS with different performances in the low-Vg stage and the high-Vg stage to form an accurate model. Finally, we improve the simulation result of two stages model by correcting function of self-heating effect.

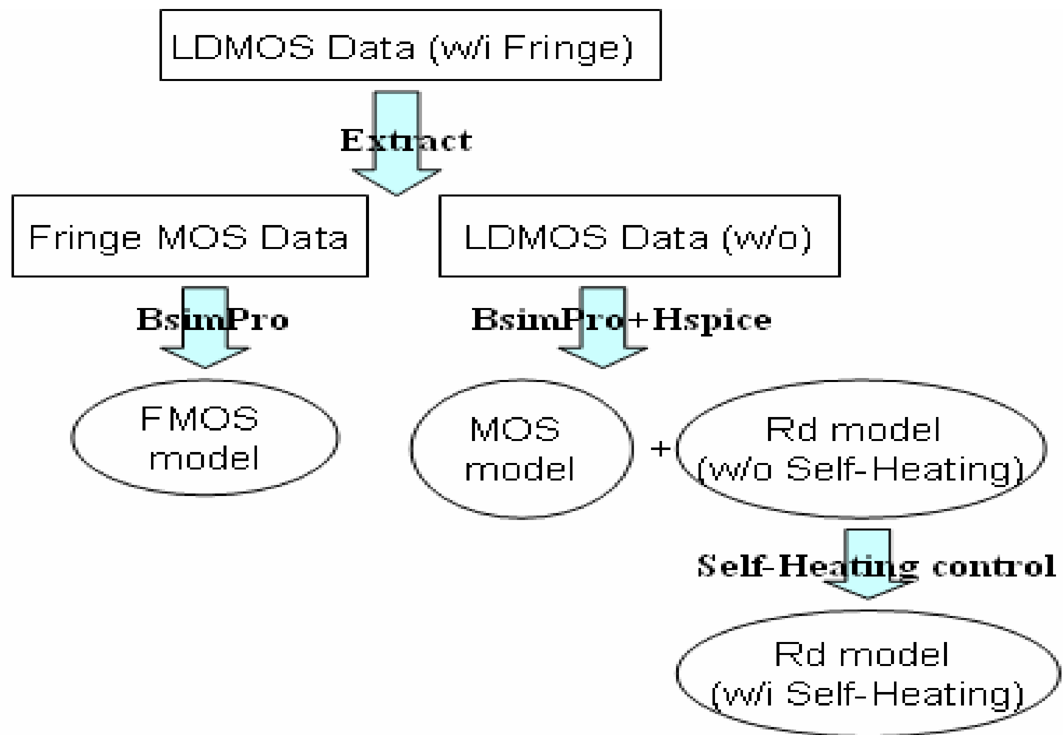


Fig. 3.1 Spice Macro Model Extraction Flow.

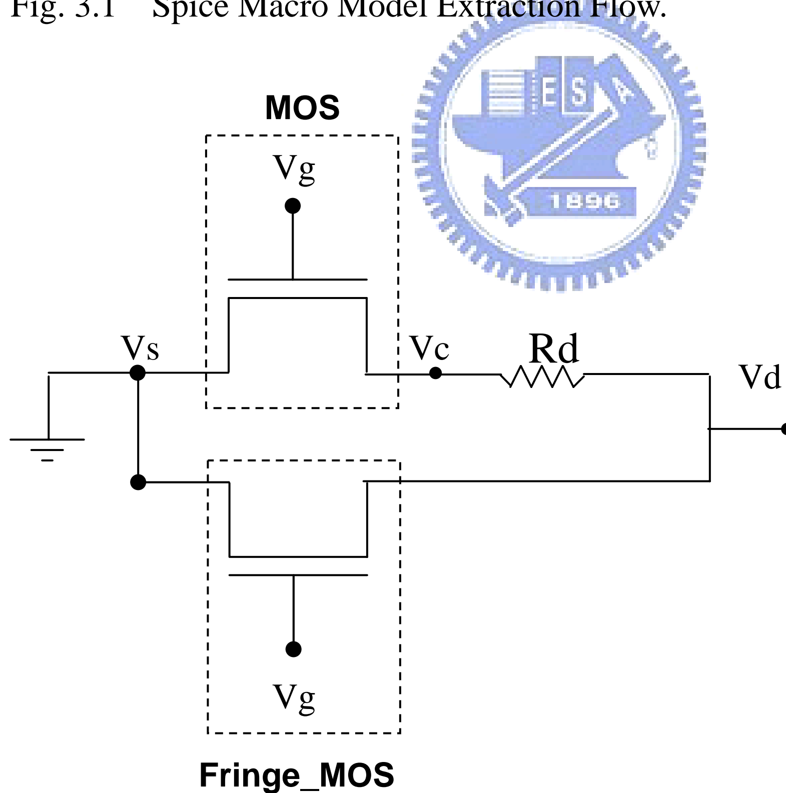


Fig.3.2 Illustration of sub-circuit model concept.

3.2 Two Stages Model

3.2.1 Motivation and Extraction Flow of Two Stages Model

The traditional built-in MOSFET models in BSIM3v3 are not capable of simulating some features of power MOSFET, such as drain-gate capacitance, body-drain diode, pinch effect between cells, and quasi-saturation effect, which are essential to the determination of the device response. Thus a key bottleneck for the modeling of LDMOS devices is the non –linear bias-dependence drift resistance dependent on drain and gate voltages, Rd(Vd,Vg) combining with the existing built-in model.

To obtain an accurate model, the concept of "two stages model" is used. We find that a LDMOS with different performances in a high-Vg stage and a low-Vg stage. I-V curve of a LDMOS shown in Fig. 3.3 can be separated into two stages. First, in a low-Vg stage region, I-V data in a LDMOS is like I-V data in a MOSFET, so it can be simulated by using a built-in MOSFET in BSIM3v3. We prove this assumption by a MESDRIFT device which is a device with K-point—an N+ implant under gate extension region, located in the boundary between the channel region and the drift region depicted in Fig. 3.4; in another word, a MESDRFT is also a LDMOS but has a K-point additionally. By sensing the voltage of the K-point—Vk, we can observe the characteristics of the intrinsic MOS data in a MESDRIFT device [7]. The Vk is used to distinguish between the operation on the intrinsic MOS and the resistance. The comparison between a KPC device and a LDMOS device is shown in Fig. 3.5 and a LDMOS is matched perfectly with a KPC device in a low-Vg stage region. Secondly, in a high-Vg stage, the I-V characteristic of a LDMOS is not equal to I-V curve in a MOSFET and the drain currents in the saturation region are reduced because of the quasi-saturation effect. In other words, power devices operating in high voltage are controlled by the bias-dependence drift resistance mainly and have the I-V

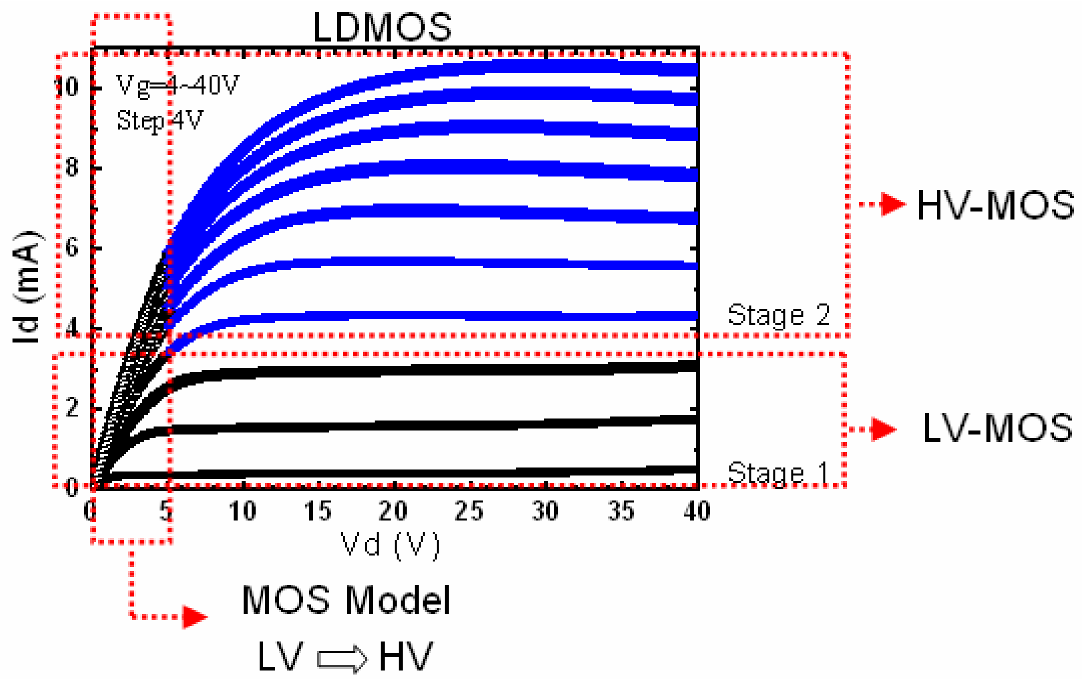


Fig. 3.3 Measured Id-Vd curve of a LDMOS illustrates concepts of two stages.

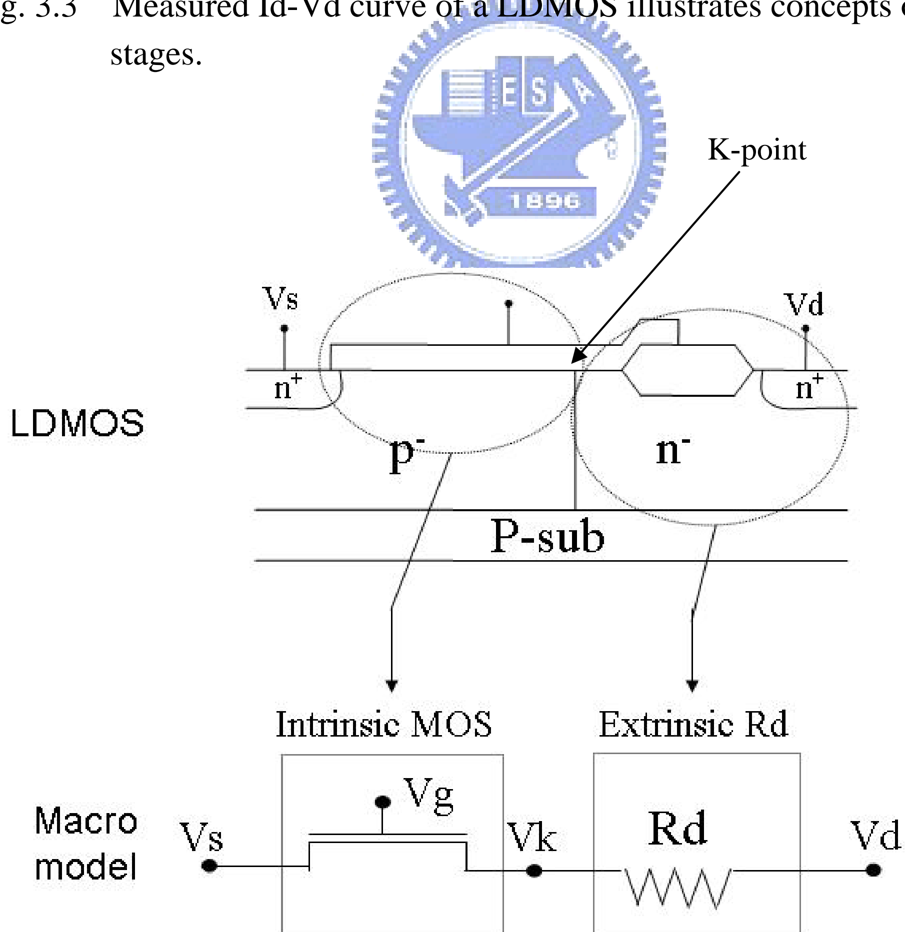


Fig. 3.4 Schematic cross section of LDMOS which is with K contact.

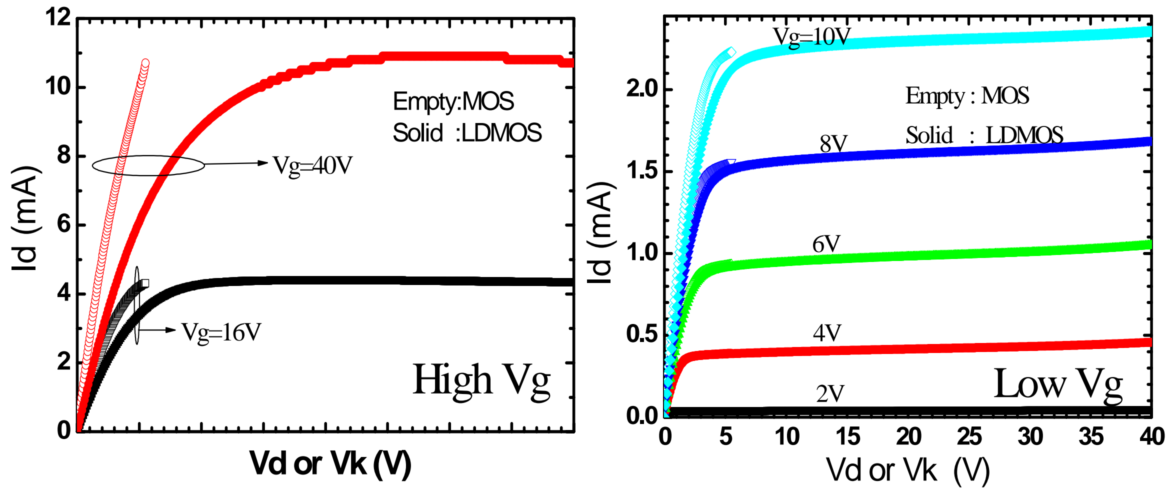


Fig. 3.5 I-V comparison between MOS and LDMOS devices.

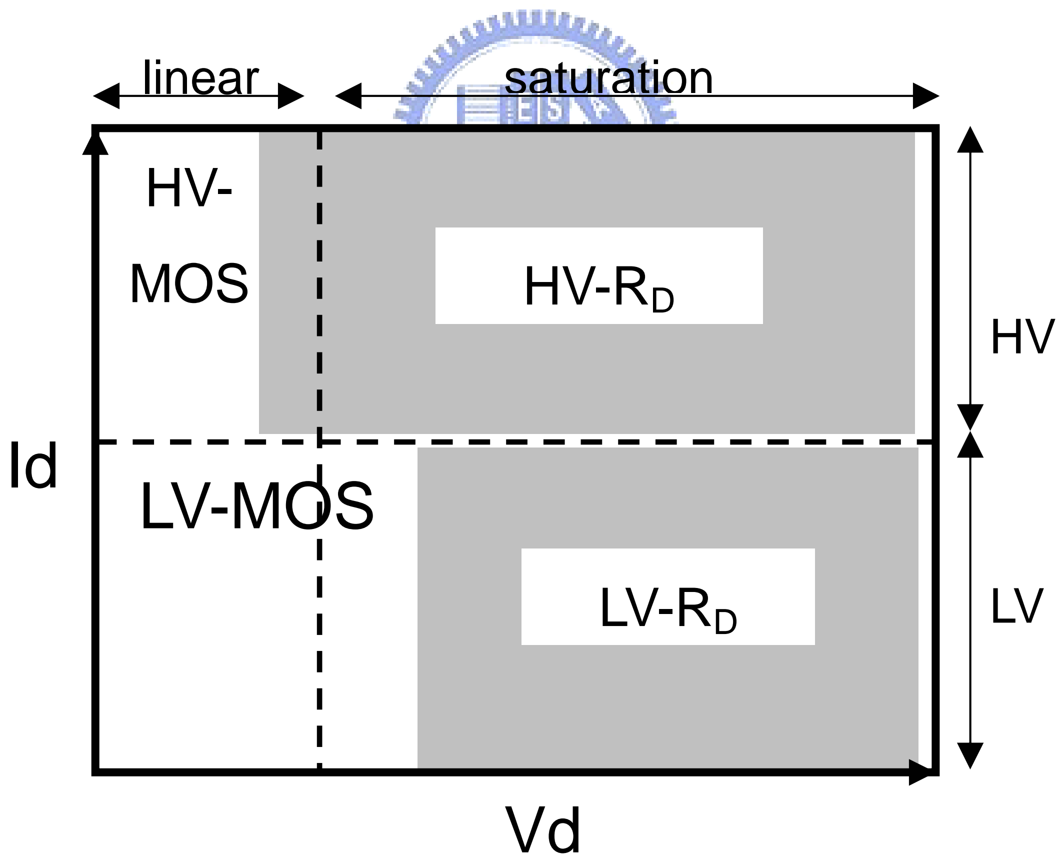


Fig. 3.6 Illustration of different controlling components in HV and LV stages.

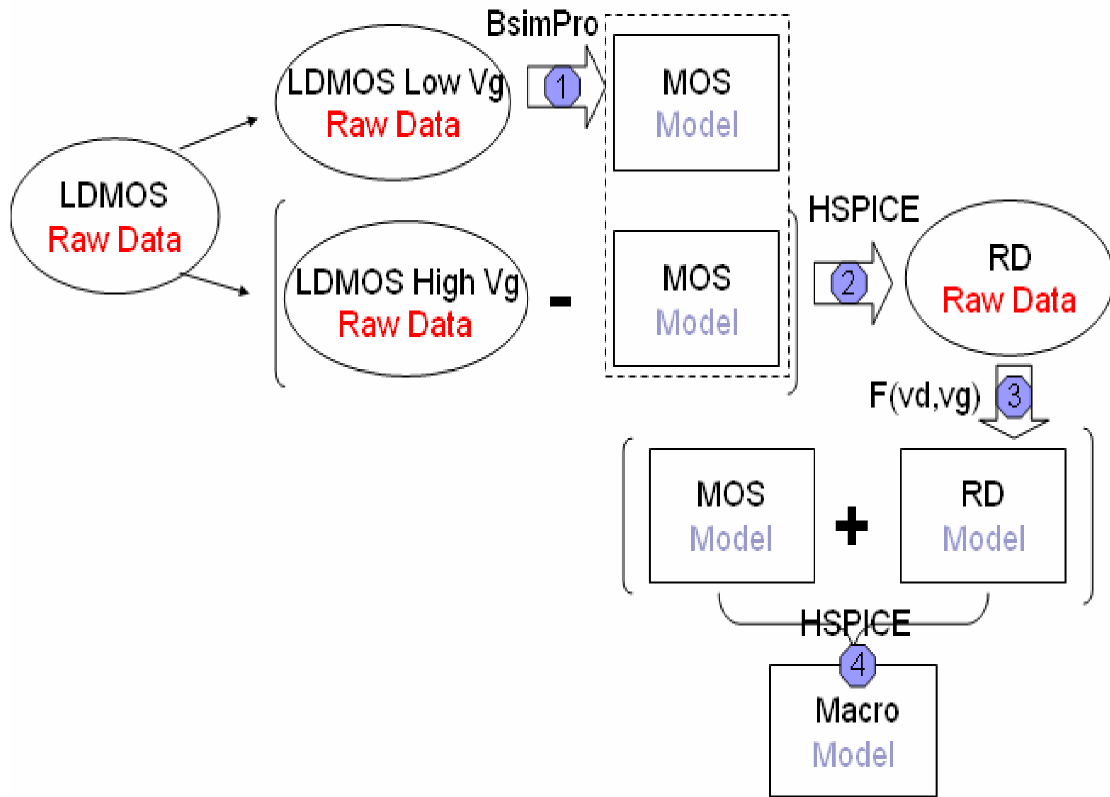


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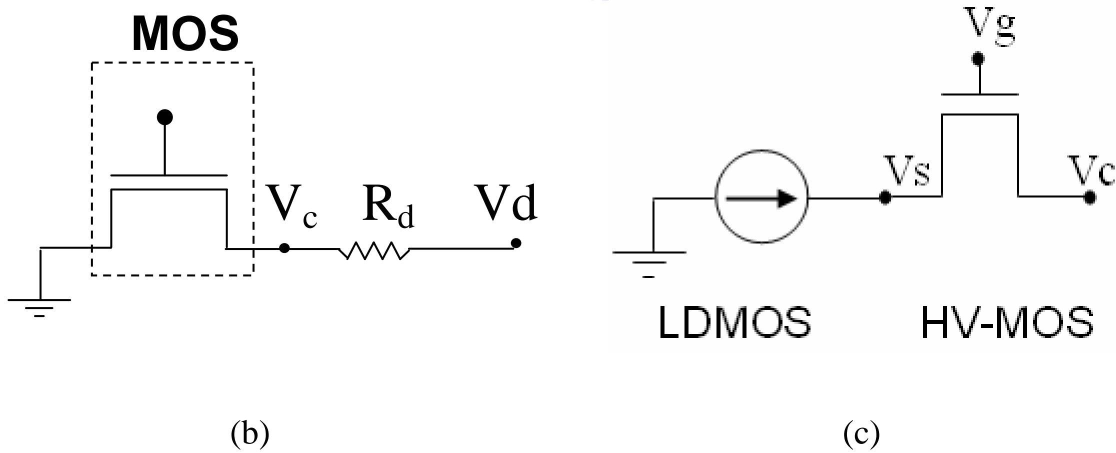
Fig. 3.7(a) Macro model extraction flow.



(b) (c)

Fig. 3.7 (b)Illustration of sub-circuit model concept.(c)Illustration of method of reverse calculate Rd.

Characteristic like a MOSFET in a low-voltage stage region. It is illustrated in Fig. 3.6.

By executing this concept, our extraction flow and sub-circuit picture are depicted in Fig. 3.7(a) and Fig. 3.7(b). There are four main steps as follows.

The first step is extracted the MOS model from the measured data of a LDMOS in low-Vg stage. For extracting the MOS model, according to BSIM manual, the following device data must be measured: (1)Id vs. Vg at Vd=0.1V(in linear region); (2)Id vs. Vd at different low gate voltages. Except fitting these data, we also need to check the measured Id vs Vg at Vd=35.2 V (in the saturation region). The data in low-Vg stage region must be fit accurately because the MOS model is extracted from a low-Vg stage region. In addition, the simulated data in high-Vg stage region must be higher than the measured data because this low-Vg MOS model is without considering the quasi-saturation effect. With these data, we can find out an intrinsic low-Vg MOS model by using BSIMPro software.

The second step is to calculate drift resistance with following equation:

$$Rd = \frac{Vd - Vc}{Id} \tag{3.1}$$

The idea picture is shown in Fig. 3.7(c). Once we get intrinsic low-Vg MOS model from LDMOS low-Vg stage measurement, we can use LDMOS I-V to calculate Rd and Vc data in high-Vg stage region. The low-Vg stage region and high-Vg stage region can use the same low-Vg MOS model in linear region because the I-V characteristic in a high-Vg region operating at linear region still perform like I-V data in a MOS. Here Vc presents a virtual point that is a voltage of the drain side in an intrinsic MOS which is one part of a LDMOS.

Thirdly, the most important part is to derive the Rd model precisely. We extract Rd model by fitting calculated Vc and the fitting functions are as followed:

$$V_c = V_{csat} \cdot \tanh(\frac{slope \cdot V_d}{V_{csat}}) \tag{3.2}$$

$$V_{csat} = (V_g - V_t) - \sqrt{(V_g - V_t)^2 - 2 \cdot \frac{(V_g - V_t - \frac{V_{dsat}}{2}) \cdot V_{dsat}}{1 + \theta_{vs} \cdot (V_g - V_t)^n}} \tag{3.3}$$

$$V_{dsat} = \frac{(V_g - V_t)}{1 + \theta_{dsat} \cdot (V_g - V_t)} \tag{3.4}$$

Deriving concepts and details will be illustrated in section 3.2.2.

Finally, we combine the MOS model with the Rd model to get a macro model which can describe I-V data of a LDMOS not only in low-Vg stage but also in high-Vg stage accurately. The final results will be shown in section 3.2.3 and 3.2.3.

3.2.2 Physical Concepts of Two Stages Model

The method of fitting calculated Vc is based on the concept of two stages model that is shown in Fig. 3.8. In Fig. 3.8, the Id-Vd curve of a LDMOS biasing at high-Vg stage needs to be modeled by calculating Vcsat of the intrinsic MOS part with the drain currents of the LDMOS biasing at Vdsat. It is different from the traditional way of changing mobility to obtain the reduction of drain currents because of the quasi-saturation effect. Vc can be solved as follows. First of all, according to the calculated Vc data in Fig. 3.9, we can find the relationship between Vc and Vd. The relation can be expressed by the equation (3.2) and the slope term in equation (3.2) is defined as the slopes of Vc versus Vd curves in linear region. The value of slope is close to unity. Then the Vcsat can be calculated in the way of assuming drain currents of a LDMOS equal to the drain currents of an intrinsic MOS which is embedded in the same LDMOS. The Vcsat equation can be derived as follows:

$$I_d(V_g, V_{csat}) = I_d(V_g, V_{dsat})$$

$$\Rightarrow \frac{W}{L}\cdot C_{ox}\cdot \mu_o \cdot (V_g - V_t - \frac{V_{csat}}{2})\cdot V_{csat} = \frac{W}{L}\cdot C_{ox}\cdot \underbrace{\frac{\mu_o}{1+\theta_{vs}\cdot (V_g - V_t)^n}}_{\text{Concept 2and 3}} \cdot \{V_g - V_t - \frac{1}{2}\cdot \underbrace{V_{dsat}\}\cdot V_{dsat}}_{\text{Concept 1}} \quad (3.5)$$

$$\Rightarrow V_{csat} = (V_g - V_t) - \sqrt{(V_g - V_t)^2 - 2\cdot \frac{(V_g - V_t - \frac{V_{dsat}}{2})\cdot V_{dsat}}{1+\theta_{vs}\cdot (V_g - V_t)^n}} \quad (3.6)$$

The Vcsat has three important physical concepts illustrated in Table. 3.1. Three concepts tell why a traditional built-in MOSFET model can't fit a LDMOS well. The first concept is the early saturation illustrated in Fig. 3.10(a). We use the parameter θ_{dsat} to describe the shift of the saturation voltage and extract it from Id-Vd curve. In a LDMOS, the saturation effect happens earlier than it of a MOSFET. The second is the drain resistance existing in a LDMOS and depicted in Fig. 3.10(b). The larger parameter n presents the larger drain resistance. The final concept is the velocity saturation represented by parameter θ_{vs}. The velocity saturation happens in the drift region and can be shown in Fig. 3.10(c). The drain current doesn't increase as fast with Vg as it in a MOSFET. The parameters n and θ_{vs} can be extracted from calculated Vc versus Vg. The coupling of drain resistance and velocity saturation phenomenon is the cause of early saturation.

However, in the extraction methodology, first of all, we calculate the parameter V_t by Gm max. method. Then extract θ_{dsat} first from the IdVd curve like Fig. 3.10(a) and keep it global in different sizes of devices. Finally, we determine n and θ_{vs} from Vc-Vg curve and find that devices with the same width have the same parameter n. Thus we call parameter n is a semi-global parameter, and the parameter θ_{vs} is a binning parameter which can be adjusted with different sizes of devices.

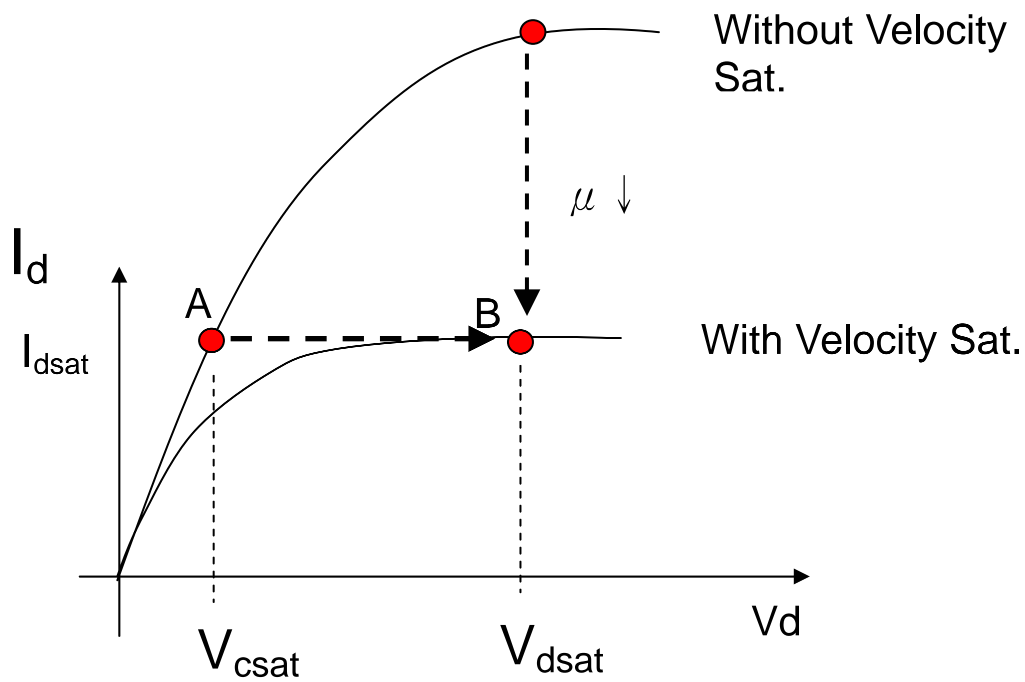


Fig.3.8 Illustration of different ways of modeling I-V characteristics of LDMOS.

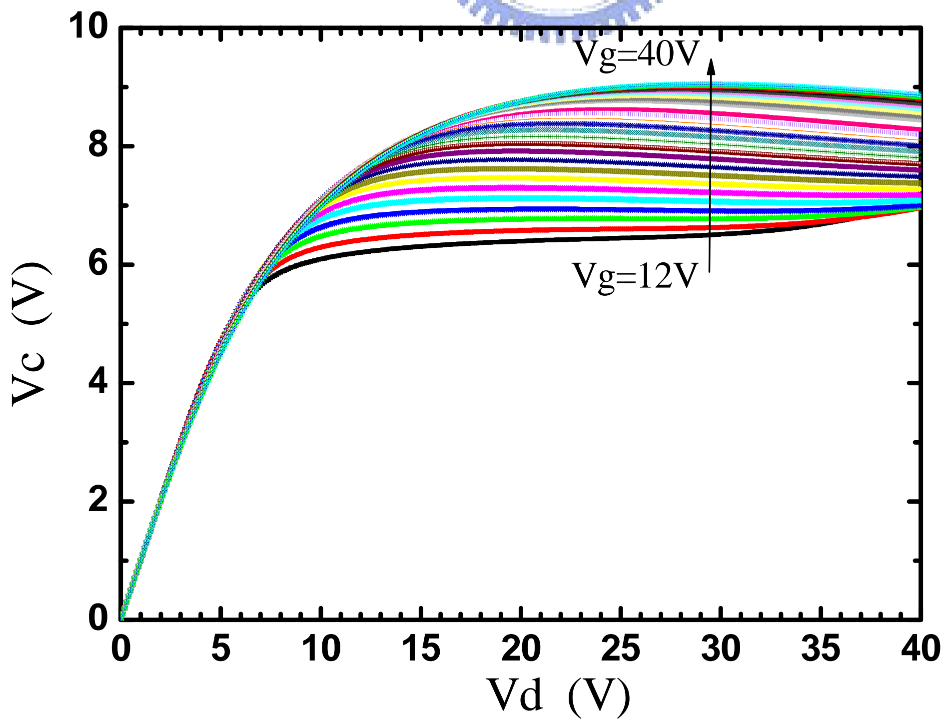


Fig.3.9 Vc-Vd curve of LDMOS.

Table. 3.1 Three physical concepts of Vcsat.

	Concept& Extracting order	Presenting Parameter	character	Equation
1	Early Saturation	θ_{dsat}	global	$V_{dsat}=\frac{(V_g-V_t)}{1+\theta_{dsat}\cdot(V_g-V_t)}$
2	Drain resistance	n	Various with L	$\mu=\frac{\mu_0}{1+\theta_{vs}\cdot(V_g-V_t)^n}$
3	Velocity Saturation	θ_{vs}	binning	$\mu=\frac{\mu_0}{1+\theta_{vs}\cdot(V_g-V_t)^n}$

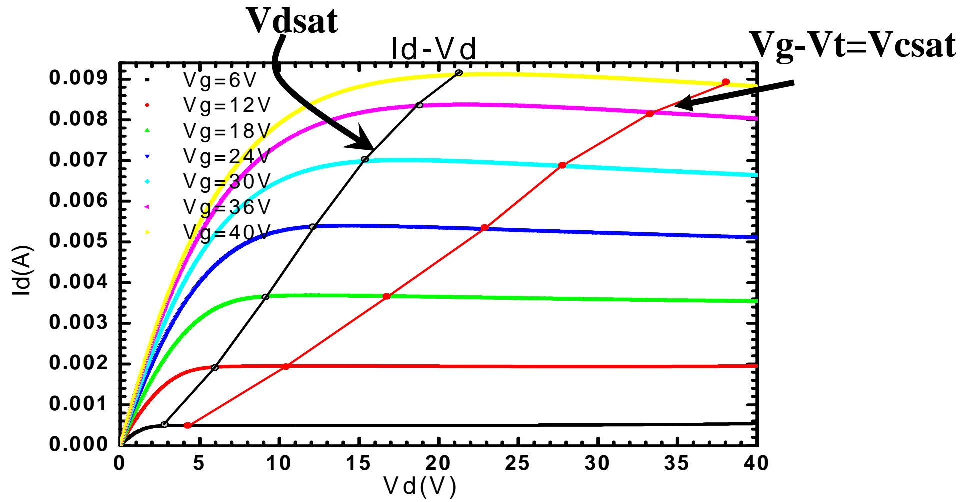


Fig. 3.10(a) Illustration of the concept of early saturation.

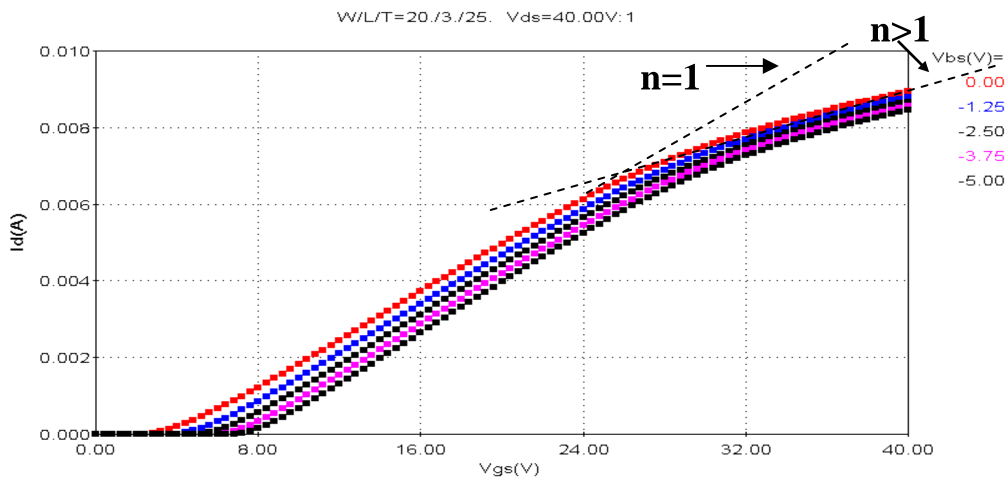


Fig. 3.10(b) Illustration of the concept of drain resistance.

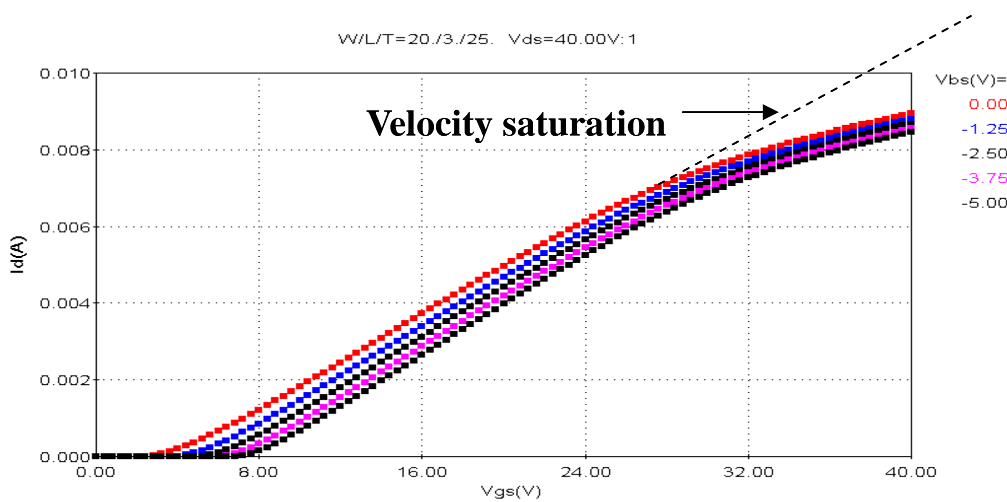


Fig. 3.10(c) Illustration of the concept of velocity saturation.

3.2.3 Single size Modeling Result

First, we would show the simulation results of LDMOS with big and small sizes (W=20 μm/L=20 μm & W=3 μm/L=3 μm) in Fig. 3.11 and Fig. 3.12 under normal operation (Temperature=25°C, Vb=0V). We can see the fitting result is good in the linear region and the simulated drain currents in the saturation region are deducted successfully and precisely by adding Rd model. Second, the simulation results of devices operated at Vb=-4V and Vb=0V are shown in Fig. 3.13. The results are still good at Vb=-4V so our model is suitable for different bulk voltages. Finally, the operation environment temperature is also considered. Idsat vs. T is shown in Fig. 3.14 and the higher temperature causes less saturation current.

The MOS model and Rd model include Vg, Vd, Vb, T dependence in a single size macro model. There are some parameters that can describe adjustment of Vb and temperature in a MOS model and be extracted with BSIMPro software. Besides, Rd model has four crucial parameters (V_t, θ_{dsat}, θ_{vs}, n) which have Vg, Vd, Vb and T dependence. These dependences relate to parameters and are summarized in Table. 3.2. We extract parameters V_t and θ_{vs} by linear functions with Vb=0, -4V and T=25,125°C. So results in Fig. 3.14 are not perfect matched at T=-40°C. But the error is bearable.

Table. 3.2 Modeling dependence related to parameters.

Dependence	Equation	Related Parameter
Vd	$V_c = V_{csat} \cdot \tanh(\frac{V_d}{V_{csat}})$	Vcsat
Vg	$V_{csat} = (V_g - V_t) - \sqrt{(V_g - V_t)^2 - 2 \cdot \frac{(V_g - V_t - \frac{V_{dsat}}{2}) \cdot V_{dsat}}{1 + \theta_{vs} \cdot (V_g - V_t)^n}}$	n, $\theta_{dsat}, \theta_{vs}, V_t$
Vb	$Vt(Vb,T) = Vt_{slope}(T) \cdot Vb + Vt_{offset}(T)$ $\theta vs(Vb,T) = \theta vs_{slope}(T) \cdot Vb + \theta vs_{offset}(T)$	Vt_{slope}, Vt_{offset} $\theta vs_{slope}, \theta vs_{offset}$
T	$Vt_{slope}(T) = Vt_{slope2} \cdot T + Vt_{slope1}$ $Vt_{offset}(T) = Vt_{offset2} \cdot T + Vt_{offset1}$ $\theta vs_{slope}(T) = \theta vs_{slope2} \cdot T + \theta vs_{slope1}$ $\theta vs_{offset}(T) = \theta vs_{offset2} \cdot T + \theta vs_{offset1}$	Vt_{slope1}, Vt_{slope2} $Vt_{offset1}, Vt_{offset2}$ $\theta vs_{slope1}, \theta vs_{slope2}$ $\theta vs_{offset1}, \theta vs_{offset2}$

3.2.4 Universal Modeling Result

The diagram of the whole sizes of LDMOS devices is shown in Fig.3.15. We want to extract a universal macro model so bin the MOS models and the Rd models of these four sizes respectively. The strategy is shown clearly in Fig. 3.16. By using BSIMPro software, a universal MOS model can be generated by binning four corner sizes MOS models. However, the extraction of a universal Rd model is more complicated. There are four parameters needed to be concerned. θ_{dsat} is a global parameter so is the same in every size of device. The parameter n is semi-global parameter so we bin two parameter n in two different lengths by the following equation:

$$n = n_1 + \frac{n_2}{L} \tag{3.7}$$

A universal parameter V_t formula and a universal parameter θ_{vs} function can be derived from four V_t and θ_{vs} of corner size models, expressed as follows:

$$Vt(Vb,T,L,W) = Vt_{slope}(T,L,W)\cdot Vb + Vt_{offset}(T,L,W)$$

$$Vt_{slope} = Vt_{slope2}(L,w)\cdot T + Vt_{slope1}(L,w)$$

$$Vt_{offset} = Vt_{offset2}(L,w)\cdot T + Vt_{offset1}(L,w)$$

$$Vt_{slope1}(L,w) = Vt_{slopeA} + \frac{Vt_{slopeB}}{l1n} + \frac{Vt_{slopeC}}{W1n} + \frac{Vt_{slopeD}}{l1n \cdot W1n}$$

$$Vt_{slope2}(L,w) = Vt_{slopeE} + \frac{Vt_{slopeF}}{l1n} + \frac{Vt_{slopeG}}{W1n} + \frac{Vt_{slopeH}}{l1n \cdot W1n}$$

$$Vt_{offset1}(L,w) = Vt_{offsetA} + \frac{Vt_{offsetB}}{l1n} + \frac{Vt_{offsetC}}{W1n} + \frac{Vt_{offsetD}}{l1n \cdot W1n}$$

$$Vt_{offset2}(L,w) = Vt_{offsetE} + \frac{Vt_{offsetF}}{l1n} + \frac{Vt_{offsetG}}{W1n} + \frac{Vt_{offsetH}}{l1n \cdot W1n}$$

$$\theta vs(Vb,T,L,W) = \theta vs_{slope}(T,L,W)\cdot Vb + \theta vs_{offset}(T,L,W)$$

$$\theta vs_{offset} = \theta vs_{offset2}(L,w)\cdot T + \theta vs_{offset1}(L,w)$$

$$\theta vs_{slope} = \theta vs_{slope2}(L,w)\cdot T + \theta vs_{slope1}(L,w)$$

$$\theta vs_{slope1}(L,w) = \theta vs_{slopeA} + \frac{\theta vs_{slopeB}}{l1n} + \frac{\theta vs_{slopeC}}{W1n} + \frac{\theta vs_{slopeD}}{l1n \bullet W1n}$$

$$\theta vs_{slope2}(L,w) = \theta vs_{slopeE} + \frac{\theta vs_{slopeF}}{l1n} + \frac{\theta vs_{slopeG}}{W1n} + \frac{\theta vs_{slopeH}}{l1n \bullet W1n}$$

$$\theta vs_{offset1}(L,w) = \theta vs_{offsetA} + \frac{\theta vs_{offsetB}}{l1n} + \frac{\theta vs_{offsetC}}{W1n} + \frac{\theta vs_{offsetD}}{l1n \bullet W1n}$$

$$\theta vs_{offset2}(L,w) = \theta vs_{offsetE} + \frac{\theta vs_{offsetF}}{l1n} + \frac{\theta vs_{offsetG}}{W1n} + \frac{\theta vs_{offsetH}}{l1n \bullet W1n}$$

In chapter3.2.3, we just consider a single size model with temperature and bulk bias dependence related to parameter Vt and θ_{vs}. Now as shown above, length and width dependence is also taken account.

Finally, we combine a universal MOS model and a universal Rd model to generate a universal macro model for every size and different conditions of LDMOS. Certainly, to examine the validity of this universal macro model is needed, so we simulate data of a device with a central size of W/L= 3 μm/5 μm shown in Fig. 3.17. The measured and simulated data still match with each other precisely. We also check the data of Idsat versus length and Idsat versus temperature shown in Fig. 3.18. and Fig.3.19. We can see that the device with longer length has lower drain currents and high temperature causes currents decrease. These results follow a basic physical theory. Therefore we can say faithfully that we have obtained a universal macro model for different sizes and operation conditions successfully.

3.3 Fringe Effect Model of LDMOS

The fringe effect has influence on our LDMOS devices because of the side effect which generate extra fringe currents. Our modeling strategy is to extract fringe currents (If) from LDMOS before applying sub-circuit modeling method and model them as a fringe MOS. The schematic picture is depicted in Fig.3.20. First, two LDMOS devices with the same length but different widths (W1&W2) are needed. Their normalized drain currents by width can be expressed as follows:

$$\frac{I_{tot}|_{W_1}}{W_1} = \frac{I_D(W_1)}{W_1} + \frac{I_f}{W_1} \tag{3.10}$$

$$\frac{I_{tot}|_{W_2}}{W_2} = \frac{I_D(W_2)}{W_2} + \frac{I_f}{W_2} \tag{3.11}$$

Then, we assume that If which go through these two devices are the same and the normalized drain currents by W1 & W2 are equal too. Thus, If can be solved by the following equation:

$$\frac{I_D(W_1)}{W_1} = \frac{I_D(W_2)}{W_2} \Rightarrow I_f = \frac{W_2 \cdot (I_{tot}|_{W_1}) - W_1 \cdot (I_{tot}|_{W_2})}{(W_2 - W_1)} \tag{3.12}$$

If versus Vg curve is shown in Fig. 3.21. We can see that If-Vg characteristic is similar to the performance of a MOSFET. So we can use two MOS in parallel to model the fringe effect shown in Fig. 3.2. Fig.3.22 shows the comparison between measured data and simulation results.

3.4 Self-Heating Effect Model of LDMOS

The self-heating effect leads to a decrease in current levels of the device and negative output conductance effect. We use the equation to describe the reduction of drain current operating at high voltage [24]. The electrical and thermal couple effect is taken into consideration. The equation is as follows:

$$I_{dsat} \propto \frac{I_{dsat0}}{1+\theta_{sh}\cdot e^{f(T)}} \quad \Longleftrightarrow^{\text{ETC}} \quad f(V_d)=\beta\cdot(V_d - V_{dsat})$$

The illustration is shown in Fig. 3.23. Higher drain voltage causes more decrease in currents because of the self-heating effect. Fig. 3.24 shows the simulation results compared by measured data.

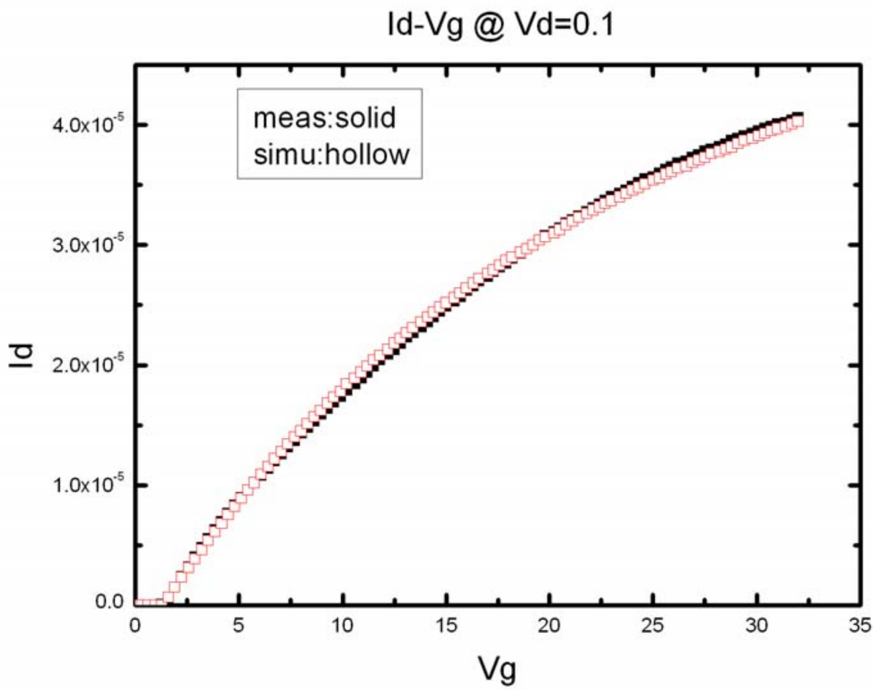


Fig. 3.11(a) Comparison between measured and simulated Id-Vg (in linear region) curve. (W/L=20/20 μm)

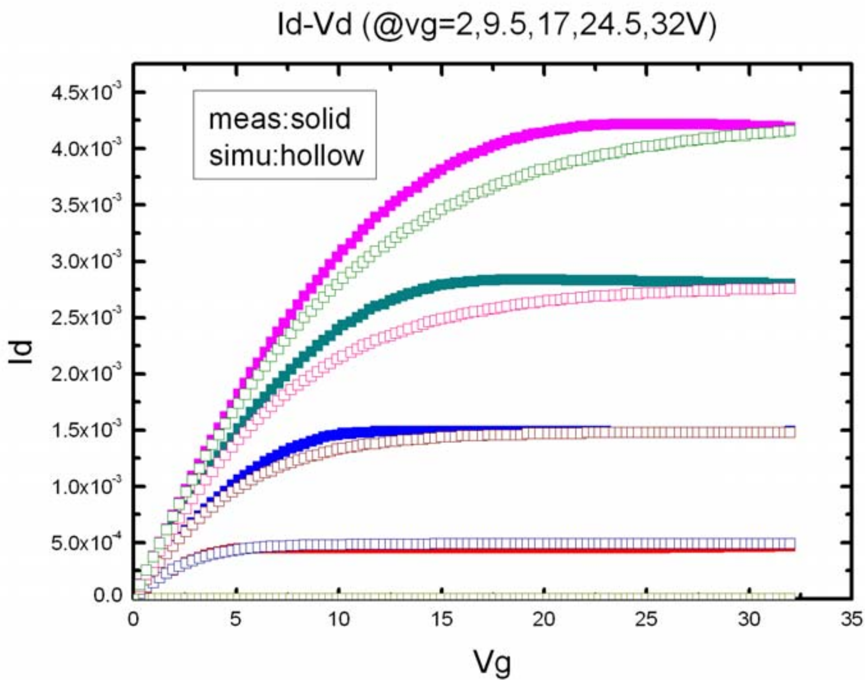


Fig. 3.11(b) Comparison between measured and simulated Id-Vd curve. (W/L=20/20 μm)

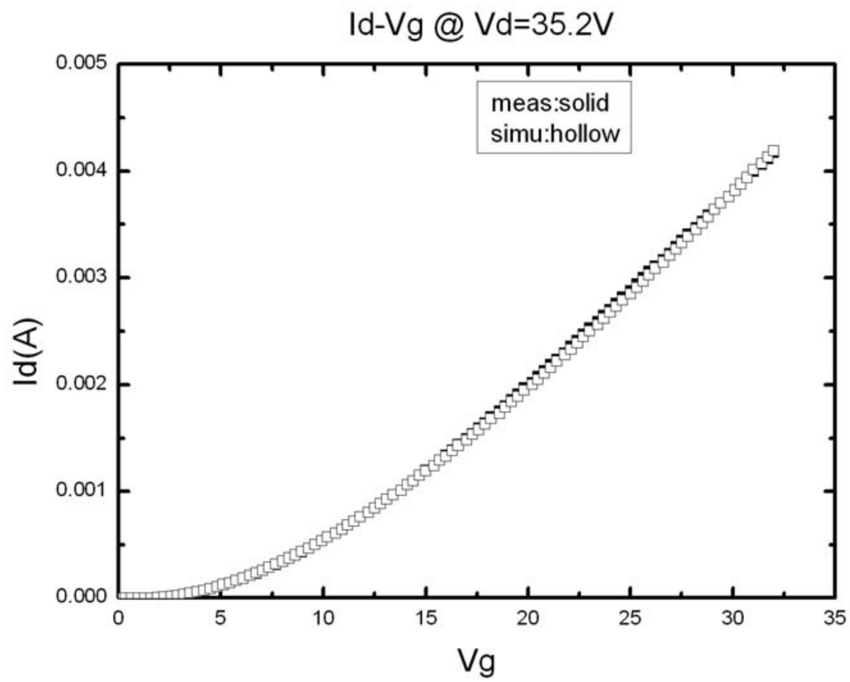
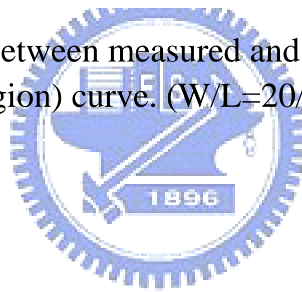
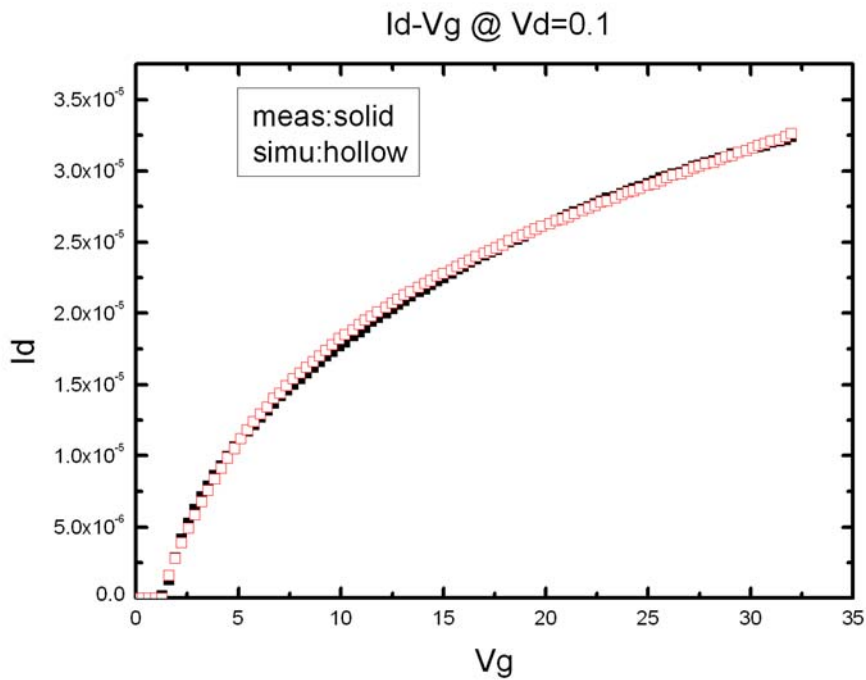
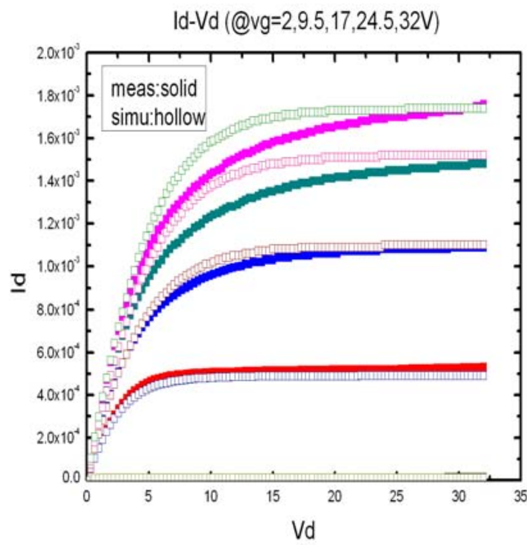


Fig. 3.11(c) Comparison between measured and simulated Id-Vg (in saturation region) curve. (W/L=20/20 μm)







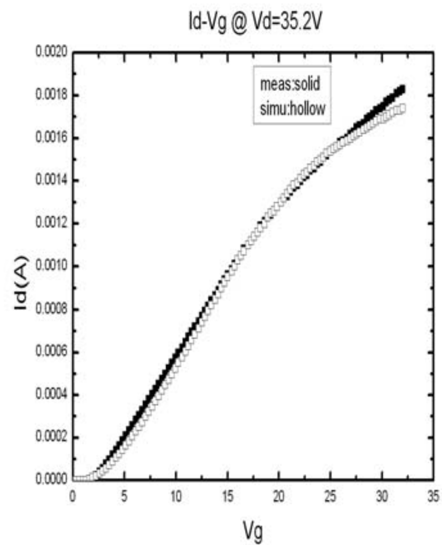


Fig. 3.12 Comparison between measured and simulated I-V data. (W/L=3/1.7 μm)

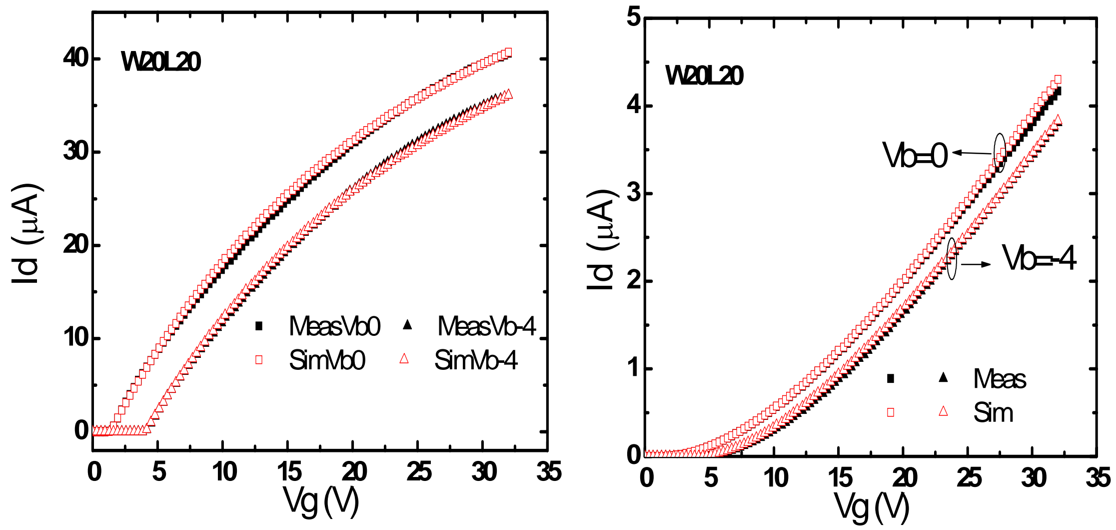


Fig. 3.13(a) Comparison between simulated and measured Idlin-Vg & Idsat-Vg. (W=20 μm/L=20 μm)

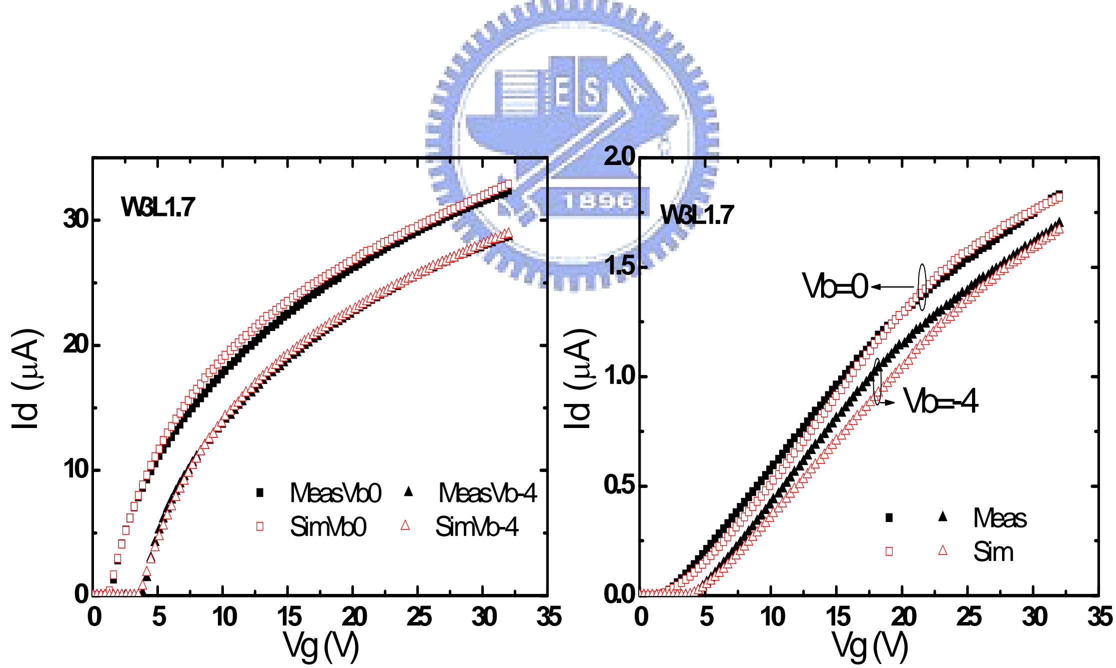


Fig. 3.13(b) Comparison between simulated and measured Idlin-Vg & Idsat-Vg.(W=3 μm/L=1.7 μm)

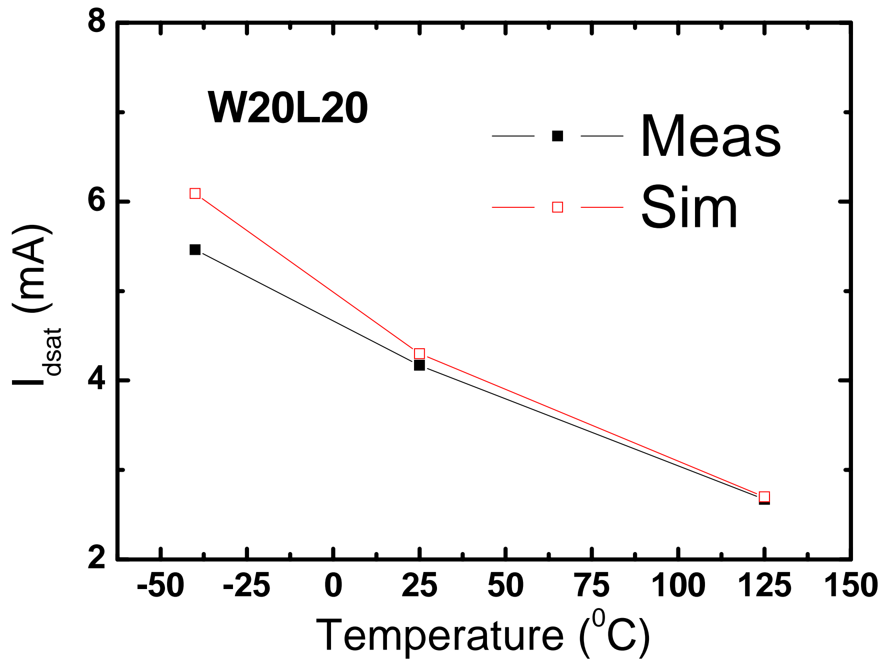


Fig. 3.14(a) Comparison between simulated and measured Idsat-T.
(W=20 μm/L=20 μm)

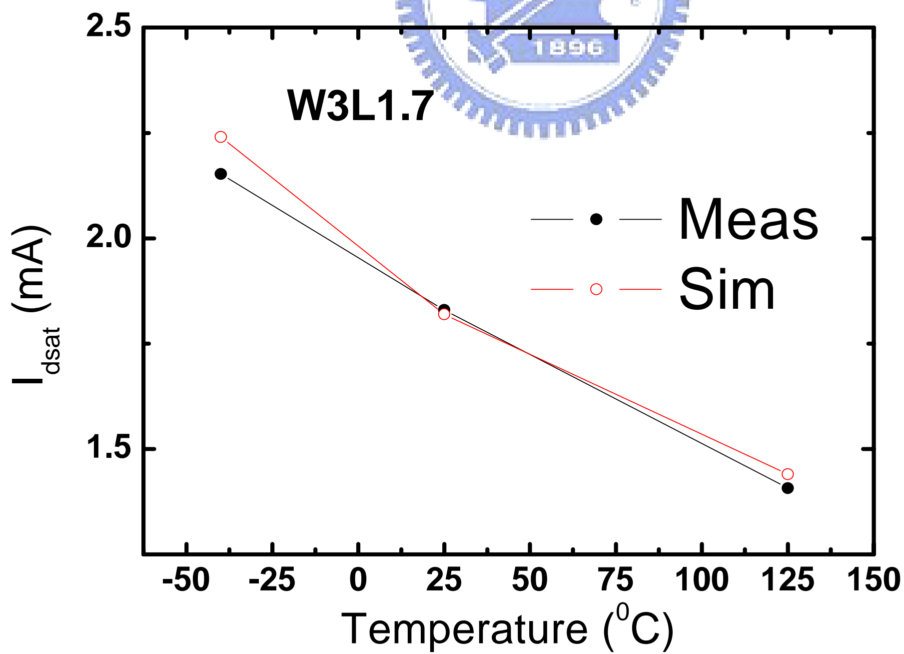


Fig. 3.14(b) Comparison between simulated and measured Idsat-T.
(W=3 μm/L=1.7 μm)

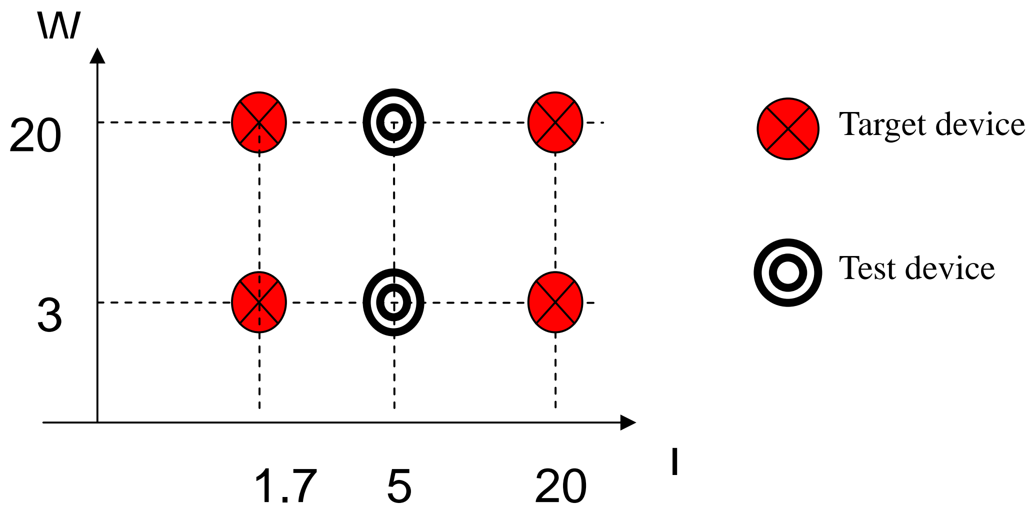


Fig. 3.15 The diagram of whole sizes of LDMOS devices in our work.

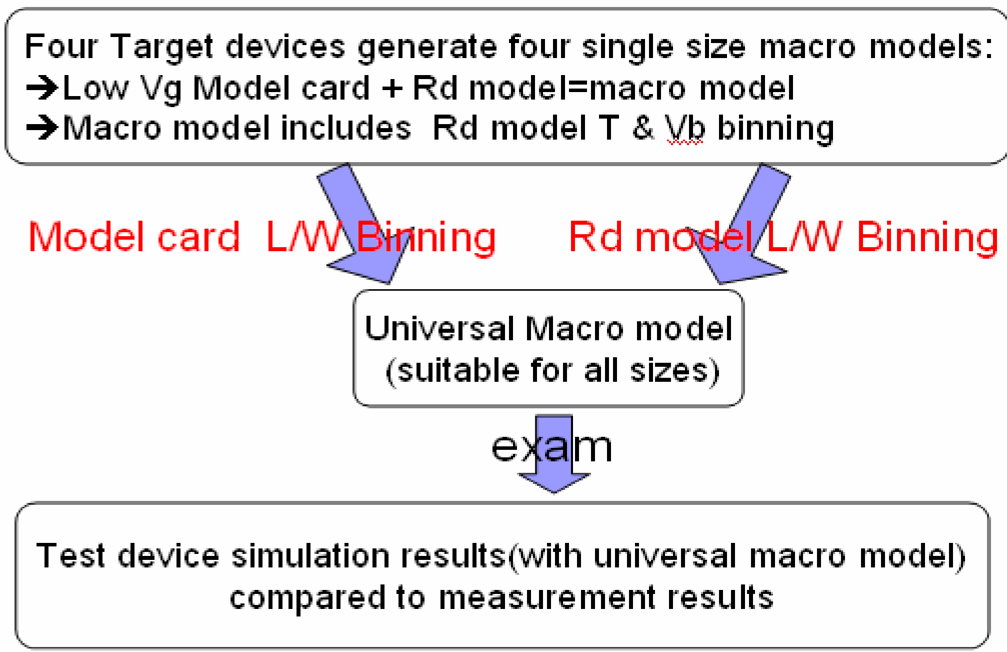


Fig. 3.16 Binning strategy of a universal macro model of LDMOS.

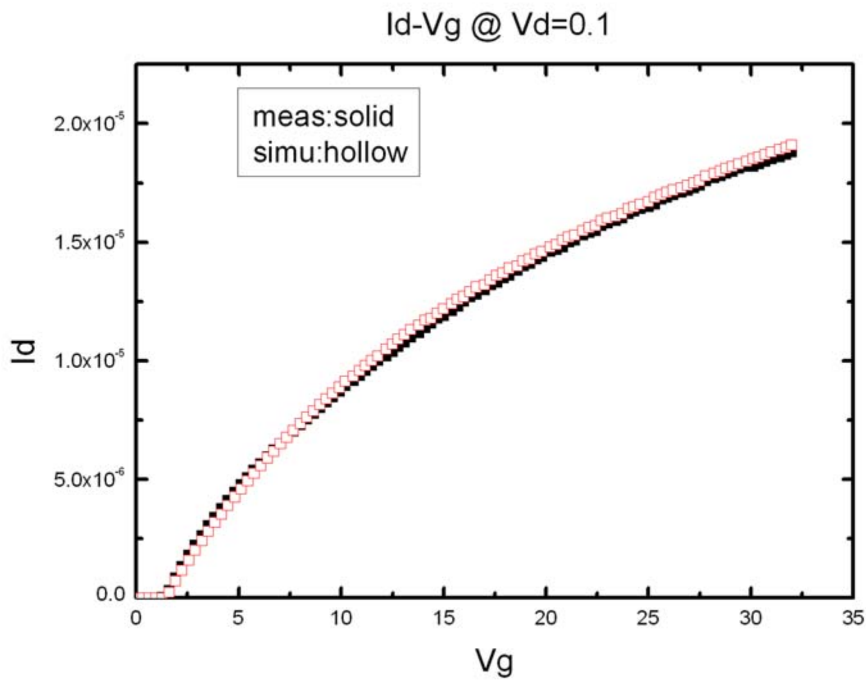


Fig.3.17(a) Comparison between measured and simulated Id-Vg (in linear region) curve.(W/L=3/5 μm)

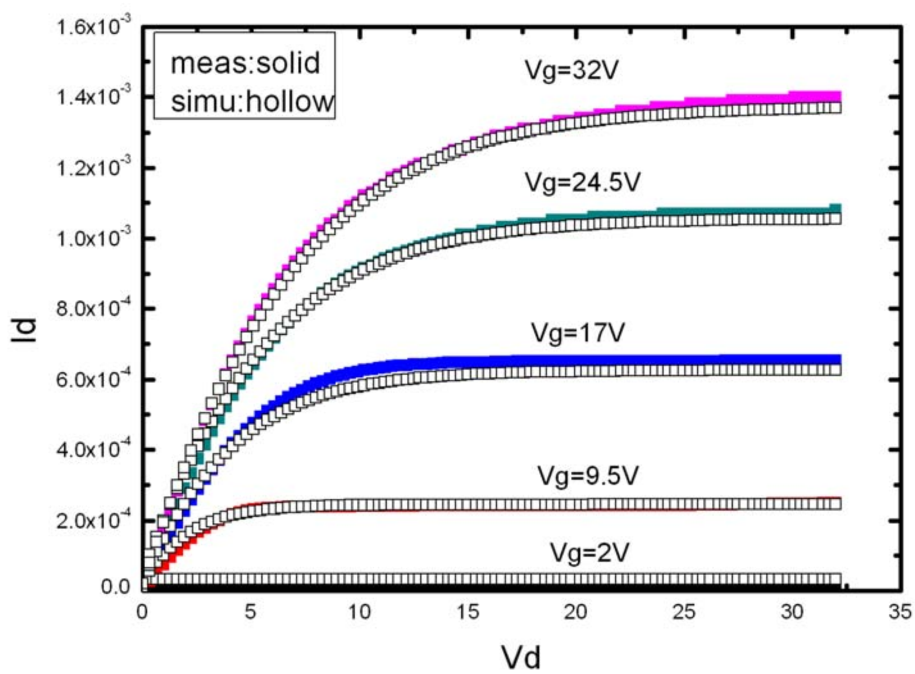
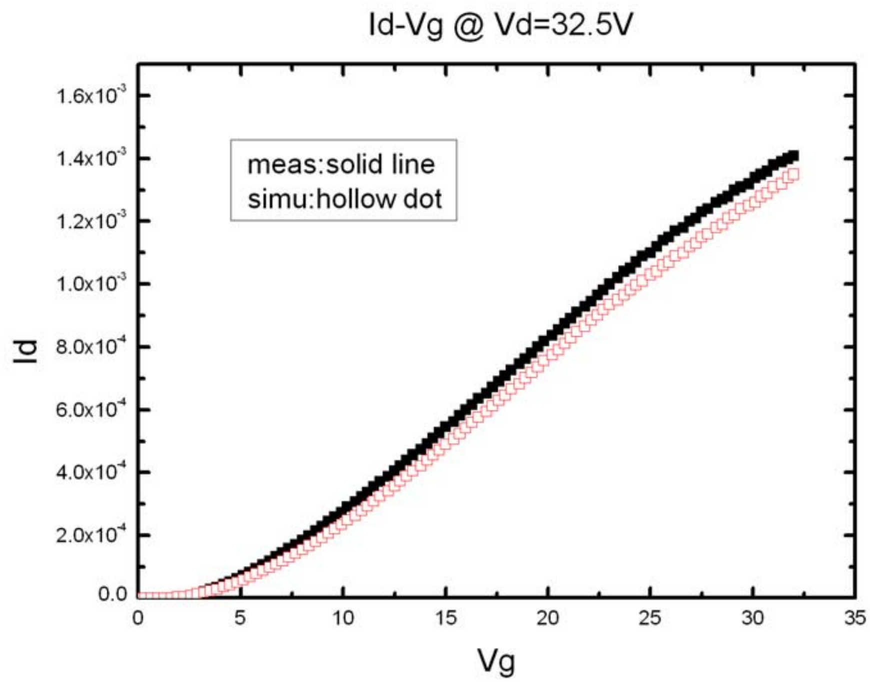


Fig.3.17(b) Comparison between measured and simulated Id-Vd curve. (W/L=3/5 μm)



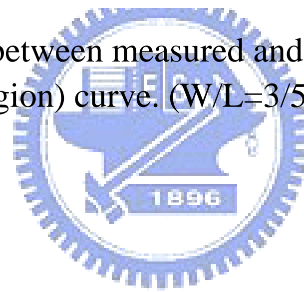


Fig. 3.17(c) Comparison between measured and simulated Id-Vg (in saturation region) curve. (W/L=3/5 μm)

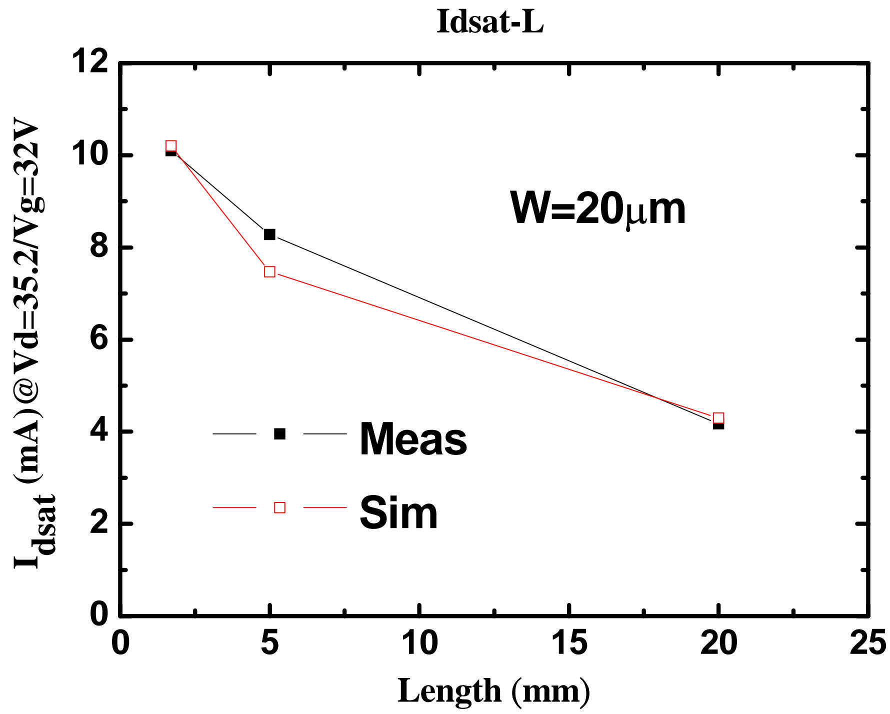


Fig. 3.18 Comparison between measured and simulated Idsat versus length.

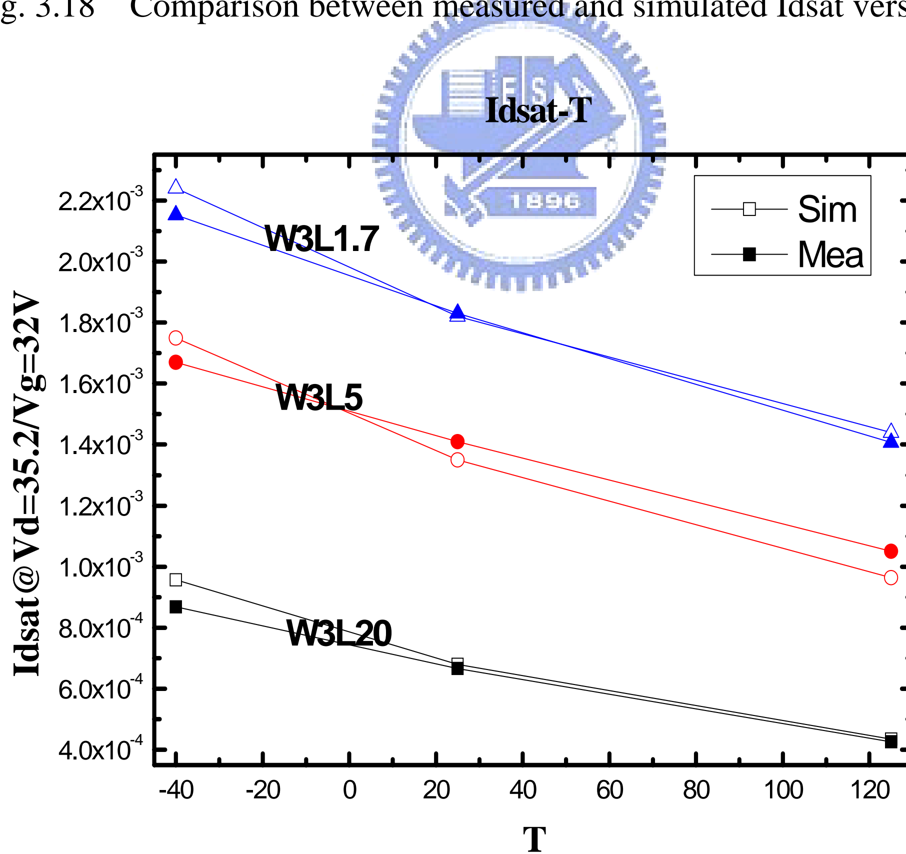


Fig. 3.19 Comparison between simulated and measured Idsat-T. (W=3 μm)

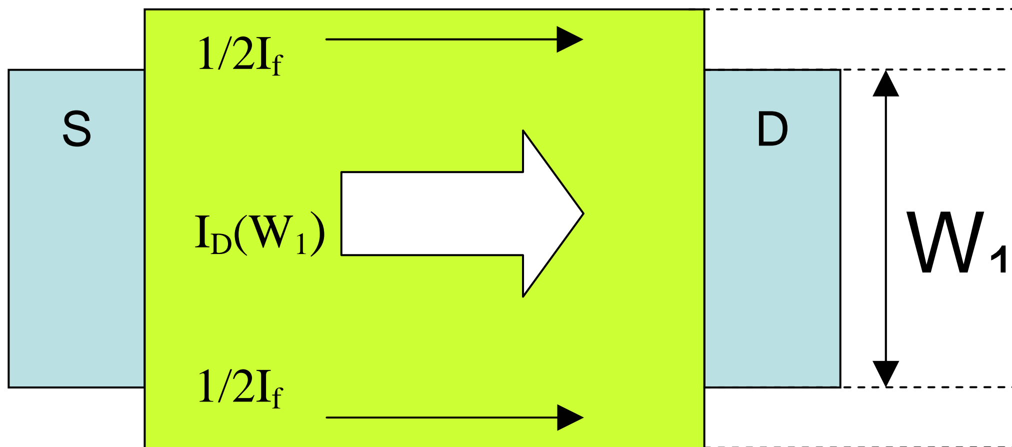


Fig. 3.20 The schematic picture of fringe currents.

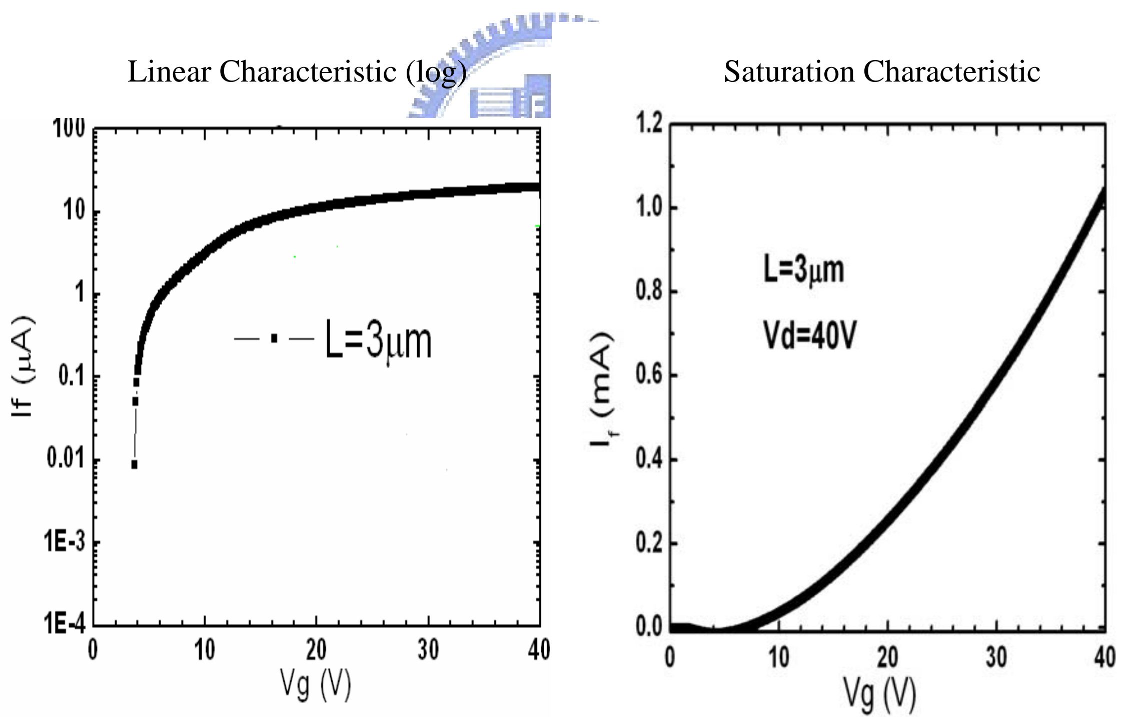


Fig. 3.21 I-V characteristics of fringe MOS.

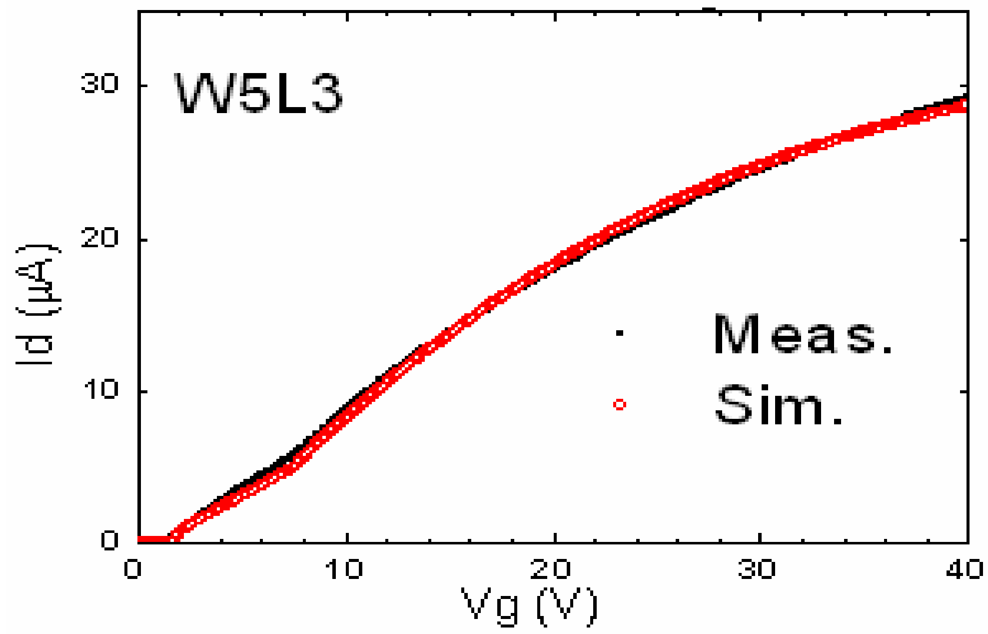


Fig. 3.22 Comparison between measured and simulated Id-Vg (at Vd=0.1V) curve.

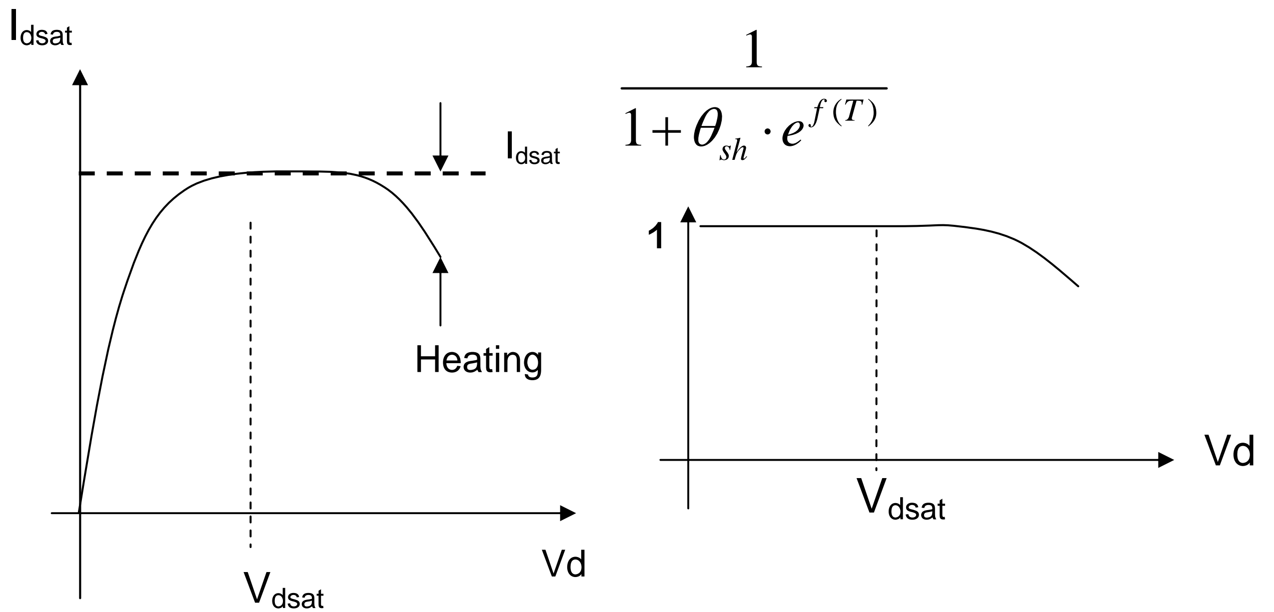


Fig. 3.23 Illustration of the way of modeling the self-heating effect.

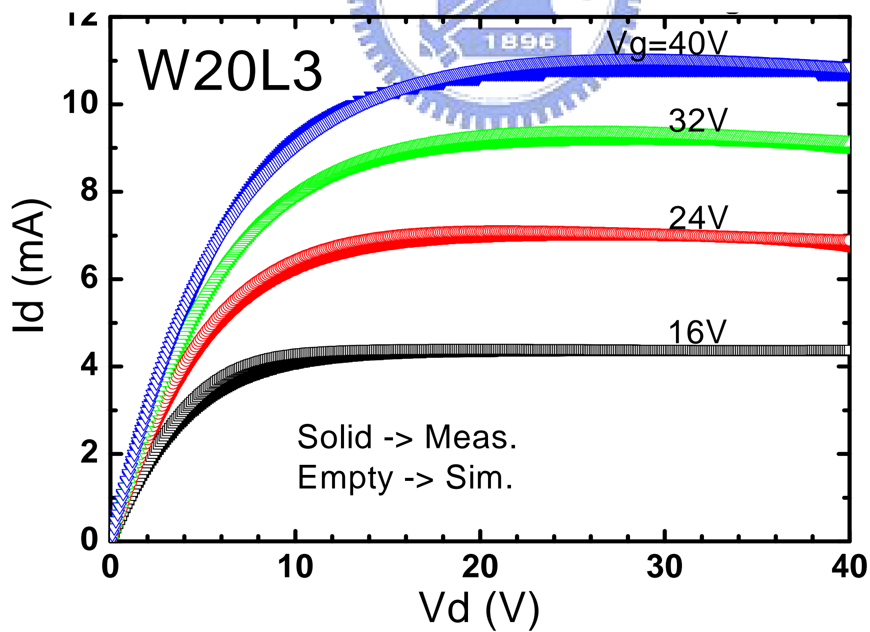


Fig. 3.24 Comparison between measured and simulated Id-Vd curve with self-heating effect.

Chapter 4
Characterization of Various Hot-Carrier Degradation Modes

4.1 Introduction

Recently, the LDMOS has been widely utilized in today's high-voltage and high-current circuits, from the standard 12V automotive battery to 100V plasma display panel drivers. A severe reliability issue of such devices is hot-carrier injection and trapping in the Si/SiO_2 interface [25-28]. The profiling of oxide degradation region and trap creation behavior, however, is rarely studied [29].

In this chapter, we demonstrate a novel three-region charge pumping (CP) technique to identify hot carrier stress induced oxide damage in a LDMOS. By comparing the pre-stress and post-stress charge pumping current in each region, we can locate oxide damage area and corresponding interface traps spread. A two-dimensional device simulation also supports our results to identify impact ionization generation (IIG) region in the device.

Three stress modes (max. Ib stress(A), Vg~1/2Vd stress(B), and max. Ig stress (C)) are investigated. The Ig-Vg and Ib-Vg curve of n-LDMOS are shown in Fig. 4.1. For each stress mode, the three-region CP method is used to measure the charge type (N_{it} or Q_{ox}) and growth characteristics. Subthreshold swing and linear drain current (Idlin) are measured to monitor device degradation

4.2 Three-Region Charge Pumping Technique

The experimental set-up of three-region charge pumping technique is illustrated in Fig. 4.2 [30]. The gate of the MOSFET is connected to a pulse generator

which gives periodic pulses with a fixed V_{gh} and varying V_{gl} while source is grounded and drain is left floating. When the gate pulses drive the channel repetitively in inversion and in accumulation, a recombination process occurs at the interface of Si/SiO_2 from the channel to drift region. We show the generation/recombination process of charge pumping energy band diagram in Fig. 4.3. I_1 is the electron trapping current from source and drain, occurring primarily in the inversion part of the pulse. I_2 is the electron emission current and electrons start to drift back to source and drain, dominant during the falling pulse edge. I_3 is the hole trapping current and the trapped electrons are recombined by bulk hole carriers, dominant during the accumulation part of the pulse. I4 is the hole emission current, dominant during the rising edge of the pulse. The net current to the substrate is then given by I_3-I_4 which is also equal to I_1-I_2. This net substrate current is generated directly proportional to the interface trap density, the transistor gate area, and the frequency of the gate pulses shown as follows:

$$I_{cp} = fQ_{cp} = fqWLN_{it} \tag{4.1}$$

This current above is called the charge pumping current and it is a direct measure of the average interface trap density.

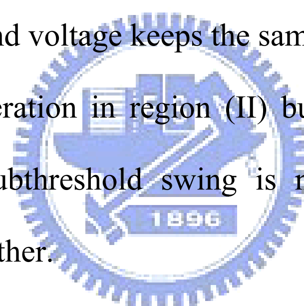
In our work, we use the device with width of 20 μm and length of 3 μm. Fig. 4.4(a) shows the device cross-section which is divided into three regions. Region (I) is the channel region. Regions (II) and (III) are accumulation region and field oxide region. The device has a threshold voltage Vt=1.5V and its flatband voltage distribution in the three regions is illustrated in Fig. 4.4(a). The CP waveform pattern is illustrated in Fig. 4.4(b) with a fixed V_{gh}=12V and varying V_{gl}. For the 100nm thick gate oxide, we can switch V_{gl} from +3.6V to -40V with a sufficiently small gate tunneling current. In this way, all of the three regions in the device can be probed. The measurement frequency is 200kHz. Typical CP measurement result is shown in Fig.

4.5. The charge pumping current (Icp) exhibits three stages, corresponding to the three regions of a n-LDMOS respectively. By measuring the change of Icp in each stage, we are able to separate N_{it} and Q_{ox} generation in each region of the device.

4.3 Various Hot Carrier Degradation Modes

4.3.1 Max. Ib Stress (Mode A)

When max. Ib stress voltage is applied, it means that the device operates under that maximum lateral electric field condition. Fig. 4.6 shows the Icp in a fresh device before and after 1400 sec. max. Ib stress (@Vg/Vd =8V/50V). The post-stress Icp of the first stage is nearly the same as the pre-stress one, indicating that region (I) oxide is not damaged by the stress. The post-stress Icp in stage 2, however, exhibits an upward shift while the flat band voltage keeps the same (no rightward shift in the Icp). This feature implies N_{it} generation in region (II) but no Q_{ox} creation. Since N_{it} is distributed in region (II), subthreshold swing is not affected. In addition, Idlin degradation is not observed either.



4.3.2 Vg~Vd/2 Stress (Mode B)

The Icp result after mode B stress (@Vg/Vd =30V/50V) is shown in Fig. 4.7. Unlike max. Ib stress mode, a distinct flat-band voltage shift in region (II) is noticed, which is manifested by a rightward shift of the Icp in stage 2. An arrow is drawn in Fig. 4.7 to indicate the flat-band voltage shift (ΔVFB). The rightward shift of the Icp is caused by negative Q_{ox} creation in region (II). The negative Q_{ox} generation rather than N_{it} generation in Vg~Vd/2 stress mode can be realized due to a reduced substrate current, as compared to max. Ib stress mode. The Q_{ox} generation rate is characterized in Fig. 4.8(a). Because of negative Q_{ox} creation, the resistance beneath the bird's beak increases. At a large Vg, region (I) resistance is relatively small and the resistance in

the bird's beak region has a larger effect. Thus, Idlin degradation measured at Vg/Vd =40V/0.1V is observed (Fig. 4.8(b)).

4.3.3 Max. Ig Stress

When a device is under max. Ig stress condition, it means that the device operates under the maximum vertical electric field condition. Fig. 4.9(a) shows the Icp result after max. Ig stress (@Vg/Vd=50V/50V) for 1000 seconds. The two-dimensional device simulation reveals that the IIG region splits into two parts (Fig. 4.9(b)); one is in the channel (region (I)) and the other is underneath the bird's beak. Two different stress induced oxide degradation mechanisms are observed; one is N_{it} generation in region (I) and the other is negative Q_{ox} creation in region (II). These two trap creation processes are reflected by an upward shift of the first stage Icp denoted by △Icp1 in Fig. 4.9(a) and by a rightward shift of the second stage Icp (△VFB2 in Fig. 4.9(a)). In contrast to max. Ib stress mode, N_{it} generation mechanism is observed in region (I) rather than in region (II), which results in an apparent subthreshold swing degradation (Fig. 4.10) in max. Ig stress mode. In addition, Q_{ox2} creation results in a more serious Idlin degradation (Fig. 4.11) in max. Ig stress mode than in Vg~Vd/2 stress mode. Note that the Idlin degradation resulting from Q_{ox} creation in region (II) should be more apparent at a larger measurement Vg, as explained above. The N_{it1} and Q_{ox2} growth rate in stress mode C are shown in Fig. 4.12 and Fig. 4.13, respectively. The Idlin degradation rate is shown in Fig.4.14. The larger Qox2 growth rate in mode C is attributed to a larger stress gate current (or a higher stress gate voltage). As a result, stress mode C has the worst Idlin degradation.

4.3.4 Result and Discussion

The LDMOS degradation behavior and trap properties in the three stress modes are summarized in Table 1. Max. Ig stress results in the worst hot carrier degradation,

which is attributed to N_{it} generation in the channel and Q_{ox} generation in the bird's beak region. Besides, max. Ib stress leads N_{it} generation in the accumulation region and thus subthreshold swing degradation is not observed. We successfully identified the trap location and property in various stress modes.

Table. 4.1 Summary of trap property and device performance degradations in various stress modes.

mode	A	B	C	
Trap Location	Region (II)	Region (II)	Region (II)	Region (I)
Trap Property	N_{it}	Q_{ox}	Q_{ox}	N_{it}
Device Degradation	N/A	I_{dlin}	I_{dlin}	$I_{subthreshold}$

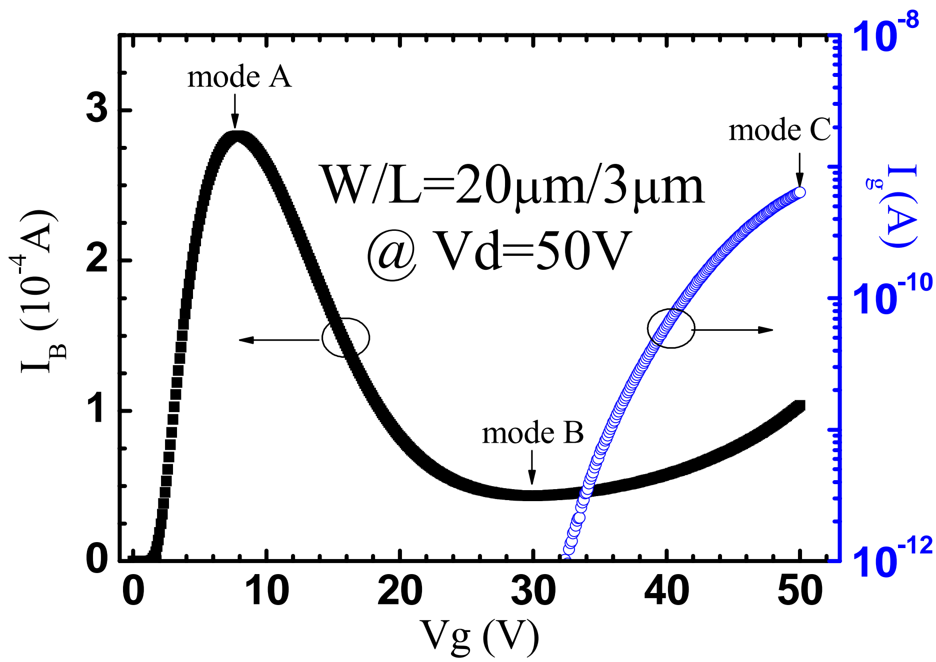


Fig. 4.1 Gate current/Bulk current versus gate voltage in a LDMOS.

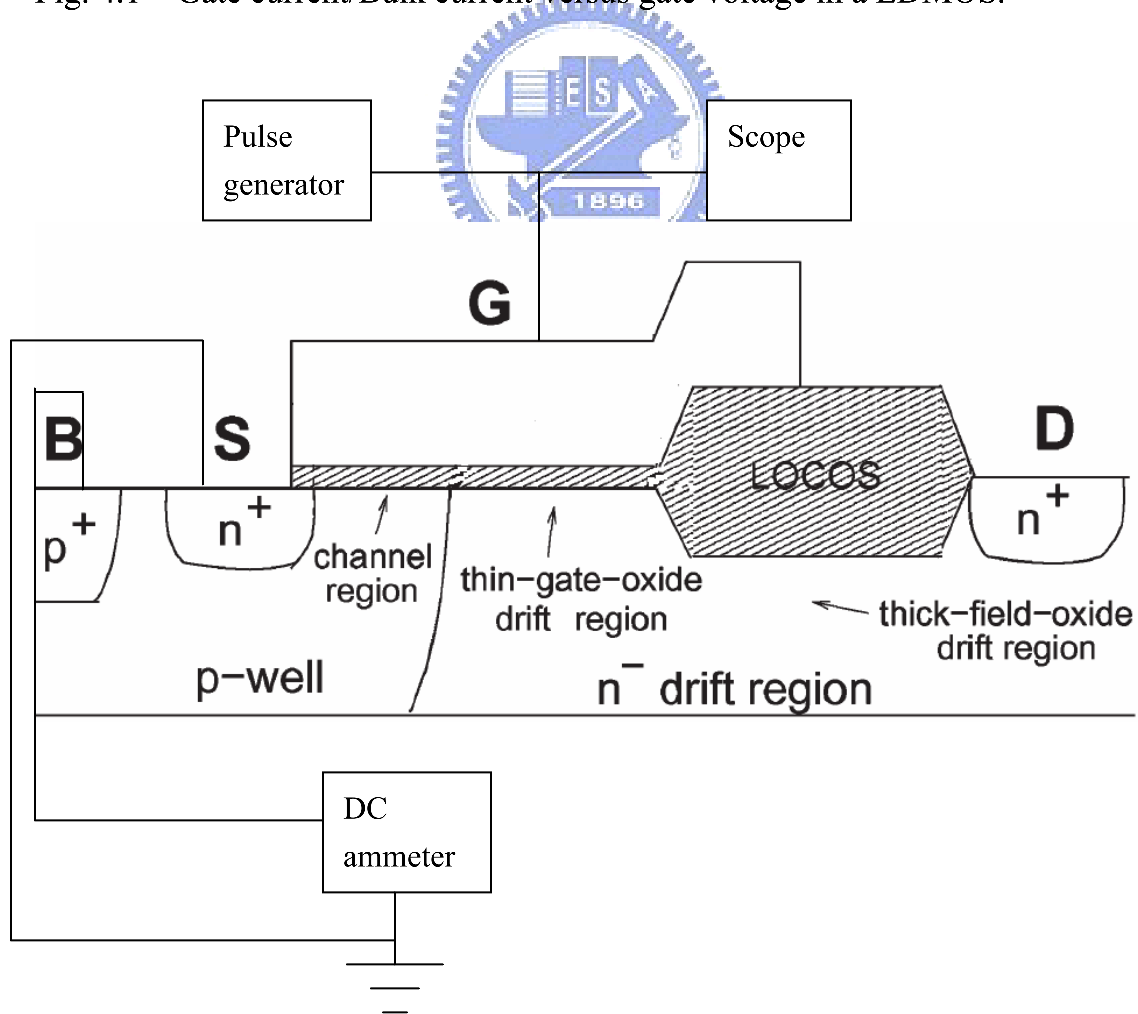


Fig. 4.2 Basic experimental set-up for charge pumping measurements.

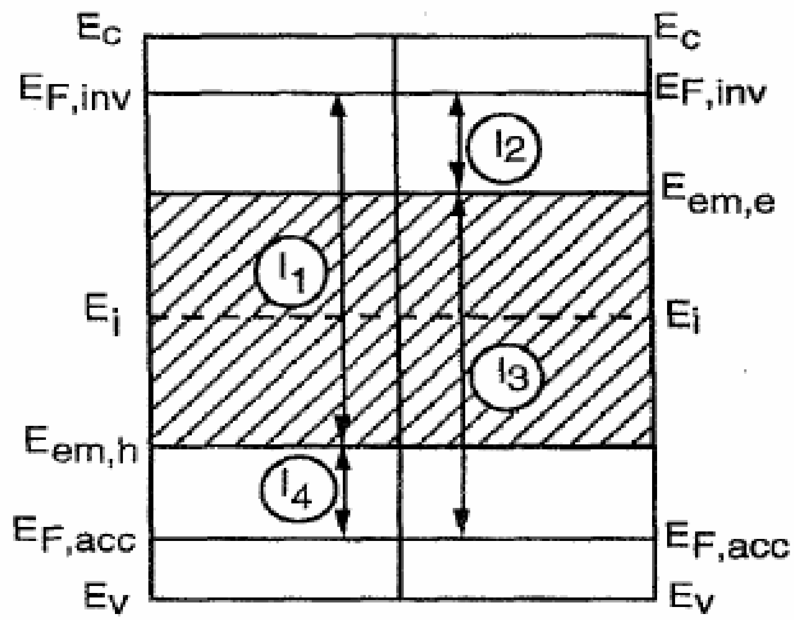


Fig. 4.3 Different energy regions associated with the four components of the charge pumping currents.

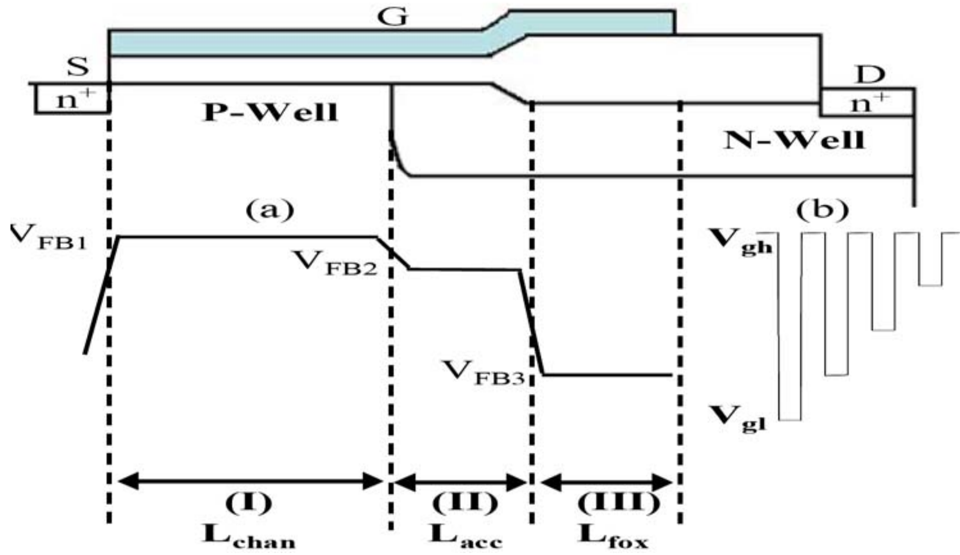


Fig. 4.4 (a) Cross-section of a N-LDMOS and flat-band voltage distribution in each region. Three different regions are indicated by L_{chan} (channel region), L_{acc}(accumulation region), and L_{fox}(field oxide region). (b)Illustration of the charge pumping measurement waveform. The V_{gh} is fixed and V_{gl} is variable.

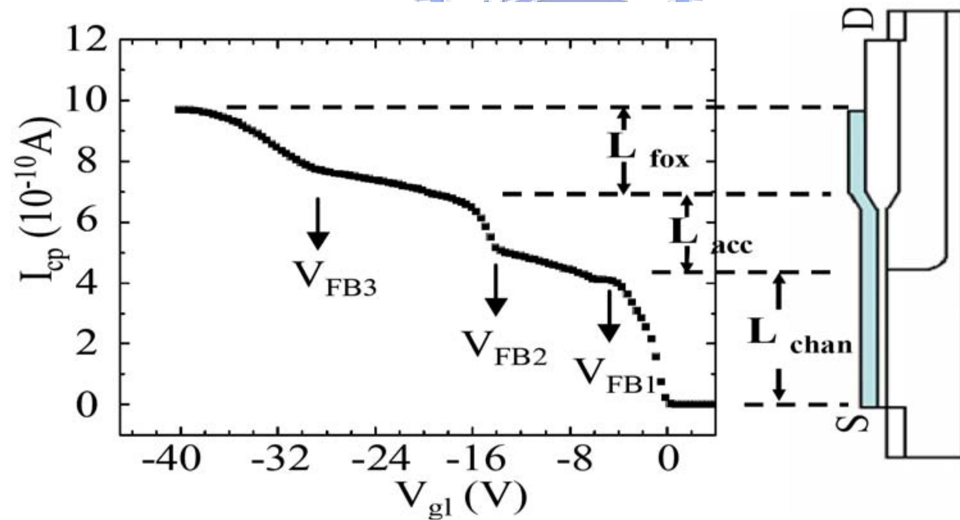


Fig. 4.5 Typical CP current in a N-LDMOS. The three stages of the CP current correspond to the three different regions of device and each stage has their flat-band voltage which is indicated in the Fig. The measurement frequency of CP is fixed at 200KHz for following experiments.

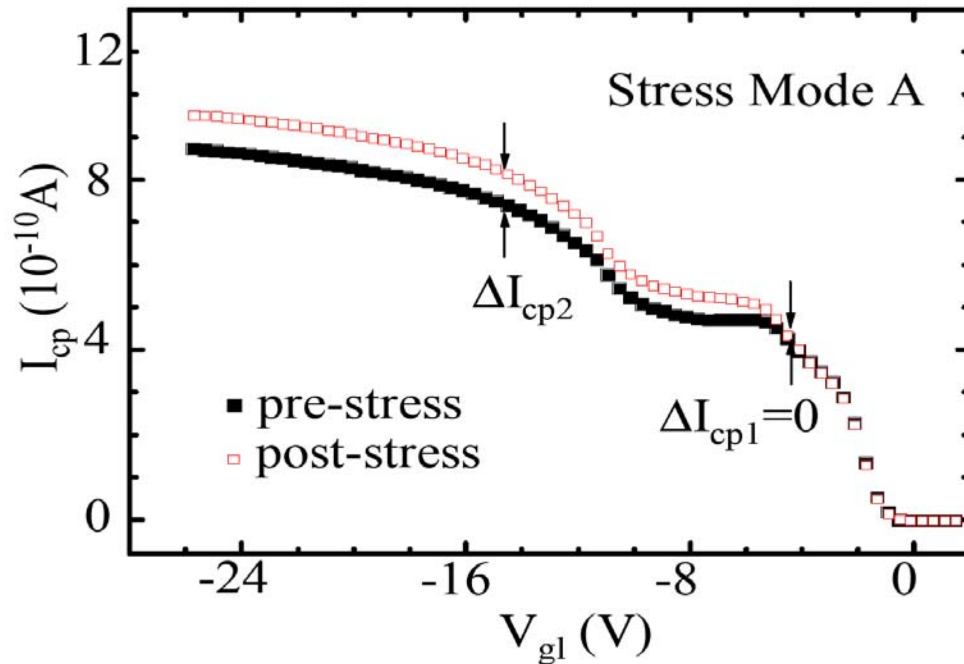


Fig. 4.6 Charge pumping result before and after 1400 sec. mode A stress. The increase of Icp2 indicated the Nit generation in accumulation region. No trap creation is observed in channel region ((ΔIcp1=0).

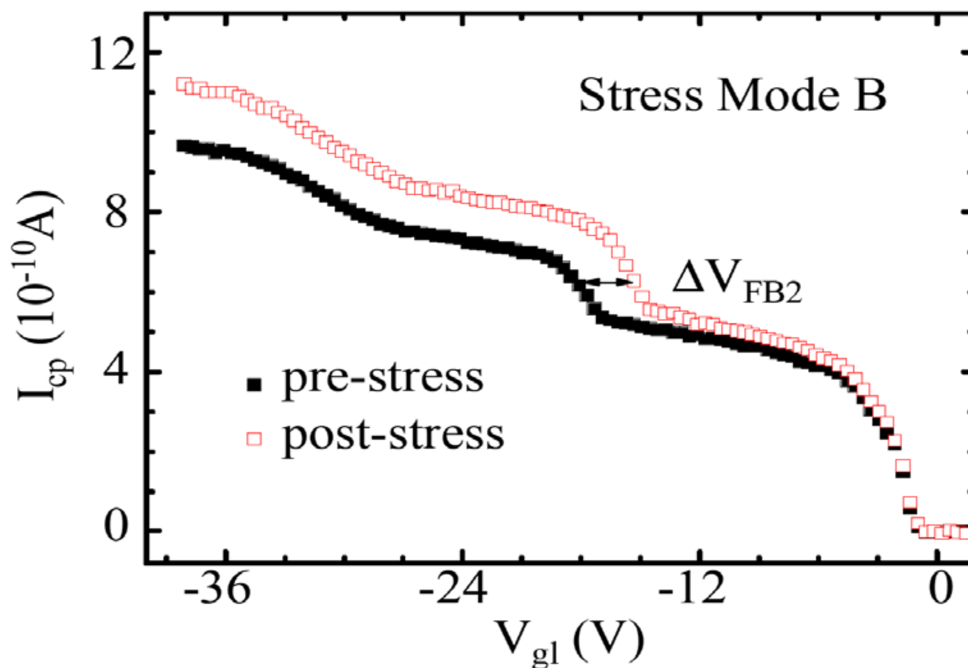


Fig. 4.7 Charge pumping result before and after 1400 sec. mode B stress. The shift of flat-band voltage implied the increase of oxide charge in accumulation region.

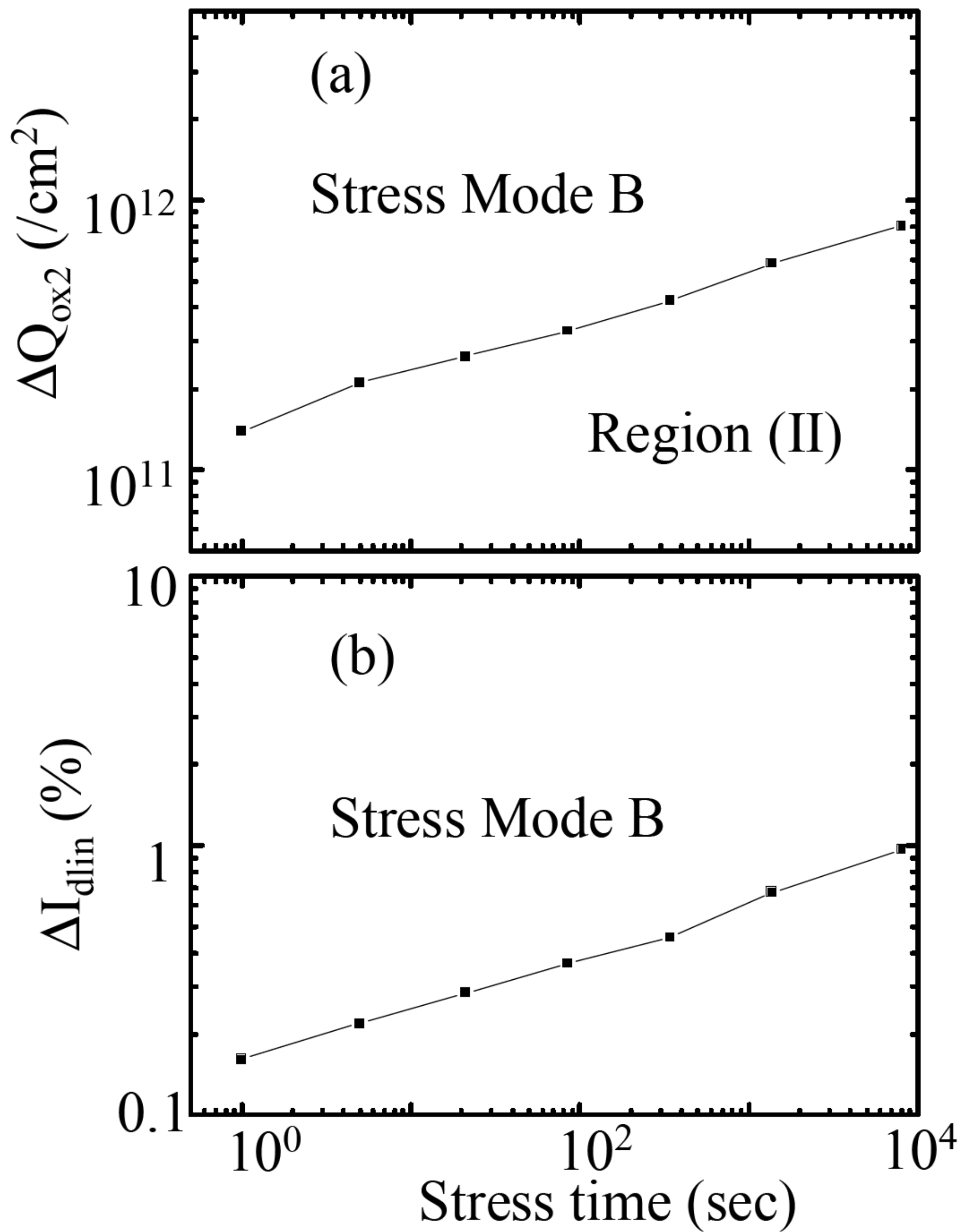


Fig. 4.8 (a) Region(II) oxide trapped charge density (average Qox2) versus stress time in stress mode B. (b) Linear drain current degradation (Idlin) rate measured at Vg/Vd=40V/o.1V in stress mode B.

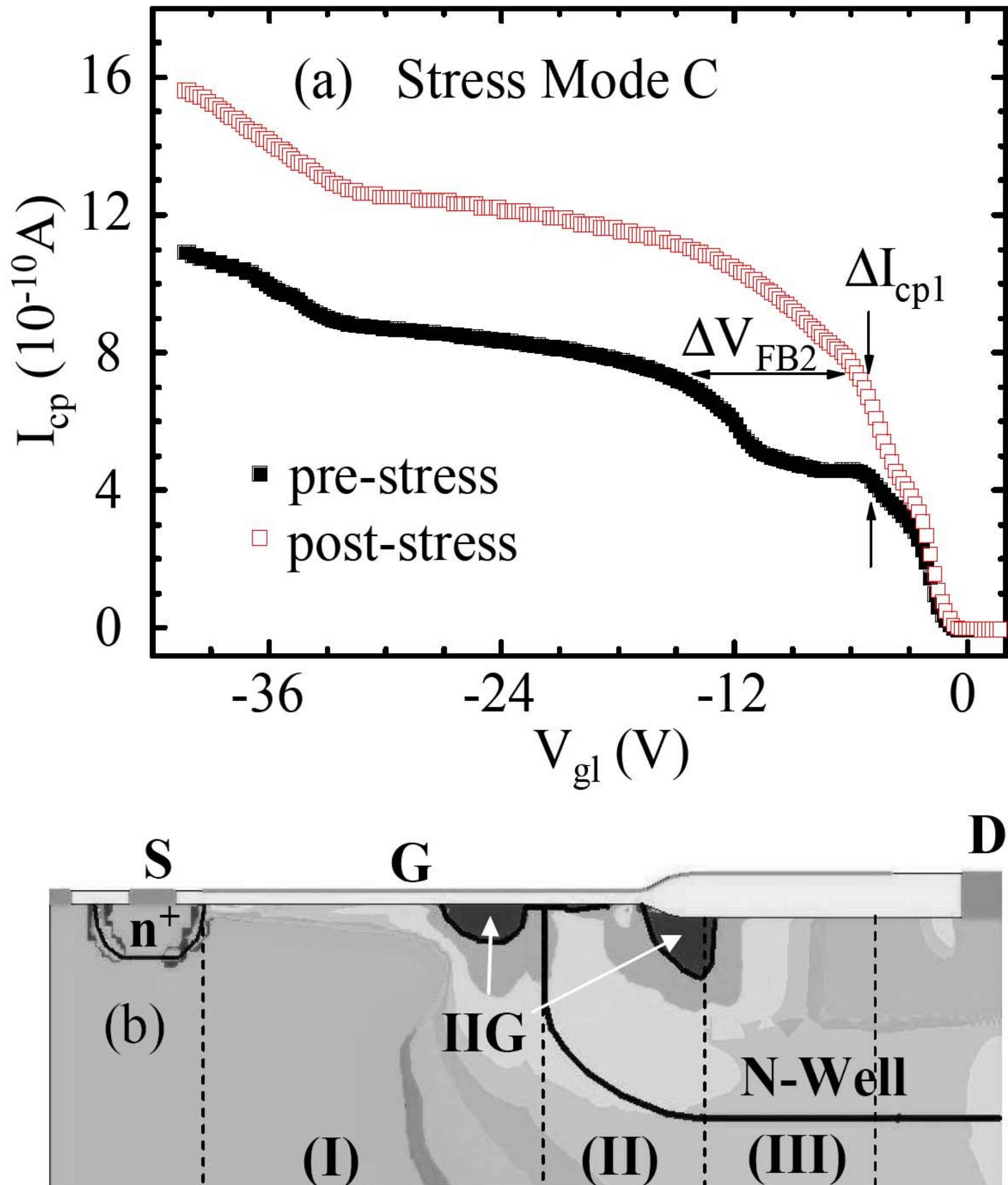


Fig. 4.9 (a) Charge pumping result before and after 1000 sec. mode C stress. Upward shift in region (I) indicated the interface trap generation in channel region and rightward shift in region (II) implied the oxide charge creation in accumulation region. (b) Simulation of impact ionization generation (IIG) distribution in stress mode C. Two IIG regions are found.

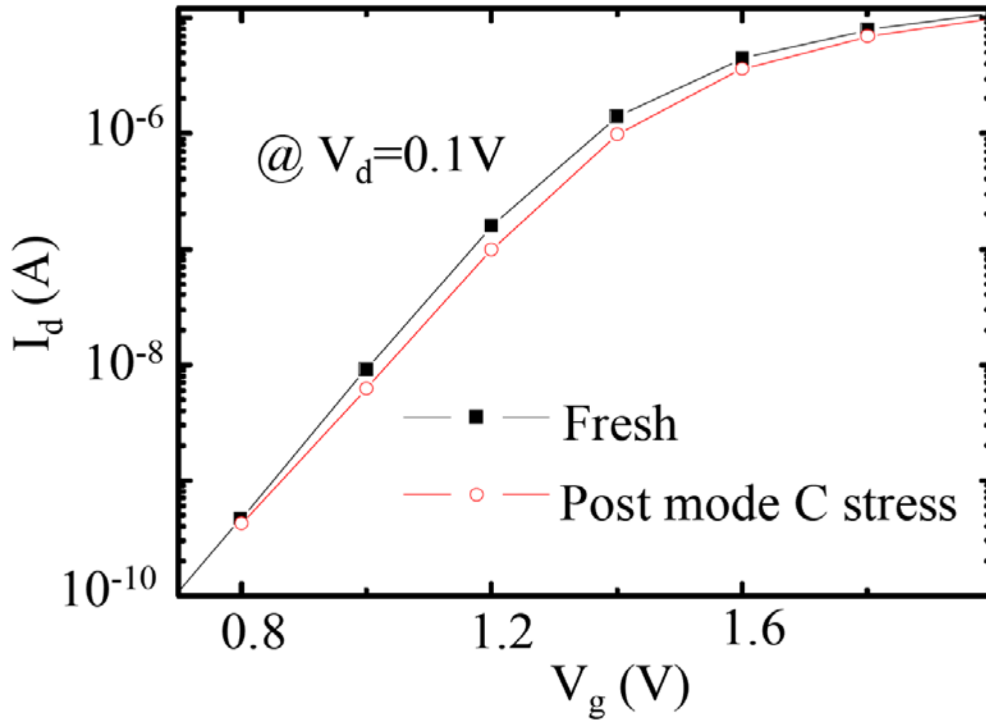


Fig. 4.10 Subthreshold characteristics before and after mode C stress. The swing degradation was due to interface trap generation in channel region.

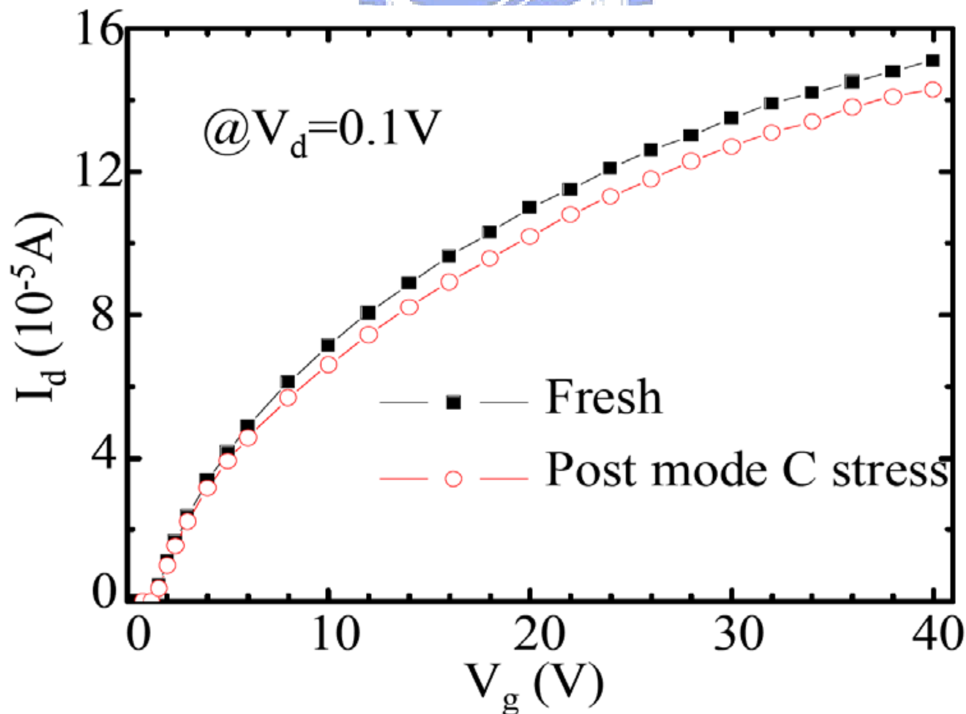


Fig. 4.11 The linear drain current before and after mode C stress. The drain current degradation is mode significant at a larger Vg and is due to oxide charge creation in accumulation region.

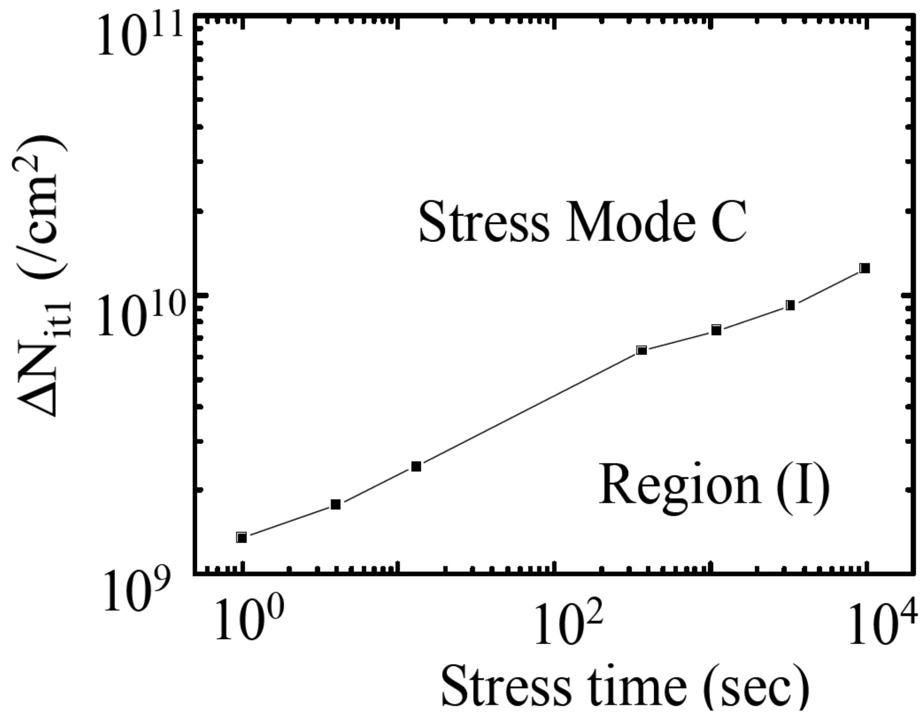


Fig. 4.12 Region (I) interface trap density (average N_{it1}) versus stress time in stress mode C.

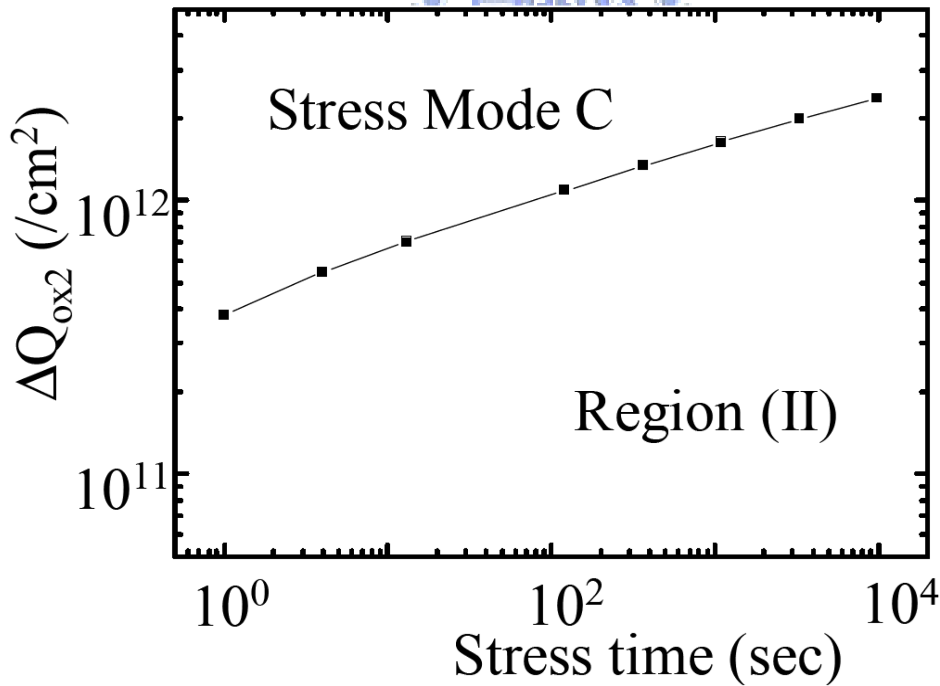


Fig. 4.13 Region (II) oxide charge density (average Q_{ox2}) versus stress time in stress mode C.

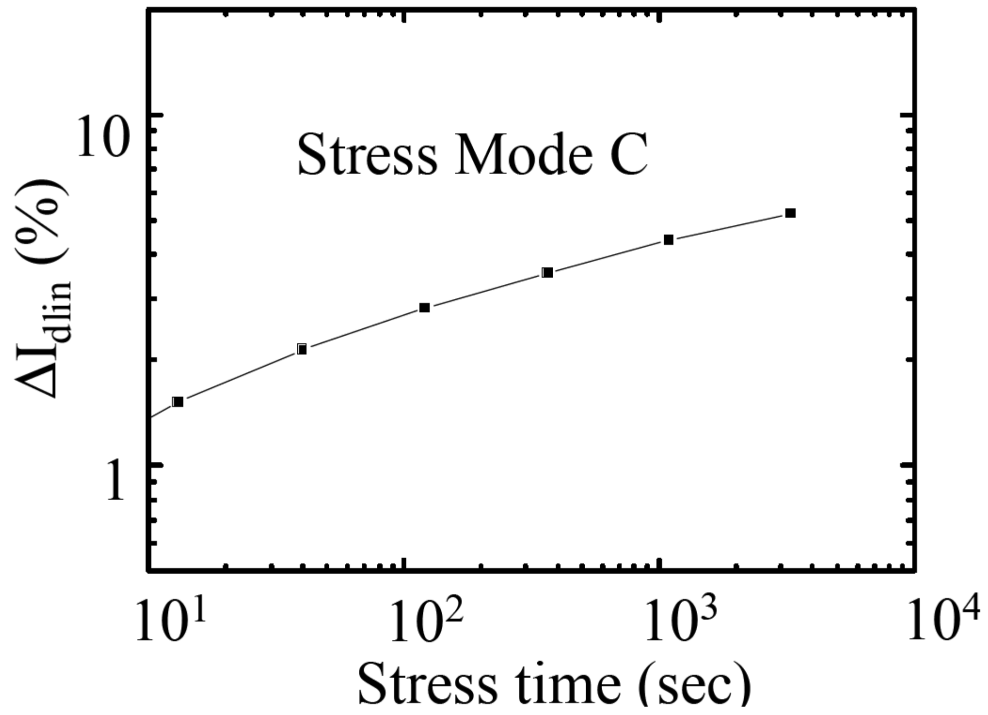
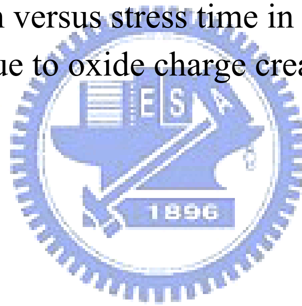


Fig. 4.14 Idlin degradation versus stress time in stress mode C. The degradation is due to oxide charge creation in accumulation region.



Chapter 5
Conclusion

According to all the investigation, we can get some conclusion. In Chapter2, lateral double diffused MOSFET (LDMOS) has been characterized including of quasi-saturation effect and three important reliability issues. By analyzing these phenomena, we get familiar with the characteristics of LDMOS and develop a SPICE macro model next.

In Chapter 3, we form a concrete SPICE macro model of LDMOS. First, we model the fringe effect by giving a MOS model (FMOS) to describe the extra fringe currents. After deducing the effect of fringe currents, we generate a sub-circuit model for LDMOS. This model consists of a voltage controlled resistance (RD) and an intrinsic MOS. By using the idea of the two stages concept, an intrinsic MOS model can be extracted by fitting measured I-V data in low-Vg stage region. Then, in high-Vg stage region, quasi-saturation effect appears and we model it by reverse calculating a virtual Vc with the intrinsic MOS model and measured I-V data and describing Rd model as a analytical expression. Finally, we bin the Rd models and intrinsic MOS models from four corner size models respectively to get a universal macro model suitable for every size and operation condition of LDMOS.

In Chapter 4, we discuss the reliability issue of LDMOS. By using the three-region charge pumping technique, the damage properties and location by stressing in different modes can be identified. Max. Ig stress condition results in most serious hot-carrier degradation, which is due to negative oxide charge occurs in bird's beak region.