

Reference

- [1] Michael S. Adler, King W. Owyang, B. Jayant Baliga, Richard A. Kokosa, "The Evolution of Power Device Technology," *IEEE Trans. Electron Devices*, vol. ED-31, NO. 11, November 1984
- [2] B. J. Baliga, "High Voltage Integrated circuits", *IEEE Press*, New York (1988)
- [3] A. Moscatelli et. al., "LDMOS implementation in a 0.35 μm BCD technology (BCD6)," *ISPSD*, pp. 323 - 326, 2000.
- [4] Z. Parpai, C. Andre, and T. Salama, "Optimization of RESURF LDMOS transistors an analytical approach," *IEEE Elect. Dev.*, Vol. 37, pp. 789 - 796, Mar. 1990.
- [5] Y. Chung, "Semi-numerical static model for nonplanar-drift lateral DMOS transistor," *IEE Proc.-Circuits Devices Syst.*, Vol. 146, No. 3, June 1999
- [6] C. Anghel, N. Hefyene, M. Vermandel, B. Bakeroot, J. Doutreloigne, R. Gillon, A. M. Ionescu, "Electrical characterization of high voltage MOSFETs using mesdrift," *CAS. Int.*, Vol. 2, Sept. 2003.
- [7] C. Anghel, N. Hefyene, A. M. Ionescu, M. Vermandel, B. Bakeroot, J. Doutreloigne, R. Gillon, S. Frere, C. Maier, Y. Mourier, "Physical modelling strategy for (quasi-) saturation effects in lateral DMOS transistor based on the concept of intrinsic drain voltage," *CAS. Int.*, Vol. 2, pp. 417 - 420, Oct. 2001.
- [8] Kyungho Lee, Jehyung Yoon, Jounghyun Yim, Jongchan Kang, Donghyun Baek, Soonhag Lee, Ilhun Shon, Bumman Kim, "An Improved Silicon RF LEMOSFET Model with a New Extraction Method for Nonlinear Drift Resistance," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 153 – 156, June 2005
- [9] E. C. Griffith, J. A. Power, S. C. Kelly, Elebert, et. al., "Characterization and modeling of LDMOS transistors on a 0.6/ μm CMOS technology," *ICMTS*, pp. 175 - 180, 2000.

- [10] J. Jaejune, T. Amborg. and Yu Zhiping, "Circuit model for power LDMOS including quasi-saturation," *SISPAD. Int.*, pp. 15 - 18, 1999.
- [11] Philip L Hower, Sameer Pendharkar, "Short and Long-Term Safe Operating Area Considerations in LDMOS Transistors," *IEEE IRPS*, pp. 545-550, April 2005
- [12] H. Rene Claessen, Piet Van Der Zee, "An Accurate DC Model for High-Voltage Lateral DMOS Transistors Suited for CACD," *IEEE Trans. Electron Devices*, vol. ED-33, NO. 12, December 1986
- [13] D. Moncoqut, D. France, P. Rossel, et. al., "LDMOS transistor for SMART POWER circuits- modeling and design," *Bipolar/BiCMOS Circuit and Technology Meeting*, pp. 216 - 219, 1996.
- [14] Annemarie C. T. Aarts, Willy J. Kloosterman, "Compact Modeling of High-Voltage LDMOS Devices Including Quasi-Saturation, " *IEEE Transaction on Electron Devices*, vol.53, NO. 4, April 2006
- [15] Y.-S. Kim, J.G. Fossum, "Physical DMOST Modeling for High-Voltage IC CAD," *IEEE Transaction on Electron Devices*, vol.37, NO. 3, pp.797-803, 1990
- [16] Y. Kim, J.G. Fossum, R. K. Williams, "New physical insights and models for high-voltage LDMOST IC CAD," *IEEE Trans. Electron Devices*, vol. 38, NO. 7, pp.1641-1649, July 1991
- [17] Gary M. Dolny, Gerald E. Nostrand, Kevin E. Hill, "The Effect of Temperature on Lateral DMOS Transistors in a PowerIC Technology," *IEEE Transaction on Electron Devices*, vol.39, NO. 4, april 1992
- [18] Belaid, M.A.; Ketata, K., Maanane, H., Gares, M., Mourgues, K., Marcon, J., "Analysis and simulation of Self-Heating Effects on RF LDMOS Device," *SISPAD*, pp.231-234, 2005
- [19] M. A.Belaid, M. Maanane, K.Mourgues, M. Masmoudi, K.Ketata, J. Marcon, "Characterization and Modelling of Power RF LDMOS Transistor Including

- Self-Heating Effects,” *Microelectronics*, pp.262-265, 2004
- [20] K. A. Jenkins, J. Y. Sun, J. Gautier, “Characteristics of SOI FET's under pulsed conditions,” *IEEE Trans. Elect. Dev.*, Vol. 44, Issue 11, pp. 1923 - 1930, Nov. 1997.
- [21] C. Anghel, A. M. Ionescu, N. Hefyene, R. Gillon, “Self-heating characterization and extraction method for thermal resistance and capacitance in high voltage MOSFETs,” *IEEE Elect. Dev. Let.*, Vol. 25, Issue 3, pp. 141 - 143, Mar. 2004.
- [22] C. Anghel, R. Gillon, A. M. Ionescu, “Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs,” *ESSDERC.*, pp. 449 - 452, Sept. 2003.
- [23] M. L. Chen, C.W. Leung, et. al., “Suppression of Hot-Carrier Effects in Submicrometer CMOS Technology,” *IEEE Trans. Electron Devices*, vol. 35, pp.2210, Dec 1988
- [24] S.M. Sze, *Physics of Semiconductor Devices*, 2nd ed., John Wiley & Sons, Inc., 1985
- [25] P. Moens, “Hot-carrier degradation phenomena in lateral and vertical DMOS transistors,” *IEEE Trans. Electron Devices*, vol.51, pp.623-628, Apr. 2004
- [26] R. Versari, “Hot-carrier reliability in submicrometer LDMOS transistors,” in *Proc. Int. Electron Device Meeting*, 1997, pp.371-374
- [27] P. Moens, “A novel hot-hole injection degradation model for lateral nDMOS transistors,” in *Proc. Int. Electron Devices Meeting*, 2001, pp.877-880
- [28] P. Moens, “Competing hot carrier degradation mechanisms in lateral n-type DMOS transistors,” in *Proc. Int. Reliability Physics Symp*, 2003, pp.214-221
- [29] J.F. Chen, “Hot carrier reliability in submicrometer 40V LDMOS transistors with thick gate oxide,” in *Proc. Int. Reliability Physics Symp*, 2005, pp.560-564
- [30] Guido Groeseneken, Herman E. Maes, “Basics and Applications of charge

pumping in submicron MOSFETs,” in *Microelectronics Reliability*, 38(1998), pp.1379-1389



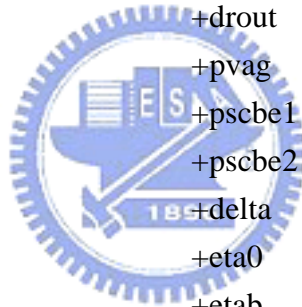
Appendix A The binning MOS model parameters extracted from LDMOS device

```

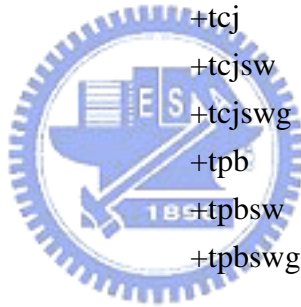
.model N NMOS {
+level = 49
+lmin    = 1.7e-006
+lmax    = 2.0001e-005
+wmin    = 3e-006
+wmax    = 2.0001e-005
+version = 3.24
+mobmod  = 1
+capmod  = 3
+nqsmod  = 0
+binunit = 2
+binflag = 0
+lref    = 1.7e-006
+wref    = 3e-006
+tref    = 25
+xl      = 0
+xw      = 0
+lmlt    = 1
+wmlt    = 1
+tox     = 8.4e-008
+toxm    = 8.4e-008
+wint    = 0
+lint    = 0
+dlc     = 0
+dwc     = 0
+hdif    = 3.53e-006
+ldif    = 8.5e-008
+ll      = 0
+wl      = 0
+lln     = 1
+wln     = 1
+lw      = 0
+ww      = 0
+lwn     = 1
+wwn     = 1
+lw1     = 0
+ww1     = 0
+cgbo    = 1e-013
+cgso    = 4e-010
+cgdo    = 3e-010
+xpart   = 1
+vth0    = 1.243
+k1      = 1.836
+k2      = 0.075663825
+l1k2    = -1.420765e-007
+w1k2    = -2.1311475e-008
+pk2     = 4.2622951e-013
+k3      = 4
+k3b     = -1.4
+nlx     = 0
+dvt0    = 4.026
+dvt1    = 0.5456
+dvt2    = -0.005512623
+ldvt2   = -1.3114754e-007
+wdvt2   = -1.9672131e-008
+pdvt2   = 3.9344262e-013
+dvt0w   = 0
+dvt1w   = 0
+dvt2w   = 0
+nch     = 1.21e+016
+voff    = -0.07161
+nfactor = 1
+cdsc    = 0
+cdscb   = 0
+cdscd   = 0
+cit     = 0.0001586

```

+u0	= 0.070526789	+pvsat	= -2.2177049e-007
+lu0	= -1.4347541e-008	+keta	= -0.051767239
+wu0	= -3.0253809e-008	+lketa	= 1.1416831e-007
+pu0	= 5.7311475e-014	+wketa	= 1.0385323e-008
+ua	= 1.8111263e-009	+pketa	= -6.8417705e-013
+lua	= 3.0768852e-015	+dwg	= 0
+wua	= -3.3471167e-015	+dwb	= 0
+pua	= 5.5409836e-022	+alpha0	= 0
+ub	= 1.0298287e-018	+beta0	= 30
+lub	= -8.6848087e-024	+pclm	= 2.0502732
+wub	= 1.8521697e-024	+lpclm	= -1.0054645e-006
+pub	= -1.7398689e-029	+wpclm	= -3.9344262e-008
+uc	= 4.7684024e-012	+ppclm	= 7.8688525e-013
+luc	= -1.4595628e-016	+pdiblc1	= 1e-005
+wuc	= -2.0362584e-017	+pdiblc2	= 1e-005
+puc	= -1.2577836e-021	+pdiblc3	= 0.01
+ngate	= 1e+023	+drouT	= 0.56
+xj	= 3.6e-006	+pvag	= 0
+w0	= 0	+pscbe1	= 4e+008
+prwg	= 0	+pscbe2	= 1e-007
+prwb	= 0	+delta	= 0.01
+wr	= 1	+eta0	= 0.0001
+rdsw	= 7000	+etab	= 0.0014480874
+a0	= 0.44028737	+letab	= -3.0961749e-008
+la0	= -9.9268852e-007	+wetab	= -3.2786885e-009
+wa0	= 8.5982642e-007	+petab	= 6.557377e-014
+pa0	= 3.4222951e-012	+dsub	= 0.56
+ags	= -0.62440939	+elm	= 5
+lags	= 1.3936176e-005	+alpha1	= 0
+wags	= 1.8971495e-006	+lalpha1	= 0
+pags	= -3.8358754e-011	+walpha1	= 0
+a1	= 0	+palpha1	= 0
+a2	= 0.9	+clc	= 1e-007
+b0	= 0	+cle	= 0.6
+b1	= 0	+cf	= 0
+vsat	= 29658.335	+ckappa	= 0.6
+lvsat	= 0.16345683	+cgdl	= 1e-010
+wvsat	= 0.014264995	+cgsl	= 1e-011



+acde	= 0.4	+mj	= 0.31
+lacde	= 0	+cjsw	= 1.17e-010
+wacde	= 0	+mjsw	= 0.3
+pacde	= 0	+pb	= 0.81
+moin	= 6	+rd	= 0
+lmoin	= 0	+rdc	= 0
+wmoin	= 0	+rs	= 0
+pmoin	= 0	+rsc	= 0
+noff	= 1.85	+xti	= 3
+lnoff	= 0	+acm	= 12
+wnoff	= 0	+calcacm	= 0
+pnoff	= 0	+nj	= 1
+voffcv	= 0	+pbsw	= 0.7
+lvoffcv	= 0	+cjswg	= 1.17e-010
+wvoffcv	= 0	+pbswg	= 0.7
+pvoffcv	= 0	+mjswg	= 0.7
+kt1	= -0.1065406	+tcj	= 0.001
+lkt1	= -1.603541e-006	+tcjsw	= 0.001
+wkt1	= -2.6916798e-006	+tcjswg	= 0.001
+pkt1	= 7.8806557e-012	+tpb	= 0.0022
+kt11	= 0	+tpbsw	= 0.0019
+kt2	= -0.09942	+tpbswg	= 0.0019
+ute	= -1.5		
+ua1	= 5.2117743e-009	}	
+lua1	= 1.3240984e-014		
+wua1	= -1.7502411e-015		
+pua1	= -4.5245902e-021		
+ub1	= -8.8196593e-018		
+lub1	= -4.5585792e-024		
+wub1	= 6.3101254e-024		
+pub1	= -7.9672131e-030		
+uc1	= -5.6e-011		
+prt	= 7000		
+at	= 33000		
+rsh	= 4.55		
+js	= 8e-006		
+jsw	= 8e-012		
+cj	= 0.000464		



簡 歷

姓名:杜冠潔

性別:女

生日:民國 71 年 02 月 22 日

籍貫:台北市

地址:台北市民生東路五段 192 號 13F-4

學歷:國立交通大學電子物理系 89.9-93.6

國立交通大學電子工程研究所碩士班 93.9-95.6

碩士論文題目:



高壓元件LDMOS可靠度分析與SPICE模型建立

Investigation of Spice Modeling and Reliability Issues in
High Voltage LDMOS