國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

超低功率高面積使用率全數位鎖相迴路頻率合成器

Ultra Low Power Area Efficient All Digital Phase-Locked Loop Frequency Synthesizer

研 究 生：陳冠華

指導教授：黃 威 教授

中 華 民 國 九 十 五 年 九 月

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摘　要

本論文提出一個運用所提出的低功率演算法的全新全數位鎖相迴路架構。低功率的搜尋演算法能使我們的全數位鎖相迴路在 22 個參考週期內完成相位鎖定，而且可以使硬體方面簡單及面積小的優點。並且在論文中提出的低功率數位控制震盪器具有兩種架構，第一種適合用在高速下，而第二種適合用在寬的頻率範圍。這兩種數位控制震盪器都可以使全數位鎖相迴路更加地省電。提出的邏輯及閘鎖存器為基礎的頻率相位偵測器可以偵測多種參考頻率的倍數。總體而言，我們所提出的全數位鎖相迴路具有面積小以及低功率消耗的特性。

本論文以TSMC 0.13um 1P8M CMOS 技術實現。供給電壓為 1.2 伏，總面積為 0.0041mm^2。模擬結果顯示當數位控制震盪器頻率為 700 萬赫茲時，全數位鎖相迴路的相位抖動為 18.4ps,1.38%(Pk-Pk)，而總功率消耗為 0.85mW。

Ultra Low Power Area Efficient All Digital Phase-Locked Loop Frequency Synthesizer

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ABSTRACT

A new all digital phase-locked loop (ADPLL) architecture with low power algorithm is presented in this thesis. The proposed low power search algorithm can accomplish phase lock process within 22 input clock cycles and make the hardware simple, area small. In thesis, proposed low power digitally controlled oscillator (DCO) has two types. The two types of proposed DCO make proposed ADPLL lower power. The proposed NAND latch based Phase-Frequency-Detector (PFD) can detect multi times of reference frequency .This ADPLL has characteristics of small area cost and lower power consumption.

The proposed ADPLL is simulated and implemented by TSMC 0.13um 1P8M CMOS technology. The supply voltage is 1.2v and total area is 0.0041mm^2. The simulation results show that when the DCO operates at

700MHz, the jitter is 18.4ps, 1.38% (Pk-Pk) and the total power consumption of ADPLL is 0.85mW.

Acknowledgements

I would like to express my deepest gratitude to my advisor Prof. Wei Hwang for his enthusiastic guidance and encouragement throughout the research. With his support, I have the confidence and energy to stride forward.

Following, I would like to thank all my friends, Po-Tsang Huang, Ming-Hung Jang, Hau-Yi Yang, Chung-Hsien Hua, Wei-Jr Shie, Jang-Shiuan Jang, Jung-Wen Liou, Shu-Wei Jang, and Tzung-Shi Yang, at LPSOC lab. They provide an interesting place for life and work and also gave me much support and discussion on my thesis research.

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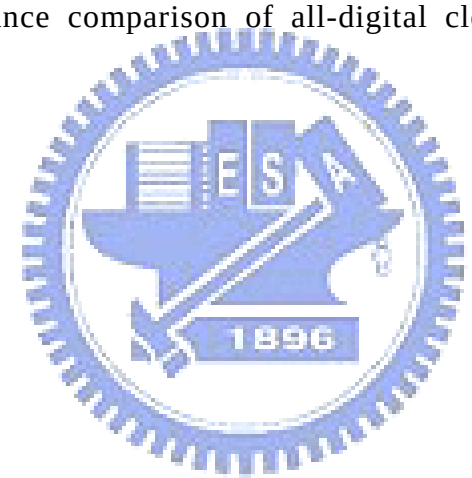

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Chapter 1 Introduction

1-1 Research motivation

The phase-locked loop (PLL) has been widely used in consumer, computer and communication aspects. It performs the tasks of frequency synthesis, clock / data recovery, clock de-skewing, duty-cycle enhancement and so on [1.1]. Now we show some applications of PLL.

1) PLL for clock de-skewing application

As shows in Figure 1-1(A), the skew between point A (or point B) and clock_in is due to the clock tree. Figure 1-1(B) shows the PLL application of clock de-skewing, skew between clock_in and point A (or point B) can be eliminated, even when there are delay differences between the two paths due to clock buffering and other factors.

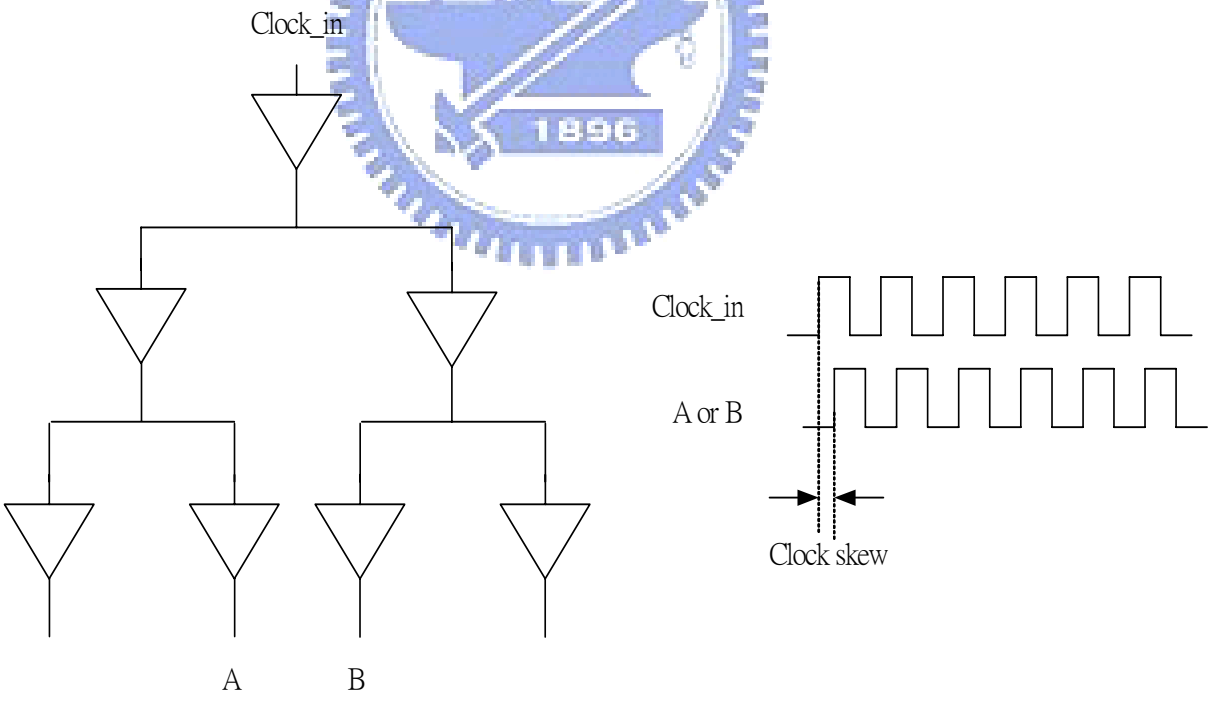

Figure 1-1(A) Clock Tree & Clock skew

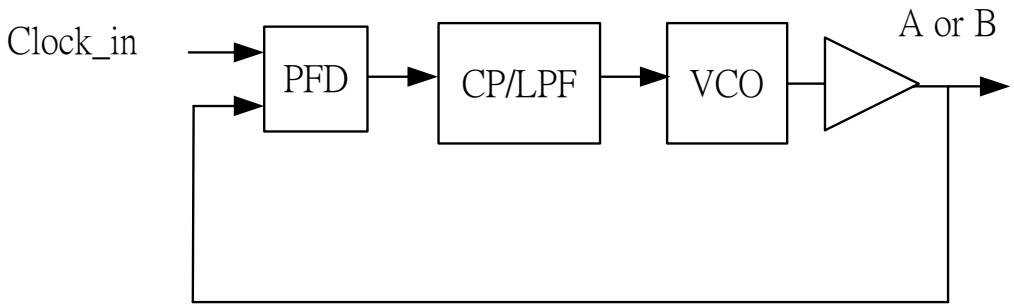

Figure 1-1(B) PLL for clock de-skewing application

2) PLL for frequency synthesizer application

As shows in Figure 1-2, the PLL is used as a frequency synthesis to generate a synthesized clock. The output frequency of F_out clock is synthesized as

$$F\_out = (M / N) \times F\_in \quad (1.1)$$

A frequency synthesizer allows the designer to generate a variety of output frequencies as multiples of a single reference frequency. The main application is in generating local oscillator (LO) signals for the up- and down-conversion of RF signals.

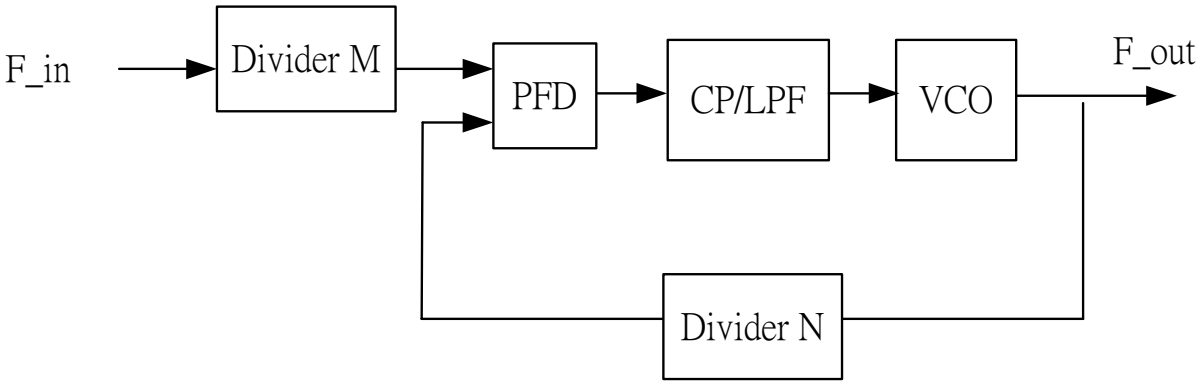

Figure 1-2 PLL for frequency synthesizer application

3) PLL for Clock Data Recovery application

As shows in Figure1-3, it is the PLL application for Clock Data Recovery (CDR). In general, the task of the Clock Data Recovery architectures is to recovery the phase-and-frequency information from the input by extracting the clock from transitions in the data stream.

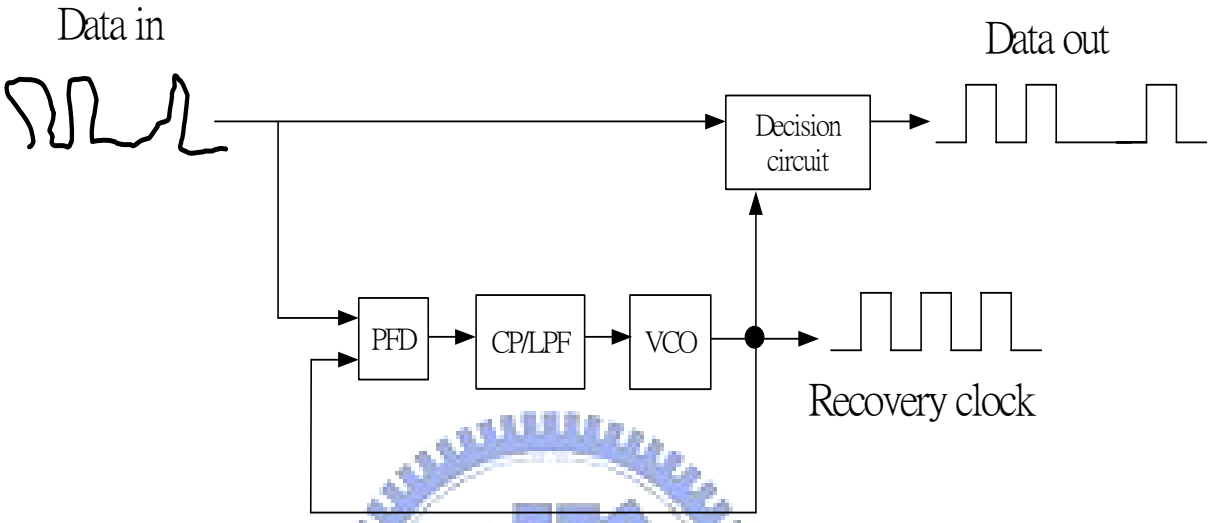

Figure 1-3 PLL for Clock Data Recovery application

Traditionally, a PLL is made as an analog building block. However, integrating an analog PLL in a digital noisy system-on-chip (SoC) environment is difficult. In addition, the analog PLL is sensitive to process parameters and must be redesigned for each new technology. Assuming that the digitally controlled PLL is implemented with only active components such as transistors, it will scale with technology. Capacitors and resistors, which are used in analog circuits will not scale with technology to the same extent [1.2][1.3].

If we integrate an analog circuit with digital circuit, the digital noise affects the performance of the analog circuit. It is difficult to isolate the noise which generated from the digital part. Also, in the IC process, the digital process is usually different from the analog process. In analog PLL, we must pay more attention to the matching problem and provide good quality of capacitor.

The Since the implementation of analog component in a digital environment is not a simple task, the linear phase-locked loop (LPLL) and classical digital phase-locked

loop (DPLL) which relay on analog component have been replaced by the all digital phase-locked loop (ADPLL). The ADPLL becomes more and more popular in recently year. It can avoid the disadvantages of analog circuits by using the ADPLL in digital system. Also, the ADPLL has characteristics of fast frequency locking, full digitization, and good stability.

1-2 Thesis organization

This thesis is organized as below.

- **Chapter 1 Introduction**
- **Chapter 2 PLL overview**
- **Chapter 3 Proposed Low Power Digitally Controlled Oscillator (DCO)**
- **Chapter 4 Proposed Low Power All Digital Phase-Locked Loop**
- **Chapter 5 Application and Simulation Result**
- **Chapter 6 Conclusion and Future Work**

Chapter 2 PLL overview

We give the overview of phase-locked loop (PLL), including LPLL, DPLL and ADPLL.

Chapter 3 Proposed Low Power Digitally Controlled Oscillator (DCO)

We introduce many kinds of digitally controlled oscillator and propose the low power digitally control oscillator.

Chapter 4 Proposed Low Power ALL Digitally Phase-Locked Loop (ADPLL)

We introduce the algorithm and architecture of conventional ADPLL which is proposed by Motorola in 1995. And, We present a low power search algorithm and multi-time phase frequency detector and state the circuit design in each function block such as control unit, enable generator match delay line..

Chapter 5 Application and simulation result

Chapter 6 Conclusion and Future Work

■ Chapter 2　PLL overview

In this chapter, we will review three kinds of phase locked-loop circuit [2.1], they are: Linear PLL (LPLL), Digital PLL (DPLL), and All-Digital PLL (ADPLL). The very first phase locked-loops (PLLs) were implemented as early as 1932 by de Bellescize; this French engineer considered the inventor of coherent communication. The PLL found broader industrial applications only when it becomes available as an integrated circuit.

The first PLL ICs appeared around 1965 and were purely analog devices. In the following years the PLL drifted slowly but steadily into digital territory. The very first digital PLL (DPLL), which appeared around 1970, was in effect a hybrid device. A few years later, the all-digital PLL (ADPLL) was invented. The ADPLL is exclusively built from digital function blocks and hence do not contain any passive components like resistor and capacitors. Different types of PLLs behave differently.

■ Classifications of PLL circuit

(1) LPLL: Linear PLL. Each block is analog.

(2) DPLL: Digital PLL. Phase Detector is digital and the others are analog.

(3) ADPLL: All Digital PLL. Each block is digital. Loop filter is from Up/Down counter. VCO (Voltage Controlled Oscillator) is from DCO (Digital Controlled Oscillator).

2-1 The operating principle of PLL

A PLL is a circuit which causes a particular system to track with another one. More precisely, a PLL is a circuit synchronizing an output signal (generate by an oscillator) with a reference or input signal in frequency as well as in phase. In the synchronized—often called locked—state the phase error between the oscillator's output signal and the reference signal is zero, or very small. If phase builds up, a control mechanism acts on the oscillator in such a way then the phase error is again reduced to a minimum. In such a control system the phase of the output signal is actually locked to the phase of the reference signal. This is why it is referred to as a phase-locked loop. The operating principle of the PLL is explained by the example of the linear PLL. [2.2]

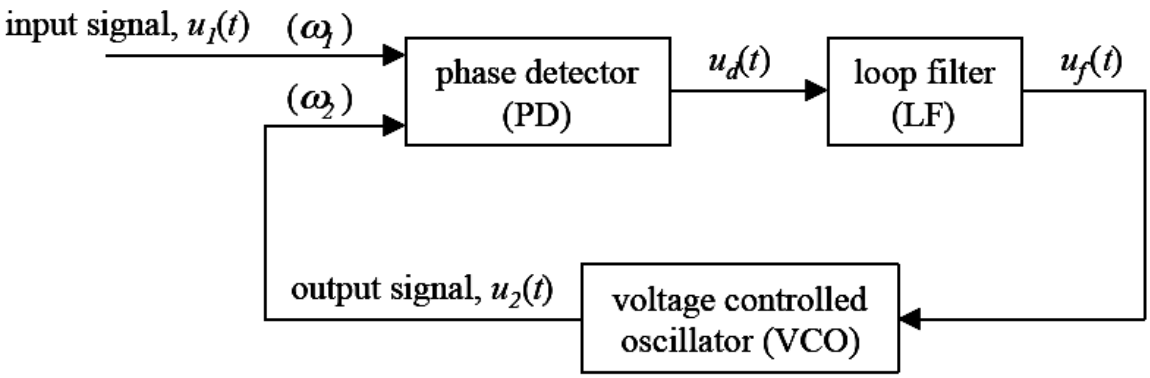

Figure 2-1 Block diagram of the PLL

In the Figure 2-1, the signals of interest within the PLL circuit are defined as follows:

$U_1(t)$: the reference(or input) signal

ω_1: the angular frequency of the reference signal

$U_2(t)$: the output signal of the VCO

ω_2: the angular frequency of the output signal

$U_d(t)$: the output signal of the detector

$U_f(t)$: the output signal of the loop filter

Θ_e: the phase error define as the phase difference between signals $U_1(t)$ and $U_2(t)$

Now we look at the operations of the three functional blocks in the Figure 2-1.

Functional Blocks：

VCO:

VCO generate an angular frequency ω_2 ,which is determined by the output signal U_f of the loop filter. The angular frequency ω_2 is given by equation (2.1) , where ω_0 is the center frequency of the VCO and the K_0 is the VCO gain. Equation2.1 is plotted graphically in the Figure 2-2.

$$\omega_2 = \omega_0 + K_0 \times U_f(t) \qquad (2.1)$$

Phase Detector:

the Phase Detector compares the phase of the output signal of VCO with the phase of reference signal and generate an output signal $U_d(t)$ which is approximately

proportional to the phase error Θ_e. So we can write the equation as equation (2.2). K_d is the gain of the phase detector.

$$Ud(t) = K_d \times \Theta_e \qquad (2.2)$$

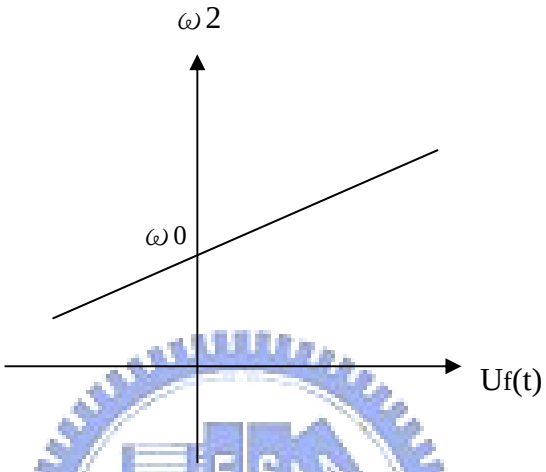

Figure 2-2 The VCO transfer function

Equation (2.2) is plotted graphically in the Figure 2-3.The output signal U_d (t) of the PD Consists of a dc component and a superimposed ac component.

Loop Filter:

Because the output signal of the PD consists ac component and it is undesired, so we need a loop filter to cancel the ac component.

Different types of PLLs have different building blocks. Following sections will discuss Linear PLL, Digital PLL and All Digital PLL The next section will analyze and design Linear PLL.

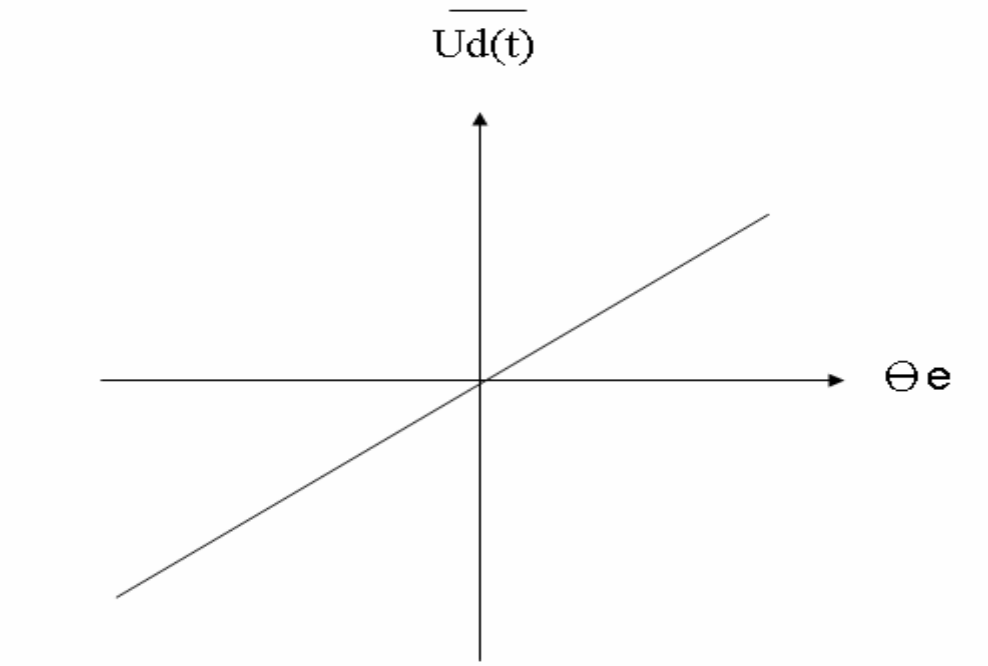

Figure 2-3 The PD transfer function

2-2 Linear PLL

Although the PLL is a non-linear system, it can be described with a linear model if the loop is in lock. [2.3] When the loop is in lock the phase error signal generates by the phase detector settles on a constant value. In the locked state, the output signal has a fixed frequency as the input reference signal. A phase difference between the input reference signal and output signal may exist depending on the type of PLL used. When the loop is in lock the phase difference remains constant.

The Linear PLL is built from three purely analog function blocks. They are Phase Detector, Loop Filter and VCO .The three blocks are describe in the following:

PD: PD can be a four phase analog multiplier or analog signal mixer.

LF: LF is a passive or active RC filter, it filter high frequency signal and noise from phase detector and environment. The output of the filter is a DC value to send to VCO.

VCO: It is a ring oscillator which construct by inverters. The frequency is controlled by

the DC value from PD.

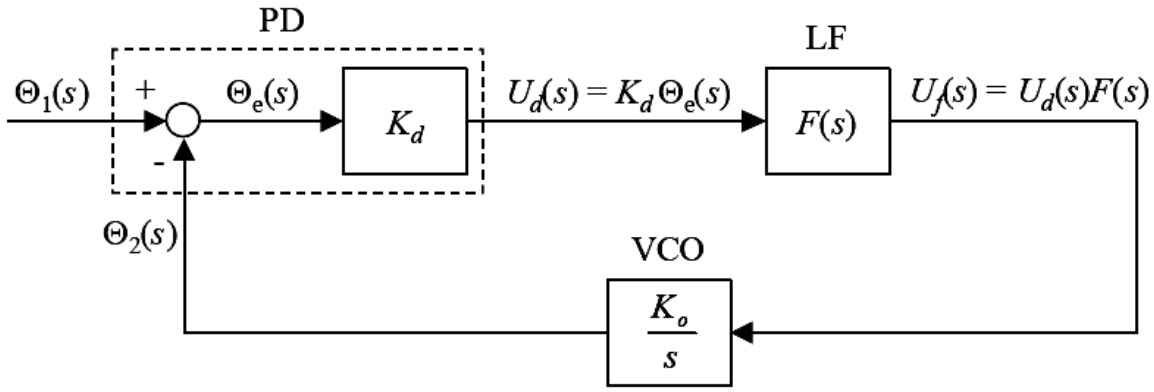

Figure 2-4 Linear PLL model

The building blocks of Figure 2-4 are taken as basis for the mathematical model of a Linear PLL in lock. The following analysis shows step by step how to obtain the Linear PLL transfer function. The next is the transfer function:

$$H(s) = \frac{\theta out}{\theta ref} \tag{2.3}$$

Note that the phase detector sums the input reference phase Θ_{ref} ,with the feedback phase Θ_{fb} ,and amplifies the difference with a gain K_{PD} to produce an error voltage V_e (s) ,and Ve(s) equal to:

$$Ve(s) = K_{PD} \times \Theta e(s) = K_{PD} \times [\Theta ref(s) - \Theta out(s)] \tag{2.4}$$

And the output of the loop filter is Vc(s), and Vc(s) equal to:

$$Vc(s) = Ve(s) \times F(s) \tag{2.5}$$

Because the VCO can be modeled as a phase integrator, the transfer function of the VCO block equal to K_{VCO}/S. So the output of the VCO equal to:

$$\theta out(S) = \frac{Vc(S) \times Kvco}{S} \tag{2.6}$$

So the transfer function of the Linear PLL H(S), is equal to the following:

$$H(S) = \frac{\theta_{out}(S)}{\theta_{ref}(S)} = \frac{K_{PD}K_{VCO}F(S)}{S + K_{PD}K_{VCO}F(S)}$$

(2.7)

The phase error transfer function is equal to the following:

$$H(S)=\frac{\theta_e(S)}{\theta_{ref}(S)}=\frac{S}{S+K_{PD}K_{VCO}F(S)} \tag{2.8}$$

The VCO control voltage transfer function is equal to the following:

$$H(S)=\frac{V_C(S)}{V_{ref}(S)}=\frac{SK_{PD}F(S)}{S+K_{PD}K_{VCO}F(S)} \tag{2.9}$$

The following observation is made from the transfer function give in equation (2.7), (2.8) and (2.9).At first, we discuss the Linear PLL transfer function, give in equation (2.7), it has a low-pass characteristic. This means that for slow (low frequency) variations in the reference phase, the loop will basically track the input signal and produce an output phase.

The phase error transfer function, give in equation (2.8), has a high pass characteristic. This implies that for slow variations in the reference phase, the phase error will be small. However, fast variations in the reference phase will not be filtered and show up as a phase error.

The VCO control voltage transfer function, give in equation (2.9), also has a high pass characteristic. However, depending on the parameter of the loop filter, it can take on a more band-pass shape.

The linear model in Figure 2-4 enables us to analyze the tracking performance of the Linear PLL, i.e., the system maintains phase tracking when excited by phase steps, frequency steps, or other excitation signals. So we can analyze the characteristic and

the responses of the Linear PLL in S-domain, and then, calculate all parameter to design a Linear PLL to satisfy the specification.

2-3 Digital PLL

In this section, we will describe the operating principle and circuit design of Digital PLL. [2.2] Figure 2-5 shows the Digital PLL which consists Digital Phase Frequency Detector, analog Charge Pump, analog Loop Filter, analog Voltage Controlled Oscillator and Frequency Divider.

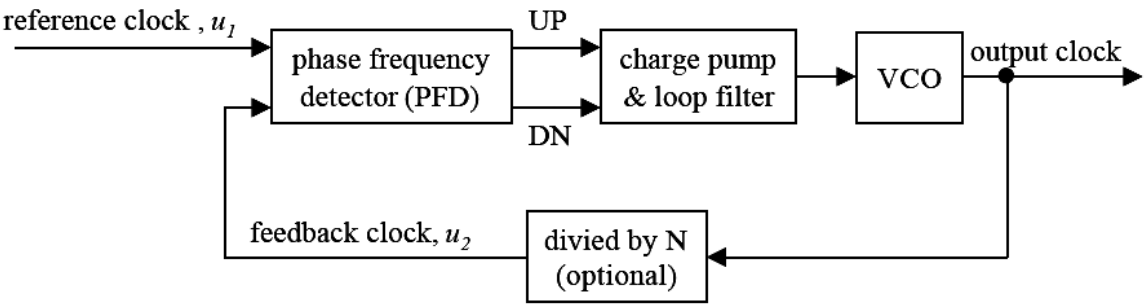

Figure 2-5 Digital PLL Block

The Phase Frequency Detector can detect the phase and frequency error between the input reference signal and feedback clock signal. The output of the PFD is up signal or down signal. The up signal and down signal control the Charge Pump to

charge or discharge. Loop Filter can filter the high frequency signal. Loop Filter outputs a low frequency signal to control the VCO. By including a Frequency Divider in the feedback path, the VCO output clock runs N times faster than the feedback clock. The next sections will describe the circuit and behavior of the PFD, CP, LP, FD, and VCO.

2-3-1 Phase Frequency Detector

This section will describe the operation and implementation of the PFD circuit. Figure 2-6 shows an example of the PFD circuit and Figure 2-7 shows the waveforms in some conditions. Unlike multipliers and XOR gate, sequential PFD generates two outputs that are not complementary. Illustrated in Figure 2-6, the operation of a typical PFD is as follows.

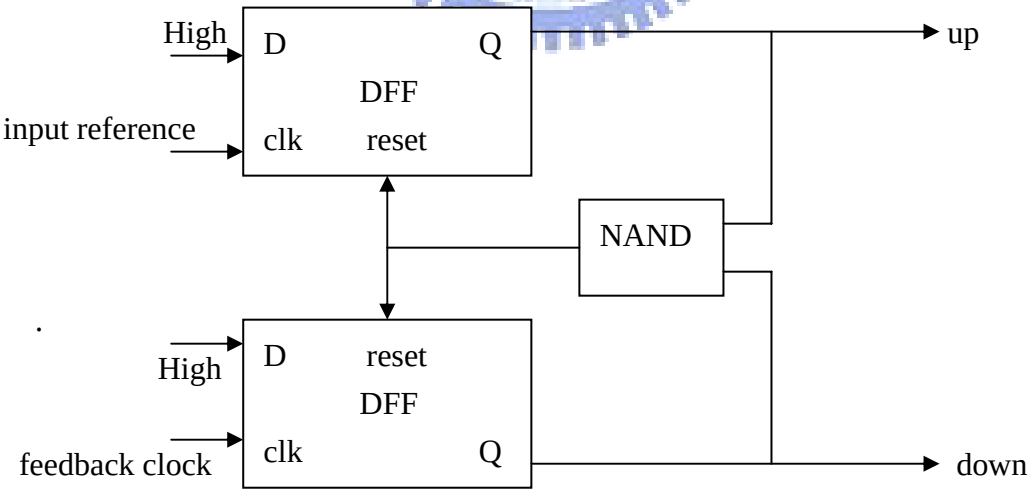

Figure 2-6 Phase Frequency Detector Block

When the feedback clock is high and the input reference is low, then the PFD

produces positive pulses at down signal, while up signal remains at zero.

Conversely, if input reference is high and feedback clock is low then positive pulses appear at up signal while down signal is zero. It should be note that, in principle, up and down are never high together in the simulation. The average value of up – down is an indication of the frequency or phase difference between input reference and feedback clock. [2.2]

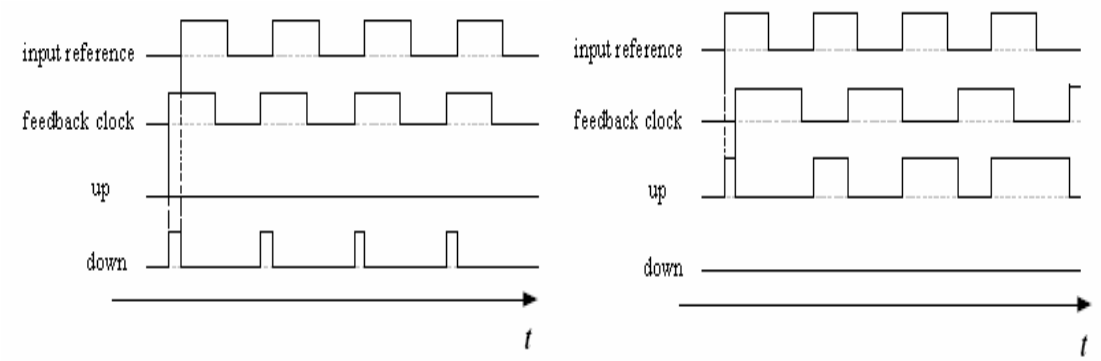

Figure 2-7(A) Figure 2-7(B)

Figure 2-7(A) PFD response with input reference lagging feedback clock

Figure 2-7(B) PFD response with ω reference lagging $\succ$ ω feedback clock

In the Figure 2-8, it shows the PFD circuit behavior. It has three state diagrams: up=1,down =0(state I) ; up=0,down=0(state 0) ; up=0,down=1(state II) ;

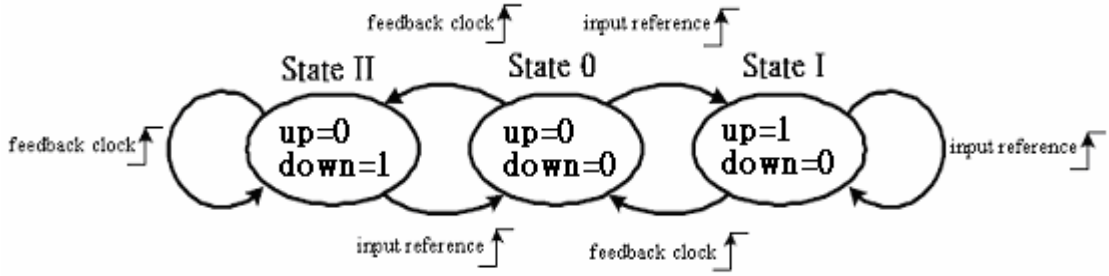

Figure 2-8 PFD state diagram

Because the PFD is buildup from two edge-triggered sequential circuits, we can avoid dependence of the output upon the duty cycle of the inputs. If the PFD is in the state 0, up=down=0, then a transition on A take it to state I, where up=1, down=0.

With state I is reached, any more rising edges at input A won't cause state change at all. The circuit will remain in this state until a transition occurs on B, upon which the PFD returns to state 0. The switching sequence between state 0 and state II is similar.

The PFD can nominally detect a full range of phase difference, i.e. $+2\pi$, -2π . A phase difference larger than 2π is truncated with respect to integer of 2π . The output of the PFD can drive a three-state charge pump. The charge pump and loop filter will be discussed followed.

2-3-2 Charge Pump/Loop Filter

In a PLL system, the charge pump transfers the digital signal of up and down from the PFD to an analog signal. Figure 2-9 shows a simple model of the charge

pump circuit. It consists of both matched current sources, each with a fixed value. When the up signal is high, the switch connects to A and Vc is charged by the up current source Iup. Similarly, when the down signal is high, the switch connects to B and Vc is charged by the lower current source Idown. If both up signal and down signal are low, then the switch maintains at original node and Vc holds the original voltage.

Most of the PLL's specifications are determined by the loop filter. The loop filter can be either passive or active. In general, a passive filter is simple to design and has better noise performance. The passive filter was shown in Figure 2-10, which may be first-order, second-order, or other high order structures.

As show in Figure 2-11, charge pump circuit convert the logic state of the PFD (Up and Down) into an analog counterpart for controlling the VCO. The charge pump output and the input of a VCO must have the low leakage tendency. So a passive loop filter shapes the output of the charge pump circuit to suppress the un-wanted message. The time domain response can be shown in Figure 2-11.

As discussed in the previous section, if the input reference signal leads the feedback signal, the pulse appear at up signal, then positive charge accumulates on capacitor steadily.

Conversely, if the input reference signal lags the feedback signal, the charge is removed from capacitor on every phase comparison. In the third state, when input reference and feedback signal are equal, up and down keep low. Both switches are off, and the output signal Vc remains constant.

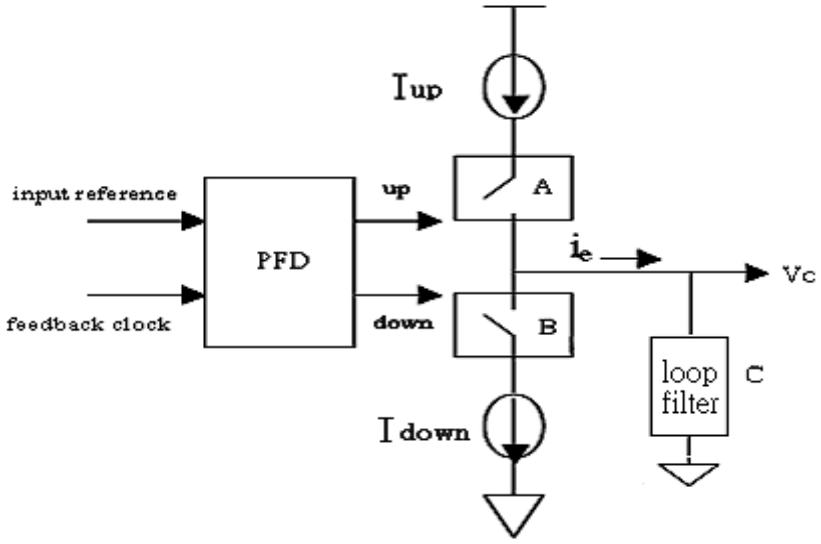

Figure 2-9 Charge Pump & Loop Filter

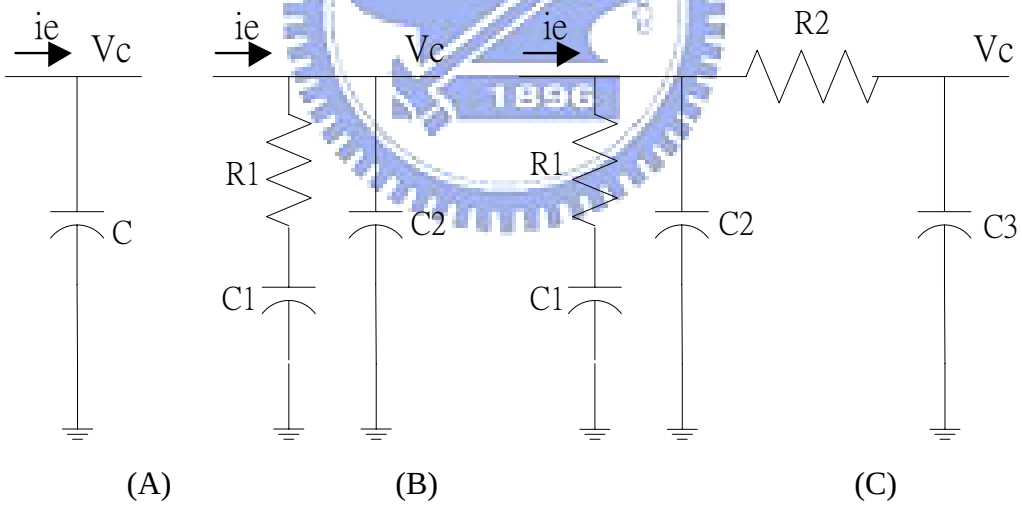

Figure 2-10 Loop Filter

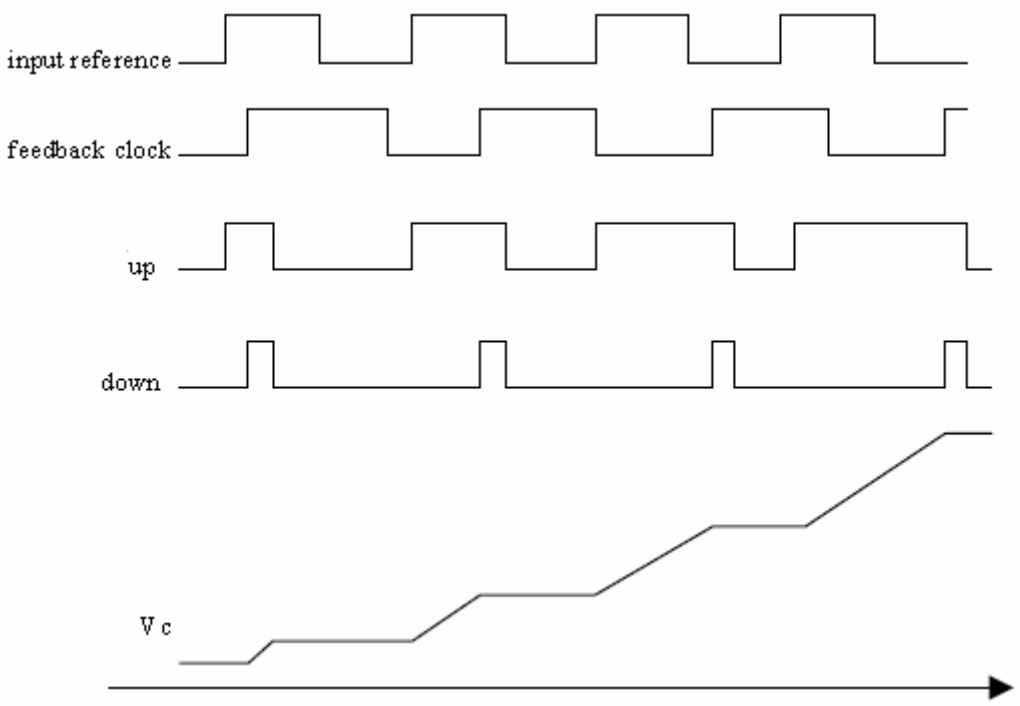

Figure 2-11 The response of charge PFD & pump & Loop Filter

The above discussions of the Figure 2-11 only use a capacitor as the loop filter. But this kind of filter makes the PLL unstable. We can use the loop filter which was shown in Figure 2-10(B), Figure 2-10(C) to avoid instability.

2-3-3 Voltage Controlled Oscillator

In this section, we will describe the voltage-controlled oscillator which is the critical circuit in the PLL. The input voltage of the VCO generated from the loop filter and the output frequency signal of VCO is controlled by the input voltage. In some oscillators, the frequency of the oscillator is controlled by a current rather then a voltage.

They are referred as current-controlled oscillators (CCO) and play the same role as those of VCOs in PLLs. The VCO and CCO are similar. Of course, there are various types of VCO than can be used in PLLs. The Table 2-1 show three various types of VCO. Basically, the VCO has to fulfill some constraints is the phase noise in the frequency domain or the timing jitter in the time domain. Other important factors are the bandwidth of the VCO, linearity of the controlled voltage, output voltage swing and the power consumption.[2.4][2.5][2.6]

Type	Advantage	Disadvantage
Voltage controlled crystal oscillators	Phase accuracy, good noise performance	Cannot be integrated and cost is high and low frequency
Ring oscillator VCOs	Suitable for integration and have wide control range	Poor jitter performance
LC-tuned oscillators	High frequency and good noise performance	The inductor is difficult to integrate and cost high

Table 2-1 The advantage and disadvantage of different type oscillators

Some of the most important considerations of VCO are: [2.7]

(1)Phase Stability:

The frequency spectrum of a VCO output should look likes an ideal impulse, i.e., the phase noise of a VCO must be as low as possible.

(2)Electrical Tuning Range:

The tunable frequency range of a VCO must be able to cover the entire required frequency range of the interested application.

(3) Tuning Linearity:

An ideal VCO has a constant gain at the entire frequency range. Also, a constant VCO gain can simplifies the design procedure of a VCO.

(4) Power Supply Sensitivity:

Since there are many digital circuits in a modern transceiver circuit, the switching activities of digital circuits will somewhat influence the power supply of the whole system. The switching noise induced by digital circuits will also couple to the power supply of the VCO and influence its output waveform. Therefore, in VCO the dependency of the oscillating frequency on the power supply must be as low as possible.

(5) Frequency pushing:

The dependency of the center frequency on the power supply voltage.

(6) Frequency pulling:

The dependency of the center frequency on the output load impendence.

(7) Low cost, Phase noise, DC consumption current, Harmonic/spurious

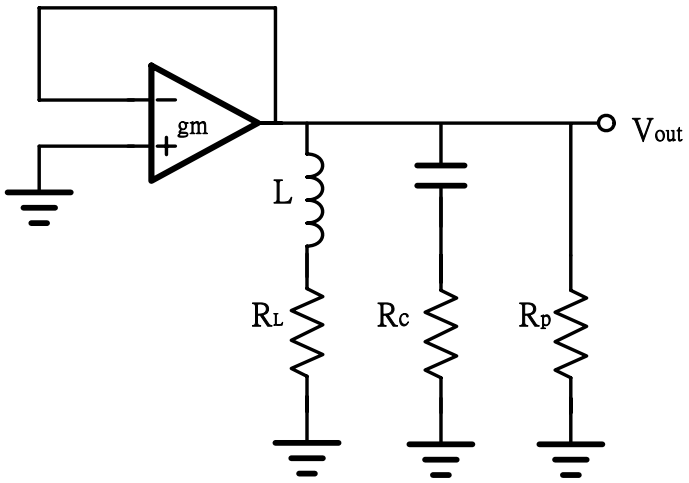

Figure 2-12 LC-Tank Voltage-Controlled Oscillator

In the next, we will show an LC-Tank VCO, relaxation oscillator and ring oscillator in the Figure 2-12, Figure 2-13 and Figure 2-17. [2.6] In the LC-Tank VCO, the oscillation conditions are already shown by [2.6]. Where R_P is the parasitic resistance in parallel to the LC-tank, and R_L and R_C are the parasitic resistances of L and C, respectively.

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.10}$$

$$R_{eff} = R_c + R_L + \frac{1}{R_P \cdot (\omega_0 C)^2} \tag{2.11}$$

$$G_M = R_{eff} (\omega_0 C)^2 = \frac{R_{eff}}{(\omega_0 L)^2} \tag{2.12}$$

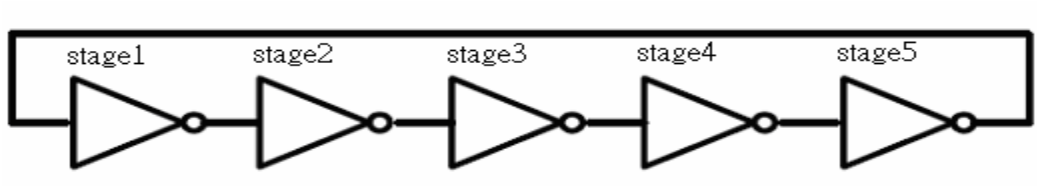

Figure 2-13 Five stage signal ended ring oscillator

The second type oscillator is ring oscillator as shown in Figure 2-13 has been widely used in PLL for application of clock recovery and clock generation before and Figure 2-14 shows the detail circuit of the Figure 2-13.

A ring oscillator can be smoothly integrated in a standard CMOS process without taking extra processing steps because it dose not require any passive resonant element.

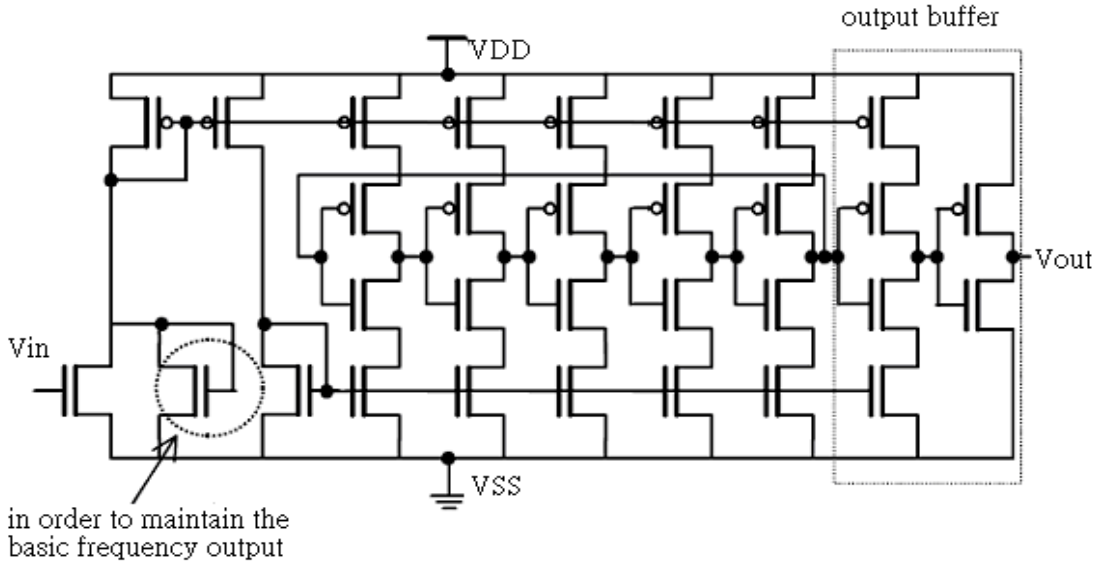

Figure 2-14 Detail five stages circuit in Figure 2-13

When the ring oscillator is employed as a voltage controlled oscillator, the desired wide operating frequency range can be easily obtained. Different output frequency is achieved by adjusting the timing delay of each stage in the ring oscillator.

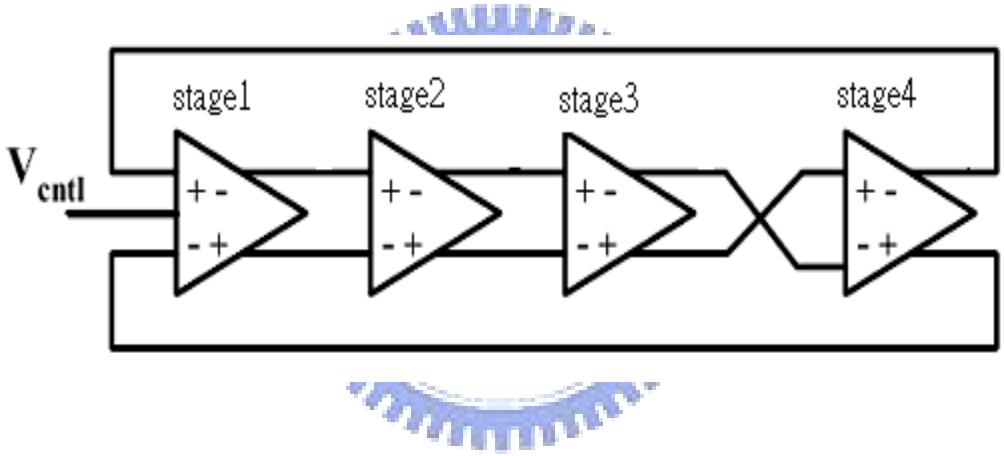

Figure 2-15 Differential Ring Oscillator

Also, there is another type of ring oscillator, differential ring oscillator, as shown in Figure 2-15.The detail circuit of Figure 2-15 show in the Figure 2-16.

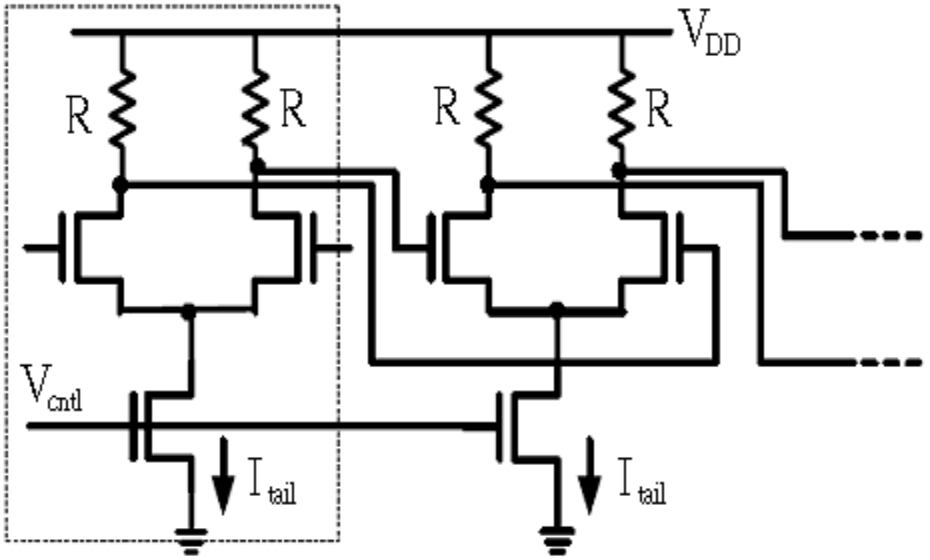

Figure 2-16 The circuit of each stage in Figure 2-15

The third type oscillator is the relaxation oscillator, it shows in the Figure 2-17. The relaxation oscillator is also known as multivibrator, incorporating hysteresis characteristics that can oscillate even with a small phase shift. The relaxation oscillator and ring oscillator utilize the positive feedback characteristics and are known as resonatorless oscillators. [2.8]

The other category of oscillator is to eliminate that the real part of the loop's impedance so that the poles are pure imaginary. The LC-tank VCO is a typical resonator oscillator that bases on the idea and is called resonator oscillator. The VCO is the most challenging part of the PLL and we have to design carefully.

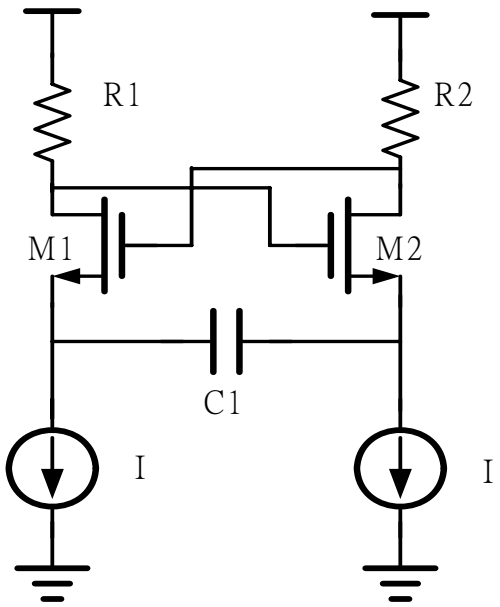

Figure 2-17 The relaxation oscillator

2-3-4 Frequency Divider

In some application, we need a high frequency clock generator and the crystal-oscillator is not satisfied, because the frequency of the crystal-oscillator is too small. Therefore, the multiple-frequency-technology that utilizes PLL is presented. For example, the divider module is four. The output frequency of VCO is a four times of the input reference signal's frequency, i.e.,

$$f_{out} = N f_{in} \quad , \quad N = 4 \tag{2.13}$$

$$f_{out} = 4 f_{in} \tag{2.14}$$

The Figure 2-18 show an example of divider, it uses a TSPC register. The next is the advantages and the disadvantages of the divider:

Advantages:

Reasonably fast

No static power consumption

Compact size

Differential clock not require

Disadvantages:

Slowed down by stacked PMOS, signals goes through three gates per cycle

Requires full swing input clock signal

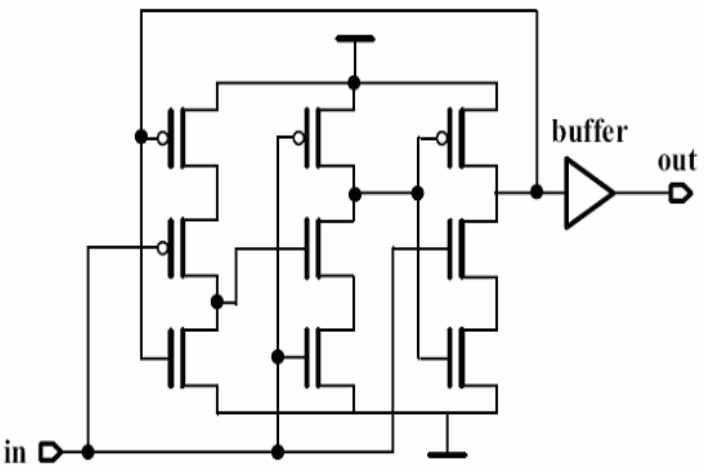

Figure 2-18 Divide-by-2 using a TSPC register

If we need higher division, it can be achieved by simple cascading divide-by-2 stages.

The Figure 2-19 shows a divider (1/4) waveform.

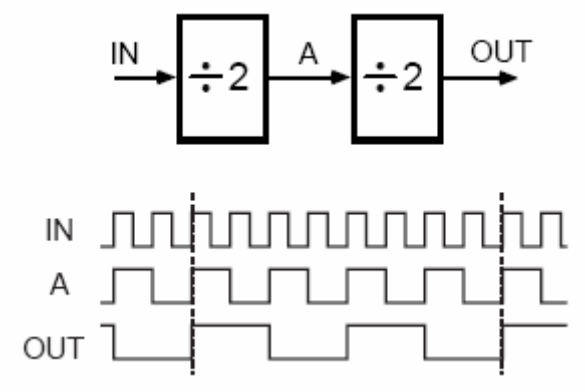

Figure 2-19 A divider (1/4) waveform

2-4 All Digital PLL

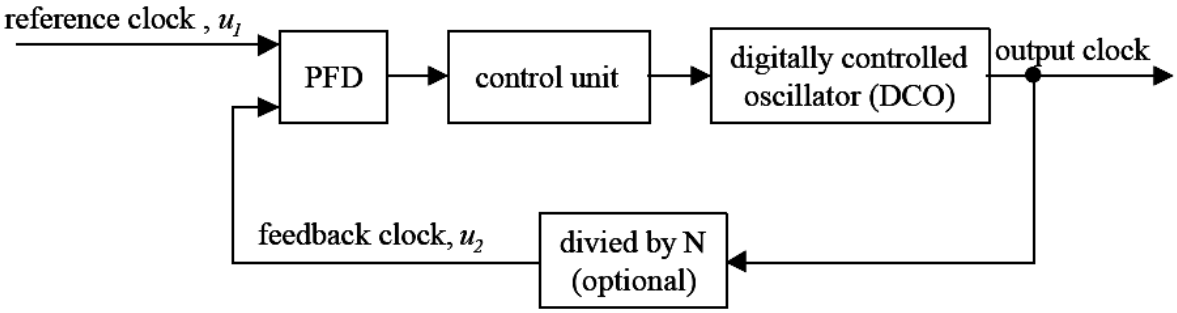

Figure 2-20 All Digital Phase-Locked Loop

In this section we will describe All Digital PLL, it has characteristics of fast frequency locking, full digitization and good stability. Because of the availability of low-cost ADPLL ICs, this type of PLL can replace the classical DPLL in many

applications today. The ADPLL is made as a digital building block, it dose not contain any passive component, such as resistors and capacitors.

The ADPLL consists of a digital phase frequency detector (PFD), a control unit, a frequency divider, and digital control oscillator (DCO) as show in Figure 2-20. All signals in the ADPLL are digital signals. The PFD detects the frequency difference and the phase difference between the input reference signal and the feedback signal. The control unit receives the signal, produced by the PFD, and produces a set of digitally controlled signals to control the DCO.

By including a divide-by-N divider in the feedback path, the DCO output frequency runs N times faster than input reference signal. The divided-by-N divider is an optional component in the ADPLL. The functional blocks of the ADPLL imitate the function of the corresponding analog blocks. Because the ADPLL consists of digital circuits entirely, there are many different of design methods to achieve the functions of them.

The ADPLL system is a discrete-time system, hence analyzing the ADPLL in s-domain is not suitable. Although it is possible to take an entire PLL-description and then transform it from s-domain into z-domain, this is unnecessary difficult. Instead, one transforms each component into z-domain and then proceeds with the analysis in z-domain. The ADPLL is best described in z-domain.

In the Linear PLL, Digital PLL and All Digital PLL, they have many advantages and disadvantages respectively. We compare and illustrate them in Table 2-2.As show in the Table 2-2, we can know they use different design methodology, because the

ADPLL is a digital circuit design so it can be designed by standard cell library.

Hence the ADPLL just need a short design cycle. The analog circuits take much time to design, so they take long turnaround time. The ADPLL has higher noise immunity than LPLL and DPLL. The VCO of the LPLL or the DPLL produces a continuous frequency band but the DCO of the ADPLL produces a discrete frequency band, so the VCO has higher resolution than DCO. In general, the digital circuits have lower power consumption than analog circuits. The ADPLL have a less power consumption. Because the loop filter of LPLL or DPLL has one or more large capacitors, whose area can not be efficiently reduced as the process technology improving. In the ADPLL, the area depends on which type of DCO we design and the area of DCO also depends on how many bits we design. The ADPLL shorten lock time by dealing with digital signal.

	LPLL	DPLL	ADPLL
Design Methodology	Analog	Mixed mode	Digital
Design cycle	Slow	Slow	Fast
Noise rejection	Poor	Poor	Good
Output frequency	High	High	Low
Oscillator resolution	High	High	Low
Lock cycle	Slow	Slow	Quick
Power consumption	Large	Large	Small
Area	Large	Large	Design dependent

Table 2-2 The advantage and disadvantage of different type PLL

The design of PLL is a trade-off jitter performance, frequency resolution, phase resolution, lock-in time, area cost, power consumption, circuit complexity and design cycle. It is hard to design one PLL suitable for all applications. For fast-locking frequency synthesizer applications, such as a frequency hopping multiple access system, the lock-in time is the most critical design issue. And for portable or mobile applications, lock-in time is also very important since the PLL must support fast entry and exit from power management techniques.

In traditional analog PLL designs, fast acquisition requires tuning of the VCO free-running frequency near the desired the frequency in advance or to increase loop bandwidth. But increasing the loop bandwidth degrades jitter performance, and the extra VCO tuning range is not easy to be achieved since there always has process variations, voltage variations, and temperate variations (PVT variations). We list some design issues about ADPLL as following table.

Digital Controlled Oscillator	The output clock of DCO is discrete, so the resolution of a DCO should be sufficiently high to maintain acceptable jitter. For searching target frequency and phase easily and efficiently, a DCO had better approach a monotonic response to the control word. A DCO had better have high noise immunity, so the output clock will not induce large jitter.
Phase Frequency Detector	The resolution of a PFD had better be as high as

	possible. In this way, the PFD can detect tiny phase difference to promote accuracy and to decrease jitter. The PFD had better have two properties simultaneously. One is to judge the modulating direction. The other is to judge the modulating magnitude.
Control Unit	Control Unit receives the signal, produced by the PFD, and produces signal to the DCO. It works as a loop filter. It both decides the speed of the lock process and suppresses the high frequency noise to reduce jitter. All responses of an ADPLL are almost decided by this control unit.

Table 2-3 Design issues of ADPLL

■ Chapter 3 Proposed Low power Digitally Controlled Oscillator

At the heart of the ADPLL is a digitally controlled oscillator because it affects many important specifications of the ADPLL, like maximum operating frequency, operating frequency range and jitter. Like most voltage-controlled oscillators the DCO consists of a frequency-control mechanism within an oscillator block. In this section, we will discuss basic concepts of digitally controlled oscillator, some type of digitally controlled oscillators and the concept of low power digitally controlled oscillator.

3-1 Basic Concepts of Digitally Controlled Oscillator

The fundamental function of a DCO is to provide an output waveform, typically in the form of square wave, which has a frequency of oscillation f_{DCO} that is a function of a digital input word D, as follows:

$$f_{DCO} = f(D) = f\left(d_{n-1} 2^{n-1} + d_{n-2} 2^{n-2} + \cdots + d_1 2^1 + d_0 2^0 \right) \quad (3.1)$$

Typically, the DCO transfer function $f(\cdots)$ is defined so that either the frequency f_{DCO} or the period of oscillation T_{DCO} is linear with D, generally with an offset. For example, a DCO transfer function that is linear in frequency is typically expressed as:

$$f(D) = f_{offset} + D \cdot \Delta f \quad (3.2)$$

where f_{offset} is constant offset frequency and Δf is the frequency quantization step.

Similarly, a DCO transfer function that is linear in period is typically expressed as:

$$T(D) = T_{offset} + D \cdot \Delta T \qquad (3.3)$$

Where T_{offset} is constant offset period and ΔT is the period quantization step. It is evident that, since the DCO period T(D) is a function of quantized digital input D, the DCO can not generate a continuous range of frequencies. In this regard, the quantization granularity of the DCO period sets some fundamental limits on the achievable jitter of an all-digital PLL. It is of course desirable to have a fairly small quantization step size (e.g. period quantization step ΔT)

3-2 Digitally Controlled Oscillator(DCO)

An odd number of inverters connected in a circular chain become a ring oscillator. The clock period of the ring oscillator is two times the loop delay time. There are two parameters to modulate the clock period of the ring oscillator. One is the variable propagation delay time of the inverter, and the other is the number of the inverter. Hence, based on tuning these two Parameters with different method, there are many methods to design DCO.

1)Variable Propagation Delay Time of the inverter

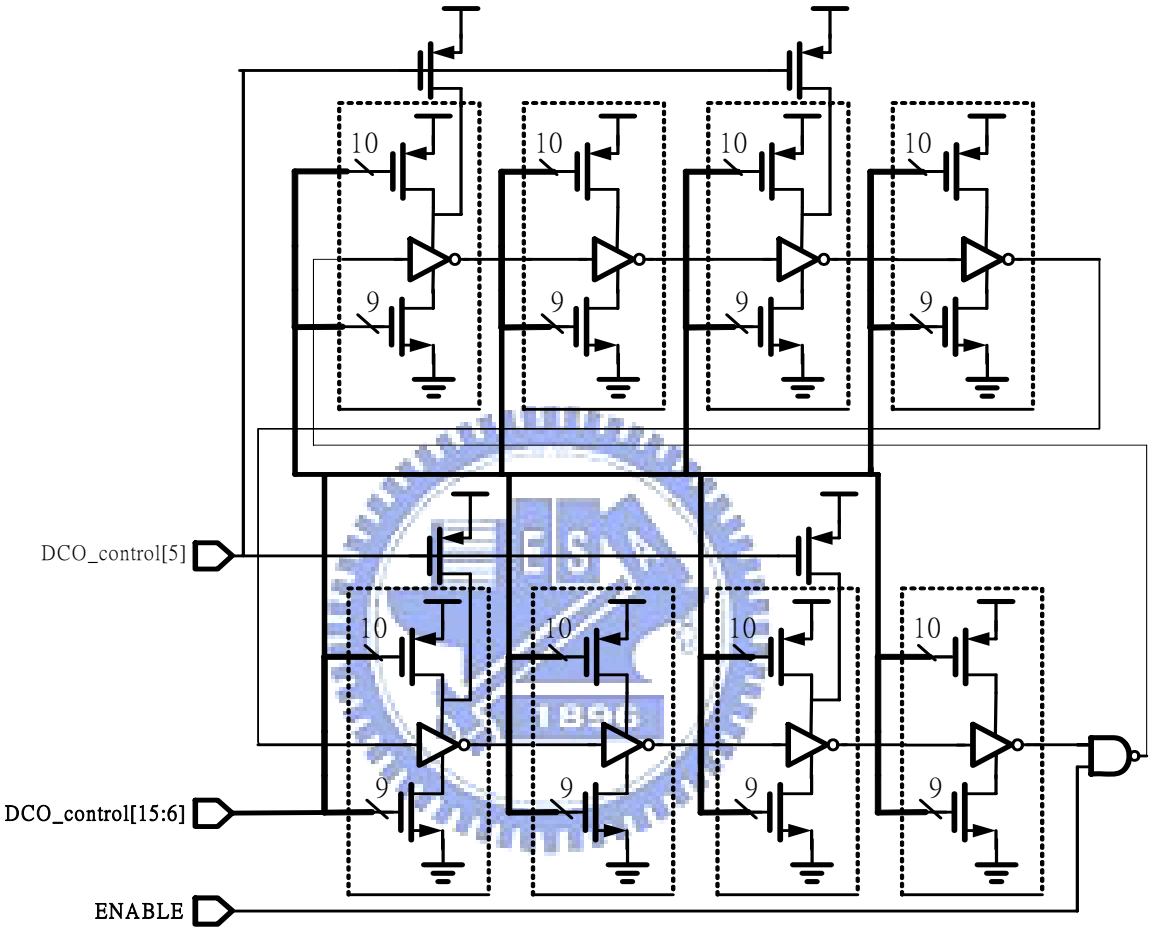

Figure 3-1 Digitally Controlled Oscillator [3.1]

As show in the Figure 3-1, it is a conventional DCO proposed by Motorola in 1995[3.1]. The ADPLL control the frequency through the DCO control word, the output of the register consisting of some binary weight control signals. The DCO is a ring oscillator with odd inverting stages. There are one enabling NAND gate and eight

controllable cells in the DCO. In order to provide sufficient DCO control word resolution to maintain acceptable jitter, Motorola also uses several techniques to increase number of the control word. The control devices in a cell have binary-weighted widths, as shown by the constituent cell in Figure 3-2.

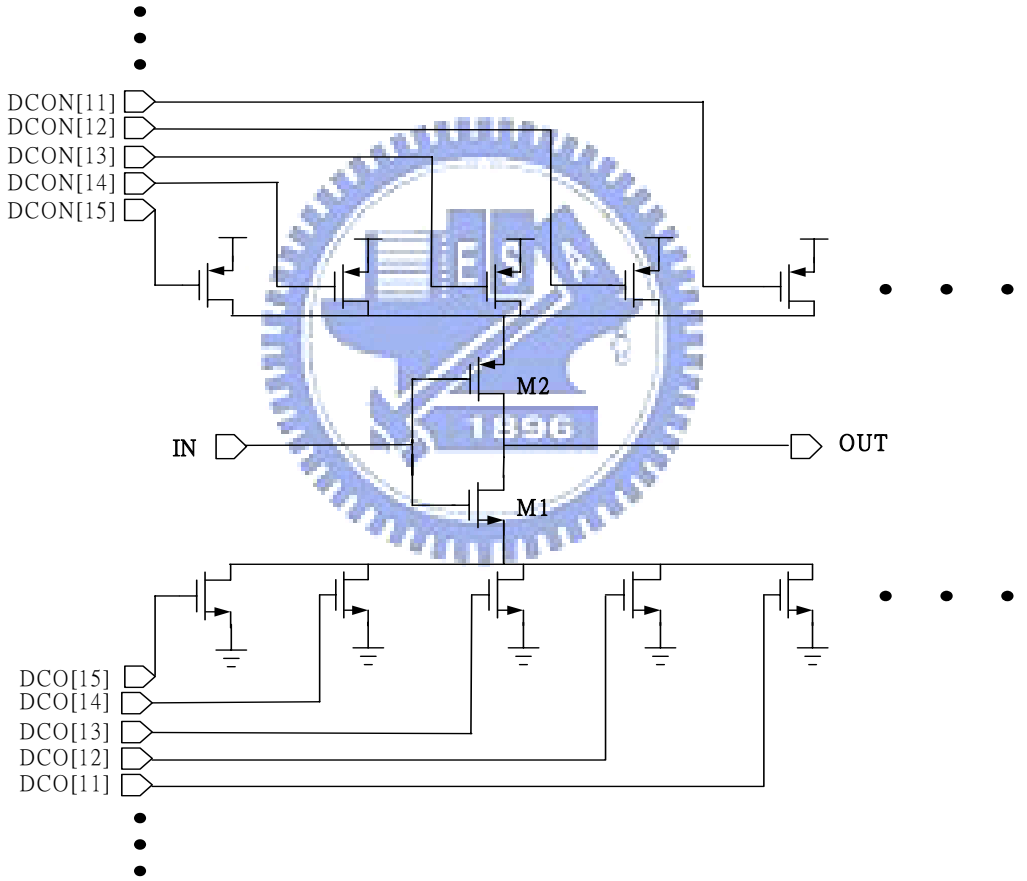

Figure 3-2 The DCO cell [3.1]

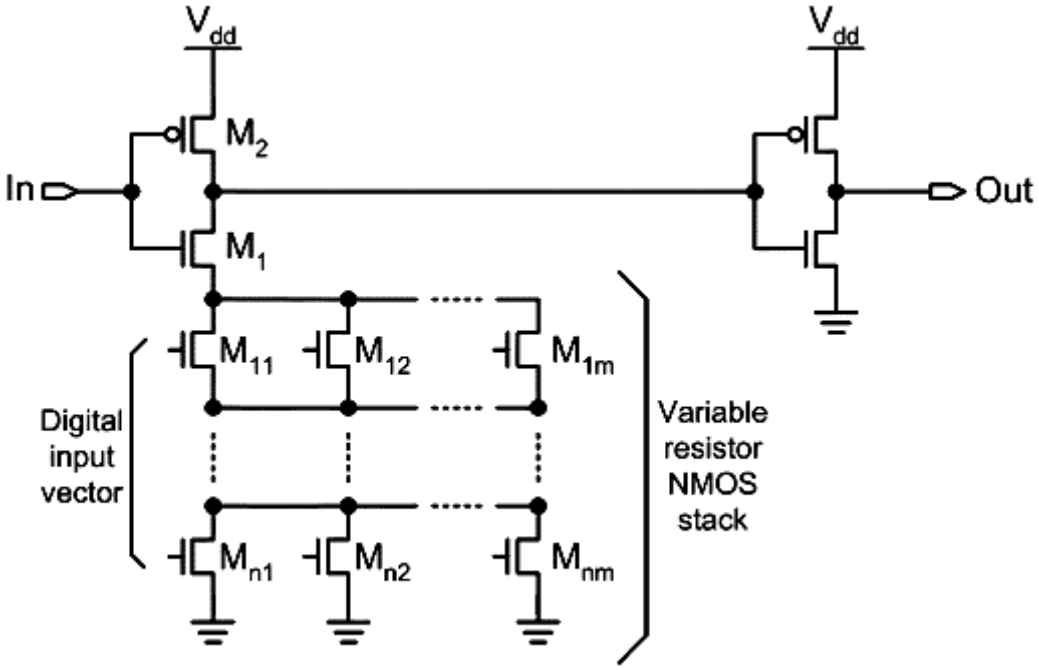

Figure 3-3 Another delay element [3.6]

Fig. 3-3 illustrates another technique for implementing a Variable Propagation Delay Time of inverter. In this circuit, a variable resistor is used to control the delay. A stack n of rows by m columns of nMOS transistors is used to make the variable resistor. This resistor subsequently controls the delay of M1. In the circuit of Fig. 3-3, only the rising edge of the Out can be changed with the input vector. Another stack of pMOS transistors can be used at the source of the pMOS transistor, M2, to have control over the delay of the falling edge.

One of the problems with the above mentioned architectures is the nonmonotonic delay behavior with ascending binary input pattern. As can be seen in the circuits of Figs. 3-2 and 3-3, the input vector changes the effective resistance of transistor(s) placed at the source of the nMOS or pMOS transistors of the first inverter. This not only changes the resistance at the source of or , but also changes the parasitic

capacitance associated with transistors at these nodes. This is because the parasitic capacitance at the drain of a MOSFET is different in the ON and OFF states. Therefore, there are two factors which depend on the input vector and affect the delay[3.6]:

The resistance of the controlling transistor: By increasing/ decreasing the effective ON resistance of the controlling transistor(s) at the source of M1(M2), the circuit delay can be increased/decreased.

The effective parasitic capacitance of the controlling transistor: As the effective capacitance of the controlling transistors at the source of M1(M2) increases due to the input vector, the charge sharing effect causes the capacitance at the output of the current-starved inverter to be (dis)charged faster and the overall delay of the circuit decreases.

The DCO shows in the Figure 3-4[3.4], it describes a possible full-custom implementation of the DCO. A common solution for designing the DCO is to make it as a combination of a D/A converter and VCO. To control the frequency of the VCO, each voltage at node Vn(0) …Vn(6) and Vp(0) …Vp(6) is separately controlled using 14 small D/A converters. So the input of this DCO is also a digital type. To start the VCO at a know state, a pull-down transistor controlled by the signal “Reset” is added. When Reset signal is high, the voltage Vp(6) is set high to prevent a short circuit from occurring.

Figure 3-5 shows the corresponding simulated period time versus digital control word for the D/A –VCO combination [3.4]. Simulated period time versus digital

control word for the D/A converter combination using linear D/A converter is also givens as comparison. Using custom-made D/A converters gives the opportunity to linearize the oscillator by using nonlinear D/A converters. Since the loop gain of the PLL is proportional to △T/T, a completely linear DCO is not the best solution. Instead, effort is made to keep the ratio △T/T constant. To achieve this, a set of control voltage is preliminary calculated. The main source of power consumption for the D/A-VCO is from the D/A converter.

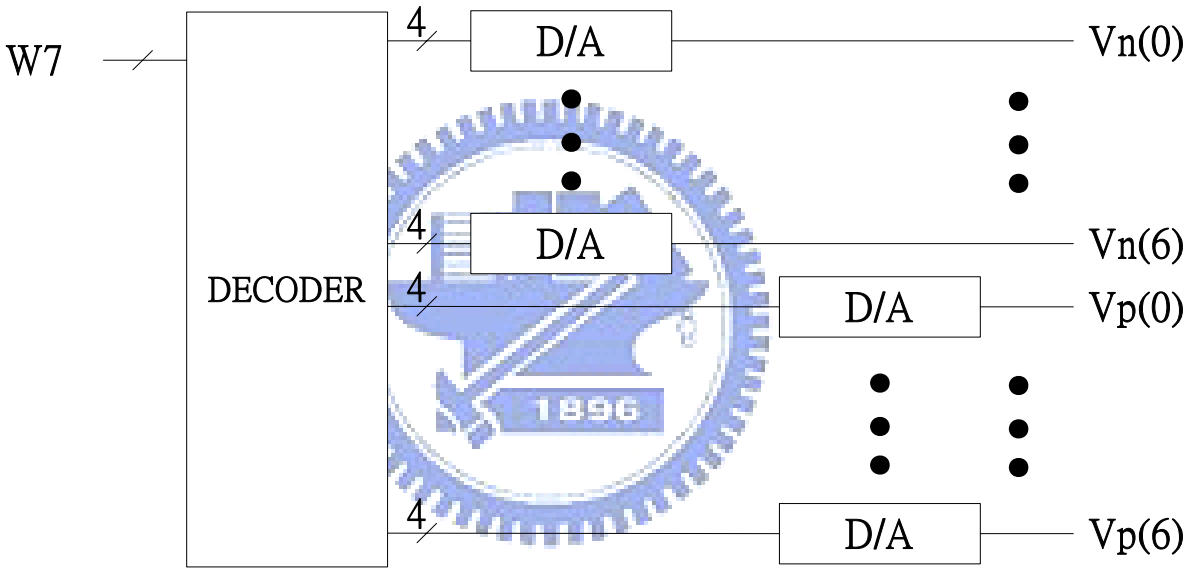

Figure 3-4 (A) DCO consisting of 14 D/A converters and a current-starved inverter VCO [3.4]

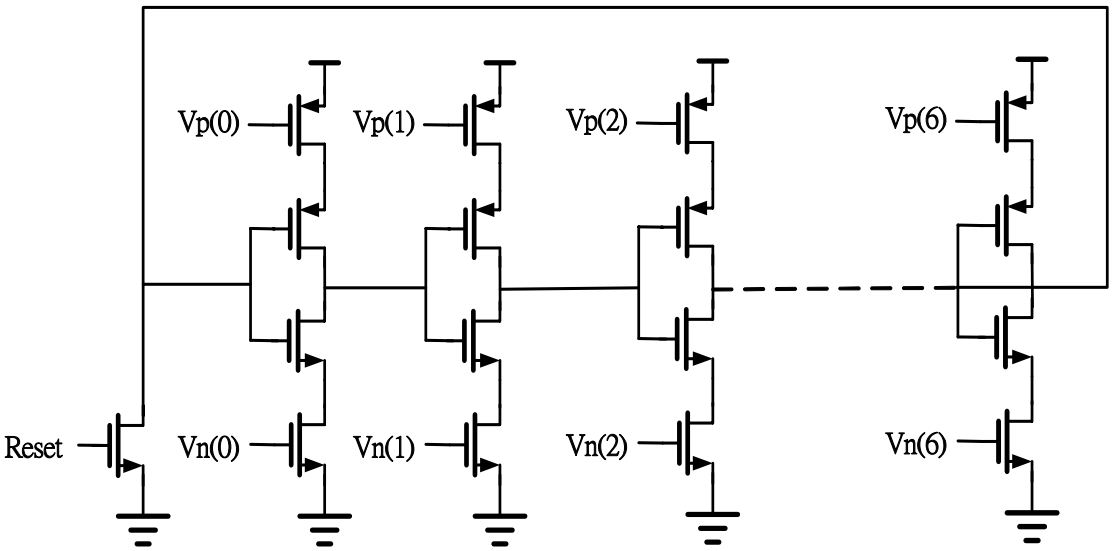

Figure 3-4 (B)DCO consisting of 14 D/A converters and a current-starved inverter

VCO [3.4]

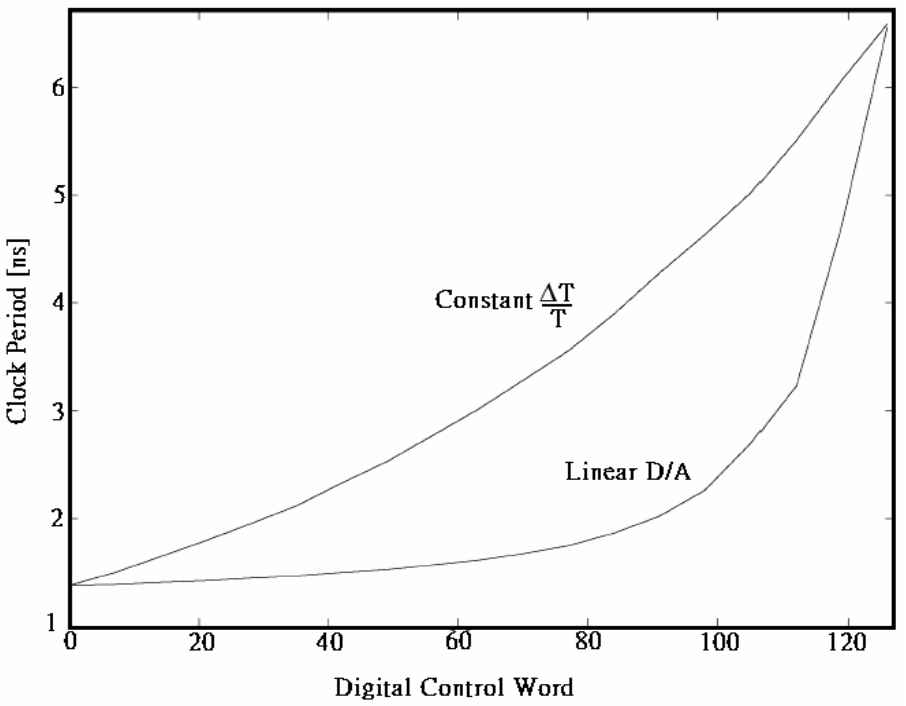

Figure 3-5 Simulated period time versus digital control word W

for the DCO of Figure 3-4 [3.4]

Figure 3-6 [3.5] was shown a 4 bits DCO circuit which consists of a D/A converter and an injection-locked oscillator. The main advantages of Figure 3-6 circuit are its simple structure, high resolution and good linearity. The circuit is composed of an injection-locked oscillator (ILO) consisting of MOS transistors M1-M9 and a simple four bits digital controlled current source consisting of MOS transistors M10-M15.

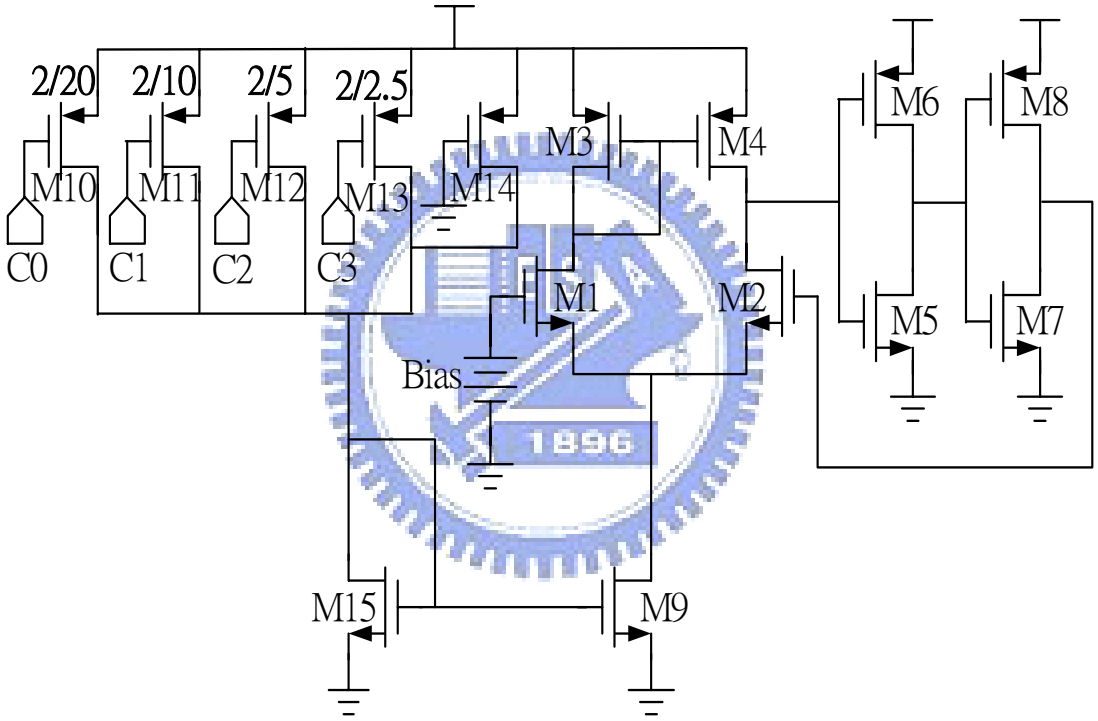

Figure 3-6 Schematic diagram of a 4 bits DCO [3.5]

In the absence of an input signal, the ILO oscillates at its free running frequency just like a ring oscillator. Its free running frequency is primarily determined by the total propagation delay time of the differential comparator and the inverter chain. The

current output from the D/A is used to bias the differential comparator. Thus, the propagation delay of the comparator is directly proportional to the digital control word.

$$f_{out} = \frac{1}{D_1 + D_2} \tag{3.3}$$

The delay of the comparator is designed to be much larger then the delay of the inverter chain to increase the sensitivity and linearity of the DCO. The output frequency is mainly determined by the sums of two terms, the delays of the comparator and the inverter chain, and these delays can be presented by D1 and D2 respectively. The relation between D1 and D2 was shown in the equation (3.3).

2) Different number of the inverter

As show in Figure 3-7, it is a multiple path selection DCO with a delay matrix [3.2]. When searching frequency, the path selection works as coarse search and the delay matrix works as fine search. The delay matrix consists of many parallel tri-state inverters. The operating range is determined by number of cascade inverters, and the resolution is decided by scale of delay matrix. Because the standard cells have the problem of accuracy, this multiple path selection DCO uses a parallel structure with matrix encoder to prove accuracy.

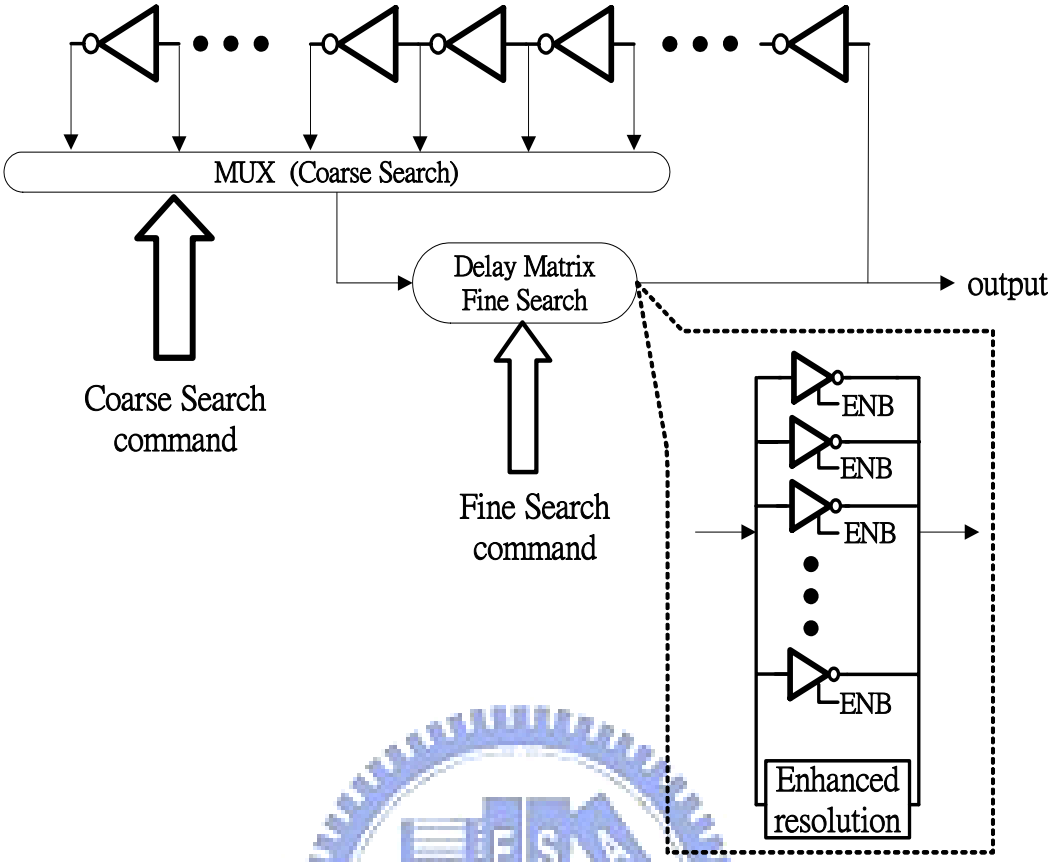

Figure 3-7 A multiple path selection DCO [3.2]

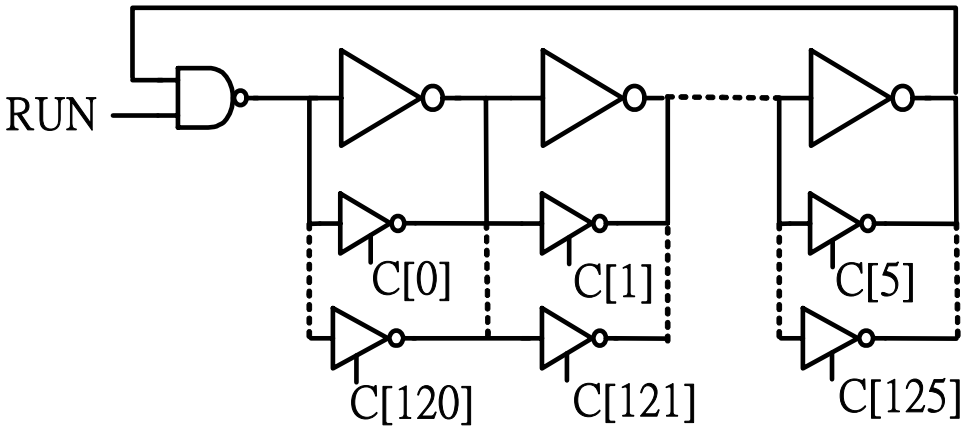

Figure 3-8 Numerically controlled oscillator [3.3]

In Figure 3-8[3.3], it shows a numerically controlled oscillator (NCO) and it is made from standard cells. To change the frequency of the ring oscillator, a set of 21 inverting tri-state gates are connected in parallel with each inverter. When the tri-state gates are enabled additional current drive is added to each inverter stage. The 126 tri-state gates are controlled by a 126 bit vector, C, which is decoded from a 7 bit control word. Although this NCO is made from standard cells, it has relative power consumption, low maximum frequency from high capacitive load in the ring oscillator.

The Figure 3-9 shows the result of the simulation in Figure 3-8. Due to fewer parallel tri-state inverters per stage in the ring oscillator, aside from having evenly distributed clock phases, also performs better both in terms of linearity and maximum clock rate. In Figure 3-10, the DCO consists of path selection with AO gates and delay matrix with several parallel inverters. Its structure is similar to that in Figure 3-7.

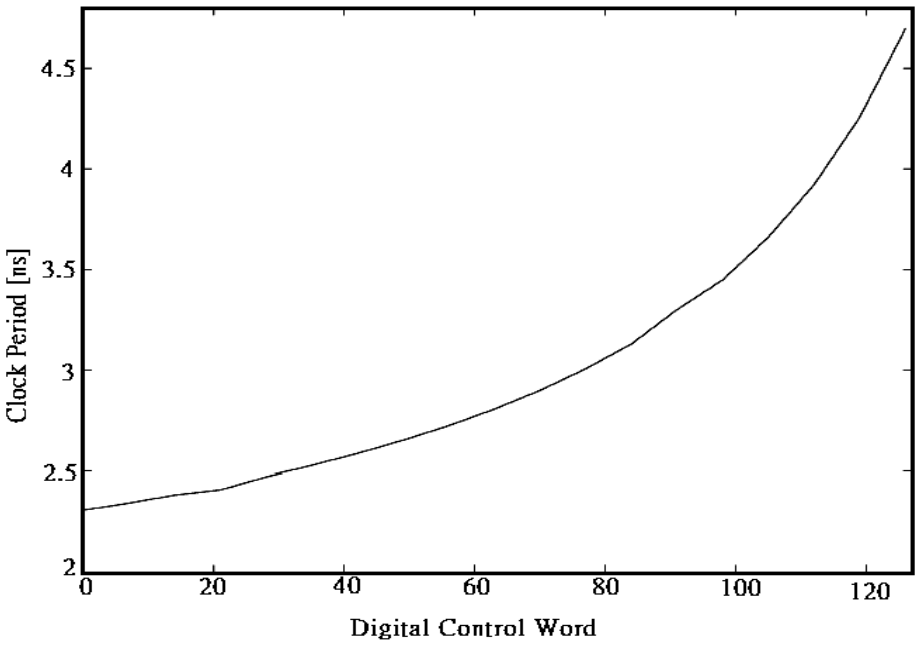

Figure 3-9 The simulated period time V.S. digital controlled word in Figure 3-8.

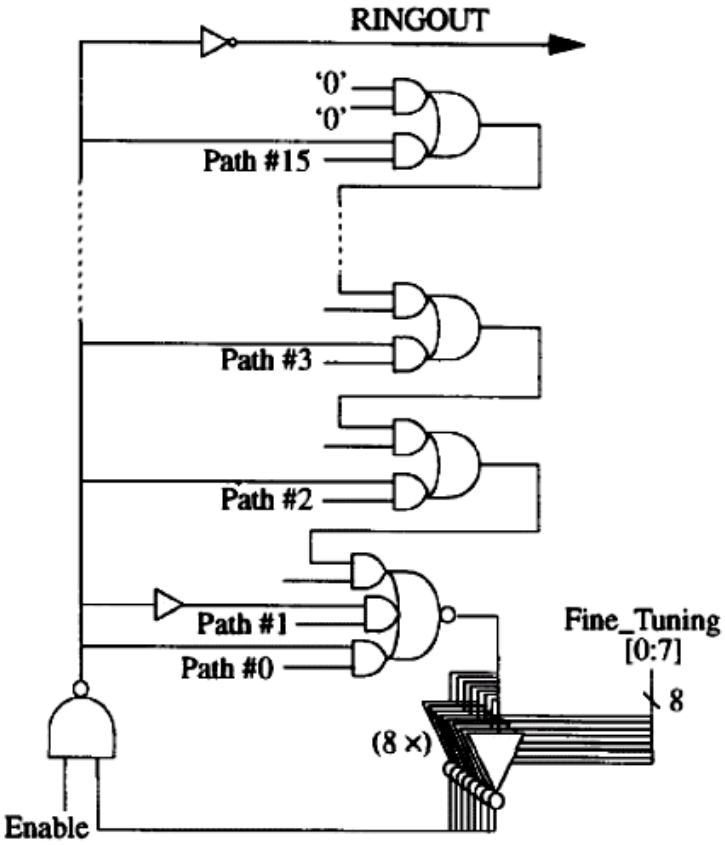

Figure 3-10 Structure of DCO in [3.7].

Power consumption with above mentioned different number of the inverter is a serious problem. Use more inverters to oscillate the target frequency will result more charging and discharging and it will waste power. In the other word, the technique exchange power for resolution (range). So next section we will introduce my proposed low power DCO.

There are many kinds of digitally controlled oscillators. Different kinds of digitally controlled oscillator have different advantages. There are some issues to design digitally controlled oscillator. First, the output frequency of the DCO is

discrete, so the resolutions of the DCO should be sufficiently high, the sufficiently high resolution to maintain acceptable jitter. Second, the DCO had better approach a monotonic response to the DCO control word. Third, a DCO had better high noise immunity, so the output clock will not induce larger jitter. However, no matter which kinds of oscillator we use, we should check our design conform to these issues or not.

3-3 Proposed Low Power Digitally controlled Oscillator

Last section, we talk about two kinds of digitally controlled oscillator. One is digitally controlled delay time and the other is digitally controlled number of the inverter. If you want to design a low power digitally controlled oscillator, you can` t choose the second type to do. The reason is that the more inverters you use, the more charging and discharging should be resulted. So proposed digitally controlled oscillator will use controlled delay time technique to design.

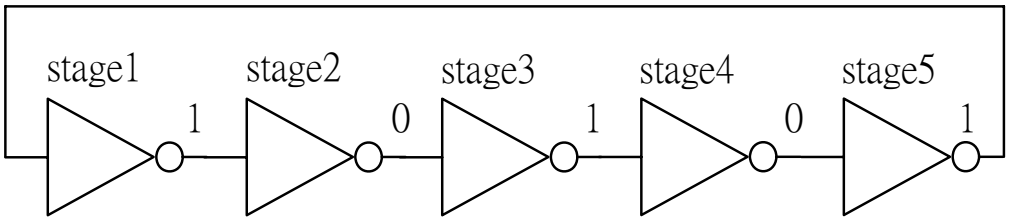

Figure 3-11(a) five stages inverter oscillator

In digital aspect, the logic values of both stage1/stage3 output is the same. The signal just passes through stage2 and stage3 with a certain delay time, so we cancel the two inverters (stage2 and stage3) to reduce power. But Changing five stages

inverter for three stages inverter changes delay time (frequency) from long (slow) to short (high), too. If we want that both the delay time (frequency) are the same and power is low, we can use some delay element in three stages inverter oscillator to increase delay time to make the both delay time the same. The most of digitally controlled oscillator use inverter chain to be coarse tune. It makes very much unless charging / discharging nodes and increases uncontrolled intrinsic delay time (like equation 3.3 T_{offset}). Figure 3-7is an example.

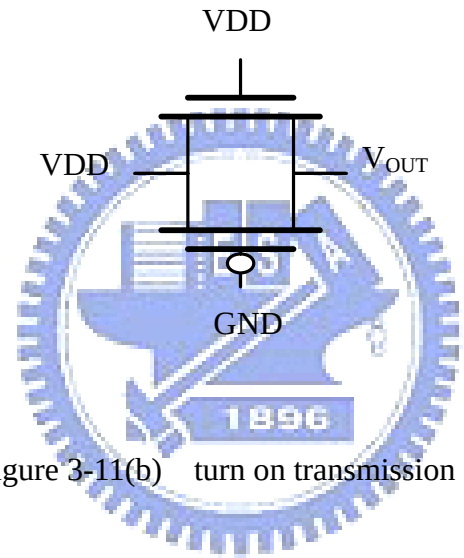

Figure 3-11(b)　turn on transmission gate

So, we can find some delay elements just passed signal to be coarse tune circuit. The proposed digitally controlled oscillator use transmission gates to be coarse tune circuit. Choosing transmission gate has three reasons. First, it full swings; doesn't affect next stage inverter charging/discharging. Second, when inverter charges, the resistance of transmission gate from 0V to 1.2V is almost the same. So we can easily calculate it` s RC delay. In Figure 3-11(b) for low values of *Vout*, the NMOS device is saturated and the resistance is approximated as:

$$R_n = \frac{V_{DD} - V_{out}}{I_N} = \frac{V_{DD} - V_{out}}{k'_n \left(\frac{W}{L}\right)_N \left((V_{DD} - V_{out} - V_{Tn}) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right)}$$

$$\approx \frac{V_{DD} - V_{out}}{k_n (V_{DD} - V_{out} - V_{Tn}) V_{DSAT}}$$

(3.4)

The resistance goes up for increasing values of *Vout*, and approaches infinity when *Vout* reaches *VDD-VTn*, this is when the device shuts off. Similarly, we can analyze the behavior of the PMOS transistor. When *Vout* is small, the PMOS is saturated, but it enters the linear mode of operation for *Vout* approaching *VDD*. The resistance then approximated by:

$$R_p = \frac{V_{DD} - V_{out}}{I_P} = \frac{V_{DD} - V_{out}}{k'_p \left(\frac{W}{L}\right)_P \left((-V_{DD} - V_{Tp})(V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2} \right)}$$

$$\approx \frac{1}{k_p (V_{DD} - |V_{Tp}|)}$$

(3.5)

The simulated value of *Req* = *Rp* || *Rn* as a function of *Vout* is plotted in Figure 3-12. It can be observed that *Req* is relatively constant. The same is true in other design instances (for instance, when discharging *CL*). When analyzing transmission-gate networks, the simplifying assumption that the switch has a constant resistive value is therefore acceptable.[3.8]

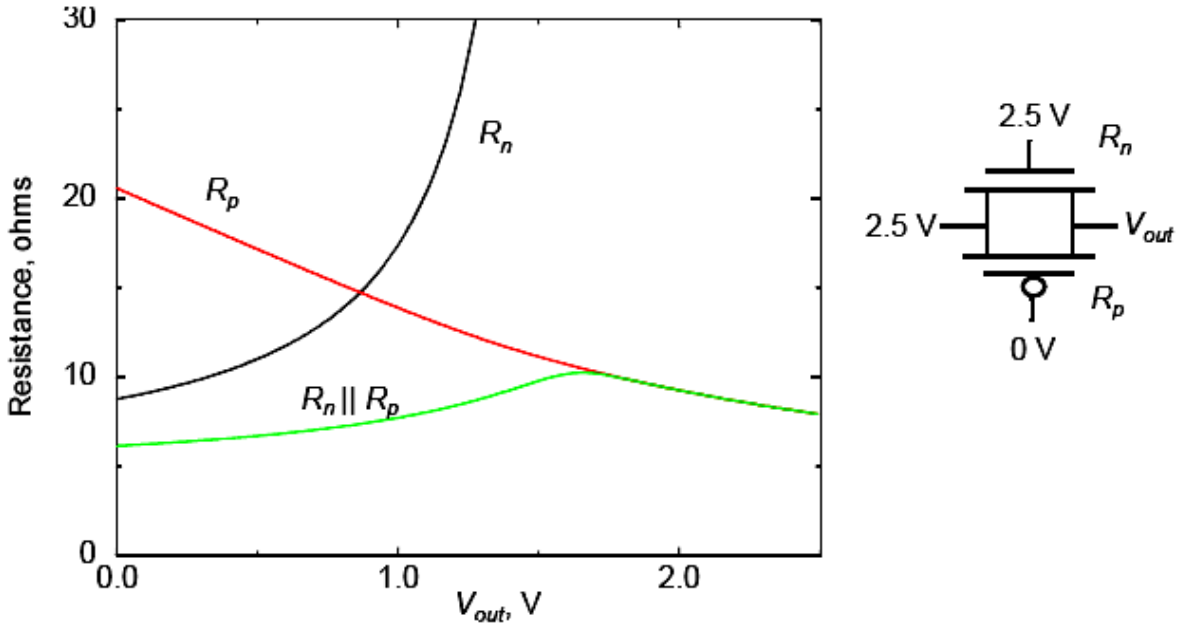

Figure 3-12 Simulated equivalent resistance of transmission gate for low-to-high transition (for $(W/L)n = (W/L)p = 0.5mm/0.25mm$).

A similar response for overall resistance is obtained for the high-to-low transition. Next, we calculate the resistance of transmission gate from high to low.

In Figure 3-12 for high values of *Vout* (high-to-low),the resistance goes up for decreasing values of *Vout*, and approaches infinity when *Vout* reaches *VDD*-|*VTp*|, this is when the device shuts off. Similarly, we can analyze the behavior of the NMOS transistor. When *Vout* is high, the NMOS is saturated, but it enters the linear mode of operation for *Vout* approaching *GND*. The resistance then approximated by:

$$R_n = \frac{V_{out}}{I_N} = \frac{V_{out}}{k'_n \left(\frac{W}{L}\right)_N \left((V_{DD} - V_{Tn}) V_{out} - \frac{V_{out}^2}{2} \right)} \approx \frac{1}{k_n (V_{DD} - V_{Tn})} \tag{3.6}$$

The PMOS device is saturated and the resistance is approximated as:

$$R_p = \frac{V_{out}}{I_P} = \frac{V_{out}}{k'_p \left(\frac{W}{L}\right)_P \left((V_{out} - |V_{Tp}|) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right)} \approx \frac{V_{out}}{k_p (V_{out} - |V_{Tp}|) V_{DSAT}} \tag{3.7}$$

The *Req* for high-to-low transition is lower than low-to-high transition. It's response is like making Figure 3-12 symmetry with y-axis. Next, we will talk about how to make both the same.

If we want the clock of DCO to be duty cycle, we need to make both rising (low-to-high) and falling (high-to-low) the same. According to RC delay equation (*DelayTime* = *RC*), we should let rising resistance and falling resistance be equal. In Table 3-1, we simulate transmission gate with different size.

Size	Rising(ns)	Falling(ns)
Wp=0.6um Wn=0.2um	0.314	0.2080
Wp=0.7um Wn=0.2um	0.253	0.2082
Wp=0.8um Wn=0.2um	0.216	0.2083
Wp=0.9um Wn=0.2um	0.190	0.2088

Table 3-1 Transmission gate simulation with different size

(TSMC 0.13um C=10fF Lp=Ln=0.13um).

According to Table 3-1, when Wp/Wn is almost 4.5 , rising time equals falling time.

Third, according to Table 3-1, we can see that for increasing Wp, it just only influences rising time. In the other word, different width does not affect the driving ability of inverter which drive transmission gate. It only changes equivalent rising/falling resistance. When we choose number of conducting transmission gate, the transmission gate based DCO has monotonic characteristic. So, proposed digitally controlled oscillator (DCO) is based on different number of conducting transmission gate.

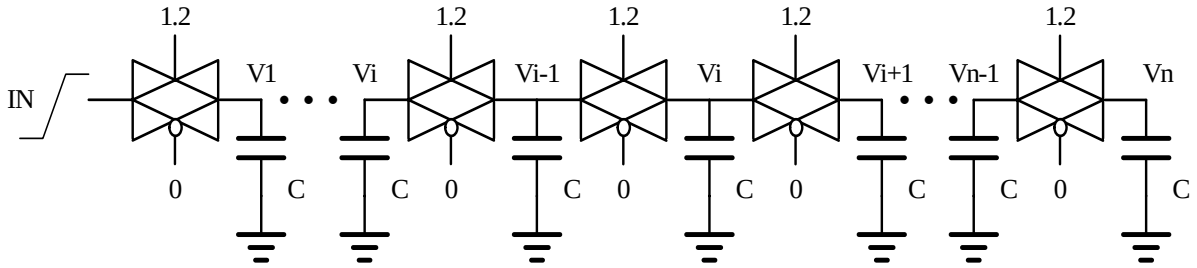

Figure 3-13 (a) A chain of transmission gates

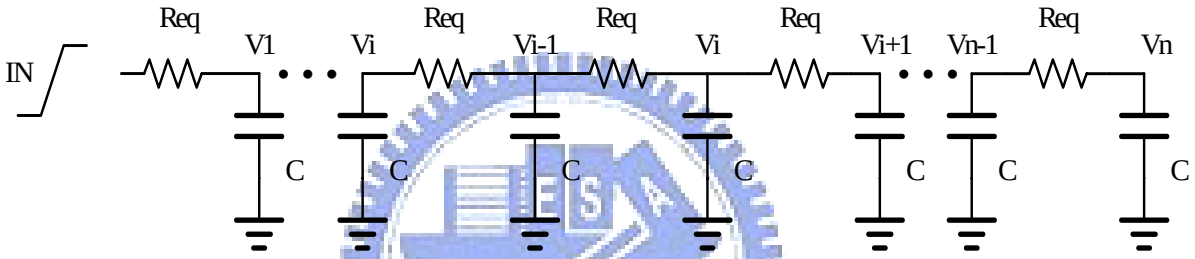

Figure 3-13 (b) Equivalent *RC* network

Now, we talk about the delay time of a chain transmission gate. Figure 3-13 (a) shows a chain of *n* transmission gates. Figure 3-13 (b) shows the transmission gate replaced by equivalent resistance. The exact analysis of delay is not simple, but as discussed earlier, we can estimate the dominant *time constant* at the output of a chain of *n* transmission gates as follows:

$$\tau(Vn) = \sum_{k=0}^{n} CR_{eq}\, k = CR_{eq}\, \frac{n(n+1)}{2} \qquad (3.8)$$

Equation 3.8 means that the delay time is proportional to n^2 and increase rapidly with the number of transmission gates. Proposed DCO architecture is two step, coarse tune and fine tune. If the difference of coarse tune cell delay time between each step is too big, the overall fine tune cell number must be more. Overall fine tune cell delay time increases and overall fine tune cell area increases, too. Choosing appropriate cascade transmission gate number is more important. So, in my proposed digitally controlled oscillator, we choose two-bit controlled signal and have four different number of transmission gate. According to table 3-1, we choose Wp=0.9um, Wn=0.2um. We proposed two architectures below and we will discuss them.

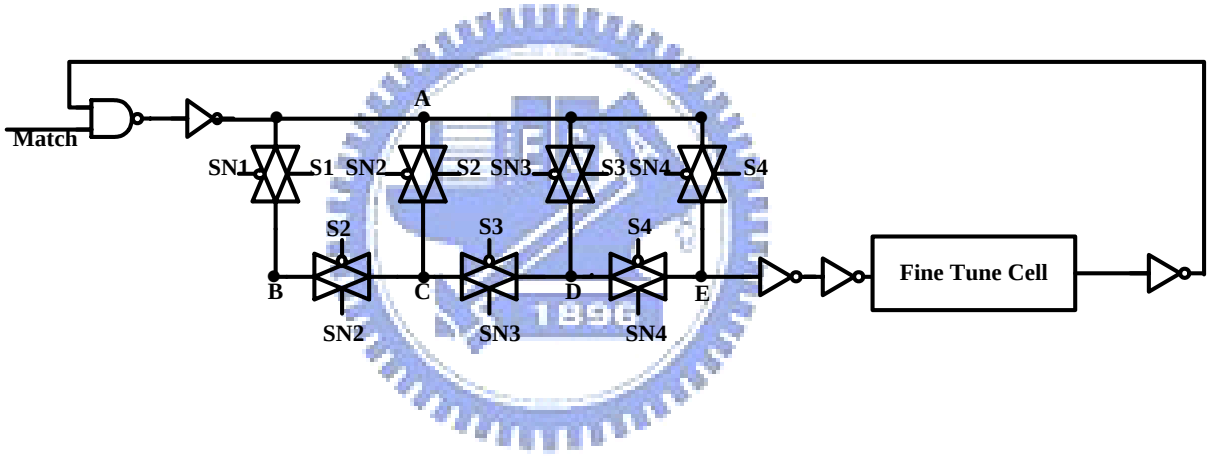

Figure 3-14 (a) Type-1 DCO

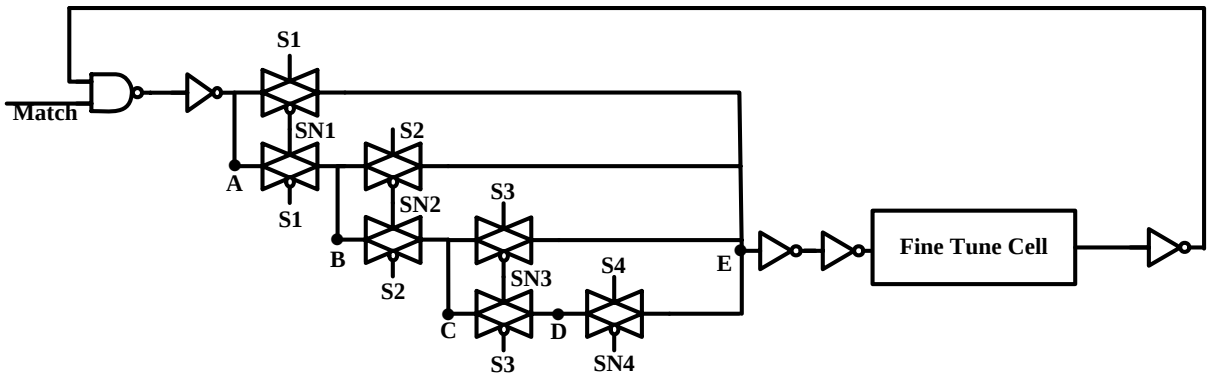

Figure 3-14 (b) Type-2 DCO

As increasing number of series transmission gate, we get delay time, CReq 3CReq 6 CReq 10 CReq • • • . Because delay time increase rapidly, we choose four transmission gate to design. In Figure 3-14, shows two proposed Type-1 and Type-2 DCO. Both Type-1 and Type-2 are controlled by two bits. Next, we will talk about the difference between them.

In Figure 3-14 (a), node A capacitance is bigger than B, C, D and E. In Figure 3-15 (b), node E is bigger than A, B, C, and D. In Figure 3-14, we can see that the charging/discharging resistance between Type-1 node A and Type-2 node E is not the same. Type-1 node A resistance is the output of last inverter. If we choose path 4 open (signal pass through A, B, C, D and E), Type-1 node A resistance is the output of last inverter and Type-2 node E resistance is the output of last inverter and 4 Req (transmission gate resistance). The difference will make Type-2 intrinsic delay time big. The big intrinsic delay time will make the DCO frequency slow. So, if we want high speed, we should choose type-1 DCO.

Above, we talked about that as increasing number of series transmission gate, delay time increase rapidly. Now we introduce the tip we reduce the amount of increasing. First, we let two transmission gates be shunt. Figure 3-15 shows the architecture of Type-1 shunt transmission gate and it` s equivalent circuit. Figure 3-16 shows the architecture of Type-2 shunt transmission gate and it` s equivalent circuit.

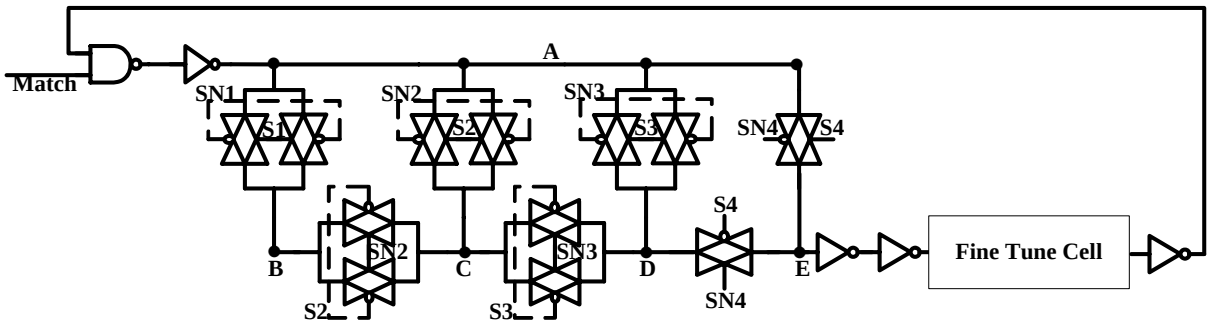

Figure 3-15 (a) Type-1 shunt transmission gate

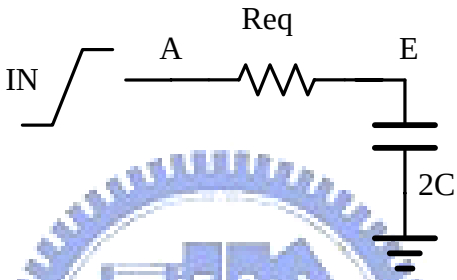

Figure 3-15 (b) Path 1 (AE) equivalent circuit

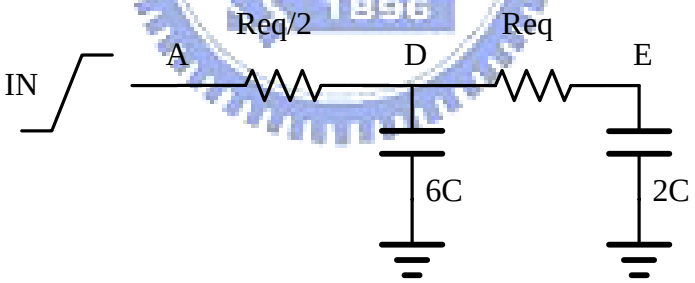

Figure 3-15 (c) Path 2 (ADE) equivalent circuit

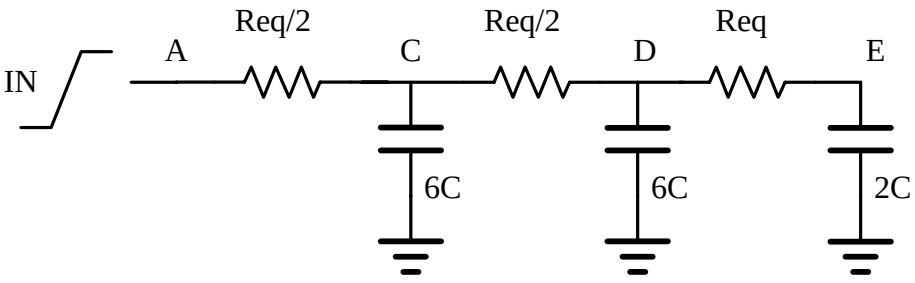

Figure 3-15 (d) Path 3 (ACDE) equivalent circuit

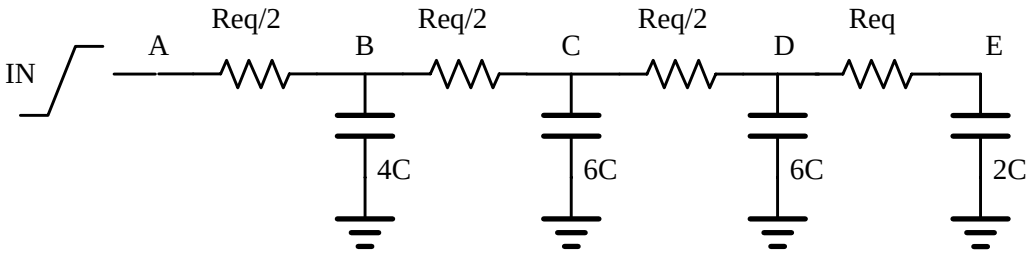

Figure 3-15 (e) Path 4 (ABCDE) equivalent circuit

Equation (3.9) is Figure 3-15(b) in mathematics

$$\tau_{p1} = \mathrm{Re}\, q * 2C \tag{3.9}$$

Equation (3.10) is Figure 3-15(c) in mathematics

$$\begin{aligned}\tau_{p2} &= (\frac{1}{2}\mathrm{Re}\ q) * 6C + (\frac{3}{2}\mathrm{Re}\ q) * 2C \\ &= \tau_{p1} + \frac{1}{2}\mathrm{Re}\ q * 6C + \left(\frac{1}{2}\mathrm{Re}\ q * 2C\right)\end{aligned} \tag{3.10}$$

Equation (3.11) is Figure 3-15(d) in mathematics

$$\begin{aligned}\tau_{p3} &= (\frac{1}{2}\mathrm{Re}\, q) * 6C + (\mathrm{Re}\, q) * 6C + (2\,\mathrm{Re}\, q) * 2C \\ &= \tau_{p2} + \mathrm{Re}\, q * 6C + \left(\frac{1}{2}\mathrm{Re}\, q * 2C\right)\end{aligned} \tag{3.11}$$

Equation (3.12) is Figure 3-15(e) in mathematics

$$\begin{aligned}\tau_{p4} &= (\frac{1}{2}\mathrm{Re}\,q)*4C + (\mathrm{Re}\,q)*6C + (\frac{3}{2}\mathrm{Re}\,q)*6C + (\frac{5}{2}\mathrm{Re}\,q)*2C \\ &= \tau_{p3} + \frac{3}{2}\mathrm{Re}\,q*6C + \left(\frac{1}{2}\mathrm{Re}\,q*2C\right)\end{aligned} \tag{3.12}$$

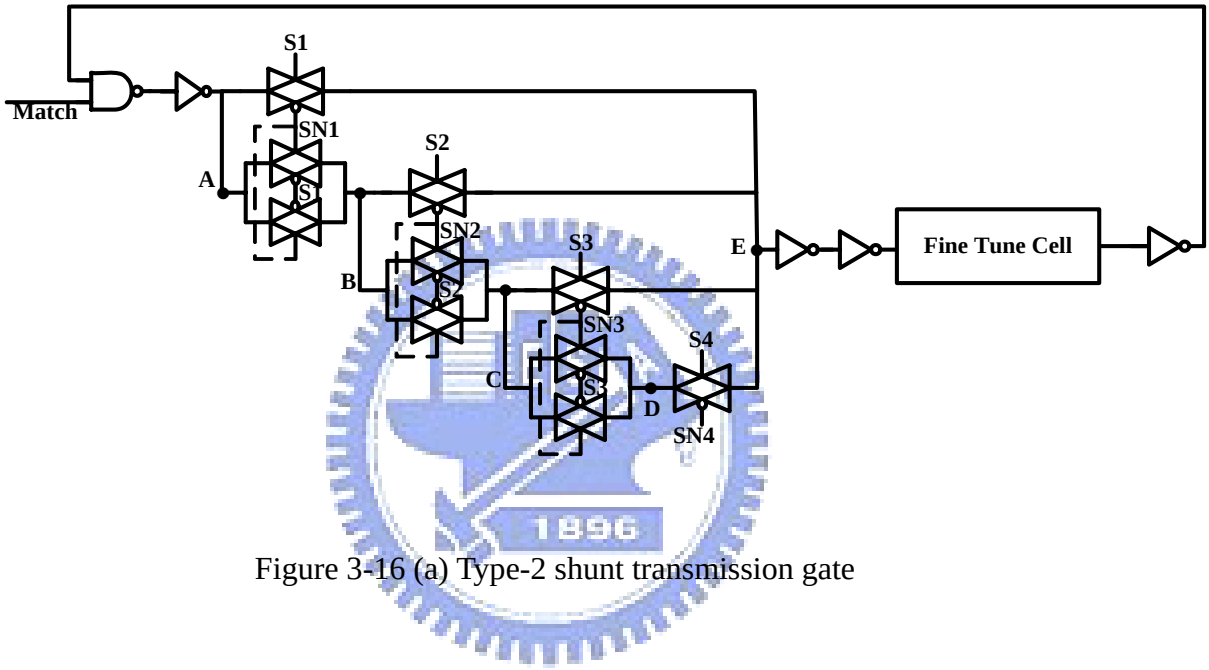

Figure 3-16 (a) Type-2 shunt transmission gate

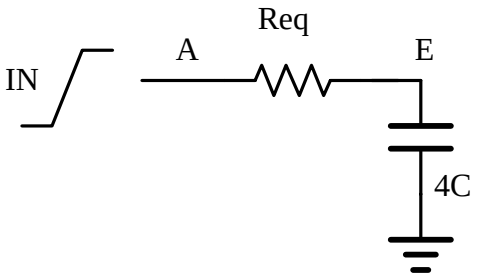

Figure 3-16 (b) Path 1 (CE) equivalent circuit

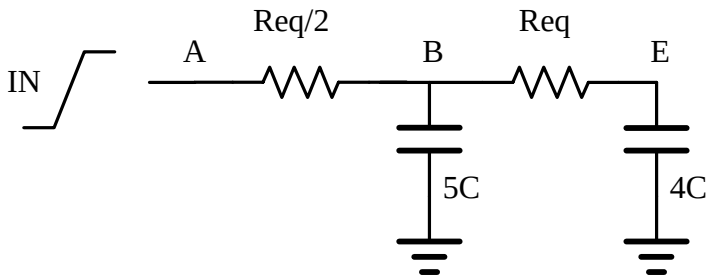

Figure 3-16 (c) Path 2 (CDE) equivalent circuit

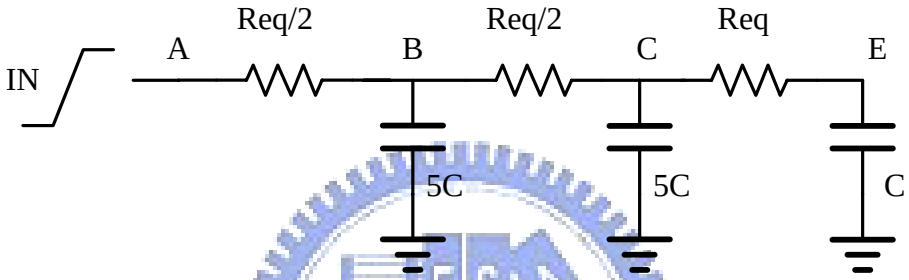

Figure 3-16 (d) Path 3 (BCDE) equivalent circuit

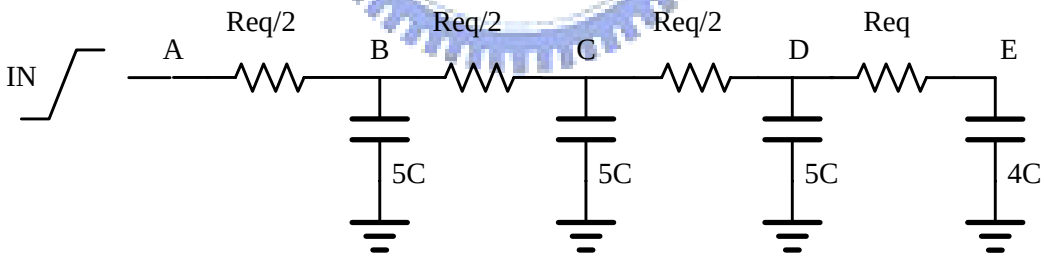

Figure 3-16 (e) Path 4 (ABCDE) equivalent circuit

Equation (3.13) is Figure 3-16(b) in mathematics

$$\tau_{p1} = (\mathrm{Re}\, q) * 4C \qquad (3.13)$$

Equation (3.14) is Figure 3-16(c) in mathematics

$$\begin{aligned}\tau_{p2} &= (\frac{1}{2}\operatorname{Re} q)*5C + (\frac{3}{2}\operatorname{Re} q)*4C \\ &= \tau_{p1} + \frac{1}{2}\operatorname{Re} q*5C + \left(\frac{1}{2}\operatorname{Re} q*4C\right)\end{aligned} \tag{3.14}$$

Equation (3.15) is Figure 3-16(d) in mathematics

$$\begin{aligned}\tau_{p3} &= (\frac{1}{2}\operatorname{Re} q)*5C + (\operatorname{Re} q)*5C + (2\operatorname{Re} q)*4C \\ &= \tau_{p2} + \operatorname{Re} q*5C + \left(\frac{1}{2}\operatorname{Re} q*4C\right)\end{aligned} \tag{3.15}$$

Equation (3.16) is Figure 3-16(e) in mathematics

$$\begin{aligned}\tau_{p4} &= (\frac{1}{2}\operatorname{Re} q)*5C + (\operatorname{Re} q)*5C + (\frac{3}{2}\operatorname{Re} q)*5C + (\frac{5}{2}\operatorname{Re} q)*4C \\ &= \tau_{p3} + \frac{3}{2}\operatorname{Re} q*5C + \left(\frac{1}{2}\operatorname{Re} q*4C\right)\end{aligned} \tag{3.16}$$

Now, we list a table to show the different by changing delay path.

Type-1	With shunt	Without shunt
Path 1 to Path 2	$3\,\mathrm{Re}\,qC+(\mathrm{Re}\,qC)$	$3\,\mathrm{Re}\,qC+(2\,\mathrm{Re}\,qC)$
Path 2 to Path 3	$6\,\mathrm{Re}\,qC+(\mathrm{Re}\,qC)$	$6\,\mathrm{Re}\,qC+(2\,\mathrm{Re}\,qC)$
Path 3 to Path 4	$9\,\mathrm{Re}\,qC+(\mathrm{Re}\,qC)$	$9\,\mathrm{Re}\,qC+(2\,\mathrm{Re}\,qC)$

Table 3-2 the increment of Type-1 with and without shunt

Type-2	With shunt	Without shunt
Path 1 to Path 2	$\frac{5}{2}\mathrm{Re}\,qC+(2\,\mathrm{Re}\,qC)$	$3\,\mathrm{Re}\,qC+(4\,\mathrm{Re}\,qC)$
Path 2 to Path 3	$5\,\mathrm{Re}\,qC+(2\,\mathrm{Re}\,qC)$	$6\,\mathrm{Re}\,qC+(4\,\mathrm{Re}\,qC)$
Path 3 to Path 4	$\frac{15}{2}\mathrm{Re}\,qC+(2\,\mathrm{Re}\,qC)$	$9\,\mathrm{Re}\,qC+(4\,\mathrm{Re}\,qC)$

Table 3-3 the increment of Type-2 with and without shunt

Compare Table 3-2 with Table 3-3, we can see that the Type-1 increment is not better than Type-2. In Table 3-3, the increment gets closer and gets smaller. If we let more transmission gates shunt, the difference is smaller. So we change Type-2 to shunt and don't change Type-1.

Above discussion, because Type-1 has small intrinsic delay, it is fit to a few of series transmission gate to make DCO high speed. Type-2 is fit to many of series transmission gate with shunt to make DCO to be wide range and another reason is that the shunt increment does not change too much. If the increment gets bigger and bigger, the fine tune cell must be more and more to fit the increment. So, we should choose receivable increment. Figure 3-17 is the overall DCO architecture. We use the drain-source MOS capacitance to be fine tune cell. The resolution is 2ps.

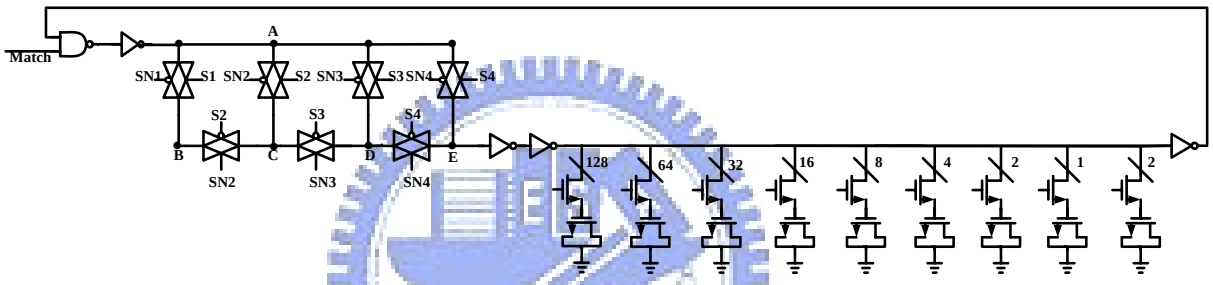

Figure 3-17 (a) Type-1 DCO

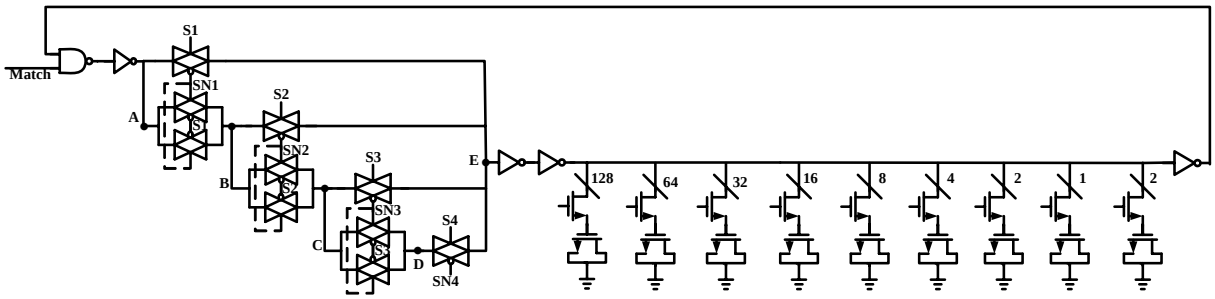

Figure 3-17 (b) Type-2 DCO

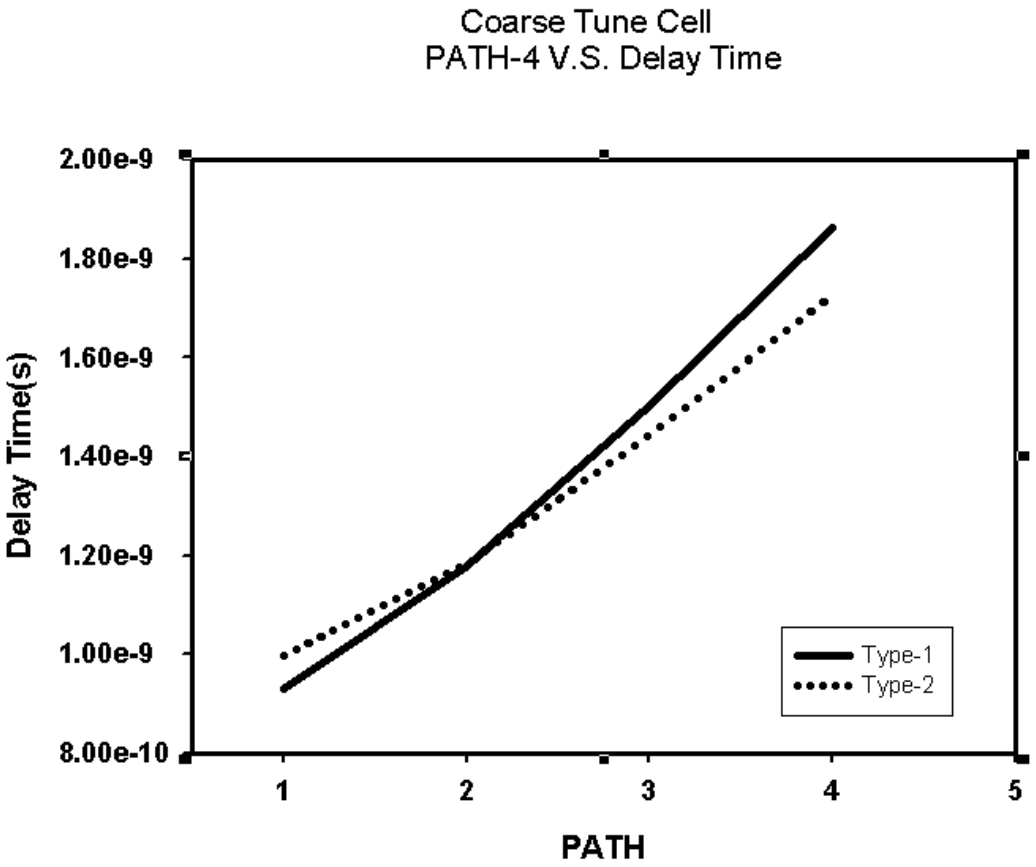

Figure 3-18 Type-1 DCO and Type-2 DCO simulation

Figure 3-18is Figure 3-17 simulation. It shows that Type-1 DCO is high speed, but the increment is bigger than Type-2 DCO. The highest frequency of Type-2 DCO is slower than Type-1. The slope of Type-1 DCO is bigger than Type-2 DCO. So, Type-1 DCO is fit to be high speed and Type-2 DCO is fit to be wide range. Figure 3-19 is the Path-8 Type-2 DCO simulation with the same number of Type-1 fine tune cell. The Path-8 Type-2 DCO range is bigger than Path-4 Type-1 DCO range but they have the same number of fine tune cell. In Figure 3-20, the fine tune cell is linear and the resolution is 2 ps.

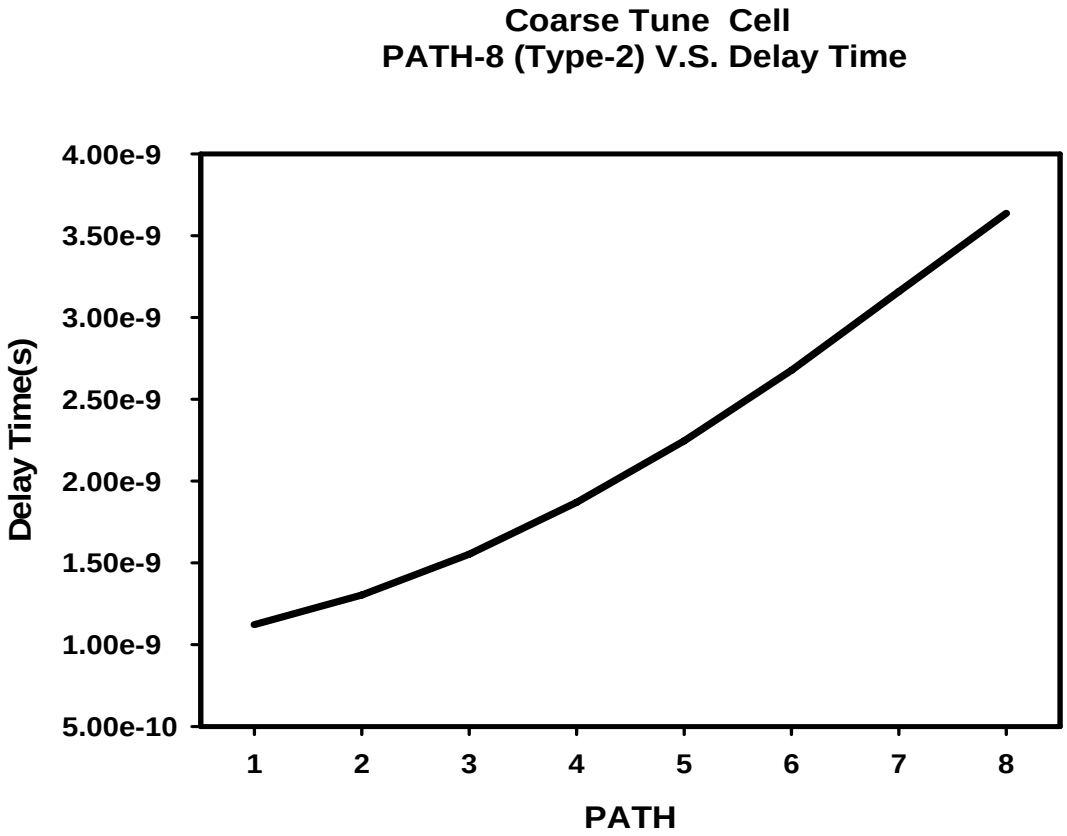

Figure 3-19 Path-8 Type-2 DCO simulation

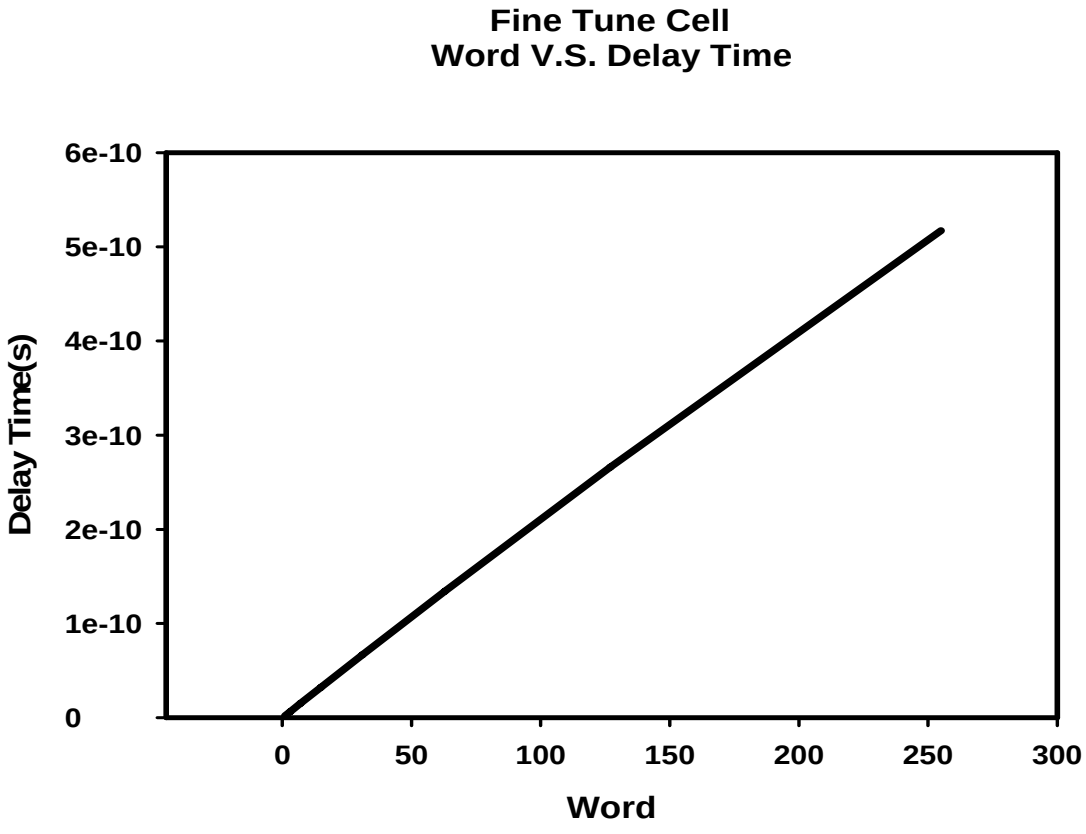

Figure 3-20 Fine Tune Cell simulaton

Table 3-4 shows that proposed DCO power is lower than the other very much.

The reason is：

1) Limiting the number of inverter to reduce dynamic power.

2) Using delay cell instead of using inverter to be coarse tune cell

Next chapter, we will introduce proposed ADPLL architecture.

$$Power\ Factor = Power \times \frac{0.13um}{\mathrm{Pr}\,ocess} \times \frac{1050MHz}{Frequency} \times \left(\frac{1.2V}{SupplyVoltage} \right)^2$$

	ISSCC 03 [3.10]	JSSC 03 [3.9]	IEEE Trans 05 [3.11]	ISCAS 06	This work
Process	0.6um @ 5V	0.35 um @ 3.3V	0.35um @ 3.3V	0.13um @ 1.2V	0.13um @ 1.2V
DCO word	10bits	12bits	15bits	8bits	11bits
Power	164mW @ 100MHz	100mW @ 450MHz	18mW @ 200MHz	0.98mW @ 870MHz	0.56mW @ 1050MHz
Range	10 ~ 12.5 MHz	45 ~ 450 MHz	18 ~ 214 MHz	200 ~ 870 MHz	450 ~ 1050 MHz
LSB resolution	10ps	5ps	1.55ps	0.5ps	2ps
Power Factor	21.49mW	11.46mW	4.64mW	1.18mW	0.56mW

Table 3-4　comparison with existing DCO

■ Chapter 4 Proposed All Digital Phase-Locked Loop (ADPLL)

4-1 Conventional ADPLL

Phase-Locked Loops are functional circuits that generate signals that are phase locked with external input signals (reference signals). In this chapter, we will discuss the architecture and algorithm of conventional ADPLL .The conventional ADPLL is proposed by Motorola in 1995[4.1]. It has a 50-cycle phase lock, has a gain mechanism independent of process, voltage, and temperate, and is immune to input jitter. The DCO in this ADPLL operates from 50 to 500 MHz and it also achieves resolution under 500fs.

The ADPLL was shown in Figure 4-4 was proposed by Motorola. Figure4-4 depicts the control unit, frequency comparator, phase comparator, DCO, DCO register, anchor, Add/Sub and Freq/Phase Gain. This ADPLL uses four loosely coupled modes of operation:

■ **Mode 1: Frequency acquisition**

As show in Figure 4-1, it is the flow chart of the frequency acquisition mode. In this mode the ADPLL lock the DCO frequency (div4) to that of the reference clock frequency, ignoring phase alignment. In order to find the target frequency, the ADPLL use a modified binary-search algorithm.

Frequency acquisition reduces frequency gain on every change in search

direction just like the step1 and step 2 in the Figure 4-1. Finally, the acquisition loads the anchor register with the DCO control word value matching the baseline frequency. This operation signifies the end of frequency acquisition.

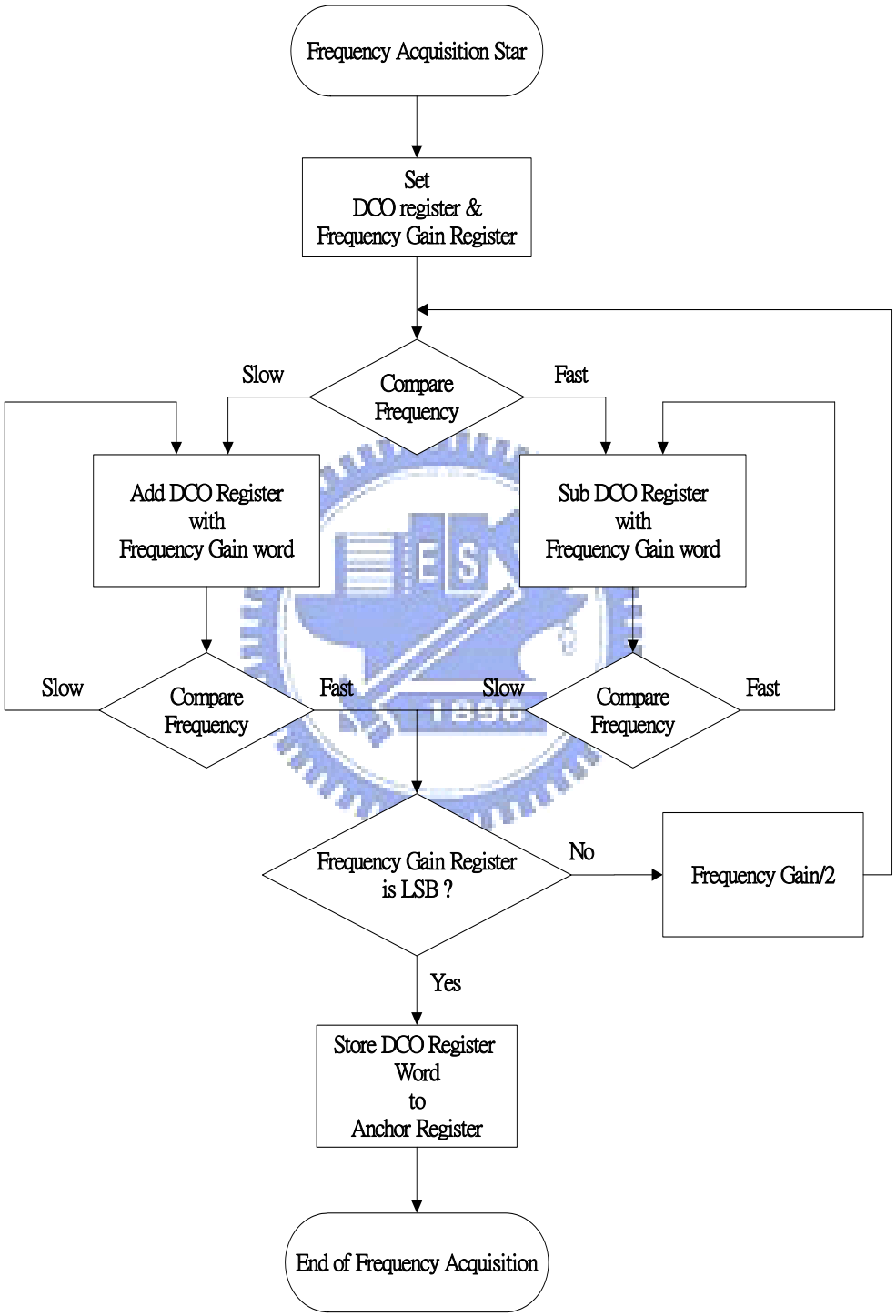

Figure 4-1 The flow chart of the frequency acquisition mode

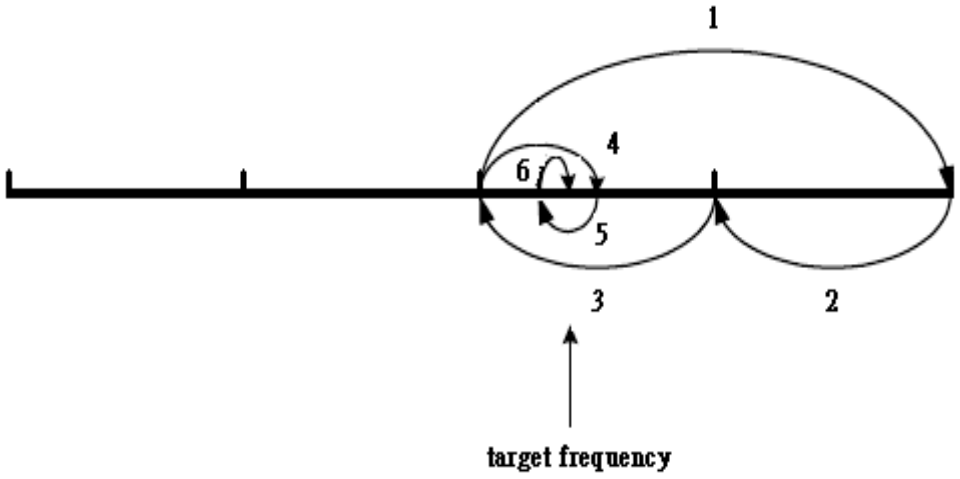

Figure 4-2 Modified binary search(Frequency acquisition)

- **Mode 2: Phase acquisition**

As show in Figure 4-3, it is the flow chart of the phase acquisition mode. In this mode we also use an algorithm. The implementation of this algorithm centers around a phase detector and a phase gain register. The phase detector asserts a digital signal, either “ahead” or “behind,” based on the relation of the DCO clock edge to the reference clock edge. When the output of the phase detector switches from “ahead” or ”behind” or vice versa on successive cycle. At this point, phase acquisition is complete, and the ADPLL transfers the anchor register content to the DCO control register, restoring the baseline frequency and completing phase lock.

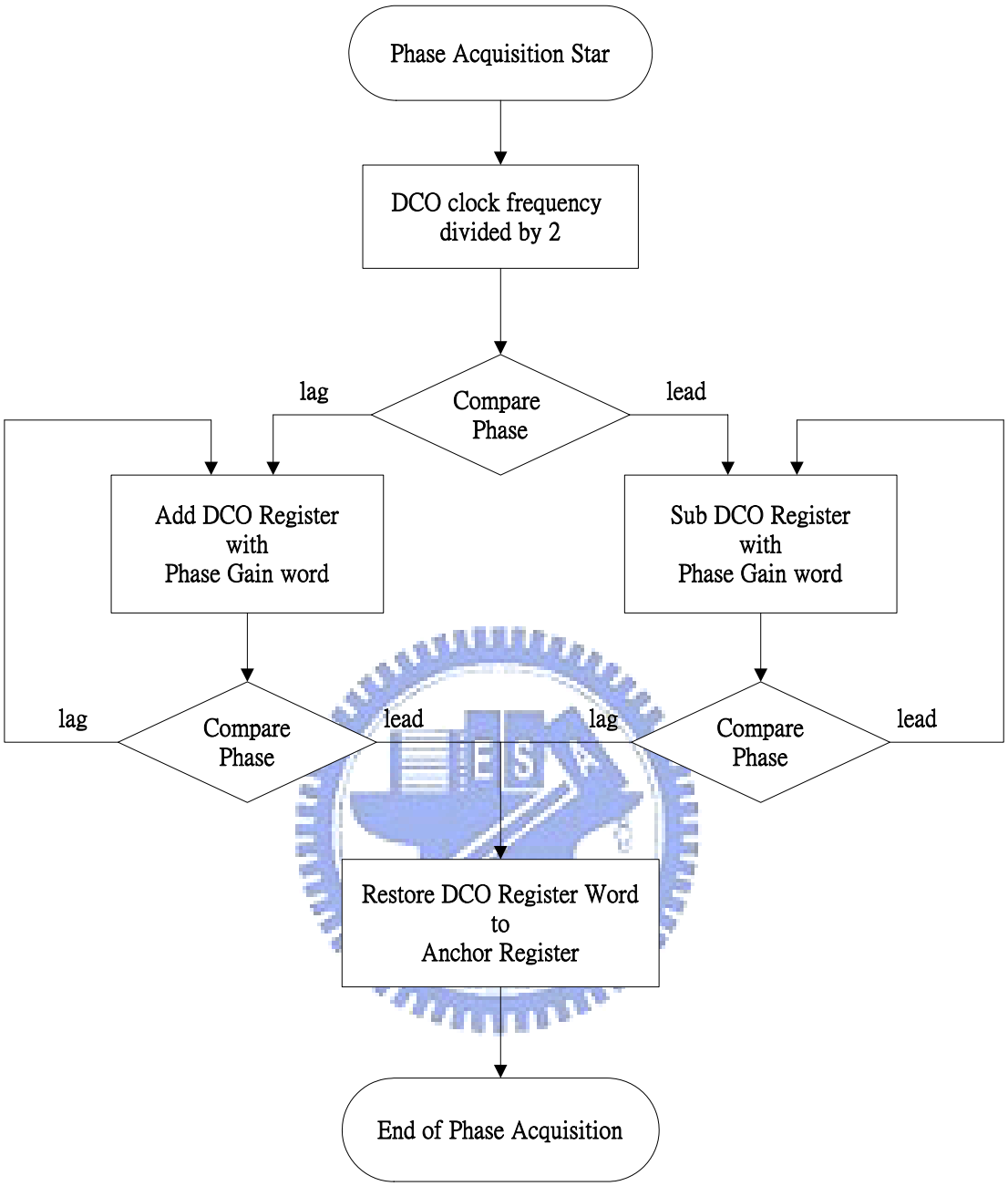

Figure 4-3 The flow chart of the phase acquisition mode

- **Mode 3: Frequency & Phase maintenance**

After the phase acquisition, the ADPLL enters the maintenance mode. In

maintenance mode, the ADPLL applies a different gain strategy from that in acquisition mode. Phase maintenance mode strives to preserve the phase alignment of the DCO clock relative to the reference clock, while the frequency maintenance mode strives to preserve the analogous match in frequency.

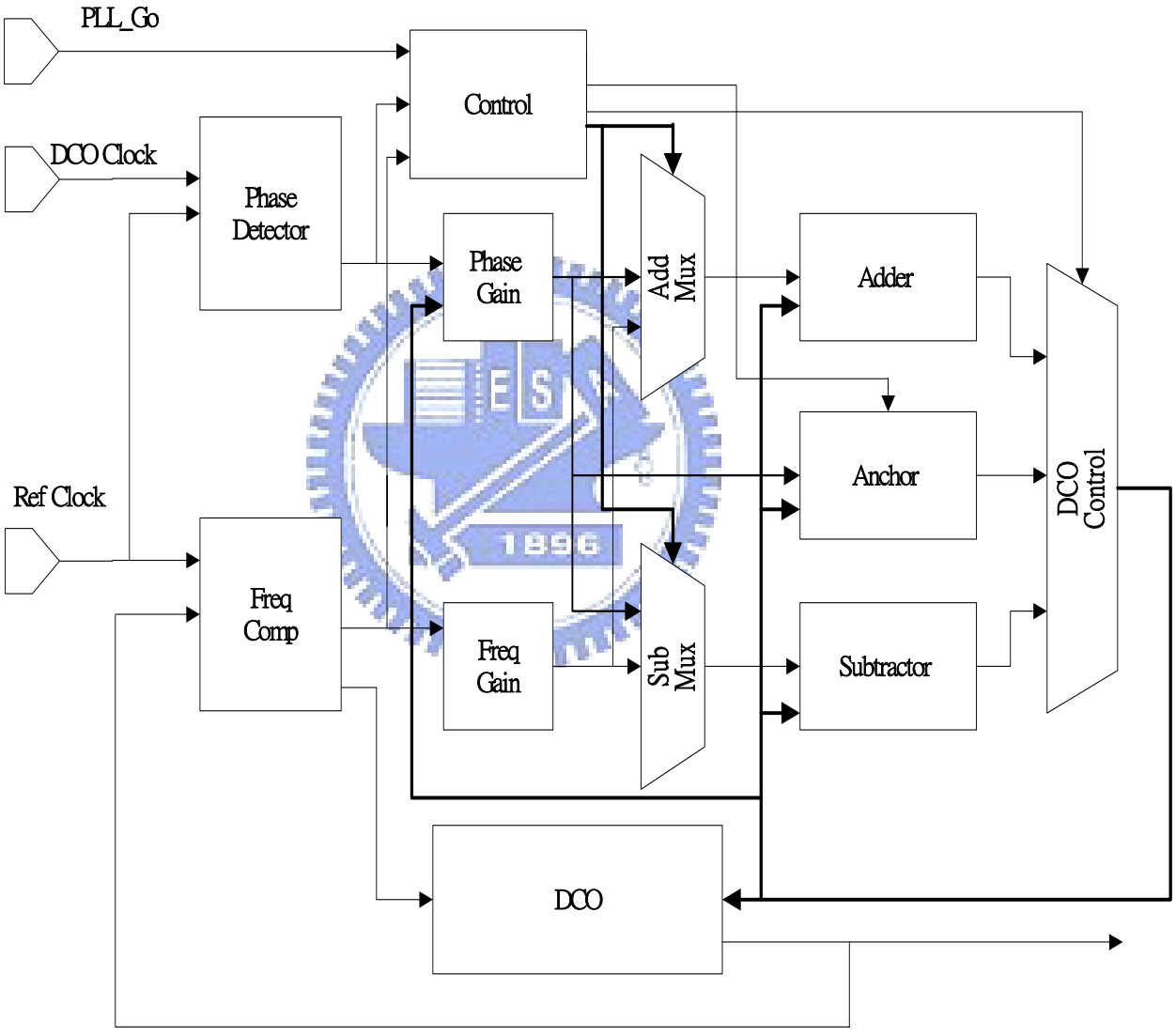

Figure 4-4 Conventional ADPLL block diagram [4.1]

The phase lock process is separated into frequency acquisition and phase acquisition, which significantly reduced the phase-lock time penalty. The sub-blocks are stated as follows:

(1)DCO:

The heart of the ADPLL is a digitally-controlled oscillator. The DCO in the ADPLL just like the VCO in the DPLL but the input of the DCO is the digital control words. The architecture of the DCO is a ring oscillator with odd inverting stages. The frequency control mechanism is through the binary weighted control word. The magnitude of the DCO control word dictates the frequency requirement of the DCO and the control word is held in the DCO control register.

(2)DCO control register:

The DCO control register holds the binary weighted DCO control words, which dictates the frequency of the DCO. Arithmetically incrementing or decrementing the DCO control word modulates the frequency and phase of DCO.

(3)The control block:

It marshals these sub-blocks to implement the different ADPLL modes of operation. By accepting the result of frequency comparator and phase detector as input, the control unit block changes the mode signal.

(4)Frequency comparison:

The frequency comparator accepts the external clock and the internal clock as its inputs. It is performed in the frequency acquisition mode, which compares the DCO frequency with the reference frequency. A frequency comparator compares the DCO

frequency divided by N with the external signal.

(5)Phase comparison:

It is performed in phase acquisition mode, which compares the phase polarity between internal signal and external signal. In the phase comparison, the phase detector tries to align the external clock edge and internal clock edge.

(6)Adder / Substrator:

They provide the updates to the DCO control register.

(7)Anchor circuit:

It is used to restore the DCO control register in the frequency maintenance mode.

(8)Frequency Gain register and Phase Gain register:

They provide operands to the adder and substrator via the add multiplexer and sub multiplexer. Also the phase gain register provides data to the anchor circuit.

4-2 The Algorithm of Proposed ADPLL

As mentioned the previous section, the conventional ADPLL decompose the phase lock into frequency acquisition, phase acquisition, frequency maintain and phase maintain. Proposed low power ADPLL locks the frequency and phase only using one mode. This is because we use a smart frequency comparator. The frequency comparator can lock the frequency and phase correctly.

The algorithm of conventional ADPLL is binary search. Figure 4-5 shows the algorithm.

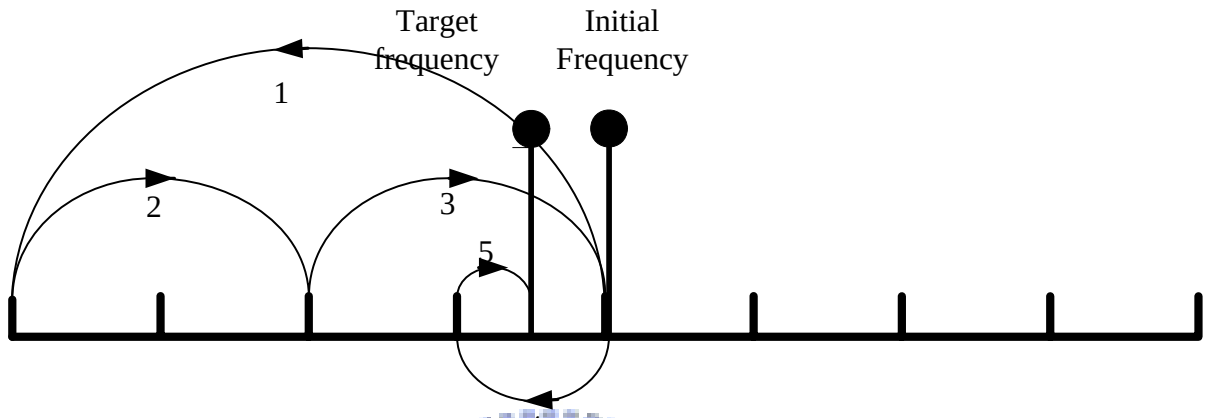

Figure 4-5 Binary Search

Initial 8 > 7

1. 8 - 8 = 0 0<7
2. 0 + 4 = 4 4<7
3. 4 + 4 = 8 8>7
4. 8 - 2 = 6 6<7
5. 6 + 1 = 7 LOCK!!

Now we introduce the binary search operation. The Initial word for DCO is half maximum word. When current word is bigger (smaller) than target word , current word will minus (add) the gain. If their relation is changed, the gain will be half. And

it repeats to compare until the ADPLL is lock. In Figure 4-5, when it is lock, it needs additions and subtractions. We propose a low power algorithm. It needs only subtraction.

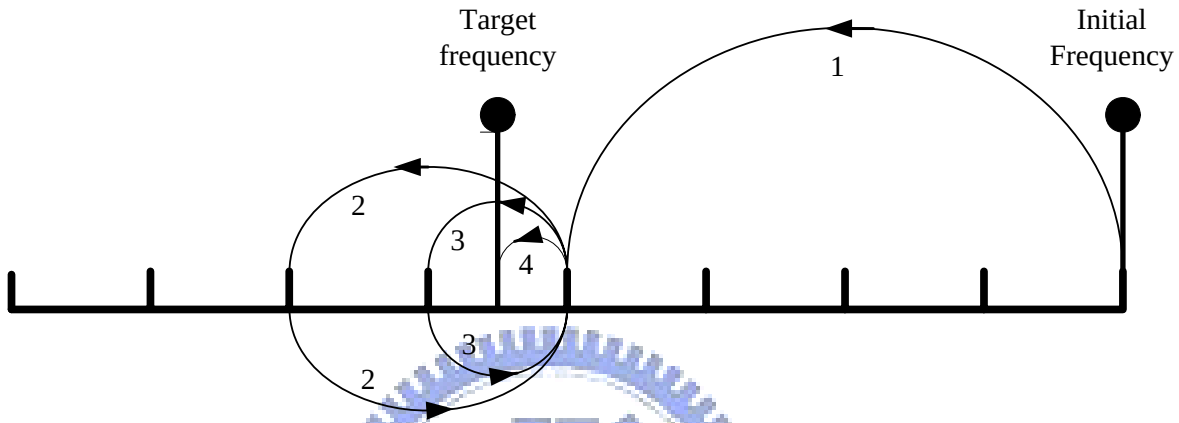

Figure 4-6 Low power binary Search

Initial 16

1. 16 - 8 = 8 8>7
2. 8 - 4 = 4 4<7
3. 8 - 2 = 6 6<7
4. 8 - 1 = 7 LOCK!!

In Figure 4-6, The Initial frequency is maximum frequency. Because initial

frequency is maximum, current frequency must be bigger than target frequency. When new frequency is bigger (smaller) than target frequency, it will not change to old frequency (it will change). If comparing is done, the gain will be half. The operation will go on until the ADPLL is lock. We can compare Figure 4-5 with Figure 4-6. Both two algorithms lock the same target frequency. Figure 4-5 needs additions and subtractions, but Figure 4-6 just needs subtractions. We give another example to prove that.

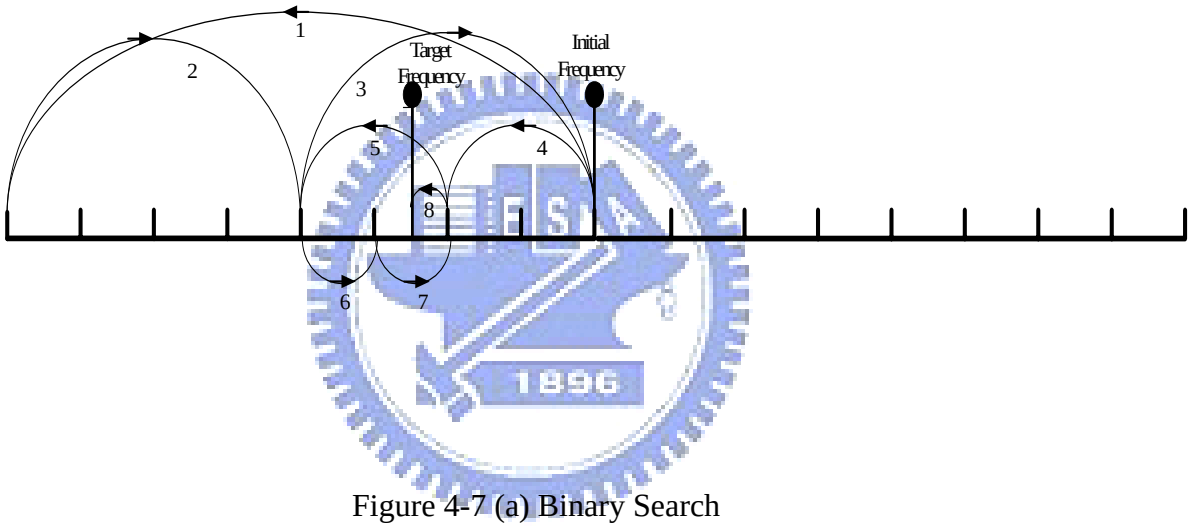

Figure 4-7 (a) Binary Search

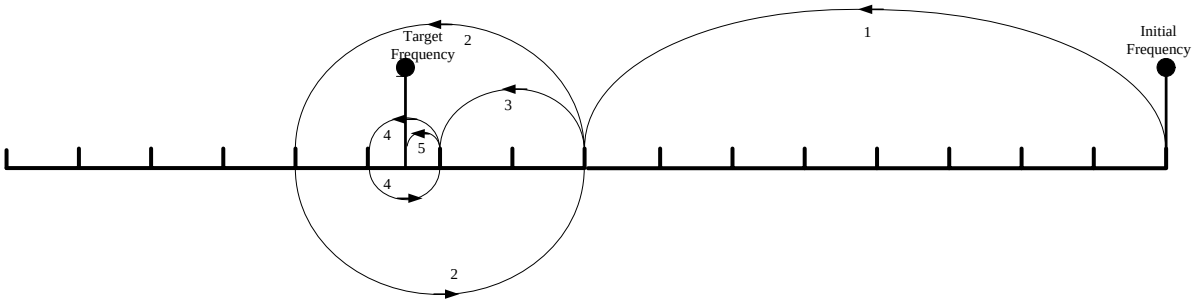

Figure 4-7 (b) Low power binary search

Figure 4-7 shows that binary search needs additions and subtractions but low

power binary search just needs subtractions. The ADPLL in binary search needs adder to do additions and subtractions. The ADPLL in low power binary needs not adder. ADPLL in low power binary changes one bit value in a comparison but ADPLL in binary changes maybe more than one bit value in a comparison. The proposed architecture is simple and area is small. So, compare the proposed algorithm with conventional one, the proposed algorithm have two advantages: low power, small area.

4-3 The Architecture of Proposed ADPLL

The system overview of proposed ADPLL was shown in the Figure 4-8. Proposed ADPLL is built from some blocks. The function of each block will be described in the following:

(1) Match Delay:

The delay path from the input of the Phase frequency detector to the output buffer of the digital-controlled oscillator should be modified.

(2)PFD:

The phase frequency detector can detect frequency & phase, and generates up or down information to search circuit. And it can detect the DCO frequency is what multiplier of the reference clock. You can decide what multiplier you want.

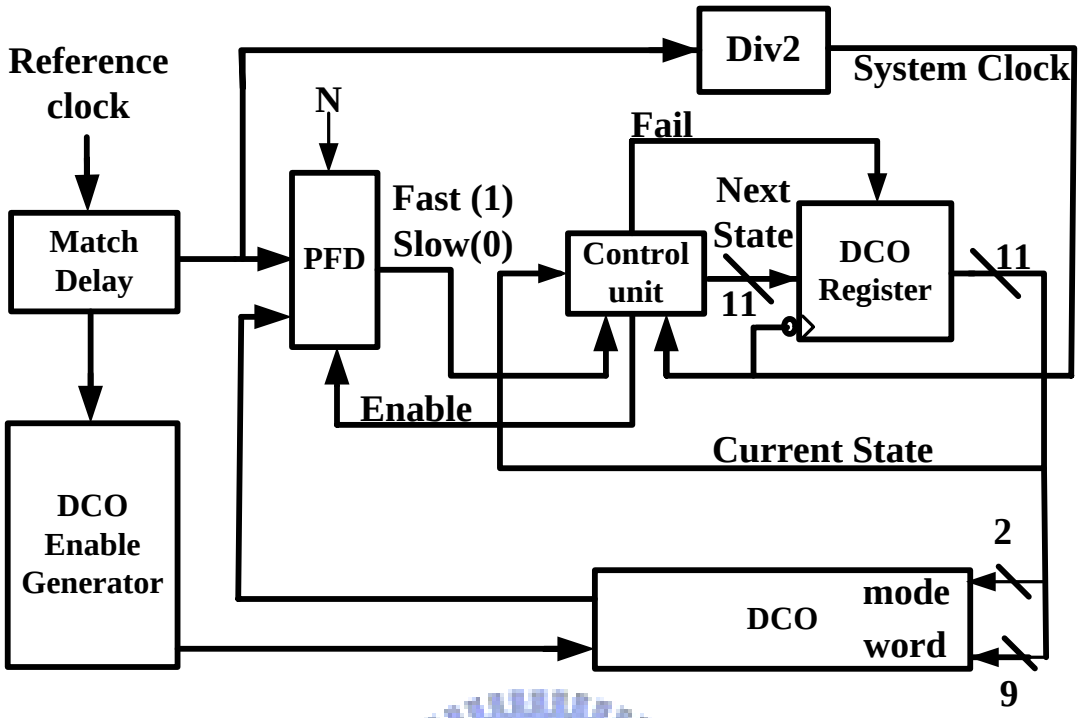

Figure 4-8 architecture of proposed ADPLL

(3) Control unit:

As PFD generates up/down signal, control unit generates DCO word for DCO register to hold for DCO. It also provide enable signal for PFD and fail signal for DCO register to reset.

(4) DCO Register:

The DCO Register holds binary weighted bit for DCO and the frequency of DCO is controlled by the value in the DCO register.

(5) DCO:

Digital-controlled oscillator is the heart of ADPLL. It is a ring oscillator and it is constructed by inverters, coarse tune cell and fine tune cell. DCO transfers input

control word to oscillate output frequency.

(6) DCO Enable Generator:

The DCO enable generator will generate the enable signal and disable signal for digital controlled oscillator. By using this DCO enable generator we can align the first rising edge of reference frequency and DCO frequency.

(7) Div2:

It generates system clock to some blocks.

Figure 4-9 shows the flow chart of the proposed low power binary search. Next, we explain the flow chart.

At the beginning, All Bit will be zero (maximum frequency). And then, Bit[i] will be high for PFD to compare with reference clock.. If signal up is high, it will change Bit[i] to low. On the other hand, if signal down is high, it will keep Bit[i] to high. Bit[1]'s delay time is twice Bit[2]'s delay time. If system is lock, Bit[1] must be zero (PFD signal up must be high).

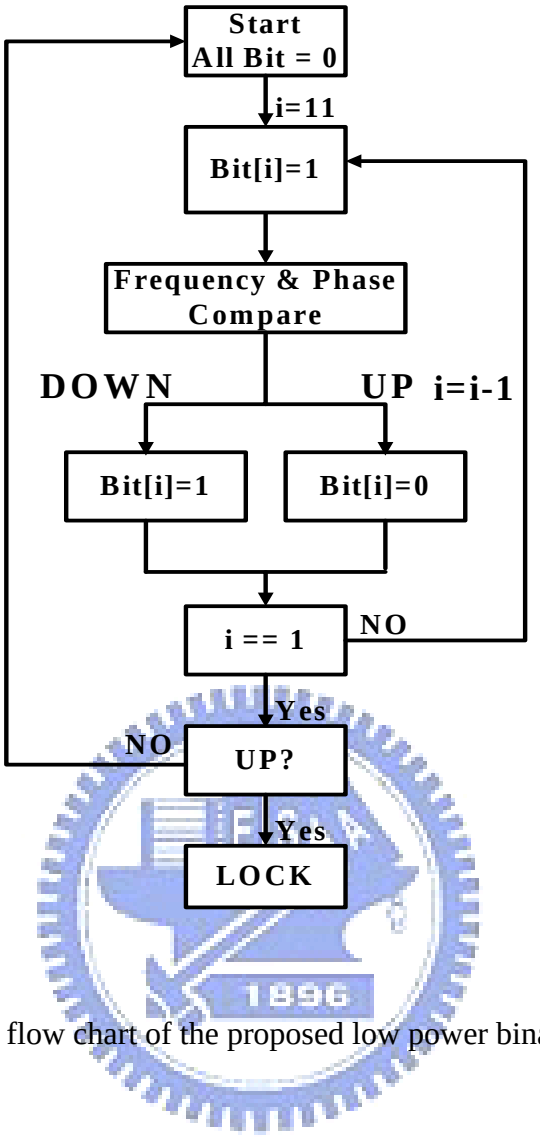

Figure 4-9 flow chart of the proposed low power binary search

4-4 Phase Frequency Detector (PFD)

In this section, we will present the phase frequency detector. Proposed PFD can detect DCO frequency is what times of reference clock. You can decide the times which are depend on the number of D-Flip-Flop. As DCO frequency is compared with target frequency, it also can detect the DCO frequency is faster than target frequency or slower than it.

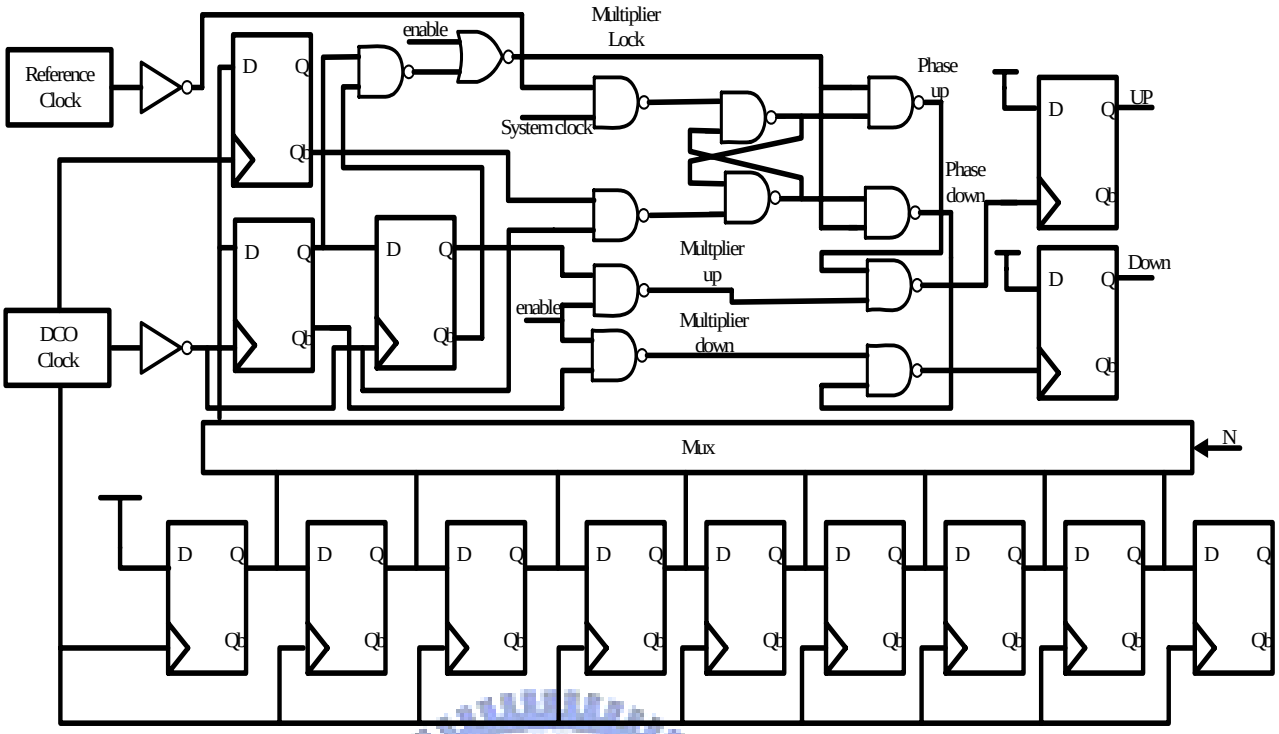

Figure 4-10 proposed phase frequency detector

Figure 4-10 shows it can detect 1~10 times of reference clock. In Figure 4-10, during a system clock, a chain of D-Flip-Flop will pull up to VDD one by one. The mux is used to choose what times do you want. The other two D-Flip-Flops are used to decide the multiplier is lock or not. The input clock of this two D-Flip-Flops is different from the input clock of a chain of D-Flip-Flop and it is the inversion of reference clock. For NAND latch comparison, we make a fine-tuning range and the PFD sends multiplier lock signal to NAND latch. So, if multiplier is lock, the NAND latch will begin to work.

Figure 4-11 shows the situation of multiplier comparison. We assume the PFD multiplier is seven. In Figure 4-11, before the dash line, DCO frequency A is small than 6.5. So the PFD will pull up UP signal to VDD. Before the dash line, DCO

frequency B is bigger than 6.5 and small than 7.5. The NAND latch comparison will begin to work. And, DCO frequency C is bigger than 7.5. The PFD will pull up DOWN signal to VDD.

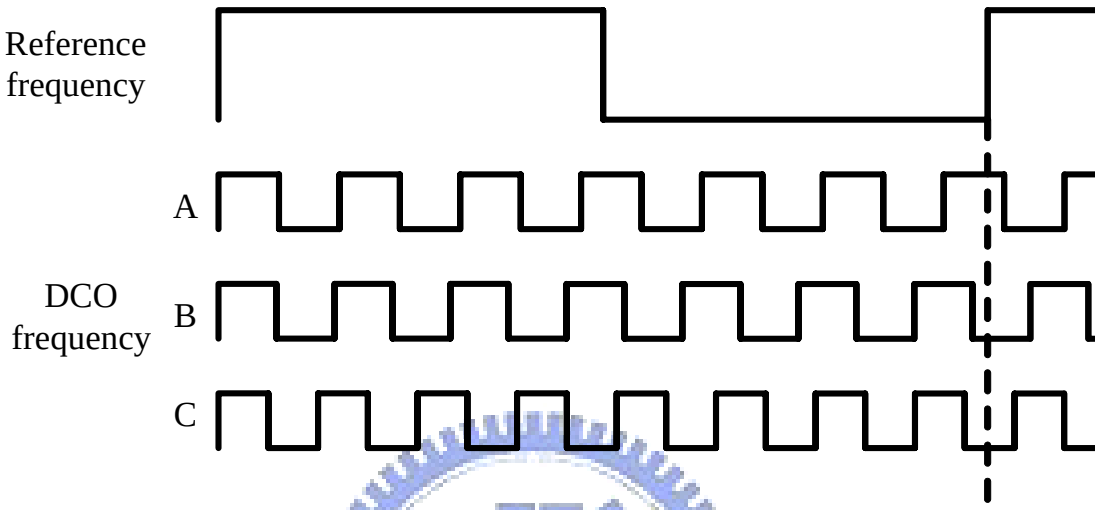

Figure 4-11 the waveform of PFD multiplier signal up/down/lock

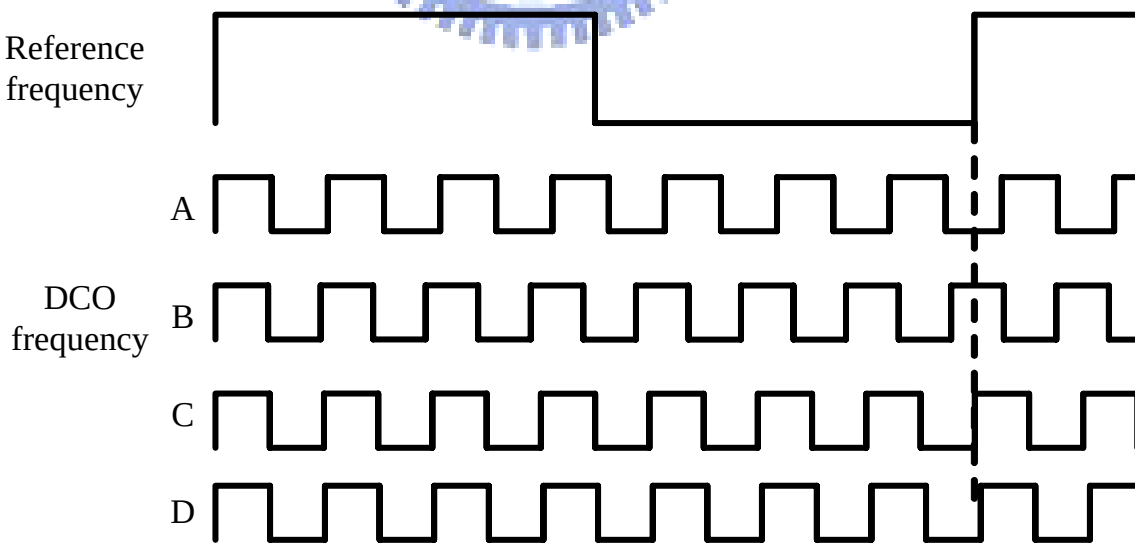

Figure 4-12 the waveform of PFD NAND latch signal up/down

Figure 4-12 shows the situation of NAND latch comparison. We assume the PFD multiplier is lock. In Figure 4-12, before the dash line, DCO frequency A is slower than target frequency. So the PFD will pull up UP signal to VDD. Before the dash line, DCO frequency B is faster than target frequency. And, DCO frequency C is lock. DCO frequency D is used to test DCO frequency is lock. The last bit delay time is 4ps. If DCO frequency C is lock, we gain 4ps delay time will change DCO frequency C to D. In Figure 4-12, D signal is slower than target frequency. At this moment, the control unit will send frequency lock signal. Otherwise it will send system fail signal to reset all block. Figure 4-13 shows the D-Flip-Flop circuit. It is a TSPC architecture with reset signal.

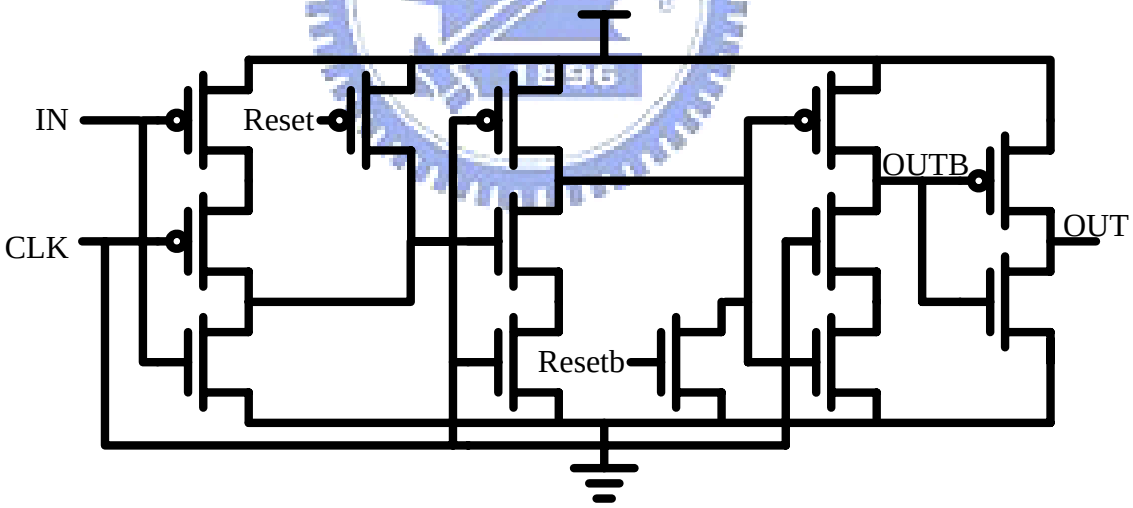

Figure 4-13 D-Flip-Flop

4-5 Low Power Digital Controlled Oscillator Design

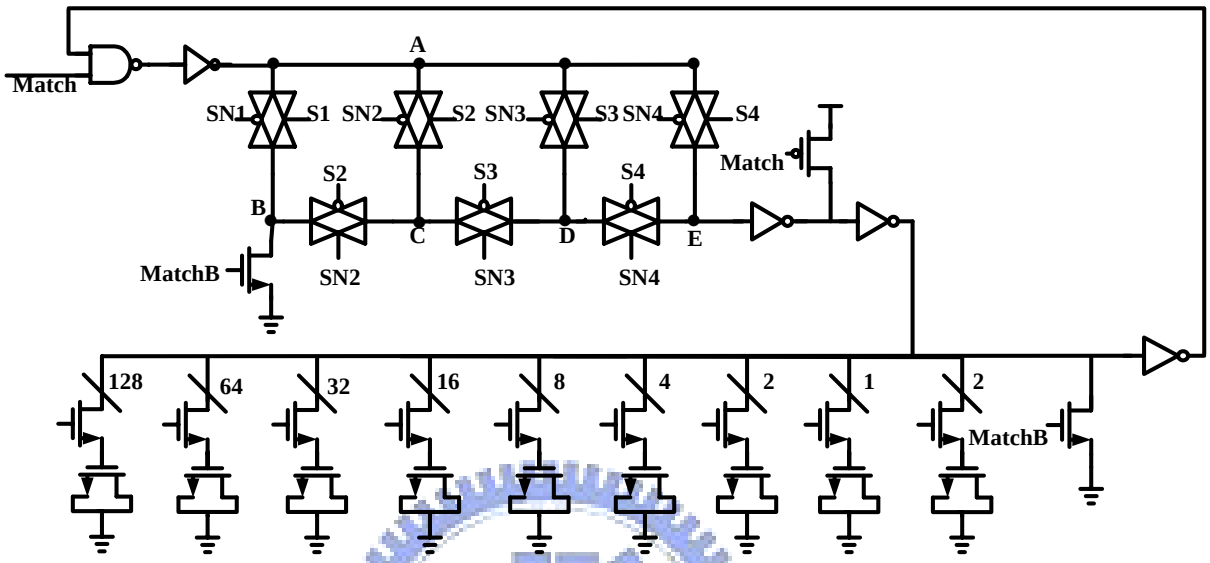

Figure 4-14 modified low power digitally control oscillator

Last Chapter, we introduce the proposed low power DCO. In order to align the reference clock, we should modify it. We put the quickly reset circuit into Type-1 DCO. Figure 4-14 shows the modified low power digitally control oscillator. The frequency range of proposed low power DCO is from 450 MHz to1050 Mhz. When output frequency is 1050MHz, power is 0.56 mW. According to Table 3-4, it's power is very low.

4-5 DCO Enable Generator / Control unit

In this section, we will present the Div2 & DCO Enable Generator circuit and control unit. In proposed ADPLL, the algorithm is different from conventional algorithm. So, the control unit is used to generate signal and decide DCO word.

In the Figure 4-15, it shows the waveform of the relation between the DCO enable signal and DCO output signal. At the beginning, the DCO enable signal is from low go to high and the DCO start to oscillate. After two cycle of reference clock, the DCO enable signal goes to low which means the DCO will be disabled and the DCO will start to oscillate at the next first rising edge of the DCO enable signal. As we can see, the disable time of the DCO enable signal should be shorter than the half cycle of the DCO signal.

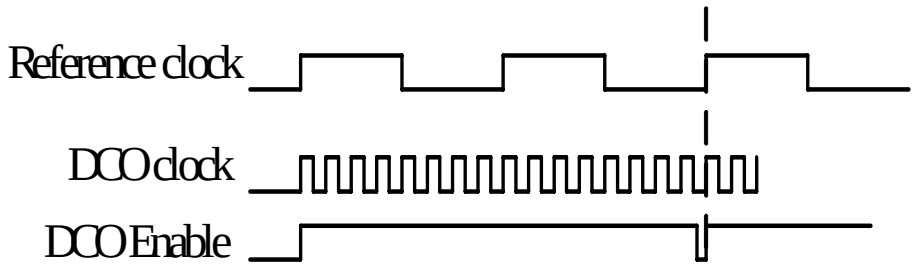

Figure 4-15 DCO Enable signal for the first rising edge aligning

(ADPLL locked)

In the Figure 4-15, it shows the signal when ADPLL is in the locked state. Also in the Figure 4-16, it shows the signal when the ADPLL is in the unlocked state.

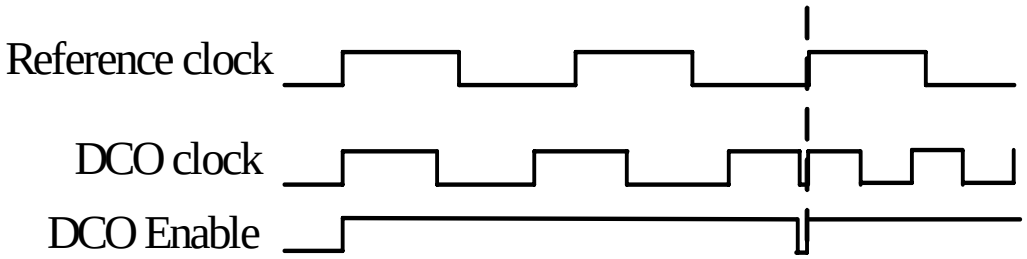

Figure 4-16 DCO Enable signal for the first rising edge aligning

(ADPLL not yet locked)

The DCO enable generator circuit was shown in the Figure 4-17. This DCO enable generator circuit includes one D flip-flop, some buffers and one nand gate. The combination of the inverter, delay buffer and nand gate is a pulse generator circuit. The pulse width of the pulse generator circuit is the time when the DCO be disabled. In proposed ADPLL system, the comparison is operated in every two cycle of the reference clock period. So we generate a clock signal for ADPLL system by a divider circuit Figure 4-17 also shows the Div2-block which is used to generate system clock.

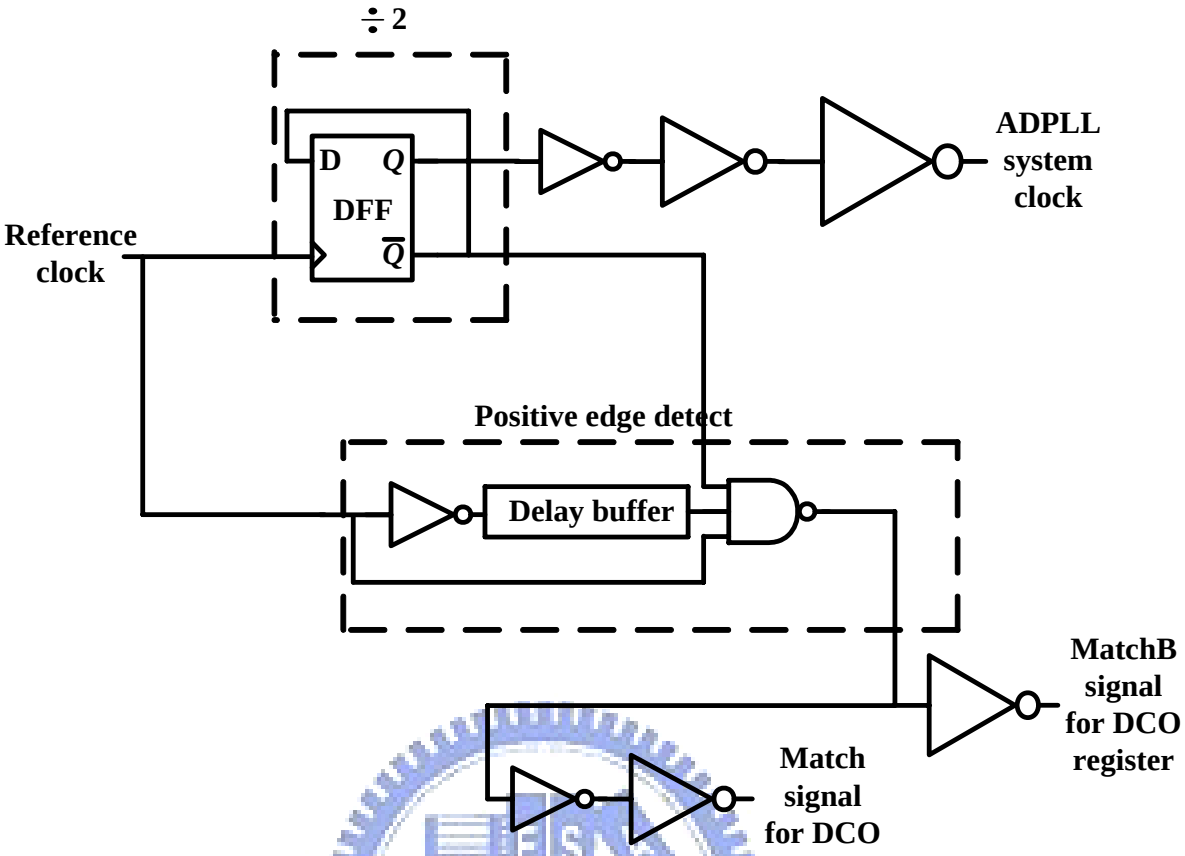

Figure 4-17 Div2 & DCO enable generator

The control unit circuit generates the PFD enable signal and generates the DCO word value for DCO register. After the multiplier is lock, PFD enable signal allows NAND latch to compare DCO frequency with target frequency. Because proposed ADPLL needs not adder, we let control to decide the DCO word value. The way of word value decision flow chart is in Figure 4-9.

Figure 4-18 shows the PFD enable signal. This PFD enable generator circuit includes one D flip-flop, some buffers and one NAND gate. The combination of the inverter, delay buffer and NAND gate is a negative generator circuit. The pulse width of the pulse generator circuit is the time when the NAND latch works.

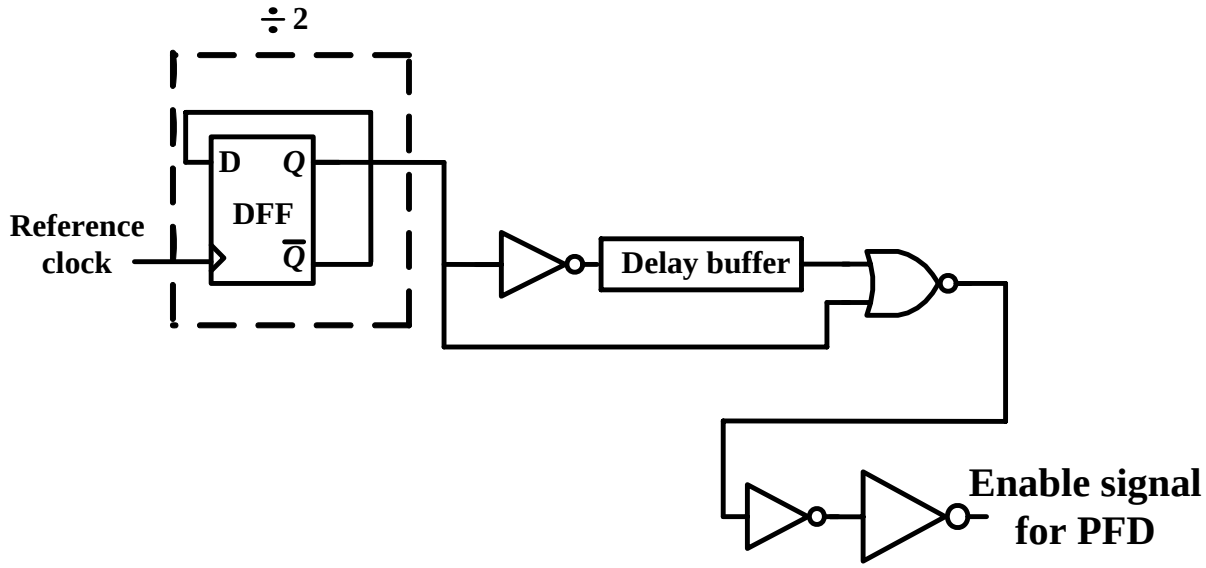

Figure 4-18 PFD enable generator

Figure 4-19 presents the DCO word value decision. It includes D Flip-Flops and logic gates. D Flip-Flops is used to make the bit value high one by one and allow one bit decision. Logic gates decide the bit value still high or low. Control unit generate the DCO word value and send it to DCO resister. So, control unit includes PFD enable generator and DCO word value decision.

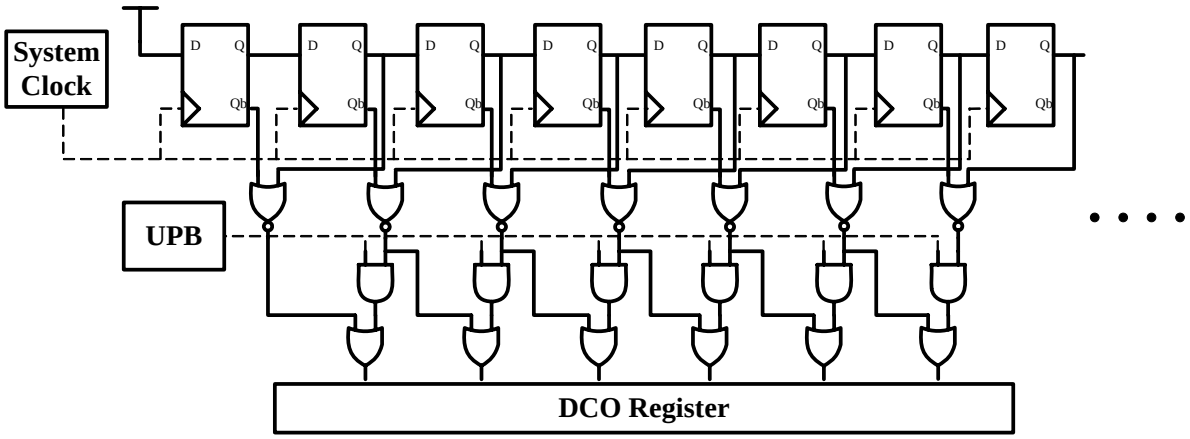

Figure 4-19 DCO word value decision

■ Chapter 5 Application and Simulation Result

5-1 Application

PLL are widely used in consumer, computer, and communication aspects. Different application has different specification. Now we show one application of All Digital Phase Locked-Loop:

Frequency synthesizer:

The ADPLL is applied to a frequency synthesizer. The characteristic of frequency synthesizer is generating a clock that runs at multiple times the reference clock frequency. The block diagram was shown in Figure 5-1. The relationship between reference clock and output clock was shown as equation (5.1).

$$\begin{aligned} &\left(Frequency_{ref}\right)\times\frac{1}{N}=\left(Frequency_{out}\right)\times\frac{1}{M} \\ &\Rightarrow Frequency_{out}=\frac{M}{N}\times\left(Frequency_{ref}\right) \end{aligned} \tag{5.1}$$

Memory is very important for computer, MP3 player, cell phone…etc. Proposed ADPLL is applied to DDR3. Using the frequency synthesizer, we can oscillator any frequency which is in ADPLL frequency range for DDR3. According to IEEE paper, we choose two frequency 700Mhz and 800Mhz [5.1], [5.2]. Next, we will show some

simulation waveforms.

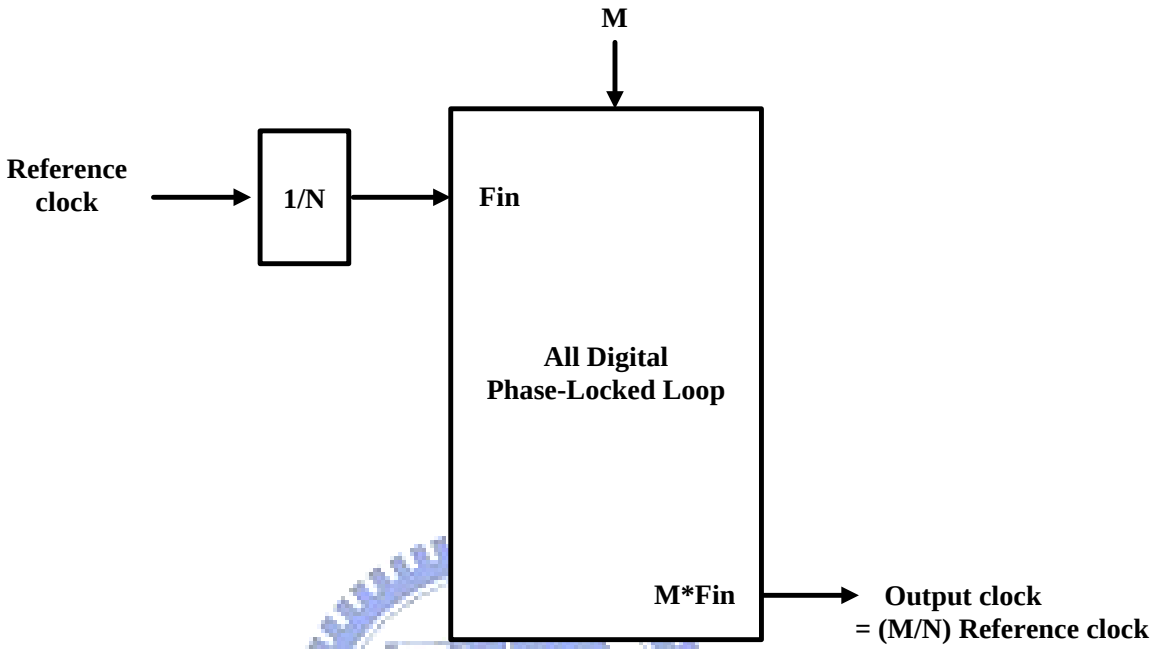

Figure 5-1 Block diagram of the frequency synthesizer

5-2 Simulation Result

In this section we will present the simulation result of our ADPLL. We will show the pre-layout simulation waveform and measure proposed ADPLL jitter. The measured jitter type is peak-to-peak jitter.

We will show the pre-layout simulation in different corners. The first corner is TT (typical model for 1.2V devices) and the second corner is SS (Slow NMOS Slow PMOS model for 1.2V devices). The SS corner is in the high temperature and low

voltage environment. In the pre-layout simulation, the reference clock is about 100MHz and the proposed ADPLL output clock is 700MHz and 800Mhz. The Figure 5-2 shows the locked process waveform of 700Mhz ADPLL (TT corner). The Figure 5-2(A) consists of word [10:0] signal, DCO_clk signal, Ref_clk signal, DCO_enable signal, Lock signal, Up signal and Down signal. Those signals are stated as follows:

(1) Ref_clk: The matched delay clock of the input reference signal.

(2) DCO_clk : The output of the DCO.

(3) DCO_enable: When the DCO_enable signal is low, the DCO will be disabled. When the dcostart signal is high, the DCO will be enabled and start to oscillate.

(4) word[10:0]: The value in the DCO control word register.

(4) up : The PFD sends to control unit to make DCO fast.

(5) down: The PFD sends to control unit to make DCO slow.

(7) Lock: When the signal is high, it means that ADPLL is in the lock state.

The Figure 5-2(B) shows the locked state waveform of 700Mhz ADPLL (TT corner) and

The Figure 5-3(A) shows the locked process waveform of 700Mhz ADPLL (SS corner), and the Figure 5-3(B) shows the locked state waveform of 700Mhz ADPLL (SS corner). In the Figure 5-4(A), shows the locked process waveform of 800Mhz ADPLL and the Figure 5-4(B) shows the locked state waveform of 800Mhz ADPLL.

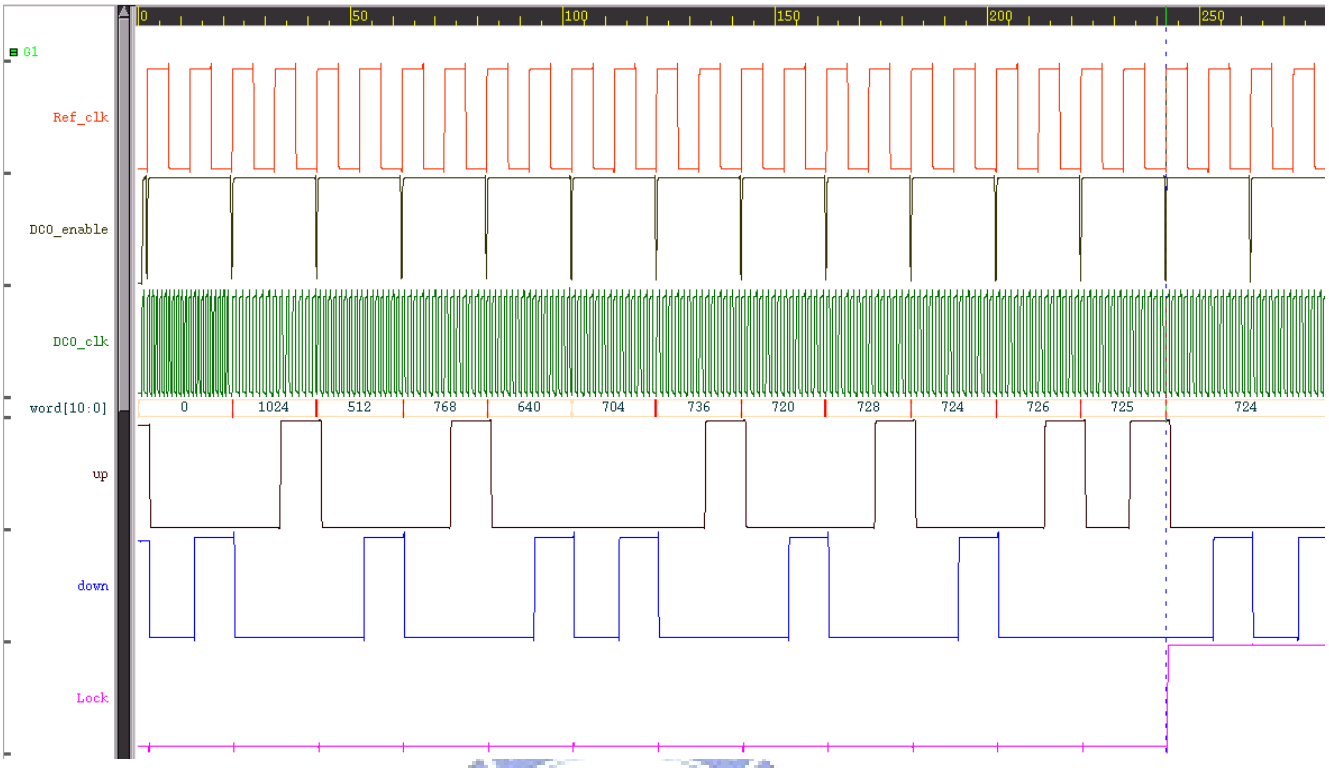

Figure 5-2(A) The locked process waveform of 700Mhz ADPLL (TT corner)

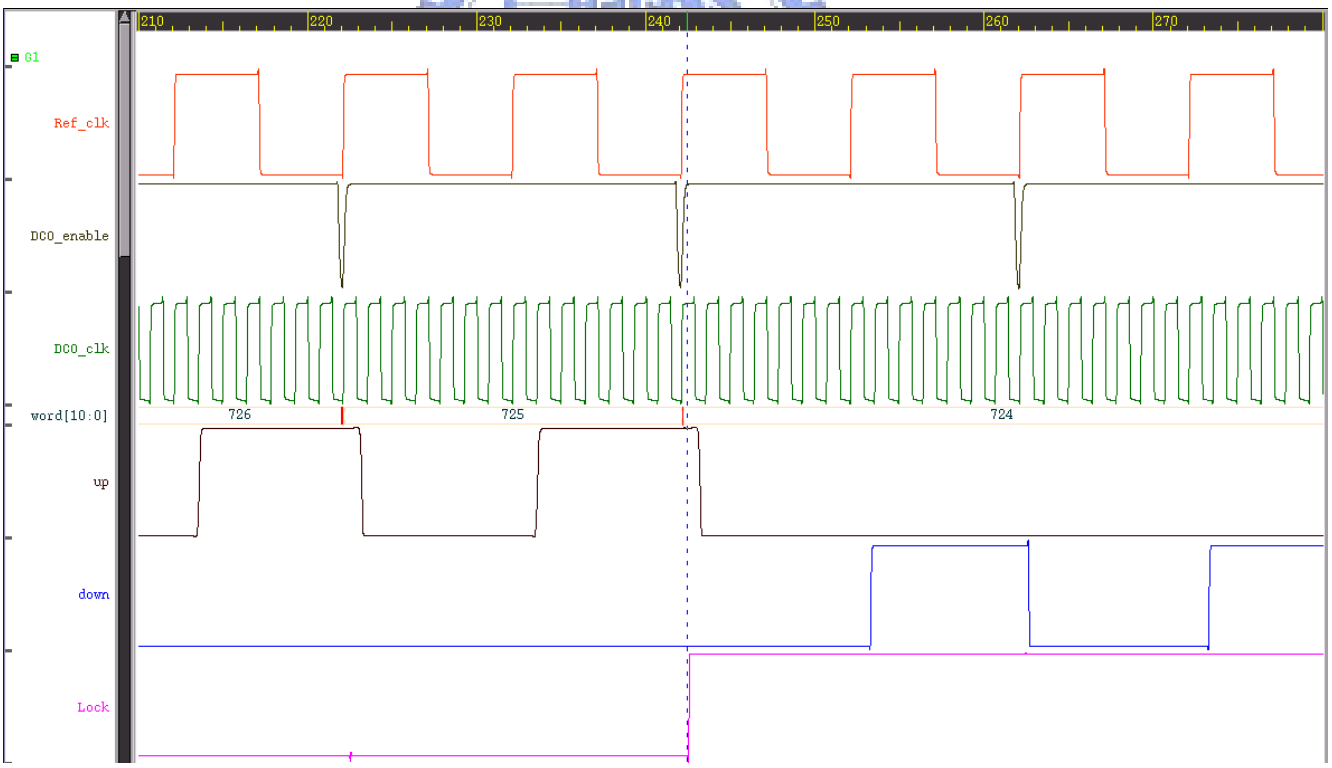

Figure 5-2(B) The locked state waveform of 700Mhz ADPLL (TT corner)

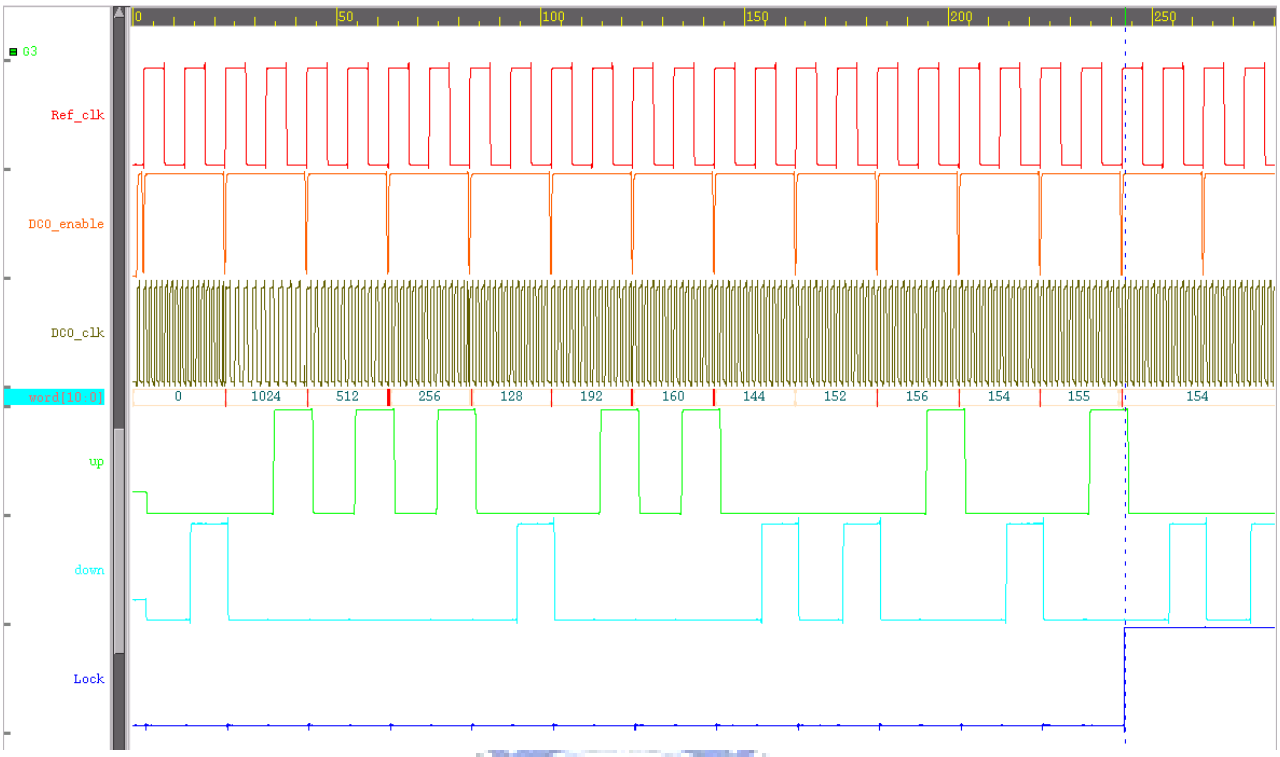

Figure 5-3(A) The locked process waveform of 700Mhz ADPLL (SS corner)

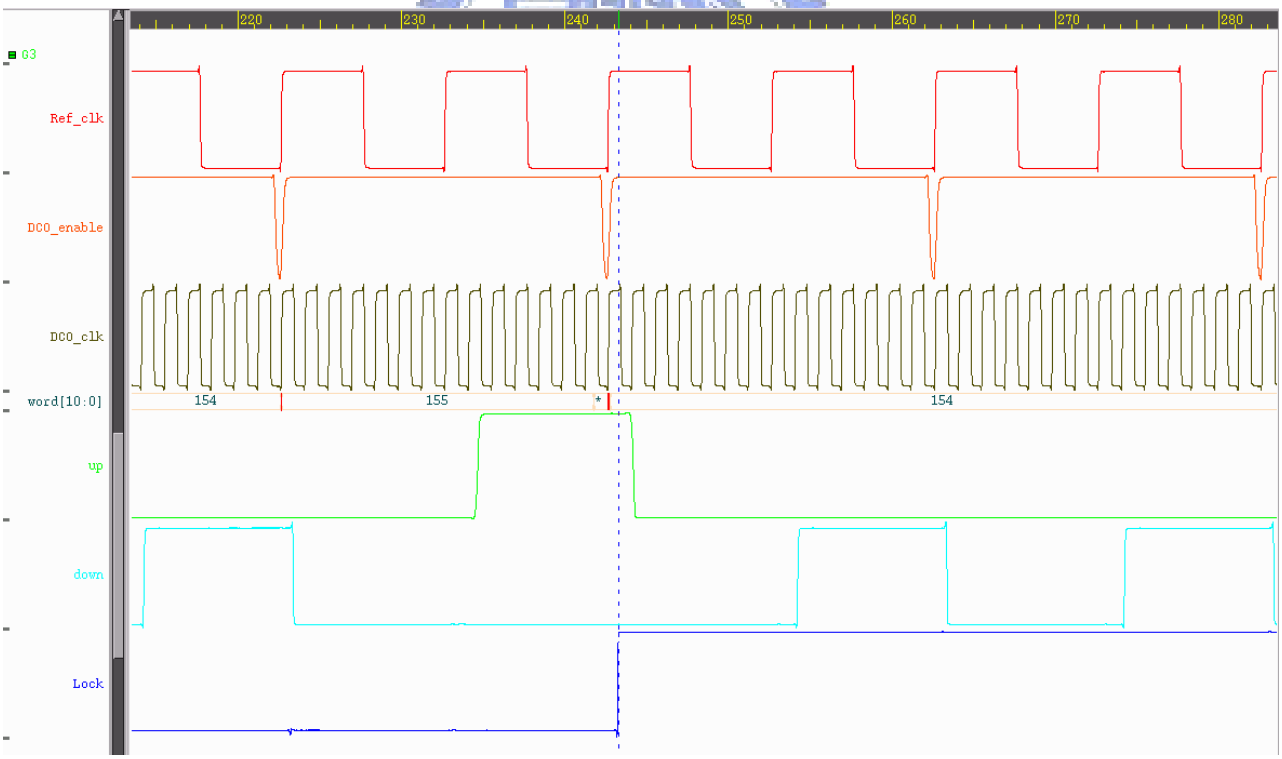

Figure 5-3(B) The locked state waveform of 700Mhz ADPLL (SS corner)

Comparing the two different results (TT corner and SS corner), we can find that the DCO control word value in SS corner is smaller. Because the SS corner simulate

with Slow NMOS Slow PMOS model environment, the DCO has smaller oscillate frequency range and the ADPLL needs smaller DCO control word value (high frequency) to control the DCO output frequency in the locked state. And, the lock state is pull up to high in the same reference clock. Next, the Figure 5-4(A) shows the locked process waveform of 800Mhz ADPLL, and the Figure 5-4(B) shows the locked state waveform of 800Mhz ADPLL.

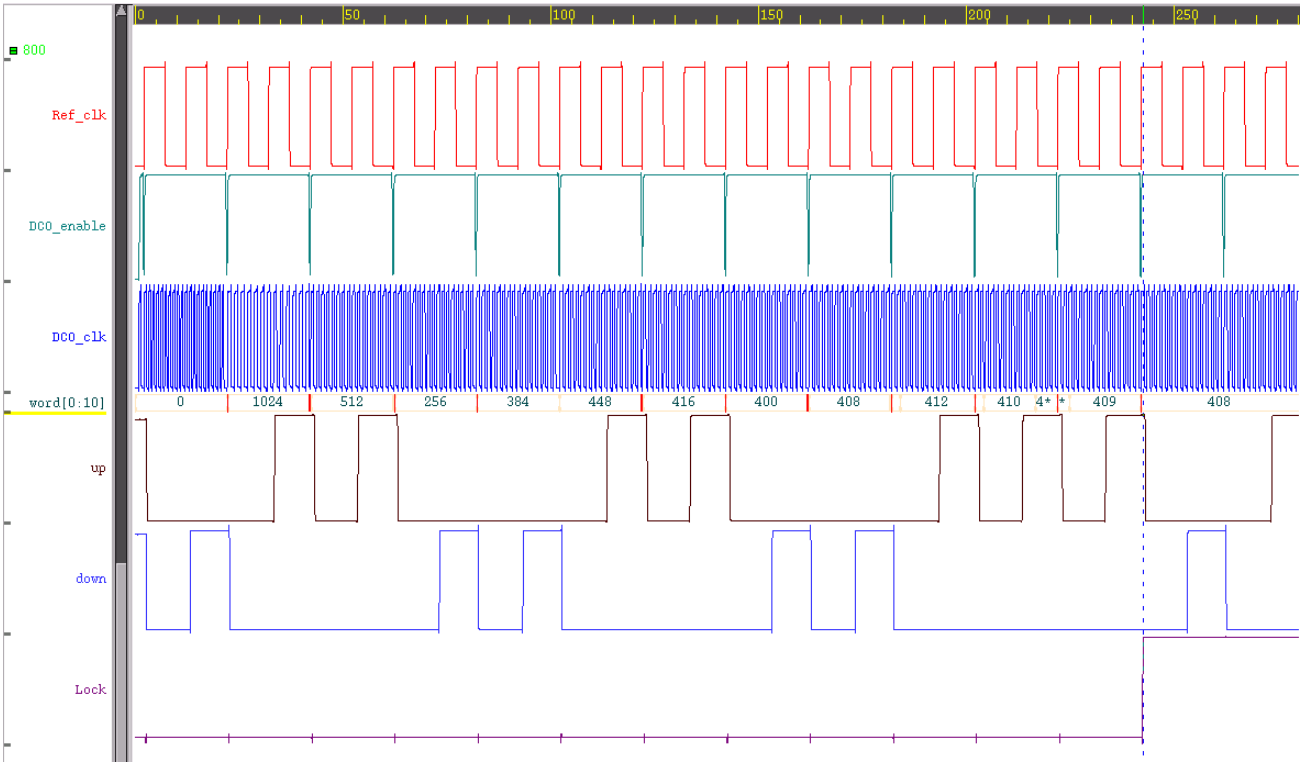

Figure 5-4(A) The locked process waveform of 800Mhz ADPLL

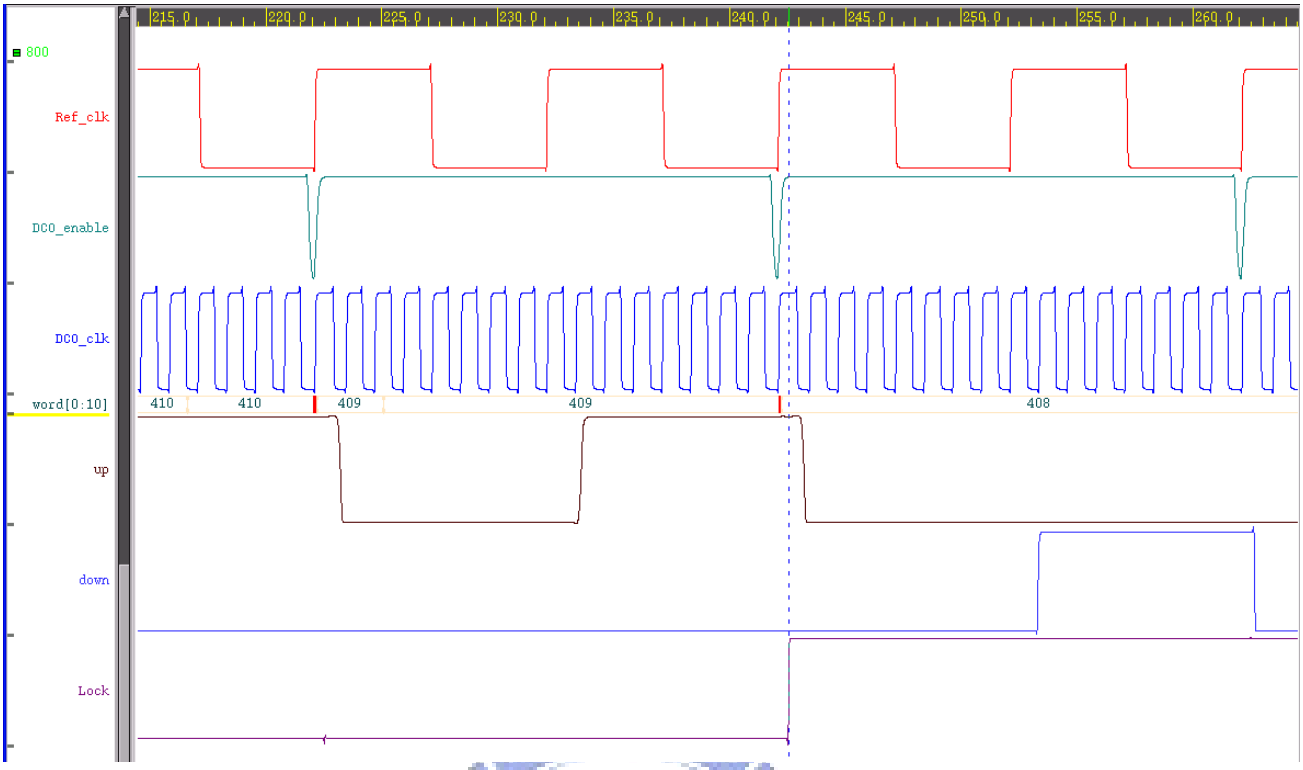

Figure 5-4(B) The locked state waveform of 800Mhz ADPLL

5-3 Layout Implementation

In this section, we will show the layout of our ADPLL. The floor planning is important procedure in layout drawing. We should consider the size of each block and the connection among them as well.

Figure 5-5 shows the floor plan of our ADPLL and Figure 5-6 shows the layout of our ADPLL. Figure 5-7 shows the final ADPLL implementation result. There are 38 % for DCO, 24% for PFD, 14% for control unit and the other shown in Figure5-7. And, the area is 58*70 um^2. The area is very small.

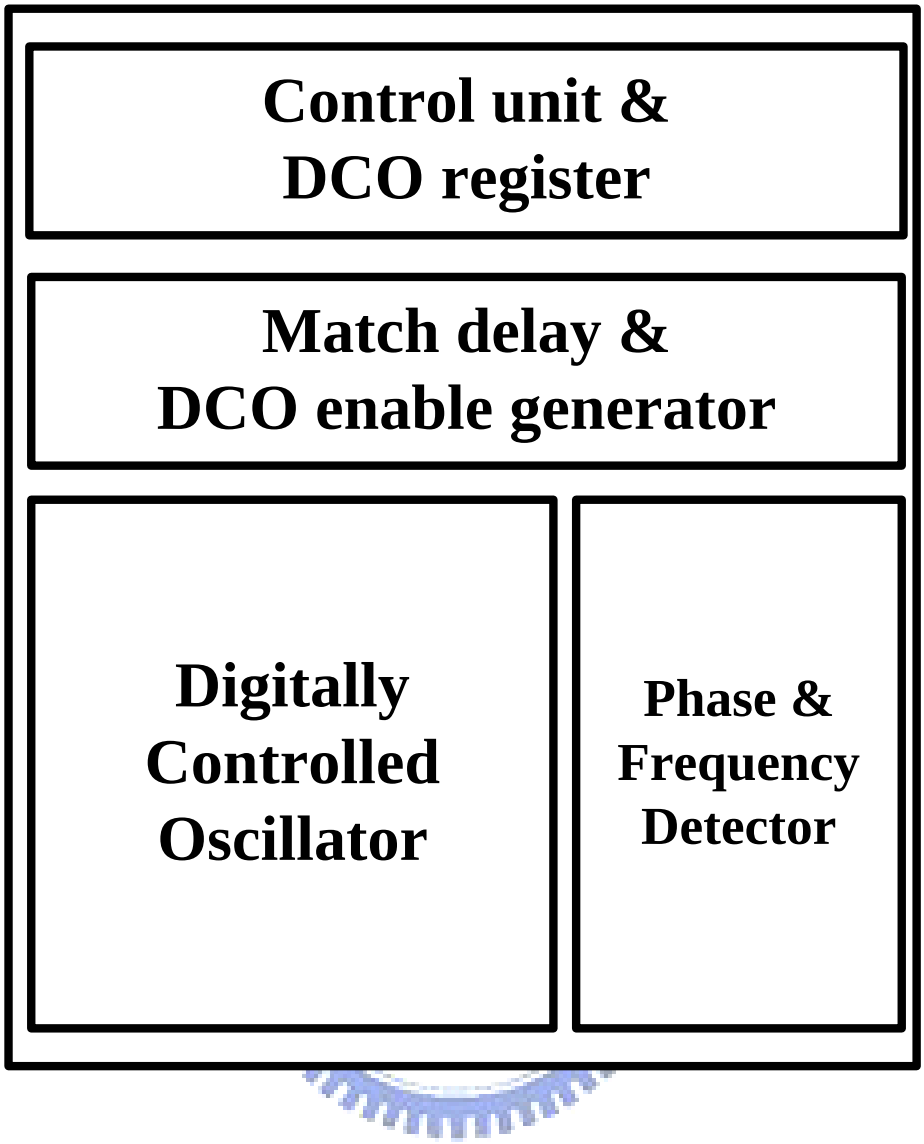

Figure 5-5 Floor planning of ADPLL

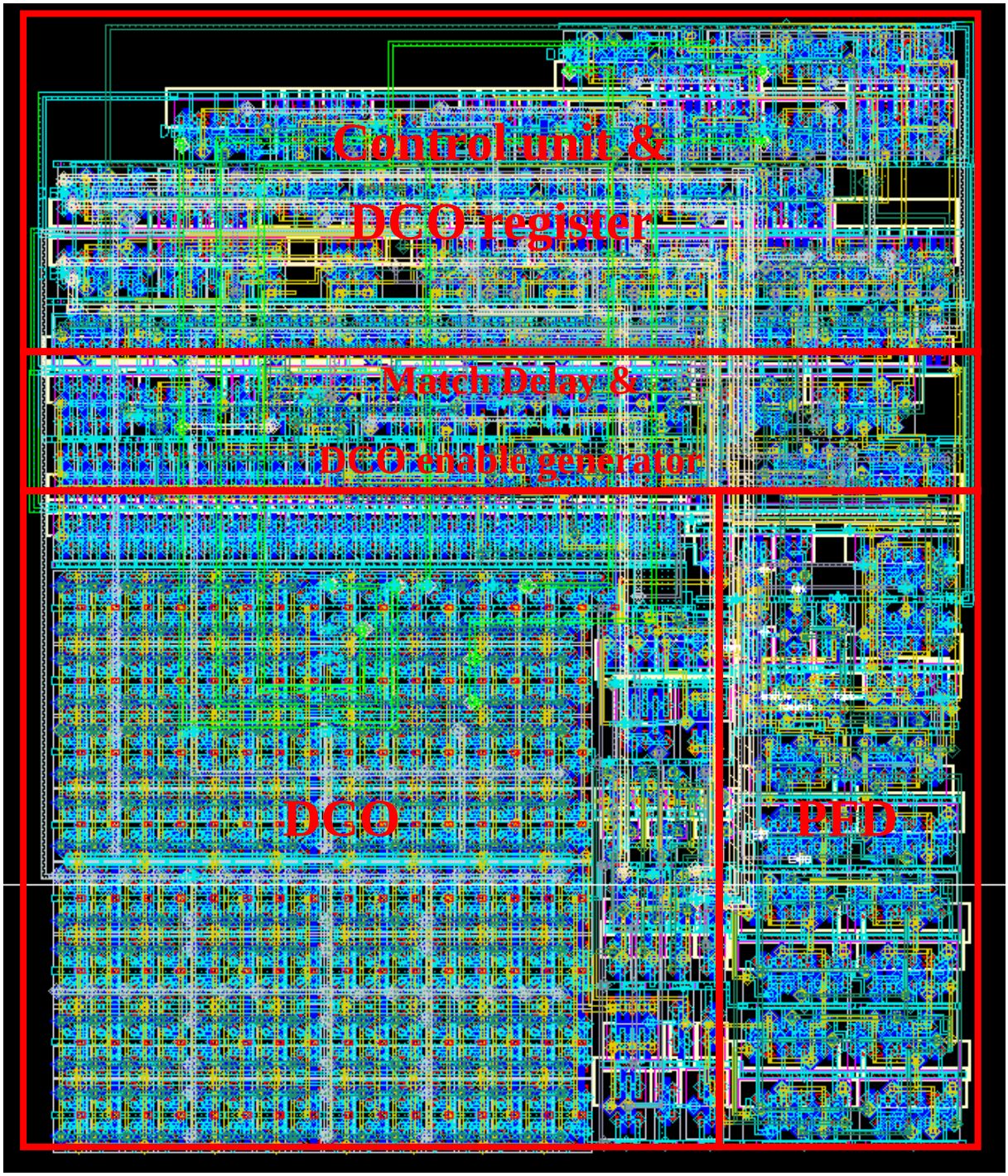

Figure 5-6 The layout of ADPLL

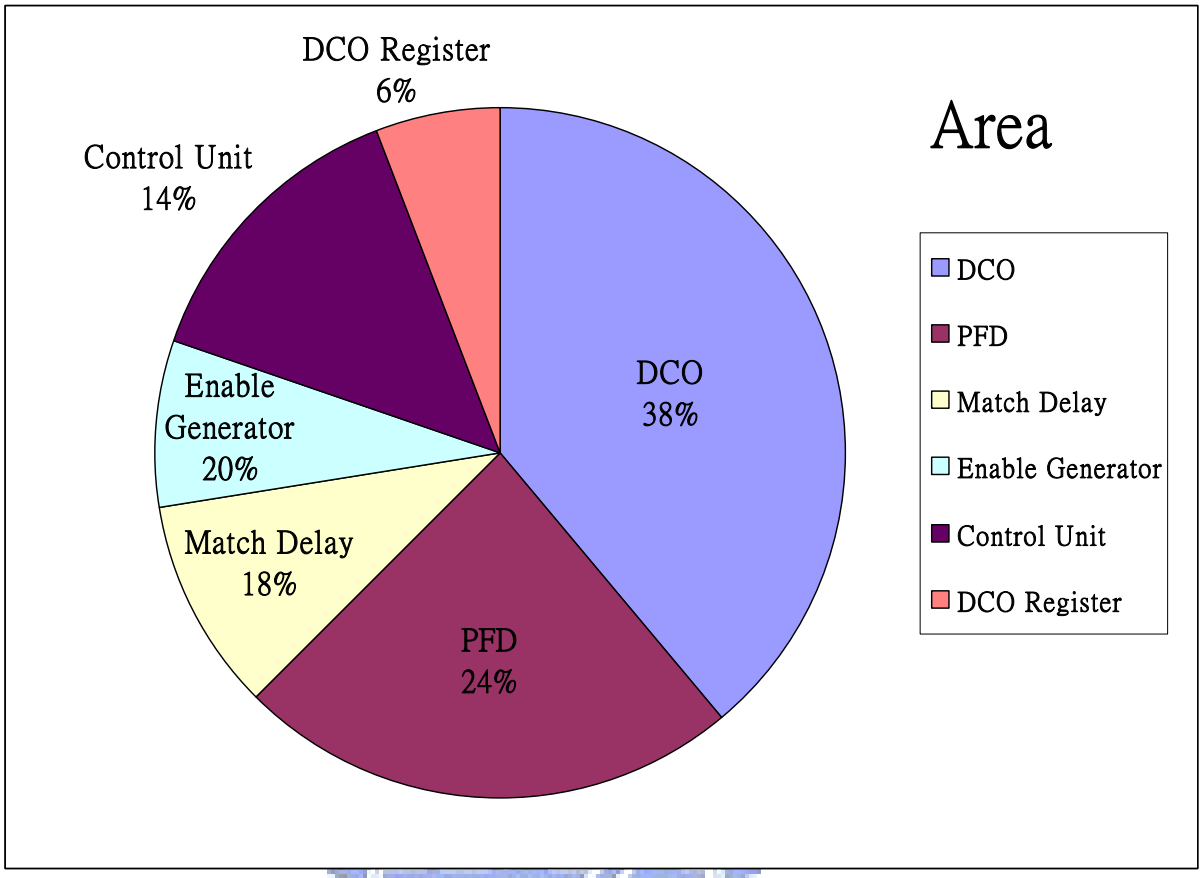

Figure 5-7 Area result of ADPLL layout

■ Chapter 6 Conclusion and Future Work

6-1 Conclusion

In this thesis, a new type ADPLL for small area and low power consumption is proposed. A proposed PFD is used to detect multi times of reference clock. Proposed low power DCO is used to reduce power consumption. The proposed low power algorithm reduces power consumption and area. The DCO in our ADPLL is with 11-bit binary weighted control and its operating frequency range is from 450MHz to 1050MHz with a supply voltage 1.2v. The DCO operation at 1050MHz just needs 0.56mW.

Through the simulation result, the phase jitter is about 18.4ps when the DCO output clock is about 700MHz. The area is 70um x 58um in a TSMC 1P8M 0.13um CMOS process and total transistor numbers of the ADPLL is about 1714. The power consumption simulated by HSPICE is about 0.85mW. The summary of the ADPLL was shown in the Table 6-1. According to Table 6-2, proposed ADPLL is the simplest and has lowest power, small area and good jitter performance among them.

Power supply voltage	1.2v
Power consumption	0.85mW @ 700MHz
DCO Frequency Range	450MHz~1050MHz
Jitter	18.4ps @ 700MHz (1.38%)
Locked time	22 Input cycles
IC Process	TSMC 1P8M 0.13um CMOS process
Area	70um x 58um
Transistor count	1714
Number of Control Bit	11bits(2bits for coarse delay cell and 9bits for fine delay cell)
Reference Frequency	100MHz

Table 6-1 The summary of our ADPLL

$$Power\ Factor \quad = Power \times \frac{0.13um}{\Pr ocess} \times \frac{700MHz}{Frequency} \times \left(\frac{1.2V}{SupplyVoltage} \right)^2$$

Performance Parameter	JSSC 03 [6.9]	JSSC 03 [6.12]	ISSCC 04 [6.10]	ISCAS 05 [6.13]	ISCAS 06	This work
Process	0.13um CMOS	0.35um CMOS	90nm CMOS	0.18um CMOS	0.13um CMOS	0.13um CMOS
POWER	7mW @ 240Mhz	100mW @ 500Mhz	1.7mW @ 520Mhz	15mW @ 378MHz	1.7mW @ 560Mhz	0.85mW @ 700Mhz
Output Range	30 ~ 650 MHz	40 ~ 510 MHz	0.18 ~ 600 MHz	2.4~378 MHz	200 ~ 750 MHz	450 ~ 1050 MHz
Supply Voltage	1.5 V	5V	1.0V	1.8 V	1.2 V	1.2 V
Lock Cycle		< 7 cycles	> 150 cycles	< 75 cycles	18 cycles	22 cycles
Resolution bit	12bits			DFC	8bits	11bits
Area	0.182 mm2	0.71 mm2	0.18 mm2	0.16 mm2	0.02mm2	0.0041mm2
Output Jitter (Pk-Pk) (% output period)	2.8 % @143MHz	1.7 % @240MHz	1.2 % @30.7MHz	4.8 % @30.4MHz	0.9 % @560MHz Long-Term-jitter)	1.38 % @700MHz
Power Factor	13mW	3mW	4.76mW	8.92mW	2.13mW	0.85mW

Table 6-2 Performance comparison of all-digital clock generator

6-2 Future Work

Recently, power dissipation is becoming an important constraint in a design. In the passage, most techniques to lower power consumption of integrated circuits

assume static behavior; that is, circuit and system parameters are chosen at design time to minimize power dissipation. In fact, in some applications adjusting the circuit during operation could save more power [6.1].

The new technique of power reduction is voltage scaling and lowering the operating clock frequency. Dynamic voltage and/or frequency control schemes have been reported in [6.2] ~ [6.5]. For low-power or mobile applications, ADPLL needs to provide a power-saving mode so that the system can turn off the ADPLL or scale down voltage if needed.

While the operating speed of microprocessors doubles every two years, memory access speed has not been improved accordingly even though memory density quadruples every three years. This imbalance has pushed memory systems to use a wide data bus and/or high-speed I/O interfaces in order to match the memory access speed with the microprocessor operating speed. However, increasing memory access speed with a wide data bus is practically limited by the maximum pin counts of memory and/or memory controller.

However, in the case of SDRAM, the memory access speed is up to the system clock speed, which is commonly less than 100 MHz. Double-data-rate (DDR) SDRAM achieves a memory access speed twice as fast as SDRAM by transmitting and receiving data at both rising and falling edges of the system clock.

Quadruple data rate (QDR) SDRAM transmits four consecutive data at a system clock edge, while keeping the compatibility with the conventional SDRAM interface. Fig 6-1 shows the overall block diagram of the QDR interface chip[6.8]. In order to

generate 4 clock signal internally, an internal PLL is used. The PLL generates 500-MHz eight-phase internal clock signals from a 125-MHz external clock signal. In the Future, we can modify proposed DCO to apply multi-phase DLL / ADPLL to QDR.

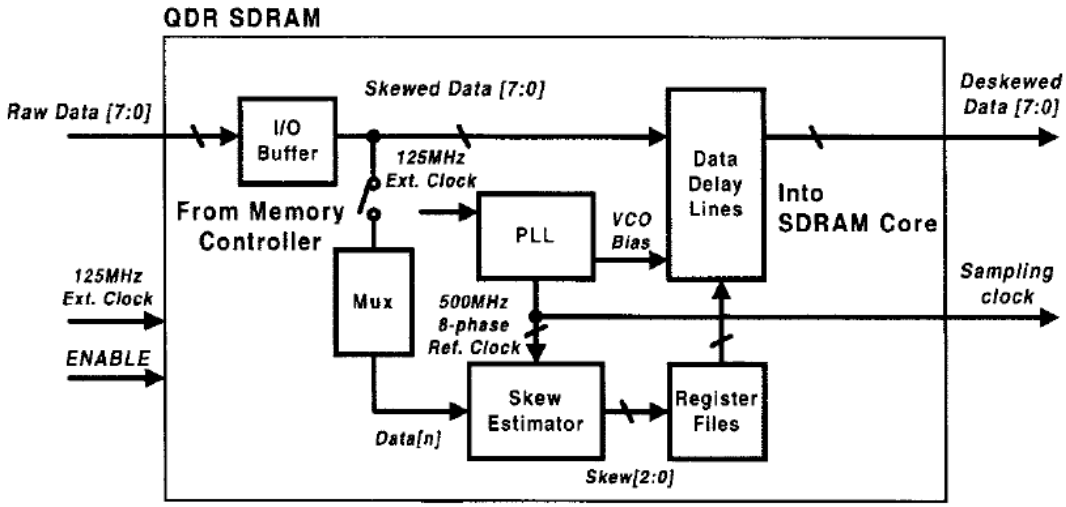

Figure 6-1 QDR interface chip[6.6]

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論文題目：超低功率高面積使用率全數位鎖相迴路頻率合成器

Ultra Low Power Area Efficient All Digital Phase-Locked Loop Frequency Synthesizer