

金氧半電晶體中通道不均勻 由 RTN 引發電流擾動效應

學生：薛至宸

指導教授：汪大暉 博士

國立交通大學 電子工程學系 電子研究所

摘要

本文中探討了在 90 奈米 CMOS 製程之下，口袋埋置效應對於 RTN 帶來的衝擊。我們的研究成果顯示了由於沿著通道方向不均勻的門檻電壓分布，口袋埋置構造將會造成雜訊特性的劣化。文中將會提出一個簡單的兩區模型來討論口袋埋置效應，並藉著對 SONOS 使用熱電子寫入的方式來確定口袋埋置結構確實會對 RTN 造成影響

本文中另外也探討了通道長度效應和 pMOS 之間的關係，當元件尺寸縮小，越小的通道長度將會因為口袋埋置濃度造成更嚴重的雜訊行為劣化。不同通道長度和不同口袋埋置濃度對元件造成的影響將會利用模擬的方式驗證。

Channel Non-uniformity induced Current Fluctuation due to Random Telegraph Noise in sub-100nm MOSFETs

Student : Chih Chen Hsueh

Advisor : Dr. Tahui Wang

Department of Electronics Engineering &

Institute of Electronics

National Chiao Tung University



The impact of pocket implant on Random Telegraph Signal Noise(RTN)in 90nm CMOS process is investigated. Our result shows that pocket implant will degrade device noise characteristic primarily due to enhanced non-uniform threshold voltage distribution along the channel. A simple Two-Region Model is proposed to take into account the pocket implant effect. By using SONOS channel hot electron programming, we confirm that pocket implant indeed has influence on RTN noise.

Length effect on pMOSFETs is studied in this thesis. As the device dimension scaling down, the shorter length device shows worse noise behavior due to pocket implant dose concentration. The influence of device characteristic of different pocket implant dose and different channel length is clarified by simulation.

誌謝

這篇論文的完成，首先要感謝吾師汪大暉教授跟馬渙琪學長的指導。沒有他們的指導，實驗的進行和模擬的分析將不可能進行得這麼順利。其次，要感謝李冠成同學的幫忙和包容，沒有與你一起進行實驗，進度不可能那麼快。

再者，要感謝實驗室的諸多學長們，David、鄭志昌、小兔等學長，除了學識上的解惑讓人無以為謝之外，精神上的支持讓這兩年過得十分平順。然後要感謝同期的冠成、冠潔和學弟們阿福、維哥、小鴨、阿雄和馬克吳，感謝你們在這兩年的碩士生活中帶來的笑談和支持。

最後，要感謝我的父母，沒有他們的包容與支持，我不會是今天的我。



Contents

Chinese Abstract	i
English Abstract	ii
Acknowledgements	iii
Contents	iv
Figure Captions	vi
Chapter 1 Introduction	1
Chapter 2 Fundamental of Random Telegraph Noise	3
2.1 Introduction	3
2.2 Random Telegraph Noise Theory	3
2.2.1 Gate Voltage dependence of RTNs	3
2.2.2 Electron Capture and Emission in RTNs	4
2.3 Measurement Setup of RTN	6
Chapter 3 Investigation and Characterization of Channel Non-uniformity induced RTN	12
3.1 Introduction	12
3.2 Two-Region Model Theory	12
3.3 Experiment and Statistic of RTN induced current fluctuation on sub-100 nm MOSFETs	13
3.4 Verification of Non-uniformity Threshold Voltage Effect by SONOS programming	15
Chapter 4 Investigation of Channel Non-uniformity Effect by Device Simulation	30
4.1 Introduction	30
4.2 Simulation of channel non-uniformity on pocket devices	30

Chapter 5	Conclusion	38
References		39



Figure Captions

- Fig 2.1 Two level RTN in the drain current of a MOSFET
- Fig 2.2 Band diagram in n-channel MOSFET. The dotted lines show the changes accompanying a positive increment in gate voltage δV_g . $\delta\phi_s$ is the change in surface potential. E_T and E_T' denote the trap energy–level positions before and after changing gate voltage. ϕ_b denotes the potential of the bulk Fermi level E_F with respect to the intrinsic level E_i .
- Fig 2.3 Configuration coordinate diagram : elastic + electronic energies against single normal coordinate. Empty circle means the empty trap plus a free electron in the inversion layer. Filled circle means the filled trap.
- Fig 2.4 Block diagram of experimental setup used for the measurement of RTN in MOSFETs
- Fig 2.5 The photograph of our micro – second measurement system
- Fig 3.1 Illustration of the pocket implant device.
- Fig 3.2 Simplified two region model for RTN in a pMOSFET. L_1 and L_2 represent pocket and channel region. n_1 and n_2 represent hole concentration in pocket and channel region.
- Fig 3.3 Measured linear I_d degradation versus stress time with low and high pocket devices.
- Fig 3.4 $I_{d,lin}$ degradation for low and high pocket device(W/L=1um/0.8um, 0.1um, 0.24um, 0.5um)
- Fig 3.5 Channel current recovery transient after stress in large area devices (W/L=10um/0.065um). Right part of dash line represents 4155

measurement range.

Fig 3.6 Normalized ΔI_{cp} with different gate length device. I_{cp} measured at $f=1\text{MHz}$

Fig 3.7 Comparison of the RTN amplitude for (a) low and (b) high pocket implant devices at the same drain current.

Fig 3.8 (a) Low and (b) high pocket induced RTN amplitude narrower and broader distribution in a small area pMOSFETs($W/L=0.12\mu\text{m}/0.08\mu\text{m}$)

Fig 3.9 The average amplitude of RTN in low and high pocket small area ($W/L=0.12\mu\text{m}/0.08\mu\text{m}$) devices versus gate length, L_{gate} .

Fig 3.10 Schematic representation of the SONOS structure and localized charge storage.

Fig 3.11 Band diagram of oxide charge tunnel trapping/de-trapping of oxide traps.

Fig 3.12 Simplified two-region model for RTN amplitude in a NROM cell. n_1 and n_2 represent the channel electron concentration in region 1 and region 2. L_1 and L_2 denote the length of each region. The amplitude of RTN is increased in non-uniform charge storage.

Fig 3.13 RTN amplitude versus ΔV_{th}

Fig 4.1 MOSFET device structure used in this simulation with channel length $0.06\mu\text{m}$

Fig 4.2 The $I_d V_g$ curves with different trapped charge concentration.

Fig 4.3 The $I_d V_g$ curves with different trapped charge locations.

Fig 4.4 The $I_d V_g$ curves with different pocket doped concentration.

Fig 4.5 ΔI_d versus different channel length.