Chapter 1

Introduction

In recent years, as the device dimensions continues to scale down, many new reliability issues have been faced. Meanwhile, many new technologies in process and structure have also developed to solve the problems. One of them is the pocket implant structure which is initially developed to control over short channel effect in small area devices. But as the device shrinks to certain dimension and below, the implant region carrier concentration will cause channel non–uniform voltage distribution and will degrade device noise characteristic, significantly increase random telegraph signal noise in device operating.

Random Telegraph Signal Noise(RTN), basically a single electron phenomenon, is also becoming a major concern in device scaling down process, especially becomes the considerate problem in analog and digital circuits operating and memory cell, because of its discrete switching behavior [1]. And our investigation shows that the non – uniformity caused by pocket implant will have larger influence on RTN with heavier dose concentration. Thus RTN, with the technology processing, will become a limitation in dimension shrinking because of its unpreventable existence.

Chap 2 starts with the fundamental Random Telegraph Signal Theory in MOSFET device. In the beginning, some introduction of noise will be reviewed briefly. After that, RTN theory is discussed. Finally, measurement setups of RTN will be shown and introduced.

Chap 3 deals with the channel non–uniformity effect in sub–100 nm pMOS devices. First, a Two–Region Model Theory will be introduced. Then the experiment setup and result will be shown. Finally, verification by SONOS channel hot electron

programming will be proposed to compare the non–uniform threshold voltage results we have by pMOSFET.

In Chap 4, we use simulation to verify current fluctuation on pocket effect. Using different carrier number, different trap location, and different channel length, we confirm our previous guess and the relationship with Two–Region Model. Finally, we will give a conclusion in Chapter 5.

Chapter 2

Fundamental of Random Telegraph Noise

2-1 Introduction

Although the research of noise started many decades ago, with devices dimension becoming smaller, those theories we have for low frequency noise are already incapable to be used and breakdown in this technology generation. The device is too small to contain only a small number of charge carriers. Instead, Random telegraph signal can successfully explain the noise behaviors in 90nm MOSFETs in many details [2]-[6]. In the beginning, the RTN theory will be discussed. After that, RTN and measurement setups will be shown.

2-2 RTN Theory

The random telegraph signal noise, generated through the trapping/de-trapping of a single electron at an individual defect residing in the oxide close to the Si/SiO_2 interface [7], with a discrete switching of the current between two or more levels at a constant bias, as shown in Fig 2.1. In small enough devices, normally, only trap energy level within a few kT from the Fermi level would make current fluctuation. k and T are the Boltzmann's constant and equilibrium temperature, respectively. Traps with energy levels several kT below the Fermi level would be permanently filled while traps with energy levels several kT above the Fermi level would be permanently empty, resulting in negligible noise power.

2-1-1 Gate Voltage dependence of RTNs

Only trap energy level near electron energy level within a few kT will RTN be generated, makes RTN having gate dependence characteristic [1]. Fig 2.2 shows a simply band diagram as we apply Vg in a small area MOSFET, which there is only one trap energy level E_T within $k_B\theta$ of the surface Fermi level E_F. The increment in Vg is shown by the dash line. Notably, the energy separation $E_T - E_F$ decreases as Vg increases. For this linear region, the occupancy of the defect can be expressed as ：

$$\frac{\bar{\tau}_c}{\bar{\tau}_e} = g \exp\left(\frac{E_T - E_F}{kT}\right)$$ where g is a degeneracy factor

2-2-2 Electron Capture and Emission in RTNs

Actually, RTN is formed through a series multi-phonon mechanism. Fig 2.3 [1] shows the detailed changes in total energy when an electron is moved from the inversion layer to an interface trap. But here we simply discuss a two–level RTN mainly defined by three parameters：the time spent in the high current state τ_c, the time spent in the low current state τ_e, and the amplitude ΔI, as illustrated in Fig 2.1 with time interval 20ms. The RTN has been measured in the drain current I_d of a small area device that the high and low times were exponentially distributed, and thus the switching is governed by $\frac{1}{\bar{\tau}_c}$ and $\frac{1}{\bar{\tau}_e}$. τ_c and τ_e follow a Poisson distribution relationship [1][8], given by：

$$P_{c,e}(t) = \frac{1}{\tau_{c,e}} \exp\left(-\frac{t}{\tau_{c,e}}\right)$$

The average values of $\bar{\tau}_c$ and $\bar{\tau}_e$ are given by τ_c and τ_e, defined as high and low time constants. They usually correspond to a trap site empty or occupied. In

other words, to the average carrier capture or emission time, the current difference between the max and the min is defined as ΔI and the two state of the drain current represents clearly two – level RTN.

The carrier capture rate for an interface defect can be expressed as：

$$\frac{1}{\bar{\tau}_c} = \int_{E_c}^{\infty} r(E)dE \qquad \text{Eq.2-1}$$

Where $r(E)$ is the transition rate per unit energy at energy E in the inversion layer, and can be expressed as：

$$r(E) = n(E)\upsilon(E)\sigma(E)$$

Where $n(E)$ represents the inversion layer density at energy level E, $\upsilon(E)$ and $\sigma(E)$ represents the carrier velocity and cross section at energy level E, respectively.

Supposed that the particle density in the inversion layer is constant n, and so is υ_{th} the average thermal velocity and σ the average capture cross section, we can simplify Eq.2-1 as：

$$\frac{1}{\bar{\tau}_c} = n\upsilon_{th}\sigma$$

Where $\sigma = \sigma_0 \exp\left(-\frac{\Delta E_B}{kT}\right)$. σ_0 means the capture cross section pre–factor. The activation energy ΔE_B is the lattice energy needed for a crossing of the conduction band with the bound state.

As for the characteristic time for electron emission τ_e, depends on the activation energy, ΔE_{ct}, defined as the energy difference between the conduction band edge and the trap energy level [1]：

$$\tau_e = \frac{\exp\left(\frac{\Delta E_{ct}}{kT}\right)}{N_c \upsilon_{th} \sigma}$$

Where N_c is the density of states in the conduction band.

2-3 Measurement of RTN noise

Cause RTN noise is characterized by three parameter：the average of the high and low time constants and magnitude of the current fluctuation, the range of the time constants is from mili–seconds to seconds. In order to obtain a reasonable estimate of high and low states of RTN, a micro–second measurement system is needed. Fig 2.4 shows the basic circuit we used for our measurements of nano–scaled MOSFETs at room temperature. Fig 2.5 shows the photograph of our micro–second RTN noise measurement system. The MOSFET bias voltage（V_D,V_G）are all controlled by batteries with tuning resistor, V_{SUB} is connected to Agilent-4155C Semiconductor Parameter Analyzer, and V_S is connected to a virtual grounded amplifier and will be converted to source current with a 100$k\Omega$ feed back resistor. With fast enough circuit sampling rate, the current fluctuation will be extracted and shown on oscilloscope.

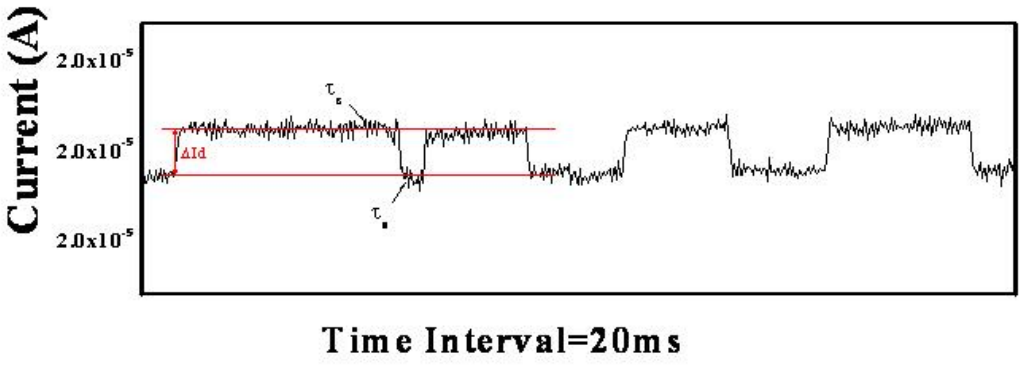

Fig 2.1 Two level RTN in the drain current of a MOSFET

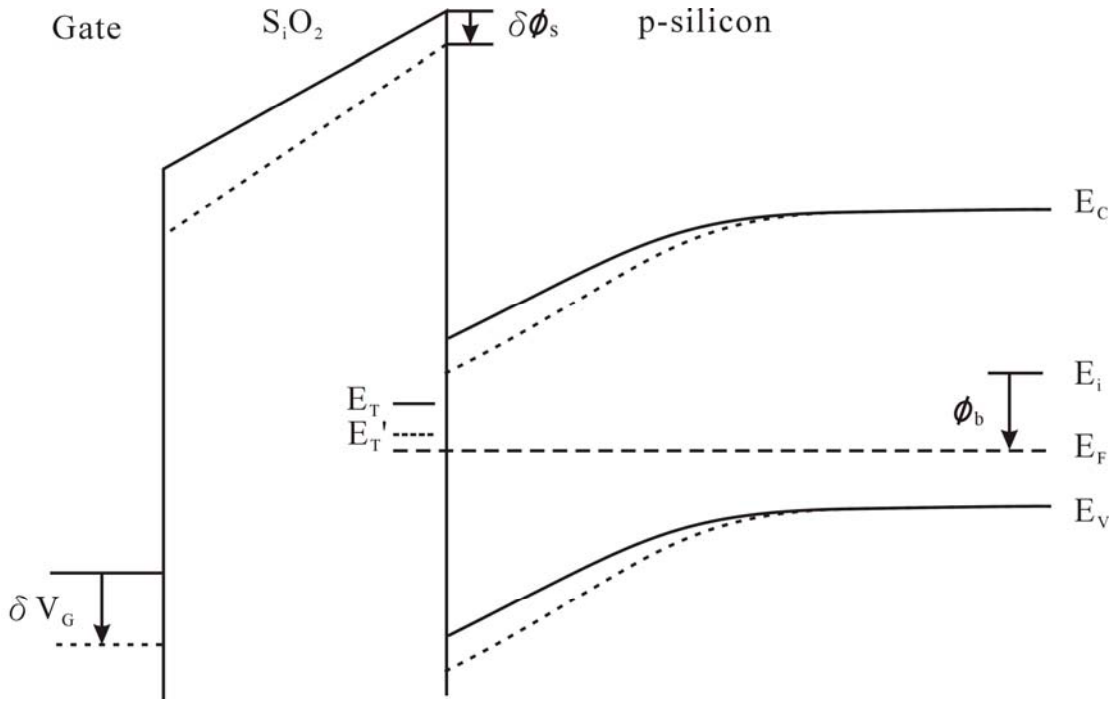

Fig 2.2 Band diagram in n-channel MOSFET. The dotted lines show the changes accompanying a positive increment in gate voltage δV_g. $\delta\phi_s$ is the change in surface potential. E_T and E_T' denote the trap energy–level positions before and after changing gate voltage. ϕ_b denotes the potential of the bulk Fermi level E_F with respect to the intrinsic level E_i.

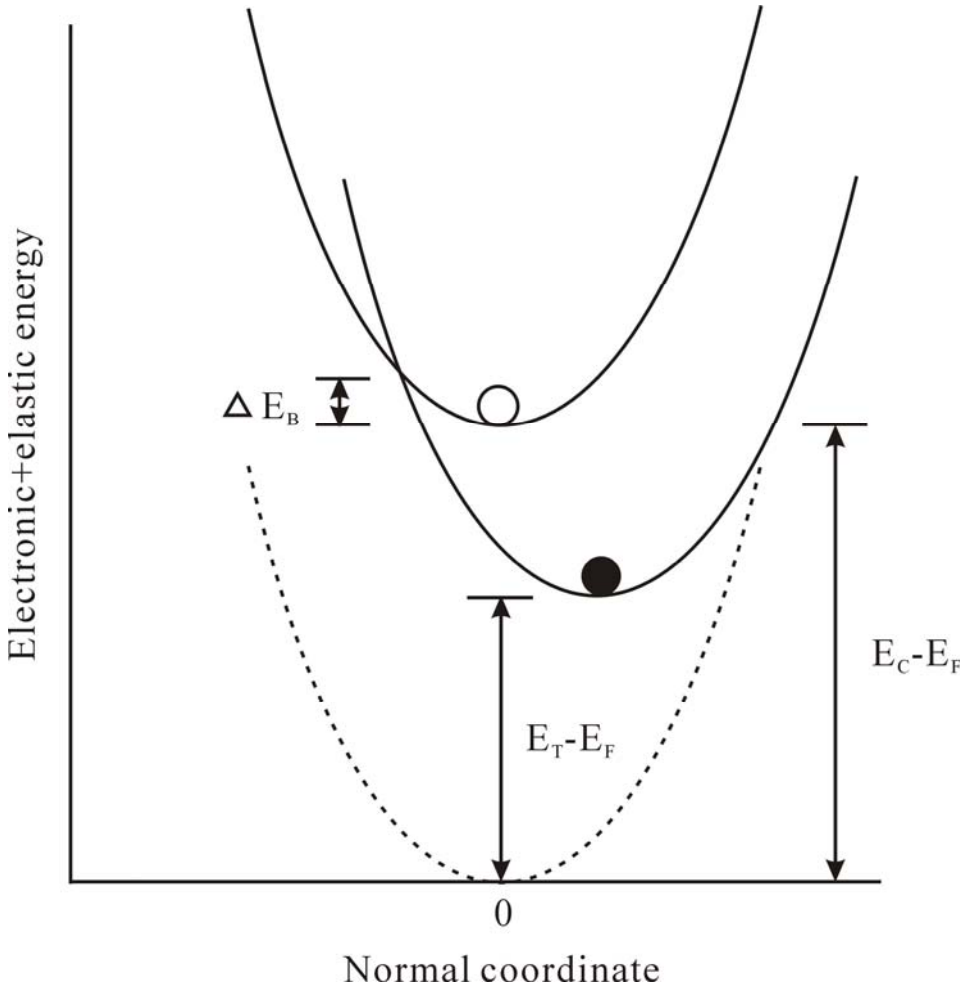

Fig 2.3 Configuration coordinate diagram：elastic + electronic energies against single normal coordinate. Empty circle means the empty trap plus a free electron in the inversion layer. Filled circle means the filled trap.

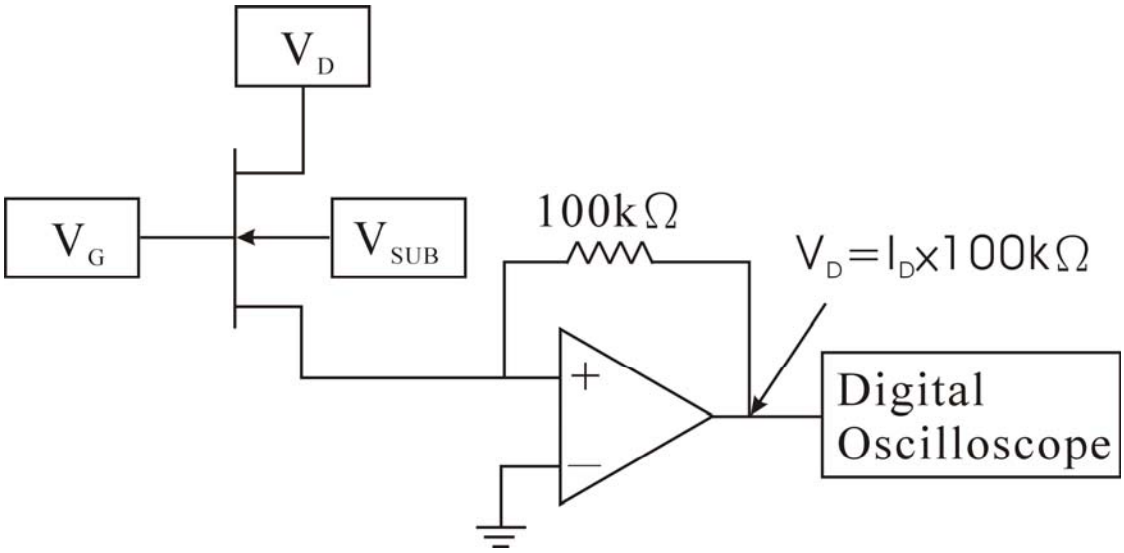

Fig 2.4 Block diagram of experimental setup used for the measurement of RTN in MOSFETs

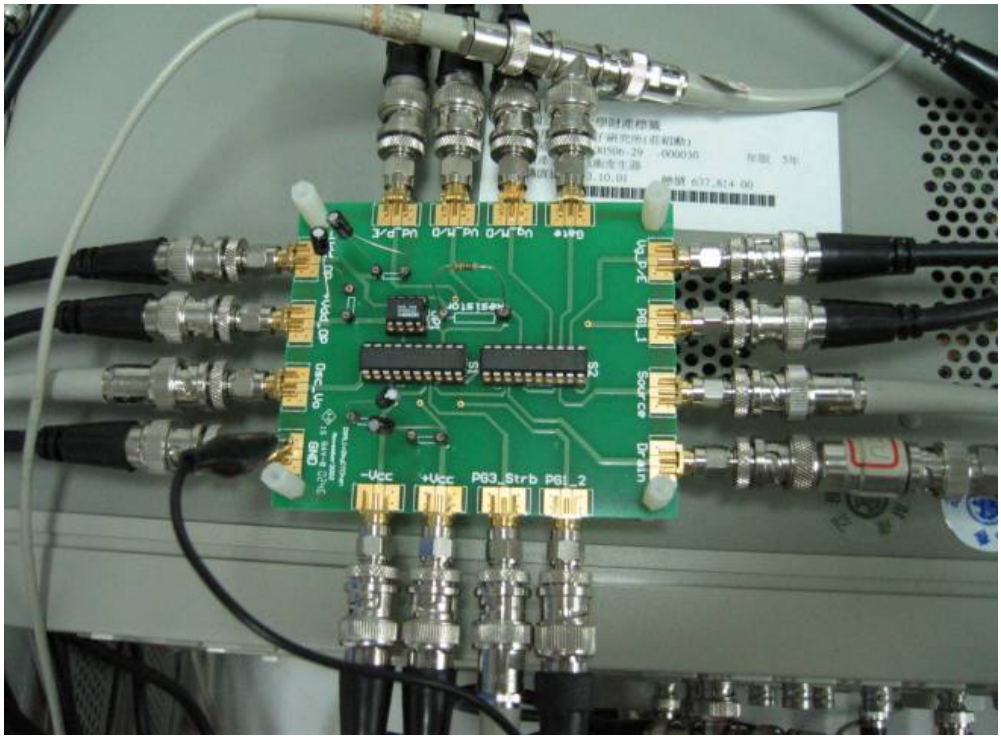

Fig 2.5 The photograph of our micro – second measurement system

Chap 3

Investigation and Characterization of Channel Non-uniformity induced RTN

3-1 Introduction

After entering sub–100nm MOSFETs generation, short channel effect（SCE）has already become an important reliability issue. To suppress SCE problem, pocket implant is thus developed. Fig 3.1 shows the pocket implant pMOS. Two high dosage pocket were implanted under channel and beside S/D side. High concentration with abrupt profiled pocket region makes depletion region smaller, preventing from additional depletion region extension, and thus SCE can be released. But pocket implant also brings about other reliability problems. A difference up to 25% linear I_d degradation arising from pocket implantation is observed, and will be discussed in the following paragraph.

3-2 Two–Region Model Theory

The total channel length cab be viewed as a pocket region of a length L_1 in series with a non–pocket region of a length L_2, as shown in Fig 3.2 [9] , a pMOSFET. Due to its locally higher threshold voltage, the inversion carrier density n_1 is lower than that of the pocket region, and ΔI_d can be expressed as：

$$\Delta I_d(RTS) \propto \frac{1}{\left(L_1 + L_2 \frac{n_1}{n_2}\right)^2} \qquad \text{Eq.3-1}$$

In a enough long channel device（ $L_2 >> L_1$ ）, the contribution from the pocket region can be neglected, because of the negligible pocket effect. For a uniformly doped channel, Eq.3-1 can be simplified as [10]：

$$\Delta I_d(RTS) \propto \frac{1}{(L_1 + L_2)^2} \qquad \text{Eq.3-2}$$

In a short channel device with comparable L_1 and L_2 and high pocket dose region（ $n_1 << n_2$ ）, Eq.3-1 can be approximated as：

$$\Delta I_d(RTS) \propto \frac{1}{L_1^{\,2}} \qquad \text{Eq.3-3}$$

ΔI_d of low pocket dose will between Eq.3-1 and Eq.3-2, because of a smaller difference between n_1 and n_2. Thus high pocket devices give a larger ΔI_d and a stronger L_{gate} dependence than low pocket ones.

3-3 Experiment and Statistic of RTN induced current fluctuation

The devices in our experiment are pMOSFETs with a nitride oxide of 1.9nm, a gate length(L_{gate}) of 65nm～0.5um, and a gate width of 0.12um～10um. Two devices with different pocket implant dosage(, called ‘high’ and ‘low’ pocket） are compared. To compensate for the difference in V_t due to distinct pocket profile, a fixed stress/measurement gate over–drive voltage($V_g - V_t$) is used, rather than a fixed V_g. Unless additional indicated, the stress condition is $V_g - V_t = -1.8V$ with other terminals grounded, and the measurement condition is $V_g - V_t / V_d = -0.35V / -0.1V$ where linear drain current（ $I_{d,lin}$ ） is monitored to facilitate fast measurement.

Utilizing a fast transient measurement setup [11], linear drain current degradation

（$\Delta I_{d,lin}$）after stress is shown in Fig3.3 for high and low pocket devices with L_{gate} = 0.08um and 0.24um. Fig 3.4 indicates for a stress time of 1000s the L_{gate} dependence of $\Delta I_{d,lin}$. Three observations can be summarized：(a) $\Delta I_{d,lin}$ is larger for a smaller L_{gate}. (b) The L_{gate} effect is more pronounce in the low pocket set. (c) The difference between high and low pocket sets grows with scaling L_{gate}（$\Delta I_{d,lin}$ higher is observed for L_{gate} = 0.08um）. The necessity of the fast transient measurement is worth mentioning. Shown in Fig 3.5 is the drain current recovery right after releasing the stress voltage. The longer the elapsed time, the smaller the $\Delta I_{d,lin}$ difference between high and low pocket sets. Since a conventional stress-and-method has a switching delay long as seconds, the pocket effect on $\Delta I_{d,lin}$ might be underestimated or even neglected.

$\Delta I_{d,lin}$ is determined by the number of trapped charges and the extent to which these charges can change the drain current. By using a charge pumping technique, Fig 3.6 shows that the oxide (interface) trap density of the two pocket split is about the same, suggest interface trap creation is independent of L_{gate}/pocket, though some researchers attributed the increase of noise to additional oxide trap creation by pocket implantation. Higher trap density at gate edges [12] for high pocket devices, can be excluded as the reason for the L_{gate}/pocket effect as in Fig 3.3 and Fig 3.4.

To investigate the role of the latter, random telegraph signal noise（RTN） in drain current [13] is performed, involving direct measurement of discrete charge trapping/de-trapping. Fig 3.7 shows the RTN measurement result. Obviously, the

amplitude of the current change in high pocket device is larger in RTN measurement result. This suggests that for an identical number of charges into/out of the traps, the corresponding ΔI_d is larger in high pocket devices. In addition, a high pocket dose gives rise to a broader distribution of RTN ΔI_d as shown in Fig 3.8. Fig 3.9 also indicates the average RTN ΔI_d as function of L_{gate}.

3-4 Verification of non–uniform threshold voltage effect by SONOS programming

In this chapter, we will use SONOS memory device in order to verify our result about the channel non-uniformity induced current fluctuation in pocket implant devices. The SONOS cell, as shown in Fig 3.10, is made of a nMOSFET with an oxide-nitride-oxide stack gate dielectrics. Charges can be stored in the nitride layer by uniform injection or by localized injection. For example, channel FN injection has uniform electron storage while channel hot electron injection has localized charge storage. Here we use channel hot electron programming in SONOS to create an electron package in nitride layer and negative FN stress to erase the electron package. After programming, non–uniform charge package store in a SONOS cell nitride layer can create a localized high voltage region and increase the read current fluctuation, just the same as the pocket device, in order to simulate the condition we met in our previous experiment.

The SONOS cells used in this work are W/L=0.12um/0.24um. A computer–controlled system including an amplifier and Agilent 4155C Semiconductor Parameter Analyzer is used to stress and monitor read current fluctuation.

In this experiment, we use channel hot electron program and negative FN erase for P/E cycling. For the P/E mode, the program voltage is V_{gate} / V_d = 6.5V/4.5V by

CHE, and the erase voltage is V_{gate} = -8V with other terminals grounded by negative FN stress. By controlling the stress time, we can change the electron quantity in the nitride layer. The programming time is 1e-7, 5e-7, 1e-6, 5e-6 second, and the erase time is 1e-5 second. The read current level is controlled near to 1uA corresponds to the current we measured in pMOSFET pocket devices for the same channel carrier number. In order to avoid the programmed electron package spreading by continuous programming, one program for one measurement is performed, and will erase the electron for the next different programming time and measurement.

The RTN exhibits two or more levels transition and results from trapping/de-trapping of oxide traps. Illusion of oxide charge tunnel trapping/de-trapping in read mode is depicted in Fig 3.11. A simplified two–region RTN model for a SONOS cell is derived in the Fig 3.12, just the same as mentioned previously in 3-2. The model reveals that the RTN amplitude increases with programmed V_t for a larger ratio of n_2/n_1, which n_1 and n_2 represent channel carrier density in pocket region and non–pocket region, respectively. Fig 3.13 shows RTN amplitude versus programmed V_t

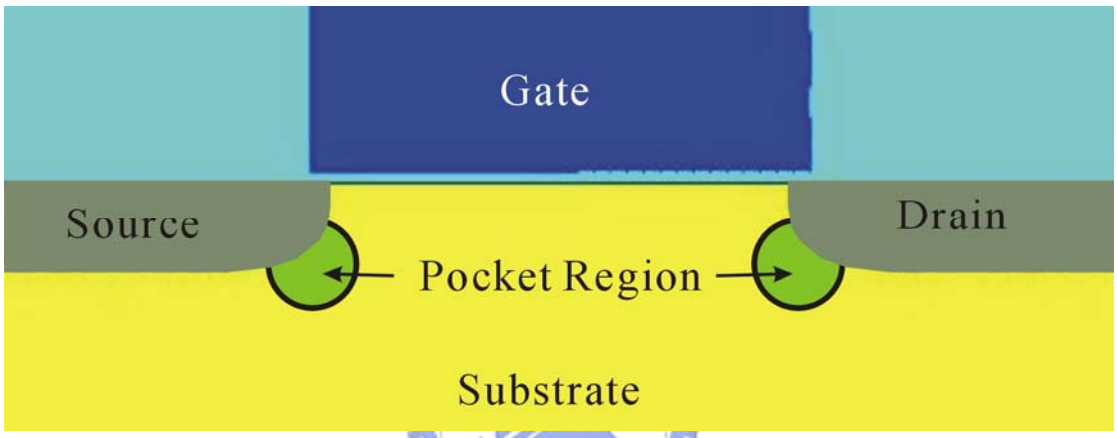

Fig 3.1 Illustration of the pocket implant device.

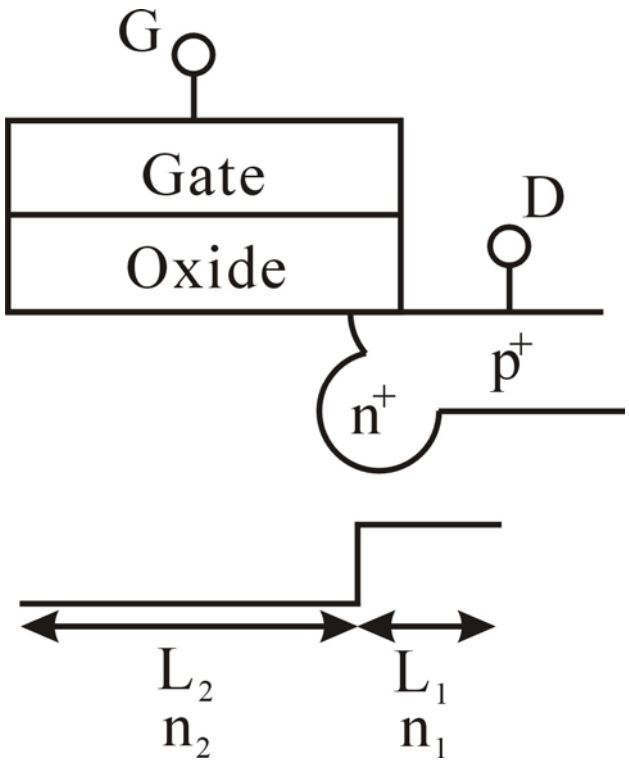

Fig 3.2 Simplified two region model for RTN in a pMOSFET. L_1 and L_2 represent pocket and channel region. n_1 and n_2 represent hole concentration in pocket and channel region.

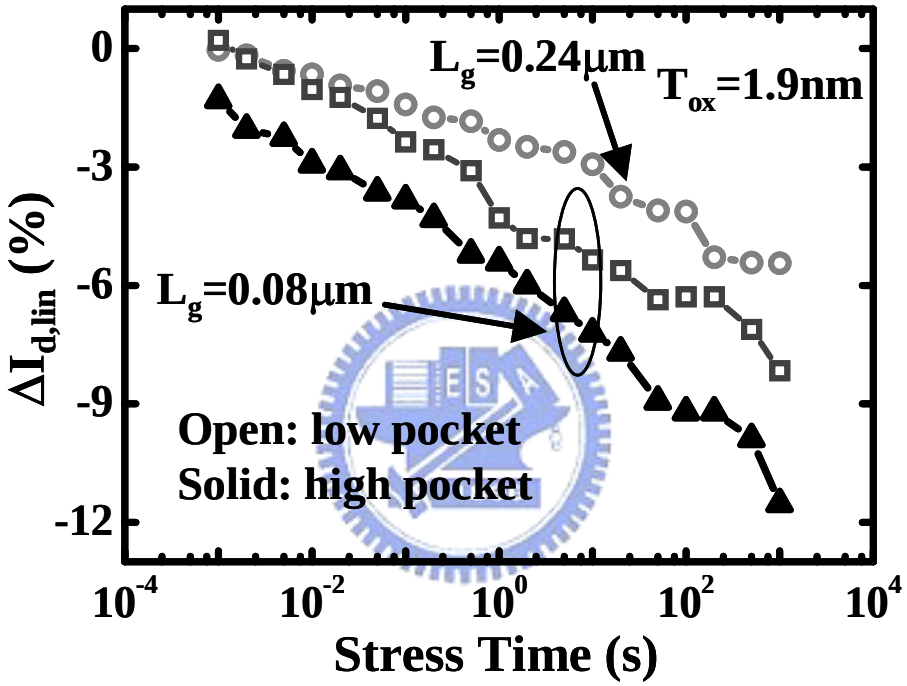

Fig 3.3 Measured linear I_d degradation versus stress time with low and high pocket devices.

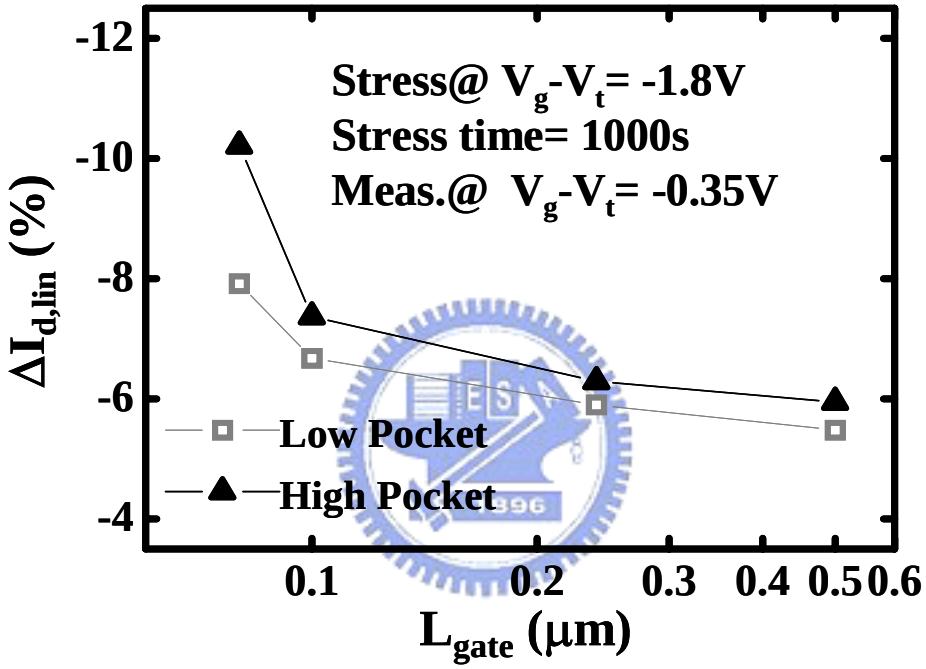

Fig 3.4 $I_{d,lin}$ degradation for low and high pocket device(W/L=1um/0.8um, 0.1um, 0.24um, 0.5um)

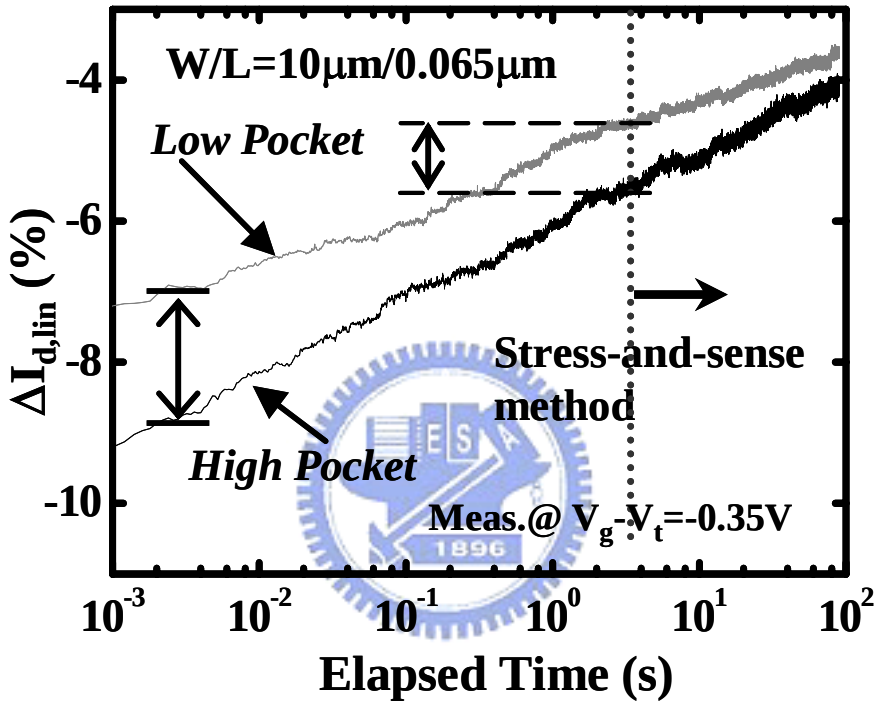

Fig 3.5 Channel current recovery transient after stress in large area devices (W/L=10um/0.065um). Right part of dash line represents 4155 measurement range.

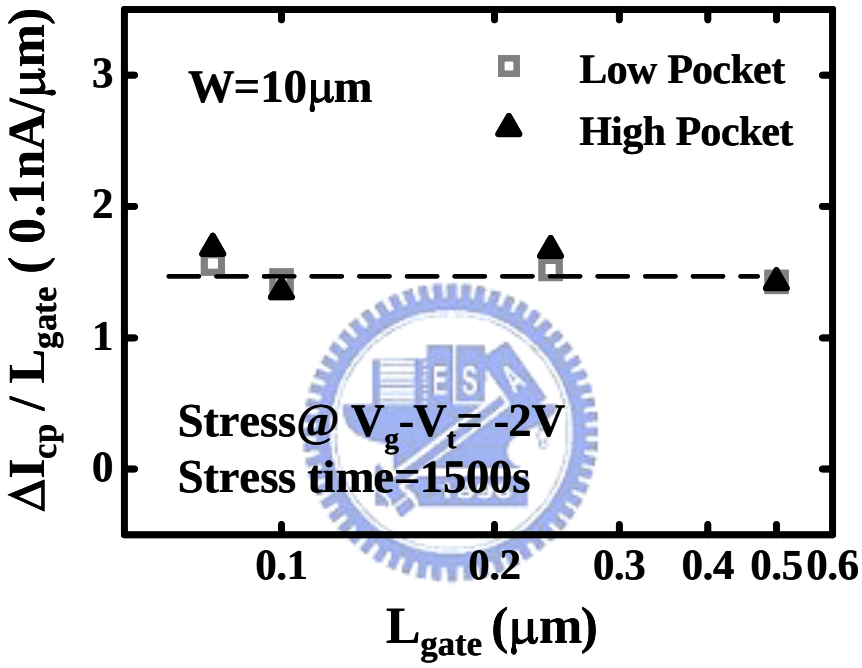

Fig 3.6 Normalized ΔI_{cp} with different gate length device. I_{cp} measured af f=1MHz

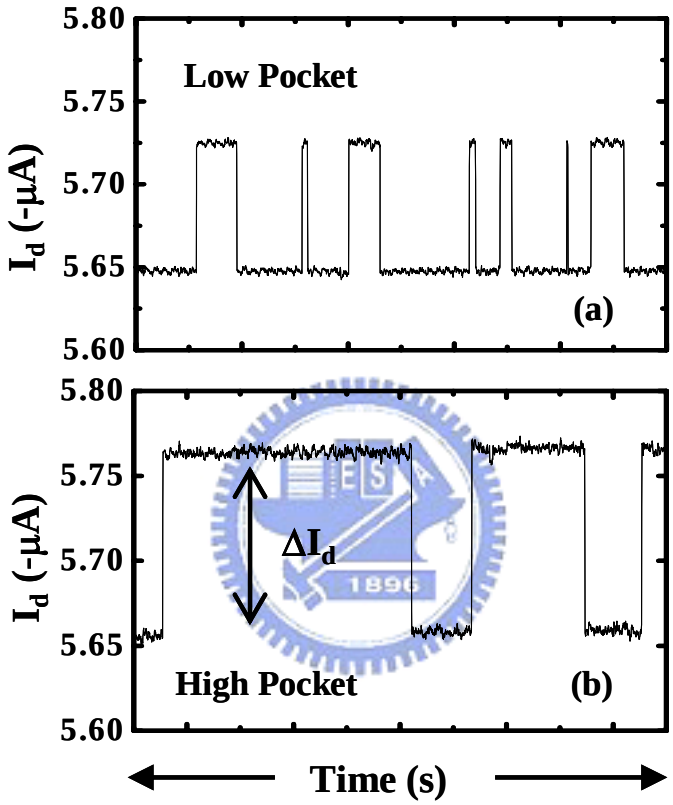

Fig 3.7 Comparison of the RTN amplitude for (a) low and (b) high pocket implant devices at the same drain current.

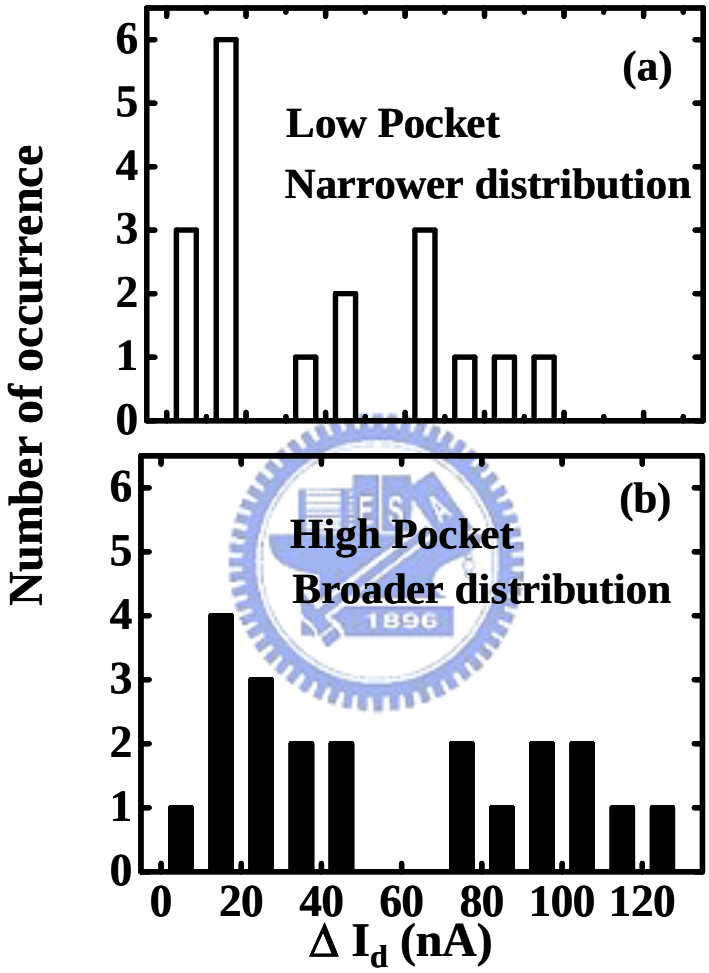

Fig 3.8 (a) Low and (b) high pocket induced RTN amplitude narrower and broader distribution in a small area pMOSFETs(W/L=0.12um/0.08um)

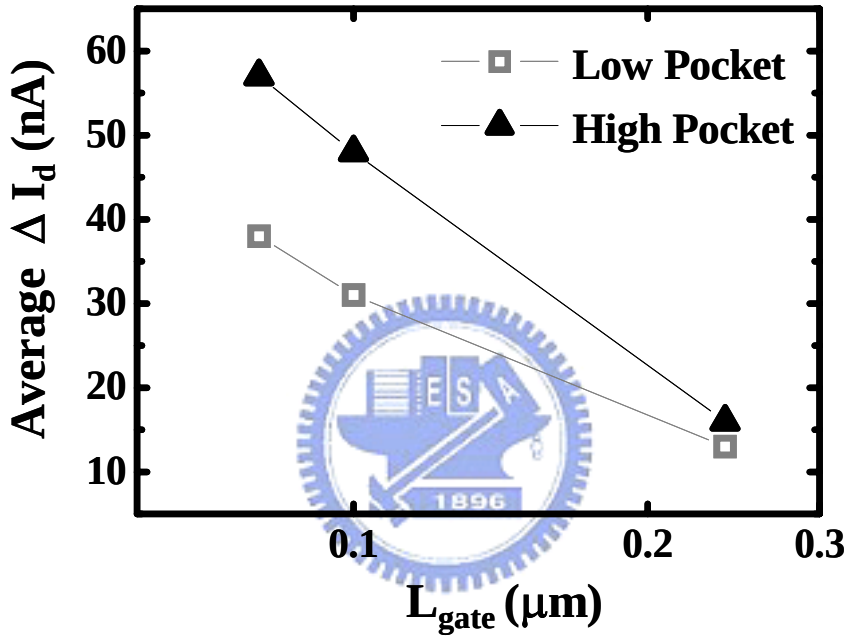

Fig 3.9 The average amplitude of RTN in low and high pocket small area (W/L=0.12um/0.08um)devices versus gate length, L_{gate} .

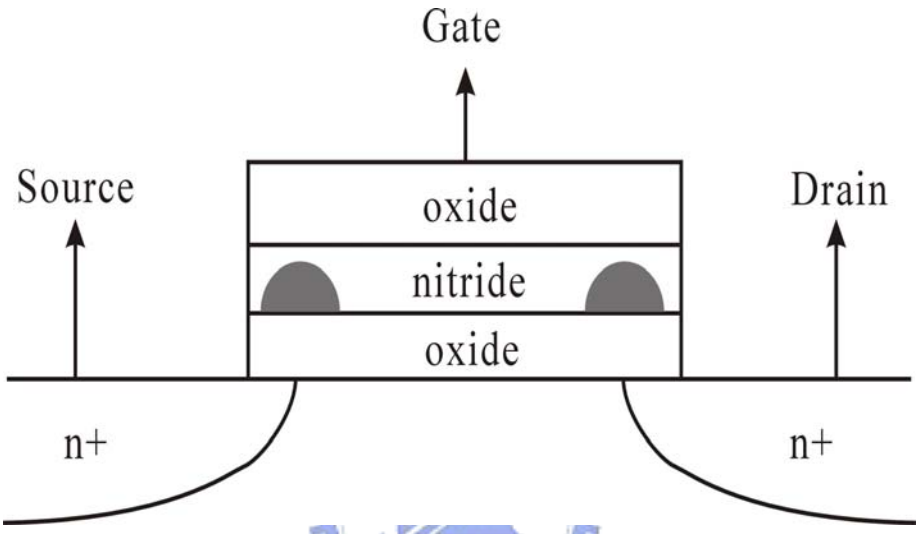

Fig 3.10 Schematic representation of the SONOS structure and localized charge storage.

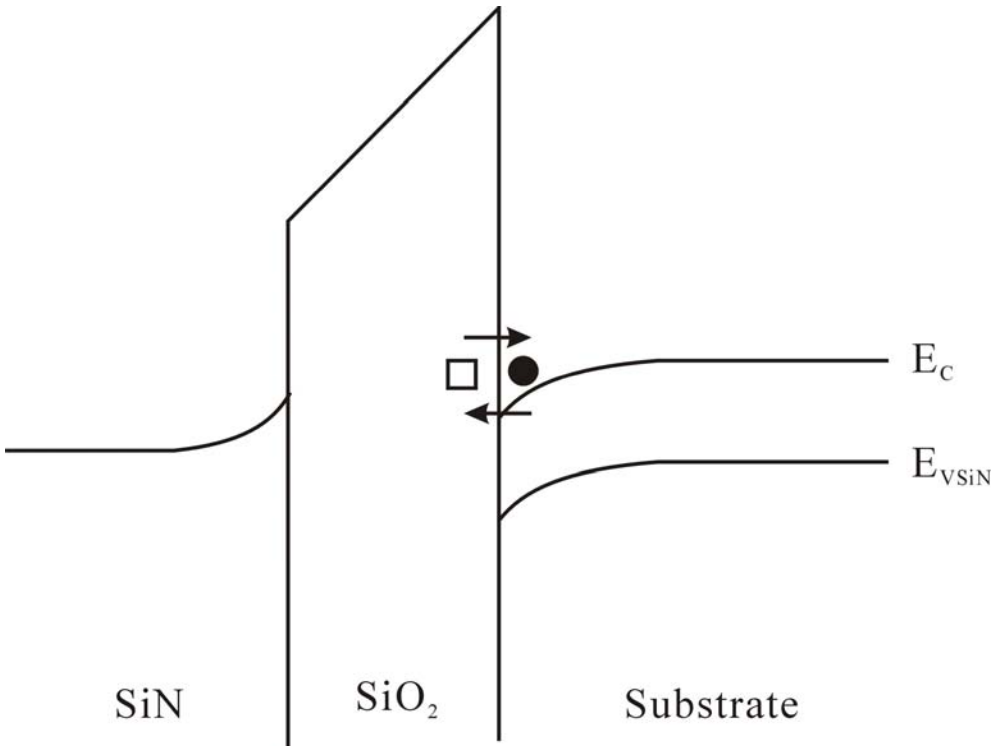

Fig 3.11 Band diagram of oxide charge tunnel trapping/de-trapping of oxide traps.

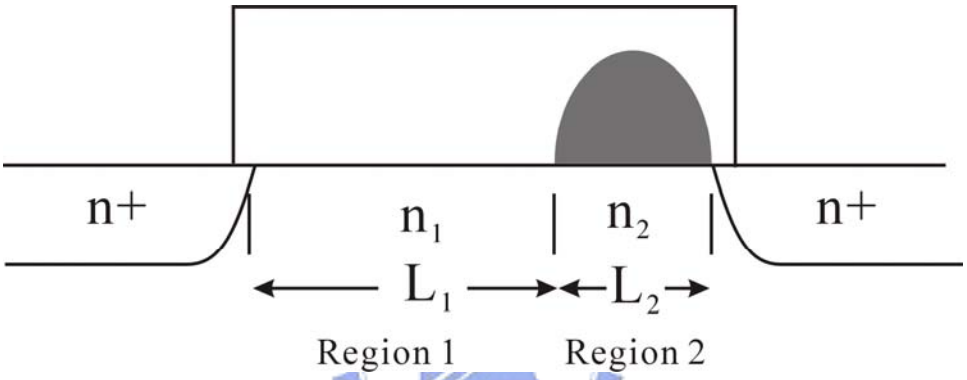

Fig 3.12 Simplified two–region model for RTN amplitude in a NROM cell. n_1 and n_2 represent the channel electron concentration in region 1 and region 2. L_1 and L_2 denote the length of each region. The amplitude of RTN is increased in non–uniform charge storage.

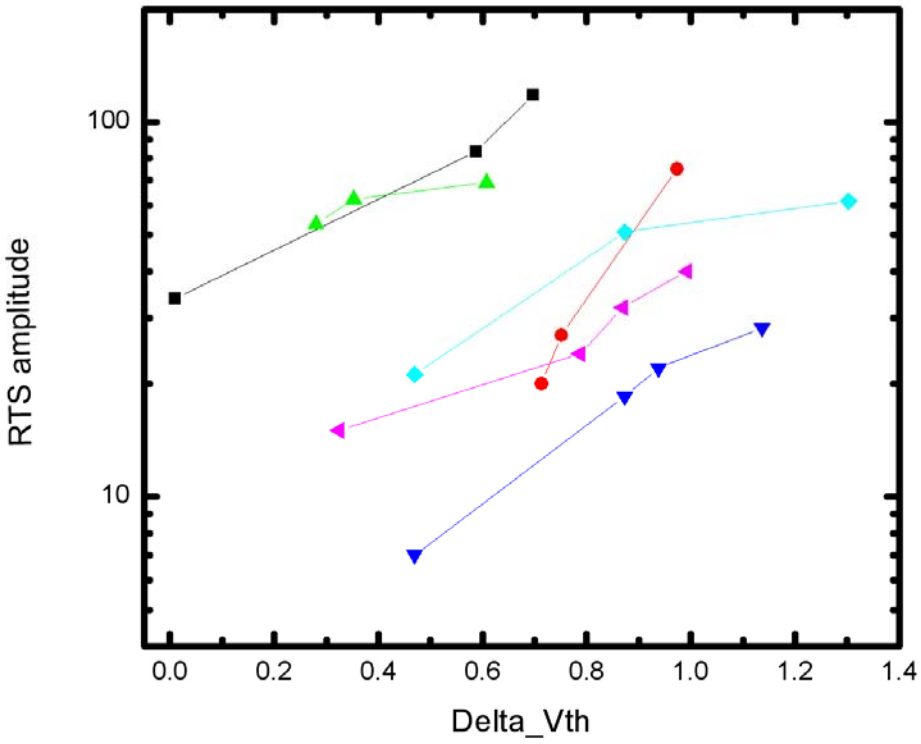

Fig 3.13 RTN amplitude versus Delta_Vth

Chapter 4

Investigation of Channel Non-uniformity Effect by Device Simulation

4-1 Introduction

The channel non–uniform distribution by pocket implant is simulated by using a two–dimensional device simulator, MEDICI. Pocket implantation not only affects the distribution of channel carriers in the vertical direction but also affects the threshold voltage distribution in the channel direction. Many different conditions of the channel carrier non–uniform distribution will be performed in order to compare those experiment results we have met in the previous chapter.

4-2 Simulation of channel non–uniformity on pocket devices

This section focuses on various pocket implantation conditions. We will present simulation result about threshold voltage shift for four different condition： (a) Four different trapped charge concentrations（ Q_f ） located at interface between the oxide and the channel are discussed. (b) Three different trapped charge locations along the channel are investigated. (c) Three different pocket implant concentrations are demonstrated. (d) Three different kinds device channel length are simulated. Device structure used in our simulation is pMOSFETs, as illustrated in Fig 4.1 with channel doped $10^{18}cm^3$. Drain voltage is controlled at 0.1V, and trapped charge is set to distributed within a small region 0.004um along the channel.

Fig 4.2 shows the threshold voltage shift by IdVg curves. The different factor

between the four pictures is the trapped charge concentration along the channel. The different trapped charge concentrations are -3.33e11/cm^2, -6.55e11/cm^2, -1e12/cm^2, and -2e12/cm^2, respectively. Trapped charge location is just above the pocket region in the drain side. In order to control the electron particle number, -3.33e11/cm^2 is used. In our device, with distributed region length 0.004um for trapped charge in the x coordinate and width 0.1um in the y coordinate, we can calculate the electron number we want. Thus for trapped charge concentration -3.33e11/cm^2, we will have：

$$3.33*10^{11}*4*10^{-7}*1*10^{-5}=1.332$$

Nearly only one electron will be set, and two particles, four particles, eight particles correspond to -6.66e11/cm^2, -1e12/cm^2, -2e12/cm^2, respectively.

Although pocket implantation can reduce the short channel effect, it also comes with locally increased potential beside source and drain side. With increased potential along the channel, channel carriers will be much fewer in the pocket region than in the channel region. Meanwhile, if we have trap near the interface and RTN happens, fewer carriers will thus induced larger current fluctuation.

Fig 4.3 also shows the threshold voltage by IdVg curves. The different factor between the four curves is the trapped charge location. Location above the drain side, the channel center and the source side is set. In this result, we can find that trapped charge above the drain side and the source side has nearly the same contribution to the threshold voltage shift, much larger than just above the channel center. In this simulation trapped charge concentration is controlled at -3.33e11/cm^2, and channel length 0.06um, as for only one electron particle.

Fig 4.4 show the threshold voltage by IdVg curves with different pocket implant split：no pocket, 1e19/cm^3, and 2e19/cm^3. Trapped charge location is set just above

the drain side, and its concentration is controlled at -3.33e11/cm^2 , and channel length 0.06um. As we can see form this figure, the larger the pocket implant concentration, the larger the threshold voltage shift, in order to maintain the same current flow. Thus carrier above the pocket region will much less than above the channel region, and the ration n_2/n_1 will increase, making the pocket effect more serious.

Fig 4.5 shows the threshold voltage by IdVg curves with different channel length. Different channel lengths are 0.06um, 0.1um, and 0.12um. Trapped charge concentration is still controlled at -3.33e11/cm^2 just above the pocket region, with pocket split 1e19/cm^3. As we mentioned in Two–Region Model Theory, the current fluctuation is dominated by the channel length and the channel carries concentration ratio. As length shrink, pocket region length will increase its importance in the equation, and will predictably cause serious RTN.

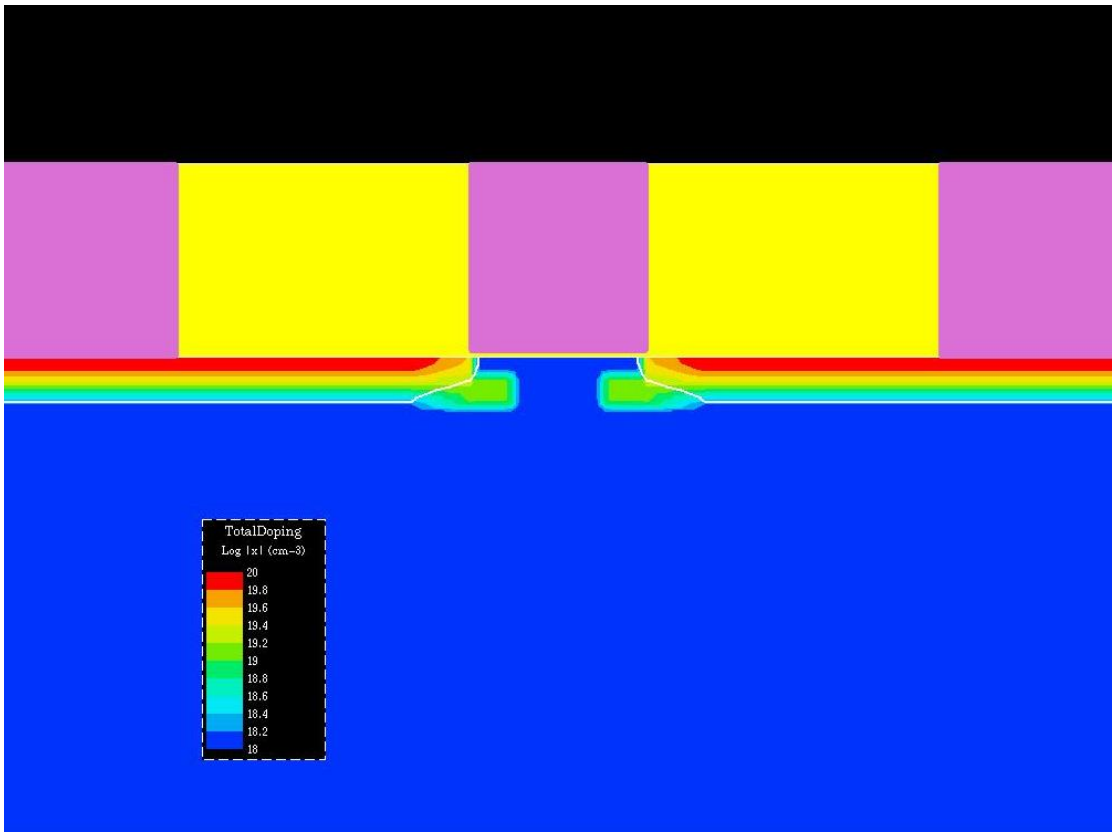

Fig 4.1 MOSFET device structure used in this simulation with channel length 0.06um

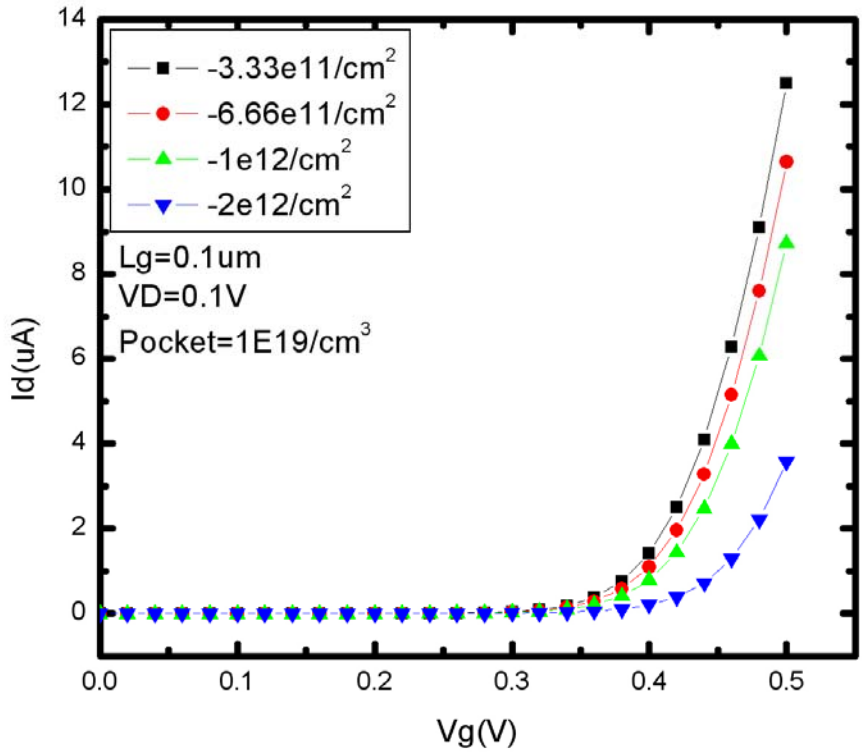

Fig 4.2 The IdVg curves with different trapped charge concentration.

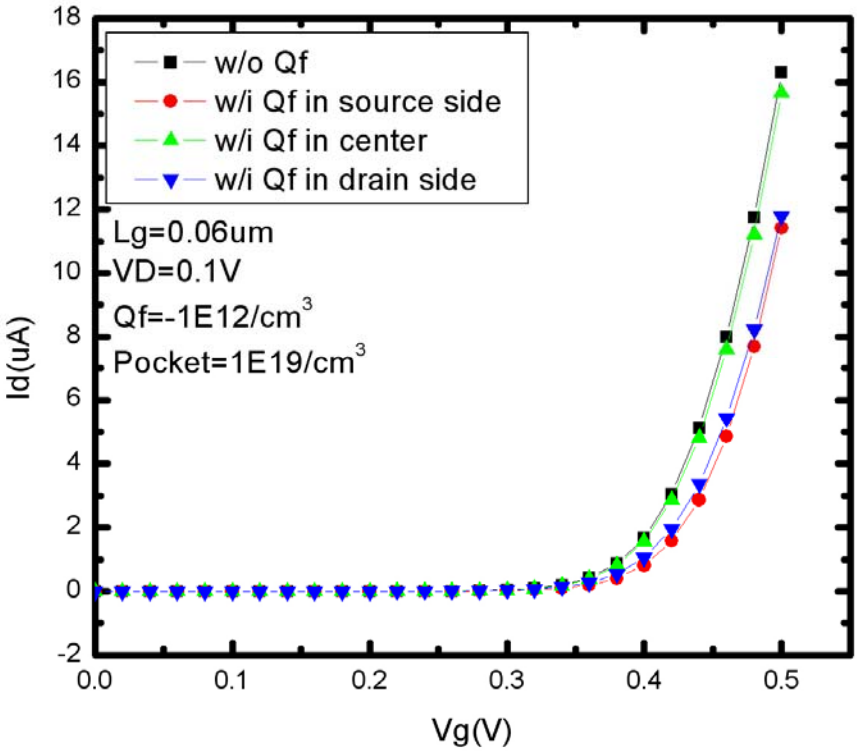

Fig 4.3 The IdVg curves with different trapped charge locations.

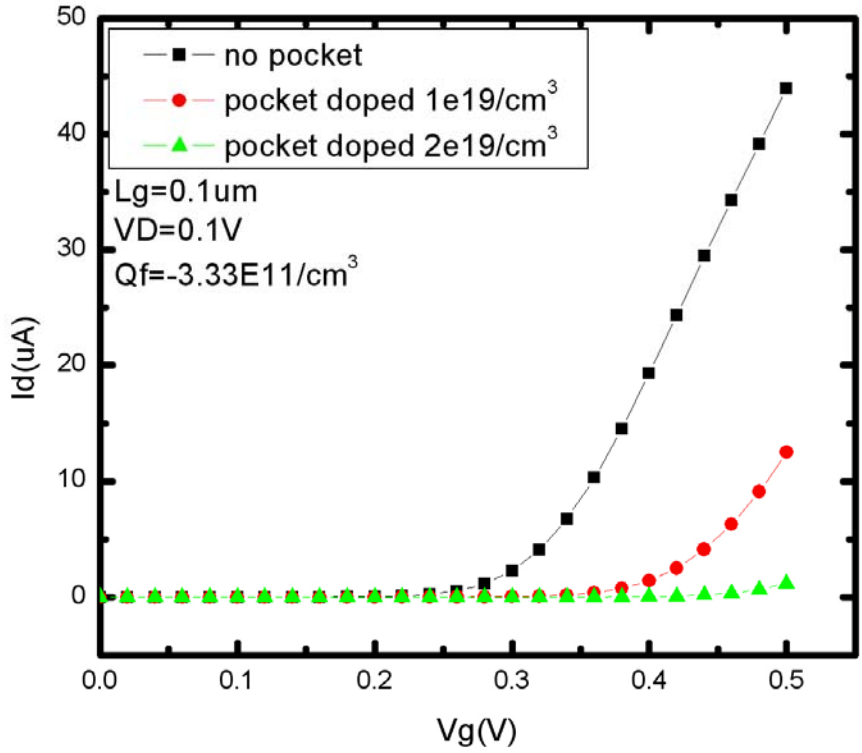

Fig 4.4 The IdVg curves with different pocket doped concentration.

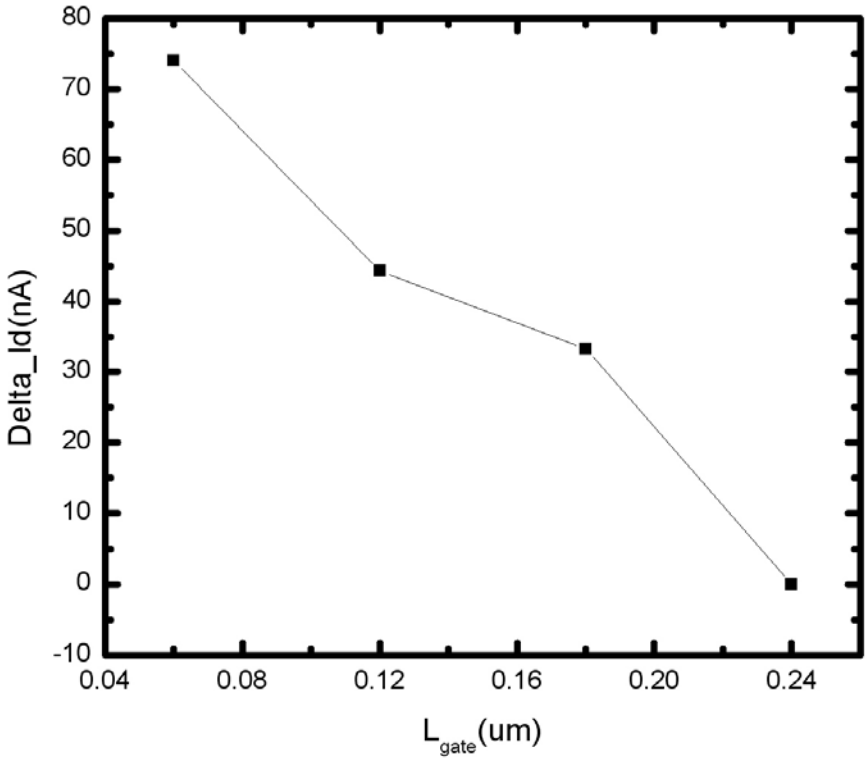

Fig 4.5 Delta_Id versus different channel length.

Chapter 5

Conclusion

The study has investigated the RTN induced degradation phenomenon due to pocket implant effect in nano–meter regime MOSFETs is demonstrated. Rather than a weaker dielectric robustness at gate edges, the root cause is the growing impact of trapped charges in the gate dielectrics on channel current as a result of stronger V_t non–uniformity given by a high pocket implant. The observed pocket and gate length effects can be qualitatively explained with a simple two–region model.

An experimental evidence of non–uniform threshold voltage effect on RTN is obtained in a SONOS cell, in order to simulate the pocket region in MOSFETs. We find that the drain current noise will be significantly increased by CHE programming. Finally, by MEDICI simulation, we also recognize the pocket effect, and the length effect induced current fluctuation indeed will become much serious as the dimension continuously shrinking.

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碩士論文題目：

金氧半電晶體中通道不均勻由 **RTN** 引發電流擾動效應

Channel Non-uniformity induced Current Fluctuation due to Random Telegraph Noise in sub-100nm MOSFETs