

I. INTRODUCTION

FOR the small-signal modeling of hetero junction bipolar transistor (HBT), either Tee or Pi circuit configurations can be used [1]–[4]. Though the Tee circuit reflects the device physics aspect of this transistor; the Pi circuit, however, is still preferred by some circuit designers and thus will be explored in this paper. As in Fig. 1, the HBT's Pi model consists of the intrinsic transistor, which is enclosed by the dotted box; the base spreading resistor R_{bb} ; the substrate network C_{sub1} , C_{sub2} and R_{sub} [5]; the external parasitic capacitor C_{ext} ; the base, emitter and collector resistors R_b , R_e , R_c ; the input and output pad capacitors C_{pad1} , C_{pad2} . Following the approach suggested by [6], two time constants τ_1 and τ_2 are added on to the trans-conductance G_m ; R_{ce} and C_{ce} are for the admittance of this voltage-induced current source [7], [8]. One challenge in HBT's small-signal Pi modeling comes from the presence of R_{bb} , whose location between C_{ext} and the intrinsic transistor makes possible the derivation of both C_{ext} and R_{bb} , so far, only by way of additional test structures or numerically [9]. In this paper, close-form expressions for these two parameters have been worked out, which, together with a revised circuit configuration, make more efficient and accurate the HBT's small-signal Pi modeling.

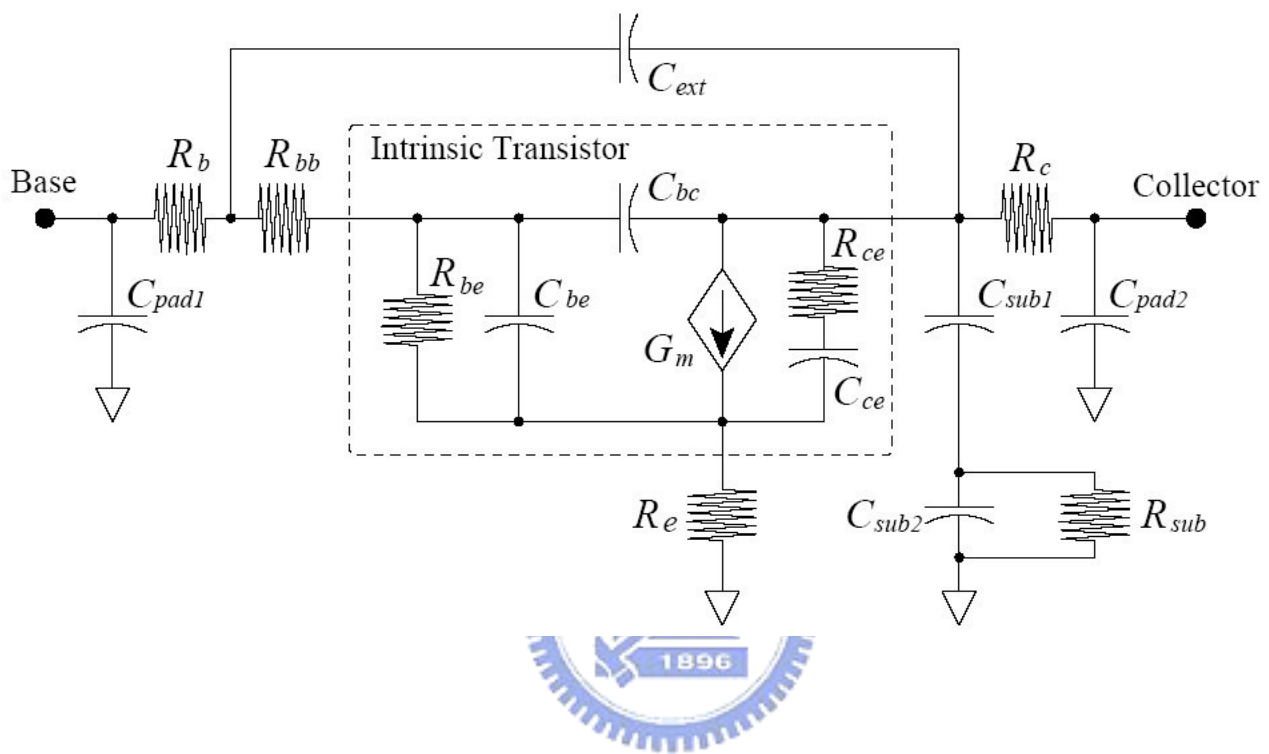


Fig. 1. HBT's small-signal Pi model where the substrate network consists of C_{sub1} , C_{sub2} and R_{sub} . Trans-conductance G_m is set to $G_{m0} e^{-j\omega \tau} / (1 + j\omega \tau)$; its associated shunt admittance is provided by R_{ce} and C_{ce} .

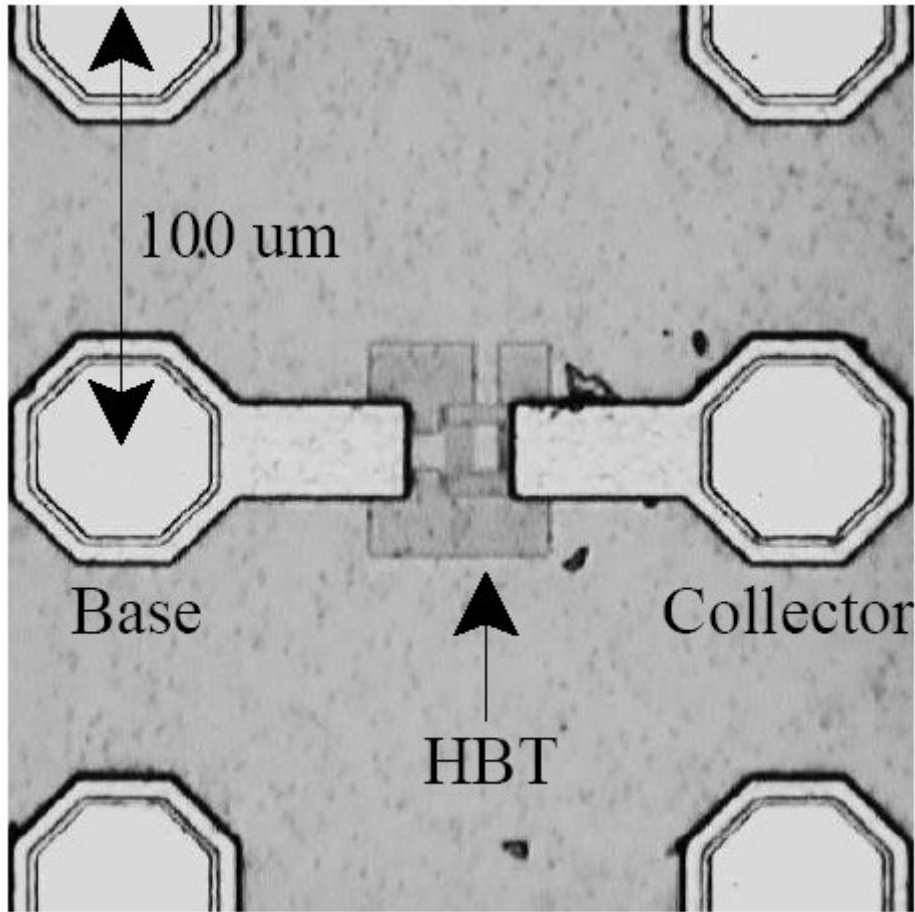


Fig. 2. The HBT under test.

II. HBT SMALL-SIGNAL PI MODELING

Fig. 2 shows the HBT under test, which is made of $0.35 \mu\text{m}$ SiGe-BiCMOS process with bulk resistivity of $8 \Omega\text{-cm}$ for the substrate. Two-port short, open, load and through (SOLT) calibration is performed using $100 \mu\text{m}$ Cascade probes on the ceramic test substrate. With the Agilent network analyzer's output power set to -10dBm , losses due to the additional cables and bias-T's will pull the power level down to -20dBm . DC bias for this transistor comes from HP4142B modular DC source/monitor.

To find out the parasitics of both the input and output pads, an open-pad test structure is designed where the transistor itself has been removed.

Frequency-independent capacitance can therefore be obtained as $C_{\text{pad1}} = 43\text{fF}$, $C_{\text{pad2}} = 46\text{fF}$. The measured cross-coupling capacitance between input and output is three orders less and can be neglected. Using appropriate de-embedding procedure, these capacitors can be removed from the transistor's Pi model.

Since R_b , R_e and R_c lie below the first-layer metal, they are beyond the reach of a short-circuit test structure and can be only determined by enforcing the transistor into saturation. With the current flowing out of the collector to be half of the gate current, we gradually increase the gate current and voltage, from 1mA and 18.8mV respectively, to 11mA and 95mV . By modeling this saturated intrinsic transistor as two conducting diodes, like that in Fig. 3, this transistor has a Tee-like circuit configuration, especially at low frequency. By extrapolating the measured resistance

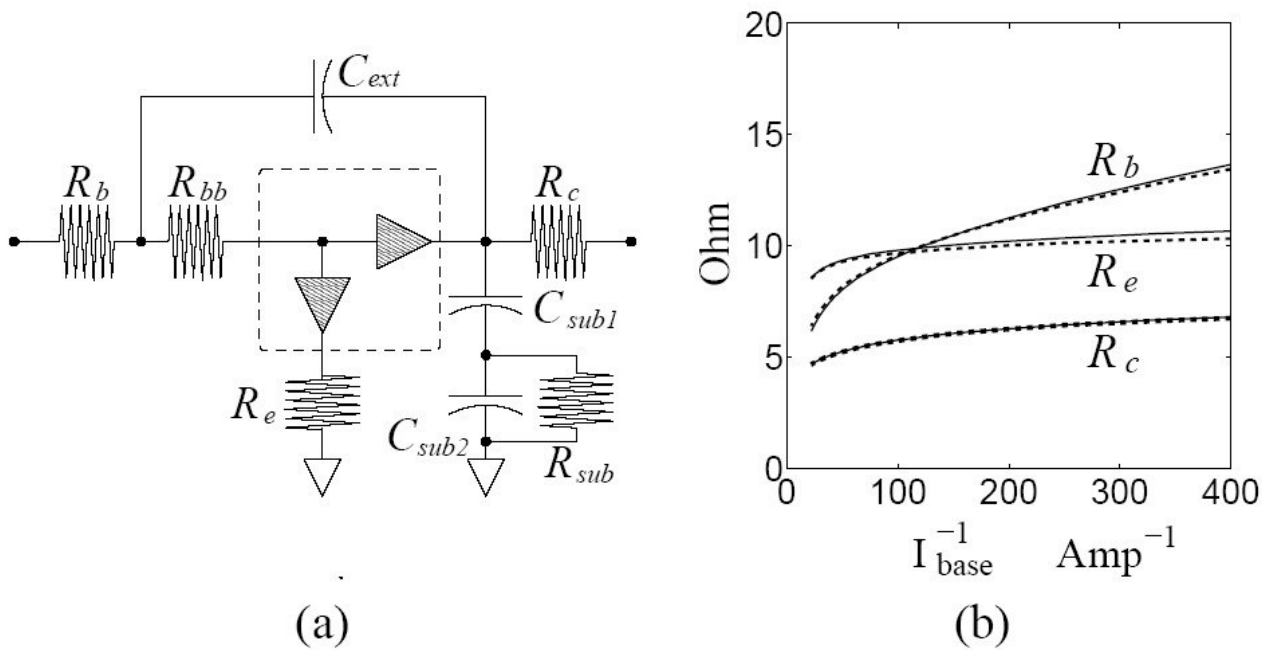
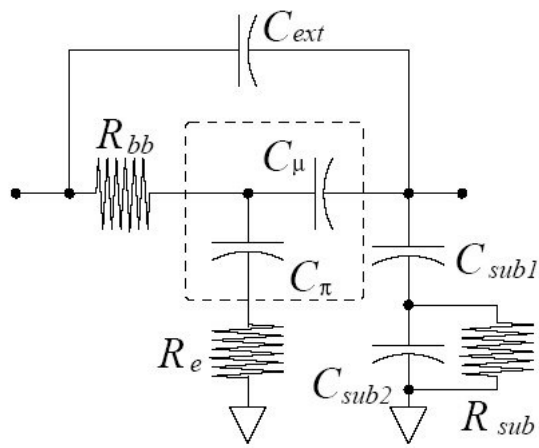


Fig. 3. Saturated HBT for the determination of R_e , R_b and R_c . (a) Schematic. (b) By extrapolating the measured resistance to those corresponding to infinite base current, we have $R_b = 7.5 \Omega$, $R_e = 4.1 \Omega$ and $R_c = 4.3 \Omega$. The solid curves correspond to 2GHz; the dashed ones are for 5GHz.

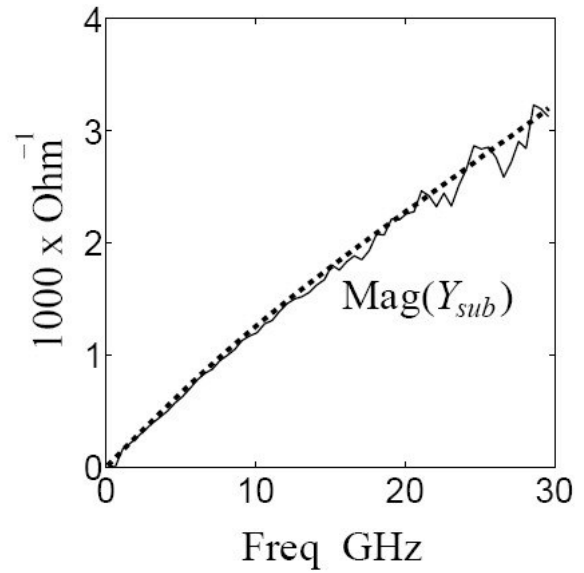
to that corresponding to infinite base current, we have R_b , R_e and R_c equal to 7.5Ω , 4.1Ω and 4.3Ω respectively. Now the impacts of both R_b and R_c on the transistor's Pi model are ready to be removed; R_e , however, will be temporarily retained for the purpose of determining the substrate network.

Though mathematically the substrate network can be decided with saturated transistor, the small in-parallel R_e , nonetheless, renders the derived values highly susceptible to measurement uncertainties. Reliable results can be obtained by reverse-biasing the transistor. With $V_c = 0\text{Volt}$, $I_c = -1.019 \cdot 10^{-2} \mu\text{A}$, $V_b = -1.05\text{Volt}$ and $I_b = -2.22 \cdot 10^{-2} \mu\text{A}$, the reverse-biased intrinsic transistor resembles two separate capacitors like that in Fig. 4. As both Y_{22} and Y_{12} are concerned, port#1 on the left of the schematic will be connected to the ground while the signal is injected into port#2 on the right. If R_{bb} is much smaller than the impedance of the series $C \pi R_e$ circuit, then most of the current passing through C^1 from port#2 will flow down the R_{bb} branch rather than the $C \pi R_e$ branch. By treating this $C \pi R_e$ branch as open-circuit, we have $Y_{sub} = Y_{22} + Y_{12}$ and the substrate network can now be determined as $C_{sub1} = 20.1\text{fF}$, $C_{sub2} = 62.6\text{fF}$ and $R_{sub} = 141 \Omega$. By contrast, if only series or parallel RC circuit is used to model the substrate network, the resulting parameters will be highly frequency-dependent.

With the impacts of substrate network and R_e readily removed, the reverse-biased circuit looks like that in Fig. 5. Analytical solutions for the constituting components can be obtained once Y_{11} and Y_{12} are known :



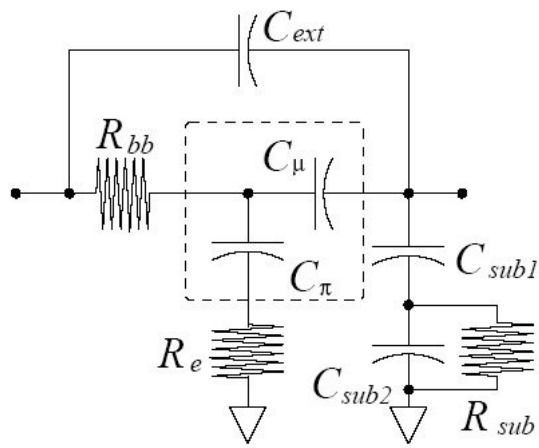
(a)



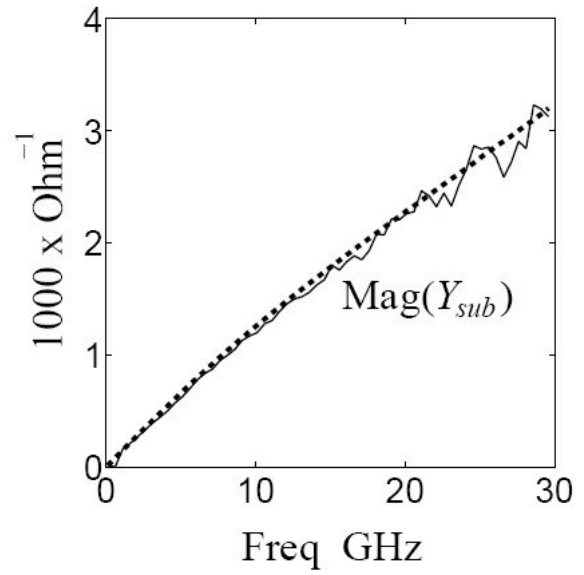
(b)



Fig. 4. Reverse-biased HBT for the determination of substrate network. (a) Schematic. (b) Measured and simulated substrate admittance Y_{sub} . The solid curve is the measured result; the dashed curve is the simulated one with $C_{sub1} = 20.1\text{fF}$, $C_{sub2} = 62.6\text{fF}$ and $R_{sub} = 141\ \Omega$.



(a)



(b)



Fig. 5. Reverse-biased HBT where the substrate network and R_e have been de-embedded for the purpose of determining C_{ext} . (a) Schematic. (b) Measured C_{ext} vs. frequency.

$$\begin{aligned}
Y_{11} &= j\omega C_{ext} + \left[R_{bb} + \frac{1}{j\omega(C_\pi + C_\mu)} \right]^{-1} \\
Y_{21} &= -j\omega C_{ext} - \frac{C_\mu}{C_\mu + C_\pi} \cdot \left[R_{bb} + \frac{1}{j\omega(C_\pi + C_\mu)} \right]^{-1} .
\end{aligned} \tag{1}$$

By defining H as

$$H = \frac{1}{Y_{11} + Y_{12}} = \left[R_{bb} + \frac{1}{j\omega(C_\pi + C_\mu)} \right] \frac{C_\mu + C_\pi}{C_\pi}, \tag{2}$$

we have the bias-dependent values of

$$\begin{aligned}
C_\pi &= \frac{-1}{\omega \cdot \text{Im}(H)}; \quad R_{bb} = \frac{1}{\text{Re}(Y_{11})} \left[\frac{\text{Re}(H)}{|H|} \right]^2 \\
C_\mu &= \left[1 - \frac{\text{Re}(Y_{11}) \cdot |H|^2}{\text{Re}(H)} \right] \frac{1}{\omega \cdot \text{Im}(H)},
\end{aligned} \tag{3}$$

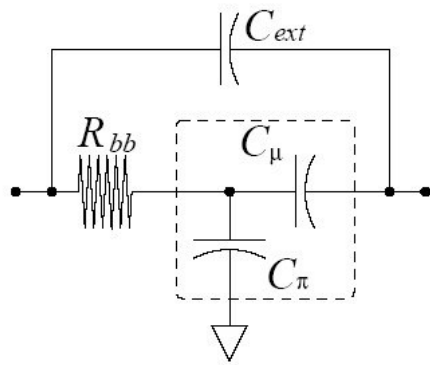
and the bias-independent value of

$$\begin{aligned}
C_{ext} &= \frac{1}{\omega} \left[\text{Im}(Y_{11}) - \text{Re}(Y_{11}) \cdot \frac{1}{\omega(C_\pi + C_\mu)R_{bb}} \right] \\
&= \frac{1}{\omega} \left[\text{Im}(Y_{11}) + \text{Re}(Y_{11}) \cdot \frac{\text{Im}(H)}{\text{Re}(H)} \right] .
\end{aligned} \tag{4}$$

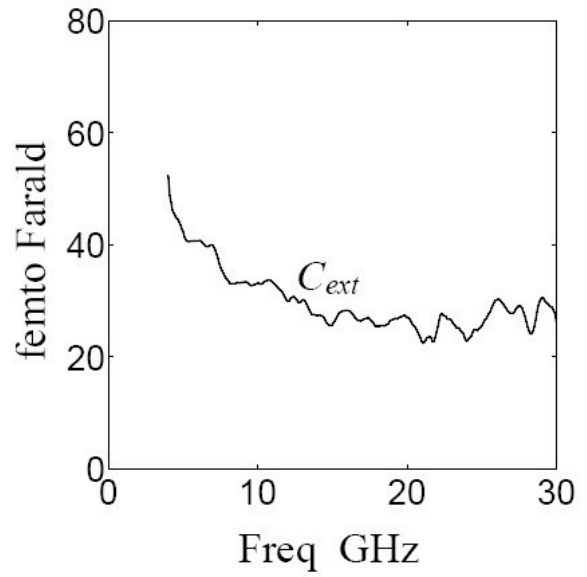
The measured results are $C_\pi = 59.4\text{fF}$, $R_{bb} = 14.5\Omega$, $C_\mu = 6.0\text{fF}$, and $C_{ext} = 25.5\text{fF}$.

The impact of C_{ext} on the transistor's Pi model can now be removed.

Finally, the transistor is set under normal bias condition with $V_c = 2\text{Volt}$, $I_c = 6.9\text{mA}$, $V_b = 0.95\text{Volt}$, and $I_b = 58.4 \mu\text{A}$. R_{bb} can be obtained once both Y_{11} and Y_{21} , as in the schematic of Fig. 6, are known :



(a)



(b)



Fig. 6. R_{bb} and the intrinsic transistor in normal bias. (a) Schematic where the trans-conductance $G_m = G_{m0} e^{-j\omega \tau_1} / (1 + j\omega \tau_2)$. (b) Measured R_{bb} vs. frequency.

$$\begin{aligned}
Y_{11} &= \left[R_{bb} + \frac{1}{j\omega(C_{be} + C_{bc}) + 1/R_{be}} \right]^{-1} \\
Y_{12} &= -j\omega C_{bc} \cdot \left[1 + \frac{R_{bb}}{R_{be}} + j\omega(C_{bc} + C_{be})R_{bb} \right]^{-1}, \quad (5)
\end{aligned}$$

i.e.

$$\frac{Y_{11}}{Y_{12}} = \left[j\omega(C_{be} + C_{bc}) + \frac{1}{R_{be}} \right] \cdot \frac{j}{\omega C_{bc}}. \quad (6)$$

Therefore,

$$\begin{aligned}
R_{bb} &= \operatorname{Re} \left(\frac{1}{Y_{11}} \right) + \frac{1}{\omega(C_{be} + C_{bc})R_{be}} \cdot \operatorname{Im} \left(\frac{1}{Y_{11}} \right) \\
&= \operatorname{Re} \left(\frac{1}{Y_{11}} \right) - \frac{\operatorname{Im}(Y_{11}/Y_{12})}{\operatorname{Re}(Y_{11}/Y_{12})} \cdot \operatorname{Im} \left(\frac{1}{Y_{11}} \right). \quad (7)
\end{aligned}$$

If the trans-conductance is a real number, it is also possible expressing Rbb in terms of Y11 and Y21, as suggested in [10]. Since the trans-conductance of the HBT under test exhibits a strong frequency dependency, it is our proposed expression that brings in consistent results. The numerical approach used in [11] tends to generate negative Rbb in this case.

Parameters of the intrinsic transistor can now be easily determined as $R_{bb} = 21.7 \Omega$, $C_{be} = 439\text{fF}$, $R_{be} = 587 \Omega$, $C_{bc} = 45\text{fF}$, $R_{ce} = 576 \Omega$, $C_{ce} = 17.6\text{fF}$, $R_{ce} = 724 \Omega$, $C_{ce} = 10\text{fF}$, $G_{m0} = 158\text{mS}$, $\tau_1 = 1.76\text{pSec}$ and $\tau_2 = 11.2\text{pSec}$. From Fig. 7, it is clear that both τ_1 and τ_2 are needed to explain the magnitude and phase variation of the transconductance. Accuracy of the HBT's small-signal Pi modeling can be verified by comparing the measured and simulated S-parameters, as in Fig. 8.

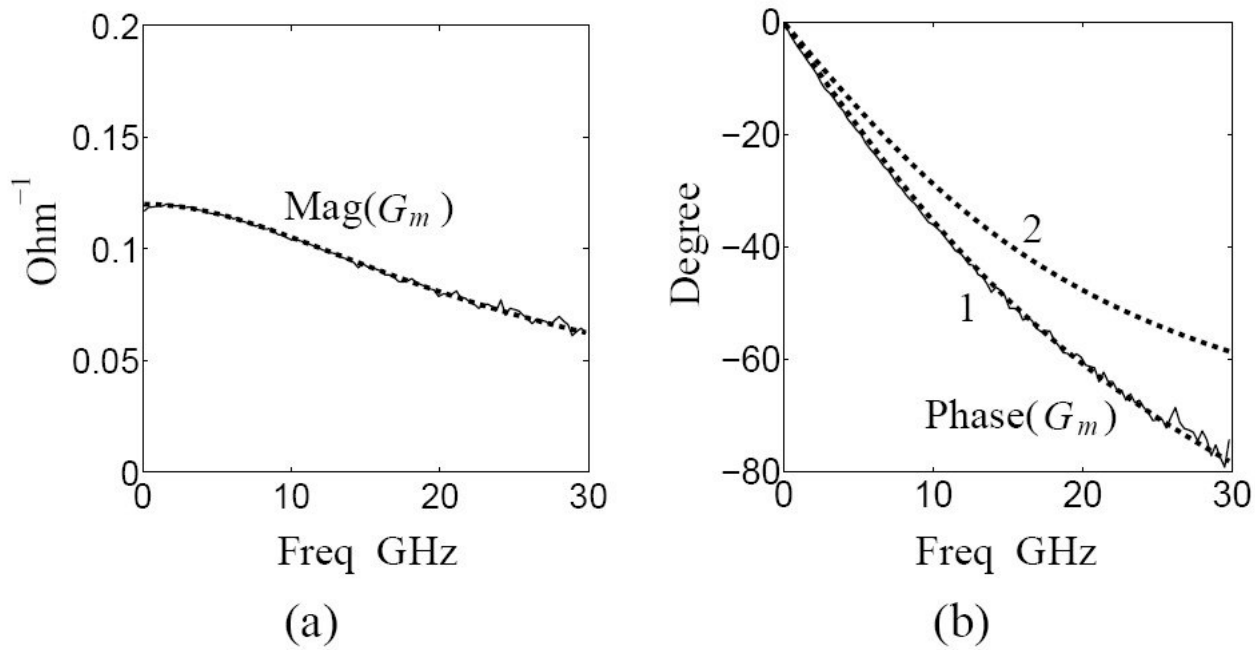
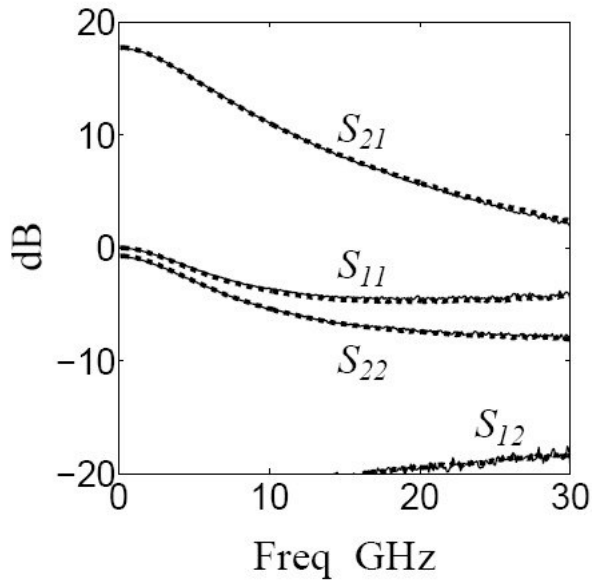
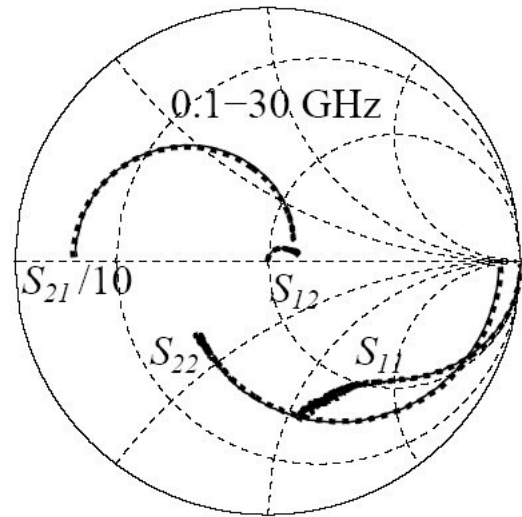


Fig. 7. Measured and simulated trans-conductance. (a) Magnitude of the trans-conductance where the solid curve is the measured result; the overlapping dashed curve is the simulated one with $G_{m0} = 158 \text{ mS}$, $\tau_1 = 1.76 \text{ pSec}$ and $\tau_2 = 11.2 \text{ pSec}$. (b) Phase of the trans-conductance where the solid curve is the measured result; the overlapping dashed curve 1 is the simulated one; dashed curve 2 is the simulated phase with $\tau_1 = 0 \text{ pSec}$.



(a)



(b)



Fig. 8. Measured and simulated S-parameters of the normal-biased HBT. (a) S-parameters in dB vs. frequency. The solid curves are the measured results; the overlapping dashed curves are the simulated ones. (b) The measured and simulated S-parameters on the Smith chart.

III. CONCLUSION

In this paper, analytical expressions for the external base collector capacitor C_{ext} and the base spreading resistor R_{bb} used in HBT's small-signal Pi model have been derived. Agreement between the measured and simulated results verifies the accuracy of the improved approach on HBT's small signal Pi modeling.



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個人簡歷

姓名：楊天仁

出生年月日：1982 年 2 月 3 日

籍貫：台灣省台南縣

址：台南縣歸仁鄉保興街 18 號

學歷：

國立台南第一高級中學

國立交通大學電子工程系

國立交通大學電子研究所



碩士論文題目：

異質接面電晶體小訊號建模之改進解析法

An Improved Analytical Approach On The Determination of HBT's Small-Signal Pi Modeling