

多重閘極絕緣矽金氧半場效電晶體的

微縮分析

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摘要

本論文探討鰭狀電晶體及三閘極電晶體結構的短通道效應特性，並且討論關於元件結構及條件設計上的考量。藉著解出搭配適當邊界條件的三維 Poisson 方程式，可求得在多重閘極電晶體中通道電位分佈的解析解。利用通道的電位分佈，可發展出鰭狀電晶體及三閘極電晶體的臨界電壓值模型。由我們的模型所得到的臨界電壓和電位分佈結果將會採用三維的元件模擬軟體來驗證。

在多重閘極電晶體中，元件的寬度微縮及高度微縮皆有助於改善短通道效應，而且寬度微縮會比高度微縮有更高的改善效率。在考量元件設計時，如果電晶體的導通電流是主要的需求，相對於三閘極電晶體，鰭狀電晶體將會是較佳的元件結構。此外，在相同的短通道特性下，三閘極電晶體的應用可以減緩最小線寬的微縮壓力，因此是最具有微縮潛力的結構。如果高介電常數的絕緣體被採用來抑制短通道效應的話，低摻雜濃度的三閘極電晶體將是可行的。一旦沒有高介電常數的絕緣體作為閘極絕緣層來幫助閘極對通道的控制能力，低摻雜濃度的三閘極電晶體在元件設計時將會面臨重大困難。

Investigation of Scaling for Multiple-Gate SOI MOSFETs Using Analytical Solution of 3-D Poisson's Equation

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Abstract

This thesis investigates the short channel characteristics and provides design considerations for FinFET and Tri-gate structures. An analytical solution of channel potential in multiple-gate devices is derived by solving 3-D Poisson's equation with adequate boundary conditions. By use of this channel potential solution, threshold voltage for FinFET and Tri-gate transistors can be obtained. The modeling results of threshold voltage roll-off and potential distribution are verified with the aid of 3-D device simulation.

Both fin width and fin height scaling improve short channel control, and fin width scaling benefits more than fin height scaling. FinFET will be a better design structure relative to Tri-gate when on-state current and short channel effect suppression are both considered. Besides, Tri-gate structure can be used to alleviate minimum feature size required for the same short channel characteristics. Lightly doped Tri-gate is feasible if high k dielectric is incorporated to suppress short channel effect. Without high k dielectric to enhance gate control, the device design for lightly doped Tri-gate will be difficult.

誌 謝

兩年碩士班生活已近尾聲，期間在研究上的成果，終能編織成這本碩士論文，雖然份量不甚多，但是在付印論文草稿的那一刻，心中依舊是相當感動。

在研究上，最要感謝的是我的指導教授蘇彬老師。老師對研究的熱忱，以及對新現象的那股好奇心和追根究柢的態度，使我印象深刻。同時十分嚮往老師的思維邏輯和研究領域上的旁徵博引，這也是將來要多加學習的。李維學長的勉勵也是碩士班生涯特別的經驗，學長並且也提供了許多寶貴建議，不管在研究上或生活上都十分受用。

同時和我拜入老師門下的天仁、Vita、小郭，大家一起準備學科考試和每週meeting的過程，現在想來還是歷歷在目。尤其是小郭這位戰友，在最後這段趕畢業的緊湊日子裡，常常一起共同奮鬥及互相討論。謝謝秉真，一直鼓勵我樂觀進取。還有其他同在 308 實驗室的同學及學弟妹，有幸能夠同在一個屋簷下。

我的研究中常需要用到元件模擬軟體來驗證，這一部分要感謝國家高速電腦中心提供軟體及 license，讓我的研究得以順利進行。

最後要謝謝我的家人對我的支持與體諒，雖然很少時間能夠陪伴你們。不論將來我的足跡能夠到達多遠，你們的關心永遠是我動力的來源。

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Fig. 2-3 Potential model verified with device simulation along the fin height direction

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Fig. 2-4 Potential model verified with device simulation along the fin width direction

(a) the positions of fin height center and gate insulator/body interface in heavily doped body, (b) the position of fin height center in heavily doped body.

Fig. 2-5 Potential model verified with device simulation along the channel length

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Fig. 4-4 Subthreshold swing of lightly doped multiple-gate devices versus total width in three different geometry devices.

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