

多重閘極絕緣矽金氧半場效電晶體的

微縮分析

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摘要

本論文探討鰭狀電晶體及三閘極電晶體結構的短通道效應特性，並且討論關於元件結構及條件設計上的考量。藉著解出搭配適當邊界條件的三維 Poisson 方程式，可求得在多重閘極電晶體中通道電位分佈的解析解。利用通道的電位分佈，可發展出鰭狀電晶體及三閘極電晶體的臨界電壓值模型。由我們的模型所得的臨界電壓和電位分佈結果將會採用三維的元件模擬軟體來驗證。

在多重閘極電晶體中，元件的寬度微縮及高度微縮皆有助於改善短通道效應，而且寬度微縮會比高度微縮有更高的改善效率。在考量元件設計時，如果電晶體的導通電流是主要的需求，相對於三閘極電晶體，鰭狀電晶體將會是較佳的元件結構。此外，在相同的短通道特性下，三閘極電晶體的應用可以減緩最小線寬的微縮壓力，因此是最具有微縮潛力的結構。如果高介電常數的絕緣體被採用來抑制短通道效應的話，低摻雜濃度的三閘極電晶體將是可行的。一旦沒有高介電常數的絕緣體作為閘極絕緣層來幫助閘極對通道的控制能力，低摻雜濃度的三閘極電晶體在元件設計時將會面臨重大困難。

Investigation of Scaling for Multiple-Gate SOI MOSFETs

Using Analytical Solution of 3-D Poisson's Equation

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Abstract

This thesis investigates the short channel characteristics and provides design considerations for FinFET and Tri-gate structures. An analytical solution of channel potential in multiple-gate devices is derived by solving 3-D Poisson's equation with adequate boundary conditions. By use of this channel potential solution, threshold voltage for FinFET and Tri-gate transistors can be obtained. The modeling results of threshold voltage roll-off and potential distribution are verified with the aid of 3-D device simulation.

Both fin width and fin height scaling improve short channel control, and fin width scaling benefits more than fin height scaling. FinFET will be a better design structure relative to Tri-gate when on-state current and short channel effect suppression are both considered. Besides, Tri-gate structure can be used to alleviate minimum feature size required for the same short channel characteristics. Lightly doped Tri-gate is feasible if high k dielectric is incorporated to suppress short channel effect. Without high k dielectric to enhance gate control, the device design for lightly doped Tri-gate will be difficult.

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Figure Captions

Fig. 2-1 The scheme of multiple-gate transistor structure.

Fig. 2-2 Verification of homogeneous dielectric approximation by 1-D exact solution

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Fig. 2-3 Potential model verified with device simulation along the fin height direction

(a) the positions of fin width center and gate insulator/body interface in heavily doped body, (b) the position of fin width center in heavily doped body.

Fig. 2-4 Potential model verified with device simulation along the fin width direction

(a) the positions of fin height center and gate insulator/body interface in heavily doped body, (b) the position of fin height center in heavily doped body.

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Fig. 3-2 Tri-gate threshold voltage roll-off derived by $2\phi_B$ method verified with device simulation (a) fin width = 20nm, and (b) fin width = 30nm.

Fig. 3-3 Tri-gate threshold voltage roll-off with fin width = 30nm derived by

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Fig. 3-7 Threshold voltage roll-off comparison between heavily doped and lightly doped bodies with oxide to be gate insulator and low drain bias.

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Fig. 4-4 Subthreshold swing of lightly doped multiple-gate devices versus total width in three different geometry devices.

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