Chapter 1
Introduction

The difficulties in shrinking the size of the conventional planar fully-depleted (FD) SOI transistors have motivated the development of new non-planar device architectures [1-3]. The main advantages of multiple-gate devices are the high current drive in the active region, and reduced short channel effect due to better gate control in the subthreshold region. Two different design geometries including FinFET and Tri-gate transistor are considered as promising candidates in multiple-gate devices. It is noticeable that in literature, the definition for FinFET is not unified. For example, in [2] and [3], FinFET denotes double gate structure. However, in [4] FinFET refers to high aspect ratio (A/R) devices. In this thesis, both definitions are used and will be mentioned in the text.

O. Faynot *et al.* [4] have demonstrated comparison results in 45nm technology node with gate length 20 to 30nm and heavily doped fin body. By simulation, they proposed that Tri-gate is a more scalable structure than FinFET. But their conclusion derived by device simulation may not be applicable when gate length is further scaled, and lightly doped case is not included either. In ITRS 2005 [5], lightly doped body is suggested to avoid threshold voltage variation and mobility degradation in multiple-gate transistors. J. W. Yang and J. G. Fossum [6] indicated that Tri-gate transistors are not feasible when undoped body is adopted. But their conclusions were based on the use of gate oxide. According to lately fabrication results in [7], Tri-gate is feasible by using lightly doped body coupled with high k dielectric HfO_2, which is not discussed in [6]. The impact of high k dielectric is necessary to investigate.

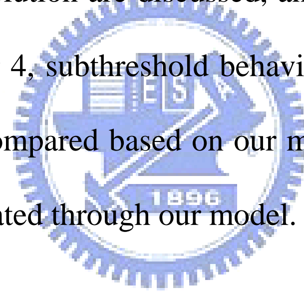
We want to derive a model to investigate the scaling in multiple-gate MOSFETs.

Short channel effect (SCE) is a significant issue in the device scaling. Therefore, emphasis has been put on the subthreshold behaviors of multiple-gate devices, like subthreshold swing, and threshold voltage roll-off. Thus, to determine the scalability of FinFET and Tri-gate structures, the comparison of subthreshold behaviors in these two architectures is necessary to be investigated.

The subthreshold characteristics are deeply influenced by the entire Si-body potential distribution. Thus, an analytical body potential model will be the first step for scaling issue investigation. An analytical model will provide us a more physical insight in device design, and the equation form will be a good reference for the development of compact model. Two-dimensional analytical model for undoped double-gate device was derived by X. Liang *et al.* [8]. But it is not applicable when Tri-gate structures push the device design consideration into the third dimension. G. Pei *et al.* [9] have obtained a three-dimensional design model for multiple-gate device structure. However, it is confined to a lightly-doped Si-fin case because Laplace's equation was used instead of Poisson's equation. In lightly-doped case, poly gate must be replaced by metal gate to achieve a moderate threshold voltage. Except metal gate engineering, another alternative to maintain a proper threshold voltage value is the use of heavily doped body, which is not discussed in [9]. Threshold voltage roll-off is one of the significant syndromes due to short channel effect, and hence threshold voltage modeling is a key step to estimate the degree of short channel effect. For this purpose, the subthreshold current model derived by D. S. Havaldar *et al.* [10] and their former study [11] considered doped-body channel with three-dimensional structure. Though accurate boundary conditions were calculated, the analytical potential solution showed tremendous complexity and difficult to duplicate, and their discussion was lack of Tri-gate transistor and heavily doped case information.

Based on the reasons above, we want to derive a general 3-D analytical potential solution for multiple-gate SOI structure, and to take the high k dielectric and body doping concentration into consideration. With a simplified analytical solution, the model will be more practical and feasible, and provide some basic insights to the short channel effect and related device parameters.

This thesis solves the boundary value problem of 3-D Poisson's equation to obtain an analytical expression for Si-fin body potential of fully-depleted multiple-gate SOI MOSFETs. In chapter 2, the boundary conditions are described and the solving method is discussed in detail, and the analytical 3-D potential solution is verified by 3-D device simulation. In chapter 3, threshold voltage determination methods via body potential solution are discussed, and the results are compared with simulation as well. In chapter 4, subthreshold behavior of various device parameters in FinFET and Tri-gate are compared based on our model, and design considerations in both structures are investigated through our model.



Chapter 2
Three-Dimensional Potential Solution and Verification

2.1 Poisson's Equation and Boundary Conditions

Since we are interested in the short channel effect of devices, threshold voltage roll-off is our primary concern, and hence we consider only the subthreshold region, in which the Si-fin body is fully-depleted with mobile carriers being negligible. In such a case, suppose that doping is ideally uniform, the charge distribution in the body region is uniform, and equal to the doping level in the body. The body potential $\phi(x,y,z)$, as a function of position, follows 3-D Poisson's equation

$$\frac{\partial^2\phi(x,y,z)}{\partial x^2}+\frac{\partial^2\phi(x,y,z)}{\partial y^2}+\frac{\partial^2\phi(x,y,z)}{\partial z^2}=-\frac{qN_d}{\varepsilon_{si}} \quad (2\text{-}1)$$

where the body charge term N_d, which is stemmed from the fixed charges after depletion, is negative for p-type body and positive for n-type body.

The Si-fin body covered by gate insulator is a cuboid with six faces, and the full scheme is illustrated in fig. 2-1. Each face is connected to a voltage bias: top gate, front gate, back gate, gate below buried oxide, source and drain, so six boundary conditions are considered. Thus, the boundary conditions are described in the Cartesian coordinate. The *x*-axis, *y*-axis, and *z*-axis are defined to be fin width, channel length, and fin height directions, respectively.

The required boundary conditions in this problem are given as

$$\phi(W_{fin},y,z)+t_{i,f}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial x}\right|_{x=W_{fin}}=V_{fg}-V_{fb} \quad (2\text{-}2)$$

$$\phi(0,y,z)-t_{i,b}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial x}\right|_{x=0}=V_{bg}-V_{fb} \tag{2-3}$$

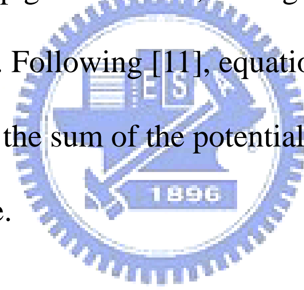
$$\phi(x,y,H_{fin})+t_{i,t}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial z}\right|_{z=H_{fin}}=V_{tg}-V_{fb} \tag{2-4}$$

$$\phi(x,y,0)-t_{ox,u}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial\phi(x,y,z)}{\partial z}\right|_{z=0}=V_{ug}-V_{fb} \tag{2-5}$$

$$\phi(x,0,z)=-\phi_{ms} \tag{2-6}$$

$$\phi(x,L,z)=-\phi_{ms}+V_d \tag{2-7}$$

where ε_{si} and ε_i are dielectric constants of Si and gate insulator, respectively. W_{fin}, H_{fin}, and L are defined as fin width, fin height, and channel length, respectively. And $t_{i,t}$, $t_{i,f}$, $t_{i,b}$, and $t_{ox,u}$ are thickness of top gate insulator, front gate insulator, back gate insulator, and buried oxide, respectively. Following [11], equation (2-2) to (2-5) indicate that the potential applied at the gate is the sum of the potential at the Si/oxide interface and the potential drop across the oxide.



2.2 Solving Method for Boundary Value Problem

Using the superposition principle, we can divide the 3-D boundary value problem into three sub-problems, including 1-D Poisson's equation, 2-D and 3-D Laplace's equation. 1-D Poisson's equation and its boundary conditions are

$$\frac{\partial^2 w(x)}{\partial x^2}=-\frac{qN_d}{\varepsilon_{si}} \tag{2-8a}$$

$$w(W_{fin})+t_{i,f}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial w(x)}{\partial x}\right|_{x=W_{fin}}=V_{fg}-V_{fb} \tag{2-8b}$$

$$w(0)-t_{i,b}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial w(x)}{\partial x}\right|_{x=0}=V_{bg}-V_{fb} \quad \text{(2-8c)}$$

where $w(x)$ is the 1-D solution and can be easily obtained:

$$w(x)=-\frac{qN_d}{2\varepsilon_{si}}x^2+Ax+B \quad \text{(2-9a)}$$

$$A=\frac{\left(V_{fg}-V_{fb}\right)-\left(V_{bg}-V_{fb}\right)+\frac{qN_d}{2\varepsilon_{si}}\left(W_{fin}{}^2+2\cdot\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,f}W_{fin}\right)}{W_{fin}+\frac{\varepsilon_{si}}{\varepsilon_i}\left(t_{i,f}+t_{i,b}\right)} \quad \text{(2-9b)}$$

$$B=\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}A+\left(V_{bg}-V_{fb}\right) \quad \text{(2-9c)}$$

To simplify the final solution form to be more manageable compared with [11], approximations have to be made in dealing with 2-D and 3-D Laplace's equation boundary value problems [12]. To eliminate the electric field difference across Si and insulator interface, which is the ratio $\varepsilon_{si}/\varepsilon_i$, replace the insulator with an equivalent silicon region and use ε_{si} as its dielectric constant by converting insulator thickness to $(\varepsilon_{si}/\varepsilon_i)$ times. This approximation moves the boundary from Si and gate insulator interface toward outside of gate insulator. Therefore, the Si-fin body and the gate insulator around it are treated as a homogeneous silicon cuboid with effective width W_{eff}, effective height H_{eff}, given in equations (2-10) and (2-11), respectively, and channel length L.

$$W_{eff}=W_{fin}+\frac{\varepsilon_{si}}{\varepsilon_i}\left(t_{i,f}+t_{i,b}\right) \quad \text{(2-10)}$$

$$H_{eff}=H_{fin}+\frac{\varepsilon_{si}}{\varepsilon_i}\left(t_{i,t}+t_{i,u}\right) \quad \text{(2-11)}$$

To understand the error between exact solution and the approximation we made (we call it "homogeneous dielectric approximation"), a simple examination can be made here. We take the 1-D exact solution in equation (2-8a) to (2-8c) to compare with another 1-D solution with homogeneous dielectric approximation. Fig. 2-2(a) shows 1-D solution comparison at the doping level 6×10^{18} cm^{-3}. Clearly we can see that as oxide thickness increases, bigger error occurs in homogeneous dielectric approximation. With $t_i = t_{ox}$=3nm, various doping concentrations are plotted in fig. 2-2(b). The results show that as doping level gets lower, homogeneous dielectric approximation is more close to the exact solution. Therefore, the error of homogeneous dielectric approximation depends on insulator thickness and doping concentration. Thicker oxide and higher doping cause the approximation away from exact solution, and the main reason for this is due to the incorrect charge term in the oxide when approximation is plugged in.

The exact boundary conditions for 2-D Laplace's equation before approximation are

$$\begin{aligned}
&\frac{\partial^2 v(x,z)}{\partial x^2}+\frac{\partial^2 v(x,z)}{\partial y^2}=0\\
&v(W_{fin},z)+t_{i,f}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial v(x,z)}{\partial x}\right|_{x=W_{fin}}=0\\
&v(0,z)-t_{i,b}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial v(x,z)}{\partial x}\right|_{x=0}=0\\
&v(x,H)+t_{i,t}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial v(x,z)}{\partial z}\right|_{z=H_{fin}}=V_{tg}-V_{fb}-w(x)\\
&v(x,0)-t_{i,u}\frac{\varepsilon_{si}}{\varepsilon_i}\cdot\left.\frac{\partial v(x,z)}{\partial z}\right|_{z=0}=V_{ug}-V_{fb}-w(x)
\end{aligned} \qquad (2\text{-}12)$$

where $v(x,z)$ is the 2-D solution. After the approximation is made,

$$v(W_{eff}, z) = 0 \tag{2-13a}$$

$$v(0, z) = 0 \tag{2-13b}$$

$$v(x, H_{eff}) = V_{tg} - V_{fb} - w(x) \tag{2-13c}$$

$$v(x,0) = V_{ug} - V_{fb} - w(x) \tag{2-13d}$$

and $v(x, z)$ can be obtained by separation of variables

$$v(x,z) = \sum_{n=1}^{\infty}\left[c_n \sinh\left(\frac{n\pi}{W_{eff}} z\right) + c_n' \sinh\left(\frac{n\pi}{W_{eff}}(W_{eff} - z)\right)\right] \cdot \sin\left(\frac{n\pi}{W_{eff}} x\right) \tag{2-14a}$$

$$c_n = \frac{1}{\sinh\left(n\pi \frac{H_{eff}}{W_{eff}}\right)}\left[2(V_{tg} - V_{fb} - B)\frac{1-(-1)^n}{n\pi} + 2A\left(\frac{\frac{\varepsilon_{si}}{\varepsilon_i} t_{i,b}}{n\pi} + \frac{\left(W_{eff} - \frac{\varepsilon_{si}}{\varepsilon_i} t_{i,b}\right)(-1)^n}{n\pi}\right)\right.$$
$$\left. + \frac{qN_d}{\varepsilon_{si}}\left(\frac{\left(\frac{\varepsilon_{si}}{\varepsilon_i} t_{i,b}\right)^2}{n\pi} - \frac{\left(W_{eff} - \frac{\varepsilon_{si}}{\varepsilon_i} t_{i,b}\right)^2 (-1)^n}{n\pi} + 2W_{eff}^{\ 2}\frac{(-1)^n - 1}{(n\pi)^3}\right)\right] \tag{2-14b}$$

$$c_n' = \frac{1}{\sinh\left(n\pi \frac{H_{eff}}{W_{eff}}\right)}\left[2(V_{ug} - V_{fb} - B)\frac{1-(-1)^n}{n\pi} + 2A\left(\frac{\frac{\varepsilon_{si}}{\varepsilon_i} t_{i,b}}{n\pi} + \frac{\left(W_{eff} - \frac{\varepsilon_{si}}{\varepsilon_i} t_{i,b}\right)(-1)^n}{n\pi}\right)\right.$$
$$\left. + \frac{qN_d}{\varepsilon_{si}}\left(\frac{\left(\frac{\varepsilon_{si}}{\varepsilon_i} t_{i,b}\right)^2}{n\pi} - \frac{\left(W_{eff} - \frac{\varepsilon_{si}}{\varepsilon_i} t_{i,b}\right)^2 (-1)^n}{n\pi} + 2W_{eff}^{\ 2}\frac{(-1)^n - 1}{(n\pi)^3}\right)\right] \tag{2-14c}$$

Similarly, after simplification of the 3-D Laplace's boundary value sub-problem

$$\frac{\partial^2 u(x,y,z)}{\partial x^2} + \frac{\partial^2 u(x,y,z)}{\partial y^2} + \frac{\partial^2 u(x,y,z)}{\partial z^2} = 0 \tag{2-15a}$$

$$u(W_{eff}, y, z) = 0 \tag{2-15b}$$

$$u(0, y, z) = 0 \tag{2-15c}$$

$$u(x, y, H_{eff}) = 0 \tag{2-15d}$$

$$u(x,y,0)=0 \tag{2-15e}$$

$$u(x,0,z)=-\phi_{ms}-w(x)-v(x,z) \tag{2-15f}$$

$$u(x,L,z)=-\phi_{ms}+V_d-w(x)-v(x,z) \tag{2-15g}$$

where $u(x,y,z)$ is the 3-D solution, and it can also be obtained by separation of variables

$$u(x,y,z)=\sum_{m_1=1}^{\infty}\sum_{m_2=1}^{\infty}\left[e_{m_1,m_2}\sinh(k_y y)+e'_{m_1,m_2}\sinh(k_y(L-y))\right]\sin\left(\frac{m_1\pi}{W_{eff}}x\right)\sin\left(\frac{m_2\pi}{H_{eff}}z\right) \tag{2-16a}$$

$$e_{m_1,m_2}=\frac{1}{\sin(k_yL)}\left\{\left[\left(-\phi_{ms}+V_{ds}-B\right)\frac{1-(-1)^{m_1}}{m_1\pi}+\frac{qN_d}{2\varepsilon_{si}}\left(-\frac{\left(W_{eff}-\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)^2(-1)^{m_1}-\left(\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)^2}{m_1\pi}\right.\right.\right.$$

$$\left.\left.+\frac{2W_{eff}^{\ 2}\left((-1)^{m_1}-1\right)}{(m_1\pi)^3}\right)+A\left(\frac{\left(W_{eff}-\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)(-1)^{m_1}+\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}}{m_1\pi}\right)\right]\cdot\frac{2\cdot\left(1-(-1)^{m_2}\right)}{m_2\pi}$$

$$\left.+c_{m_1}\frac{\frac{(-1)^{m_2}}{m_2\pi}\sinh\left(m_1\pi\frac{H_{eff}}{W_{eff}}\right)}{1+\left(\frac{m_1}{m_2}\frac{H_{eff}}{W_{eff}}\right)^2}-c'_{m_1}\frac{\frac{1}{m_2\pi}\sinh\left(m_1\pi\frac{H_{eff}}{W_{eff}}\right)}{1+\left(\frac{m_1}{m_2}\frac{H_{eff}}{W_{eff}}\right)^2}\right\} \tag{2-16b}$$

$$e'_{m_1,m_2}=\frac{1}{\sin(k_yL)}\left\{\left[\left(-\phi_{ms}-B\right)\frac{1-(-1)^{m_1}}{m_1\pi}+\frac{qN_d}{2\varepsilon_{si}}\left(-\frac{\left(W_{eff}-\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)^2(-1)^{m_1}-\left(\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)^2}{m_1\pi}\right.\right.\right.$$

$$+\frac{2W_{eff}{}^{2}\left(\left(-1\right)^{m_1}-1\right)}{\left(m_1\pi\right)^{3}}\Bigg)+A\left(\frac{\left(W_{eff}-\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}\right)\left(-1\right)^{m_1}+\frac{\varepsilon_{si}}{\varepsilon_i}t_{i,b}}{m_1\pi}\right)\Bigg]\cdot\frac{2\cdot\left(1-\left(-1\right)^{m_2}\right)}{m_2\pi}$$

$$+c_{m_1}\frac{\frac{\left(-1\right)^{m_2}}{m_2\pi}\sinh\left(m_1\pi\frac{H_{eff}}{W_{eff}}\right)}{1+\left(\frac{m_1}{m_2}\frac{H_{eff}}{W_{eff}}\right)^{2}}-c_{m_1}^{'}\frac{\frac{1}{m_2\pi}\sinh\left(m_1\pi\frac{H_{eff}}{W_{eff}}\right)}{1+\left(\frac{m_1}{m_2}\frac{H_{eff}}{W_{eff}}\right)^{2}}\Bigg\} \quad (2\text{-}16c)$$

and the final solution is the superposition of 1-D, 2-D, and 3-D sub-problem solutions

$$\phi(x,y,z)=w(x)+v(x,z)+u(x,y,z) \quad (2\text{-}17)$$

We have derived the analytical solution of potential in the Si-fin body region. The functional form is a sinusoidal series summation because of the solving techniques we use. Generally, fifteen terms in 2-D and 3-D solutions are sufficient to describe the potential distribution. Parameters like channel length (L), fin height (H_{fin}), fin width (W_{fin}), control gate insulator thickness ($t_{i,t}$, $t_{i,f}$, $t_{i,b}$), buried oxide thickness ($t_{ox,u}$), body doping (N_d), control gate bias (V_{tg}, V_{fg}, V_{bg},), and source/drain bias (V_d, V_s) are included in the solution.

2.3 Verification of Potential Solution

The analytical potential model has to be verified through device simulation. We use the TCAD *ISE v10.0* [13] 3D simulator to verify our model. The device structure is illustrated in fig. 2-1, and the device parameters in our boundary conditions are shown. In our comparisons, in heavily doped body the gate insulator is oxide, and its thickness is 1nm, while in lightly doped body, the gate insulator is high k dielectric HfO_2, as in [7]. The buried oxide thickness is 30nm, which are close to 45nm node

technology predicted in ITRS 2005. Channel length L is mainly focused on 20nm, and the minimum size of fin width and fin height is 20nm as well. Since our model is applicable in both heavily doped and lightly doped fin body, doping level of 6×10^{18} and 1×10^{17} cm^{-3} are discussed. In heavily doped case, the gate electrode is equivalent to a very n^{+} poly gate material. However, gate workfunction is selected to obtain reasonable threshold voltage value in lightly doped body, and is equal to 4.7eV in our discussion. Gate bias is selected to achieve fully depletion, which is around -0.2V in both heavily and lightly doped bodies. Drain bias is fixed at 0.05V in our potential comparison to keep the device operating in the linear region.

In the following comparisons, we will focus on n-MOSFET, and the dominant carrier in n-MOSFET is electron. Positions with higher potential will enhance the conduction of electrons. Fig. 2-3(a) shows the potential distribution along height direction in heavily doped case. In fig. 2-3(a), the potential near the body/BOX interface (at $z=0$) show a noticeable discrepancy at both $x=W_{fin}$ (side surface) and $x=0.5W_{fin}$ (width center). In our model, the potential distribution is always highest at $z=H_{fin}$ (top surface), and decreases gradually along height direction, and the lowest potential is at $z=0$ (body/BOX interface). But in simulation, a potential rise is found at $z=0$, and hence the lowest potential position moves from body/BOX interface into the body. The error may be attributed to the lateral field in the BOX region, which is not considered in our boundary conditions. Fig. 2-3(b) shows the potential distribution along height direction in lightly doped case. Only the potential at width center is plotted because the potential distribution in the body is more significant than surface in lightly doped case. Besides, the highest potential is not at body surface but near the body/BOX interface in lightly doped body.

Fig. 2-4(a) and (b) illustrate the potential distribution along width direction in

heavily and lightly doped body, respectively. Highest potential is observed at the two side surfaces $x=0$ and $x=W_{fin}$ in heavily doped case, while the highest potential occurs at the width center $x=0.5W_{fin}$ in lightly doped case. Therefore, different current conduction paths are expected in heavily and lightly doped case. In heavily doped body, current flows at gate insulator/body interface. But in lightly doped body, initially the current flows in the Si-body instead of the interface. Though high k dielectric increases the potential coupling from gates, the current paths are still away from gate insulator/body interface due to severe short channel effect.

Fig. 2-5(a) and (b) show the potential distribution along channel length direction in heavily and lightly doped body, respectively. Both figures are similar in shape, and the lowest potential occurs near $L/2$ because the source and drain sides is almost symmetric at small V_{DS}. The lowest potential along the channel length direction will constitute a barrier for electron conduction, which will be discussed in next chapter.

We have verified the accuracy of our model by 3-D device simulation. Though some discrepancies compared with simulation results still exists, the error is not significant. We notice that the error is minor in high k dielectric cases. This is because the approximation we made (homogeneous dielectric approximation) is smaller when vertical field is much larger than lateral field. If the gate insulator is high k, effective oxide thickness (EOT) will be scaled down. Vertical field will be enhanced while the electric field from source/drain sides remains unchanged. Therefore, our potential model is applicable and even more accurate when high k material is selected as gate insulator.

Homogeneous dielectric approximation is made in the process of solving the 2-D and 3-D boundary value problem. Besides, some fringing field is not considered in our boundary conditions. Those are the error sources in our analytical potential model,

and the error may impact the determination of threshold voltage or subthreshold swing value. Therefore, some efforts may still be required to further improve the accuracy of our potential model.

Since we have derived an analytical body potential model, some benchmark in multiple-gate MOSFETs can be testified. Fig. 2-6 shows variations of top channel surface potential distribution with different fin width. The two sides at normalized width denote corner regions in Tri-gate transistors. As shown in fig. 2-6, devices with 30nm fin width have lower potential at width center than those with 10nm fin width, while the potential at corner region are very close in the two cases. Therefore, Tri-gate transistors with wider fins induce more potential difference between corner region and width center position, and this implies that the electron density in corner region is much higher than width center, as demonstrate in [14]. Besides, fig. 2-6 also illustrates two different body doping levels. With higher doping level, Tri-gate transistor exhibits higher difference in electron density between corner region and non-corner channel region, which is consistent with [15].

2.4 Summary

The boundary conditions for Si-body potential in multiple-gate transistor are demonstrated. The boundary value problem can be divided into three sub-problems. 1-D problem possesses exact solution, while approximations are made in dealing 2-D and 3-D sub-problems. Separation of variables method is used in solving the 2-D and 3-D sub-problems, and the equation form of potential solution is summation of sinusoidal series due to the Fourier expansion used. After potential solution of Si-body is derived, the verification was through the 3-D simulation tool *ISE v10.0*.

Our potential model is proposed to deal with multiple-gate SOI devices initially. However, in the future the multiple-gate devices on bulk may be another candidate in CMOS scaling. The main difference between SOI and bulk devices is the boundary condition at the bottom of body. The boundary conditions in our model are flexible, and some modifications are needed if we intend to manage the bulk devices. Besides, strain technology is becoming a mainstream in nanoscale technology. The impact of strain on our model is not thoroughly investigated yet, and will be an important study.

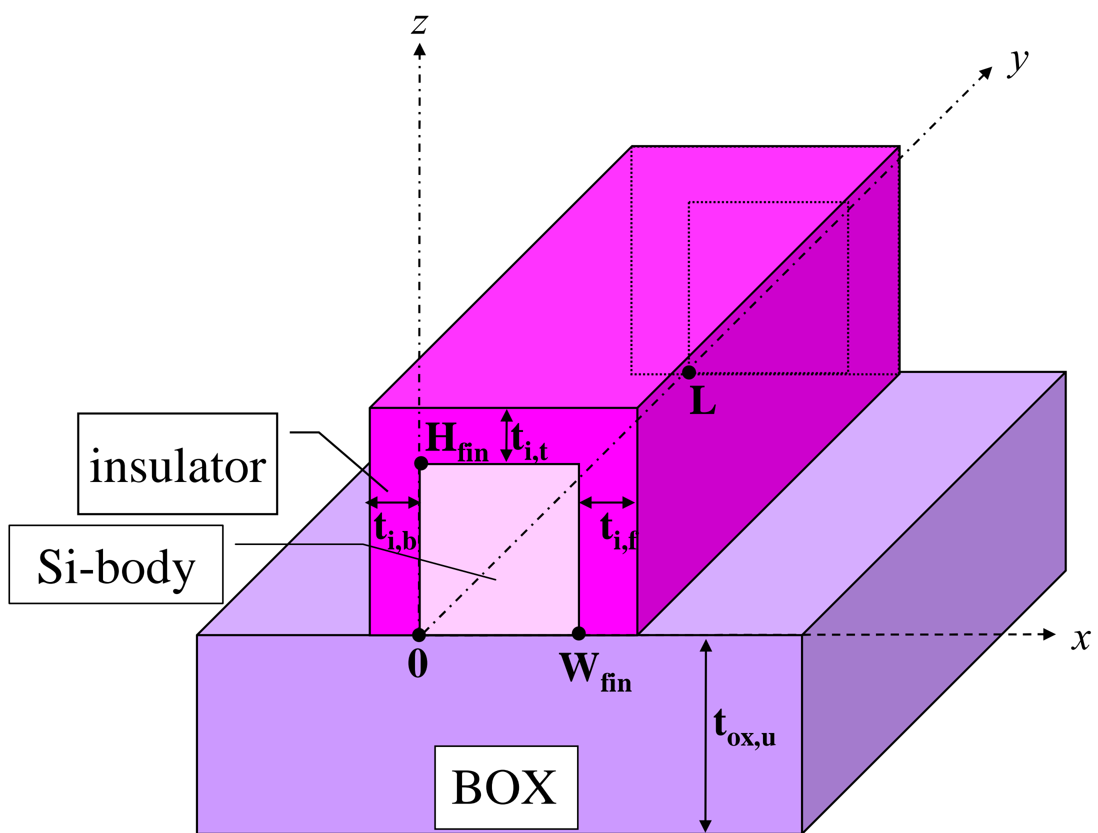
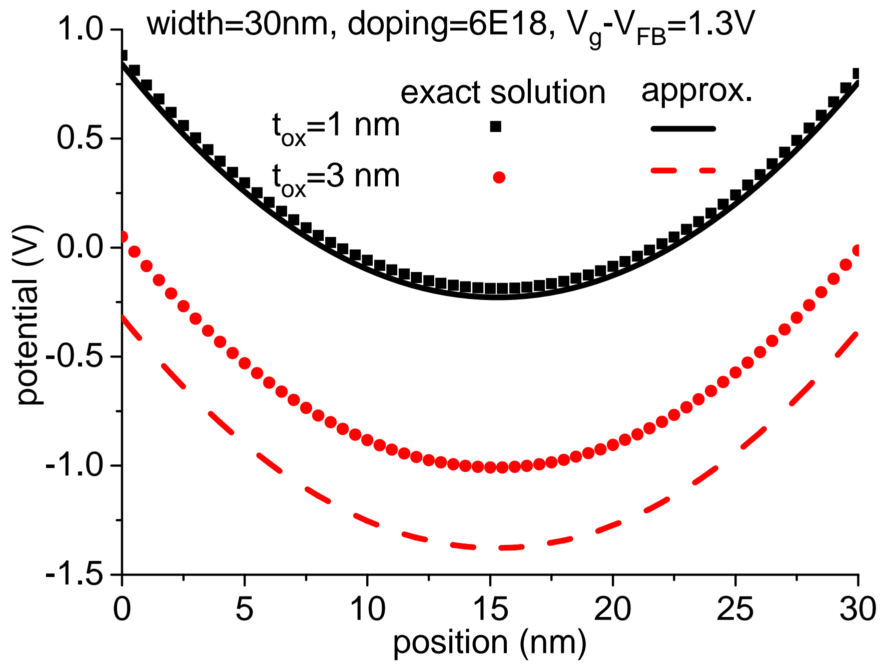
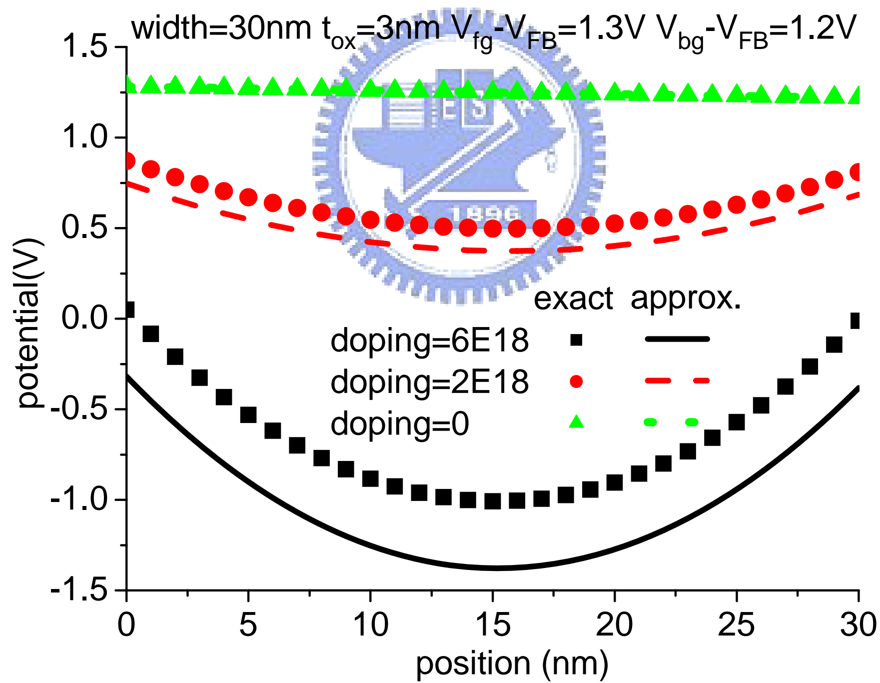


Fig. 2-1 The scheme of multiple-gate transistor structure.

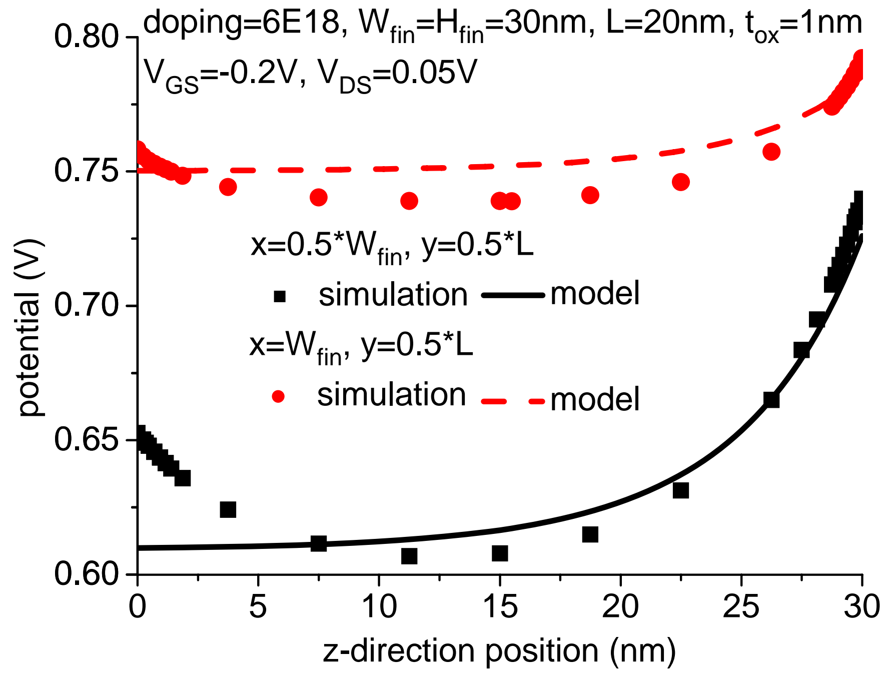


(a)

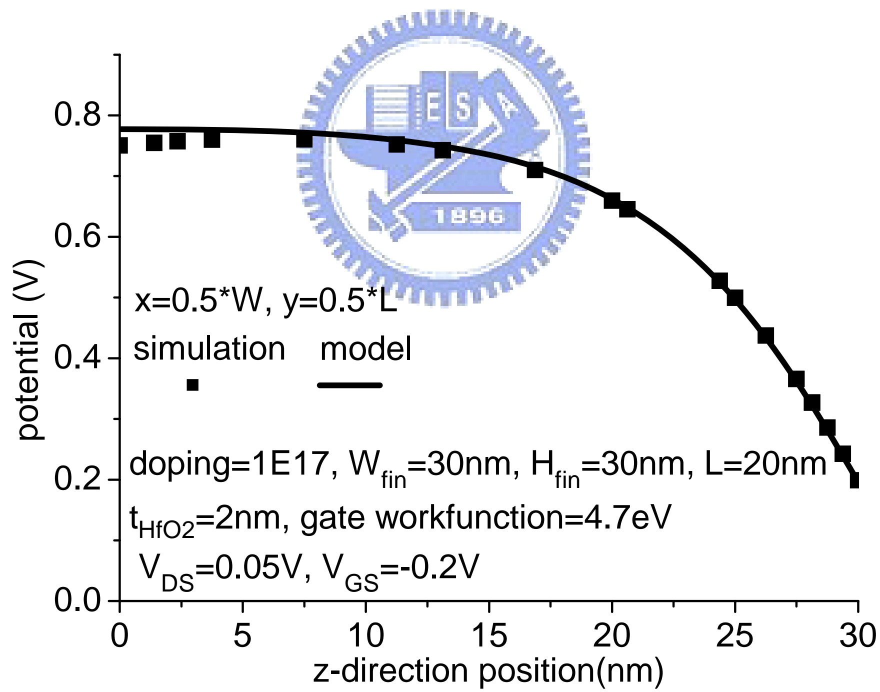


(b)

Fig. 2-2 Verification of homogeneous dielectric approximation by 1-D exact solution (a) with various oxide thicknesses, (b) with various doping concentration.

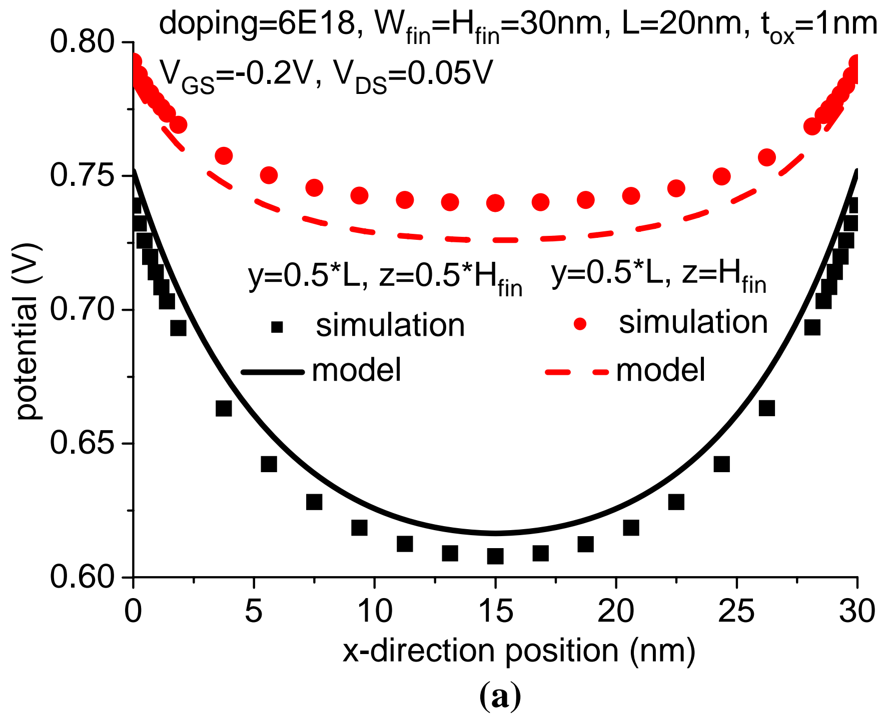


(a)

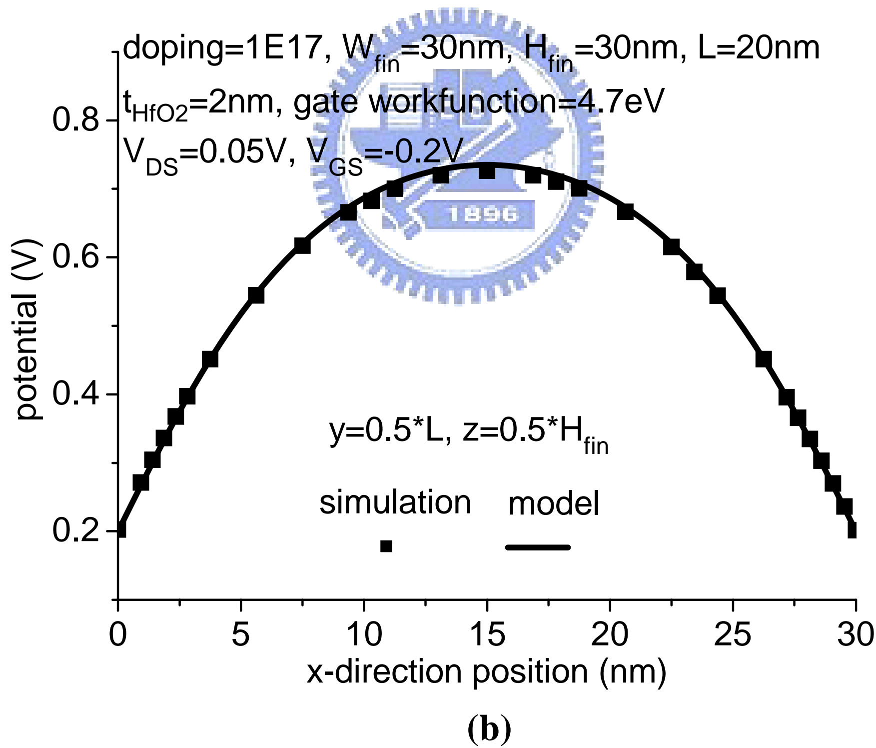


(b)

Fig. 2-3 Potential model verified with device simulation along the fin height direction (a) the positions of fin width center and gate insulator/body interface in heavily doped body, (b) the position of fin width center in heavily doped body.

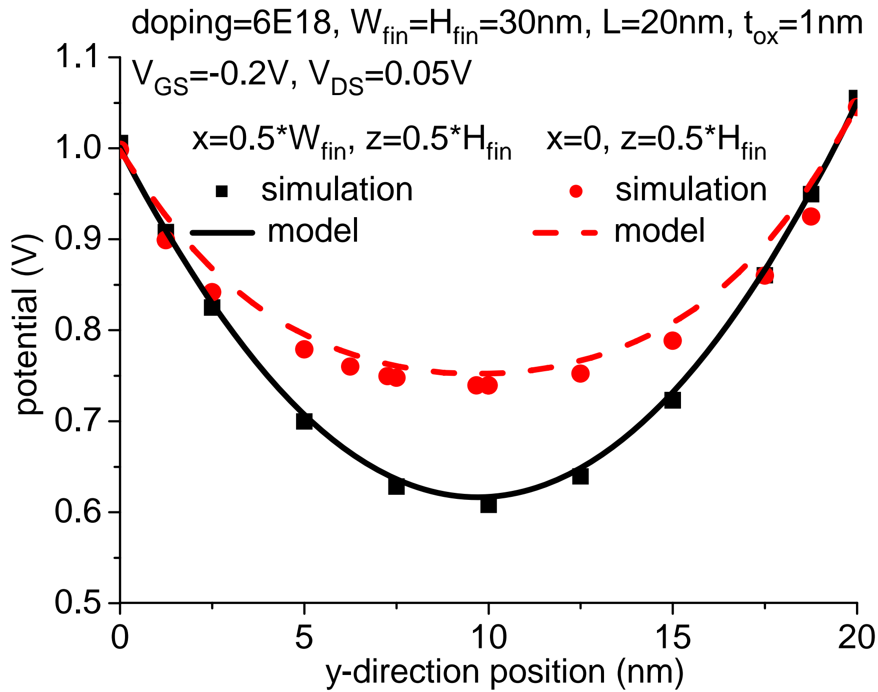


(a)

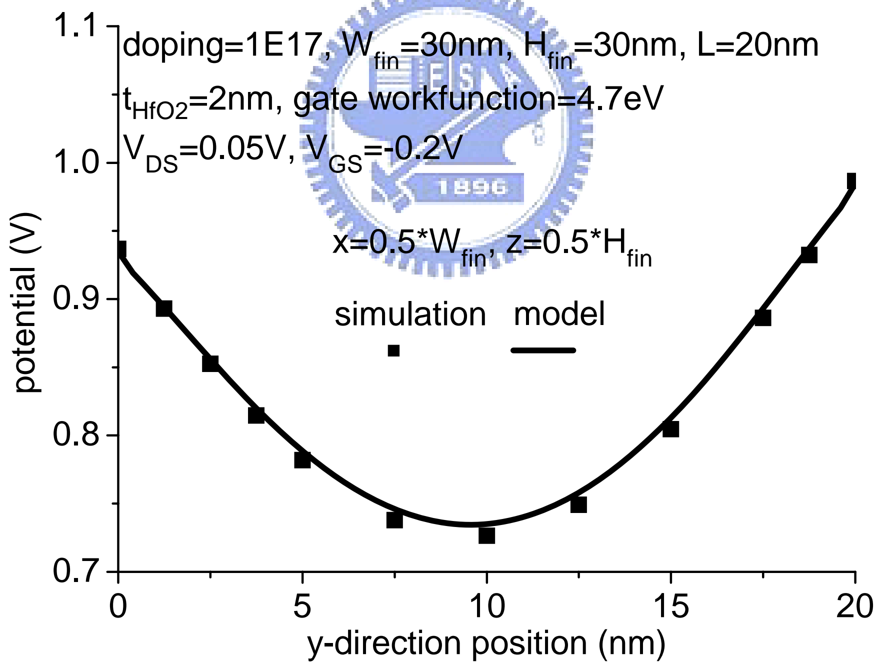


(b)

Fig. 2-4 Potential model verified with device simulation along the fin width direction (a) the positions of fin height center and gate insulator/body interface in heavily doped body, (b) the position of fin height center in heavily doped body.



(a)



(b)

Fig. 2-5 Potential model verified with device simulation along the channel length direction (a) the positions of body center and side gate insulator/body interface in heavily doped body, (b) the position of body center in heavily doped body.

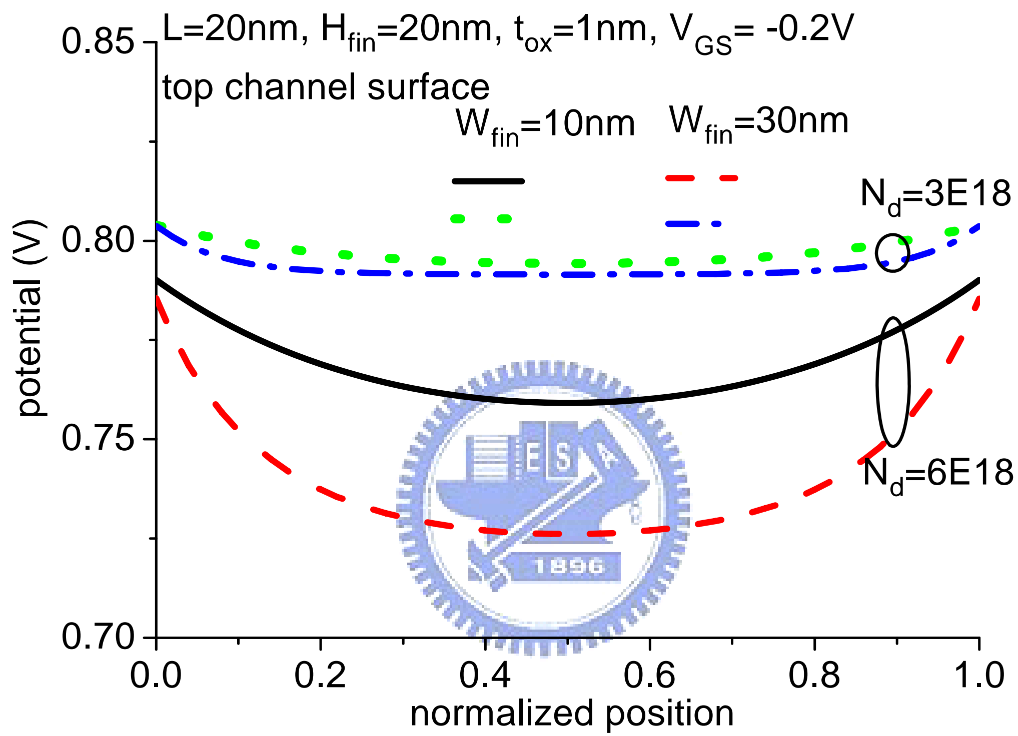


Fig. 2-6 Potential profiles of top channel showing corner effect with various fin width (10nm and 30nm) and various body doping (3E18 cm^{-3} and 6E18cm^{-3}).

Chapter 3
Threshold Voltage Determination

3.1 Introduction

After deriving the fin body potential distribution, threshold voltage for multiple-gate devices can be obtained. In this thesis, we follow two different methods for the threshold voltage analysis, one is $2\phi_B$ method [16], and the other is subthreshold current method [17]. The determination of threshold voltage will inform us of the subthreshold characteristics in multiple-gate transistors.

3.2 $2\phi_B$ Method and Verification

We suppose that the definition of threshold voltage is the gate voltage at which the highest potential barrier of the channel achieves $2\phi_B$, where ϕ_B is the difference between the Fermi level and intrinsic level of silicon in the body [16]. Thus, position of the critical point in which the highest energy barrier occurs must be determined. For electrons in NMOS, the lowest potential in the channel forms the critical barrier.

Usually drain bias is below 100mV if we focus on $V_{th,lin}$, so the potential profile along channel length direction is nearly symmetric in the source/drain sides and the lowest potential is at L/2 in length direction, as shown in fig. 2-5. Besides, in multiple-gate devices, current flows in more than one channel and each one must be included when considering the whole device characteristics.

For heavily-doped double-gate FinFETs, two symmetrical side gates induce two current conduction paths. According to fig. 2-3(a) in chapter 2, our potential model

predicts the lowest potential is at position $z=0$, i.e. body/BOX interface. However, the device simulation shows a different result in fig. 2-3(a), and the lowest potential moves into Si-fin body due to lateral field in BOX region. Therefore, we pick $z=0.5H_{fin}$ as the critical point to represent the side channel since the lowest potential is located around height center actually. Threshold voltage can be uniquely determined similar to conventional single-gate case due to symmetry in double-gate FinFET.

Fig. 3-1 illustrates the threshold voltage roll-off of double-gate FinFET, and the results are compared with 3-D device simulation. The double-gate FinFET structure demonstrated in fig. 3-1 possesses two side channels with oxide thickness 1nm. The top oxide thickness is equal to 5nm, which is five times thicker than side gate oxides and ensures top channel insulated from top gate coupling. The result shows that $2\phi_B$ method can model threshold voltage roll-off of double-gate FinFET.

As for heavily-doped Tri-gate transistors, in addition to the two side channels, top gate also contributes to a top channel and its lowest potential is at $W_{fin}/2$ in fin width direction, as illustrated in fig. 2-4(a). Therefore, in Tri-gate transistor, threshold voltage value for top gate is not equal to these of the two identical side gates, and the two different values construct upper and lower bounds for the whole device threshold voltage. Based on the method of $2\phi_B$ at the critical point, we can estimate a spread of threshold voltage for multiple-gate transistor.

Fig. 3-2(a) and (b) show the threshold voltage roll-off of Tri-gate compared with simulation. The simulation result of fin width 20nm in fig. 3-2(a) is located at the spread formed by the side and top channel bounds predicted by our model, as we expected. Unfortunately, the simulation result of fin width 30 nm in fig. 3-2(b) drops out the spread estimated by our model. The spread predicted by our model is more severe in threshold voltage roll-off relative to the simulation results. Another

mechanism enhances gate control ability and lowers the degree of threshold voltage roll-off. Since in our model, only one critical point in each channel is considered, other positions are omitted in determining threshold voltage of the whole device. In Tri-gate transistors, the corner regions also influence the subthreshold characteristics, as demonstrated in [14]. But the distribution of corner region is not considered in our model. Therefore, the model error for this case is attributed to corner effect, which has been discussed in chapter 2.

Thus, although the $2\phi_B$ method is simple and also useful for conventional planar MOSFETs, some disadvantages still exist:

(1) Not all the positions in Si-fin body are included in this method. Only the highest barrier position in each channel is considered, which is not reasonable in Tri-gate case because there may be significant current flowing in the corner region.

(2) This method is not suitable for lightly doped case. In lightly doped fin body, according to the potential profile in fig. 2-3(b), the potential close to the Si/BOX interface is relatively high, and hence most electrons move in the Si-fin instead of the surface position in subthreshold region. The concept of the highest potential barrier at the body surface is not applicable anymore. Moreover, in lightly doped case, even though the highest barrier can be determined, this definition cannot be used because of $2\phi_B \approx 0$ [16].

(3) In Tri-gate devices the threshold voltage is not a unique value. From the $2\phi_B$ method, threshold voltage value from the top channel and side channel form a spread. Though the exact threshold voltage may be located in the spread, it is inconvenient to investigate the threshold voltage values of multiple-gate devices with regard to comparison in various conditions.

Based on these reasons above, the second method for threshold voltage

determination is introduced.

3.3 Subthreshold Current Method

In order to improve (1) and (3) in $2\phi_B$ method drawbacks, it is straightforward to adopt some weighting method to consider more positions in the fin body to obtain a unique threshold voltage value representing the overall transistor. A physical weighting method is to calculate the contribution of current density at every position in the fin body. For this purpose, the subthreshold current model is used.

The subthreshold current density [17] can be demonstrated as

$$J = -q\mu n(x, y, z)\frac{d\phi_n(y)}{dy} \tag{3-1}$$

Integrating the current density in fin width (W_{fin}) and height (H_{fin}) directions gives

$$I_{ds}(y) = -\mu\frac{d\phi_n(y)}{dy}Q_i(y_{min}) \tag{3-2}$$

and $Q_i(y_{min})$ is the inversion charge term at y_{min}, and is written as

$$Q_i(y_{min}) = -q\int_0^{H_{fin}}\int_0^{W_{fin}} n(x, y_{min}, z)dxdz = -q\int_0^{H_{fin}}\int_0^{W_{fin}} \frac{n_i^2}{N_d}\cdot e^{\frac{q[\varphi(x,y_{min},z)-\phi_n(y)]}{kT}}dxdz \tag{3-3}$$

By use of potential equation derived in Chapter 2, we get the subthreshold current

$$I_{ds} = q\mu\frac{n_i^2}{N_d}\frac{kT}{q}\left(1-e^{-\frac{qV_{DS}}{kT}}\right)\cdot\frac{1}{L}\cdot\int_0^{H_{fin}}\int_0^{W_{fin}} e^{\frac{q\phi(x,y_{min},z)}{kT}}dxdz \tag{3-4}$$

where $\phi(x, y_{min}, z)$ is the potential at y_{min}. And the mobility μ is assumed to be constant ($1417cm^2/Vs$ for electron and $470.5cm^2/Vs$ for hole) [8] in the subthreshold region,

which is the same as default values in our device simulation.

The integration in equation (3-4) is replaced by summation in our numerical calculation, and the equation can be rewritten as

$$I_{ds} = q\mu \frac{n_i^2}{N_d} \frac{kT}{q}\left(1 - e^{-\frac{qV_{DS}}{kT}}\right) \cdot \frac{1}{L} \cdot \sum_{x_i}^{n_x} \sum_{z_i}^{n_z} \left[e^{\frac{q\varphi(x_i, y_{\min}, z_i)}{kT}} \left(\frac{W_{fin}}{n_x}\right) \cdot \left(\frac{H_{fin}}{n_z}\right) \right] \quad (3\text{-}5)$$

where n_x and n_z denote the partition number in fin width and fin height, respectively.

Besides, in order to consider the transistor under the saturation region, the highest barrier along the length direction will be no longer at the length center. In linear region, the highest barrier for electron is at L/2 due to nearly symmetrical potential distribution at source and drain sides. When high V_{DS} is exerted, the potential at the drain side is pulled up, and the lowest potential moves toward the source side. And the revised equation for the critical position where the lowest potential occurs along the length direction can be written as [12]

$$y_c = \frac{L}{2} + \frac{L_d}{2\pi} \ln\left(\frac{-\phi_{ms}}{-\phi_{ms} + V_{DS}} \right) \quad (3\text{-}6)$$

where $L_d = \dfrac{1}{\sqrt{\left(1/W_{fin}\right)^2 + \left(0.5/H_{fin}\right)^2}}$ (3-7)

Here we can clearly tell that the critical position along channel length direction depends on geometry and source/drain barrier. When V_{DS} is small, the critical point y_c again returns to L/2.

After deriving the subthreshold current of the whole device, a constant current definition of threshold voltage is used. Here, we define the threshold voltage as the gate voltage when $I_d = 300\,nA \times W_{total}/\text{L}$, where W_{total} is the total width, which is $2H_{fin}+W_{fin}$ for Tri-gate, and $2H_{fin}$ for double-gate FinFET.

Fig. 3-3 redraws fig. 3-2(b), and the threshold voltage roll-off derived by

subthreshold current model is added in. The simulation result is not captured by the upper and lower bounds from $2\phi_B$ method, but the subthreshold current method fits the simulation points very well. It seems that the subthreshold current method includes the corner regions in multiple-gate devices, as we expect. The disadvantages (1) and (3) are successfully solved in this case, and further verification will be discussed in the next section.

Since we have determined threshold voltage through subthreshold current instead of the method $2\phi_B$ at the critical point, now the threshold voltage value for lightly doped case can be derived as well, and the disadvantage (2) in $2\phi_B$ method can also be accessed by subthreshold current method. The subthreshold current method will be adopted to be the primary one to obtain threshold voltage in this thesis. The threshold voltage comparison agrees well with simulation result, but the assumption in the subthreshold current model is not very reasonable. The parameter mobility is required in subthreshold current model, which is temporarily assumed to be constant in both our model and simulation. In reality, the mobility in subthreshold region is an issue for argument. It seems that the assumption of constant mobility in subthreshold region is too rough. The concept of $2\phi_B$ method is straightforward because it is related to the basic band diagram theory in MOSFET. The annoying parameter mobility is not involved in the $2\phi_B$ method. But due to some disadvantages in dealing with multiple-gate structures, subthreshold current method replaces the $2\phi_B$ method. Once the problems in critical points determination are solved, the $2\phi_B$ method will be a good candidate for threshold voltage modeling. Therefore, the equation form for the threshold voltage in multiple-gate transistors will be more visible, and may be a good implication for the establishment of compact model.

3.4 Verification for Subthreshold Current Method

The modeling results of threshold voltage by subthreshold current method are shown as following. In addition, by modeling subthreshold current, subthreshold swing can be derived at the same time. Besides, in both our model and numerical simulation, the gate workfunction issue is not considered yet. Thus, the threshold voltage values are not optimized for realistic application. However, it is not a matter since our purpose here is to verify the accuracy of our threshold voltage model. And the conditions for device simulation and model can be adjusted to the same level artificially. The gate electrode is equivalent to conventional heavily doped n^+ poly gate in n-MOSFET.

Fig. 3-4(a) and (b) show the threshold voltage and subthreshold swing versus doping concentration, respectively. Two insulator materials including oxide thickness 1nm and HfO_2 (high k dielectric) thickness 2nm are plotted. The figures tell us that beyond $1\times10^{18}cm^{-3}$, the value of threshold voltage and subthreshold swing are both very sensitive to doping level. This implicates that it is a useful method to suppress short channel effect by rising doping concentration. As doping level is below $1\times10^{18}cm^{-3}$, subthreshold swing becomes very worse, and apparently not feasible if no other factors are added in to increase short channel control. Apart from body doping, gate insulator is another factor to determine gate control ability. However, oxide thickness below 1nm is technologically difficult to achieve due to serious gate leakage issue. Therefore, high k dielectric materials are suggested to replace oxide to reduce equivalent oxide thickness (EOT). In fig. 3-4(a), the HfO_2 ones have better gate control than those with oxide, and the degradation of threshold voltage by reducing doping concentration is smaller. As long as the gate workfunction is regulated to

optimize threshold voltage values in n-MOSFET, the use of high k dielectric will be a good alternative to suppress short channel effect. In fig. 3-4(b), subthreshold swing of HfO_2 ones are lower than these with oxide. In lightly doped region (below $10^{18}cm^{-3}$), high k dielectric noticeably improves the subthreshold swing. In heavily doped region, the use of high k dielectric will further suppress the short channel effect.

Threshold voltage values versus other geometric parameters are discussed as well. Fig. 3-5(a) shows threshold voltage values versus fin height, and the upper line and lower dash denote the model for heavily doped and lightly doped body, respectively. In the following discussion, the gate insulator used for heavily doped body is oxide, while the gate insulator for lightly doped case is high k dielectric [7]. Heavily doped body coupled with high k dielectric will indeed have excellent short channel behaviors, but the gate insulator for heavily doped body is oxide due to process complexity. The model is consistent with simulation results. But the threshold voltage seems insensitive to various fin height at this scale. After rescaling the vertical-axis (threshold voltage) in fig. 3-5(a), as shown in fig. 3-5(b), the behavior of threshold voltage versus fin height can be observed more clearly. In heavily doped body, corner regions exhibit higher potential than other positions in the channel, as discussed in chapter 2. The corner region will dominate the whole device as the transistor size scales down, and early turn on due to corner region is observed. Therefore, with decreasing fin height, threshold voltage rolls off in heavily doped body, while it rises up in lightly doped one, as shown in fig. 3-5(b). In lightly doped case, the reason for threshold voltage increase with fin height scaling is simply due to better short channel control. The contradictory in heavily and lightly doped cases is mainly attributed to corner effect.

Threshold voltage versus fin width is similar to the consequences in fin height, as

shown in fig. 3-6(a) and (b). Besides, a larger variation in threshold voltage is observed with fin width scaling than fin height scaling. This is due to sensitivity difference to fin width and fin height, which will be discussed in the next chapter.

The typical phenomenon to represent short channel effect is threshold voltage roll-off with decreasing channel length, as shown in fig. 3-7 to fig. 3-9. Three sets of different conditions are compared between model and simulation. Heavily doped with oxide thickness 1nm, lightly doped with oxide thickness 1nm, and lightly doped with high k dielectric (HfO_2) 2nm are included. It is well known that increasing doping concentration and reducing EOT (equivalent oxide thickness) both improve short channel effect, but increasing V_{DS} degrades short channel control. Fig. 3-7 shows the threshold voltage value in heavily doped and lightly doped bodies, and simulation results and model are included. Heavily doped ones have higher threshold voltage values, and slighter roll-off relative to lightly doped ones. Gate workfunction engineering is needed for the threshold voltages in lightly doped case.

Fig. 3-8 shows the threshold voltage value in heavily doped body, and low V_{DS} threshold voltage ($V_{t,lin}$) and high V_{DS} threshold voltage ($V_{t,sat}$) are compared. High drain bias degrades short channel behavior, and the impact on threshold voltage value and roll-off can be observed. Fig. 3-9 shows lightly doped body with oxide thickness 1nm and HfO_2 thickness 2nm. Apparently high k dielectric HfO_2 (dielectric constant=25) has better short channel control even its realistic thickness is thicker than oxide (dielectric constant=3.9). Our model can point out the difference in threshold voltage roll-off of insulators with different dielectric constant.

3.5 Summary

By use of potential solution derived in chapter 2, two methods for determining threshold voltage are proposed. $2\phi_B$ method is simple and useful for planar devices and double-gate FinFET. However, the critical position in Tri-gate is difficult to determine, and the weighting of threshold voltages from different critical positions is still an unsolved issue. Therefore, subthreshold current method is used to compensate the drawbacks in $2\phi_B$ method. The subthreshold current is calculated from integration of terms related to body potential, and by use of constant current method for threshold voltage, the threshold voltage values are obtained and verified with simulation. By our model, the threshold voltage dependences on doping concentration, fin height, fin width, and channel length are shown, and the results agree with the threshold voltage values from device simulation.

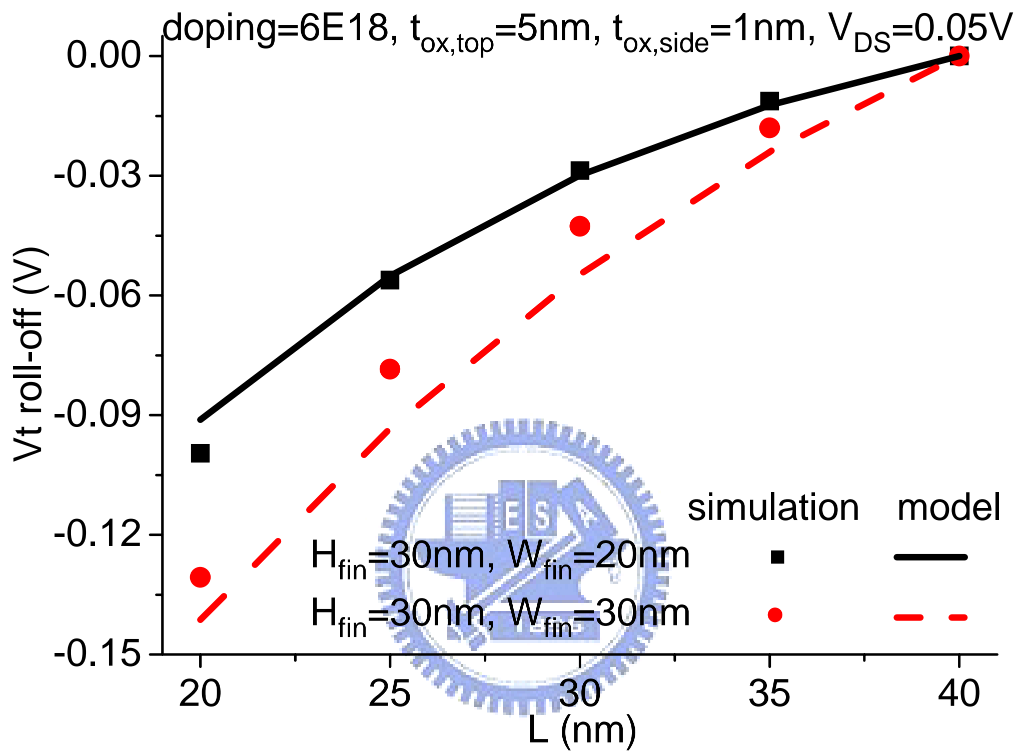
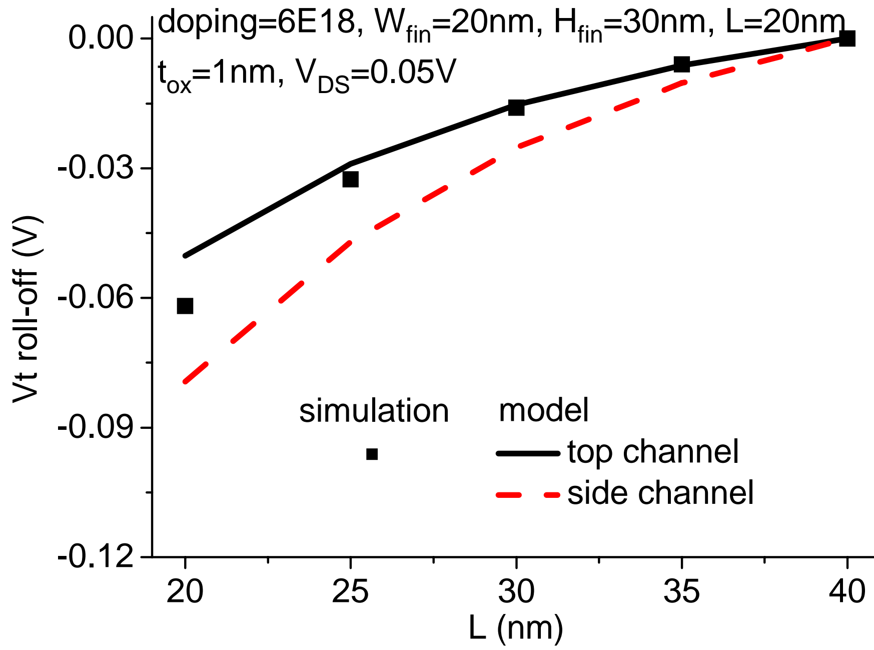
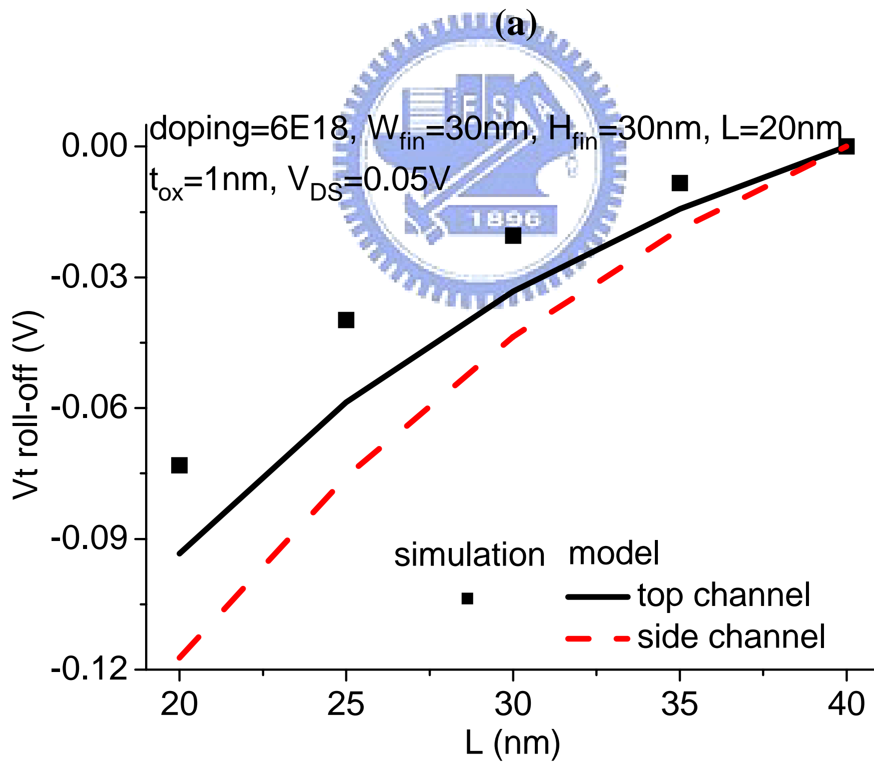


Fig. 3-1 Double-gate FinFET threshold voltage roll-off derived by $2\phi_B$ method verified with device simulation.



(a)



(b)

Fig. 3-2 Tri-gate threshold voltage roll-off derived by $2\phi_B$ method verified with device simulation (a) fin width = 20nm, and (b) fin width = 30nm.

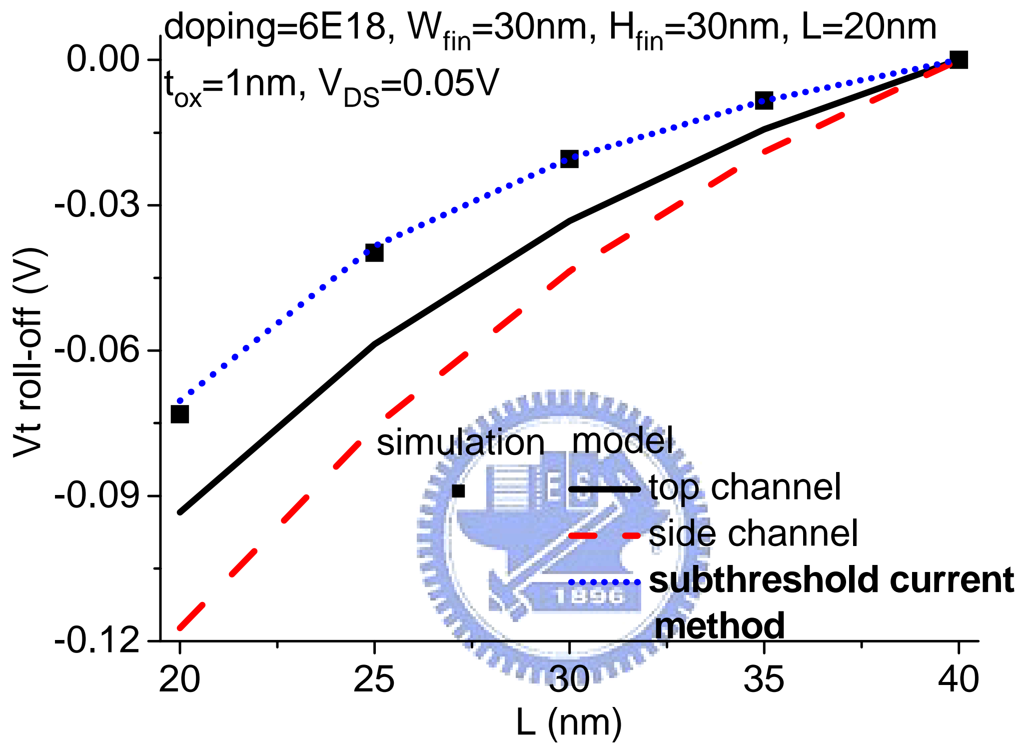
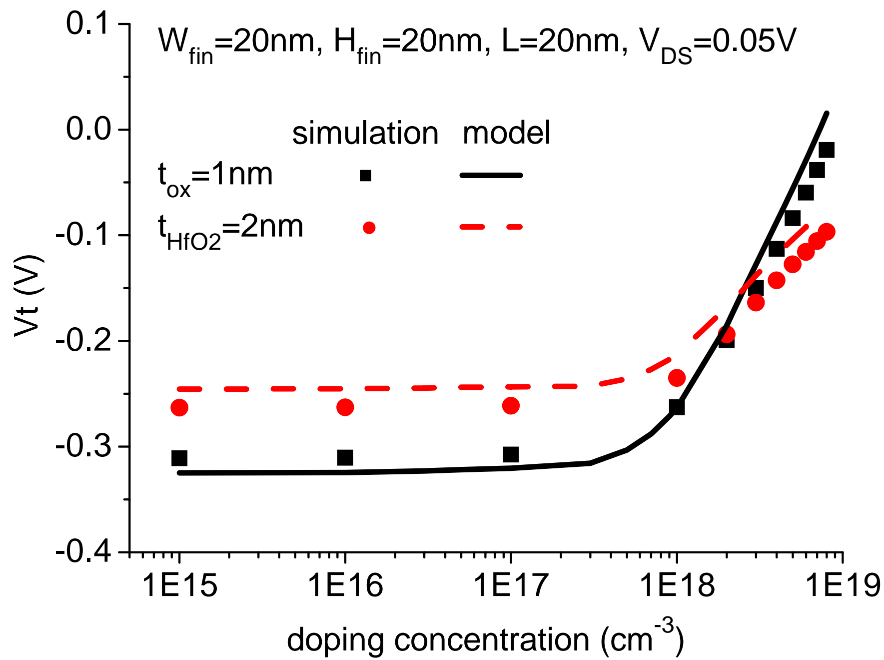
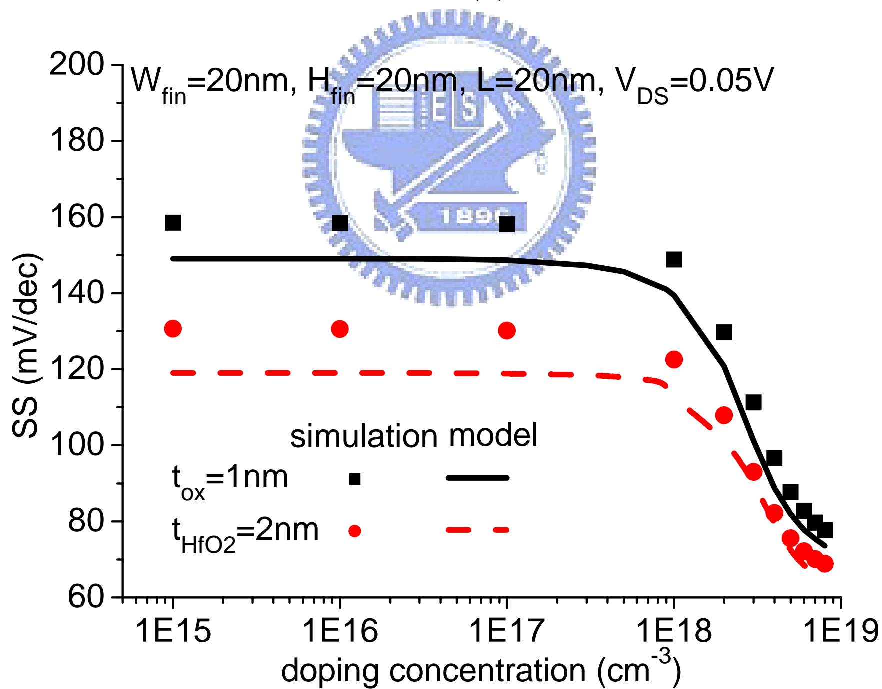


Fig. 3-3 Tri-gate threshold voltage roll-off with fin width = 30nm derived by $2\phi_B$ method and subthreshold current method, verified with device

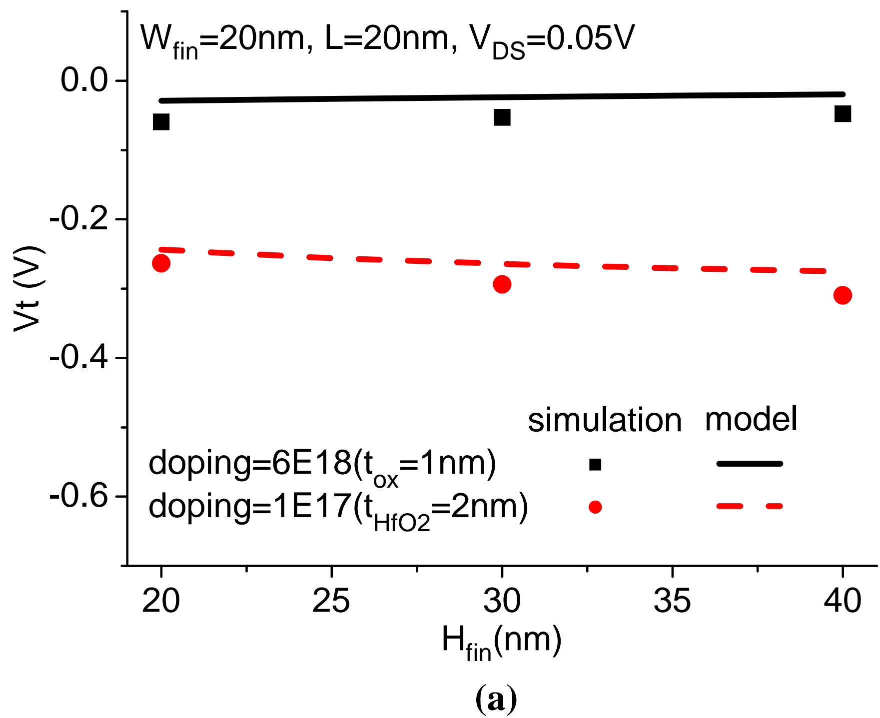


(a)

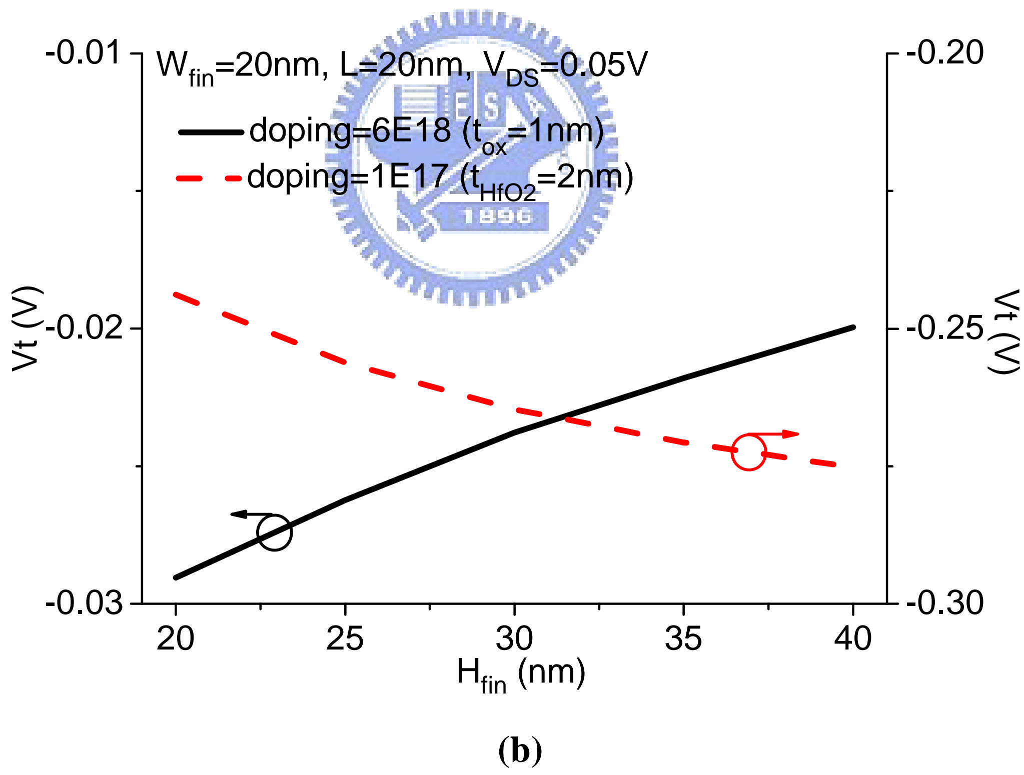


(b)

Fig. 3-4 Subthreshold current model predicted heavily doped body with oxide and lightly doped body with high k dielectric (a) threshold voltage values and (b) subthreshold swing values, verified with device simulation.

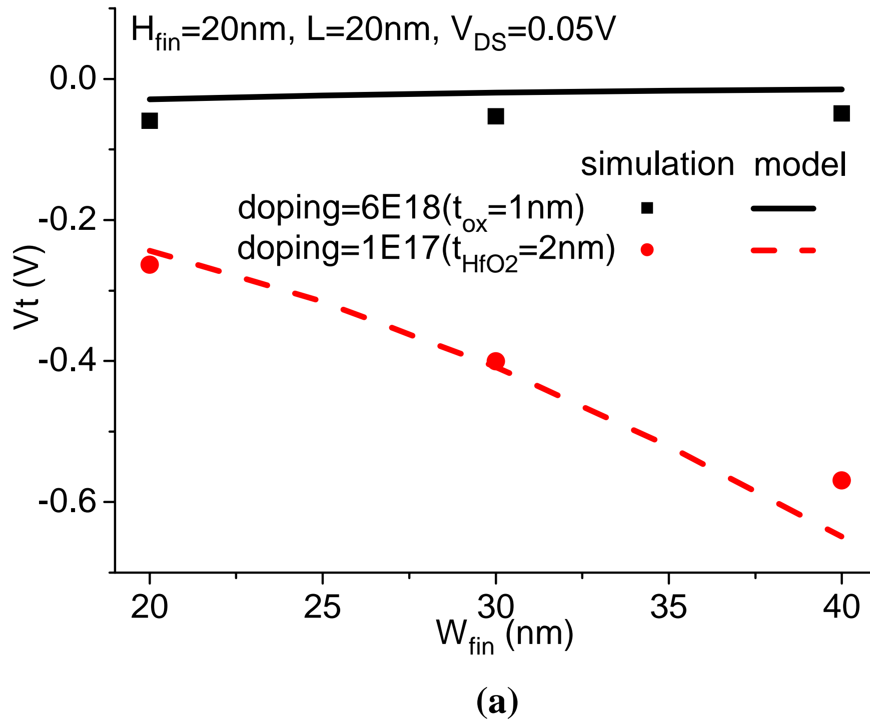


(a)

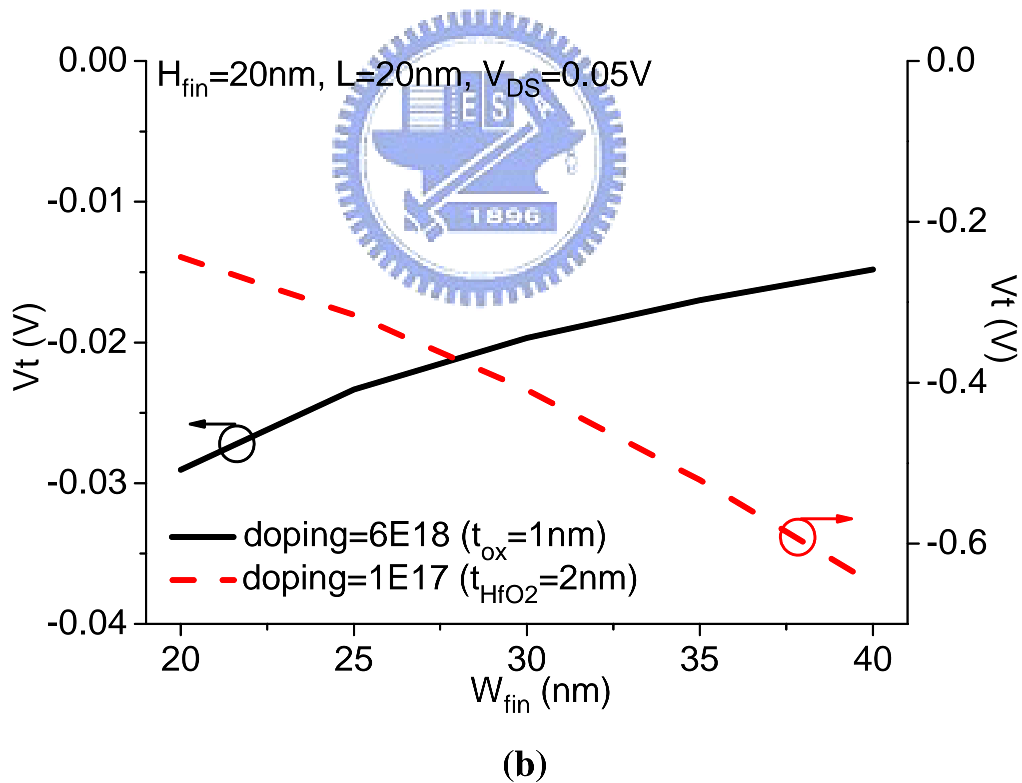


(b)

Fig. 3-5 Threshold voltage with various fin height in (a) heavily doped body with oxide and lightly doped body with high k dielectric, and (b) the rescaling of (a) to show the opposite trend between heavily and lightly doped cases.



(a)



(b)

Fig. 3-6 Threshold voltage with various fin width in (a) heavily doped body with oxide and lightly doped body with high k dielectric, and (b) the rescaling of (a) to show the opposite trend between heavily and lightly doped cases.

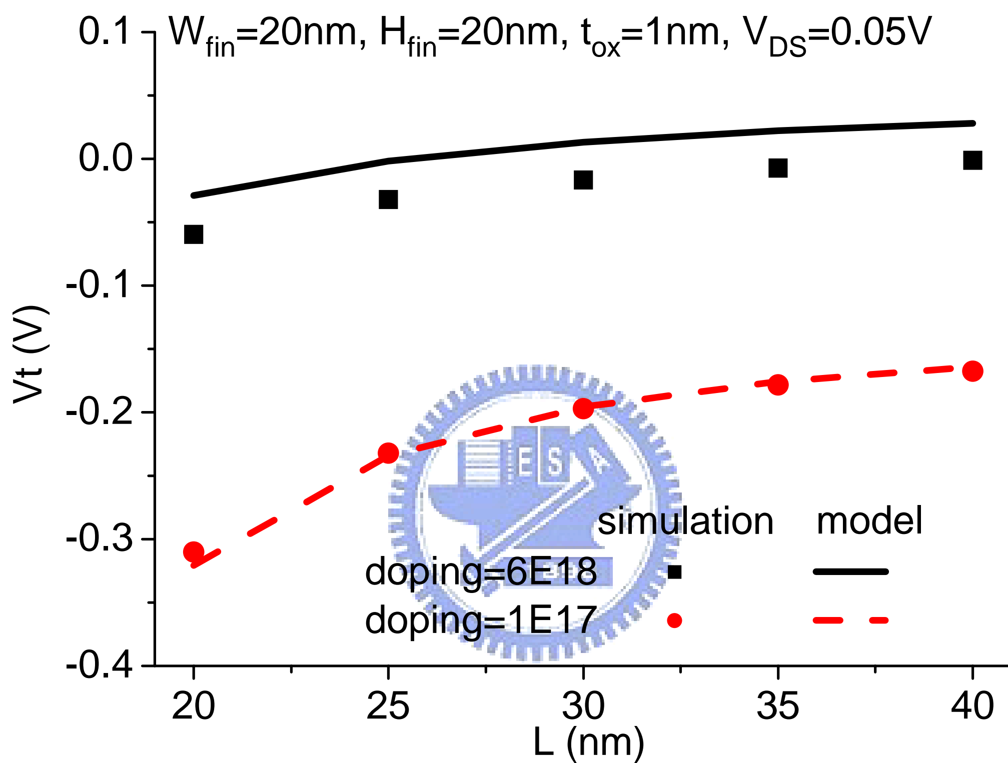


Fig. 3-7 Threshold voltage roll-off comparison between heavily doped and lightly doped bodies with oxide to be gate insulator and low drain bias.

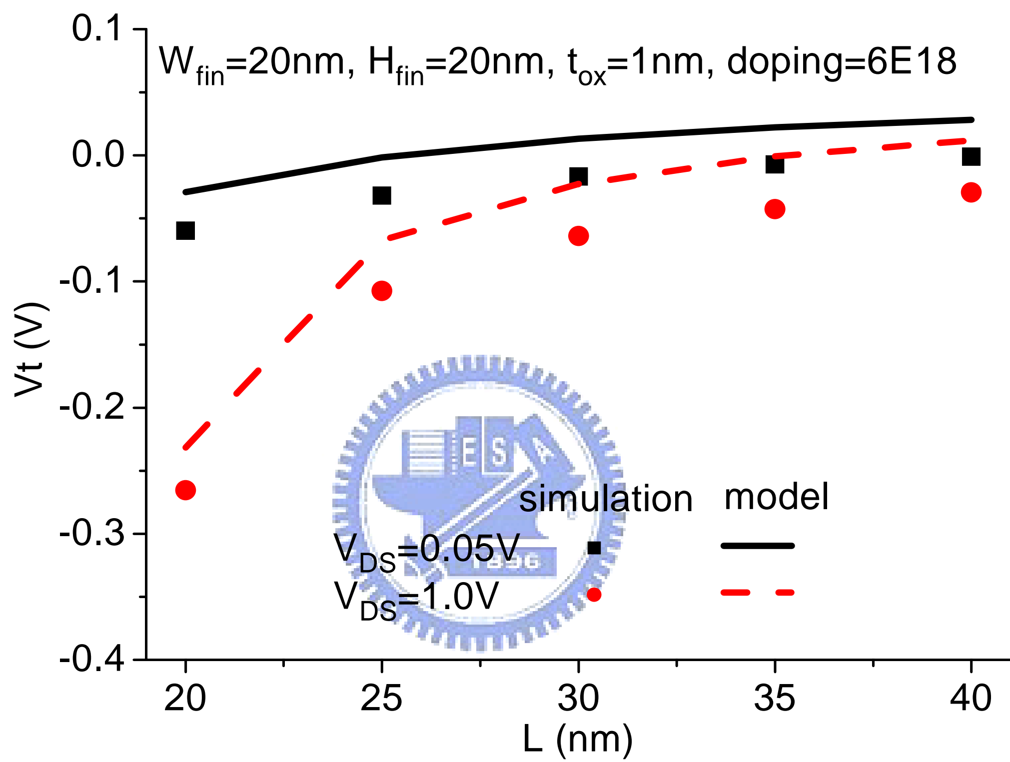


Fig. 3-8 Threshold voltage roll-off comparison between high drain bias and low drain bias with oxide to be gate insulator and heavily doped body.

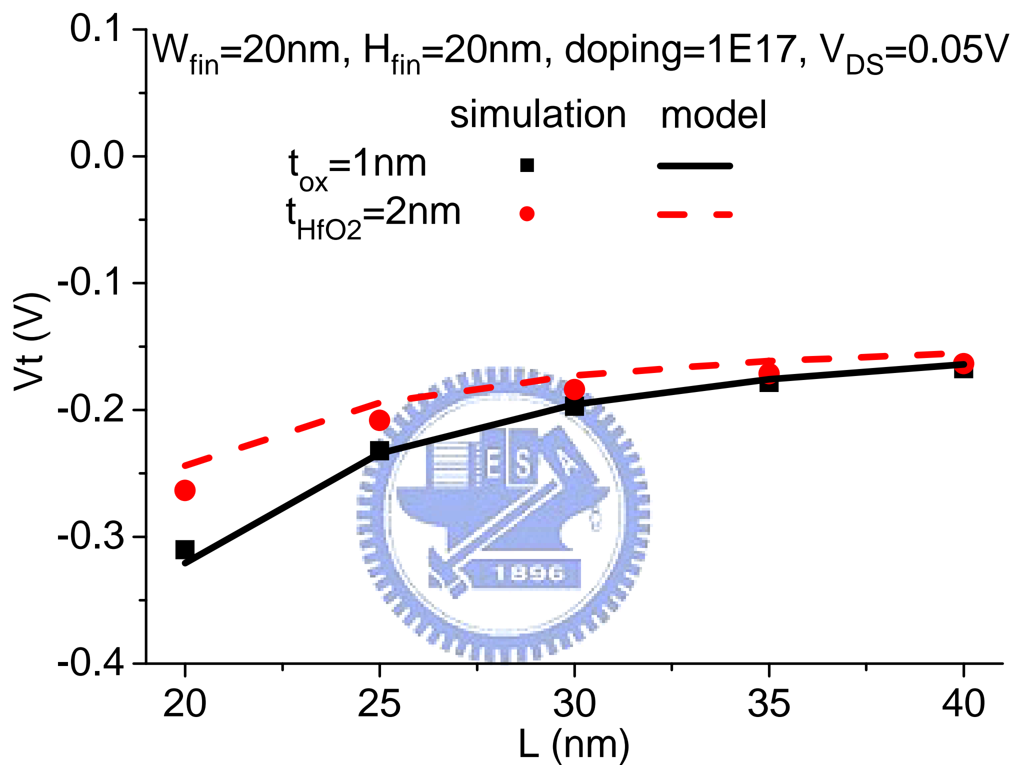


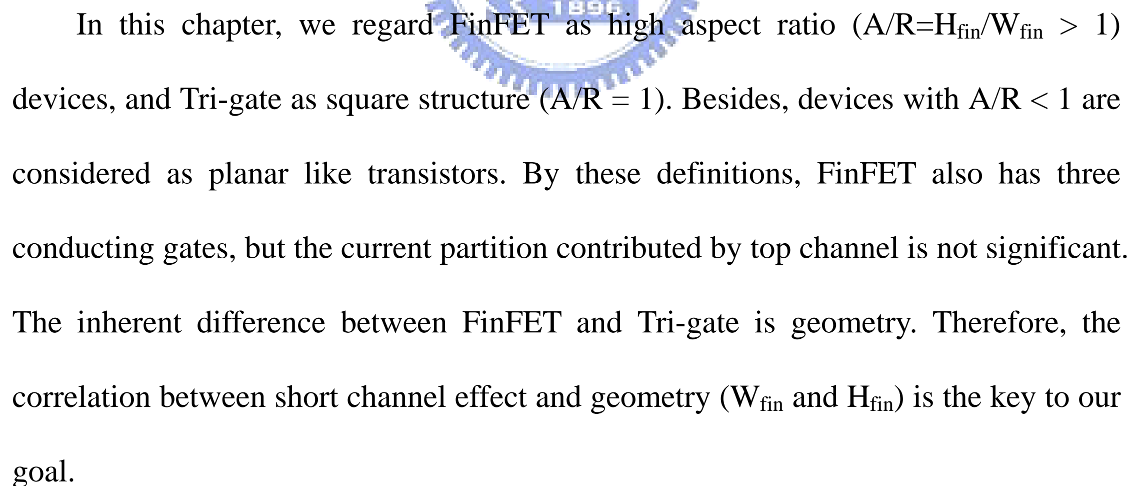
Fig. 3-9 Threshold voltage roll-off comparison between gate insulator oxide and gate insulator high k dielectric with lightly doped body and low drain bias.

Chapter 4
Design Considerations in Multiple-Gate Transistors

4.1 Introduction

We have derived a threshold voltage model, and the subthreshold swing can be obtained by subthreshold current method. As mentioned in chapter 1, the primary purpose of this thesis is to investigate the short channel behavior in multiple-gate MOSFETs, and to select a better design structure between FinFET and Tri-gate.

4.2 Sensitivity Difference in Fin width and Fin Height



In this chapter, we regard FinFET as high aspect ratio ($A/R=H_{fin}/W_{fin} > 1$) devices, and Tri-gate as square structure ($A/R = 1$). Besides, devices with $A/R < 1$ are considered as planar like transistors. By these definitions, FinFET also has three conducting gates, but the current partition contributed by top channel is not significant. The inherent difference between FinFET and Tri-gate is geometry. Therefore, the correlation between short channel effect and geometry (W_{fin} and H_{fin}) is the key to our goal.

It is well known that both W_{fin} and H_{fin} scaling improve short channel control [4], [9], [18]. The fabrication result in [19] showed that decreasing H_{fin} causes degradation of subthreshold swing, which is not consistent with [4] and [9]. There may be some variation issue in the fabrication data in [19]. Our model shows the same trend as [4], [9], [18], and will be shown in the following figures. In multiple-gate devices, along

width direction the two side gates are symmetrical and identical, while along height direction, the gate electrode under BOX is nearly insulated to Si-body, and only the top gate is functional. With fin width scaling, the body is affected by better control of both two side gates. However, as fin height scales, the Si-body is affected merely by the single top gate. Fig. 4-1 shows the variations in threshold voltage roll-off when fin width and fin height are scaled down separately in heavily doped body. The results show that threshold voltage roll-off is more sensitive to fin width scaling as fin height kept the same. Therefore, fin width scaling benefits more than fin height scaling in suppressing short channel effect. The intrinsic difference between W_{fin} scaling and H_{fin} scaling in Tri-gate will influence the device geometry design.

Fig. 4-2(a) shows the results in lightly doped case. The primary difference in lightly doped body is greater discrepancy between W_{fin} scaling and H_{fin} scaling. This is because in lightly doped body, geometry is the dominant factor to suppress short channel effect instead of doping level in heavily doped case. The threshold voltage roll-off sensitivity difference to W_{fin} and H_{fin} is more obvious in lightly doped body. However, if another factor is added in to suppress short channel effect, this threshold voltage roll-off sensitivity difference will be reduced. Fig. 4-2(b) shows the results in lightly doped body with high k dielectric HfO_2. As mentioned in the previous chapters, EOT reduction by using HfO_2 assists in short channel effect suppression, and the sensitivity difference to W_{fin} and H_{fin} is reduced compared with fig. 4-2(a), in which oxide is the gate insulator. Besides, if the short channel effect becomes more severe, the sensitivity difference to W_{fin} and H_{fin} will be amplified. Fig. 4-2(c) shows the results in heavily doped body at high drain bias, and can be compared with low drain bias results in fig. 4-1. In the short channel region (L=20nm), the sensitivity difference increases due to subthreshold characteristic degradation by drain induced

barrier lowering. To sum up, if geometry is the dominant factor in short channel effect suppression, the threshold voltage roll-off sensitivity difference to W_{fin} and H_{fin} will be enlarged. Besides, if short channel effect is serious, the sensitivity difference to W_{fin} and H_{fin} will increase as well.

The idea that fin width scaling benefits more than fin height scaling is a significant implication in multiple-gate geometry design. For example, to maintain good subthreshold behavior, fin width reduction by 10nm is needed with fixed fin height. However, with fixed fin width, fin height reduction by more than 10nm (perhaps 20nm) is necessary. This means that keeping small fin width will be the first alternative in the suppression of short channel effect.

4.3 Total Width

Geometry scaling will suppress the short channel effect, but degrades the on-state current (I_{on}) at the same time. When transistor is turned on, the current is proportional to the total width of the transistor. For double gate FinFET, the total width is equal to $2H_{fin}$, and for Tri-gate the total width is equal to $2H_{fin} + W_{fin}$. Total width is also an important parameter in device design because it is directly related to I_{on}. Fig. 4-3 shows the subthreshold swing versus total width in heavily doped devices, and three difference aspect ratio devices including A/R=1 (Tri-gate), 2 (FinFET), and 0.5 (planar device). The result shows that at fixed total width, devices with higher aspect ratio have better subthreshold swing. This denotes when total width is considered, FinFET is the best choice to maintain good subthreshold characteristic. According to last paragraph, fin width scaling is more beneficial than fin height scaling. Therefore, in order to keep enough I_{on} and to maintain good subthreshold

swing simultaneously, fin width will be minimized to suppress short channel effect, and increase fin height to gain sufficient total width. The other extreme case, which is A/R=0.5, exhibits the worst subthreshold behavior due to inefficient fin height scaling instead of width scaling.

FinFET is superior to Tri-gate when both short channel control and I_{on} are both considered. The superiority depends on the short channel control difference to W_{fin} and H_{fin}. Thus, when geometry is the dominant factor in suppressing short channel effect, fin width scaling will be more significant than fin height scaling, and FinFET will be more advantageous than Tri-gate. As previously mentioned, lightly doped body and high drain bias will enhance the sensitivity difference, while heavily doped and the use of high k dielectric (smaller EOT) will decrease the sensitivity difference. Fig. 4-4 shows the subthreshold swing with various total widths in lightly doped body. The discrepancy between different aspect ratio is more pronounced compared with heavily doped case in fig. 4-3, as we predicted. On the contrary, if the gate insulator is replaced by high k dielectric, the discrepancy will be reduced, and Tri-gate design will be closer to FinFET.

The square points in fig. 4-5(a) are double-gate FinFET fabrication data in [20]. We can extract and estimate the device parameters, as the lines show. The large discrepancy in fin width 50nm may attribute to not fully depletion in such a wide width. The extraction results are listed in fig. 4-5(a). We use this parameter set to predict the FinFET and Tri-gate behaviors through our model, as shown in fig. 4-5(b). Note that subthreshold swing values of double-gate FinFET are almost independent of total width. In Tri-gate, subthreshold swing at low total width is even superior to FinFET with minimum fin width (W_{fin}=10nm), but becomes worse as increasing total width. At total width equal to 100nm, as the condition in [20], FinFET with fin width

10nm is better than Tri-gate design in short channel suppression. This case demonstrates that in FinFET design, fin width is suggested to be minimized to enhance side gate control. Larger total width favors FinFET design, while Tri-gate may be better than double-gate FinFET as total width is small.

In conclusion, when total width is considered, FinFET is a better candidate than Tri-gate in controlling short channel effect. The superiority depends on sensitivity difference to W_{fin} and H_{fin} and the total width needed. Prominent sensitivity difference and larger total width favor FinFET structure.

4.4 Minimum Feature Size

The simulation results in [14] have demonstrated some information concerning heavily doped Tri-gate transistor. Fig. 4-6(a) shows various doping concentration in the geometry domain. Contours of subthreshold swing equal to 70mV/dec, as shown in [4], is plotted in fig. 4-6(a). Following [6], [14], [21], we assume the Tri-gate design as $W_{fin}=H_{fin}=L$, and in this case we choose L=30nm, which is equal to fin width and fin height. The cross mark in fig. 4-6(a) denote the point $W_{fin}=H_{fin}=L=30nm$. By rising doping level from 5.0×10^{18} to $5.5\times10^{18}cm^{-3}$ relaxes the W_{fin} and H_{fin} size design, and make Tri-gate structure feasible because the cross mark is enclosed by the contour of $5.5\times10^{18}cm^{-3}$. According to the contour plot, doping concentration equal to $5.3\times10^{18}cm^{-3}$ is the closest one to Tri-gate subthreshold characteristic in [14]. Besides, Tri-gate is apparently feasible by adjusting the halo doping concentration

In Tri-gate structure, we regard the minimum value between W_{fin} and H_{fin} as the minimum feature size. It is straightforward that smaller minimum feature size

implicates more stringent challenge in fabrication and scaling difficulty. We take the device parameters in [14] and assume the doping concentration is $5.3\times10^{18}cm^{-3}$ as illustrated in fig. 4-6(a). Fig. 4-6(b) shows the minimum feature size with equivalent subthreshold swing 70mV/dec versus channel length. Three different aspect ratio including Tri-gate, FinFET, and planar devices are shown. In fig. 4-6(b), Tri-gate (with A/R=1) is the most scalable structure due to the biggest minimum feature size allowed. The result is consistent with [4], in which heavily doped body Tri-gate and FinFET are discussed as well. Besides, the minimum feature size in FinFET is W_{fin} due to high aspect ratio, while in planar device the minimum feature size is H_{fin} due to aspect ratio lower than 1. Minimum feature size needed for planar device at a given subthreshold swing is more stringent than that of FinFET. This is because the inefficient scaling of H_{fin} (planar device) is chose instead of W_{fin} scaling (FinFET) when suppressing short channel control.

$W_{fin}=H_{fin}$ is the most scalable structure, as shown in fig. 4-6(b). However, in the conditions of fig. 4-6(b), when channel length is reduced, the minimum feature sizes needed are aggressively scaled down as well. This is because the subthreshold swing criterion (70mV/dec) is too stringent in our investigation. If the criterion is looser, the minimum feature size needed for short channel devices will not be so difficult to achieve. Fig. 4-6(c) shows the minimum feature size in Tri-gate, and two different criteria for subthreshold swing are compared. The minimum feature sizes needed for subthreshold swing equal to 75mV/dec is more relaxed relative to 70mV/dec ones.

4.5 Feasibility of Lightly Doped Tri-gate

J. W. Yang and J. G. Fossum [6] have claimed that much more stringent body

scaling for lightly doped body is needed relative to heavily doped ones, and lightly doped Tri-gate is not feasible if the geometry $W_{fin}=H_{fin}=L$ is considered. However, the fabrication results in [7] have demonstrated that Tri-gate with lightly doped body is feasible, and in their chart n-MOSFET showed good subthreshold swing 80mV/dec and DIBL 90mV/V. By use of our model, the contradicted conclusions between these two works will be investigated.

The primary different factor for short channel control in [7] relative to [6] is the addition of high k dielectric HfO_2. Though strain technology may improve short channel control, the influence is not very significant. We use the parameters from [7] to analyze the minimum feature size needed for different structures, as illustrated in fig. 4-7(a). The square dot in fig. 4-7(a) denote the fabrication result in [7], which is located on the curve of Tri-gate ($H_{fin}=W_{fin}=L=25nm$). Fig. 4-7(a) shows Tri-gate has biggest minimum feature size at subthreshold swing 80mV/dec, and hence is the most scalable structure in lightly doped body coupled with high k dielectric. The result is very similar to heavily doped body in fig. 4-6(b), and hence Tri-gate is the most scalable structure irrespective of doping level and the criterion for subthreshold swing.

By using the conditions in fig. 4-7(a), we can duplicate the simulation work in [6] by our model. Fig. 4-7(b) is the contour plot of subthreshold swing equal to 80mV/dec in the geometry domain. The dash line denotes devices with oxide thickness equal to 15 angstrom as gate insulator. The Tri-gate condition $W_{fin}=H_{fin}=L=30nm$ (the cross mark) is too big to achieve the criterion 80mV/dec (the dash line), and obviously not feasible if we use oxide thickness 15 angstrom as the gate insulator. Nevertheless, if HfO_2 is used to reduce EOT, short channel effect will be further suppressed, and the geometry design is relaxed. The solid line in fig. 4-7(b) denotes devices with HfO_2

thickness equal to 20 angstrom. The use of HfO_2 moves the 80mV/dec contour to bigger device size. The cross mark (Tri-gate design point) is now enclosed by the solid line. That means with the aid of high k dielectric, lightly doped Tri-gate achieves the criterion subthreshold swing equal to 80mV/dec. The utilization of high k dielectric enables the feasibility of lightly doped Tri-gate, which modifies the conclusion claimed by [6].

4.6 Summary

Threshold voltage roll-off with H_{fin} scaling and W_{fin} scaling are investigated by our model. The sensitivity difference between H_{fin} scaling and W_{fin} scaling influences the geometry design. FinFET structure is suggested to achieve sufficient I_{on} and suppress short channel effect simultaneously. Tri-gate structure is more scalable than FinFET due to bigger minimum feature size allowed for given subthreshold swing. Besides, lightly doped Tri-gate is feasible if high k dielectric is plugged in.

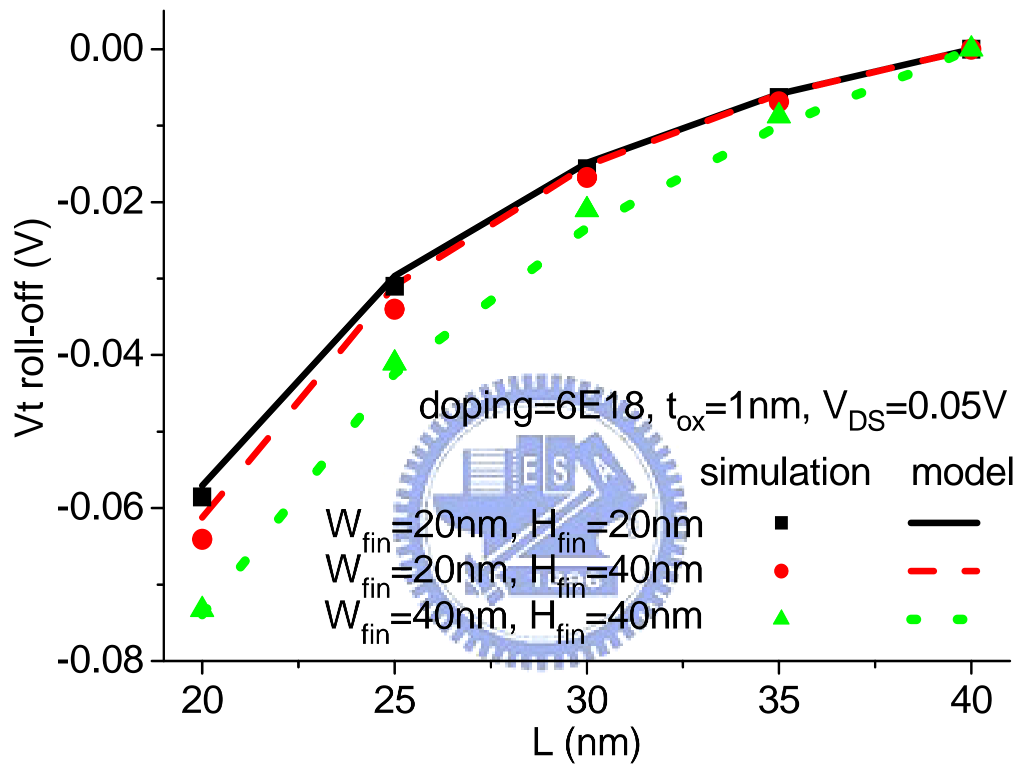


Fig. 4-1 Threshold voltage roll-off comparison between fin height scaling and fin width scaling in heavily doped body with low drain bias.

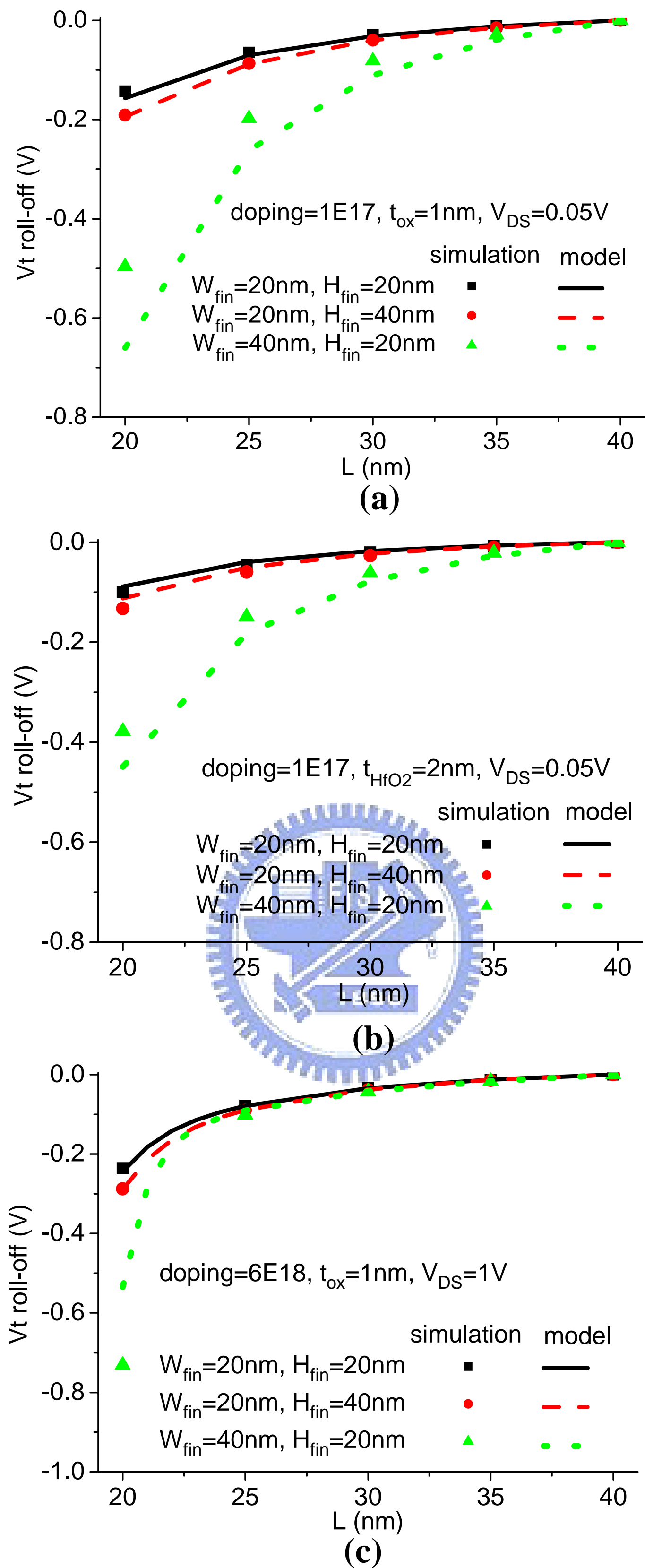


Fig. 4-2 Threshold voltage roll-off comparison between fin height scaling and fin width scaling in (a) lightly doped body with oxide to be gate insulator, and (b) lightly doped body with high k dielectric to be gate insulator, (c) heavily doped body with high drain bias.

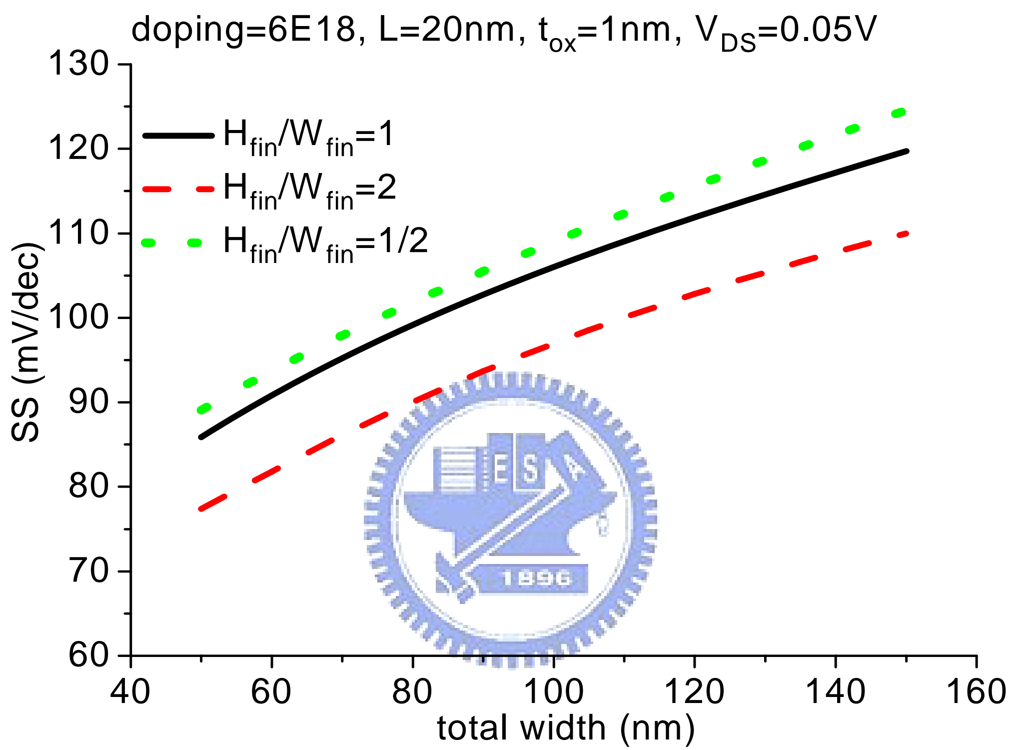


Fig. 4-3 Subthreshold swing of heavily doped multiple-gate devices versus total width in three different geometry devices.

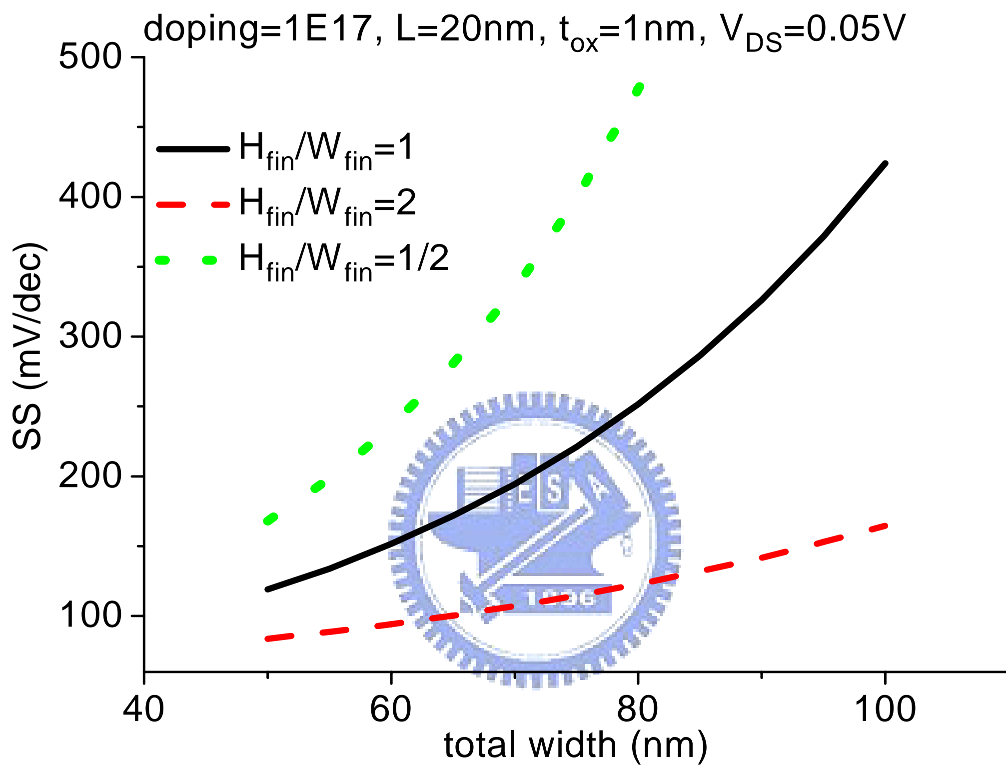
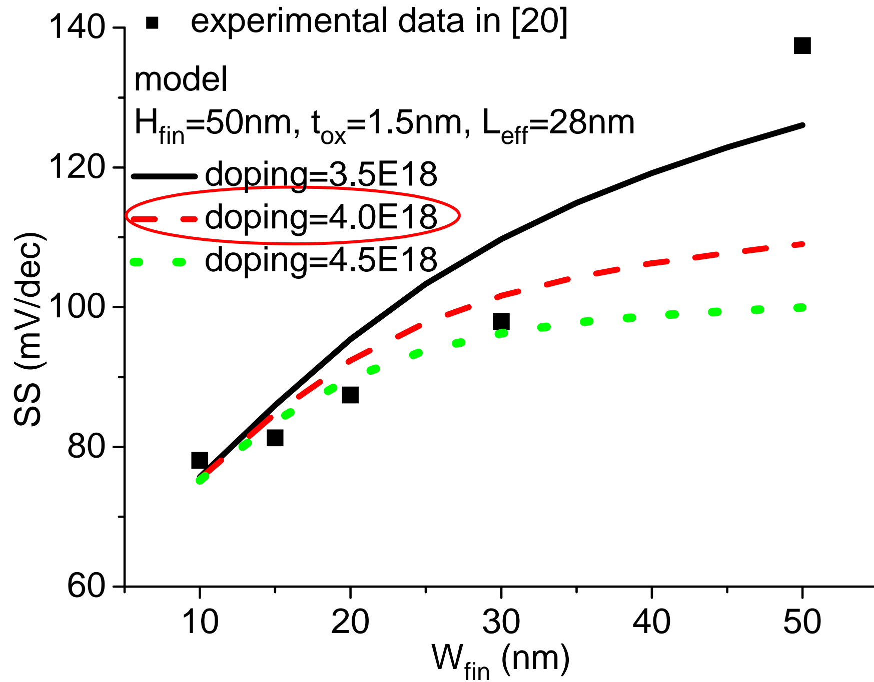
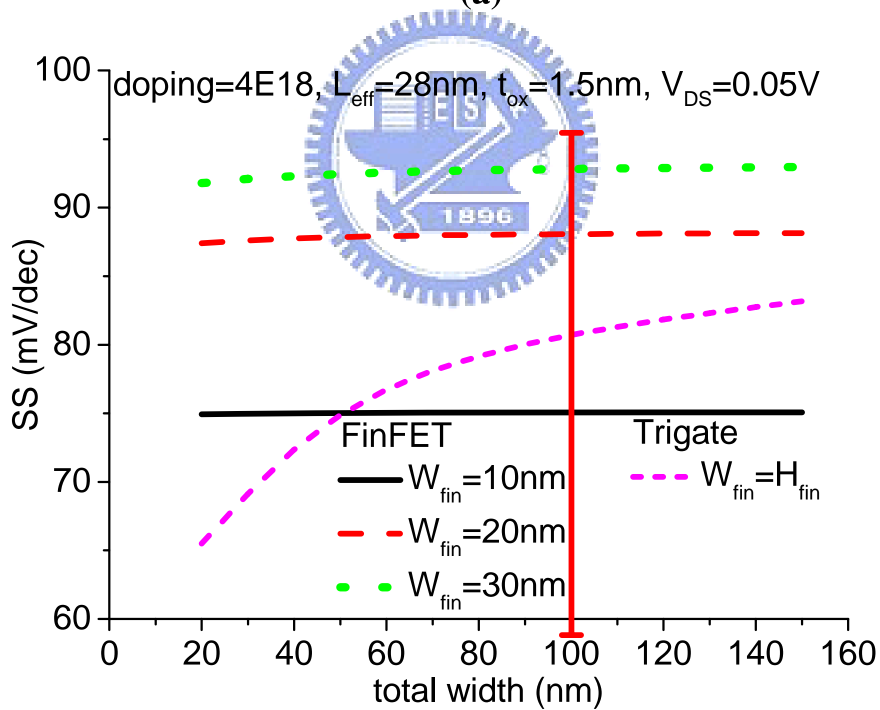


Fig. 4-4 Subthreshold swing of lightly doped multiple-gate devices versus total width in three different geometry devices.

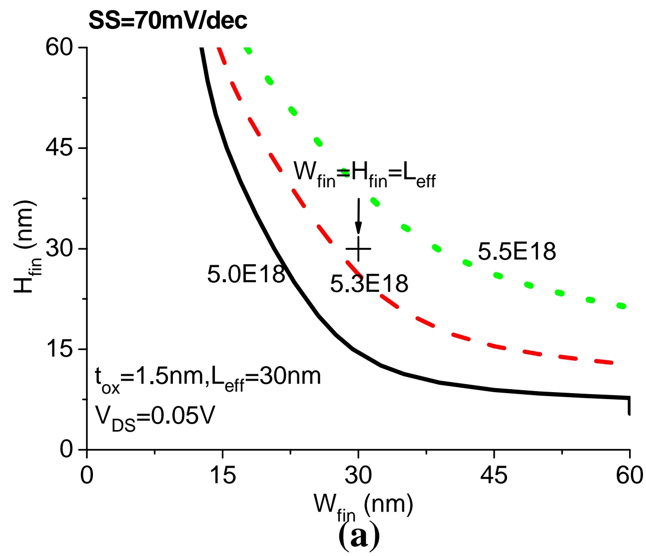


(a)

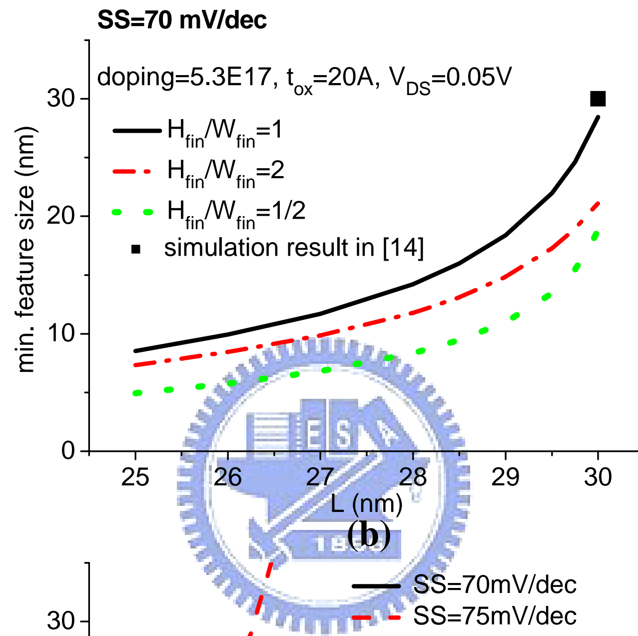


(b)

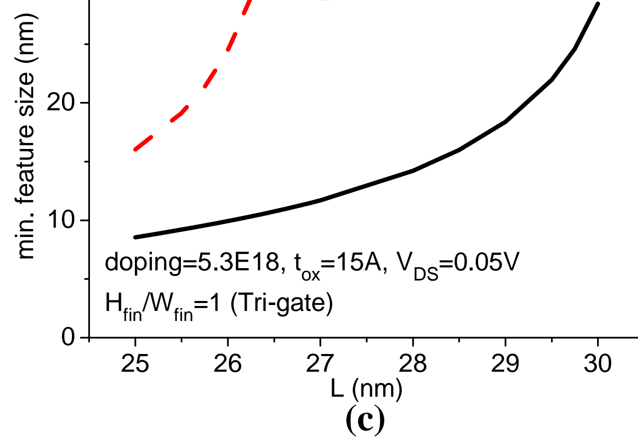
Fig. 4-5 (a) Comparison of fabrication data of [20] with our model, and (b) the comparison of subthreshold swing versus total width between FinFET and Tri-gate by using the parameters in (a).



(a)

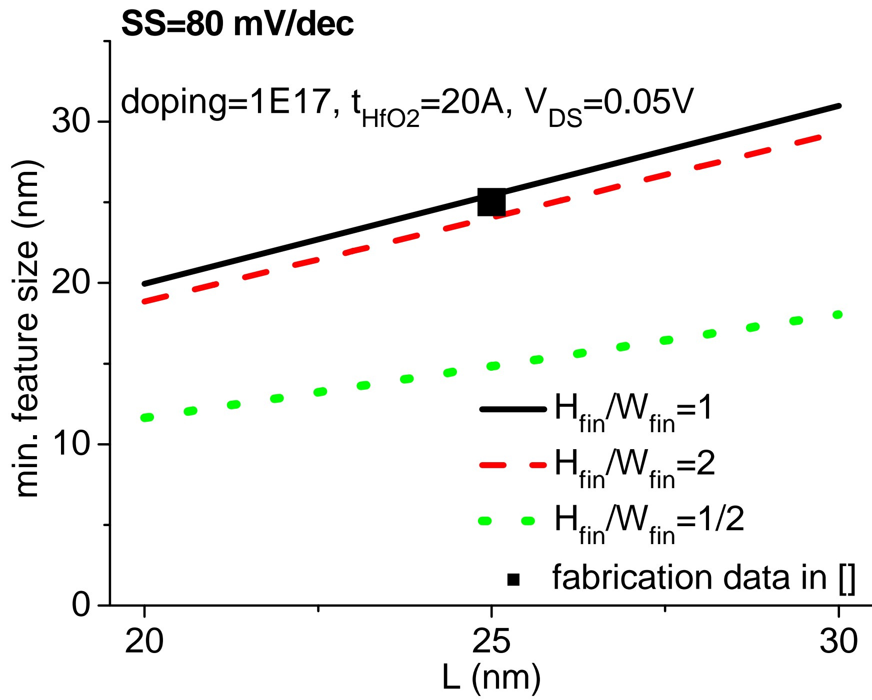


(b)

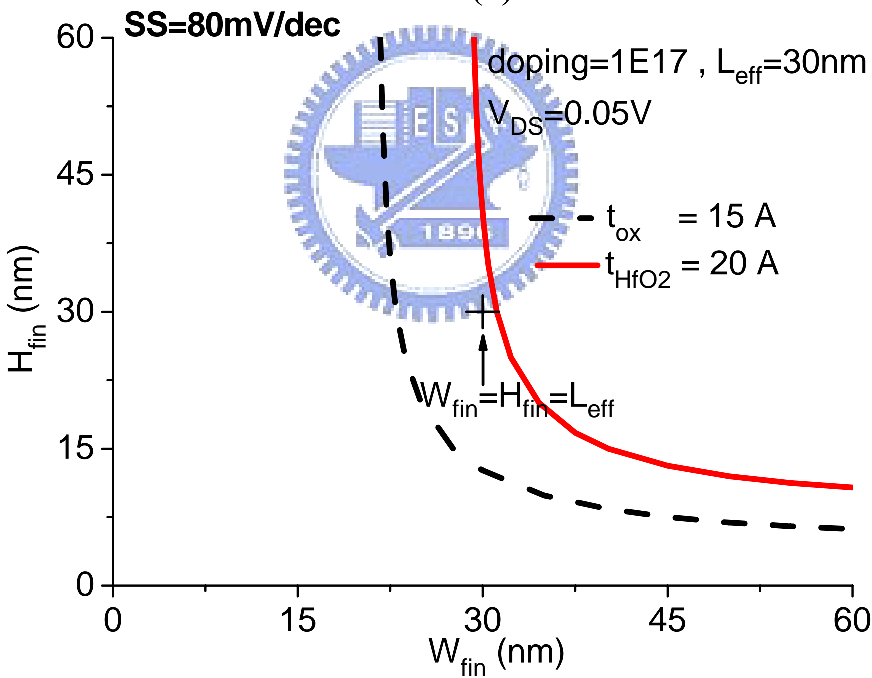


(c)

Fig. 4-6 (a) Contours of various doping concentration for the same subthreshold swing, (b) the comparison of minimum feature size versus channel length between FinFET, Tri-gate, and planar device by using the parameters in (a), and (c) a relaxed subthreshold swing criterion for Tri-gate in (b)and Tri-gate by using the parameters in (a).



(a)



(b)

Fig. 4-7 (a) Minimum feature size of three different geometry devices versus channel length in lightly doped body with high k dielectric, and (b) contours of various gate insulator for the same subthreshold swing compared with the Tri-gate condition (W_{fin}=H_{fin}=L) and Tri-gate by using the parameters in (a).

Chapter 5
Conclusions and Future Work

5.1 Conclusions

This thesis studies the design considerations in multiple-gate transistors, and the estimation is based on the subthreshold characteristics of the devices. By use of analytical solution of 3-D Poisson's equation, threshold voltage and subthreshold swing values can be obtained without time-consuming numerical simulation or device fabrication. Our model is verified by the device simulation and data in the literature.

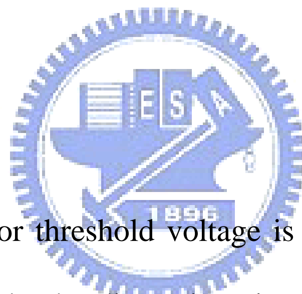
Our model includes both heavily doped and lightly doped cases, and the benchmarks in these two different cases are investigated. In heavily doped body, significant corner effect is observed in wide fin width devices. Once the device size is smaller, the corner region dominates the whole device and reduces the threshold voltage. This is responsible for the threshold voltage decreasing with fin width scaling and fin height scaling. Lightly doped body can eliminate corner effect, but the short channel characteristics degrade severely without the channel doping. Therefore, lightly doped body is not feasible unless high k dielectric is added to suppress short channel effect.

Good accuracy in high k dielectric is also observed in our model. The use of high k dielectric reduces the threshold voltage sensitivity to doping concentration, and the threshold voltage variation with doping concentration in heavily doped body is alleviated. Our model has confirmed that lightly doped Tri-gate with H_{fin}=W_{fin}=L is feasible with gate oxide replaced by high k dielectric.

We found that threshold voltage roll-off is more sensitive to W_{fin} scaling than to

H_{fin} scaling, and hence W_{fin} scaling benefits more than H_{fin} scaling in improving short channel characteristics. The sensitivity difference will be increased if geometry is the dominant factor in suppressing short channel effect. This inherent difference will influence the device geometry design. FinFET structure is more advantageous than Tri-gate if large I_{on} and short channel effect suppression are required simultaneously. The superiority of FinFET is proportional to sensitivity difference between H_{fin} scaling and W_{fin} scaling. Tri-gate structure is more scalable than FinFET in both heavily doped and lightly doped cases due to bigger minimum feature size allowed for given subthreshold swing. This is because high aspect ratio FinFET and low aspect ratio planar-like devices have inherent tighter fin width and fin height, respectively.

5.2 Future Work



In chapter 3, modeling for threshold voltage is verified with device simulation and good accuracy is achieved. The discussions in chapter 4 mainly concentrate on subthreshold characteristics of FinFET and Tri-gate. Another consideration in device design is threshold voltage sensitivity to process variation. The uniformity issue in realistic device fabrication becomes more and more important due to the ultra small device size nowadays. Therefore, the variation of fin width, height, channel length, and doping level will influence the threshold voltage value, and the immunity to process variation in multiple-gate structures is necessary to evaluate. In our model, threshold voltage fluctuation due to device geometry and doping concentration can be investigate, and will provide an insight in the manufacturability of FinFET and Tri-gate.

References

[1] J. P. Colinge, M. H. Gao, A. Romano, H. Maes, and C. Claeys, "Silicon-on-insulator Gate-all-around device," in *IEDM Tech. Dig.*, 1990, pp. 595-598.

[2] J. Kedzierski *et al*, "High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices," in *IEDM Tech. Dig.*, 2001, pp. 247-250.

[3] Y. K Choi, L. Chang, P. Ranade, J. S. Lee, D. Ha, S. Balasubramanian, A. Agarwal, M. Ameen, T. J. King, and J. Bokor, "FinFET process refinements for improved mobility and gate workfunction engineering," in *IEDM Tech. Dig.*, 2002, pp. 259-262.

[4] O. Faynot, G. Barna, R. Ritzenthaler, and P. Gidon, "Scaling of Multiple-Gate Fully Depleted SOI Transistors," in *Proc. Int. Conf. Solid State Devices and Materials*, Sept. 2004, pp. 764-765

[5] http://www.itrs.net/

[6] J. W. Yang and J. G. Fossum, "On the Feasibility of Nanoscale Triple-Gate CMOS Transistors," *IEEE Trans. Electron Devices,* Vol. 52, pp. 1159 - 1164, June 2005.

[7] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, and R. Chau, "Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering," in Symp. *VLSI Tech. Dig.*, June 2006,

[8] X. Liang, Y. Taur, "A 2-D Analytical Solution for SCEs in DG MOSFETs," *IEEE Trans. Electron Devices,* Vol. 51, pp. 1385 - 1391, August 2004.

[9] G. Pei, J. Kedzierski, P. Oldiges, M. Ieong, and E. C. Kan, "FinFET design

considerations based on 3-D simulation and analytical modeling," *IEEE Trans. Electron Devices,* Vol. 49, pp. 1411-1419, August 2002.

[10] D. S. Havaldar, G. Katti, N. DasGupta, and A. DasGupta, "Subthreshold current model of FinFETs based on analytical solution of 3-D Poisson's equation," *IEEE Trans. Electron Devices,* Vol. 53, pp. 737-742, April 2006.

[11] G. Katti, N. DasGupta, and A. DasGupta, "Threshold voltage model for mesa-isolated small geometry fully depleted SOI MOSFETs based on analytical solution of 3-D Poisson's equation," *IEEE Trans. Electron Devices*, Vol. 51, no. 7, pp. 1169-1177, Jul. 2004.

[12] T. N. Nguyen, "Small-geometry MOS transistors: physics and modeling of surface- and buried-channel MOSFETs," Ph.D. dissertation, Stanford Univ., Stanford, CA, 1984.

[13] *ISE TCAD Release 10.0* Manual

[14] B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalierous, T. Linton, R. Rios, and R. Chau, "Tri-gate fully-depleted CMOS transistors: Fabrication, design and layout," in *Symp. VLSI Tech. Dig.*, June. 2003, pp. 133-134

[15] J. G. Fossum, J. Yang, and V. P. Trivedi, "Suppression of corner effects in triple-gate MOSFETs," *IEEE Electron Device Lett.,* Vol. 24, pp. 745-747, December 2003.

[16] Q. Chien, E. M. Harrell, II, and J. D. Meindl, "A Physical Short-Channel Threshold Voltage Model for Undoped Symmetric Double-Gate MOSFETs," *IEEE Trans. Electron Devices*, Vol. 50, no. 7, pp. 1631-1637, Jul. 2003.

[17] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, New York, NY, 1998.

[18] M. C. Lemme, T. Mollenhauer, W. Henschel, T. Wahlbrink, M. Baus, O. Winkler, R. Granzner, F. Schwierz, B. Spangenberg and H. Kurz, "Subthreshold behavior of triple-gate MOSFETs on SOI material," *Solid-State Electronics,* Volume 48, Issue 4, April 2004, pp. 529-534.

[19] A. Dixit, K. G. Anil, A.Mercha, N. Collaert, S. Brus, O. Richard1, R. Rooyackers, M. Goodwin, M. Jurczak, and K. DeMeyer, "Towards Optimally Shaped Fins in P-Channel Tri-Gate FETs: Can Fin Height Be Reduced Further?," in *IEEE VLSI-TSA International Symposium*, April 2005, pp. 112-113.

[20] K. Okano, T. Izumida, H. Kawasaki, A. Kaneko, A. Yagishita, T. Kanemura, M. Kondo, S. Ito, N. Aoki, K. Miyano, T. Ono, K. Yahashi, K. Iwade, T. Kubota, T. Matsushita, I. Mizushima, S. Inaba, K. Ishimaru, K. Suguro, K. Eguchi, Y. Tsunashima and H. Ishiuchi, "Process Integration Technology and Device Characteristics of CMOS FinFET on Bulk Silicon Substrate with sub-10 nm Fin Width and 20 nm Gate Length." in *IEDM Tech. Dig.*, 2005, pp. 247-250.

[21] R. Chau, B. Doyle, J. Kavalieros, D. Barlage, A. Murthy, M. Doczy, R. Rios, T. Linton, R. Arghavani, B. Jin, S. Datta, and S. Hareland, "Advanced depleted-substrate transistors: Single-gate, double-gate, and tri-gate," in *Proc. Int. Conf. Solid State Devices and Materials*, Sept. 2002, pp. 68-69

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碩士論文題目：

多重閘極絕緣矽金氧半場效電晶體的微縮分析

Investigation of Scaling for Multiple-Gate SOI MOSFETs Using Analytical Solution of 3-D Poisson's Equation