國立交通大學

電子工程學系 電子研究所

博 士 論 文

前瞻非揮發性奈米點記憶體元件之製作與特性研究

Fabrication and Electrical Characterization of Advanced Nanocrystals Nonvolatile Memories

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研 究 生：陳緯仁　　Student：Wei-Ren Chen

指導教授：張俊彥 院士　　Advisor：Dr. Chun-Yen Chang

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摘 要

目前非揮發性記憶體在元件尺寸持續的微縮下，其需求為高密度記憶單元、低功率損耗、快速讀寫操作以及良好的可靠度(Reliability)。然而傳統浮動閘極(Floating gate)記憶體在操作過程中，穿遂氧化層產生漏電路徑會造成所有儲存電荷流失回到矽基版，隨著尺寸微縮這種情況會更糟，所以在資料保存時間(Retention)和耐操度(Endurance)的考量下，微縮穿遂氧化層的厚度是非常困難的。具非揮發性奈米點記憶體及 SONOS 記憶體被提出並希望可取代傳統浮動閘極記憶體，由於彼此分離的儲存點作為儲存中心，所以上述兩者可以有效改善小尺寸記憶體元件多次讀寫操作下的資料儲存能力。

在本論文中，主要提出三種不同性質的奈米點(鍺、矽化鎳與錳矽氧化物奈米點)材料來克服傳統非揮發性記憶體在微縮過程中會遭遇到的困難，我們首先提出一種矽鍺氧薄膜的堆疊結構作為鍺奈米點的自我析出層(Self-assembled layer)，並應用在奈米點非揮發性記憶體上。在室溫環境中，利用濺鍍(Sputtering)矽鍺($Si_{0.5}Ge_{0.5}$)混合靶材的方式來形成電荷儲存層，同時加入氫氣及氧氣一起共鍍，此方式可以成功的將氧氣原子摻入至矽鍺中形成矽鍺氧三元結構的薄膜，另外，在我們的實驗中，我們也發現在氮氣熱退火之前先疊加上一層氧化矽作為阻擋鍺揮發的阻擋層，此為使用矽鍺氧薄膜作為電荷儲存層的一個關鍵步驟。之後我們再利用氧、矽與鍺之間不同氧化競爭的現象，經由快速熱退火製成來形成均

勻且高密度(~$10^{12}cm^{-2}$)的鍺奈米點埋藏於氧化層中。此鍺奈米點製程相對於傳統鍺奈米點製作，可以有效地防止鍺被過度氧化並且降低電荷儲存效率。同樣地，我們運用類似的鍺奈米點形成機制，在濺鍍的過程中將氧氣置換成氮氣，利用同樣的方式製作鍺奈米點且奈米點可以在析出過程被包覆在氮化矽(SiN_x)的結構中，其記憶窗口比先前的鍺奈米點埋藏在氧化矽結構還顯著，此乃因為鍺奈米點埋在氮化矽為主的電荷儲存層裡，會與奈米點周圍的介電層產生額外的電荷儲存中心，進而增加記憶體整體效能，另外，我們比較這兩種結構的鍺奈米點記憶體，由於氮化矽能使儲存電荷均勻分佈於儲存層以降低庫倫斥力效應，所以在本研究中不論在電荷儲存能力與可靠度上，埋藏在氮化矽的鍺奈米點記憶體都展現較好的記憶體特性。

近年來已經發展了許多方法來形成奈米點記憶體，一般而言，大多數的方法都需要長時間且高溫的熱退火製程，這個步驟會影響現階段半導體製程中的熱預算和產能。因此在本論文中，我們使用一個簡單、低溫的製程方法來形成鎳氧矽化物(Ni-O-Si)和鎳矽氮化物(Ni-Si-N)奈米點，並將其應用於非揮發性記憶體元件上。我們一樣在氬氣和氧氣(Ar/O_2)的環境中濺鍍混合鈀材 $Ni_{0.3}Si_{0.7}$ 形成氧化矽(SiO_x)包覆著鎳氧矽化物(Ni-O-Si)的非揮發性記憶體結構，我們認為在此濺鍍過程中會形成奈米點結構，氧氣扮演一個不可或缺的角色，可以簡單並均勻地形成高密度(~10^{12} cm^{-2})的奈米點分佈。我們同時也提出室溫下在氬氣和氮氣(Ar/N_2)的環境中濺鍍混合鈀材 $Ni_{0.3}Si_{0.7}$ 來形成鎳矽氮化物(Ni-Si-N)奈米點，結果也可發現高密度鎳矽氮化物奈米點被包覆在氮化矽(SiN_x)中，並且擁有更好的儲存能力。因此我們利用這些元素之間的不同吉布斯自由能(Gibbs free energy)來產生一個內部競爭機制，可以在較低溫的環境中形成所謂的低溫化的非揮發性金屬奈米點記憶體。

我們進一步利用一個500°C~600°C的快速熱退火製程，藉由鎳與矽的化合反應來增進奈米點的結晶性(Crystallization)，矽化鎳(NiSi)金屬奈米點會因此形成並且擁有較高的態位密度(Density of state)來儲存電荷並增加記憶窗口與儲存電荷穩定性；因為熱退火處理也可以改善氮化矽本身的品質與減少奈米點周圍氮化矽中的淺層缺陷(漏電路徑)，記憶體的可靠度同時也被有效率地改善。因此我們成功地製作出一個具有SONOS性質的金屬奈米點記憶體，此外，根據奈米點埋

藏於不同介電層中的電場結構模擬，與氧化矽包覆的金屬奈米點相較之下，由於不同介電質中具有不同的電場分佈，氮化矽包覆奈米點作為電荷儲存層有較佳的可靠度表現。最後我們製作多層的矽化鎳奈米點記憶體結構並探討其特性，發現多層奈米點比單層奈米點不僅在室溫下且在高溫時也擁有較好的電荷儲存能力和保存能力，此乃因為多層奈米點的第一與第二層因尺寸所產生的量子侷限效應(Quantum confinement effect)，可以加以阻擋第三層的主要儲除電荷的流失路徑。

再者，針對介電質奈米點記憶體，我們也使用濺鍍系統形成錳矽氧化物($MnSiO_x$)奈米點，且進一步利用X光光電能譜(XPS)鑑別錳矽氧化物奈米點的組成以及能隙與能帶圖的建立。並藉由量測電流密度與溫度的關係，使用缺陷輔助穿隧模型來萃取錳矽氧化物的缺陷深度與密度，進而可以發覺氧原子的摻雜濃度會影響缺陷深度，使得電荷保持能力會有所差別。我們也製作雙層錳矽氧化物($MnSiO_x$)奈米點記憶體結構並探討其特性，可以發覺其比單層的介電層奈米點有較好的電荷儲存特性與保持能力，此乃因為介電層奈米點的電荷儲存方式是藉由自身的缺陷捕獲所致，所以已被捕獲的電荷必須先克服介電質奈米點的缺陷能障，方能逃脫出奈米點並流失掉。最後，我們所提出的奈米點結構與製造技術都可以應用於非揮性奈米點記憶體的製程技術同時也適用於現階段積體電路製程。

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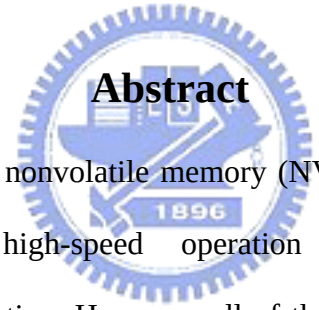
Student: Wei-Ren Chen Advisors: Prof. Chun-Yen Chang

Department of Electronics Engineering and Institute of Electronics

National Chiao Tung University, Hsinchu, Taiwan



Abstract

Current requirements of nonvolatile memory (NVM) are the high density cells, low-power consumption, high-speed operation and good reliability for next-generation NVM application. However, all of the charges stored in the floating gate will leak into the substrate if the tunnel oxide has a leakage path in the conventional NVM during endurance test. Therefore, the tunnel oxide thickness is difficult to scale down in terms of charge retention and endurance characteristics. Nanocrystals (NCs) NVMs are one of promising candidates to substitute for conventional floating gate memory, because the discrete storage nodes as the charge storage media have been effectively improve data retention for the scaling down device.

In this thesis, we propose three kinds of NCs with different properties (Ge, NiSi and MnSiO NCs) to overcome the limitation of conventional NVMs during the scaling down process. First, we proposed a SiGeO stacking structure serving as Ge

NCs self-assembled layer for application of NCs NVMs. We successfully incorporated the oxygen atoms into SiGe layer to form a SiGeO ternary film by sputtering a commixed $Si_{0.5}Ge_{0.5}$ target in an Ar/O_2 ambiance at room temperature. In this work, we fond out that pre-annealing-capping oxide (PACO) is a critical step in our experimental process, and the charge storage layer can be used the different oxidized competition mechanism between Si and Ge to form Ge NCs embedded in oxide. Hence, a uniform and high density ($\sim 10^{12} cm^{-2}$) of Ge NCs was fabricated after a rapid thermal annealing (RTA) process. Our propose technique compared with traditional Ge NCs process can be efficiently to prevent the over-oxidation phenomenon of Ge NCs which reduces the charge trapping ability. Furthermore, we also used this similar method that oxygen was replaced by nitrogen to form the Ge NCs embedded in SiN_x structure. The memory window for the stacked structure with Ge NCs embedded in SiN_x layer was larger than Ge NCs embedded in SiO_x layer, due to the extra charge trapping centers generated from the surrounding dielectric of Ge NCs. To compare these Ge NCs structures, we found that the Ge NCs embedded in nitride had better charge storage ability and reliability for NVM characteristics, because the nitride layer can uniformly distribute the stored charge to reduce Coulomb repulsive force effect under retention test.

In recent years, most methods of NCs fabrication generally need the thermal treatment with high temperature and long duration. This procedure will influence thermal budget and throughput for the current manufacture technology of semiconductor industries. Hence, an ease and low temperature fabrication technique of Ni-O-Si and Ni-Si-N NCs was demonstrated for NVM application in this thesis. The NVM structure of Ni-O-Si NCs embedded in the SiO_x layer was fabricated by sputtering a commixed target ($Ni_{0.3}Si_{0.7}$) in an Ar/O_2 environment at room temperature. It can be considered that the oxygen plays a critical role during sputter process for the

NC formation. In addition, a high density (~10^{12} cm^{-2}) NCs also can be simple and uniform to be fabricated in our study. We also proposed a formation of Ni-Si-N NCs by replacing O_2 by N_2 environment during the sputtering process. It was also found that a high density Ni-Si-N NCs was embedded in the silicon nitride (SiN_x) which presented larger memory effect. Therefore, by using this internal competition mechanism of charge trapping layer for these elements (Ni, Si, and O/N), we can obtain a metallic NCs NVM with low temperature process.

A RTA process with temperatures about 500 and 600 °C at short duration was further used to improve the crystalline quality of metallic NCs and its memory reliability. Thermal treatment can efficiently reduce the defects (leakage path) in the SiN_x which surrounds the nanocrystal. The charge storage layer of NCs embedded in SiN_x shows larger memory window and better reliability over NCs embedded in SiO_x, due to different distributions of electronic field in the NC and surrounding dielectric by the simulation results. In addition, multi-layer NiSi NCs NVM structure had better charge storage and retention over than single-layer metal nanocrystals under high temperature test, because of the first and second layer of multi-layer with Quantum confinement effect depended by the NC size.

For dielectric NCs NVMs, we also used the sputter system to fabricate the manganese silicate ($MnSiO_x$) NCs. The XPS results of charge trapping layer can be identified the chemical state of NCs and built the energy band diagram of our produced $MnSiO_x$ thin film. Moreover, by the relationship of current density with temperature, the trap assisted tunneling model can be used to extract the charge trapping level and density of $MnSiO_x$. In the experiment results, the oxygen doping concentration will affect the trap level positions and also influence the retention presentations for the reliability test. Moreover, double layer $MnSiO_x$ NCs NVM also was fabricated and discussed its NVM effect. The double layer was better trapping

and keeping charges ability than single layer because the trapped charges must overcome the trap barrier and then escape from NCs due to the trapping mode of dielectric NCs.

Key words: **Nanocrystal, SONOS type, Nonvolatile memory, Ge, NiSi, MnSiO, multi layer, double layer.**

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秋分

緯仁

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Chapter 1

Introduction

1.1 Overview of Nonvolatile Memory

Recently, the portable electronic products can provide the convenient life for human. These products all need the flash memories which are considered as a technology driver for next-generation semiconductor industry. It can be classified into two major markets: code storage and data storage applications. NOR type flash memory has been targeted at code storage application, such as PC bios and DVD player [1.1]. NAND type flash memory is most suitable for the code storage application [1.2], such as PDA, memory cards, MP3 audio players, digital cameras, and USB flash personal disc etc. These products all are based on flash memories that are nonvolatile and can keep stored information when the power supply is switched off. Flash memory also has exhibited several advantages, such as the ability to be electrical programmed and fast simultaneous block electrical erased in a single-cell, smallest cell size to achieve a highest chip density, and good flexibility [1.3, 1.4]. The flash memory fabrication process can be compatible with the current CMOS process and be a suitable solution for the embedded memory application. Flash memories are easily scaled down to replace for EPROMs (Erasable Programmable Read Only Memory) and EEPROMs (Electrically Erasable Programmable Read Only Memory). As these critical advantages flash memory possesses, it has become the mainstream nonvolatile memory device in last few decades.

In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory (or flash memory) at Bell Labs [1.5]. A standard conventional FG device structure is shown in Fig. 1-1. The structure is basic on a Metal Oxide

Semiconductor Field Effect Transistor (MOSFET) with a modified stacking gate which composed by control gate, dielectric, floating gate and dielectric as a sandwich structure. Charges injected in the FG are maintained there, allowing the difference between threshold voltages of the cell transistor for nonvolatile memory (NVM) application.

Nowadays, NVM devices are moving toward high density memory array, low cost, low power consumption, high-speed operation, and good reliability. However, the conventional FG NVMs have their limitation which the most prominent one is the limited potential for the continued scaling of device structure. This scaling limitation stems from the extreme requirements of tunnel oxide layer. The tunnel oxide must be thin enough to allow the charges to transfer fast to the FG. According to the 2007 International Technology Roadmap (ITRS) of Semiconductor flash memory [1.6], the FG memory devices have to reduce the tunnel oxide thickness to 6-7 nm in 2010s, as shown in Fig. 1-2. Moreover, the scaling of the gate stack and operation voltages is often related to each other. A tunnel oxide thickness of more than 8 nm is currently used in the commercial flash memory chip to meet the ten years data retention time requirement. If the tunnel oxide were to be scaled below 2 nm, the operation voltage could be reduced from more than 10 V to below 4 V [1.7]. Unfortunately, the retention time would also be reduced, from 10 years to several seconds. The tunnel oxide needs to provide superior isolation under retention, endurance, and disturbed conditions in order to guarantee the data integrity for 10 years. Hence, for faster operation speed, thin tunnel oxide is desirable. Nevertheless, it is also desirable to increase the thickness of tunnel oxide for the better isolation and reliability. There is a trade-off between speed and reliability for the optimum tunnel oxide thickness [1.8].

In addition, for the conventional FG memory, if there are several defects generated in the tunnel oxide after the endurance operated steps, these defect might

induce a leakage path that will make all charges stored in the FG leak back to the channel. To alleviate the trade-off of tunnel oxide design for FG memory devices, memory-cell structures employing discrete traps as charge storage media have been proposed in the past few years. Unlike conventional continuous FG, charges stored in the discrete nodes cannot easily redistribute amongst themselves. Therefore, only a relatively small number of nodes near the oxide defects will be affected. Local charge storages in the discrete nodes can enables more aggressive scaling of tunnel oxide by relieving the total charge loss concern. Therefore, two suggestions, poly-Si/oxide/nitride/oxide/Si (SONOS) [1.7-1.9] and nanocrystal nonvolatile memory devices [1.10-1.12] are proposed to overcome this oxide quality limit of the conventional FG structure. Hence the tunnel oxide thickness can be reduced to allow faster programming and lower voltage operation.

1.1.1 SONOS Nonvolatile Memory Devices

The first nitride-base devices is metal-gate nitride device MNOS (Metal/Nitride/Oxide/Silicon) which was reported in 1967s by Wegener et al. [1.13]. However, it is well known that silicon nitride film contains much carrier traps which cause a threshold voltage shift. Then the silicon nitride trap-based devices are widely studied for charge storage device application in the early 1970s. Fig. 1-3 illustrates the progression of device cross section, which has led to the present SONOS device structure. Initial device structures in the early 1970s were p-channel metal-nitride-oxide-silicon (MNOS) structures with aluminum gate electrodes and thick (45nm) silicon nitride charge storage layers. Write/erase voltages were typically about 25-30 V. In the late 1970s and early 1980s, the NVM devices moved to n-channel SNOS devices with write/erase voltages of 14-18 V. In the late 1980s and early 1990s, n- and p-channel SONOS devices emerged with write/erase voltages of

5-12 V. The ONO triple dielectric structure has some advantages, such as (1) lower programming voltage since the blocking action of the top oxide removes any limitation on the reduction of the nitride thickness; (2) charge injection from and to the gate electrode is minimized for both gate polarities, particularly for hole injection; (3) improved memory retention since there is a minimal loss of charge for the gate electrode.

The SONOS (poly-Silicon-Oxide-Nitride-Oxide-Silicon) memory devices, as shown in Fig. 1-4, have attracted a lot of attention due to its advantages over the traditional FG flash device. These include reduced process complexity, lower voltage operation, high speed operation, improved cycling endurance, and elimination of drain-induced turn-on [1.14-1.15]. The main difference between FG and SONOS structure is the method of charge storage. Conventional FG structure charges carriers in the continuous conductive polysilicon. In contrast with conventional FG structure, SONOS structure charges carriers in the physical discrete traps of the silicon nitride dielectric. Typical traps have a density of the order 10^{18}-10^{19} cm^{-3} according to the calculation of Yang et al. [1.16] and can store both electrons and holes injected from the channel. The charges stored in the silicon nitride cannot move easily, hence the SONOS can tolerate the defects in the tunnel oxide induced the leakage path. Therefore, the SONOS memory device has better endurance than the conventional FG memory.

The SONOS memory devices still face challenge in the future for high density NVM application, which requires low voltage (< 5V), low power consumption, long-term retention, and superior endurance. Various approaches have been proposed for improving the SONOS performance and reliability. Chen et al. demonstrate a Si_3N_4 bandgap engineering (BE) control method for better endurance and retention. A nitride with varied relative Si/N ratio throughout the film has increased the

charge-trapping efficiency significantly [1.17].

In recent research, high-k dielectric materials were proposed to replace the silicon nitride film as the charge trapping layer, such as HfAlO and Al_2O_3. Tan et al. showed that over-erase phenomenon in SONOS memory structures can be minimized by replacing silicon nitride with HfO_2 as the charge storage layer. The charge retention and endurance performance is improved by the addition of 10% Al_2O_3 in HfO_2 to form HfAlO thin film served as charge trapping layer, while maintaining the over-erase resistance of HfO_2 [1.18]. She et al. demonstrates that high-quality nitride is applied as the tunnel dielectric for a SONOS-type memory device. To compare control devices with SiO_2 tunnel dielectric, faster programming speed and better retention time are achieved under a low programming voltage [1.19]. Lee et al. present a device structure of $SiO_2/SiN/Al_2O_3$ (SANOS) with the TaN metal gate. It is demonstrated that the use of TaN metal gate can block electron current through Al_2O_3 layer more efficiently than a conventional polysilicon gate, resulting in faster program/erase speed and significant decrease of the saturation level of the erase V_T [1.20].

Chen et al. studies a polycrystalline silicon thin-film transistor (poly-Si TFT) with oxide/nitride/oxide (ONO) stack gate dielectrics and multiple nano-wire (NW) channels for the applications of both nonvolatile SONOS memory and switch transistor [1.21]. The proposed NW SONOS-TFT exhibits superior memory device characteristics with high program/erase efficiency and stable retention characteristics at high temperature. Such SONOS-TFT is thereby highly promising to apply for the future system-on-panel (SOP) display applications.

New device structures are also indispensable in making flash memory more scalable. Since SONOS flash memory offers a thinner gate stack than floating gate flash memory, and a FinFET structure controls the short channel effect much better

than a bulk structure. It has been demonstrated that the FinFET SONOS flash memory devices with a much smaller cell size can provide both excellent performance and reliability. Therefore, FinFET SONOS memories have also potential to become the candidates of the next generation flash memories [1.22-1.13].

1.1.2 Nanocrystal Nonvolatile Memory Devices

Nanocrystal nonvolatile memories are one particular implementation of storing charge by dielectric surrounding with nanocrystals, and were first introduced in the early 1990s by IBM researchers who proposed flash memory with a granular floating gate made from silicon nanocrystals [1.24]. The name nanocrystal referred to a crystalline structure with a nanoscale dimension. Fig. 1-5 illustrates a typical nanocrystal NVM device structure and it is observed that the nanocrystals are separated from each other within the gate dielectric. Its electronic properties seem more similar to an atom or molecule rather than the bulk crystal. In the nanocrystal NVM device, the charges were charged in the isolated nanocrystals instead of the continuous FG polysilicon layer. Each nanocrystal will typically store only a handful of electrons and the charges stored in these dots collectively control the channel conductivity of the memory transistor.

Nanocrystal-based NVM devices have recently received much attention due to their potential to overcome the limitations of conventional FG flash memory for the scaling down tunnel oxide process. Using nanocrystals as charge storage media offers several advantages, the main one being the potential to use thinner tunnel oxide (< 5 nm) without sacrificing non-volatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to reduce the operating voltage and speed. This claim of improved scalability results from the local charge storage in discrete nodes, which makes the storage more fault-tolerant and immune to the leakage caused

by localized oxide defects. Further, the lateral charge migration effect between nanocrystals can be suppressed by the strongly isolation of surrounded dielectric. There are other important advantages except the above-mentioned benefits. First, nanocrystal memories use a more simplified fabrication process as compared to conventional stacked-gate FG NVMs by avoiding the fabrication complications and costs of a dual-poly process. Second, due to the absence of drain with FG coupling, nanocrystal memories suffer less from drain-induced-barrier-lowering (DIBL). One way to exploit this advantage is to use a higher drain bias during the read operation and to improve memory access time [1.25]. Hence, nanocrystals NVMs are allowed the use of shorter channel lengths to achieve the high density cell. Finally, nanocrystal memories are characterized by excellent immunity to stress induced leakage current (SILC) and oxide defects due to the distributed nature of the charge storage in the charge trapping layer. Research in this regime has focused on the development of fabrication processes, nanocrystal materials and the integration of nanocrystal-based storage layers in actual memory devices.

A nanocrystal NVM fabrication requires a perfect control of four main parameters: (1) the tunnel oxide thickness, (2) the nanocrystal density, (3) the nanocrystal size, and (4) the control oxide thickness. An important consideration is the average size and distributable density of nanocrystals. Larger-size nanocrystal array provides higher programming/erasing (P/E) efficient due to small quantum confinement and coulomb blockade effects. However, it is desirable to reduce the nanocrystal size leading to the high density on the channel for a uniform devices array. Therefore, there is a trade-off in selecting the nanocrystal size. A typical target is a density of at least 10^{11}-10^{12} cm^{-2}, and requires nanocrystal size of 5-10 nm. Moreover, good process control is needed with regards to such nanocrystal features as: planar nanocrystal layer; inter-nanocrystal interaction (lateral isolation); and nanocrystal

shape. We prefer that the fabrication processes are simple and compatible with the standard semiconductor equipment.

Currently, the nanocrystals NVMs can be classified three major categories by the materials: (1) semiconducting, (2) metallic and (3) high-k dielectric nanocrystals. Figure 1-6 shows the energy band diagrams of (a) Ge, (b) Ni and (c) HfO_2 nanocrystals nonvolatile memories. In this thesis, the authors will intro the developments and advantages of three kinds of nanocrystals.

A. Semiconducting Nanocrystal Memories

After the first proposal of a memory transistor using silicon nanocrystals as floating gates. In order to improve the data retention in NVM, double layer Si nanocrystals memory has been investigated [1.26]. It seems interesting to use Ge nanocrystals rather than Si nanocrystals because of its smaller band gap (~ 0.6 eV), as shown in Fig. 1-6(a). Indeed King and Hu et al. have recently demonstrated the superior memory properties of Ge based nanocrystal memories over those based on Si [1.27]. Recently, germanium/silicon (Ge/Si) heterojunction nanocrystals have been reported to possess superior charge retention capability than single Ge or Si nanocrystals. This is due to the fact that Ge has a smaller band gap than Si, and thus by introducing a Si interface around the Ge nanocrystal, it can create an additional barrier height between the Ge and Si interface to prevent the stored charges to leak out of the nanocrystals [1.28, 1.29]. However, semiconductor nanocrystal memory may not be the ultimate solution to nonvolatile memory scaling, although it still attracts a lot of attention now.

B. Metallic Nanocrystal Memories

In optimizing nanocrystal NVM devices, the ideal goal is to achieve the fast write/erase of DRAM and the long retention time of Flash memories simultaneously. For this purpose, we must create an asymmetry in charge transport through the gate

dielectric to maximize the $I_{G,\ Write/Erase}/\ I_{G,\ Retention}$ ratio. One approach for achieving this goal is to engineer the depth of the potential well at the storage nodes, thus creating a large energy band offset between the Si substrate and the storage nodes for programming speed and retention operation. This can be achieved if the storage nodes are made of metal nanocrystals by engineering the metal work function. The major advantages of metal nanocrystals over semiconductor nanocrystals include (1) higher density of states around the Fermi level, (2) scalability for the nanocrystal size, (3) a wide range of available work functions, and (4) smaller energy perturbation due to carrier confinement [1.30]. In addition, an electrostatic modeling from both analytical formulation and numerical simulation is demonstrated that the metal nanocrystals will significantly enhance the electric field between the nanocrystal and the sensing channel set up by the control gate bias, and hence can achieve much higher efficiency in low-voltage P/E [1.31].

Toward better NVM device performance and reliability, numerous attempts have been made using metal nanocrystals. Liu et al. reported the growth of Au, Pt, and Ag nanocrystals on SiO_2 using an e-beam deposition method [1.32]. Lee et al. proposed a NVM structure using the Ni nanocrystals and high-*k* dielectrics [1.33]. Chen et al. present the stacked Ni silicide nanocrystal memory was fabricated by sputtering a commixed target followed by a low temperature RTO process [1.34]. W nanocrystals on atomic-layer-deposited $HfAlO/Al_2O_3$ tunnel oxide were presented for application in a memory device [1.35]. Using W nanocrystal double layers embedded in HfAlO to enhancement of memory window was demonstrated from the short channel devices down to 100nm [1.36]. Tang et al. demonstrate that a chaperon in protein lattice can be used as a template to assemble PbSe and Co nanocrystal arrays for Flash memory fabrication. This provides a new approach to achieve a high density and good distribution uniformity nanocrystal array [1.38].

C. High-K dielectric Nanocrystal Memories

The high-k dielectric nanocrystal nonvolatile memories (HfO_2 and CeO_2 nanocrystals) are first proposed by C. H. Chien et al. [1.39, 1.40]. C. H. Chien et al. reported a method of co-sputtering Hf and Si in oxygen followed with high-temperature annealing to form the high-K dielectric nanocrystals for SONOS-type memory devices. These devices are not only like SONOS-type nonvolatile memories but also can restrain the stored charge lateral migration effect. Hence, the performance of high-k dielectric nanocrystals for 2-bits operation is better than SONOS-type memory devices.

In the future, the primary drivers behind nanocrystal memories are the potential to scale the tunnel oxide thickness, resulting in lower operating voltages, and the simplicity of a single poly-silicon process. But there are still challenges await nanocrystal memories in the long road to commercialization. Nanocrystal memories have yet to deliver on most of their promises. In reality, part of the voltage gain is offset because of the poor control gate coupling. For fabrication processes, it is hard to control the uniformity of the nanocrystal size and their physical locations in the channel. It is not a surprise that nanocrystal memories exhibit large device-to-device variation. Moreover, it has yet to be demonstrated that both the nominal and the statistical retention behavior are sufficient to meet true non-volatility requirements. Although single-dot memories have been demonstrated [1.41,1.42], but a more fundamental understanding of the scaling limits of nanocrystal memories is necessary, concentrating especially on the aspect of controlling channel conductance when relying on only a few discrete charge centers [1.43, 1-44]. Finally, in order for that to happen, their claimed benefits will need to be more unambiguously substantiated, and a more appealing bundle of memory features will have to be demonstrated.

1.2 Motivation

The Semiconductor Industry Association (SIA) International Technology Roadmap for Semiconductors (ITRS) indicates the difficult challenge, beyond the year 2007, for nonvolatile semiconductor memories is to achieve reliable, low-power, low-voltage performance [1.6]. For nonvolatile flash memories, two limitations encountered at the present time are: (1) the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer. In order to get balance between program/erase speed and retention time, there is a trade-off between speed and reliability to get the optimal tunnel oxide thickness; (2) the quality and strength of tunnel oxide (or tunnel dielectric) after plenty of program/erase cycles. Once a leaky path has been created in tunnel oxide, all the charges stored in the floating gate will be lost. Therefore, two suggestions, the SONOS and the nanocrystal nonvolatile memory devices, are proposed to overcome this oxide quality limit of the conventional FG structure. These technologies replace the floating gate structure with a great number of charge-storage nodes in the dielectric or in the nanocrystal. Unlike the floating gate, the local leaky path will not cause the fatal loss of information for the nanocrystal nonvolatile memory device.

In this thesis, we propose three kinds of NCs with different properties (Ge, NiSi and MnSiO NCs) to overcome the limitation of conventional NVMs during the scaling down process. The proposed NCs combined with nitride layer can be efficiently improved the charge trapping ability and reliability. When a memory device has a larger memory window, it is easier to meet the requirement of retention of 10 years. And, hope to solve the two limitations mentioned above.

1.3 Organization of This Thesis

In this thesis, we propose three kinds of NCs with different properties (Ge, NiSi and MnSiO NCs) to overcome the limitation of conventional NVMs during the scaling down process.

In chapter 3, we proposed a SiGeO stacking structure serving as Ge nanocrystals self-assembled layer for application of NCs NVM. In additional we fond out that pre-annealing-capping oxide (PACO) is a critical step in our experimental process, and then we used the different oxidized competition mechanism between Si and Ge to form Ge NCs embedded in oxide. The uniform and high density (~$10^{12}$$cm^{-2}$) of Ge nanocrystals was fabricated after a rapid thermal annealing (RTA) process. Our propose technique compared with traditional Ge NCs process can be efficiently to prevent the over-oxidation phenomenon of Ge NC which reduces the charge trapping ability.

In chapter 4, we used the similar method that oxygen was replaced by nitrogen to form the Ge NCs embedded in SiN_x structure. The memory window for the stacked structure with Ge NCs embedded in SiN_x layer is larger than Ge NCs embedded in SiO_x layer, due to the extra charge trapping centers generated from the surrounding dielectric of Ge NCs. Furthermore, to compare these Ge NCs structures, we found that the Ge NCs embedded in nitride had better charge storage ability and reliability for NVM characteristics.

In chapter 5 and 6, an ease and low temperature fabrication technique of Ni-O-Si and Ni-Si-N NCs was demonstrated for the application of nonvolatile memory in this thesis. This result can be considered that the oxygen plays a critical role during sputter process for the formation of nanocrystal. In addition, the high density (~10^{12} cm^{-2}) NC can be simple and uniform to be fabricated in our study. We

also found that high density Ni-Si-N NCs embedded in the silicon nitride (SiN_x) and larger memory effect. Therefore, by using an internal competition mechanism of charge trapping layer for these elements, we can form a metallic NCs NVM with low temperature process.

In chapter 7, 8 and 9, a RTA with temperature about 500°C and 600°C at short duration was further used to improve the crystalline quality of NCs and memory reliability. Thermal treatment can efficiently reduce the defects (leakage path) in the SiN_x which surrounds the nanocrystal. The charge storage layer of NCs embedded in SiN_x shows larger memory window and better reliability over NCs embedded in SiO_x, due to different distributions of electronic field in the NC and surrounding dielectric by the simulation results. In addition, multi-layer NiSi NCs NVM structure had better charge storage and retention over than single-layer metal nanocrystals under high temperature test, due to the first and second layer of multi-layer with Quantum confinement effect depended by the NC size.

In chapter 10, for dielectric NCs process, we also used the sputter system to fabricate the manganese silicate ($MnSiO_x$) NCs. The XPS results of charge trapping layer can be identified the chemical state of NCs and built the energy band diagram of our produced $MnSiO_x$ thin film. Moreover, by the relationship of current density with temperature, the trap assisted tunneling model can be used to extract the trapping level and density of $MnSiO_x$. The oxygen doping concentration will affect the trap level position and also influence the retention characteristics for the reliability test. Double layer $MnSiO_x$ NCs NVM also was fabricated and discussed its NVM effect. The double layer was better trapping and keeping charges ability than single layer because the trapped charges must overcome the trap barrier and then escape from NCs due to the trapping mode of dielectric NCs.

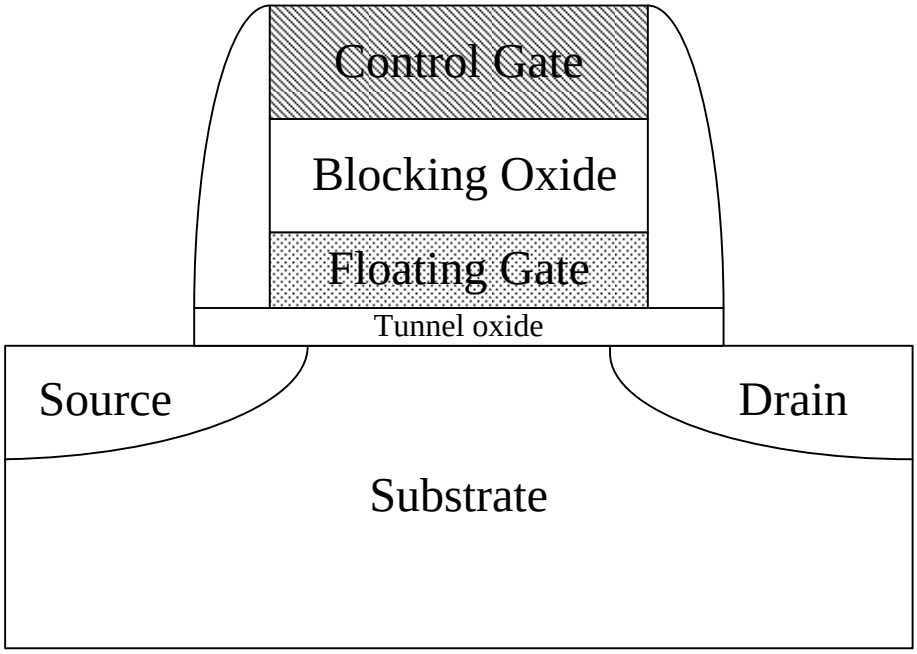


Figure 1-1 Structure of the conventional floating-gate nonvolatile memory device. Continuous poly-Si floating gate is used as the charge storage element.

Year of production	2004	2007	2010	2013	2016
Technology node (nm)	90	65	50	35	25
Flash NOR Lg(um)	0.2-0.22	0.19-0.21	0.17-0.19	0.14-0.16	0.12-0.14
Flash NOR highest W/E voltage (V)	7-9	7-9	7-9	7-9	7-9
Flash NAND highest Voltage (V)	17-19	15-17	15-17	15-17	15-17
NOR tunnel oxide(nm)	8.5-9.5	8-9	8-9	8	8
NAND tunnel oxide(nm)	7-8	6-7	6-7	6-7	6-7

Solution exist | Solution known | Solution NOT known

Figure 1-2 Tunnel oxide and operation voltage scaling predicted by the 2007 International Technology Roadmap for Semiconductors.

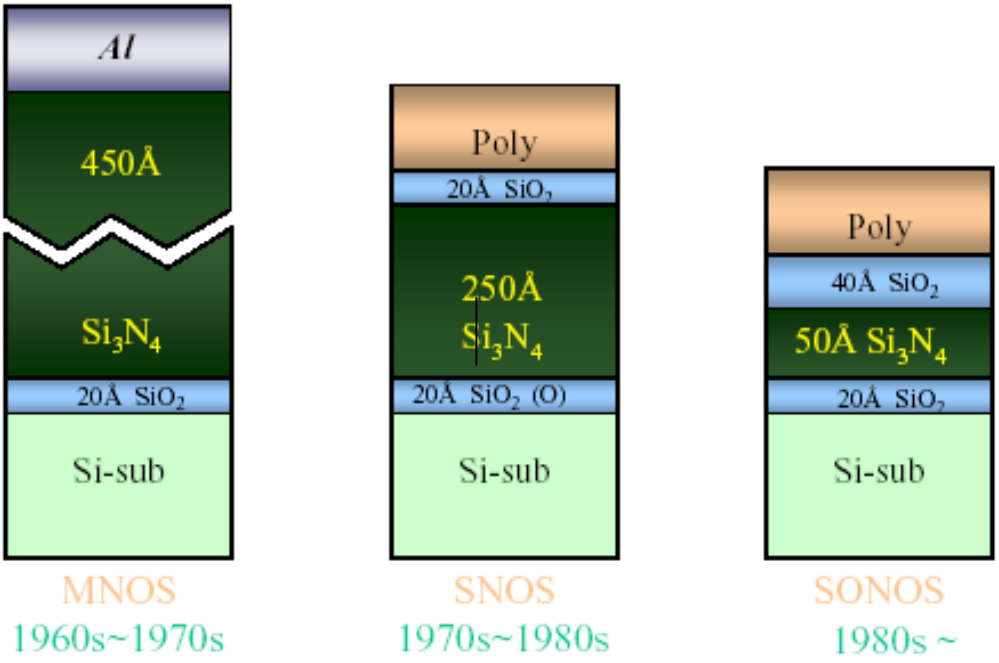


Figure 1-3 Development of the gate stack of SONOS EEPROM memory devices. The optimization of nitride and oxide films has been the main focus in recent years.

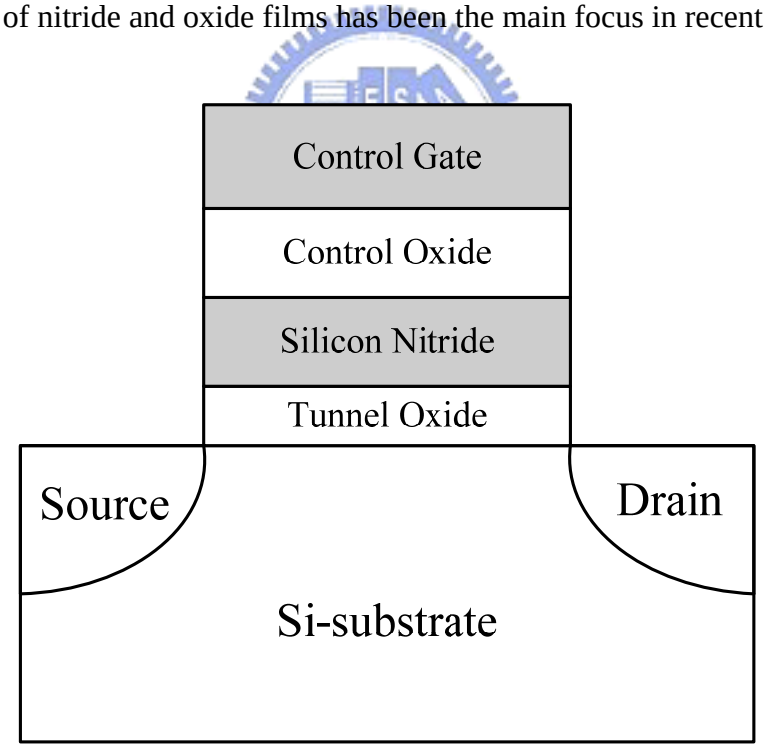


Figure 1-4 Structure of the SONOS nonvolatile memory device. The nitride layer is used as the charge trapping media.

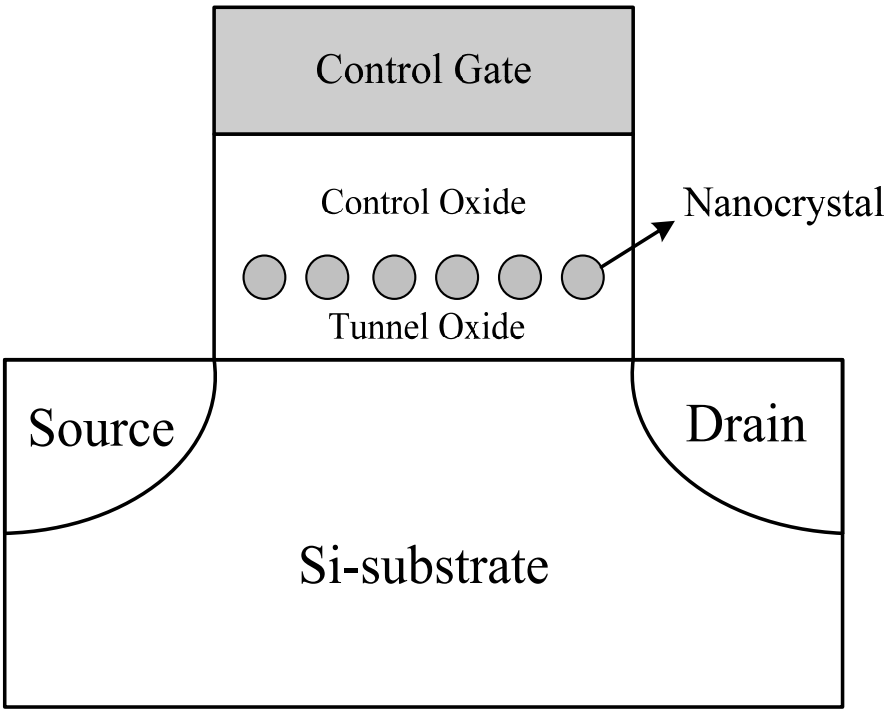


Figure 1-5 Structure of the nanocrystal nonvolatile memory device. The nanocrystals are used as the charge storage element instead of the continuous poly-Si floating gate.

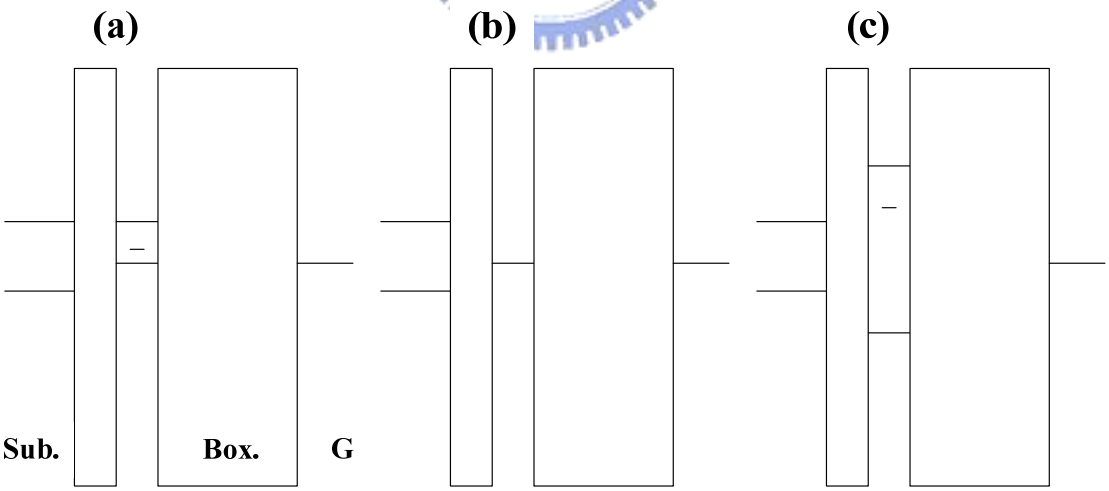


Figure 1-6 Energy band diagrams of (a) Ge, (b) Ni and (c) HfO_2 nanocrystals nonvolatile memories. Sub.: Silicon substrate, Box.: Blocking oxide, G: Gate.

Chapter 2

Basic Principles of Nonvolatile Memory

2.1 Programming/Erasing mechanisms of nonvolatile memory

Most novel nonvolatile memories (NVMs), such as nanocrystals and SONOS memories are based on the concept of Flash memory. If a datum has to be stored in a bit of the memory, there are different procedures. The threshold voltage shift of a Flash transistor can be written as [2.1-2.3]:

$$\Delta V_T = -\frac{\overline{Q}}{C_{FC}} \tag{2-1}$$

where $\overline{Q}$ is the total charge stored in the floating gate, and C_{FG} is the capacitances between the floating-gate (FG) and control gate. The threshold voltage of memory cell can be altered by charging (discharging) the amount of charge into the FG and defined to the two states of the memory cell, i.e., the binary values ("1" and "0") of the stored bit. Figure 2-1 shows the threshold voltage shift between two states in a Flash memory. The cure A of Fig. 2-1 is an initial state "1" before the programming operation and the cure B is a writing state "0" when negative charges are stored in the FG. There are many solutions to achieve "programming" or "erasing" operation. In general, tunneling effects included with direct tunneling, Fowler-Nordheim tunneling and band to band tunneling and hot carriers injections are the two kinds of operation mechanisms employed in the NVMs. These modes of stored charges transportation mechanisms will lead to difference characteristics for NVMs and the authors will briefly intro them, as follows,

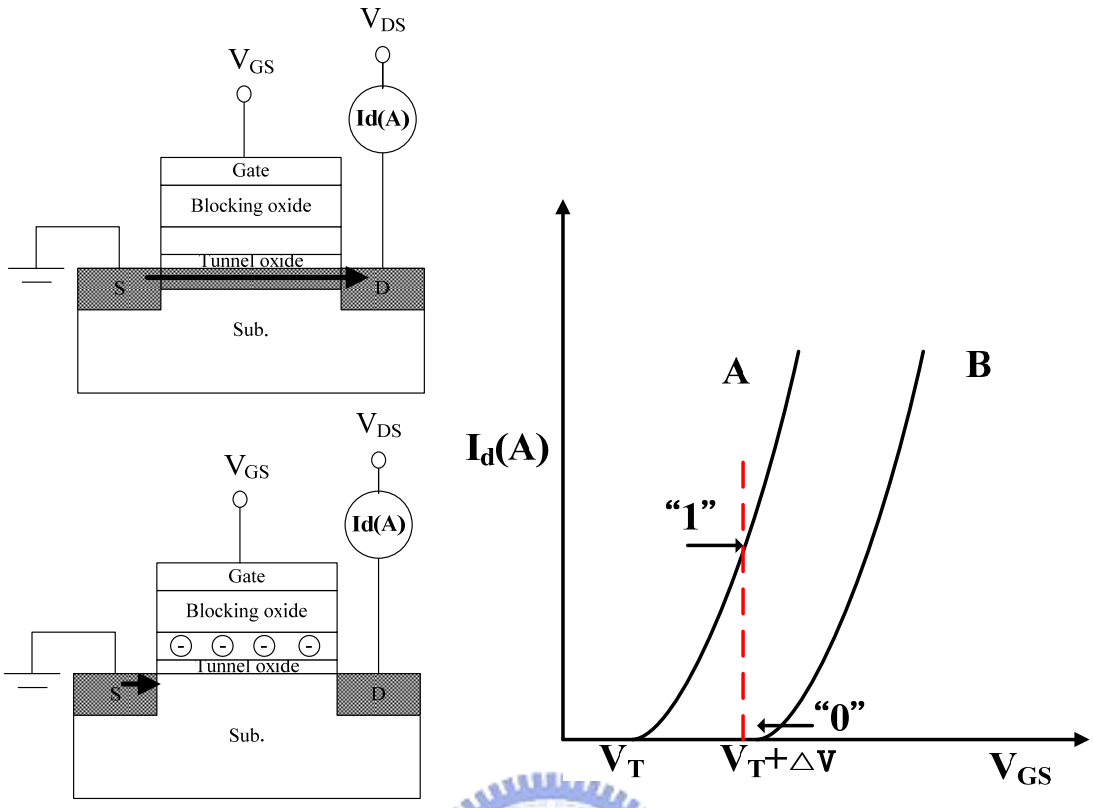


Figure 2-1 I–V curves of an FG device when there is no charge stored in the FG (curve A) and when negative charges are stored in the FG (curve B).

Modes of Stored Charges Transportation

2.1.1. Tunneling effect

Tunneling mechanisms are demonstrated in the quantum mechanics. Basically, carriers tunneling injection must to have available states to exist on the other side of the barrier. If we assume elastic tunneling, this is a reasonable assumption due to the thin oxide thickness involved. In other words, there is no any energy loss during tunneling processes. The tunneling probability is depended on electron barrier height (φ (x)), tunnel dielectric thickness (d) and effective mass (m_e), that is express as:

$$T = \exp(-2\int_0^d \frac{\sqrt{\varphi(x)m_e}}{\eta} dx) \qquad (2\text{-}2)$$

The carriers tunneling effect through the tunnel oxide can be attributed to different carrier-injection mechanisms which depend on the tunnel dielectric thickness and the

applied gate electric field. Hence, Direct tunneling (DT), Fowler-Nordheim tunneling (FN), modified Fowler-Nordheim tunneling (MFN) and trap assistant tunneling (TAT) are the main programming mechanisms employed in the NVM application. Fig. 2-2 shows these four tunnel effects approaches to programming methods.

A. Direct Tunneling effect (DT)

For nanocrystal memories, the control-gate coupling ratio of nanocrystal memory devices is inherently small [2.4]. As a result, FN tunneling cannot serve as an efficient write/erase mechanism when a relatively thick tunnel oxide is used, because the strong electric field cannot be confined in one oxide layer. When the thickness of tunnel oxide is below 5 nm, the direct tunneling is employed in nanocrystal memories instead. In the other hand, the direct tunneling is more sensitive to the barrier width than barrier height which two to four orders of magnitude reduction in leakage current can still be achieved if the metals with large work function, such as Au or Pt [2.5].

B. Fowler–Nordheim Tunneling effect (FN)

The Fowler–Nordheim (FN) tunneling mechanism occurs when applying a strong electric field (in the range of 8–10 MV/cm) across a thin oxide. In these conditions, the energy band diagram of the oxide region is very steep. Therefore, there is a high probability of electrons' passing through the energy barrier itself. Using a free-electron gas model for the metal and the WKB approximation for the tunneling probability [2.6], one obtains the following expression for current density [2.7]:

$$J = \frac{q^3 F^2}{16\pi^2 h^2 \Phi_B} \exp\left[\frac{-4(2m_{OX}^*)^{0.5}\Phi_B^{1.5}}{3\eta q F}\right] \qquad (2\text{-}3)$$

where Φ_B is the barrier height, m_{OX}^* is the effective mass of the electron in the forbidden gap of the dielectric, h is the Planck's constant, q is the electronic charge, and F is the electric field through the oxide. However, the exponential dependence of

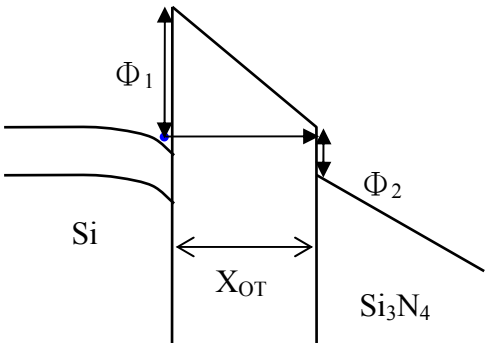
tunnel current on the oxide-electric field causes some critical problems of process control because, for example, a very small variation of oxide thickness among the cells in a memory array produces a great difference in programming or erasing currents, thus spreading the threshold voltage distribution in both logical states.

C. Modified Fowler-Nordheim tunneling (MFN)

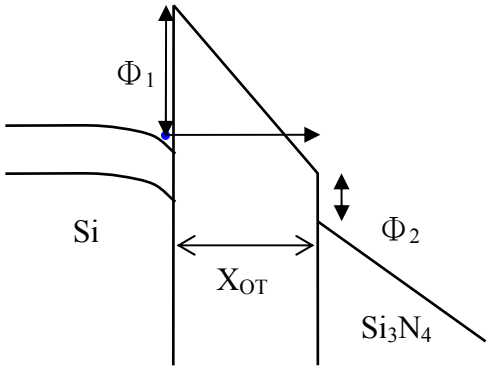
Modified Fowler–Nordheim tunneling (MFN) is similar to the traditional FN tunneling mechanism, yet the carriers enter the nitride at a distance further from the tunnel oxide-nitride interface. MFN mechanism is frequently observed in SONOS-type memories. The SONOS-type memory is designed for low-voltage operation (<10V, depending on the Equivalent oxide thickness), a relatively weak electric field cannot enhance charges to inject into the charging trapping layer by DT or FN mechanism.

D. Trap assistant tunneling effect (TAT)

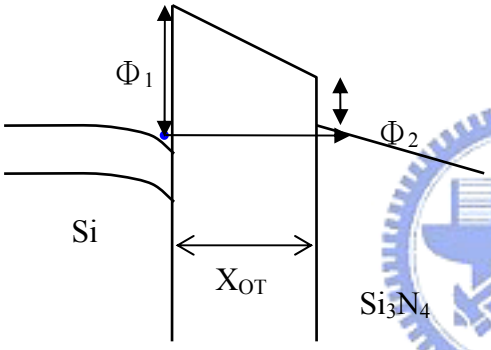
The charge storage mediums with many traps may cause another tunneling mechanism. For example, the charges tunnel through a thin oxide and arrive to the traps of nitride layer at very low electric field in SONOS systems. During trap assisted injection the traps are emptied with a smaller time constant then they are filled. The charge carriers are thus injected at the same distance into the nitride as for MFN injection. Because of the sufficient injection current, trap assistant tunneling may influence in retention [2.8].



DT occur when $\frac{\Phi_1}{X_{OT}} > |E_{OT}| > \frac{\Phi_1 - \Phi_2}{X_{OT}}$

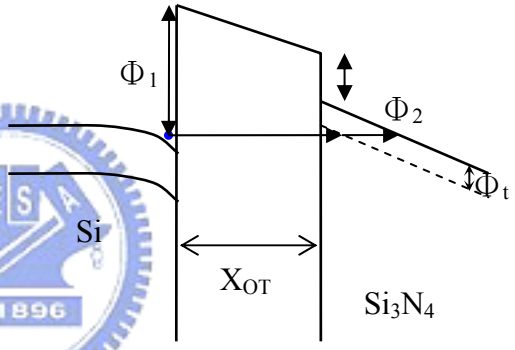


FN occur when $|E_{OT}| > \frac{\Phi_1}{X_{OT}}$



MFN occur when

$$\frac{\Phi_1 - \Phi_2}{X_{OT}} > |E_{OT}| > \frac{\Phi_1 - \Phi_2}{X_{OT} + \left(\varepsilon_{ox} / \varepsilon_N\right) X_N}$$



TAT occur when

$$\frac{\Phi_3}{X_{OT}} > |E_{OT}| > \frac{\Phi_3}{X_{OT} + \left(\varepsilon_{ox} / \varepsilon_N\right) X_N}$$

$$\Phi_3 = \Phi_1 - \Phi_2 - \Phi_t$$

Figure 2-2 Four tunnel effects approaches to programming methods described by Hu and White et al.

2.1.2. Channel Hot-Electron Injection (CHEI)

The physical mechanism of CHEI is relatively simple to understand qualitatively. An electron traveling from the source to the drain gains energy from the lateral electric field and loses energy to the lattice vibrations (acoustic and optical phonons). At low fields, this is a dynamic equilibrium condition, which holds until the field strength reaches approximately 100kV/cm [2.9]. For fields exceeding this value, electrons are no longer in equilibrium with the lattice, and their energy relative to the conduction band edge begins to increase. Electrons are "heated" by the high lateral electric field, and a small fraction of them have enough energy to surmount the barrier between oxide and silicon conduction band edges. Figure 2-3 shows schematic representation of CHEI MOSFET and the energy-distribution function with different fields. In the other hand, the effective mass of hole is heavier than one of electron. It is too hard to obtain enough energy to surmount oxide barrier. Therefore, hot-hole injection rarely is employed in nonvolatile memory operation. For an electron to overcome this potential barrier, three conditions must hold [2.10].

1) Its kinetic energy has to be higher than the potential barrier.

2) It must be directed toward the barrier.

3) The field in the oxide should be collecting it.

Nevertheless, a description of the injection conditions can be accomplished with two different approaches. The CHEI current is often explained and simulated following the "lucky electron" model [2.11]. This model is based on the probability of an electron's being lucky enough to travel ballistically in the field G for a distance several times the mean free path without scattering, eventually acquiring enough energy to cross the potential barrier if a collision pushes it toward the Si/SiO_2 interface. Consequently, the probability of injection is the lumped probability of the

following events, which are depicted in Figure 2-4 [2.12].

1) The carrier has to be "lucky" enough to acquire enough energy from the lateral electric field to overcome the oxide barrier and to retain its energy after the collision that redirects the electron toward the interface ($P_{\Phi b}$).

2) The carrier follows a collision-free path from the redirection point to the interface (P_{ED}).

3) The carrier can surmount the repulsive oxide field at the injection point, due to the Schottky barrier lowering effect, without suffering an energy-robbing collision in the oxide (P_{OC}).

The current density of CHEI is expressed as

$$I_{inj} = A_d I_{ds} (\frac{\lambda E_m}{\varphi_b})^2 \exp(-\varphi_b / \lambda E_m) \qquad (2\text{-}4)$$

Here I_{ds} is the channel current and A_d is a constant. φ_b is the injection barrier and λ is the mean free path associated with the phonon scattering. E_m is the lateral electric field at drain.

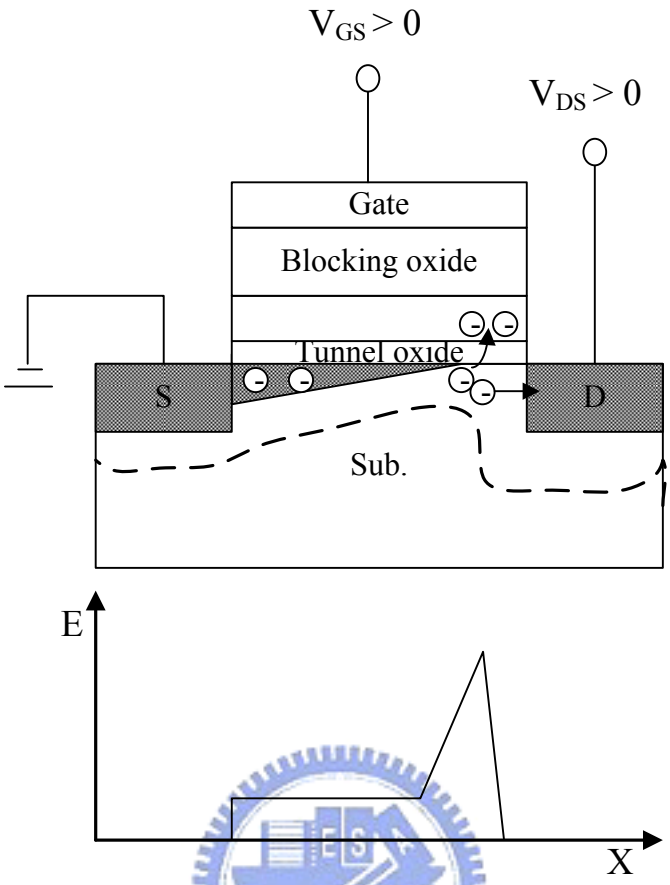


Figure 2-3 Schematic cross section of MOSFET. The lateral electric field (E) distribution function is also shown.

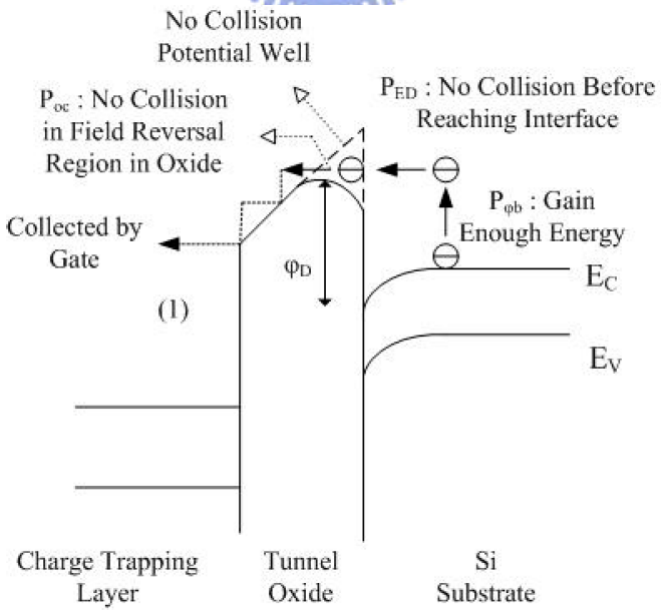


Figure 2-4 A schematic energy band diagram describing the three processes involved in electron injection.

2.1.3. Band to Band Tunneling (BTBT)

Band to band tunneling application to nonvolatile memory was first proposed in 1989. I. C. Chen and et al. demonstrated a high injection efficiency (~1%) method to programming EPROM devices [2.13]. Band-to-band Tunneling (BTBT) process occurs in the deeply depleted doped surface region under the gate to drain / gate to source overlap region. In this condition, the band-to-band tunneling current density is expressed as

$$J_{b-b} = \frac{\sqrt{2m^*}q^3\varepsilon V_{app}}{4\pi^3\eta^2 E_g^{0.5}} \exp\left[-\frac{4\sqrt{2m^*}E_g^{1.5}}{3q\varepsilon\eta}\right] \quad (2\text{-}5)$$

(a) Band to Band Hot Electron Tunneling Injection

This injection mechanism is used to nonvolatile memory of PMOS structure. When band-bending is higher than the energy gap of the semiconductor, the tunneling electron from the valence band to the conduction band becomes significant. The mechanism is at the condition for positive gate voltage and negative drain voltage. Hence, the hot electrons are injected through the tunnel oxide and then recombine the stored electrons as shown in Fig. 2-5.

(b) Band to Band Hot Hole Tunneling Injection

The injection is applied for NMOS nonvolatile memory device. The mechanism is at the condition for negative gate voltage and positive drain voltage. Hence, the hot holes are injected through the tunnel oxide and then recombine the stored electrons as shown in Fig. 2-6.

The electrons (n-type) / holes (p-type) are accelerated by a lateral electric field toward the channel region and some of the electrons with sufficient energy can surmount the potential barrier of SiO_2 [2.14-2.16]. Due to the small oxide field, the electron/hole influence through the oxide can easily reach hundreds of coulombs per square centimeter without failure, it means to the improvement reliability of memory

cells.

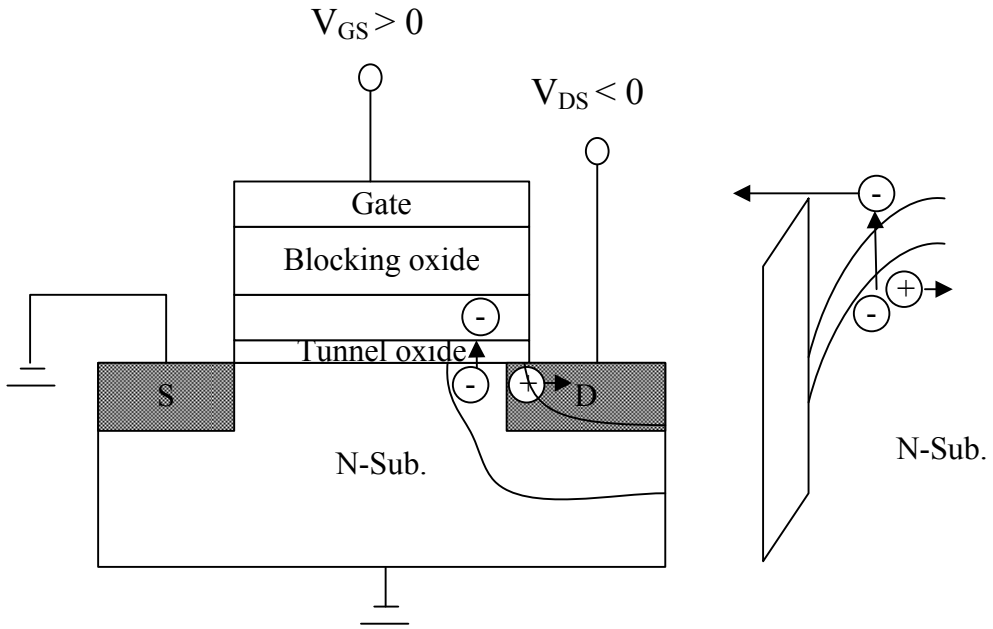


Figure 2-5 Schematic sketch and energy band diagram of Band to Band Hot Electron Tunneling Injection.

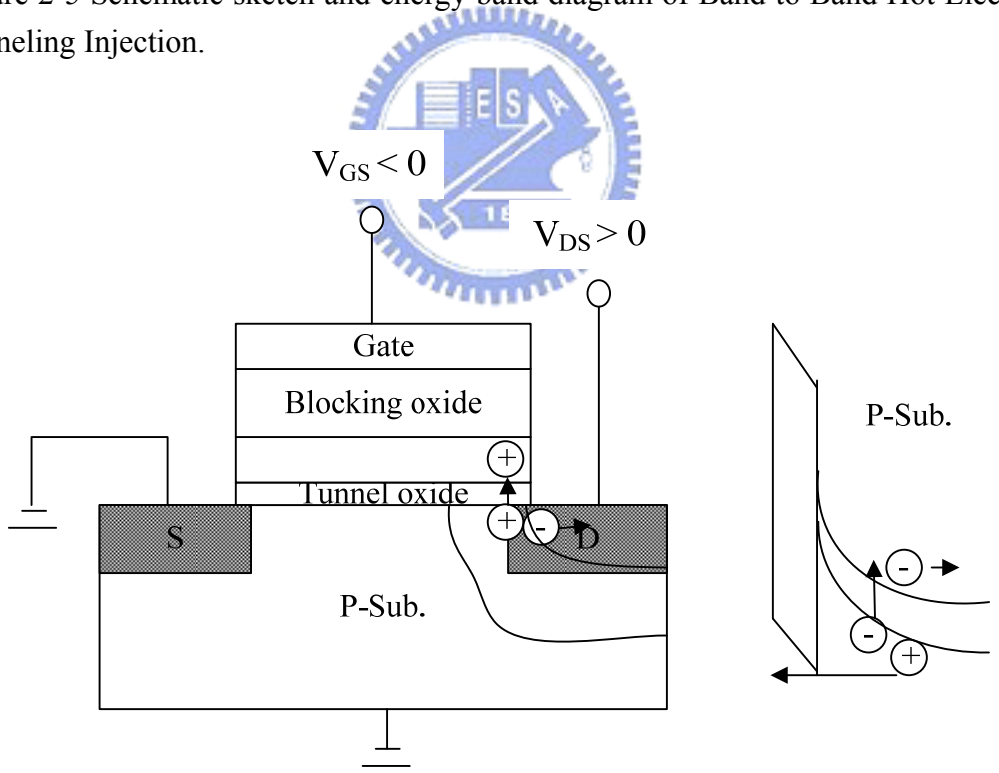


Figure 2-6 Schematic sketch and energy band diagram of Band to Band Hot Hole Tunneling Injection.

2.1.4. Channel Initiated Secondary Electron Injection (CHISEI)

The main difference between CHE and CHISEL is that CHISEL is highly sensitive to the lateral electrical field and vertical electrical filed. The operation condition is at CHI condition plus negative body voltage (VB). The procedure and the band diagram for the application of CHISEL are as shown in Fig. 2-7. The superior injection of CHISEL operation mode leads to more program efficiency. The improved program efficiency results from the substrate enhanced gate current component. Under optimized substrate condition, the substrate hot carriers and subsequent injection are expected for the application of low power and high speed.

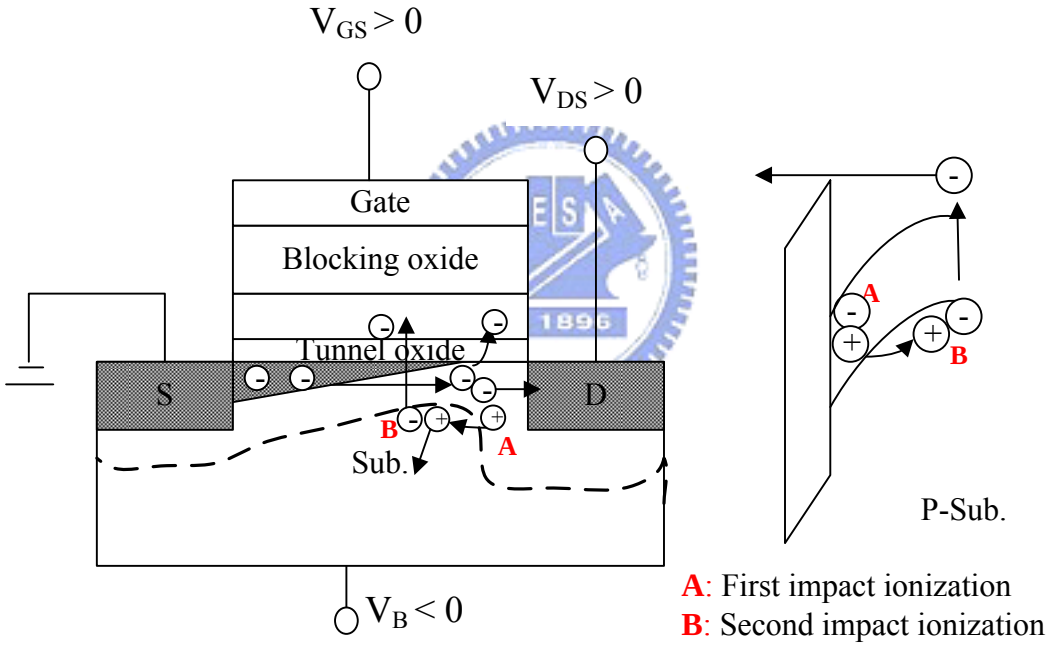


Figure 2-7 Schematic sketch and energy band diagram of Channel Initiated Secondary Electron Injection.

2.2 Basic Physical Characteristic of Nanocrystal Memory

The nanocrystal size is about 3 nm ~ 5 nm and hence we must consider that the quantum effect is how to affect the charge storage ability, programming/erasing efficiency and retention. The major quantum effects include with quantum confinement effect and coulomb blockade effect.

2.2.1 Quantum Confinement Effect

The quantum dot is a quasi-zero-dimensional nano-scale object and is also composed by small amount of atoms. The quantum confinement energy depended on nanocrystal size has been studied both experimentally and theoretically with the tight-binding model [2.17]. The quantum confinement effect becomes significant when the nanocrystal size shrinks to the nanometer range, which causes the ground state of nanocrystal to shift to higher energy compared with bulk material [2.18]. This result will reduce the charge storage ability and programming efficiency for the semiconductor nanocrystals. The theoretical ground state shift of semiconductor and metal nanocrystals has been proposed by W. Guan et al. at 2007 [2.19]. The ground state shift (△E) of Ge and Ni nanocrystals are expressed as

$$\Delta \mathrm{E}_{\mathrm{Ge}} = E(\infty) + \frac{11.8637}{d_{Ge}^2 + 2.391 d_{Ge} + 4.252} \qquad \Delta E_{Ni} = \frac{0.1639}{d_{Ni}^3} \tag{2-6}$$

Where E (∞) is the conduction band minimum for bulk Ge and d is the diameter of nanocrystal. For example, a 3 nm Ge nanocrystal can have a conduction band shift of 0.5 eV as compared with bulk Ge, which is significant enough to affect the electrical performance of the nanocrystal memory cell. Figure 2-8 shows the conduction band minimum up-shift of silicon nanocrystal and Fermi level up-shift of metal NC as a function of nanocrystal size by W. Guan's model.

2.2.2 Coulomb Blockade Effect

When one electron is stored, the nanocrystal potential energy is raised by the electrostatic charging energy $e^2/2C$, where C is the nanocrystal capacitance, which depends mainly on the nanocrystal size, though it also depends on tunnel oxide thickness and control oxide thickness. The capacitance is self-consistently calculated using an electrodynamics method [2.20]. The electron charge will raise the nanocrystal potential energy and reduce the electric field across the tunnel oxide, resulting in reduction of the tunneling current density during the write process. It is more dominant at low programming voltages (< 3V). In a flash memory array, device cells often encounter disturbances with low gate voltage soft-programming. The Coulomb blockade effect can effectively inhibit the electron tunneling at low gate voltage and improve the flash memory array immunity to disturbance. However, the Coulomb blockade effect should be reduced by employing large nanocrystal if large tunneling current and fast programming speed were desired. The Coulomb blockade effect has a detrimental effect on the retention time, since the electrons in the nanocrystal have large tendency to tunnel back into the channel if the nanocrystal potential energy is high in retention mode. In the energy band diagram of Fig. 2-9, the Coulomb blockade charging energy only raises the electrostatic potential of the nanocrystal.

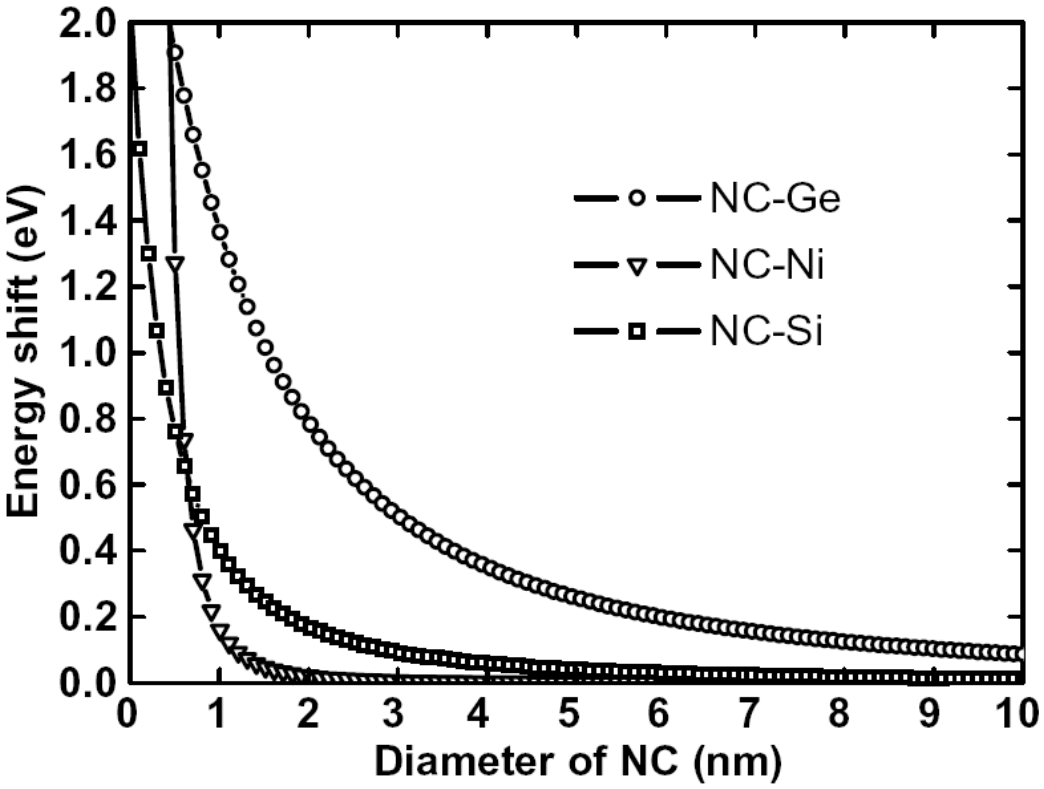


Figure 2-8 Conduction band minimum up-shift of silicon nanocrystal and Fermi level up-shift of metal NC as a function of nanocrystal size by W. Guan's model [2.19].

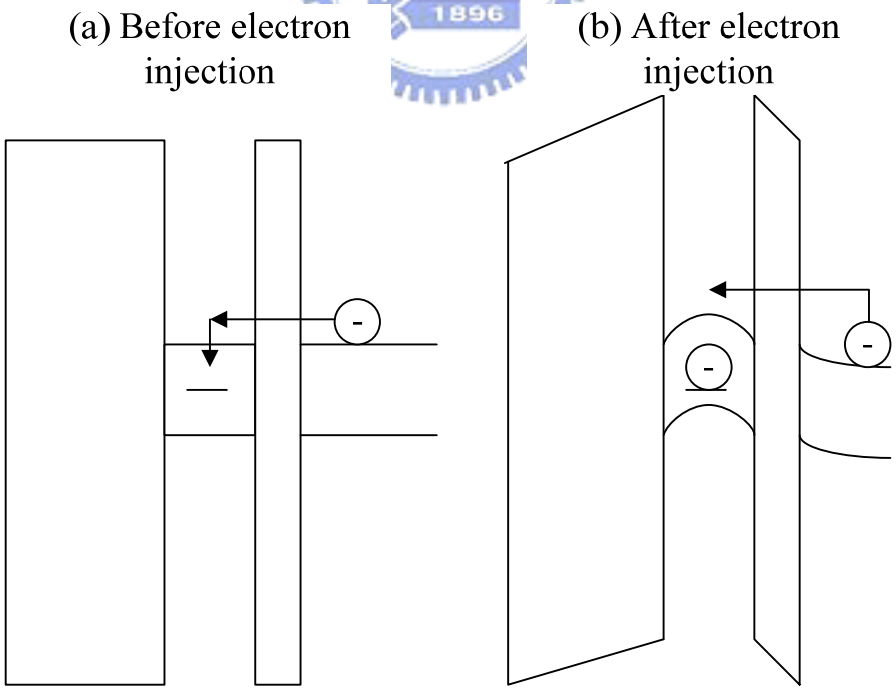


Fig. 2-9 Schematic energy band diagram of coulomb blockade effect (a) before electron injection, and (b) after one electron injection.

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2.3 Reliability of Nonvolatile Memory

The reliability of nonvolatile memory has two major parts which one is retention and the other is endurance. These reliability tests are very importance for nonvolatile memory application to the portable electronic productions market and they are norm to define the charge loss ratio in the long-term use. In general, NVMs are required to withstand up to 100K-1M program/erase cycles (endurance) with 10-year memory retention. Therefore, in this section, the authors will present the operation mechanisms and related non-ideal factors of retention and endurance tests.

2.3.1 Retention

In any nonvolatile memory technologies, they are essential to retain data in formation for over ten years. This means the loss of charge stored in the storage medium must be as low as possible. For example, in modern Flash cells, FG capacitance is approximately 1 fF. A loss of only 1 fC can cause a 1V threshold voltage shift. If we consider the constraints on data retention in ten years, this means that a loss of less than five electrons per day can be tolerated [2.21].

Possible causes of charge loss are: 1) by tunneling or thermionic emission mechanisms; 2) defects in the tunnel oxide; and 3) detrapping of charge from insulating layers surrounding the storage medium.

First, several discharge mechanisms may be responsible for time and temperature dependent retention behavior of nonvolatile memory devices. Figure 2-10 shows an energy band diagram of SONOS device in the excess electron state [2.22], illustrating trap-to-band tunneling, trap-to-trap tunneling, and band-to-trap tunneling, thermal excitation and Poole-Frenkel emission retention loss mechanisms.

These mechanisms may be classified into two categories. The first category contains tunneling processes that are not temperature sensitive (trap-to-band tunneling, trap-to-trap tunneling and band-to-trap tunneling). The second category contains those

mechanisms that are temperature dependent. Trapped electrons may redistribute vertically inside the nitride by Poole–Frenkel emission, which will give rise to a shift in the threshold voltage. Moreover, at elevated temperatures, trapped electrons can also be thermally excited out of the nitride traps and into the conduction band of the nitride (thermal excitation), and drift toward the tunnel oxide, followed by a subsequent tunneling to the silicon substrate.

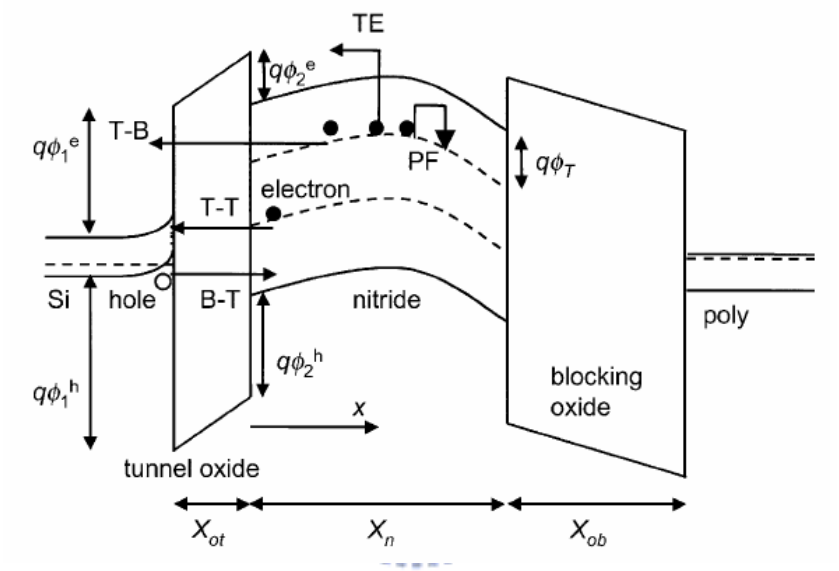


Figure 2-10 Energy band diagram of a SONOS device in the excess electron state, showing retention loss mechanisms: trap-to-band tunneling (TB), trap-to-trap tunneling (T-T), band-to-trap tunneling (B-T), thermal excitation (TE) and Poole–Frenkel emission (PF). [2.22]

Secondly, the defects generated in the tunnel oxide can be divided into an extrinsic and an intrinsic one. The former is due to defects in the device structure; the latter to the physical mechanisms that are used to program and erase the cell. Electrons can be trapped in the insulating layers surrounding the storage medium during wafer processing, as a result of the so-called plasma damage, or even during the UV exposure normally used to bring the cell in a well-defined state at the end of the process. The electrons can subsequently detrap with time, especially at high

temperature. The charge variation results in a variation of the storage medium potential and thus in channel length decrease [2.23]. The retention capability of Flash memories need to be checked by using accelerated tests that usually adopt screening electric fields and hostile environments at high temperature.

2.3.2 Endurance

Endurance is the number of erase/write operations that the memory will complete and continue to operate as specified in the data sheet. Generally speaking, Flash products are specified for 10^6 erase/program cycles. Nevertheless, the endurance requirement may be relaxed with the increase of memory density for the other applications. Figure 2-11 shows the Endurance requirements of NAND Flash memories [2.24].

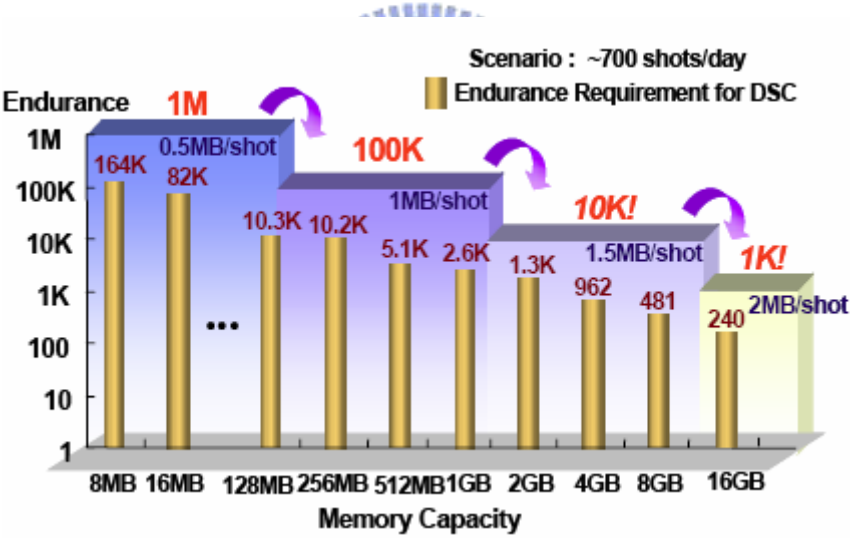


Figure 2-11 Endurance requirements as a function of memory capacity. [2.24]

The endurance requirement is relaxed to 100K cycles for 256 MB density. In the higher density, a certain cell in a block has less possibility to be written and erased since the memory operation on the cell is repeated after using up the whole memory blocks. The endurance requirement is sufficient for the user to take 700 photos with a 1MB size every day for 10 years. A typical result of an endurance test on a single cell

is shown in Fig. 2-12. As the experiment is performed applying constant pulses, the variations of program and erase threshold voltage levels are described as "program/erase threshold voltage window closure" and give a measure of the tunnel oxide degradation [2.25, 2.26].

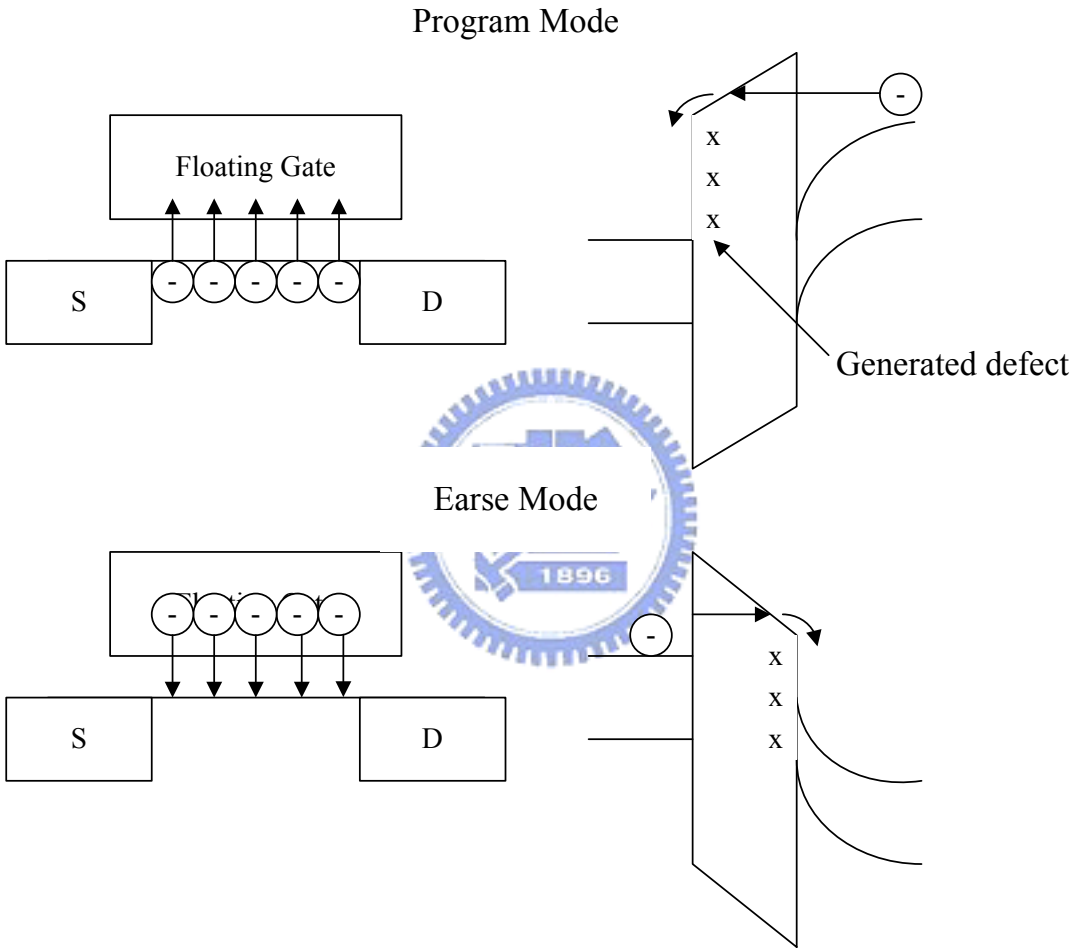


Figure 2-12 Threshold voltage window closure as a function of program/erase cycles on a single cell due to the degradation of tunnel oxide.

In particular, the reduction of programmed threshold voltage with cycling is due to trap generation in the oxide and to interface state generation at the drain side of the channel. The evolution of the erase threshold voltage reflects the dynamics of net fixed charge in the tunnel oxide as a function of the injected charge. The initial lowering of the erase is due to a pile-up of positive charge which enhances tunneling efficiency, while the long-term increase of the erase is due to a generation of negative traps.

Moreover, a high field stress on thin oxide is known to increase the current density at low electric field. The excess current component, which causes a significant deviation from the current–voltage curves from the theoretical FN characteristics at low field, is known as stress-induced leakage current (SILC). SILC is clearly attributed by stress-induced oxide defects, which leads to a trap assisted tunneling, as shown in Fig. 2-13. The main parameters controlling SILC are the stress field, the amount of charge injected during the stress, and the oxide thickness. For fixed stress conditions, the leakage current increases strongly with decreasing oxide thickness [2.27-2.28].

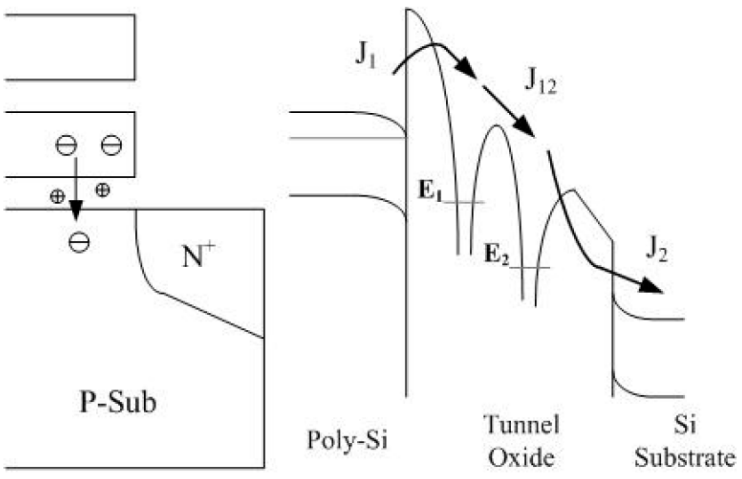


Figure 2-13 Anomalous stress induced leakage current (SILC) modeling. The leakage is caused by a cluster of positive charge generated in the oxide during erase. [2.24]

2.4 Gibbs free energy

In thermodynamics, the Gibbs free energy is a thermodynamic potential which measures the "useful" or process-initiating work obtainable from an isothermal, isobaric thermodynamic system. When a system changes from a well-defined initial state to a well-defined final state, the Gibbs free energy (ΔG) equals the work exchanged by the system with its surroundings, less the work of the pressure forces, during a reversible transformation of the system from the same initial state to the same final state. The change (ΔG) in Gibbs free energy is a parameter to measure a spontaneous tendency of the reaction. The ΔG is usefully defined by

$$\Delta G = \Delta H \ — \ T\Delta S$$

Where H is the enthalpy, T is temperature, and S is the entropy. If Δ*G* is negative, the reaction is a spontaneous. If Δ*G* is positive, the reverse reaction is a spontaneous. The larger Δ*G* value indicates that the reaction is easier to take place with higher reaction rate. After reaction, the Δ*G* value represents the energy which is released as heat to the environment. At chemical equilibrium, the rate of forward reaction is equal to the rate of reverse reaction, Δ*G* = 0. In generally, the Δ*G* value is nearly dominated by the enthalpy (Δ*H*) because the *T*Δ*S* value is much less than Δ*H.*

Chapter 3

Germanium Nanocrystals Nonvolatile Memories

3.1 Formation and Nonvolatile memory effect of Germanium Nanocrystal embedded in Oxide layer using Silicon-Germanium-Oxygen layers

3.1.1 Introduction

The nonvolatile memory (NVM) for portable electronic productions is very important to the semiconductor industries because of its superiority in the low-power consumption, low-cost, high-memory capacity and enough data retention [3.1, 3.2]. However, the current NVM with floating gate (FG) structure cannot efficaciously prevent data loss in terms of the reliability trials for the future scaling down process [3.3, 3.4]. Due to the discrete charge storage nodes acting as charge trapping layer to reform the drawbacks of current FG memory, the NVMs using various semiconductor nanocrystals have been widely investigated in the past few years , such as silicon (Si) , germanium (Ge) and Zine-Oxide (ZnO) nanocrystals [3.2, 3.5]. Moreover, the Ge nanocrystals have better memory performance than the Si and ZnO nanocrystal because of theirs smaller energy band gap (~0.6eV) and higher dielectric constant (~16.0, i.e., stronger coupling with the conduction channel).

According to the current research, the self-assembled and direct growth of Ge nanocrystals embedded in SiO_2 layer has successfully been implemented, such as Ge implantation into SiO_2 [3.6, 3.7], oxidation, reduction of Ge/Si islands [3.8], UV-assisted oxidation of $Si_{1-x}Ge_x$ alloy [3.9], and rapid thermal oxidation (RTO) of Ge NCs [3.10, 3.11] or Ge + SiO_2 [3.12]. Among various formation methods, the self-assembled method was reported by many previous studies because it could control better density and size of nanocrystal than direct growth. Nevertheless, the

self-assembled method must need a high temperature (~900-1100^{o}C) with the long duration (~30-60 min) oxidation process to anneal the charge trapping layer which is generally deposited by the various ratio of SiGe layer, and we need to take account of an over-oxidation phenomenon of Ge nanocrystals after the foregoing oxidation process [3.13]. This is a very serious drawback for the Ge nanocrystals in the future NVM application. Hence, a redox step must be added to the formation flow of Ge nanocrystal by using an additional high pressure H_2 treatment or steam process [3.14].

We therefore undertook a different line of investigations to shun the disadvantages of self-assembled method of conventional Ge nanocrystals fabrication and reduce thermal budget. Our investigation focused on the use of silicon-germanium-oxygen (SiGeO) thin film to form the high density and good spatial distribution of Ge nanocrystals embedded in the dielectric for the NVM application. Here, we also used different annealing ambiances (N_2 and O_2) to obtain the different experiment results and tried to explain their diversity on the electrical characteristics by the suppositional energy band diagram structures. In addition, in this study, we found that pre-annealing-capping-oxide (PACO) was a critical step for the formation and electronic characteristics of Ge nanocrystals using the SiGeO thin layer.

3.1.2 Experiment

The fabrication of NVM structure was started with a thermal dry oxidation at 950 ^{o}C to form a tunnel oxide about 5 nm on p-type (100) Si wafer which had been removed native oxide and particles by RCA process, and then a 10-nm-thick charge tapping layer was deposited by the reactive sputtering of $Si_{0.5}Ge_{0.5}$ alloy target in the Ar/O_2 (24 sccm / 2 sccm) ambiance at room temperature. This step could obtain a $Si_{1.33}Ge_{0.67}O_2$ layer whose the ratio of atoms concentration was analyzed by X-ray photoelectron spectroscopy (XPS). The XPS analysis by using an Al *K*α (1486.6 eV) x-ray radiation is demonstrated the chemical composition of the charge trapping layer (SiGeO thin layer), as shown in Fig. 3-1. From the Si 2*p*, Ge 3*d*, O 1*s* orbits of Fig. 3-1, we can roughly define the atomic concentration of charge trapping layer by a common method. For example, we calculated the Ge concentration of the SiGeO thin film by below formula:

$$Ge \sim \frac{I_{Ge3d}/S_{Ge3d}}{I_{Si2p}/S_{Si2p} + I_{Ge3d}/S_{Ge3d} + I_{O1s}/S_{O1s}} \qquad (3\text{-}1)$$

The “I” means the peak intensity of element, and “S” the element sensitivity of the ESCA. The atomic concentration of silicon, germanium and oxygen in the charge trapping layer are 32%, 16.8%, and 51.2%. We found that oxygen was successfully incorporated in the charge trapping layer during sputter process.

Before a rapid thermal annealing (RTA) process at 900 ^{o}C for 30sec in the N_2 (sample A) and O_2 (sample B) ambiances respectively, the $Si_{1.33}Ge_{0.67}O_2$ layer must be capped a 20-nm-thick oxide using a plasma enhanced chemical vapor deposition (PECVD) system at 300 ^{o}C (this step was called PACO: pre-annealing-capping-oxide). Here, we considered that the PACO process was a requirement for the use of $Si_{1.33}Ge_{0.67}O_2$ layer as the charge trapping layer and discussed its importance on the performance of NVMs later. The RTA process was performed to cause the

self-assembled effect of Ge nanocrystal in the charge trapping layer. After the RTA process, a 20-nm-thick blocking oxide was deposited by PECVD and then deposited Al gate electrodes to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. Here, the total thickness of blocking oxide included both a 20 nm PACO and a 20 nm PECVD oxide was about 40nm. The formation flow of Ge nanocrystals MOIOS structure is shown in Fig. 3-2. In addition, electrical characteristics of the capacitance-voltage (C-V) hysteresis were measured by the HP4284 precision LCR meter with high frequency of 1 MHz.

3.1.3 Results and Discussion

3.1.3.1 Chemical analyses and formation mechanism of Ge nanocrystals

Figure 3-3(a) shows a cross-sectional TEM image of sample A and presents the Ge nanocrystals embedded in oxide layer containing spherical and separated Ge nanocrystals. However, Fig. 3-3(a) shows a kind of double Ge nanocrystal layer. This is a non-ideal result for our fabrication. If we well-control the content of Ge, the double Ge nanocrystal layer maybe become only single Ge nanocrystal layer. In addition, the average diameter of the nanocrystals is approximately 5-6 nm and the area density of the nanocrystals is estimated to be about 1.73×10^{12} cm^{-2} by TEM analysis.

For the formation of Ge nanocrystals, it was necessary to take into consideration the Gibbs free energy of Si–O and Ge–O at 900°C. Because of the smaller Gibbs free energy of Si–O (-805 kJ mol^{-1}) compared with Ge–O (-666 kJ mol^{-1}) [3.15], the oxygen atoms can interact with the Si atoms easier than with the Ge atoms in the $Si_{1.33}Ge_{0.67}O_2$ layer during the RTA process. This result could be attributed that an internal competition reaction induced the self-assembled effect of Ge nanocrystals in the $Si_{1.33}Ge_{0.67}O_2$ layer, which was dependent on the amount of oxygen of charge trapping layer. The formation mode would be expressed as

$$SiO_x + GeO_x = Ge + SiO_2 \qquad x < 2 \tag{3-2}$$

During the thermal treatment, Si atoms will move and bond with oxygen of GeO_x resulting in the self-assembled effect of Ge nanocrystals. Figure 3-3(b) shows the XPS analysis of Ge 3*d* before and after RTA process. In this Ge 3*d* orbit, the peak is shifted form Ge-O bond (31 eV) to Ge-Ge bond (29 eV) during RTA process.

Figure 3-4(a) shows a cross-sectional TEM of $Si_{1.33}Ge_{0.67}O_2$ thin layer after the RTA process at O_2 ambiance (sample B) and the XPS analysis of charge trapping

layer indicates that only GeO_2 peak (1220 eV) is existed in the Ge 2*p* spectra, as shown in Fig. 3-4(b). This result was different to sample A and it was attributed to the excess oxidation during RTA process at O_2 ambiance. The chemical reaction of formation of GeO_2 nano-dots was expressed as

$$SiO_x + GeO_x = Ge + SiO_2 \qquad x < 2 \xrightarrow{Outside\ \ Oxygen\ \ defusion} Ge + SiO_2 + O_2 = SiO_2 + GeO_2$$

Here, an over-oxidation phenomenon of Ge nanocrystal was to completely form GeO_2 nano-dots embedded in the oxide. Therefore, according these experiment results, the Ge nanocrystals embedded in oxide could be formed at the lower thermal budget (short annealing time) and no use of further high pressure H_2 treatment or steam process in our experimental method. We successfully used this internal competition reaction between the oxygen, silicon and germanium to prevent the over-oxidation phenomenon of Ge nanocrystals in our work.

3.1.3.2 Electrical characteristics of Ge nanocrystals embedded in oxide

Figures 3-5 shows the electrical characteristics of C-V hysteresis under ± 5 gate voltage operation with (a) Ge nanocrystal embedded in oxide (sample A, use of PACO step), (b) GeO_2 nano-dots embedded in oxide (sample B, use of PACO step), and (c) sample A (no use of PACO step). In this case, the memory window for C-V measurement was influenced by PACO process as shown in Fig. 3-5(c), because the Ge atoms of charge trapping layer had out-diffused phenomenon during RTA process by the secondary ion mass spectrometer (SIMS) analysis, as shown in Fig. 3-6 [3.16, 3.17]. In Fig. 3-6, it is found that the counts of Ge signal of "no use of PACO (sample A)" are lower than the sample A. Hence, we must use the PACO step to avoid the Ge atoms out-diffusion and keep higher Ge concentration in the charge trapping layer to get better charge storage ability. From Figs. 3-5(a) and (b), it is found that the memory windows of sample A and sample B exhibit 1.0 and 0.5 V under ± 5 gate voltage

operation, respectively. It is perceived that the hysteresis is counterclockwise, due to injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of Si substrate [3.19]. Moreover, the Ge nanocrystals embedded in oxide presents the superior charge storage ability under ± 10 gate voltage operation, as shown in Fig. 3-5(a). According to the energy band diagrams of Fig. 3-7, we considered that the charge storage ability of semiconductor nanocrystals was decided by the trap density of charge trapping layer. Therefore, except the self-trap of Ge nanocrystals, the surrounding dielectric of nanocrystals also would provide the trap states for the stored charge injection. Due to the better electronic property of Ge nanocrystals embedded in oxide, we would detail to study its programming/erasing characteristics, endurance and retention tests later.

Programming/erasing characteristics of the Ge nanocrystals embedded in oxide under ±5 V gate voltage are shown in Fig. 3-8. The flat band voltage shift is increased as the programming/erasing duration is increased. Moreover, the defined memory window 1.0 V can be obtained at programming/erasing time ~10^{-5} s under ±5 V operation. However, the programming/erasing characteristics were found that the flat band voltage shift shown the saturation phenomenon after programming/erasing time ~10^{-3} s. This result was due to the Coulomb blockade effect that stored charges were existed in nanocrystal and raised the nanocrystal potential to block the other charge injection. Our proposed memory device revealed a high speed programming/erasing time for further nonvolatile memory application.

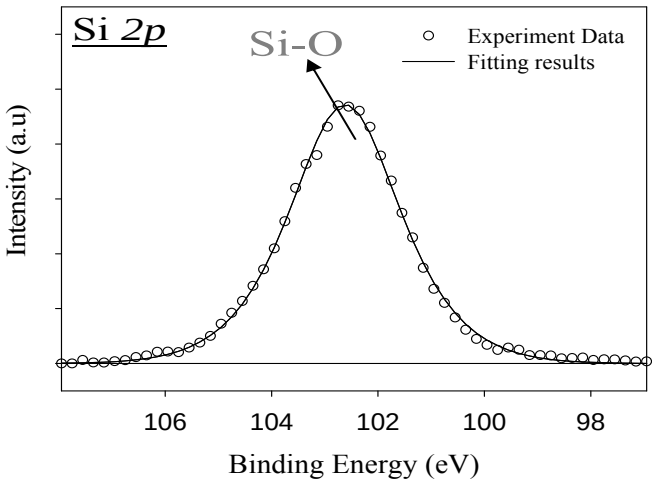
To further investigate the reliability of Ge nanocrystals embedded in oxide, Fig. 3-9 presents the endurance characteristics of Ge nanocrystals embedded in oxide under the pulse conditions of $V_G - V_{FB} = \pm 5$ V for 1 ms. The flat-band voltage can be defined by using the C-V hysteresis under ± 10 gate voltage operation. From Fig. 3-8, it is found that the variation of memory window is stable after 10^6 P/E cycles for

using the $Si_{1.33}Ge_{0.67}O_2$ layer to form the Ge nanocrystals NVMs. Hence, we used the internal competition reaction method which this technique could be fabricated a good high frequency operation of Ge nanocrystal NVM in our research.

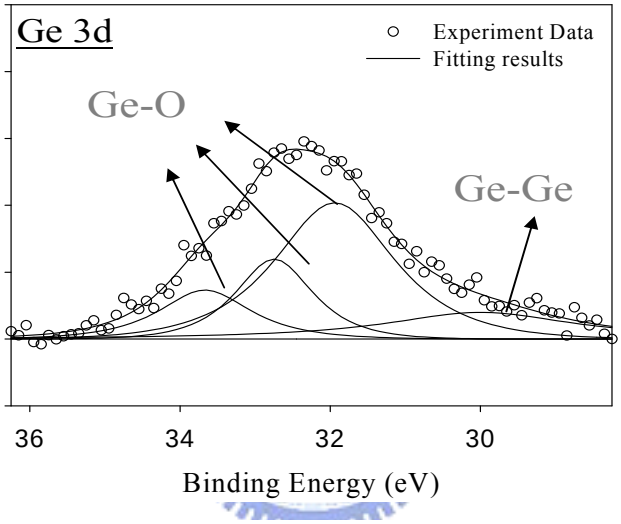
The retention of nonvolatile nanocrystal memory structure with sample A is illustrated in Fig. 3-10. The retention mensuration was performed at room temperature by operating a ± 15 V gate voltage stress for 10 s and measured up to 10^4 sec. The flat band voltage shift ($\triangle V_{fb}$) was obtained by comparing the C-V curves from the charged carries state and quasi-neutral state. We found that the charge holding ratio of Ge nanocrystals embedded in oxide, 25%, after 10ys by analyzing the extrapolation value of retention data (dotted line for program and erase states). Here, the stable charge storage was conserved and the memory window also was retained 1.5V after 10ys. In the previous research, the memory effect for nanocrystals embedded in dielectric is resulted from (1) interface states between the silicon substrate, (2) traps inside the dielectric layer, (3) nanocrystal confined state, and (4) interface states between nanocrystals and the surrounding dielectric. [3.20, 3.21]. The charge retention ability of the deep trap is better than shallow tarp due to lower charge escaping probability for the deep trap. Hence, the rapidly decay in the retention test is due to the charge stored in shallow trap states which is higher energy compared with silicon substrate leading to charges escape to substrate [3.22, 3.23]. This remainder memory window of 1.5 V was enough to define the data information “1” and “0” according by ITRS road map.

3.1.4 Conclusion

In conclusion, we successfully fabricated the Ge nanocrystals embedded in the oxide layer by using the internal competition reaction characteristics of $Si_{1.33}Ge_{0.67}O_2$ thin layer, and cut down thermal budget. The over-oxidation phenomenon of Ge nanocrystals could be prevented through different Gibbs free energies of compounds. The Ge nanocrystals embedded in the oxide layer shown good electronic performance for nonvolatile memory application and we also obtained the good endurance test for our samples. In addition, this fabrication technique can be compatible with current manufacture process of the integrated circuit manufacture.



(a)



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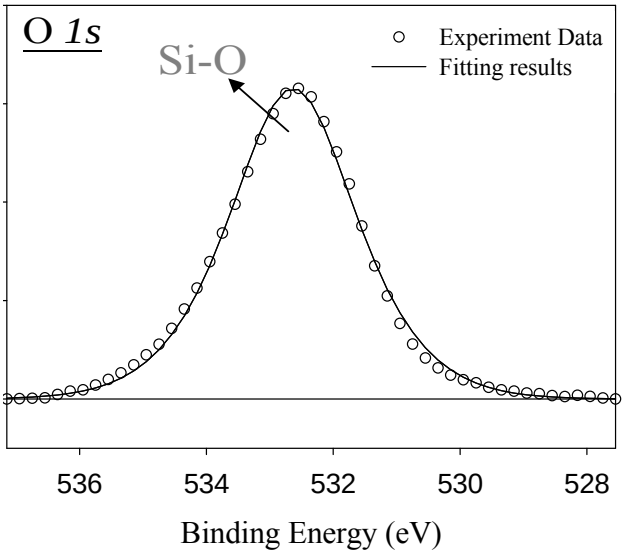


(c)

Figure 3-1 The XPS analysis by using an Al *K*α (1486.6 eV) x-ray radiation is demonstrated the chemical composition of (a) Si 2*p*, (b) Ge 3*d* and (c) O 1*s* core-level spectra.

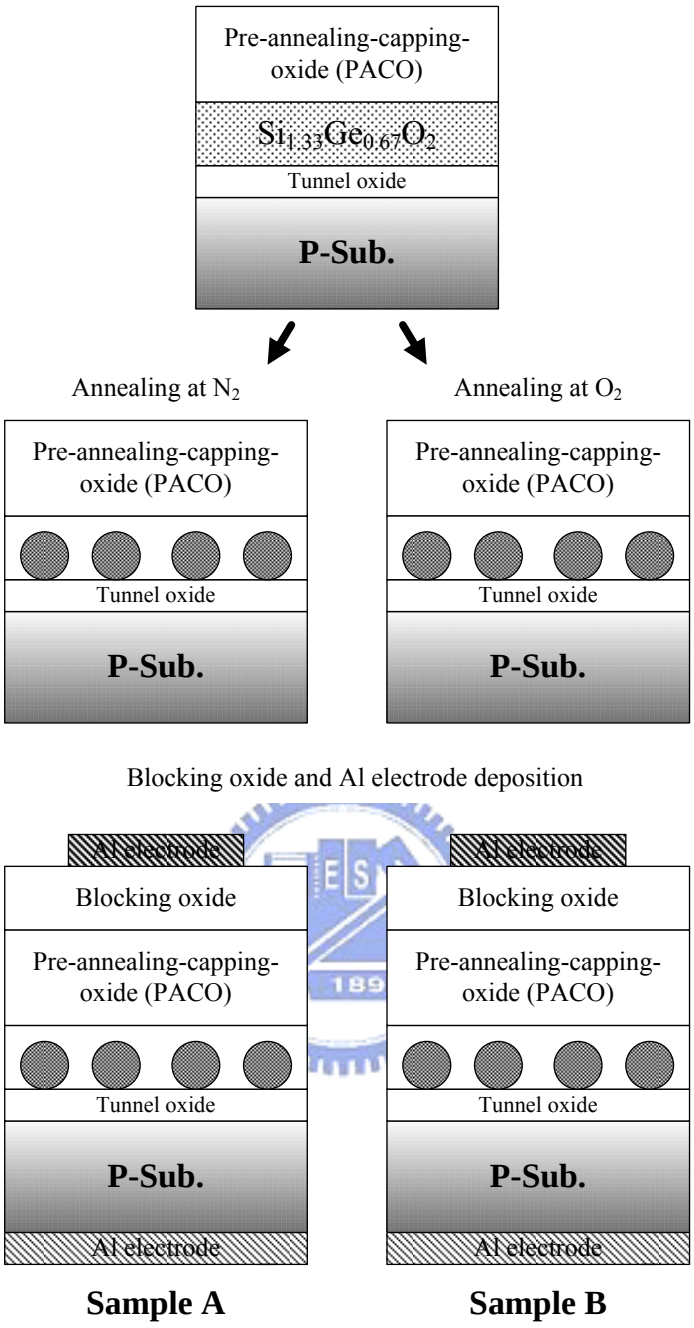


Figure 3-2 Formation flow of Ge nanocrystals MOIOS structure.

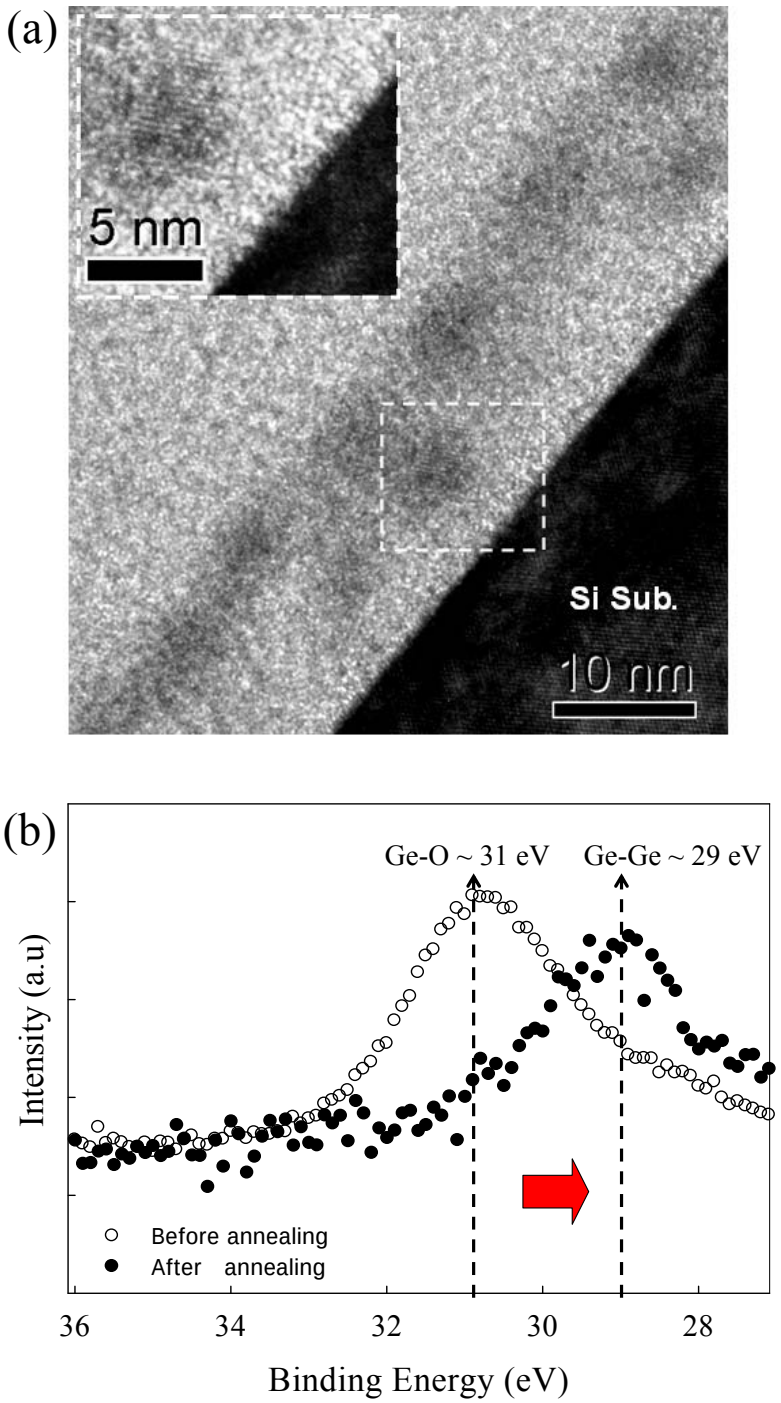


Figure 3-3 (a) Cross-sectional transmission TEM analysis of MOIOS structure with Ge nanocrystal embedded in oxide (the nanocrystals size and density are about 5-6 nm and 1.73×10^{12} cm^{-2}, respectively) and inset is the lattice image of Ge nanocrystal. (b) XPS analysis of the Ge 3*d* core-level spectrum. The Ge-O signal is at about 31 eV shift to lower bonding energy 29 eV which is the Ge-Ge signal peak position after RTA process.

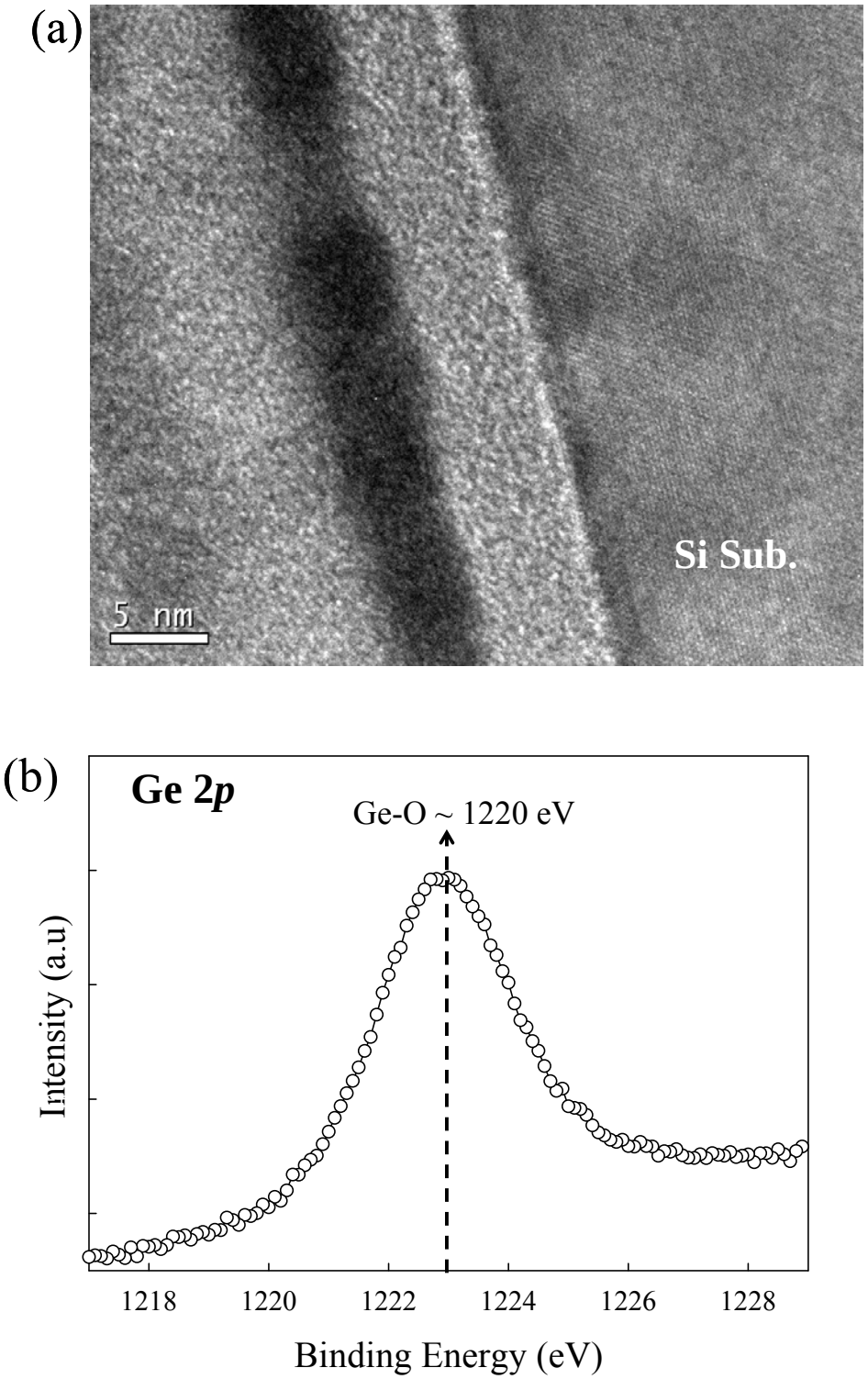


Figure 3-4 (a) Cross-sectional transmission TEM analysis of MOIOS structure with GeO nanocrystal embedded in oxide (the nanocrystals size and density are about 5-6 nm and 4.4×10^{11} cm^{-2}, respectively). (b) XPS analysis of the Ge 2*p* core-level spectrum and the Ge-O signal is at about 1220 eV after RTA process.

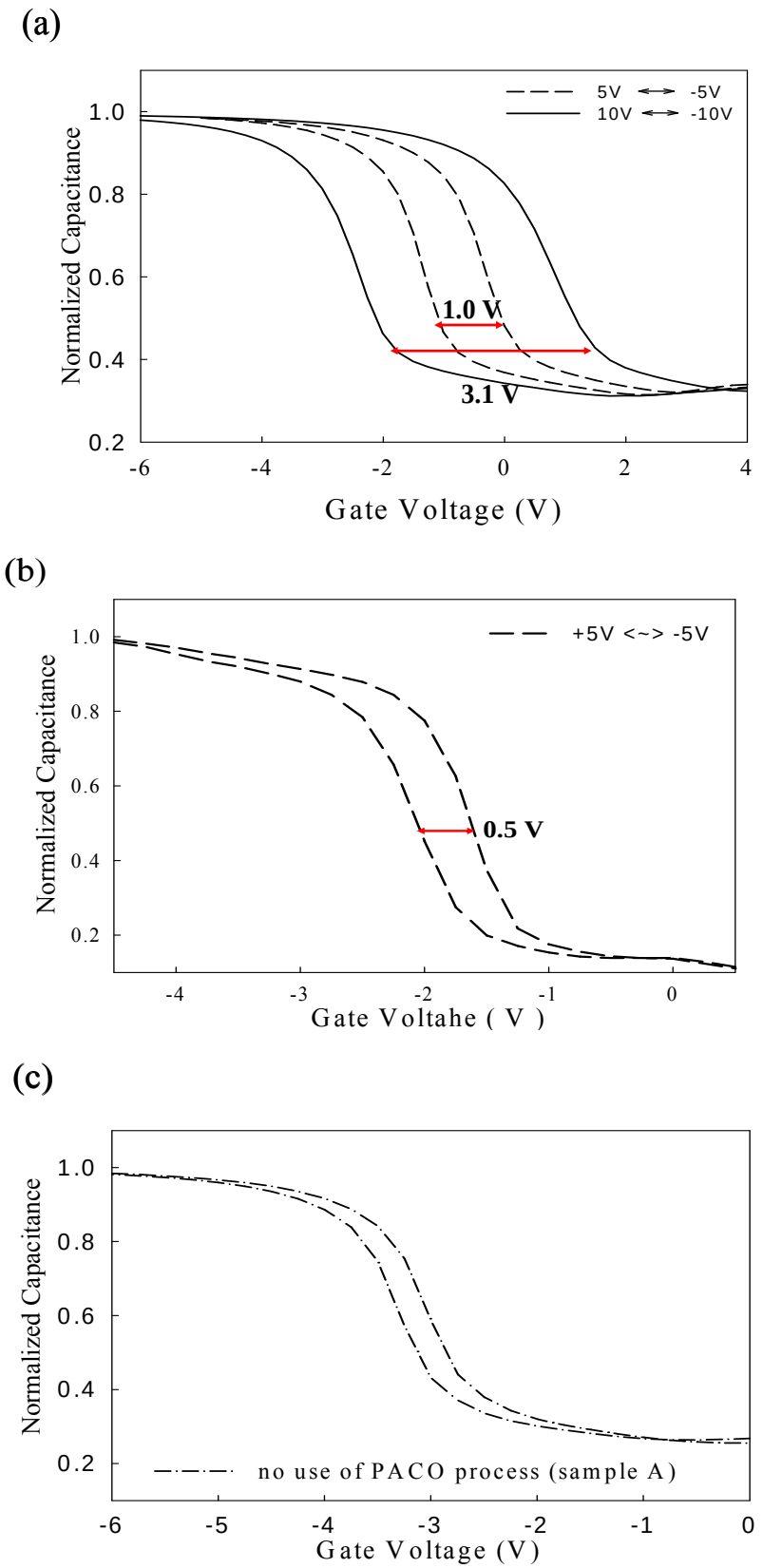


Figure 3-5 Electrical characteristics of C-V hysteresis under ± 5 gate voltage operation with (a) sample A (use of PACO step), (b) sample B (use of PACO step), and (c) sample A (no use of PACO step).

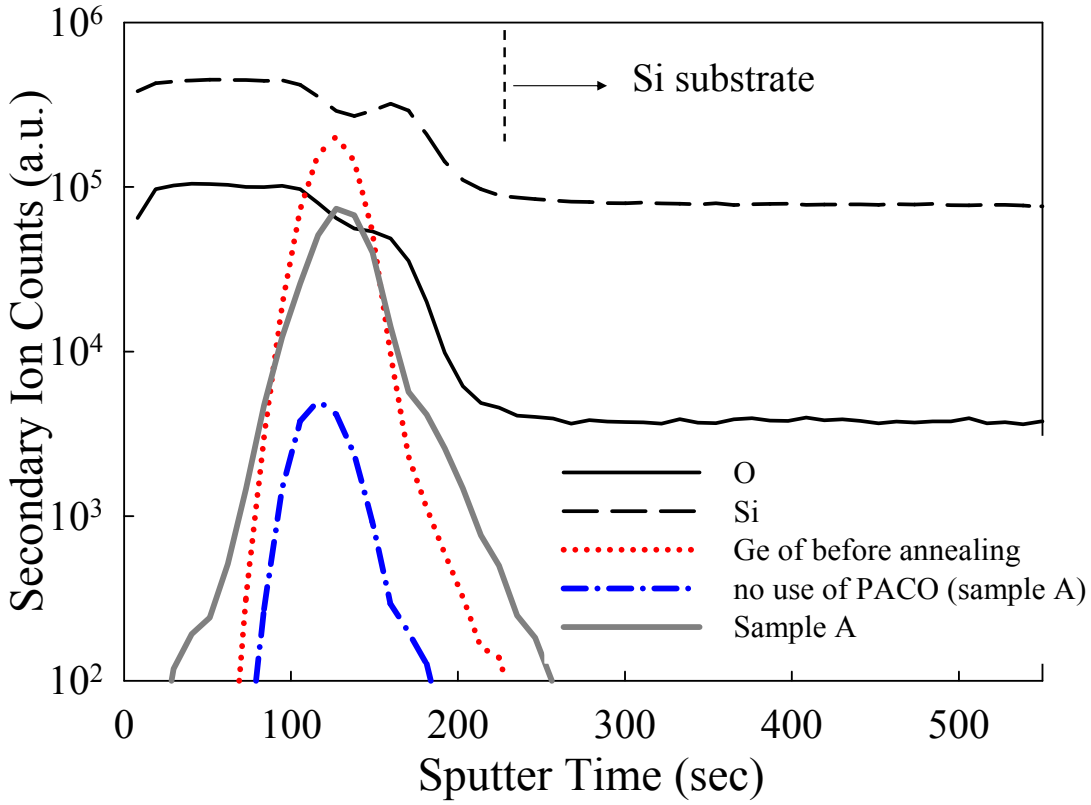


Figure 3-6 Secondary ion mass spectrometer (SIMS) analysis of MOIOS structure with Ge of before annealing, sample A, and no use of PACO (sample A).

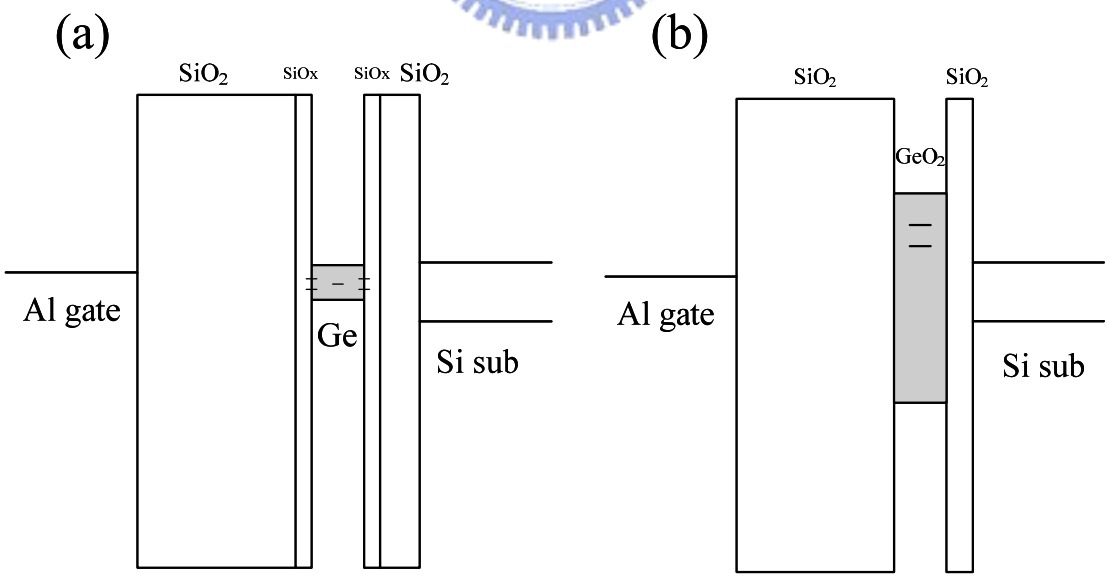


Figure 3-7 Energy band diagrams of (a) sample A and (b) sample B. The band gap of Ge and GeO_2 are 0.6 and 3.92 eV [3.24].

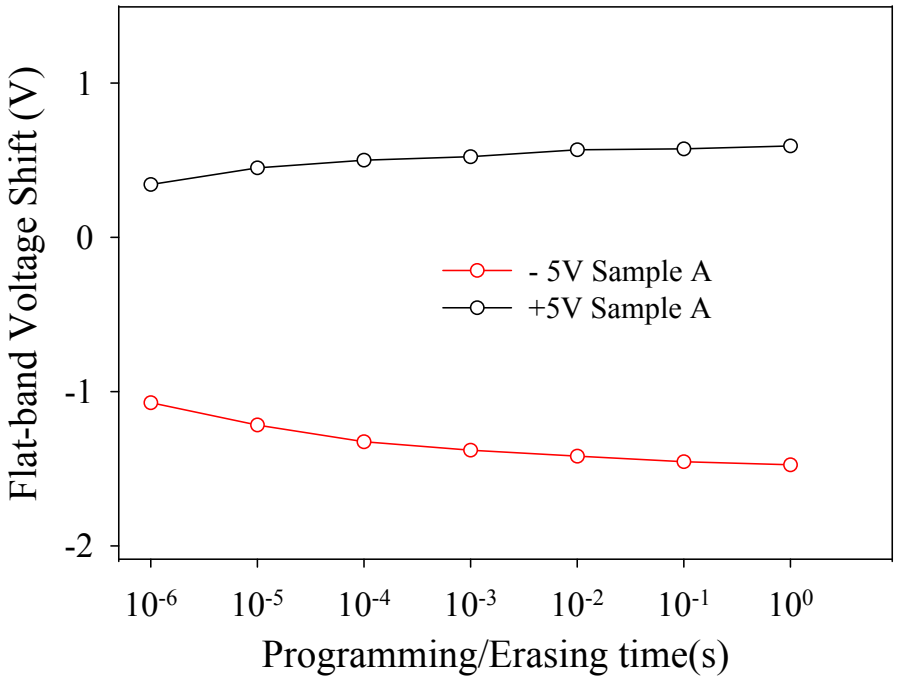


Figure 3-8 Programming and erasing characteristics of the Ge nanocrystals embedded in oxide under ± 5 V gate voltage operation.

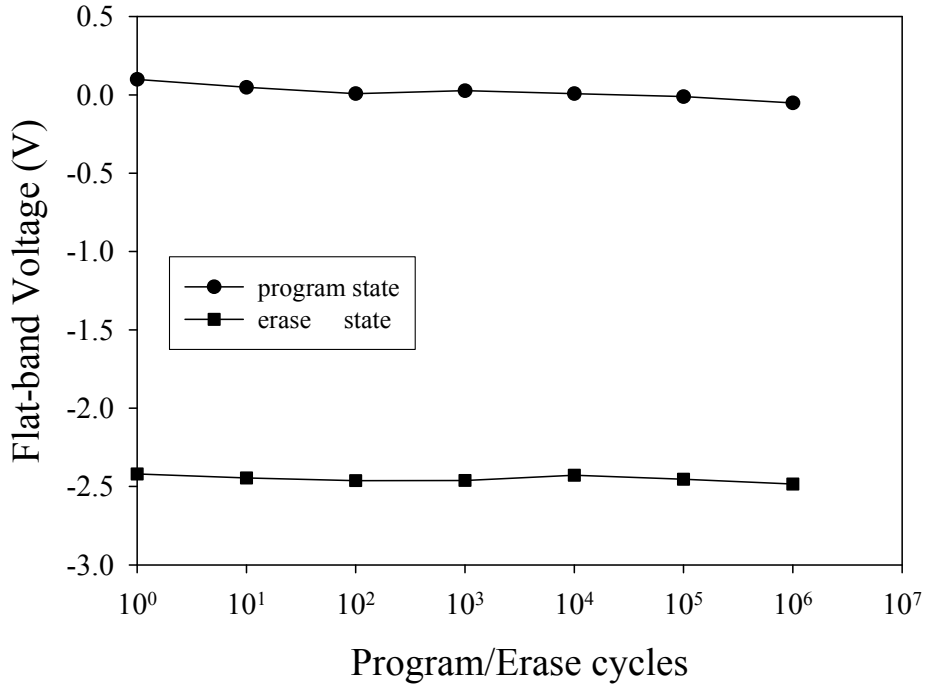


Figure 3-9 Endurance characteristics of Ge nanocrystals embedded in oxide under the pulse conditions of V_G - V_{FB} = ±5 V for 1 ms. The flat-band voltage can be defined by using the C-V hysteresis.

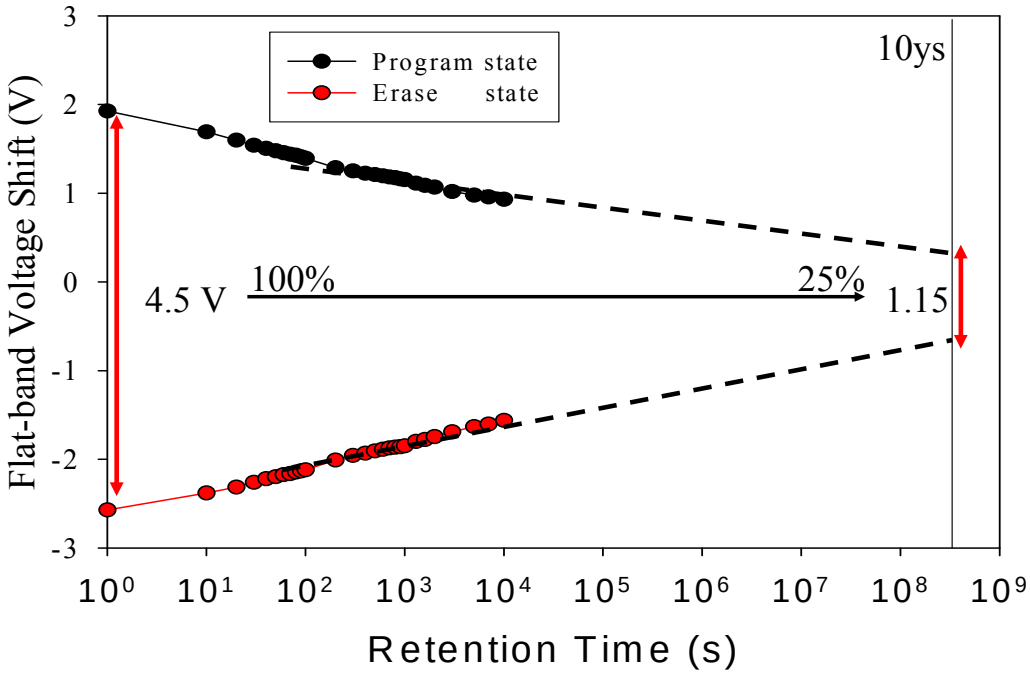


Figure 3-10 Retention time test with Ge nanocrystal embedded in oxide at room temperature operating a ±15 V gate voltage stress for 10 s. The charge holding ratio of is 25% after 10ys.

3.2 Formation and Nonvolatile memory effect of Germanium Nanocrystal embedded in Nitride layer using Silicon-Germanium-Nitride layers

3.2.1 Introduction

As we mentioned at Chapter 1 in the thesis, poly-Si/oxide/nitride/oxide/silicon (SONOS) nonvolatile memory devices have been widely used in the integrated circuit market. The charge storage elements in SONOS memory are the charge traps distributed throughout the volume of the silicon nitride (Si_3N_4) layer. A typical trap density has an amount of the order 10^{18}-10^{19} cm^{-3} according to Yang et al. [3.24] and stores both electrons and holes (positive charge) injected from the silicon channel. In addition, the charge trapping layer also can contain some Si-N bonds which increase trapping states to improve charge storage capacity and program/erase efficiency for the nonvolatile nanocrystal memory devices.

Therefore, base on this high trap density of silicon nitride, some study was reported to fabricate germanium (Ge) nanocrystal embedded in SiNx dielectric [3.25]. The nitride can increase trapping states to improve memory window under electrical operation. Comparing to SONOS and Ge nanocrystals NVMs, a larger memory window can be obtained. When a memory device has a large memory window, it is easier to meet the requirement of 10 years.

In this chapter, the authors proposed a formation mechanism of Ge nanocrystals embedded in the dielectric by using $Si_{2.67}Ge_{1.33}N_2$ thin film for nonvolatile memory application in this study. Because of internal competition reaction, this formation process reduced the thermal budget and eliminated the use of high pressure H_2 treatment or steam process. The metal/oxide/insulator/oxide/silicon capacitor structure with nanocrystals was also studied and exhibited hysteresis characteristics after electrical operation. In addition, the obvious memory window can be used to define

"1" and "0" states at low voltage program operation. Furthermore, good endurance and retention characteristics are exhibited for the Ge nanocrystals embedded in SiN_x structure that compared with the Ge nanocrystals embedded in oxide.

3.2.2 Experiment

Figure 3-11 indicates a schematic of experimental procedure. This nonvolatile memory-cell structure in this study was fabricated on a 4 inches p-type silicon (100) wafer, which had been removed native oxide and particles by RCA process. After a standard RCA clean, a 5-nm-thick tunnel oxide was thermally grown by a dry oxidation process at 950℃ in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Subsequently, a 10-nm-thick nitrogen incorporated $Si_{0.5}Ge_{0.5}$ (SiGeN) layer was deposited on tunnel oxide by reactive sputtering of $Si_{0.5}Ge_{0.5}$ co-mixed target in the Ar/N_2 (24sccm/20sccm) ambiance at room temperature. This step could obtain a $Si_{2.67}Ge_{1.33}N_2$ layer whose the ratio of atoms concentration was analyzed by X-ray photoelectron spectroscopy (XPS). The XPS analysis by using an Al *Kα* (1486.6 eV) x-ray radiation is demonstrated the chemical composition of the charge trapping layer (SiGeN thin layer), as shown in Fig. 3-12.

In order to prevent the Ge to interact with the outside oxygen in the chamber during RTA process, we also used a 20-nm-thick PACO process on the trapping layer before RTA. After that, we annealed the sample by RTA at 900℃ for 60sec in pure N_2 ambiance. The RTA process was performed to cause the self-assembled of Ge nanocrystal in the charge trapping layer. After RTA process, a 20-nm-thick blocking oxide was deposited by PECVD at 300℃. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. Electrical characteristics, including the capacitance-voltage (C-V) hysteresis, current density-voltage (J-V),

retention, and endurance characteristics, were also performed. The J-V and C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency 1 MHz.

3.2.3 Results and Discussions

According to the previous experiment results at **Chapter 3.1**, we also used the internal competition reaction for the $Si_{2.67}Ge_{1.33}N_2$ layer to form Ge nanocrystals embedded in SiN_x (the Gibbs free energy of Si-N is about -470 kJ mol^{-1}) [3.26], as shown in the cross-sectional TEM image of Fig. 3-13. The average diameter of the nanocrystals is approximately 7-8 nm and the area density of the nanocrystals is estimated to be about 1.12×10^{12} cm^{-2} by TEM analysis. In addition, the charge trapping layer contained SiN_x matrix between the Ge nanocrystals and tunnel oxide which this part would increase trapping states to improve charge storage capacity.

Figure 3-14 shows the electrical characteristics of C-V hysteresis under ± 10 gate voltage operations with (1) Ge nanocrystal embedded in oxide and (2) Ge nanocrystal embedded in SiN_x. From Fig. 3-14, it is found that the memory windows of (1) and (2) exhibit 3.1 and 3.75 V, respectively. Due to the electronic property of SiN_x (e.g. high dielectric constant and additional trapping states), the structure (2) has better charge efficiency than structure (1). Moreover, Fig. 3-15 shows the programming/erasing characteristics of the Ge nanocrystals embedded in oxide (1) and nitride (2) under ±5 V gate voltage. The flat band voltage shift is increased as the programming/erasing duration is increased. Moreover, the defined memory window 1.0 V can be obtained at programming/erasing time ~10^{-5} s under ±5 V operation. The programming/erasing characteristics were found that the charge trapping layer contains SiN_x matrix would improve charge storage capacity and programming/erasing efficiency by the higher

dielectric constant of nitride than oxide. Our proposed memory device reveals a high speed programming/erasing time for further nonvolatile memory application. Due to the electronic property of SiN_x (e.g. high dielectric constant and additional trapping states), the structure (2) has better charge efficiency than structure (1).

These electrical results could be explained by our proposed energy band diagrams, as shown in Fig. 3-16. Figures 3-16(a) and (b) illustrate the energy band diagram of two different Ge nanocrystals structure; (a) Ge nanocrystals embedded in SiO_x and (b) Ge nanocrystals embedded in SiN_x. We found that the charge trapping centers of the structure (b) were not only the interface states between the nanocrystals and surrounding dielectric but also the inside traps of SiN_x dielectric layer. Because the SiN_x supplied the additional accessible charge trap states, the Ge nanocrystals embedded in SiN_x structure shown the larger memory window than the Ge nanocrystals embedded in SiO_x. We thought that the Ge nanocrystals embedded in SiN_x NVM structure was combined the nanocrystal with SONOS structure. Hence, we also used the internal competition reaction method for the $Si_{2.67}Ge_{1.33}N_2$ layer to successfully fabricate SONOS-type Ge nanocrystals NVM.

To further compare the reliability of Ge nanocrystal embedded in oxide and nitride, the retention of Ge nanocrystals nonvolatile memory structure are illustrated in Fig. 3-17. The retention mensuration was performed at room temperature by operating a ±15 V gate voltage stress for 10 s and measured up to 10^4 sec. The flat band voltage shift ($\triangle V_{fb}$) was obtained by comparing the C-V curves from the charged carries state and quasi-neutral state. We find that the charge holding ratio of structure (b), 33%, is better than structure (a), 25%, after 10ys by analyzing the extrapolation value of retention data. Because structure (b) provided trapping states of SiN_x for charging carries, this result could reduce the Coulomb blockade effect of charge trapping layer leading to the lower tunneling probability between the tunnel

oxide and conduction channel under retention state [3.27]. We also verified this point form the current density with gate voltage (0 →+10 V and 0 → -10 V) analysis, as shown in Fig. 3-18. The current density of Ge nanocrystals embedded in nitride is smaller than Ge nanocrystals embedded in oxide, which was attributed to the stored charges to build a Coulomb repulsive force and to block the charge transportation, i.e. this Coulomb repulsive force also prevented the charge loss under retention state when the stored charges was existed in SiN_x. Hence, the Ge nanocrystals combined with SiN_x matrix would improve the performance of nonvolatile nanocrystal memory in terms of retention operation in our investigation.

Figures 3-19(a) and (b) present the endurance characteristics of Ge nanocrystals embedded in oxide and nitride under the pulse conditions of $V_G - V_{FB} = \pm 5$ V for 1 ms. The flat-band voltage can be defined by using the C-V hysteresis under ± 10 gate voltage operation. From Fig. 3-19, it is found that the variation of memory window is stable after 10^6 P/E cycles for using the $Si_{1.33}Ge_{0.67}O_2$ and $Si_{2.67}Ge_{1.33}N_2$ layer to form the Ge nanocrystals NVMs. Hence, we used the internal competition reaction method which this technique could be fabricated the good reliability of NVM in our research.

3.2.4 Conclusions

In conclusion, we successfully fabricated the Ge nanocrystals embedded in the dielectric by using the internal competition reaction characteristics of $Si_{1.33}Ge_{0.67}O_2$ and $Si_{2.67}Ge_{1.33}N_2$, and cut down thermal budget. The over-oxidation phenomenon of Ge nanocrystals could be prevented through different Gibbs free energies of compounds. The Ge nanocrystals combined with SiN_x matrix shown better electronic performance for nonvolatile memory application and we also obtained the good endurance test for our samples. In addition, this fabrication technique can be compatible with current manufacture process of the integrated circuit manufacture.

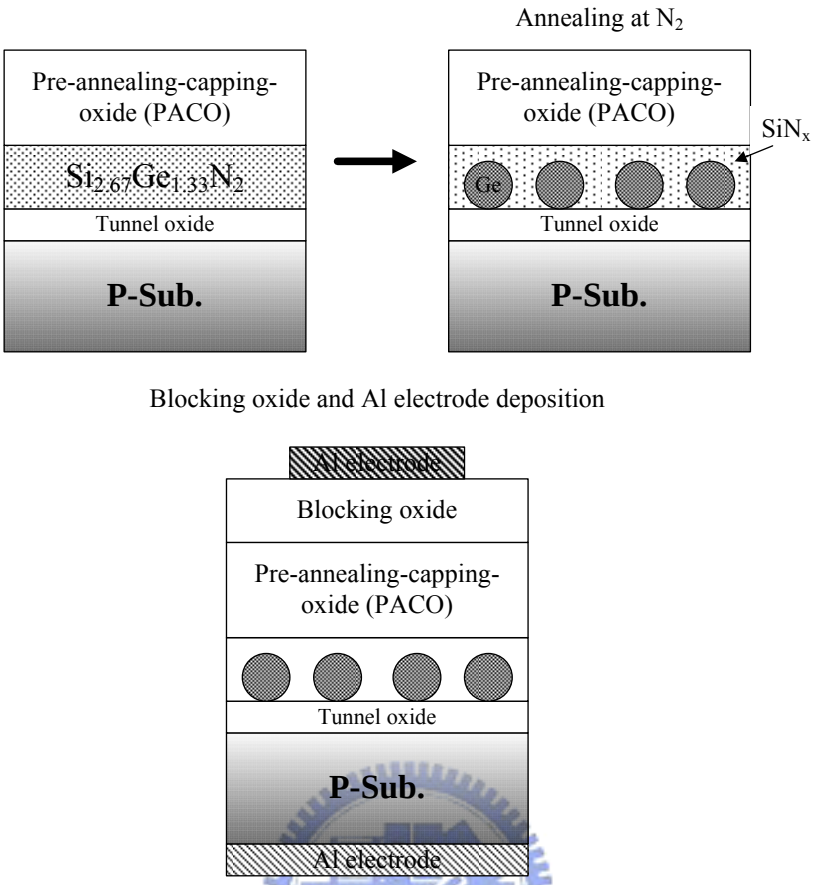
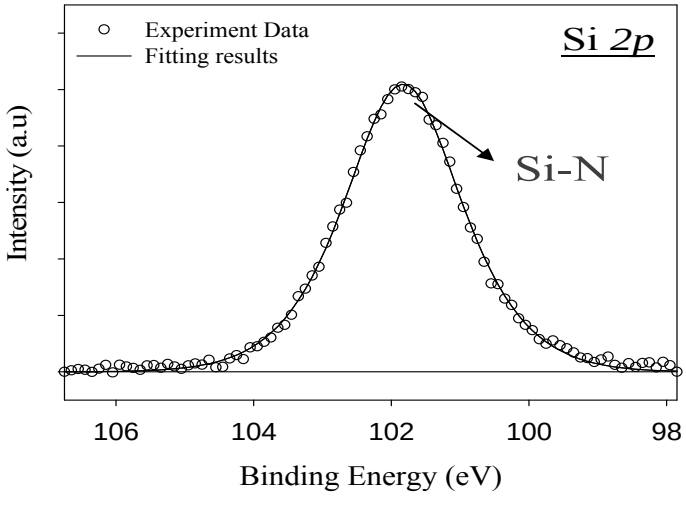
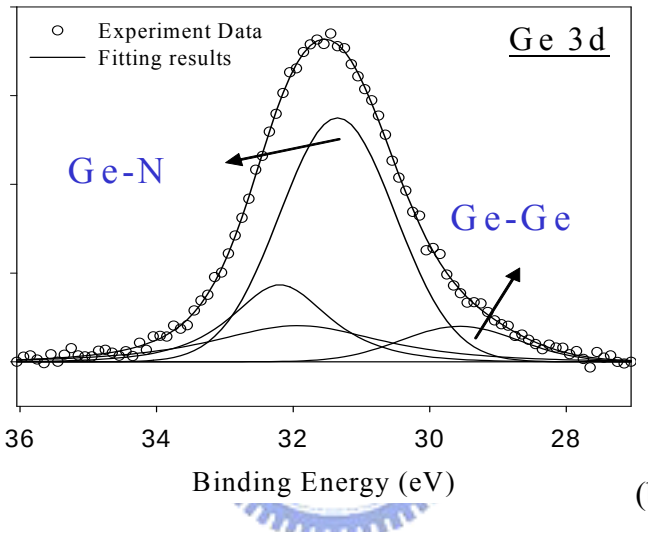


Figure 3-11 Formation flow of Ge nanocrystals embedded in SiN_x MOIOS structure.



(a)



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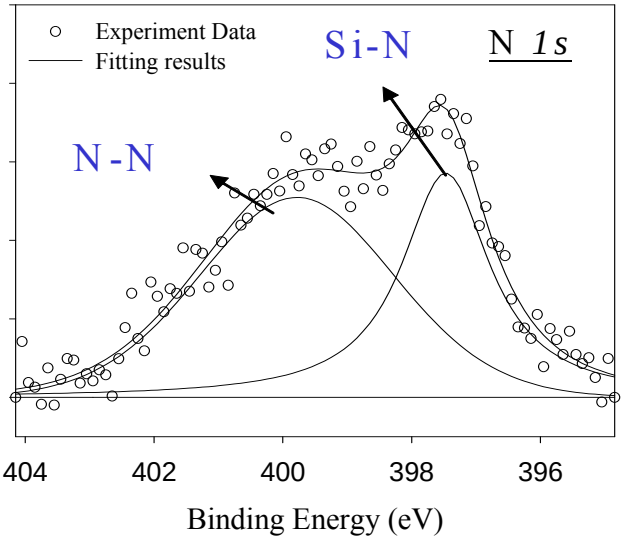


(c)

Figure 3-12 XPS analysis by using an Al *Kα* (1486.6 eV) x-ray radiation is demonstrated the chemical composition of (a) Si 2*p* , (b) Ge 3*d* and (c) N 1*s* core-level spectra for $Si_{2.67}Ge_{1.33}N_2$ thin layer.

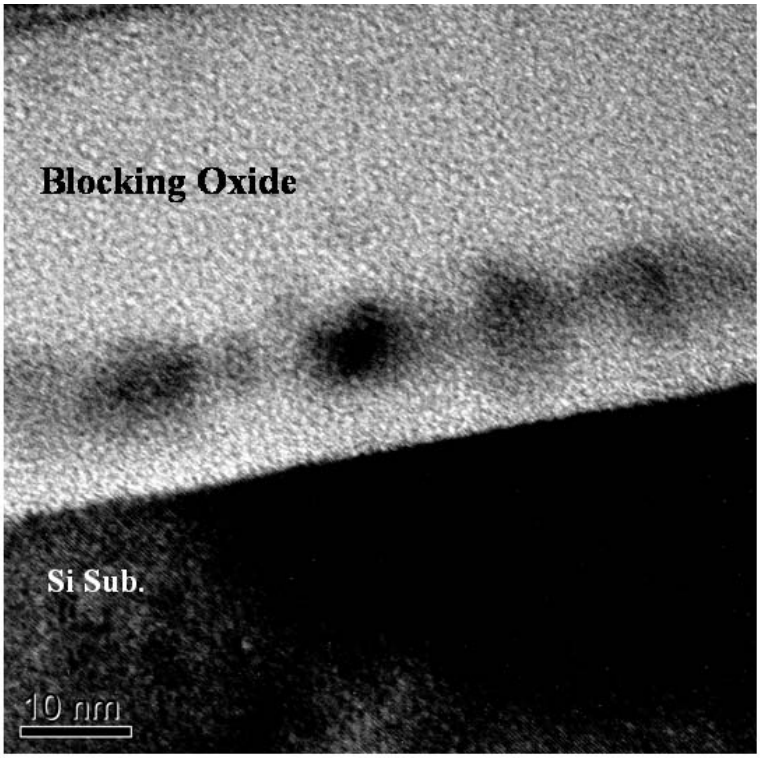


Figure 3-13 Cross-sectional transmission TEM analysis of MOIOS structure with Ge nanocrystal embedded in SiN_x (the nanocrystals size and density are about 7-8 nm and 1.12×10^{12} cm^{-2}, respectively)

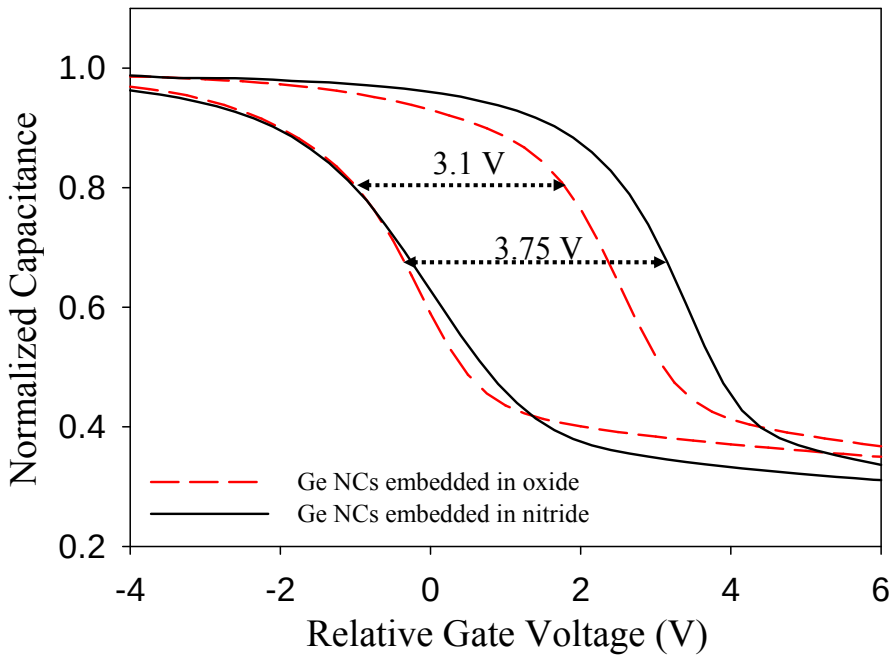


Figure 3-14 Electrical characteristics of C-V hysteresis under ± 10 gate voltage operation with Ge nanocrystals embedded in oxide and nitride.

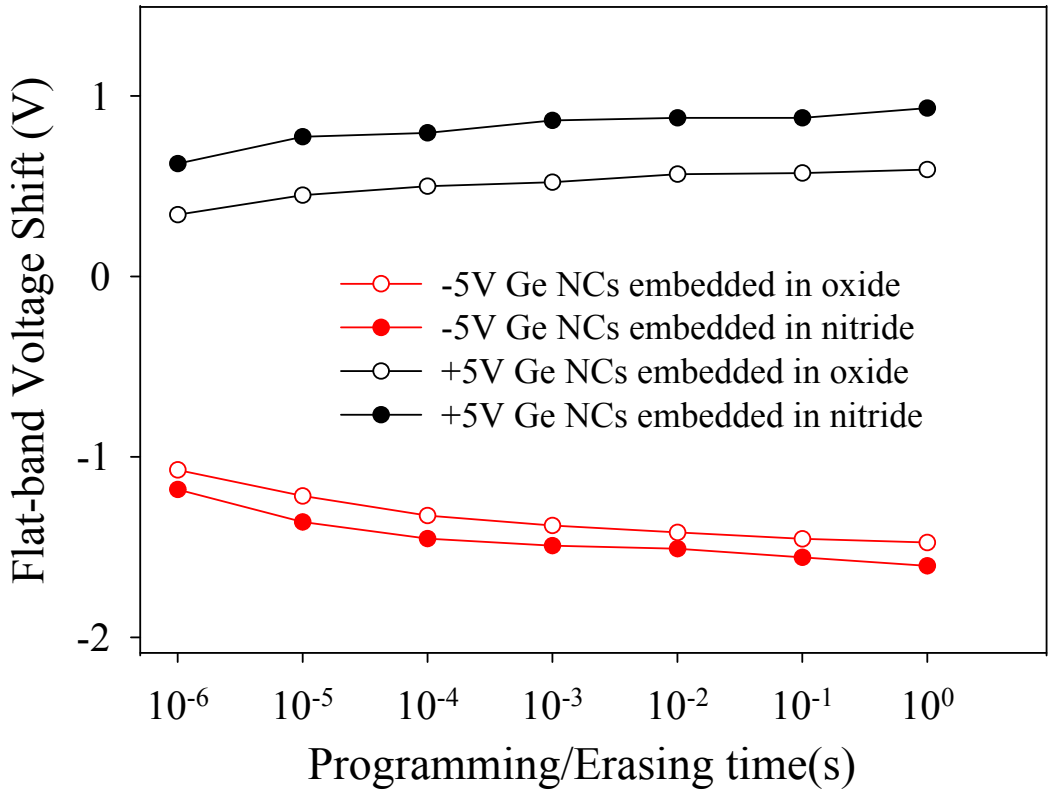


Figure 3-15 Programming and erasing characteristics of the Ge nanocrystals embedded in oxide and nitride under ± 5 V gate voltage operation.

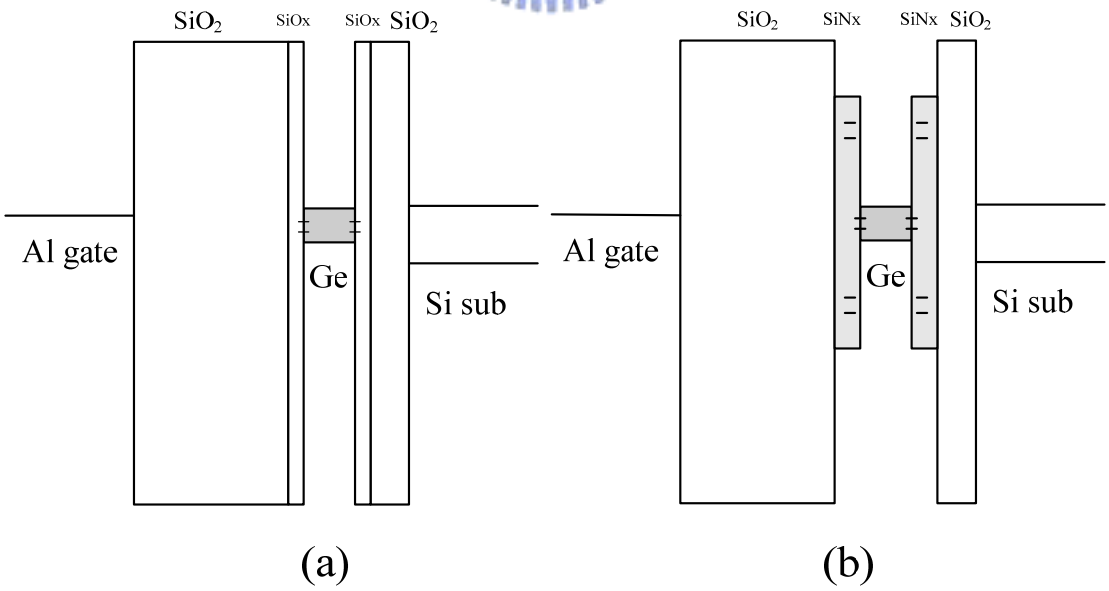
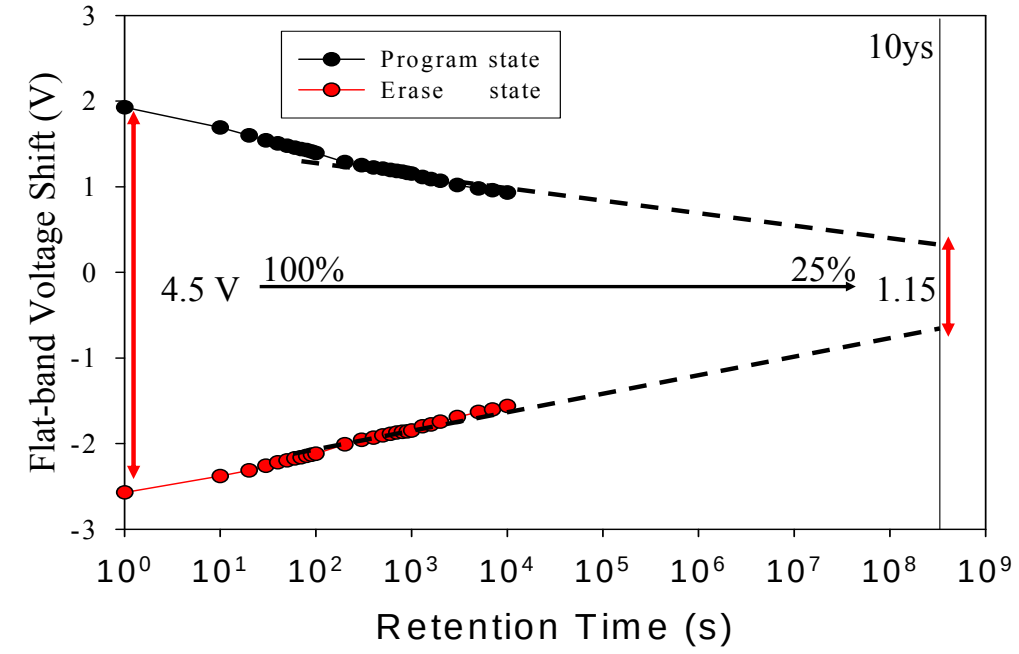


Figure 3-16 Energy band diagrams of Ge nanocrystals embedded in (a) oxide and (b) nitride. The band gap of Ge and SiN_x are 0.6 and 5.1 eV. The trap level of SiN_x below the conduction band energy of SiN_x is about 0.8 – 1.5 eV.

(a)



(b)

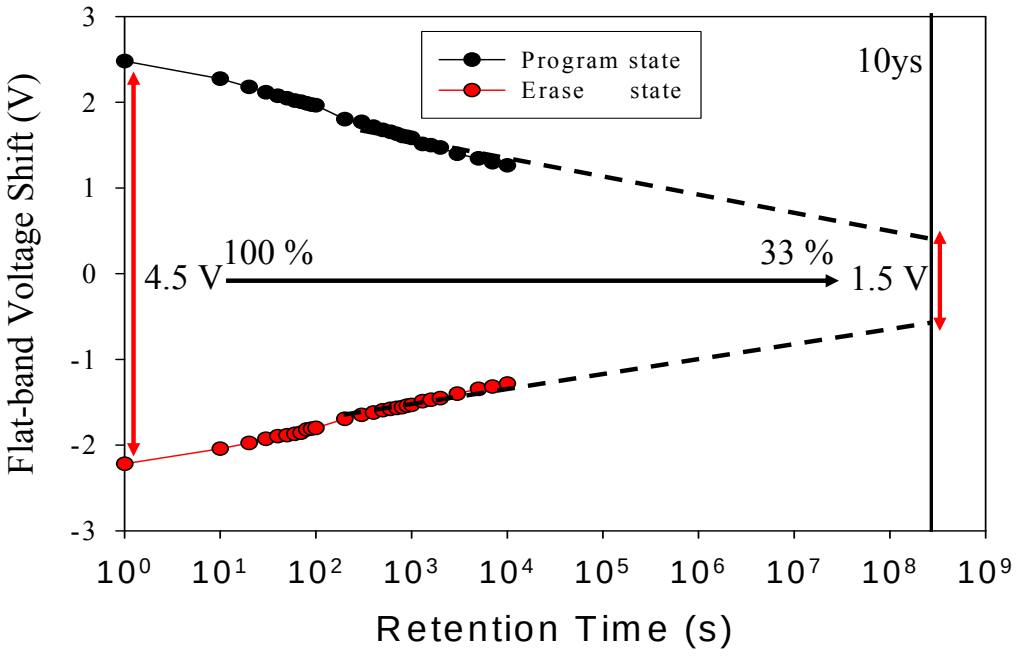


Figure 3-17 Retention time test with Ge nanocrystal embedded in (a) oxide and (b) nitride at room temperature operating a ±15 V gate voltage stress for 10 s. The charge holding ratio of are 25% and 33% for the Ge nanocrystal embedded in (a) oxide and (b) nitride after 10ys, respectively.

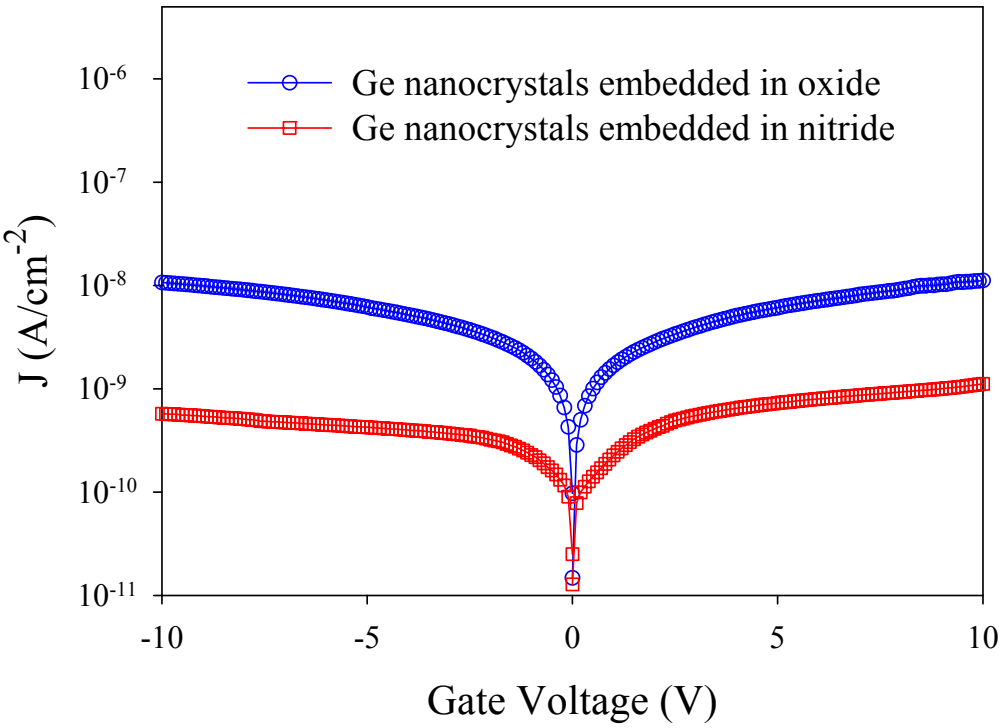


Figure 3-18 Current density-gate voltage (J-V) of Ge nanocrystals embedded in oxide and nitride.

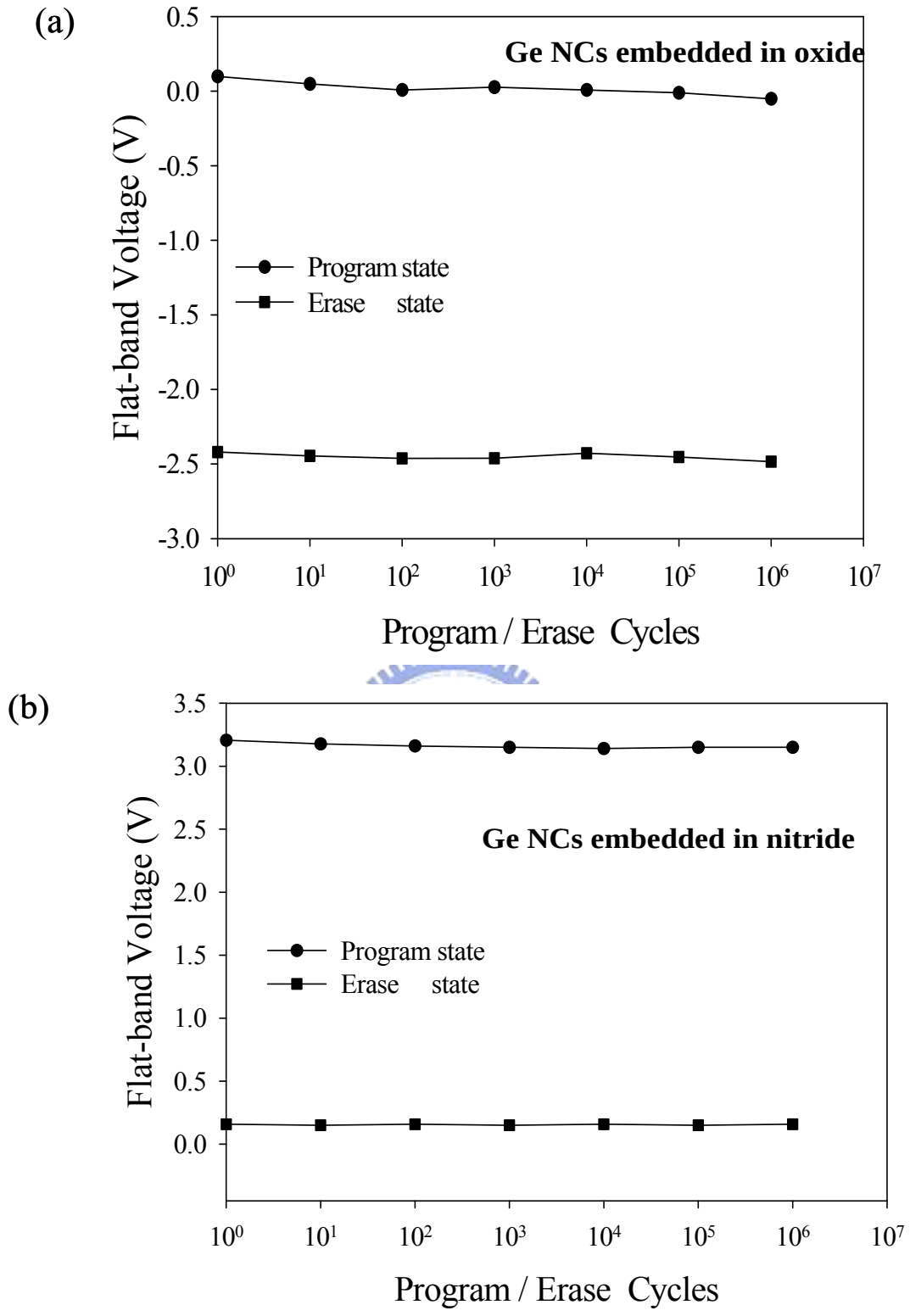


Figure 3-19 Endurance characteristics of Ge nanocrystals embedded in (a) oxide and (b) nitride under the pulse conditions of V_G - V_{FB} = ±5 V for 1 ms. The flat-band voltage can be defined by using the C-V hysteresis.

Chapter 4

Ni-silicide Nanocrystals Nonvolatile Memories

4.1 Electrical Characteristics of Nonvolatile Nickel-Oxygen-Silicon (Ni-O-Si) Nanocrystals memory

4.1.1 Introduction

Nonvolatile memory (NVM) plays an important role in the market of portable electronic products and is required further possessing the high memory capacity, low-voltage and high-speed operation for next-generation memory with scaling down devices [4.1-4.3]. However, the carriers will run out of the floating gate since the tunnel oxide of conventional NVM generates leakage paths during endurance test. Therefore, the tunnel oxide thickness is difficult to scale down in terms of charge retention and endurance characteristics. The nonvolatile nanocrystal memory devices are promising to substitute for the conventional floating gate memory, because the discrete traps as the charge storage media have been reported that they can effectively avoid data loss under reliability test for the scaling down devices [4.4, 4.5]. Among various nanocrystals for memory technology, the metallic nanocrystals were extensively investigated over semiconductor nanocrystals, because of several benefits, such as enhanced gate control ability (i.e., stronger coupling with the conduction channel), higher density of states (DOS), smaller energy disturbance and larger work function (faster programming time and better data retention) [4.5, 4.6]. A nonvolatile memory device for various metal nanocrystals has been formed by several experiment techniques, for instance, self-assembled of tungsten (W) nanocrystal by using thermal oxidation process [4.7], separation of nickel (Ni) or gold (Au) nanocrystal by direct thermal annealing [4.8, 4.9], formation of platinum (Pt) or cobalt (Co) nanocrystal by

using molecular beam epitaxy (MBE) [4.10, 4.11].

In recent years, nickel silicide has been widely used in advanced CMOS device as contact and interconnection materials. The larger work function of nickel silicide is ~5 eV within the silicon band gap which enhances better retention. Most important of all, nickel silicide can be formed at low temperature annealing [4.12]. As a result of those advantages, nickel silicide is chosen as the storage material of memory device. Its implementation is compatible with the current manufacturing technology of semiconductor industry and represents a viable candidate for nonvolatile memory application.

Some methods have been developed recently for the preparation of Ni-Silicide metal nanocrystal nonvolatile memory. Such as, Yeh *et al.* fabricated of $NiSi_2$ nanocrystals embedded in SiO_2 with memory effect by oxidation of the amorphous $Si/Ni/SiO_2$ structure [4.13]. However, the formation of nanocrystals needs thermal oxidation process at high temperature 900 °C for a long duration. Chen *et al.* present the stacked Ni-Silicide nanocrystal memory was fabricated by sputtering a co-mix target ($Ni_{0.3}Si_{0.7}$) followed by RTO process [4.14]. Due to Ni atoms diffusing during the RTO process, the position and distribution of Ni silicide nanocrystals is random and uncontrollable.

The composition of deposited Ni silicide film was the critical process to determine the result of the size of the nanocrystals. In order to control thickness of the thin film more easily, a novel material target of sputter-deposited was used as the source of Ni silicide film. In the present research, the Ni-Silicide (Ni_xSi_{1-x}) was widely studied using co-sputtering method (two targets used). However, it is difficult to uniformly control the component of the deposited Ni silicide thin film. The component of the film Ni_xSi_{1-x} can be well controlled using a co-mix target with a fixed component ratio. The target is manufactured by powder of Nickel (30%)-Silicon

(70%) and it is compressed directly, not sintering. Atoms of this target do not interconnect so that it could use to deposit a fixed ratio film under low power operation.

In this thesis, we introduced oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer as charge trapping layer by sputtering a commixed target ($Ni_{0.3}Si_{0.7}$) in the argon (Ar) and oxygen (O_2) environment at room temperature. The purpose to initially incorporate oxygen in $Ni_{0.3}Si_{0.7}$ layer is to reduce the temperature and duration of thermal treatment for nanocrystal formation. In addition, the distribution of Ni silicide nanocrystals can be well controlled without Ni atoms diffusing during thermal oxidation.

4.1.2 Experiment

This nonvolatile memory-cell structure in this section was fabricated on a 4 in. p-type silicon (100) wafer. After a Radio Corporation of America (RCA) standard clean process which removed native oxide and micro-particles form wafer surface, 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process at 950^{o}C in an atmospheric pressure chemical vapor deposition furnace. Afterward, a 10-nm-thick charge tapping layer was deposited by reactive sputtering (metallic mode) with the 4 in. $Ni_{0.3}Si_{0.7}$ commixed target in the Ar/O_2 [24/2 SCCM (SCCM denotes cubic centimeter per minute at STP)] ambiance at room temperature. The direct current (DC) sputtering power and pressure of sputter system were set to 80 W (the deposition rate ~ 0.2 Å/sec) and 7 mtorr. During the foregoing process, nanocrystals could be found to precipitate and embed in SiO_x layer because of the competition of oxygen between silicon and nickel in the oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer (we discuss this formation mechanism of nanocrystals later). Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition system at 300^{o}C. Al gate electrodes were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. Figure 4-1 shows the formation flow of nanocrystals embedded in oxide. Transmission electron microscope (TEM) analysis and X-ray photoelectron spectroscopy (XPS) were adopted for microstructure and chemical material analysis of nanocrystals. Electrical characteristics of the capacitance-voltage (C-V) hysteresis were also measured by HP4284 Precision LCR Meter with high frequency 100 kHz. Moreover, we fabricated an oxygen deficient $Ni_{0.3}Si_{0.7}$ layer which only used Ar (24 SCCM) during sputter process as charge trapping layer of MOIOS structure (control sample, as shown in Fig. 4-2) to compare with the above-mentioned MOIOS structure for electrical characteristics of C-V.

4.1.3 Results and Discussion

Figure 4-3(a) shows a cross-sectional TEM image of control sample. It was found that a uniform $Ni_{0.3}Si_{0.7}$ layer was deposited on the tunnel oxide and the thickness of the $Ni_{0.3}Si_{0.7}$ layer was about 10-11 nm. However, the cross-sectional TEM image of MOIOS structure containing spherical and separated nanocrystals was shown in Fig. 4-3(b). It is found that the thickness of tunnel oxide is larger than 3 nm by TEM analysis, since this redundant SiO_x matrix is formed form oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer during sputter process. From TEM analysis, the average diameter of the nanocrystals is approximately 5-6 nm and the area density of the nanocrystals is estimated to be about 1.33×10^{12} cm^{-2}.

Capacitance-voltage (C-V) hysteresis is shown in Figs. 4-4(a) and (b) for the control sample and nanocrystals, respectively. From Fig. 4-4(a), nonvolatile memory effect is not found in the control sample under ± 10 V gate voltage operation. On the contrary, it is clearly observed that a 0.8 V and a 2.5 V of memory windows can be obtained, respectively, under ±10 V and ±15 V gate voltage operation for the MOIOS structure with nanocrystals, as shown in Fig.4-4(b). Hence, it is considered that the memory effect of nanocrystals is dominated by formation of nanocrystals as compared with Fig. 4-4(a). Moreover, the hysteresis loops follow the counterclockwise due to injection of electrons from the inversion state and discharge of electrons from the accumulation state of Si substrate. The memory window of MOIOS with nanocrystals is enough to determine data information by different memory window for nonvolatile memory application. As a result, our electrical characteristics of C-V show that formation and nonvolatile memory effect of nanocrystals are influenced by oxygen doping during sputter process.

In our work, the chemical composition of the nanocrystals is demonstrated by

XPS analysis using an Al *K*α (1486.6 eV) x-ray radiation, as shown in Fig. 4-5. Figure 4-5(a) exhibits the XPS Ni 2*p* core-level photoemission spectra that consist of two main peaks, Ni $2p_{3/2}$ and satellite. According to previous research [4.15, 4.16], the composition of Ni $2p_{3/2}$ peak can be separated out Ni-O-Si (854.6 eV) and Ni_2O_3 (856.8 eV) by fitting results of XPS analysis [4.17]. The nanocrystal is thereby believed to be composed of Ni-O-Si ternary element. Moreover, the XPS O 1*s* photoemission spectra can be utilized to verify this contention, as shown in Fig. 4-5(b). By fitting result of experiment data, it is found that the main peak can be composed into two components which center at 531.5 eV and 532.4 eV corresponding to Ni-O-Si bond and Si-O-Si bond, respectively [4.16]. In addition, we can use XPS analysis to evaluate the atomic concentration in the trapping layer, which is 14%, 47%, and 39% for nickel, silicon, and oxygen of charge trapping layer, respectively.

For the formation of Ni-O-Si nanocrystals during sputter process, the enthalpies ($-\Delta H$) of Si-O, Ni-O and Ni-Si at room temperature, are 799, 382 and 318 kJ mol^{-1}, respectively [4.18]. Because of the higher enthalpy of Si-O compared with Ni-O, the oxygen radicals can interact with Si atom easier than with Ni atom on the wafer surface during the sputter process. It can be explained that an internal oxidation reaction will induce self-assembled phenomenon of Ni-O-Si nanocrystals, which is dependent on the different enthalpies of compounds of charge trapping layer. Therefore, Ni-O-Si nanocrystals would be formed at low temperature during our fabrication process and no need of further thermal annealing in our experimental method.

Figure 4-6(a) demonstrates the data retention characteristics of the nonvolatile NiOSi nanocrystals memory at room temperature. The memory cell is programmed by 10 V, 5 s, and erased -10 V, 5 s. The flat band voltage shift is obtained by comparing the *C-V* curves from a charged state and the quasi-neutral state. The memory window

significantly decays during the first 100 s due to charge emission from the shallow traps in SiO_x matrix (surrounding dielectric of nanocrystals) to the substrate. However, a 1.4 V memory window (charge remained ratio of 50%) can be obtained even after 10 years by analyzing the extrapolation value of retention data (stable range, 10^2~$4x10^4$ sec).

Figure 4-6(b) shows the programming/erasing characteristics of NiOSi nanocrystals under ±10 V and ±15 V. The flat band voltage shift is increased as the programming/erasing voltage increased at the same programming/erasing duration, and also increased with the increasing programming/erasing duration at the same programming/erasing voltage. Moreover, the defined window 0.5 V can be obtained at programming/erasing ~10^{-4} s under ±10 V operation. This memory device reveals a high speed programming/erasing time for further nonvolatile memory application.

We also tested the endurance of Ni-O-Si nanocrystals nonvolatile memory under pulses condition of V_G-V_{FB} = ± 5 V for 0.1 ms, as shown in Fig. 4-7. The obvious closure of voltage window between the program and erase state results from degradation of SiO_x dielectric. It was also believed that the SiO_x quality was much worse than the tunnel oxide. The defect generation under frequent P/E operation would increase leakage paths and degrade the charge storage capability. However, it retains a memory window of 0.6V which is enough to define “1” and “0” of memory states.

4.1.4 Conclusion

In conclusion, the NiOSi nanocrystals embedded in the SiO_x layer were fabricated for the nonvolatile memory application by sputtering a commixed target in an Ar/O_2 environment at room temperature. Due to different enthalpies of Si-O, Ni-O and Ni-Si, the nanocrystals can be self-assembly fabrication in this study. A larger memory window of 2.5 V was clearly observed after ±15V voltage sweep and the retention got up to 10 years for NVM application. The endurance also tolerated the P/E operation to be about one million times. In addition, this memory device is suitable for high speed operation and low temperature fabrication, such as glass, stainless steel or 3-D IC process. The fabrication technique of NiOSi nanocrystals can be compatible with current manufacture process of the integrated circuit manufacture.

Sputtering $Ni_{0.3}Si_{0.7}$ in Ar/O_2 ambiance

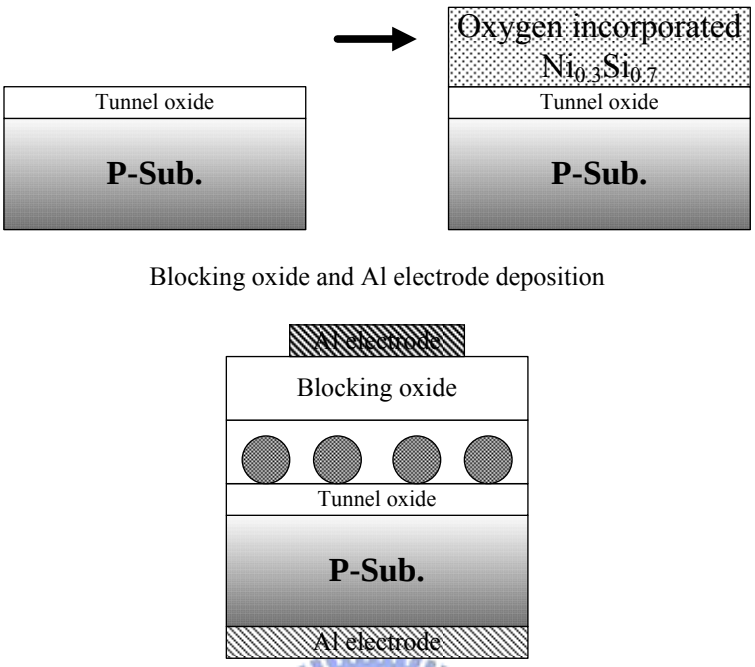


Figure 4-1 Formation flow of nanocrystals embedded in oxide MOIOS structure.

Sputtering $Ni_{0.3}Si_{0.7}$ in Ar ambiance

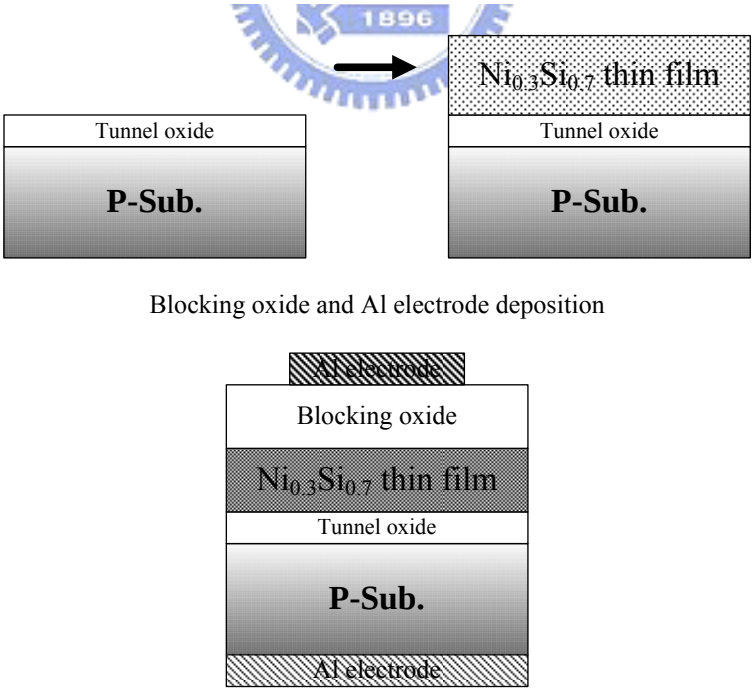


Figure 4-2 Formation flow of control sample MOIOS structure (Oxygen deficient $Ni_{0.3}Si_{0.7}$ layer as charge trapping layer).

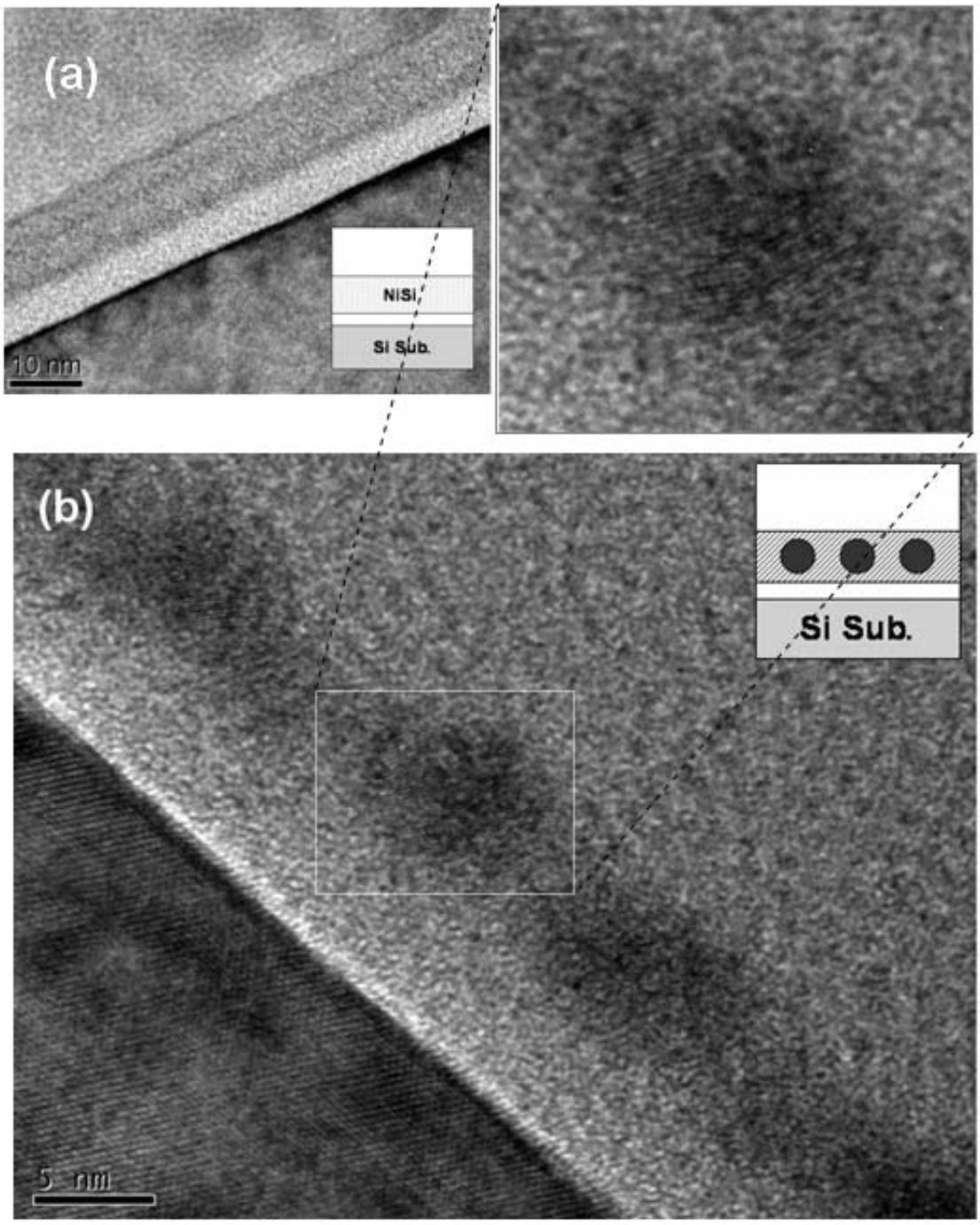


Figure 4-3 Cross-sectional TEM analyses of (a) control sample, and (b) MOIOS structure containing nanoparticles. The nanocrystal size and density are about 5-6 nm and 1.33×10^{12} cm^{-2}, respectively. The inset shows sketch diagrams of control sample and MOIOS structure.

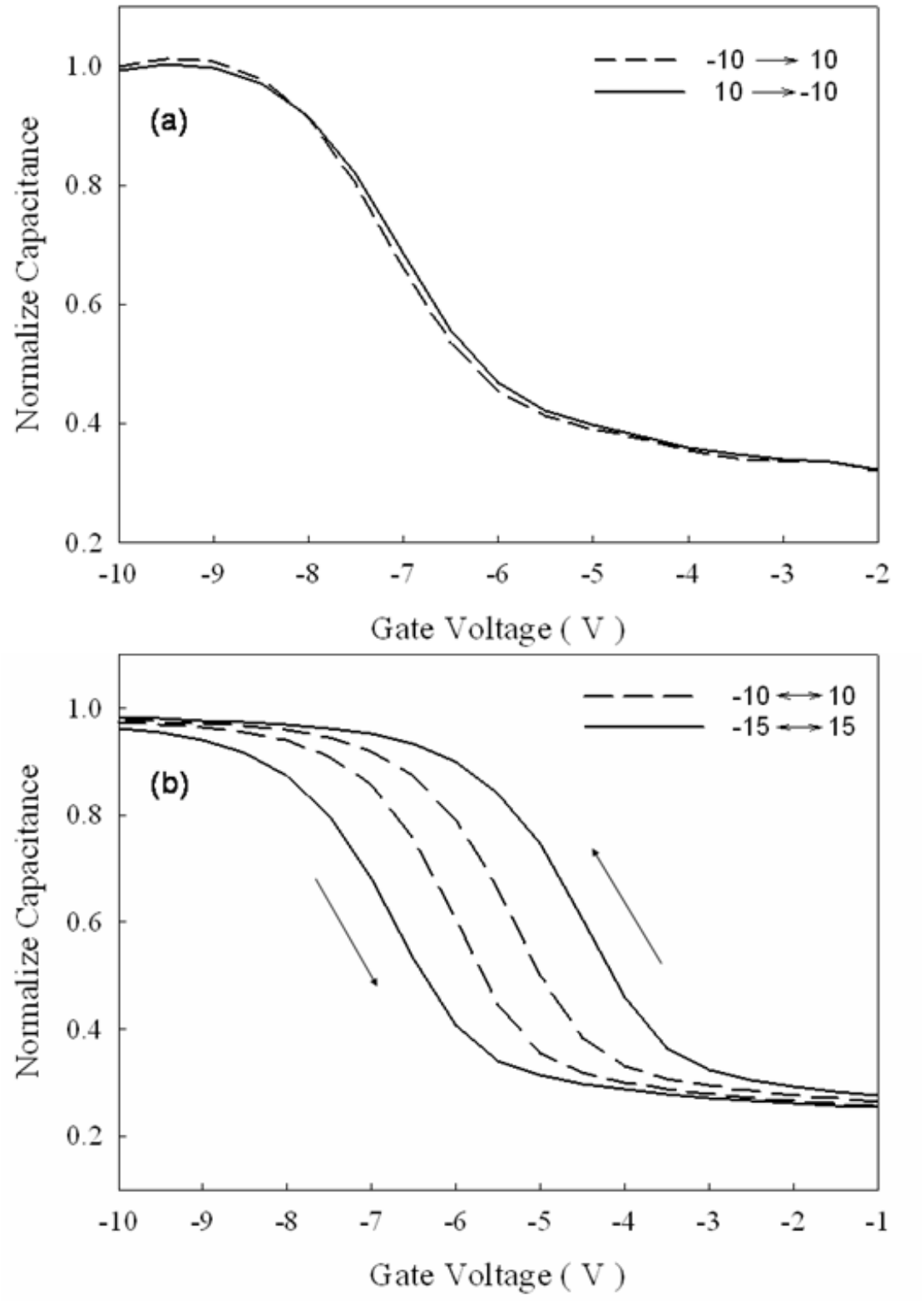


Figure 4-4 Capacitance-voltage (*C-V)* hysteresis of MOIOS structure with (a) the control sample, and (b) NiOSi nanoparticles. The memory windows of NiOSi nanoparticles, 0.8 V and 2.5 V, can be obtained under ±10 (dash line) V and ±15 V (solid line) gate voltage operation, respectively.

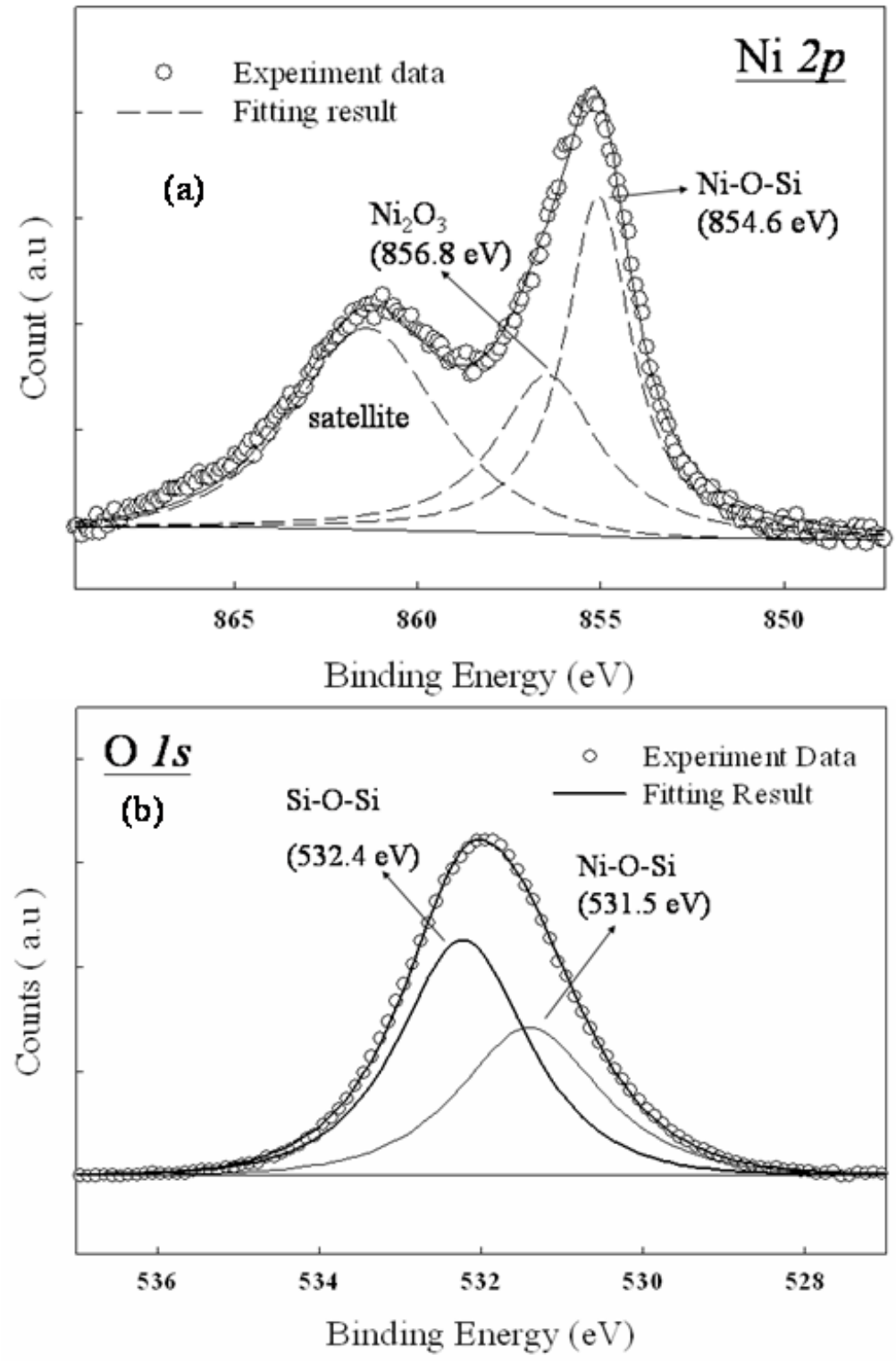


Figure 4-5 (a) Ni 2*p* and (b) O 1*s* X-ray photoelectron spectroscopy (XPS) analysis of the charge trapping layer. Empty circles and straight line indicate experimental and fitting results, respectively.

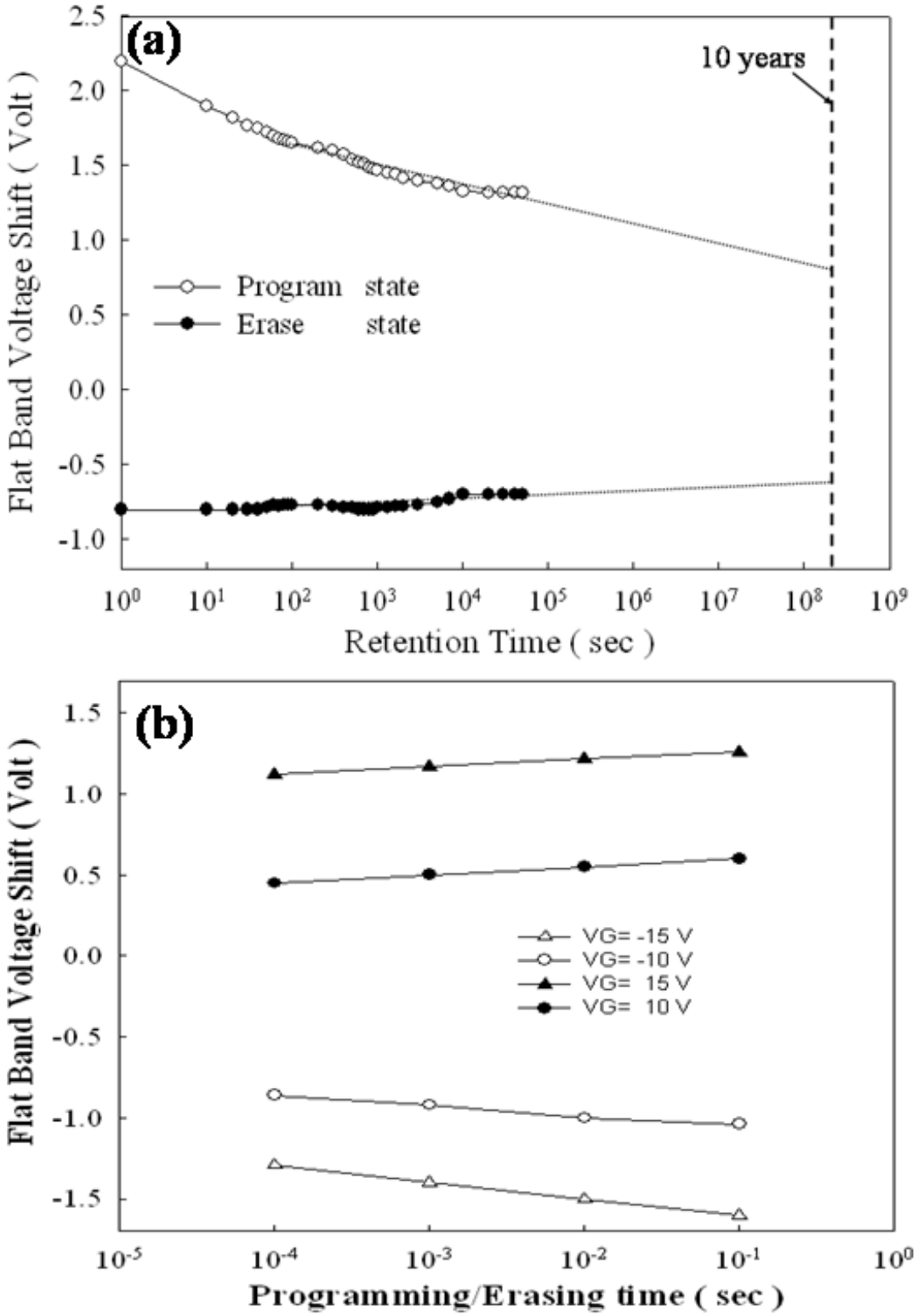


Figure 4-6 (a) Retention characteristics of the memory structure with NiOSi nanoparticles using a ±10 V gate voltage stress for 5 sec at room temperature. The dotted line is the extrapolated value of retention data after 100 sec. (b) Programming and erasing characteristics of the NiOSi nanoparticles under ±10 V and ±15 V gate voltage.

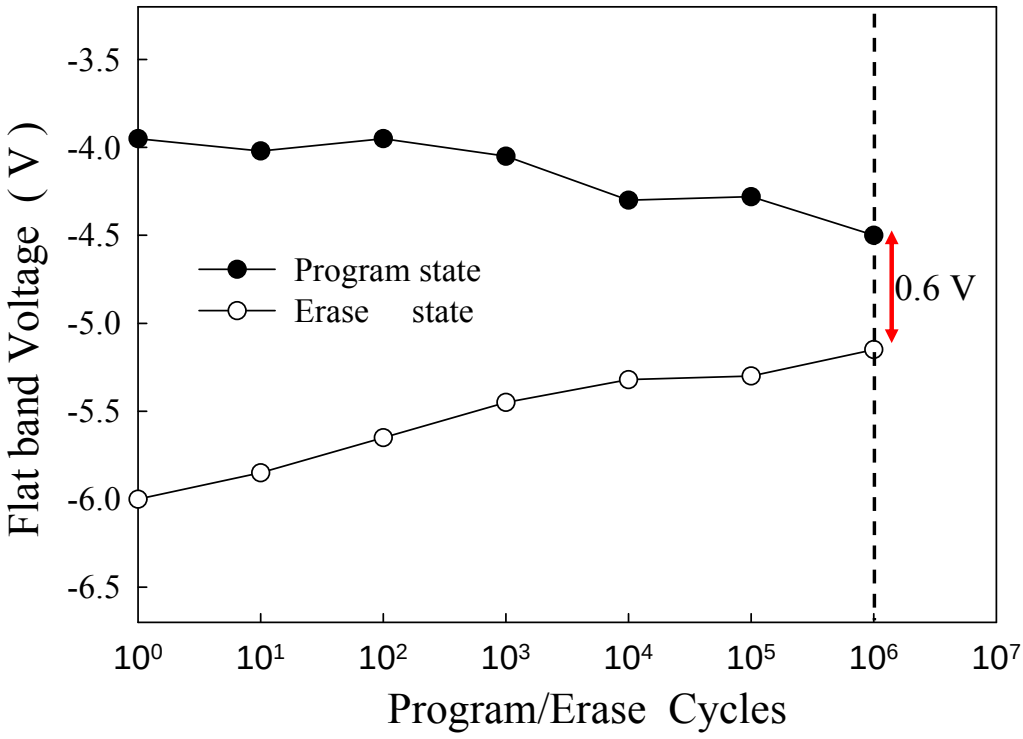


Figure 4-7 Endurance characteristics of Ni-O-Si nanocrystals embedded in oxide under the pulse conditions of $V_G - V_{FB} = \pm 5$ V for 0.1 ms. The flat-band voltage can be defined by using the C-V hysteresis.

4.2 Electrical Characteristics of Nonvolatile Nickel-Silicon-Nitride (Ni-Si-N) Nanocrystals memory

4.2.1 Introduction

Nonvolatile nanocrystal memories have recently been one of promising candidates to take the replace of conventional floating gate nonvolatile memory, because the discrete traps as the charge storage media have effectively improved data retention under endurance test for the device scaling down [4.19-4.21]. In past years, the requirements of next-generation nonvolatile nanocrystal memory are the high density cells, low-power consumption, high-speed operation and good reliability. Hence, the nonvolatile metal nanocrystal memory devices were extensively investigated over semiconducting nanocrystals, because of several advantages, such as stronger coupling with the conduction channel, higher density of states (transport perspectives) than semiconductor (i.e. larger charge storage) and a wide range of available work functions (faster programming time and better data retention) [4.22, 4.23]. A nonvolatile memory device with metal nanocrystals has been formed by several experiment techniques, for instance, self-assembled of tungsten (W) nanocrystal by using thermal oxidation process [4.24], separation of nickel (Ni) or gold (Au) nanocrystal by direct thermal annealing [4.25, 4.26], and formation of platinum (Pt) or cobalt (Co) nanocrystal by using molecular beam epitaxy (MBE) [4.27, 4.28]. Besides, the charge trapping layer also can contain some Si-N bonds which increase trapping states to improve charge storage capacity and program/erase efficiency for the nonvolatile metal nanocrystal memory devices, such as metal-oxide-nitride-oxide-semiconductor (MONOS) structure or silicon-germanium-nitride (SiGeN) structure [4.29, 4.30].

In this study, an ease process for Nickel-Silicon-Nitride (Ni-Si-N) nanocrystals

formation will be proposed by sputtering a commixed target ($Ni_{0.3}Si_{0.7}$) in the argon (Ar) and nitrogen (N_2) environment at room temperature. It was found that the Ni-Si-N nanocrystals embedded in the silicon nitride (SiN_x), due to larger Gibbs free energy of chemical bond of Si-N than Ni-N at the room temperature [4.31, 4.32]. In addition, high resolution transmission electron microscope (HRTEM) and x-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical material analysis of Ni-Si-N nanocrystals. Furthermore, these electrical characteristics of Ni-Si-N nanocrystals would be compared with the performance of Ni-O-Si nanocrystals nonvolatile memory.

4.2.2 Experiment

This memory-cell structure in this section was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process, 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 10-nm-thick nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ commixed target in the Ar (24 standard cubic centimeters per minute (sccm)) and N_2 (10 sccm) environment at room temperature, and the DC sputtering power was set to 80 W. Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition (PECVD) system at 300^{o}C. Hence, these ternary nanocrystals could be found to precipitate and embed in SiN_x during the foregoing process. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. The formation flow of MOIOS structure was shown in Fig. 4-8. Electrical characteristics, including the capacitance-voltage (C-V) hysteresis, current density-voltage (J-V), and retention characteristics, were also performed. The J-V and C-V characteristics were measured

by Keithley 4200 and HP4284 Precision LCR Meter with high frequency of 1 MHz.

4.2.3 Results and Discussion

4.2.3.1 Material and electrical analyses of Ni-Si-N nanocrystals

Figure 4-9 exhibits a cross-sectional TEM image of the nitrogen incorporated $Ni_{0.3}Si_{0.7}$ film containing spherical and separated nanocrystals embedded in the SiN_x matrix. It is found that the thickness of tunnel oxide is larger than 3 nm, due to the contribution of SiN_x matrix by TEM analysis. This SiN_x matrix can be used to improve charge storage ability for nonvolatile memory application [4.30]. Moreover, the average diameter of the nanocrystals is approximately 5-6 nm and the area density of the nanocrystals is estimated to be about 1.08×10^{12} cm^{-2} by HRTEM analysis.

To further investigate the nanocrystals, we have performed XPS analysis by using an Al *K*α (1486.6 eV) X-ray radiation to demonstrate the chemical composition of the nanocrystals. To correct possible charging effect of the film, the binding energy was calibrated using the C 1s (284.6 eV) spectra of hydrocarbon that remained in the XPS analysis chamber as a contaminant. Figure 4-10(a) shows the XPS Ni 2*p* core-level photoemission spectra which consist of two main peaks, $2p_{3/2}$ (~ 855 eV) and $2p_{1/2}$ (~ 873 eV), with two small satellite peak. According to the values of other literature, Ni $2p_{3/2}$ binding energies are at 852.3 eV and 853.4 eV for metallic nickel (Ni–Ni) and Ni-silicide (Ni–Si), respectively [4.33]. However, it cannot be found that the above-mentioned peak signals are observed at the Ni $2p_{3/2}$ peak by XPS analysis. Due to the strong electronegativity of nitrogen atom, it is reasonably assumed that the larger Ni $2p_{3/2}$ binding energy (~ 855 eV) of the nanocrystals can be assigned to Ni–Si–N ternary bond. This result is also supported by the XPS N 1*s* photoemission spectra, as shown in Fig. 4-10(b). By the fitting result of binding energy, it is found that the main peak can be compose into two components which center at 398.5 eV and

397 eV corresponding to Si–N bond and Ni–N bond, respectively [4.34, 4.35].

For chemical characteristics of Si–N and Ni–N, the enthalpies ($-\Delta H$) at room temperature, are 470 and 70~85 kJ mol^{-1}, respectively [4.31, 4.32]. Hence, because of the higher enthalpy of Si–N compared with Ni–N, the N radicals can interact with Si atom easier than Ni atom during the sputtering process. It could be considered that a nitridation reaction will induce self-assembled phenomenon of Ni-Si-N nanocrystal, as shown in Fig. 4-11. In the previous research, Ni atom can diffuse in the SiN_x even at room temperature and formation of a Ni-Si-N ternary solid solution [4.36]. Therefore, the nanocrystals are simple and uniform to be formed at low temperature by sputtering a commixed target in the Ar/N_2 environment due to different Gibbs free energy of chemical bond of Si-N than Ni-N.

The typical capacitance-voltage (*C-V*) hysteresis obtained with gate voltage from accumulation to inversion and in reverse is shown in Fig. 4-12. It is clearly observed that 1.5 V and 3.5 V memory windows can be obtained under ±10 V and ±12 V operation, respectively. The MOIOS structure with the Ni-Si-N nanocrystals embedded in SiN_x matrix exhibits clear counterclockwise hysteresis by a flat band voltage shift (V_{FB}), indicating the significant memory effect. We consider that the charges can be stored in both the Ni-Si-N nanocrystal and the SiN_x traps. Moreover, the hysteresis loops follow the counterclockwise due to injection of electrons from the deep inversion layer and discharge of electrons from the deep accumulation layer of Si substrate. Hence, this memory window of Ni-Si-N nanocrystals embedded in SiN_x matrix is enough to be defined “1” and “0” states. In addition, current density-voltage (*J-V*) characteristics in the inset of Fig. 4-12 shows the current density of the MOIOS structure by gate voltage sweeping from 0 V to 10 V and 0 V to -10 V. It is evident that the high quality of blocking oxide can avoid the stored carriers of charge trapping layer to leak into gate electrode.

Retention characteristics of the memory structure with Ni-Si-N nanocrystals are illustrated in Fig. 4-13. The retention measurements are performed at room temperature by operating a ±10 V gate voltage stress for 5 s. The V_{FB} is obtained by comparing the *C-V* curves from a charged state and a quasi-neutral state. When carriers are stored in the nanocrystals, the stored charges will raise the nanocrystal potential energy and increase the probability of escaping from the nanocrystal to the silicon substrate [4.37]. Moreover, carriers trapped in the shallow traps are unstable and can easily leak back to the silicon substrate. It is found that the window of V_{FB} significantly reduces during the first 1000 s, and then becomes more stable for long retention time. This result is consistent with partial carriers trapping in the shallow trap state of the SiN_x matrix around the nanocrystals. However, we use an extrapolation to give a long-term predictable result (dotted line) after 1000s (stable region of retention) and extrapolate a memory window of 1.8V (total charge hold ratio 57%) after ten years. The majority carriers stored in the deep trapping states of Ni-Si-N nanocrystals surrounding with SiN_x matrix exhibit good retention characteristics.

Endurance characteristics for Ni-Si-N nanocrystals embedded in SiN_x matrix is shown in Fig. 4-14. Pulses (V_G - V_{FB} = ± 5 V, 0.1 ms) were applied to evaluate endurance characteristics for the P/E operations. An obvious difference of two logical states can be maintained until 10^4 P/E cycles. Subsequently, the closure of window between two logical states appears after 10^4 P/E cycles. We consider that this closure was caused by the degradation of SiN_x dielectric. However, this memory structure exhibits better endurance characteristics than Ni-O-Si nanocrystals nonvolatile memory. It retained a memory window of 1.0 V after 10^6 P/E cycles which was enough to define “1” and “0” of memory state.

4.2.3.2 Comparison of Electrical Characteristics between Ni-O-Si and Ni-Si-N Nanocrystals Nonvolatile Memory

The comparisons of memory window and nanocrystal density for the Ni-O-Si and Ni-Si-N Nanocrystals nonvolatile memory devices are listed in Table 4-1. The estimated density of Ni-O-Si nanocrystal by TEM analysis is close to that of Ni-Si-N nanocrystal. To compare with Ni-O-Si nanocrystal embedded in SiO_x, Ni-Si-N nanocrystal embedded in SiN_x as charge trapping layer exhibits lager memory window under ±10V operation. Additional accessible charge trap states in SiN_x matrix cause the much larger memory effect [4.30]. From an electrostatics consideration, SiN_x matrix with a higher dielectric constant than SiO_x will cause a smaller voltage drop across the charge trapping layer and a greater voltage drop across the tunnel oxide. This effect will result in increasing of the electric field across the tunnel oxide, and stored charges can tunnel more efficiently from substrate into the trapping layer under the same gate operation voltage.

The current density-voltage (J-V) characteristics of different MOIOS structure by gate voltage sweeping from 0 V to 10 V and 0 V to -10 V are shown in Fig. 4-15. In this experiment result, it is found that the leakage current of the memory structures containing Ni-O-Si or Ni-Si-N nanocrystals is significantly reduced as compared to that of control sample. This result can verify our proposed in-situ internal oxidation (nitridation) for the dielectric layer of charge trapping layer and be also explained that the coulomb blockade effect was caused by the stored charges trapped in the nanocrystals and its surrounding dielectric. The trapped charges would raise the nanocrystal potential energy and reduce the electric field across the tunnel oxide, resulting in reduction of the tunneling current density.

Table 4-2 lists the retention characteristics after 10ys for the Ni-O-Si and Ni-Si-N nanocrystal nonvolatile memory. The Ni-Si-N nanocrystal embedded in SiN_x

shows better retention characteristics, that is, a larger long-term extrapolated window of 1.8V (charge remained ratio of 57%) is maintained after 10ys. According to previous research [4.30], the charges can be shared among the nitride trap and hence the electric field across the tunneling oxide can be reduced by separated stored charges (reduction of Coulomb repulsive force). This result decreases the probability of charge escaping from the nanocrystal. Moreover, charges are likely to be relaxed to the nitride traps. Charge loss through the intermediate medium can also be inefficient due to Coulomb blockade effect. Therefore, carriers stored in nanocrystals embedded in nitride layer cannot easily leak back to the silicon substrate by our investigation.

4.2.4 Conclusion

The nonvolatile memory structure of Ni-Si-N nanocrystals embedded in the SiN_x layer was fabricated by sputtering a commixed target ($Ni_{0.3}Si_{0.7}$) in an Ar/N_2 environment at room temperature. It would be considered that the nitrogen played a critical role during the sputtering process for the formation of nanocrystal. The self-assembled phenomenon of Ni-Si-N nanocrystals was explained that the released energy will induce Ni atoms to diffuse in the SiN_x during the fabrication process. The high density (~10^{12}) nanocrystal was also simple and uniform to be fabricated on the tunnel oxide in this study. The memory window of Ni-Si-N nanocrystals enough to define "1" and "0" states is clearly observed for the nonvolatile memory application. The retention and endurance characteristic are good enough to be maintained after 10 years and 10^6 P/E cycles. A larger memory window of 1.5 V was observed after ±10V voltage sweep as compared with Ni-O-Si nanocrystals NVM. This improvement was attributed to the additional accessible charge trap states in the SiN_x matrix. In addition, the charge trapping layer combined with Ni-Si-N nanocrystals and SiN_x exhibited better reliability characteristics than Ni-O-Si nanocrystals.

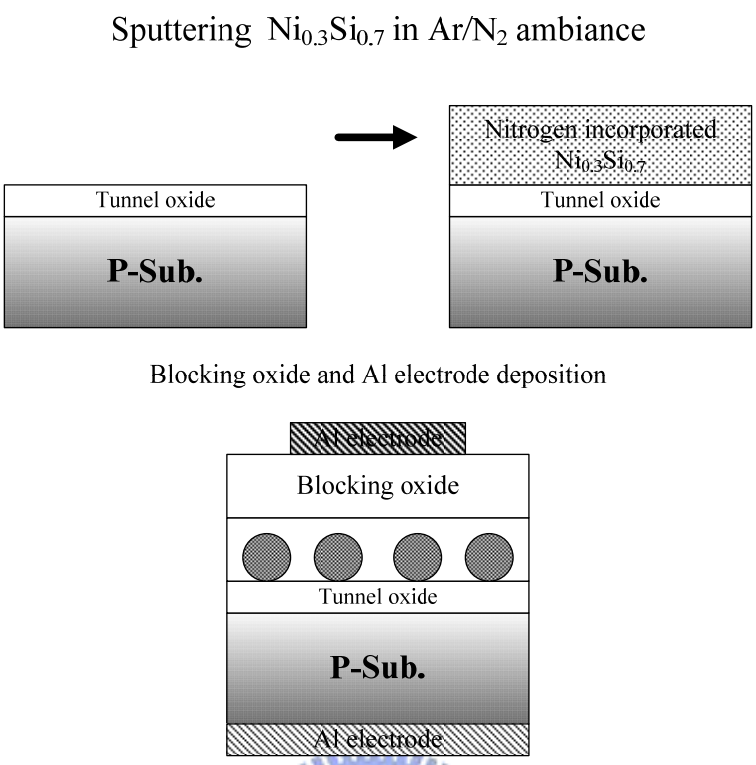


Figure 4-8 Schematic sketches of the experimental procedures. Nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer as charge trapping layer was fabricated the nanocrystal nonvolatile memory.

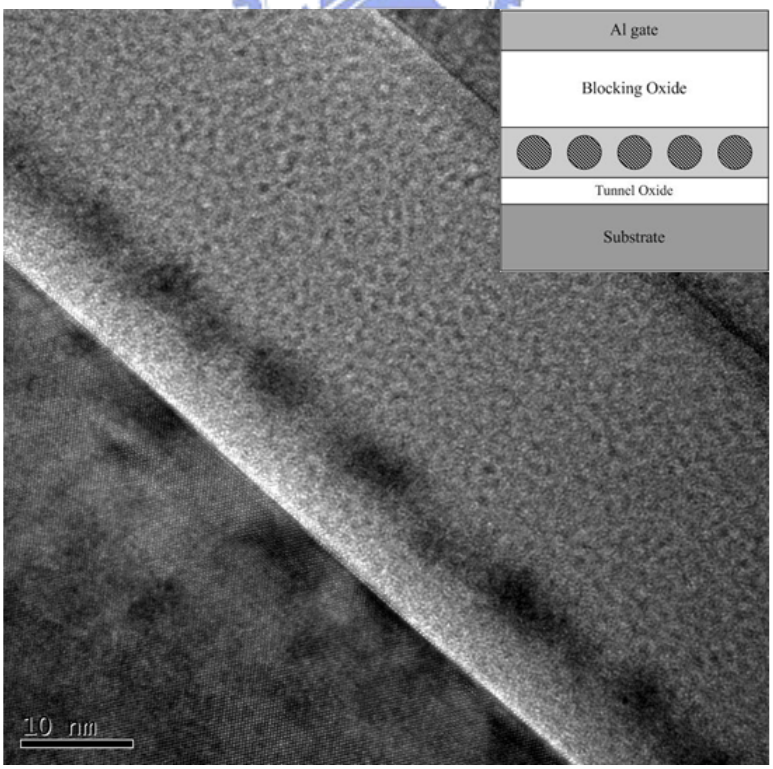


Figure 4-9 Cross-sectional TEM image of the MOIOS structure with nanocrystals during our proposed fabrication. The inset was a schematic sketch of MOIOS.

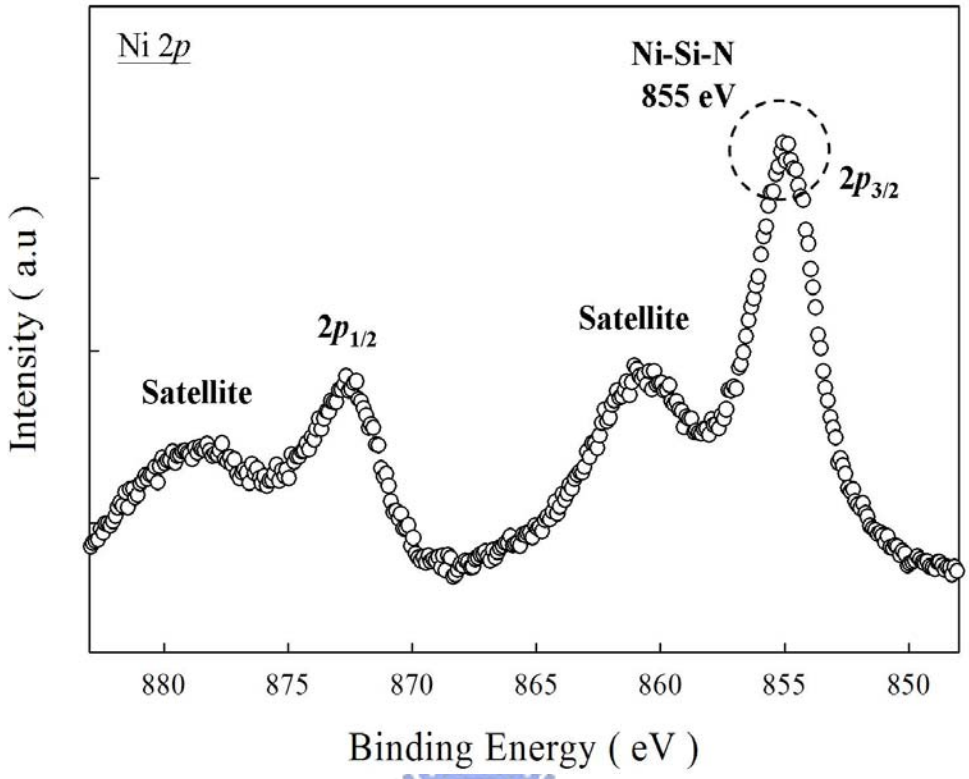


Figure 4-10 (a) Ni 2*p* XPS analysis of the charge trapping layer. The Ni $2p_{3/2}$ peak can be assigned to Ni-Si-N ternary bond (~ 855 eV).

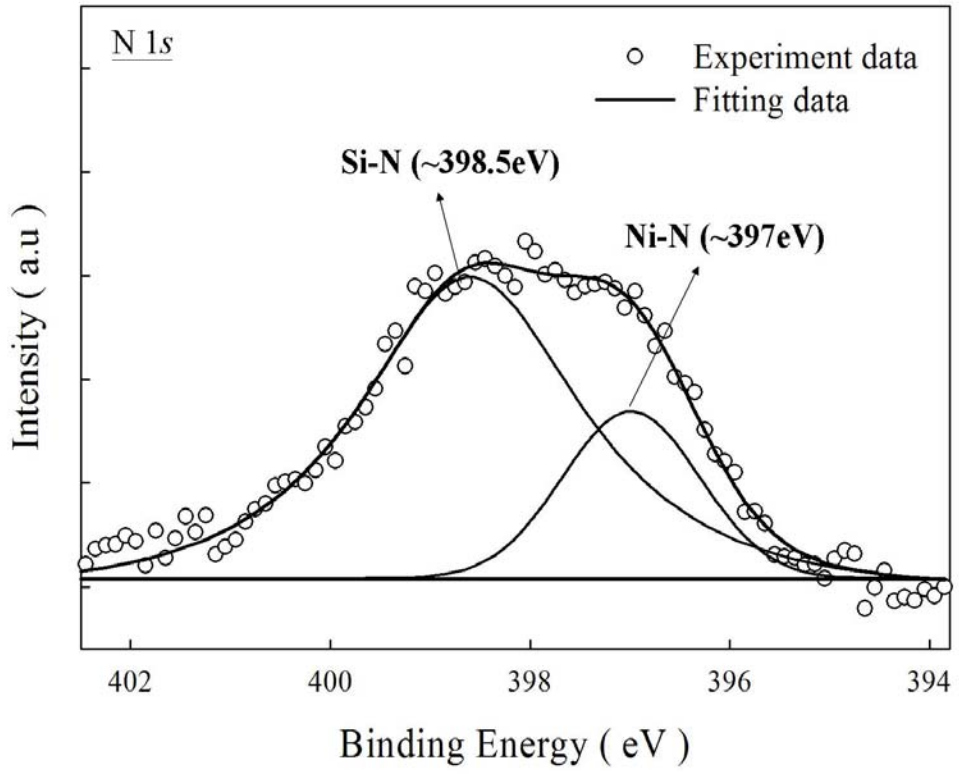


Figure 4-11 (b) N 1*s* XPS analysis of the charge trapping layer. Empty circles and straight line indicate experimental and fitting results, respectively.

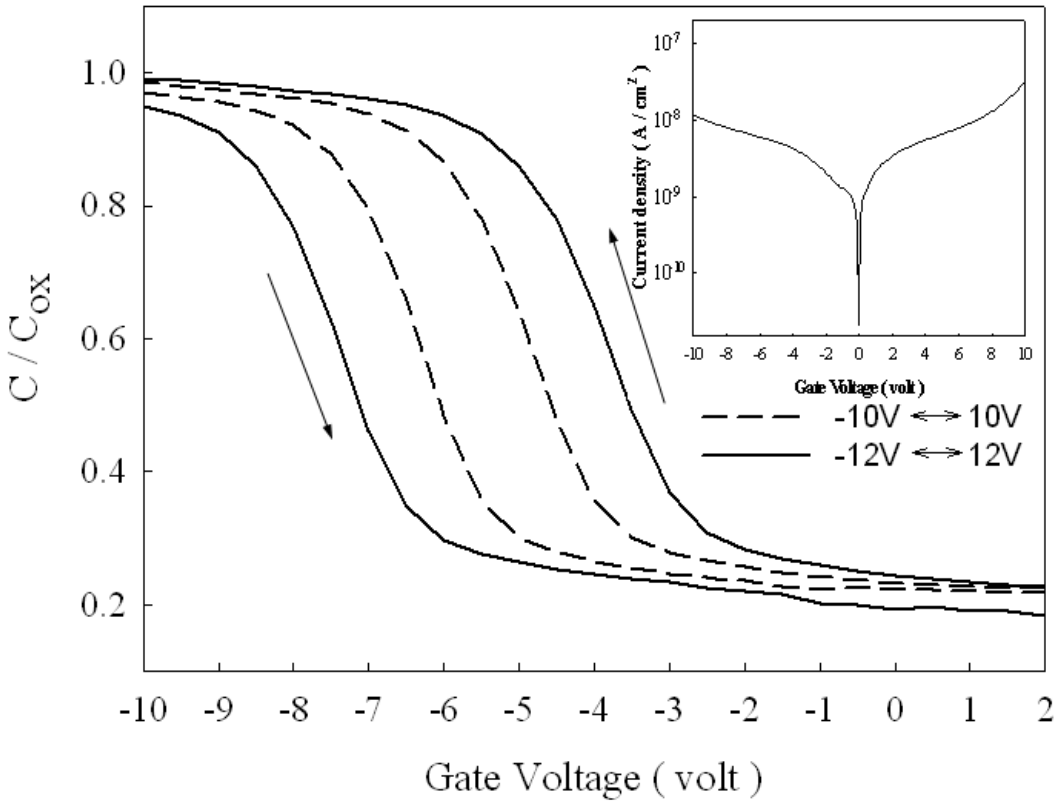


Figure 4-12 Capacitance-voltage (*C-V*) hysteresis of the fabricated MOIOS structure with the Ni-Si-N nanocrystals embedded in SiN_x matrix as a charge trapping layer. The inset shows current density-voltage (*J-V*) characteristics.

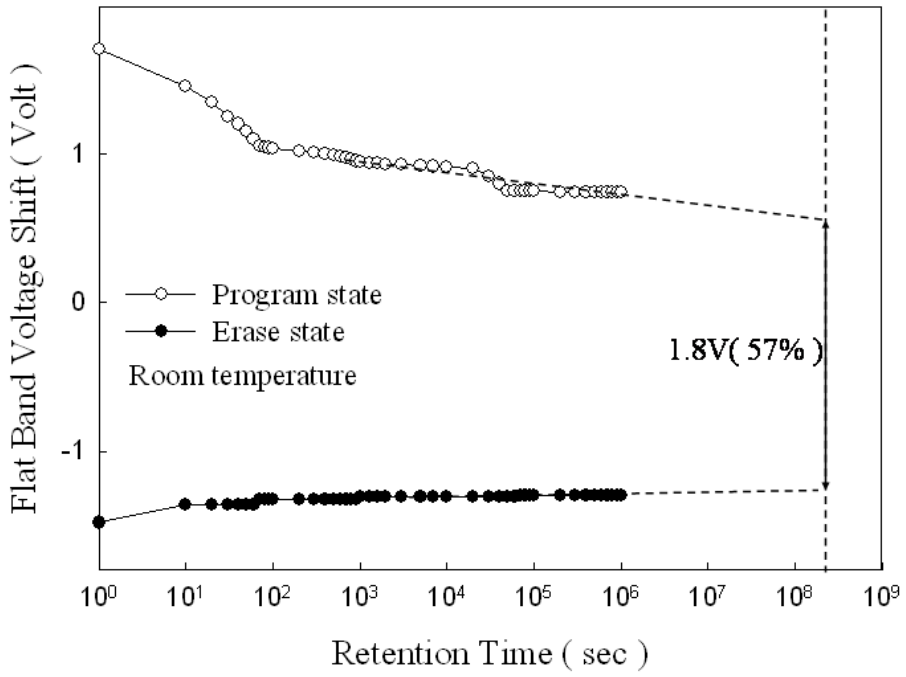


Figure 4-13 Retention characteristics of the memory structure with Ni-Si-N nanocrystals embedded in SiN_x matrix using a ±10 V gate voltage stress for 5 sec at room temperature. The dotted line is the extrapolated value of retention data after 1000 sec.

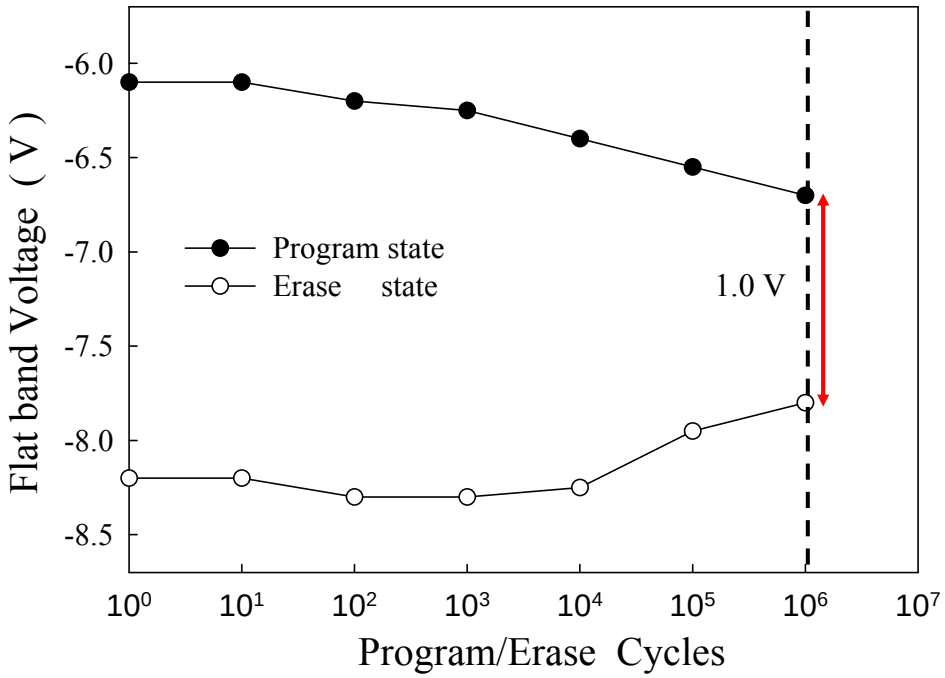


Figure 4-14 Endurance characteristics of the Ni-Si-N nanocrystal nonvolatile memory. The memory window is about 1.0 V after one million P/E cycles operation.

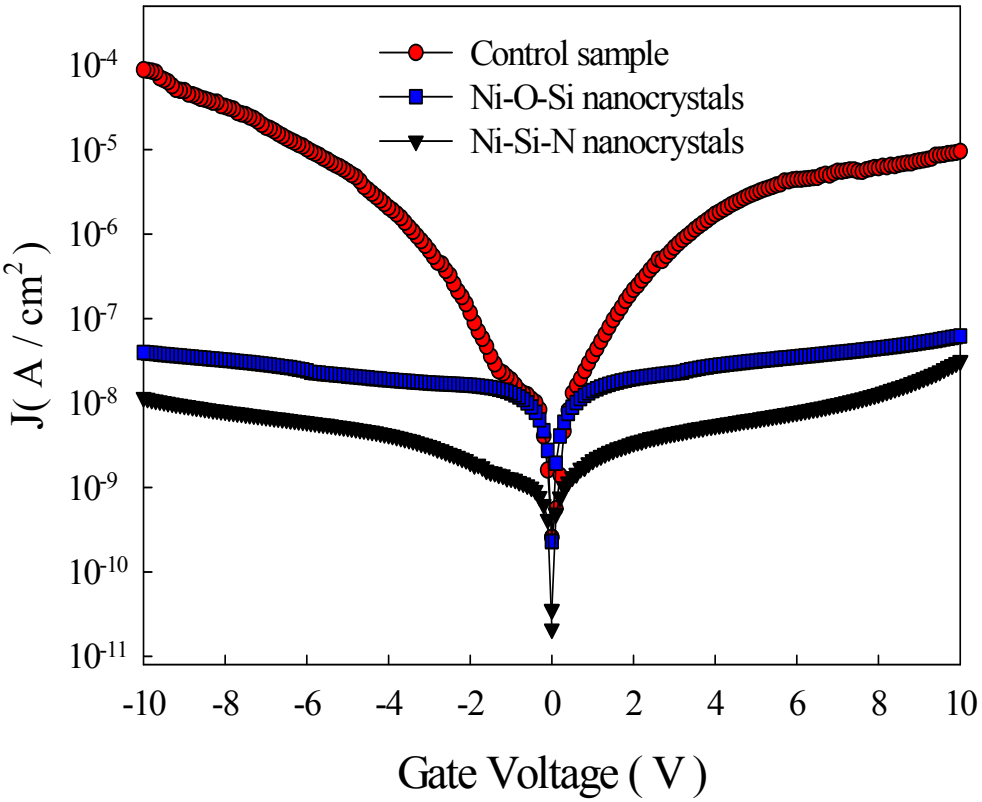
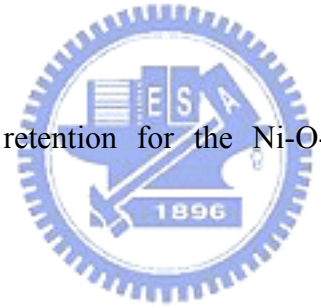


Figure 4-15 Current density-voltage (J-V) characteristics of the MOIOS nonvolatile memory structures with the control sample, Ni-O-Si nanocrystals and Ni-Si-N nanocrystals.

Table 4-1 Comparisons of memory window and nanocrystal density for the Ni-O-Si and Ni-Si-N nanocrystals nonvolatile memory devices.

Nonvolatile Memory	Memory window under ±10V operation	NC density (cm^{-2})
Ni-O-Si Nanocrystals embedded in SiO_x	0.8V	1.33×10^{12}
Ni-Si-N Nanocrystals embedded in SiN_x	1.5V	1.08×10^{12}

Table 4-2 Comparisons of retention for the Ni-O-Si and Ni-Si-N nanocrystals nonvolatile memory devices.



Nonvolatile Memory	Memory window after 10 years	Remained Charge Ratio
Ni-O-Si Nanocrystals embedded in SiO_x	1.2V	40%
Ni-Si-N Nanocrystals embedded in SiN_x	1.8V	57%

4.3 Enhancement of charge storage Performance of Ni-Si-N Nanocrystals Embedded in Nitride Memory by Rapid Thermal Annealing treatment

4.3.1 Introduction

Recently, nonvolatile memory devices (NVM) are moving toward high density cell array, low operation voltage, and good reliability. Although conventional flash memories do not require refreshing currently, they have some drawbacks that must be solved for further high performance memory application, such as quantum effect under thin tunnel oxide situation (< 4 nm) and data retention time for reliability test [4.38]. For the development of next-generation NVM technique, devices fabrication should be required be compatible with current manufacture process of the integrated circuit manufacture. Therefore, the silicon-oxide-nitride-oxide-semiconductor (SONOS) type and nanocrystals (NCs) memory structures have been proposed and demonstrated to lead to an improvement in retention time compared with conventional NVM because of employing discrete traps or quantum wells served as charge storage media [4.39-4.45].

To alleviate the tunnel oxide design trade-off for NVM devices, we proposed the memory structure that was combined with SONOS-type and metal nanocrystals to obtain better charge storage ability and strong coupling with conduction channel. In this section, a simple process for nickel-silicide (Ni-Si) and nickel-nitride (Ni-N) nanocrystals embedded in nitride layer was formed by sputtering a commixed target in argon (Ar) and nitrogen (N_2) environment. It is found that the crystallization of nanocrystals and the quality of surrounding dielectric were distinct with different temperature annealing, thus the annealing temperature was really a key parameter for the charge storage properties of NVM.

4.3.2 Experiment

Figure 4-16 indicates a schematic sketch of experimental procedures. This memory-cell structure was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace (APCVD). Subsequently, a 10-nm-thick nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ co-mix target in the Ar (24 sccm) and N_2 (10 sccm) environment at room temperature, and the DC sputtering power was set to 80 W. Next, the rapid thermal annealing (RTA) process was performed in N_2 ambient. The annealing conditions are 500^{o}C for 100sec and 600^{o}C for 100sec.Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition (PECVD) system at 300^{o}C. Al gate electrodes on back and front side of the sample were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. Here, we had a STD sample which was no use of RTA process as the memory cell of **Chapter 4.2**.

Electrical characteristics, including the capacitance-voltage (C-V), current density-voltage (J-V), retention, and endurance characteristics, were also performed. The J-V and C-V characteristics were measured by Keithley 4200 and HP4284 Precision LCR Meter with high frequency of 1 MHz. In addition, Transmission electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical material analysis.

4.3.3 Results and Discussion

Figure 4-17 exhibits the material analyses of charge trapping layer under the annealing temperature conditions of STD (the thermal treatment was only existed in blocking oxide process, 300^{o}C), 500^{o}C (RTA), and 600 ^{o}C (RTA). Figure 4-17(a) shows the N 1*s* core-level spectra with different temperature annealing. Obviously, the spectra are composed of two peaks, SiN (396.8 eV) and Ni-N (398.5 eV) for STD state and 500^{o}C annealing [4.46, 4.47]. The peak signal of Si-N bonding shifted toward higher binding energy and the peak signal of Ni-N was decayed gradually to disappear as temperature increases. To further ascertain the crystallizations of NCs with different temperature annealing, the XRD analyses were executed. As shown in Fig. 4-17(c), the diffraction peak of 32.8 degree indicate the Ni-Si NCs are formed as annealing temperature over 500^{o}C [4.48]. (Control sample is only a structure of Si substrate with tunnel oxide) From the XPS analyses, we considered that the quality of surrounding dielectric, SiN_x, had been improved by a reducible reaction of Ni-N during the thermal annealing process. To verify this viewpoint, the leakage current density J (A/cm^2) with gate voltage was measured (as shown in Fig. 4-17(b)). It was found the leakage current after 600 ^{o}C annealing was the lowest under 0 V to ±10 V sweeping. Moreover, the compound of NCs could be changed form Ni-N to Ni-Si after the annealing process and also affect charge storage characteristics for the NVM application.

In general, the forward (from accumulation state to inversion state) and reverse *C-V* hysteresis was measured to investigate the charge storage abilities of nonvolatile NCs memories. When the RTA temperature increases to 500 ^{o}C and 600^{o}C, the memory window raises to 5.0 V and 4.0 V under ±10 V sweeping operation. Moreover, these samples also can be found that the roundness and isolation of NCs are better than STD sample by TEM analyses as shown in Figs. 4-18 and 4-19. These

physical phenomena could be contributed by a thermal enhanced congregation of Ni-atoms. According to previous theoretical model about the probability of an electron escaping from the NC back to the channel, the spherical NCs can reduce the Weinberg impact frequency that is affected by geometry effect [4.49]. On the other hand, the more separated NCs also could restrain the electrons lateral migration effect under a retention test, because the electrons stored in the NC lift the energy level of NC conduction band resulting in the increase of the escaping probability. Therefore, the rotundity and severance of NCs are good for the sub-50nm gate length process application.

The charge retention characteristics of NiSi nanocrystals embedded in SiN_x after thermal treatment, 500 ^{o}C and 600^{o}C, are demonstrated in Fig. 4-20. This measurement is carried out at room temperature using ±10 V gate voltage stress for 5 sec. The shift in the flat-band voltage as a function of time is obtained by comparing the C-V curves. Figure 4-20(a) exhibits retention characteristic of charge storage layer after RTA at 500 °C for 100 sec. A memory window of 2.1 V is expected to maintain after 10 years, which is approximately 52% of the stored charges retained in the nanocrystals. In the meantime, the retention characteristic after RTA at higher 600 °C for 100 sec is also shown in Fig. 4-20(b). The long-term extrapolated gives a memory window of 1.8V (charge retained ratio 56%) after 10 years. The retention characteristic was also performed at 85°C, which increases the charge loss rate. However, an expected memory window of 0.6V after 10 years is still enough to define two memory states.

The endurance characteristics of MOIOS structure after RTA at 500 °C and 600 °C are shown in Figs. 4-21(a) and (b), respectively. Pulses (V_G - V_{FB} = ± 5 V, 0.1 ms) were applied to evaluate endurance characteristics for the P/E operations. We found that the flat-band voltages of program and erase states almost have no any change till

10^6 P/E cycles. Both of thermal treatment conditions all retained the clear memory window of 2.1V for our endurance test.

We further compared the charge storage characteristics of our proposed samples, such as the memory window, retention and endurance. The results are listed in Table 4-3. It can be noted that the memory window of NiSi NCs embedded in nitride (500^{o}C) is three times larger than the STD sample. Because the resistivity of Ni-Si (14-20 $\mu\Omega$cm) is smaller that Ni-N (151.7 $\mu\Omega$cm) and the resistivity is inverse with the density of states which is a property that affects the number of storage charges [4.50], NiSi NCs embedded in nitride (500^{o}C) NVM has the superior memory window due to the less amount of Ni-N NCs (as shown in Fig. 4-17(a)). Hence, it should be believed that the nonvolatile memory capacity was greatly influenced by the crystallizations characteristic of Ni-Si and Ni-N NCs. In addition, the initial memory window was fixed at the same value for the retention and endurance test. Table 4-3 clearly indicates that the reliability of nonvolatile Ni-Si NCs memories (500 ^{o}C and 600^{o}C) is better than Ni-N NCs (STD). Acorrding to the above-mentioned material analyses, we concluded that the annealing temperature had a great influence on the properties of NCs and this factor also significantly affected the memory window.

Here, the conjectural energy band diagrams were proposed to explain these physical phenomena of charge storage, as shown in Fig. 4-22. Because of the density of traps in nitride layer decreased as the annealing temperature increases, the NiSi NCs embedded in nitride (600^{o}C) NVM has the least trap density, as shown in Fig. 4-22(c). However, the reduction of the trap density results in the memory window of NiSi NCs embedded in nitride (600^{o}C) NVM lower than that of the NiSi NCs embedded in nitride (500^{o}C) NVM, because the traps of nitride could provide additional charges storage nodes.

Although the nitride traps can improve the memory window, electrons stored in these shallow traps of nitride will easily escape to substrate. In addition, the nitride traps surrounding the NCs also provide the leakage paths for the stored carriers of NCs. Both the above drawbacks cause the retention of STD and NiSi NCs embedded in nitride (500^{o}C) NVM worse than the NiSi NCs embedded in nitride (600^{o}C) NVM. As shown in Table 4-3, the electron holding ratio (50%) of NiSi NCs embedded in nitride (600^{o}C) NVM was estimated for ten years much better than the NiSi NCs embedded in nitride (500^{o}C) NVM (31%) and STD (20%). Moreover, the endurance results reveal that the NiSi NCs embedded in nitride (500^{o}C and 600^{o}C) NVMs had excellent reliability after 10^{6} P/E cycles operation because the stronger silicon-nitrogen bonding (as shown in Fig 4-17(a)) could suppress the damage during the P/E operation. Summarizing the above results, the nonvolatile Ni-Si NC memory after the annealing temperature 600^{o}C exhibits the best NVM performance and this device also can be used on a low temperature substrate (< 600^{o}C) for the next-generation application.

4.3.4 Conclusion

In conclusion, the nonvolatile memory characteristics were influenced by the crystallizations of Ni-Si and Ni-N NCs. The nonvolatile Ni-Si NC memory shows the better charge storage ability and reliability than STD memory, since Ni-Si NCs have higher density of states and stronger surrounding dielectric than the others. Hence, the MOIOS structure needed a 600^{o}C thermal annealing process to obtain a high performance nonvolatile NCs memory in this work. In addition, the proposed energy band diagrams could clearly explain the trap density of surrounding dielectric, SiN_x, how to affect the NVM characteristics.

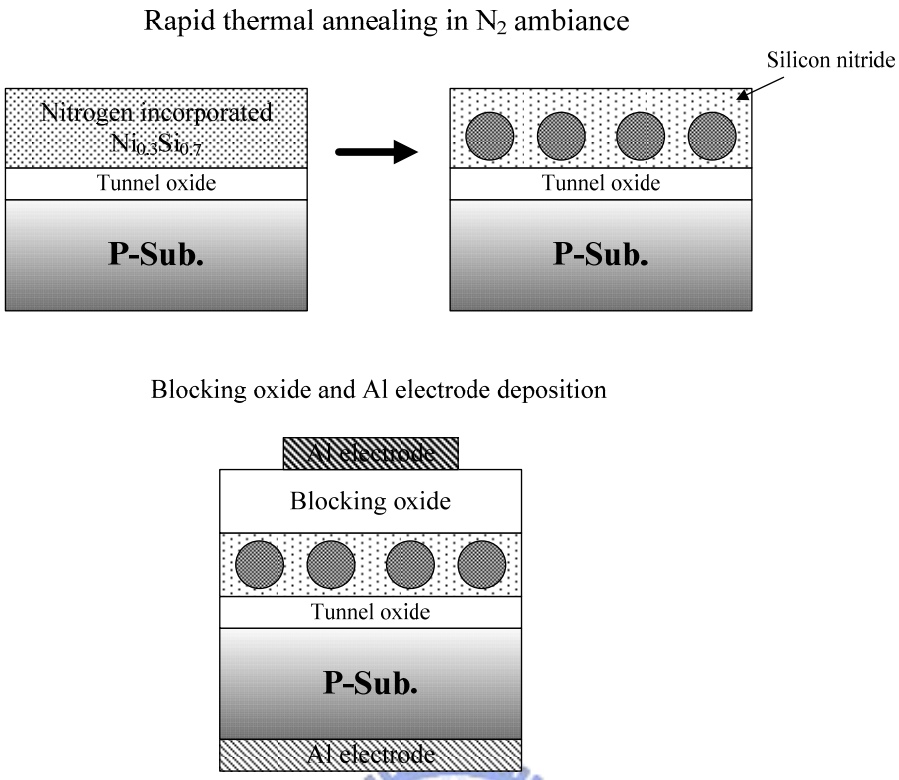


Figure 4-16 Formation flow of NiSi nanocrystals embedded in nitride layer by using rapid thermal annealing treatment in N_2 ambiance.

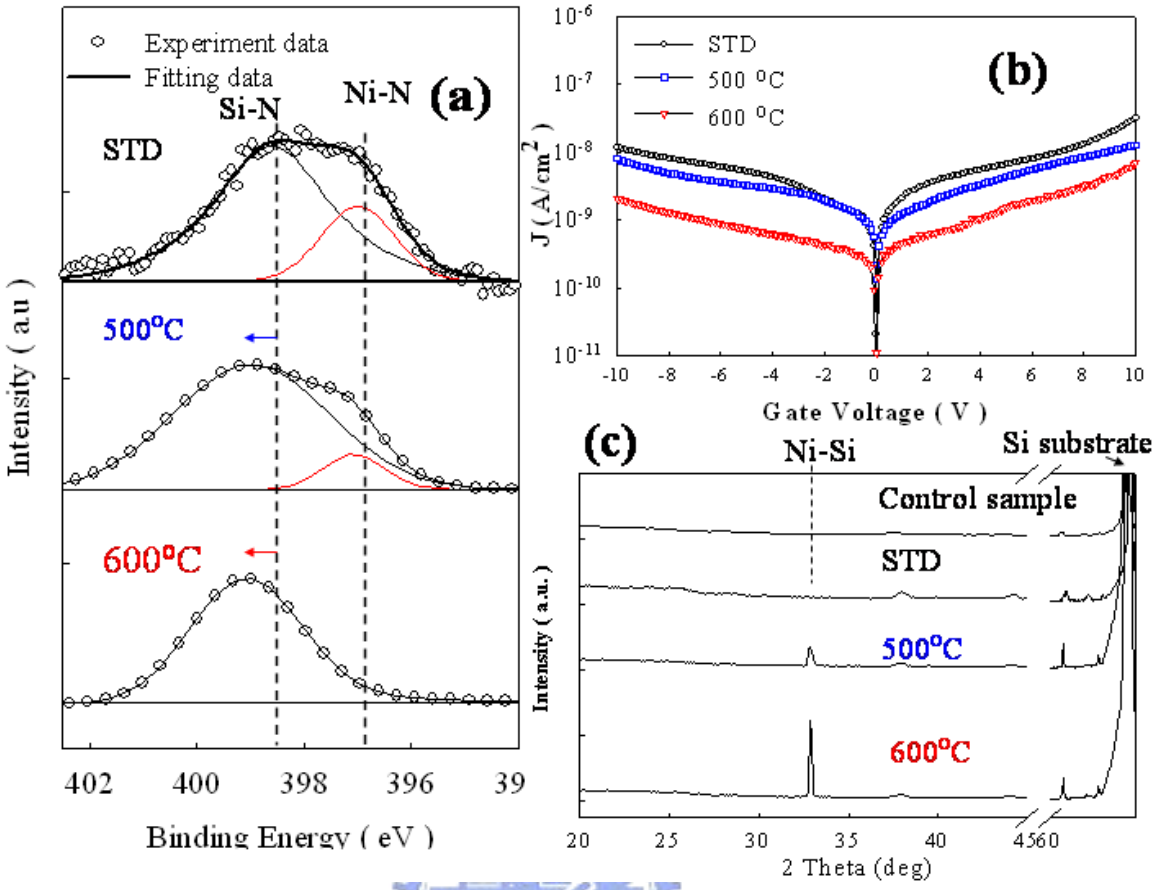


Figure 4-17 (a) N 1*s* x-ray photoelectron spectroscopy (XPS) analysis of the nanocrystals (Empty circles and straight line indicate experimental and fitting results, respectively). (b) Leakage current density (A/cm^2) with gate voltage and (c) X-ray diffraction (XRD) analysis of the nanocrystals during different thermal annealing temperature (Control sample is only a structure of Si substrate with 5-nm tunnel oxide).

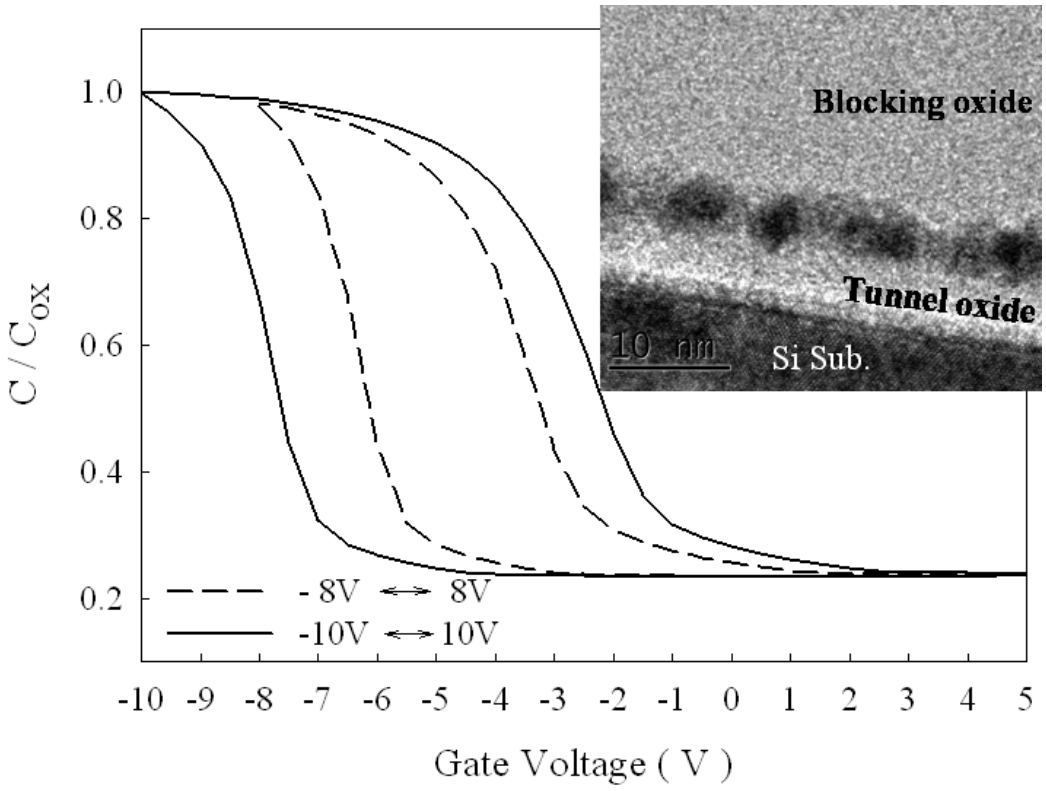


Figure 4-18 *C-V* hysteresis and TEM image (inset) of NiSi nanocrystals nonvolatile memories (500°C). The memory window was 5.0 V under ± 10 V operation.

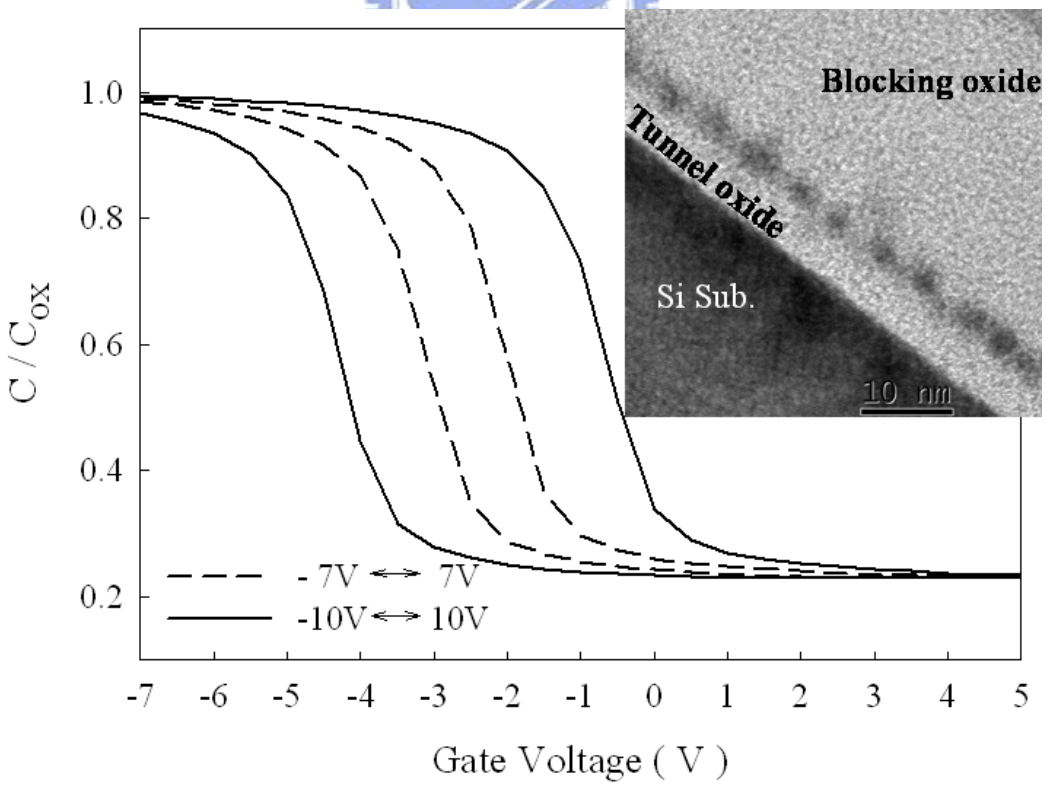


Figure 4-19 *C-V* hysteresis and TEM image (inset) of NiSi nanocrystals nonvolatile memories (600°C). The memory window was 4.0 V under ± 10 V operation.

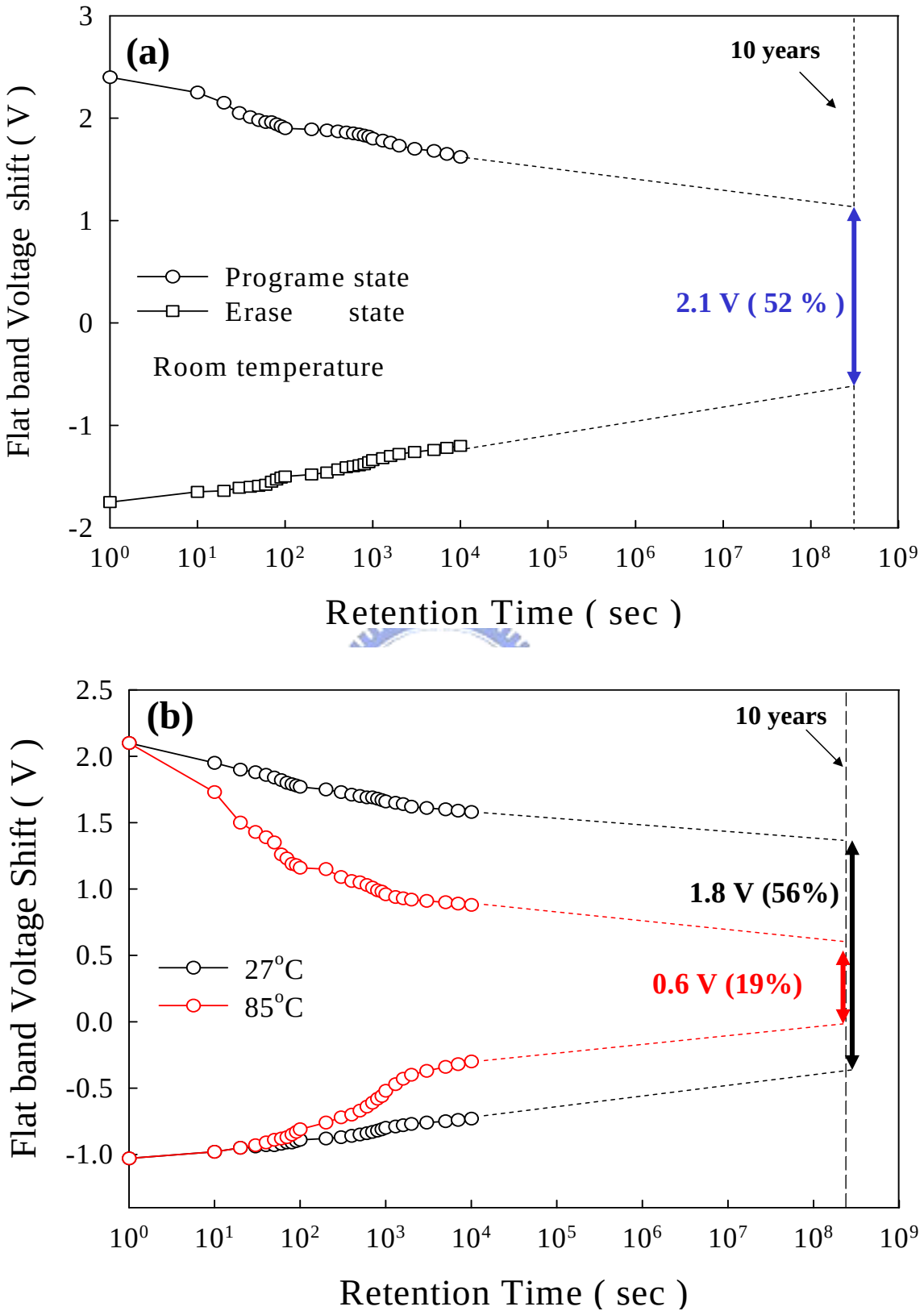
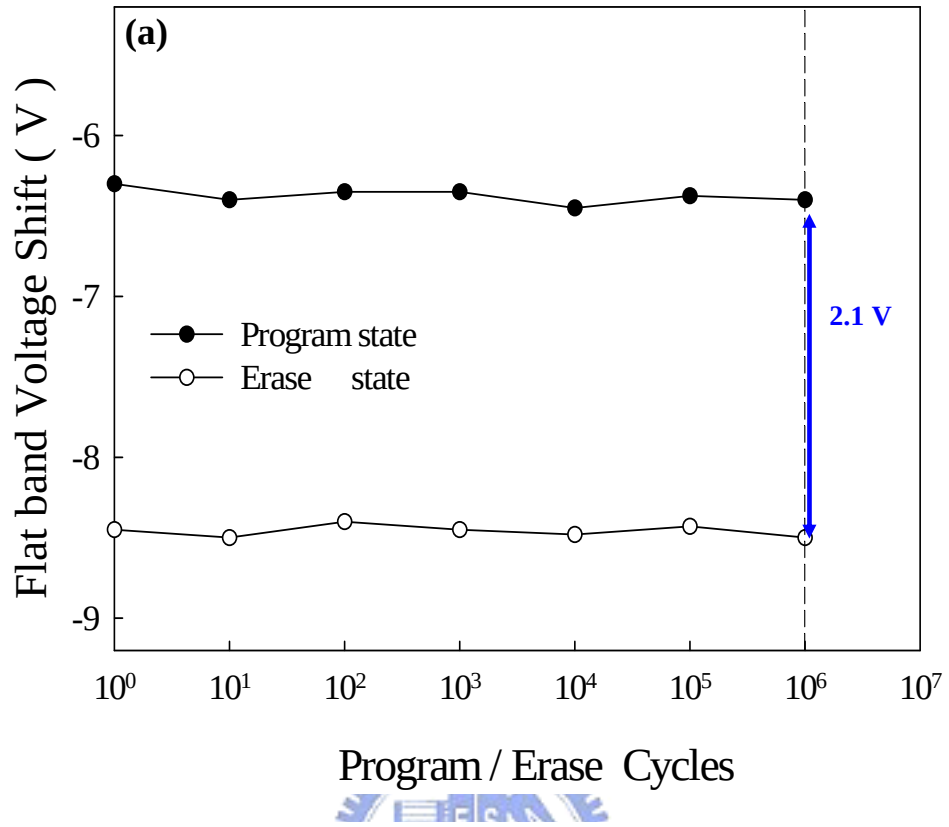


Figure 4-20 Retention characteristics of the NiSi nanocrystals nonvolatile memories through RTA treatment at (a) 500 °C for 100 sec and (b) 600 °C for 100 sec.



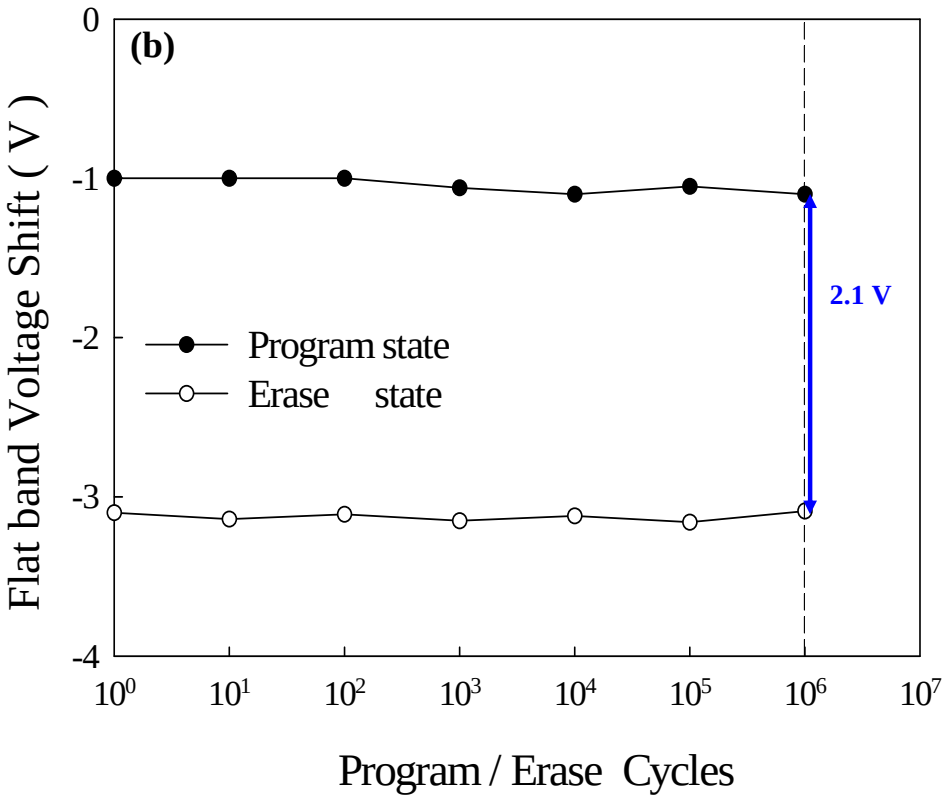
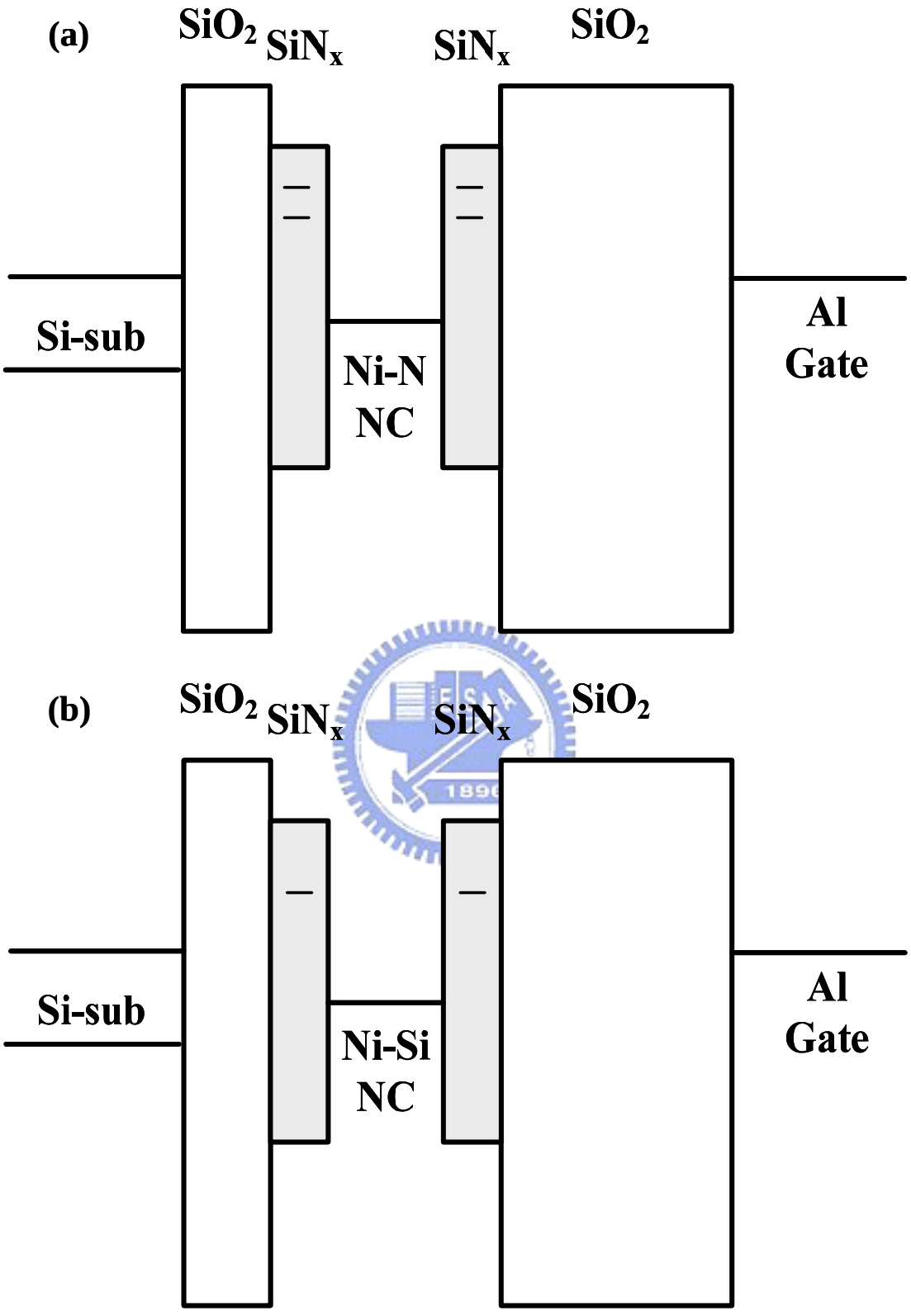


Figure 4-21 Endurance characteristics of the NiSi nanocrystals nonvolatile memories through RTA treatment at (a) 500 °C for 100 sec and (b) 600 °C for 100 sec.


(a)
SiO2
SiNx
SiNx
SiO2
Si-sub
Ni-N
NC
Al
Gate
(b)
SiO2
SiNx
SiNx
SiO2
Si-sub
Ni-Si
NC
Al
Gate

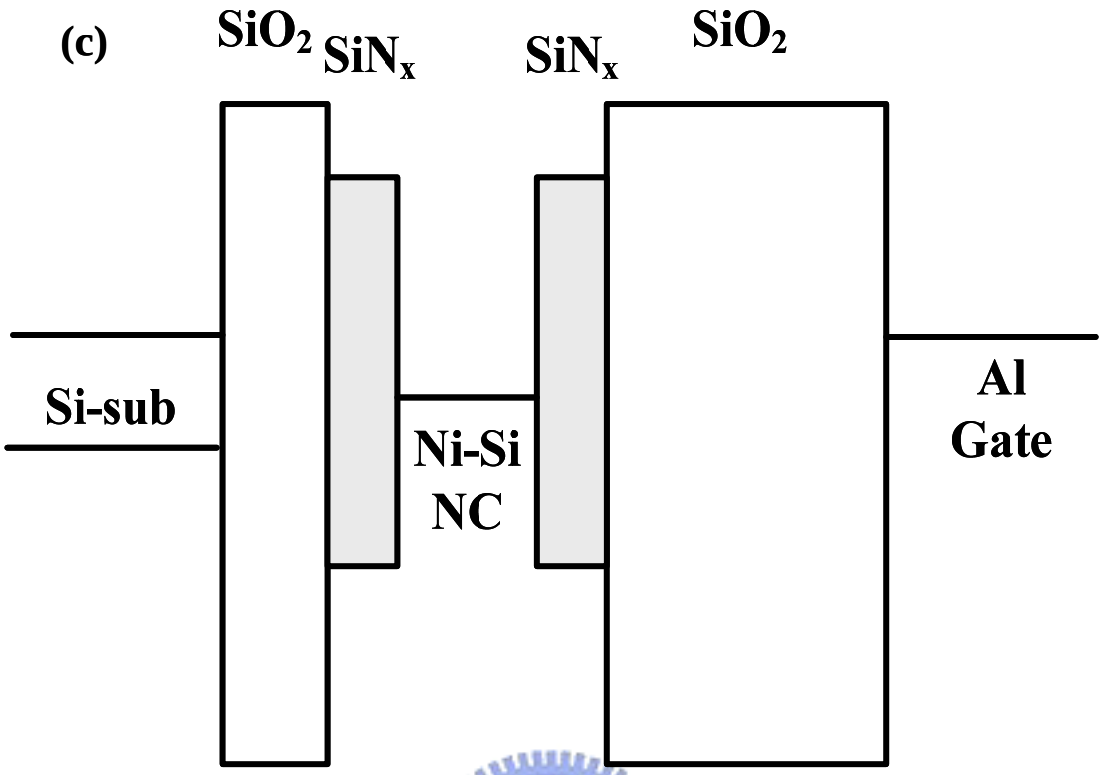


Figure 4-22 Energy band diagrams of (a) Ni-N NCs (STD), (b) Ni-Si NCs (500^{o}C) and (c) Ni-Si NCs (600^{o}C) embedded in nitride layer.

Table 4-3 Comparisons of memory characteristics for Ni-Si-N nanocrystal memory before and after RTA annealing in N_2.

Nonvolatile Memory	Memory window under ±10V	Memory window after 10 years (electrons holding ratio)	Memory window after 10^6 P/E cycles (degradation)
STD	1.5 V	0.5 V (20 %)	1.0 V (-50%)
500 ºC	5.0 V	0.7 V (31 %)	2.1 V (0%)
600 ºC	4.0 V	1.1 V (50 %)	2.1 V (0%)

4.4 Reliability characteristics of NiSi nanocrystals embedded in oxide and nitride layer for nonvolatile memory application

4.4.1 Introduction

Nonvolatile nanocrystals (NCs) memories have been promising candidates to substitute for the conventional nonvolatile floating gate memory, because the discrete traps served as the charge storage media have effectively improved the data retention for the scaling down process [4.51, 4.52]. Among various NCs for the nonvolatile memory technology, the metallic NCs were extensively investigated over semiconductor NCs because of several benefits, such as enhanced gate control ability (i.e., stronger coupling with the conduction channel), higher density of states, smaller energy disturbance and larger work function [4.53, 4.54]. However, the surrounding dielectric with NCs can not be ignored its importance in terms of density of NCs, retention and endurance. By the pervious studies, the high-k materials can be used to increase the density of NCs due to the nucleated sites effect and to achieve the better retention [4.55-4.57].

In this section, we presented the nonvolatile nickel-silicide (NiSi) NCs memories embedded in oxide and nitride layer, respectively. These proposed memory structures were compared for the reliability test, and then we also proposed a simply simulation of electric field to explain the advantages by using high-k dielectric surrounding with NCs.

4.4.2 Experiment

These nonvolatile NCs memory were fabricated on a 4 in. p-type silicon (100) wafer which the resistivity was about 20 Ωcm. After a standard RCA process which was removed native oxide and micro-particles, a 3-nm-thick tunnel oxide was grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition. Afterward, a 10-nm-thick oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer was deposited by sputtering of $Ni_{0.3}Si_{0.7}$ commixed target in the Ar [24 SCCM (SCCM denotes cubic centimeter per minute at STP)] and O_2 (2 SCCM) environment at room temperature. The DC sputtering power and pressure were set to 80 W and 7.6 mtorr. Next, the rapid thermal annealing (RTA) process was performed in N_2 ambient and the annealing conditions were settled at 600 ^oC for 100sec. In addition, we changed the charge trapping layer from the oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer to the nitrogen (10 SCCM) incorporated $Ni_{0.3}Si_{0.7}$ layer and the formation flow was used the same recipes including the deposition condition and annealing condition. Then, a 30-nm-thick blocking oxide was deposited by the plasma enhance chemical vapor deposition for the above-mentioned devices. Al electrodes on back and front side of the sample were finally deposited and patterned. The formation flows of nanocrystals embedded in nitride and oxide nonvolatile memories are shown in Fig. 4-23. Moreover, the electrical characteristics including the capacitance-voltage (C-V) hysteresis and reliability test were performed, which they were measured by Keithley 4200 and HP4284 Precision LCR Meter.

4.4.3 Results and discussion

Figure 8-2 shows the cross-sectional TEM image relative to the C-V characteristics of NiSi NCs embedded in oxide [Figs. 4-24(a) and (c)] and nitride [Figs. 4-24(b) and (d)] layer. In the comparison of TEM, it is found that the shape and density of NCs in Fig. 4-24(b) are superior to Fig. 4-24(a), because the incomplete silicon nitride (SiN_x) layer could keep thermal energy to enhance the self-assembled ability of NCs, and the dangling bonds of nitride also increased the nucleated sites to obtain high density of NC during the RTA process [4.57]. Hence, the memory window of NiSi NCs embedded in nitride layer (4.0 V) was larger than NiSi NCs embedded in oxide layer (2.0 V) under ± 10 V gate voltage operation.

To further investigate into the reliability of NiSi NCs embedded in oxide and nitride layer, the retention tests are shown in Fig. 4-25. We used the same programing (+10 V for 5sec) and erasing (-10 V for 5sec) conditions to treat these nonvolatile memories. The shift of flat band voltage (V_{FB}) as a function of time is obtained by comparing the C-V curves of charging state and quasi-state. According to the previous research, the memory window has the saturation phenomenon under the state of fixed charging voltage with long charging duration and all of trapped states (included sallow and deep states) are filled with storage carries [4.58]. Moreover, if the charges are trapped in the same stored sites, the escaping probability of storage charges will be increased by the coulomb blockade effect under retention test. In our work, Fig. 4-25(b) with NiSi NC embedded in nitride layer has better charge holding rate (56%) than Fig. 4-25(a) with NiSi NC embedded in oxide layer (50%) after 10 years. This result could be considered that the charges only were stored in the NCs for the NiSi NC embedded in oxide layer structure, but the nitride had the trapping states to trap charges and dispersed the distribution of storage charge resulting in a lower coulomb repulsive force in the charge trapping layer.

Figures 4-26(a) and (b) present the endurance characteristics of NiSi NC embedded in oxide and nitride under the pulse conditions of $V_G - V_{FB} = \pm 5$ V for 0.1 ms. From the data trend of Fig. 4-26(a), it is found that the variation of memory window is serious (memory window narrowing effect) after 10^6 P/E cycles. Nevertheless, the NiSi NC embedded in nitride reveals more stable memory window for the endurance test, as shown in Fig. 4-26(b). In order to clarify the influence of surrounding dielectric (oxide and nitride) and NCs on the behavior of endurance process, we provided a simple simulation of electric field distribution for the NCs surrounded with the dielectric structures to explain the above-mentioned degradation phenomenon, as shown in Figs. 4-27 and 4-28. The simulation conditions of NCs structures corresponded with the TEM image (as shown in Fig. 4-24) and the gate voltage was settled at the inversion state. Here we used the ISE (Integrated Systems Engineering) TCAD software to build the nanocrystal structure and model. The simulation nanocrystals structure conditions of tunnel oxide thickness, metal NCs diameter, blocking oxide thickness, and the distance between NCs and tunnel oxide/blocking oxide are set 3 nm, 5 nm, 30 nm, and 2 nm. In addition, the dielectric constants of SiO_2 and SiN were given to 3.9 and 7.5, respectively.

Figure 4-27 shows the electric field distribution of metal NCs embedded in oxide layer and the red line (black line) of inset is a distribution of vertical electric field across a single NC (without any NCs). To compare the range of maximum electric field (E_{max}) between the substrate and NC, it is clearly found that the average E_{max} of red line (9 MV/cm) are lager than the average E_{max} of black line (6 MV/cm) for the distance of 3-5 nm from the substrate, because of the stronger coupling effect of metal NCs than oxide. On the contrary, in Fig. 4-28, the diversity of average E_{max} of red (with NC) and black (without NCs) lines among the NC and Si substrate is less than that of NCs embedded in oxide. In the other words, the distribution of electric field

for metal NCs embedded in nitride layer was more uniform by the simulation analysis. Considering the influence of electric field distribution for the metal NCs embedded in oxide layer structure, the charges had larger tunneling probability in the tunnel oxide under the metal NCs, but the tunneling probability was almost the same in the tunnel oxide for the metal NCs embedded in nitride layer structure. Figure 4-29 shows the schematic sketches of stored charges transportation under Program/Erase operation for the MOIOS structure containing NiSi nanocrystals embedded in (a) oxide and (b) nitride. These schematic sketches were according to the simulation results and shown the different mode of stored charge injection between the NCs embedded in nitride and oxide layers [4.59].

Hence, the tunnel oxide below the NCs surrounded with the oxide layer would be degraded seriously under P/E cycling operation, because a large number of storage charges would cause the defects in the tunnel oxide during charges transportation process resulting in memory window narrowing effect [as shown in Fig. 4-26(a)]. In addition, the nitride had trapping centers to store the charges and the NCs surrounded with the nitride layer had the uniform tunneling probability. Therefore, the degradation result would be alleviated due to the distributed charge injection mode.

4.4.4 Conclusion

Nonvolatile NiSi NCs embedded in oxide and nitride layer memories using the low thermal budget were fabricated. These memory structures also exhibited enough memory windows to define the data information. However, nonvolatile NiSi NCs embedded in nitride layer memory has better reliability than nonvolatile NiSi NCs embedded in oxide memory. Moreover, the simulation of electric field distribution was enough to explain the divergence of NCs embedded in nitride and oxide layers in the endurance test which was due to the stored charges transportation mode.

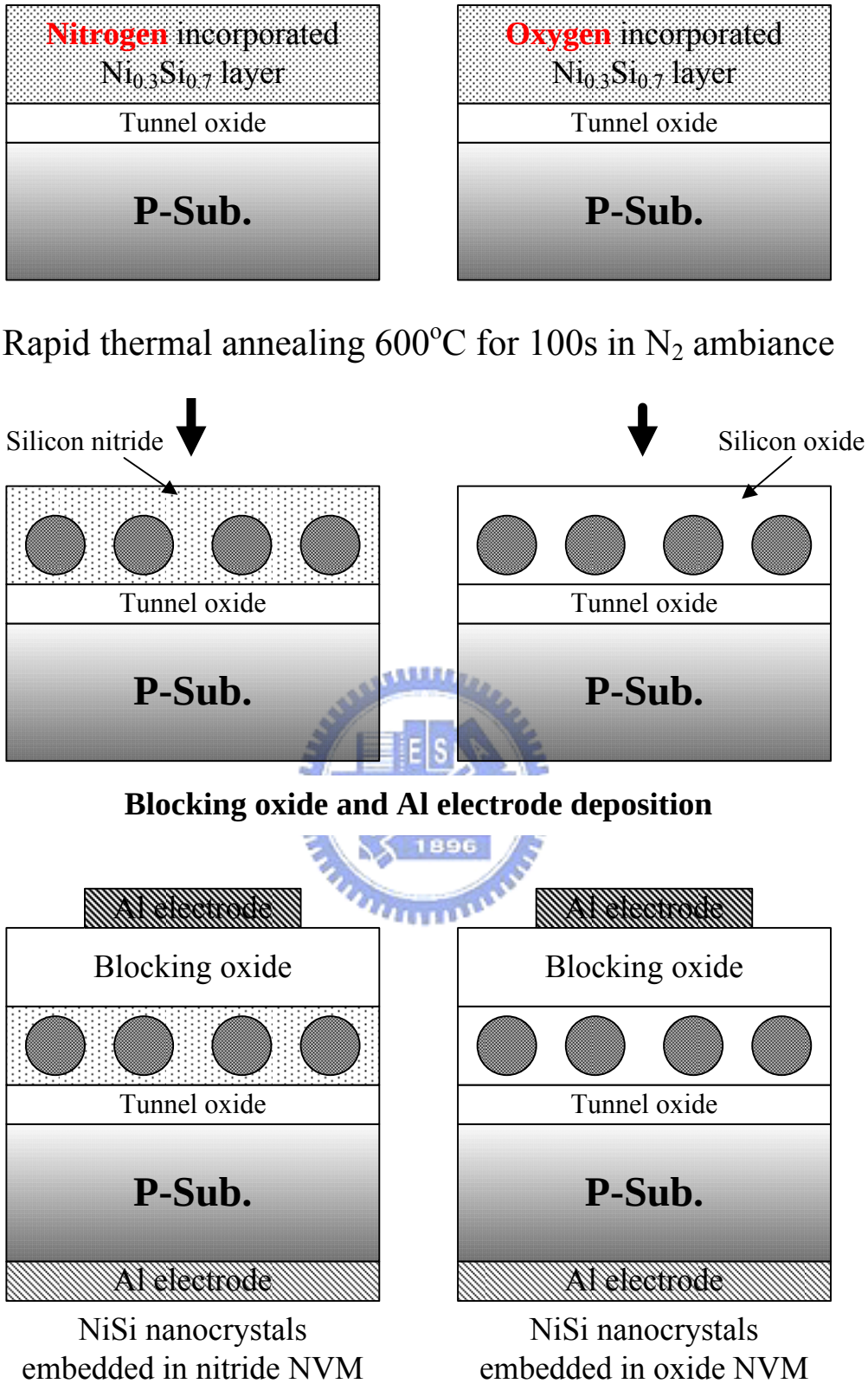


Figure 4-23 Formation flow of NiSi nanocrystals embedded in nitride and oxide nonvolatile memories.

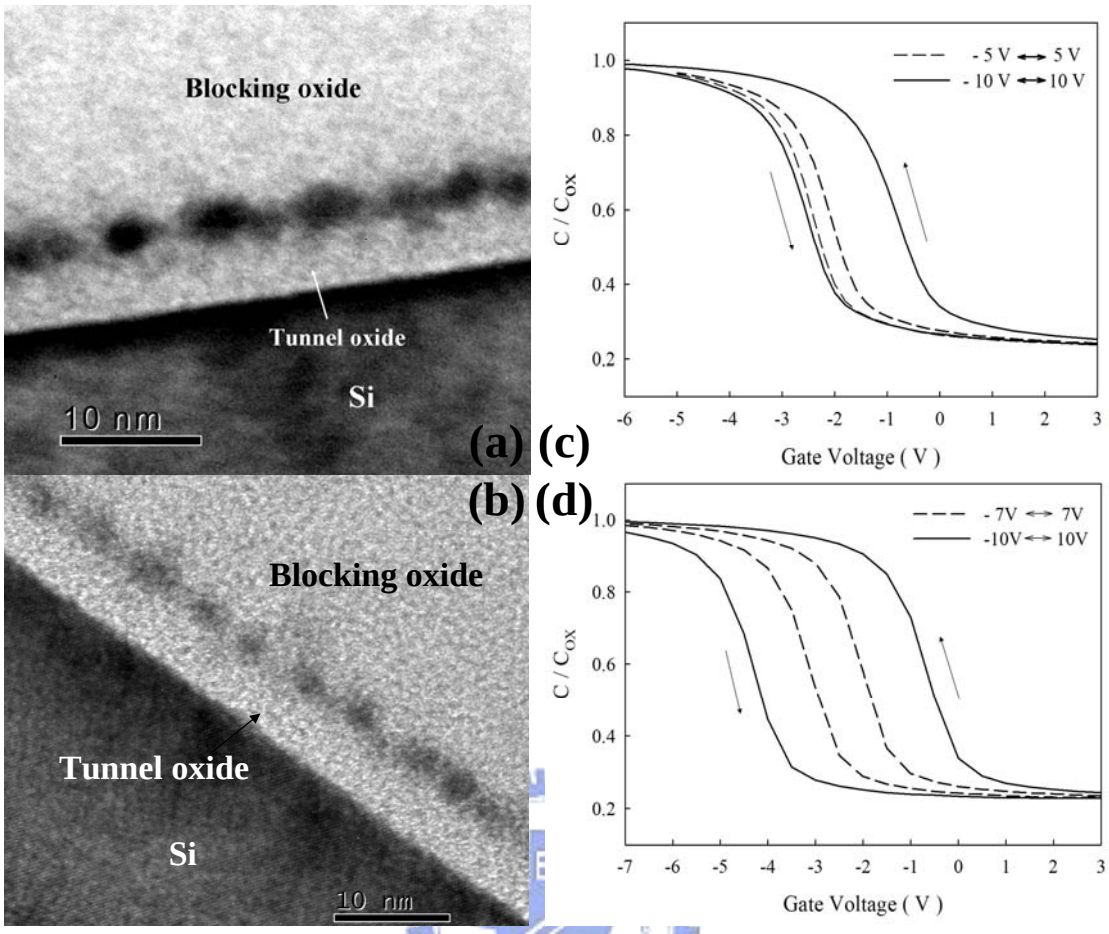


Figure 4-24 Cross-sectional TEM analysis of (a) NiSi NCs embedded in oxide layer, and (b) NiSi NCs embedded in nitride layer. *C-V* hysteresis of memory structure with (c) NiSi NCs embedded in oxide layer and (d) NiSi NCs embedded in nitride layer. The memory windows of (c) 2.0 V and (d) 4.0 V can be obtained under ±10 gate voltage operation, respectively.

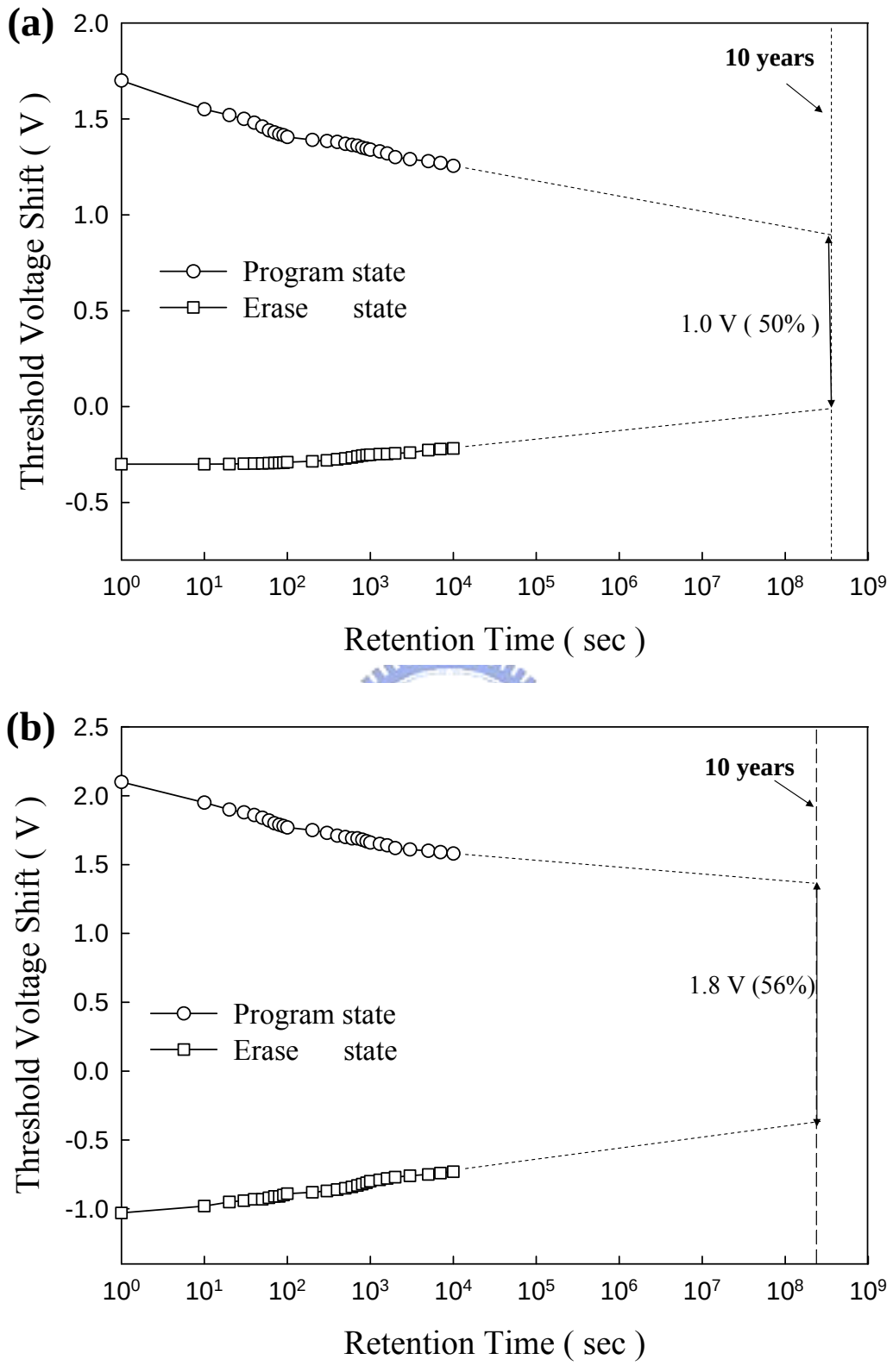
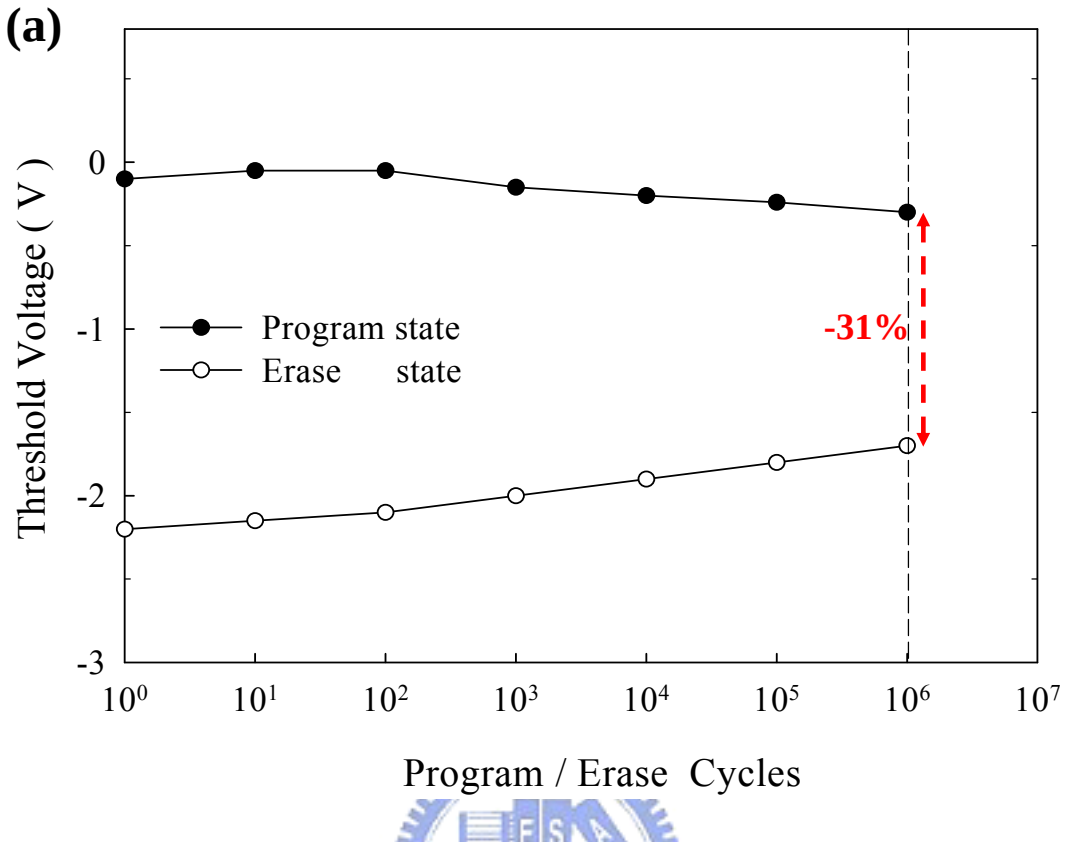


Figure 4-25 Retention of the NCs memory structure embedded in (a) oxide layer (charge holding rate: 50%) and (b) nitride layer (charge holding rate: 56%). The dotted line is the extrapolated value of retention data after 100 s, which this range is a steady state.



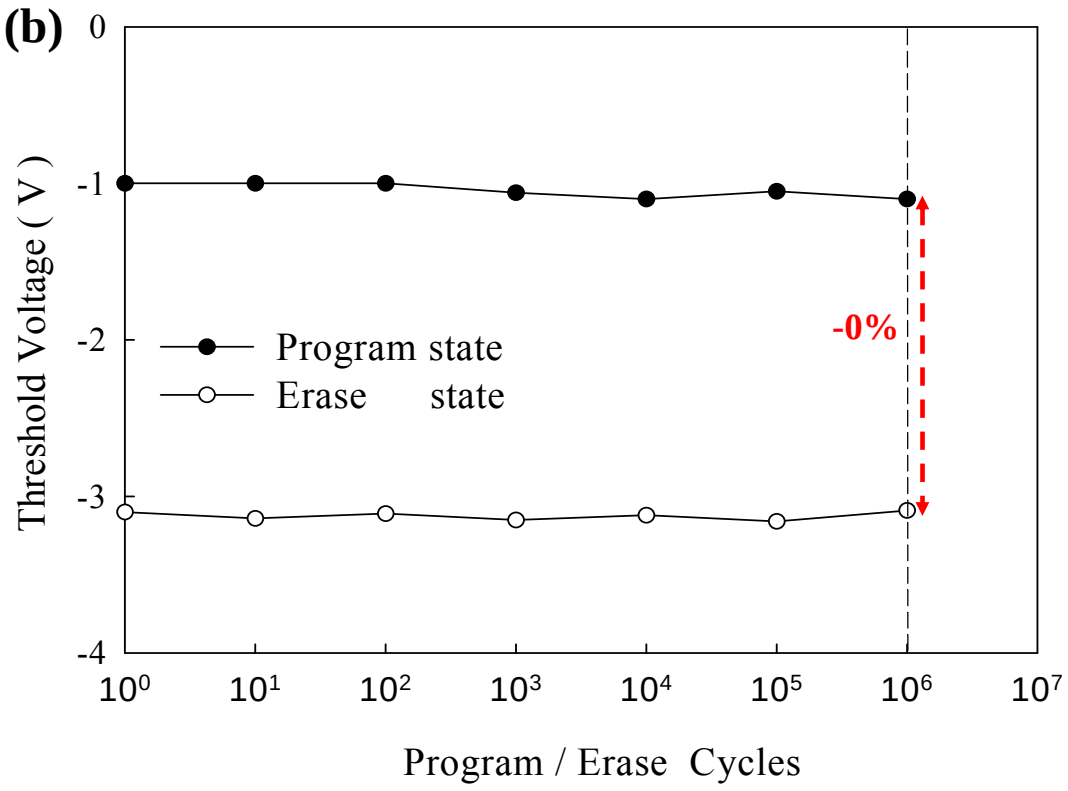


Figure 4-26 Endurance characteristics of the NCs memory structure embedded in (a) oxide layer and (b) nitride layer. Pulses condition of VG - VFB = ±5 V for 0.1 ms.

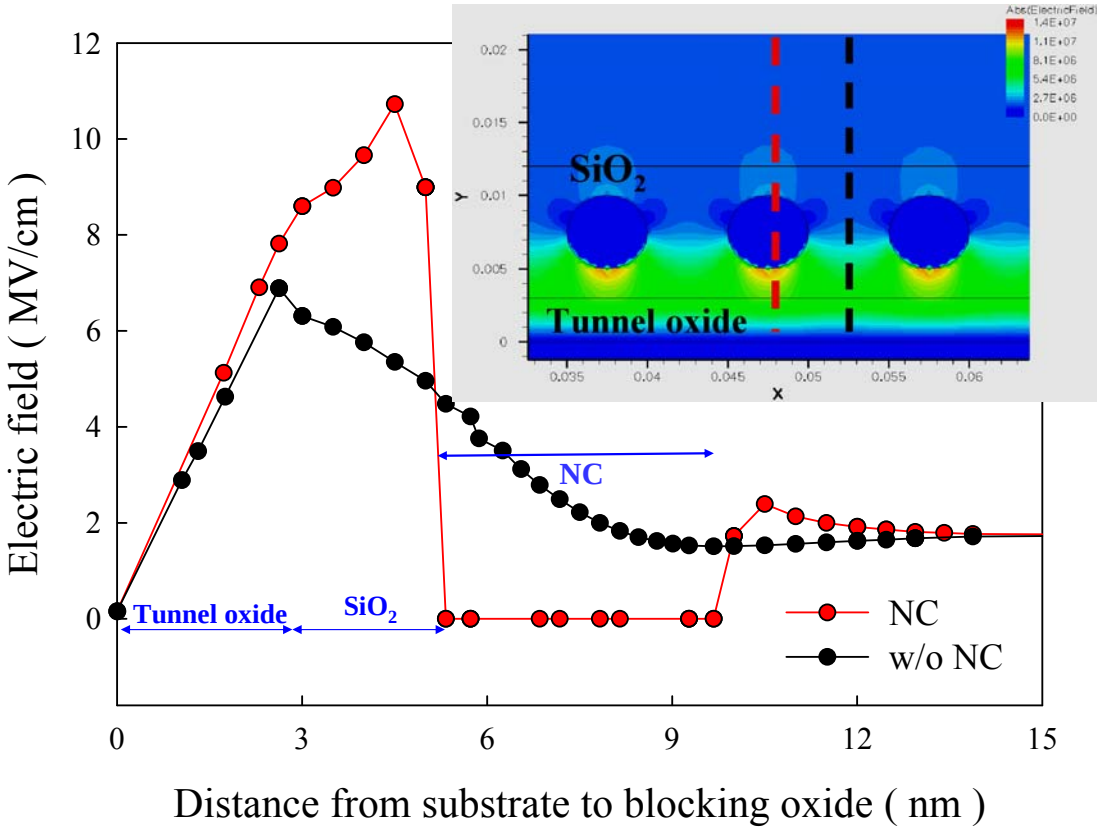


Figure 4-27 Simulation of electric field distribution of NiSi NCs embedded in oxide layer. The red line/black line of inset is a distribution of vertical electric field across a single NC/without any NCs. The simulation structure conditions of tunnel oxide thickness, metal NCs diameter, blocking oxide thickness, distance between NCs and tunnel oxide or blocking oxide are set 3 nm, 5 nm, 30 nm, and 2 nm. In addition, the dielectric constants of SiO_2 and SiN were given to 3.9 and 7.5, respectively.

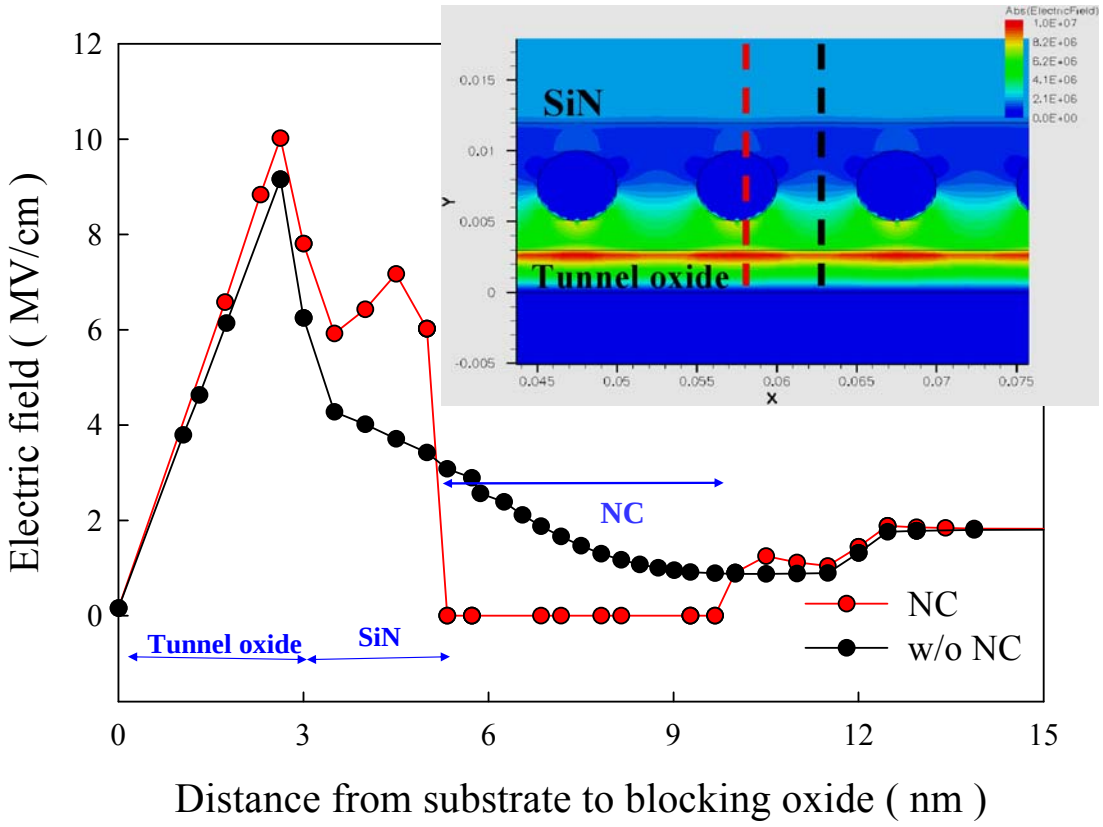


Figure 4-28 Simulation of electric field distribution of NiSi NCs embedded in nitride layer. The red line/black line of inset is a distribution of vertical electric field across a single NC/without any NCs. The simulation structure conditions of tunnel oxide thickness, metal NCs diameter, blocking oxide thickness, distance between NCs and tunnel oxide or blocking oxide are set 3 nm, 5 nm, 30 nm, and 2 nm. In addition, the dielectric constants of SiO_2 and SiN were given to 3.9 and 7.5, respectively.

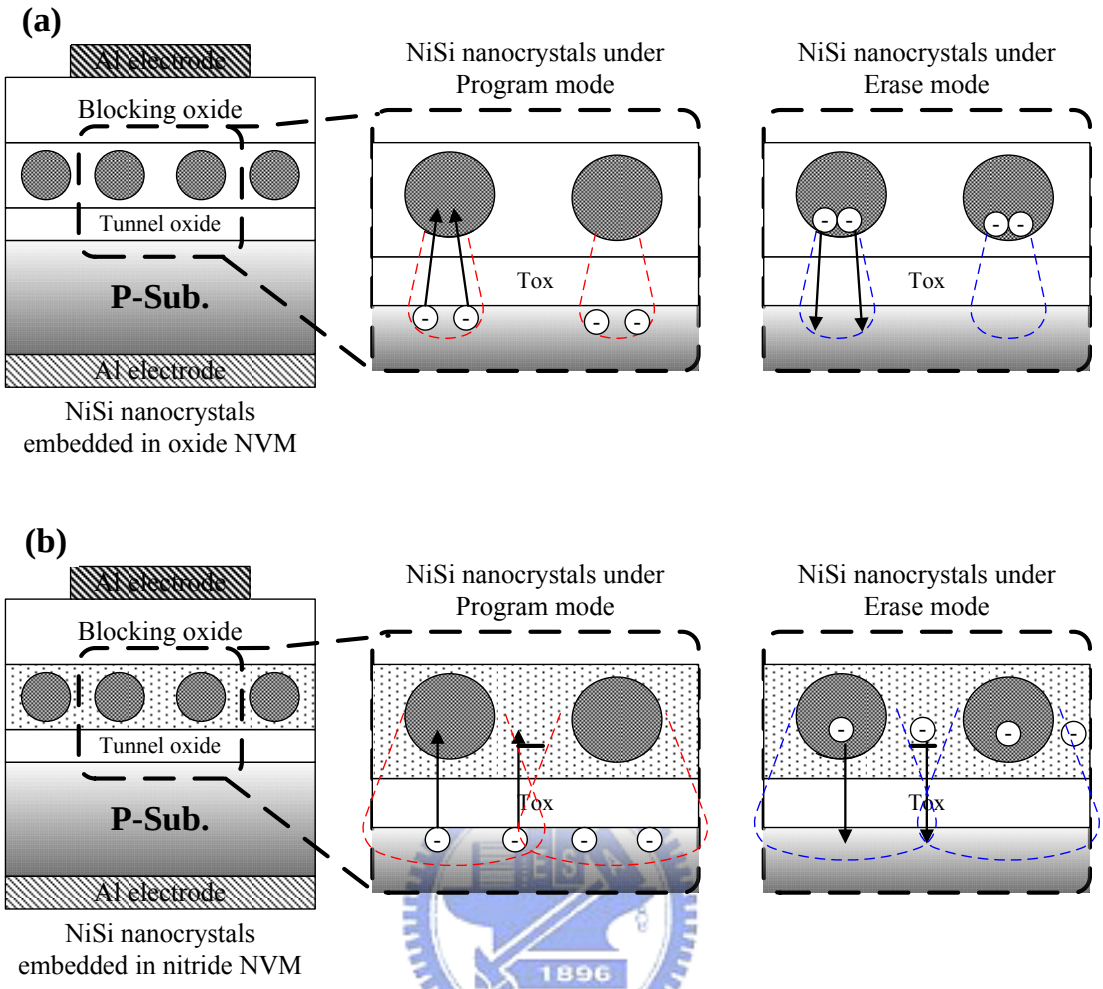


Figure 4-29 Schematic sketches of stored charges transportation under Program/Erase operation for the MOIOS structure containing NiSi nanocrystals embedded in (a) oxide and (b) nitride.

Chapter 5

Formation and Nonvolatile Memory Characteristics of Multi-layer Nickel-silicide NCs embedded in Nitride Layer

5.1 Introduction

Nonvolatile NCs (NCs) memories and SONOS-type memories have recently been promising candidates to take the place of the conventional floating gate nonvolatile memory, because the discrete quantum wells and traps as the charge storage media have effectively improved data retention for the scaling down devices [5.1-5.3]. Although the scaling down tunnel oxide (< 4 nm) is defect-free and high quality, it is still difficult to prevent the storage charges to leak into substrate under retention test. Because of the factor of quantum effect, the wave function of stored electrons can appear in the silicon substrate resulting in larger tunneling probability to increase the charge loss for retention state [5.4], [5.5]. In the pervious studies, the high-k materials can be used to increase the physical thickness of tunnel oxide layer and achieve the same efficiency for scaling down process, such as Si_3N_4, HfO_2 and Al_2O_3 [5.6], [5.8]. Moreover, C. Y. Ng et al. have proposed a densely stacked silicon NC layers to keep the better retention time, because the charges stored in the NCs near the blocking oxide have low tunnel probability to leak into substrate [5.7]. However, there are very few researches to investigate the formation and nonvolatile memory effect of multi-layer metal NCs.

In our work, the formation and charge storage effect of nonvolatile multi-layer nickel-silicide (NiSi) NCs memory (NMLNCM) were revealed. The NCs were formed by the Ni-Si-N thin film and this proposed memory structure was combined with the benefits of SONOS-type and multi-layer NCs. Hence, we used the

NMLNCM structure to compare with single-layer nickel-silicide NCs for the electrical characteristics of capacitance-voltage (C-V), retention and endurance test in this study.

5.2 Experiment

This memory-cell structure was fabricated on a 4 in. p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, a 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace. Subsequently, a 10-nm-thick nitrogen incorporated $Ni_{0.3}Si_{0.7}$ layer served as the charge trapping layer was deposited by reactive sputtering of $Ni_{0.3}Si_{0.7}$ commixed target in the Ar (24 SCCM) and N_2 (10 SCCM) environment at room temperature. The dc sputtering power and pressure were set to 80 W and 7.6 mtorr. Here, the ratio of commixed target (Ni:Si) was decided by the volumes of NCs and surrounding dielectric. Next, a rapid thermal annealing (RTA) process was performed in N_2 ambient and the annealing condition was 600^{o}C for 100sec. After the annealing step, the NCs would self-assemble in the dielectric layer and the single-layer NCs memory structure was formed by capping a 30-nm-thick SiO_2 as the blocking oxide. The cross-sectional transmission electron microscope (TEM) and fabrication flow of NCs embedded in the nitride layer are shown in Fig. 5-1.

Moreover, we used this internal competition mechanism of Ni-Si-N thin film to fabricate the second NiSi NCs layer of multi-layer memory sample and the annealing condition imitated the formed state of our first NCs layer. Then, a 20-nm-thick blocking oxide was deposited on the charge trapping layer to completely make a multi-layer NiSi NCs memory. Finally, Al gate electrodes on back and front side of the samples were deposited and patterned for our proposed memory structures. Form

the NMLNCM cross-sectional TEM image of Fig. 5-2, it is found that the first deposited NCs layer was separated to two layers and we believed this phenomenon was caused by a partial of NiSi NCs diffusing into SiN_x during the second RTA process (the conjectured formation flow of multi-layer NCs structure is also shown in Fig. 5-2) [5.9-5.11]. Therefore, the upper-layer NC size (5-6 nm) is larger than lower-layer (2-3 nm) and we can use this material characteristic to fabricate the multi-layer NCs. By TEM image analysis, there were totally three layers of NCs in this proposed memory structure and the physical thickness of memory cell was the same with single-layer memory structure. Because of this, we were very interested in the nonvolatile memory effect of multi-layer compared with single-layer NCs.

5.3 Results and discussion

Figure 5-3(a) shows the C-V characteristics of single-layer NCs structure and its memory window is only about 4.0 V under ±10 V gate voltage operation. However, the multi-layer NCs structure is clearly observed that the memory windows of 5 V and 13 V can be obtained under ±5 V and ±10 V operation, respectively, as shown in Fig. 5-3(b). The C-V hysteresis loops are counterclockwise, which is due to injection of electrons from the deep inversion layer and injection of holes from the deep accumulation layer of Si substrate [5.12]. The memory window of multi-layer NC structure was much larger than the single-layer NCs at the same voltage sweeping (±10 V) condition. The enhancement of storage capacity was attributed to the high density number of NCs (three-dimensional structure) and strong coupling with conduction channel of metal NCs which was related to the high dielectric constant of charge trapping layer [5.13], [5.14]. In addition, the difference of flat-band voltage between single-layer and multi-layer was also due to strong coupling with conduction channel by the metal NCs density. The high density of metal NCs can enhance the

gate control ability in our work. Moreover, the large charge storage ability at scale-down devices can be maintained for the multi-layer structure with NCs embedded in the nitride.

The endurance characteristics of multi-layer NCs and single-layer NCs are provided in Fig. 5-4. Pulses condition of $V_G - V_{FB} = \pm 5$ V for 0.1 ms were applied to evaluate endurance characteristics for the Program/Erase cycles operations. In the endurance test, first, we used this pulse condition to stress our samples and then programmed to a program state or erased to an erase state. After that, we used the read mode to detect the flat band voltage, V_{FB} (Read mode: The V_{FB} is obtained by comparing the *C-V* curves from a charged state or a quasi-neutral state). Figures 5-4(a) and (b) all show the negligible degradation of memory window up to 10^6 P/E cycles for the multi-layer structure and single-layer. In the endurance test, our proposed memory structures had the advantages for the nonvolatile memory application.

Further analysis of the reliability indicated that the charge retention properties of single-layer and multi-layer NCs memory structures at 27°C and 85°C are demonstrated in Figs. 5-5(a) and (b), respectively. This measurement results were carried out using a fixed gate voltage stress (± 5 V for 10 ms at 27°C and 85°C) and the shift in the flat band voltage as a function of time is obtained by comparing the C-V curves. Form Fig. 5-5(a), we used an extrapolation to give a long-term predictable result (solid and dotted line) after 1000s (stable region of retention) [5.15]. We find that single-layer and multi-layer NiSi NCs all have good chare storage ability and get up to 10 years at room temperature, as shown in Fig. 5-5(a).

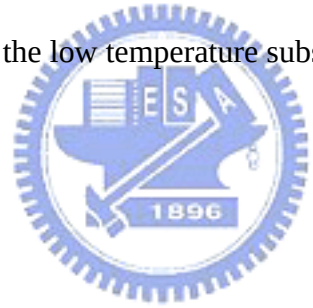
However, a serious condition of 85°C can show the advantages of multi-layer NiSi NCs memory and it is found that the charge loss ratio of multi-layer is much lower than single-layer NCs. In this study, we found the leakage currents of single and multi layer NCs memories were very small. Therefore, the blocking oxide was enough

to block the stored electrons to leak into the Al gate. If the stored electrons loss is due to lateral migration effect, the retention test of single and multi layer NCs memories under 85℃ will have the same results. The biggest difference of single and multi layer NCs memory is the position of main stored carriers. The position of main stored carriers for only single layer NCs memory is like the first NCs layer of multi-layer NCs memory. However, the position of main stored carriers for multi-layer NCs memory is the third NCs layer.

Hence, based on the TEM images, we established a energy band diagram of multi-layer NCs embedded in SiN_x layer (as shown in Fig. 5-6) to consider that the reason was due to the charges stored in the upper-layer NCs (the third layer of multi-layer structure) that can be suppressed to leak into substrate under thermal test by the coulomb blockade effect and energy level quantization of the lower-layer NCs (the first and second layers of multi-layer structure) [5.16, 5.17]. The coulomb blockade effect was cause by the carriers existed in second layer NCs (as shown in the second layer of energy band diagram) and this stored charge reduced the electron loss probability from the third layer to the first layer. In addition, the energy level quantization of NCs is limited to the size and effective mass of NC by the theoretical simulation of W. Guan et al. [5.17]. Hence, in this model, the ground states (Fermi level) of first and second layer of multi-layer structure were higher than the third layer because their NC size was smaller than 3 nm. This Fermi level shift can partially suppress the electrons stored in the third NC layer to leak into the first and second NC layers under thermal test. We also depicted this physical phenomenon in the Fig. 5-6 to appear that the nonvolatile multi-layer nickel-silicide NCs memory can effectively keep carriers in the charge trapping layer for a harsh environment.

5.4 Conclusion

In this study we adopted the Ni-Si-N thin film to easy fabricate the NiSi NCs embedded in SiN layer after a RTA process and also proposed a nonvolatile NiSi NCs memory with multi-layer using low thermal budget. This multi-layer NCs structure exhibited superior memory performance for the charge storage capacity and reliability more than single-layer NCs sample. A larger memory window of 13 V was clearly observed after ±10V voltage sweep and the retention can get up to 10 y for next-generation nonvolatile memory application. We also provided an energy band diagram of multi-layer NCs structure to display the predominance of NMLNCM at scaling down process. In addition, this formation technique of charge trapping structure was also suitable for the low temperature substrate on the flexible electronics application.



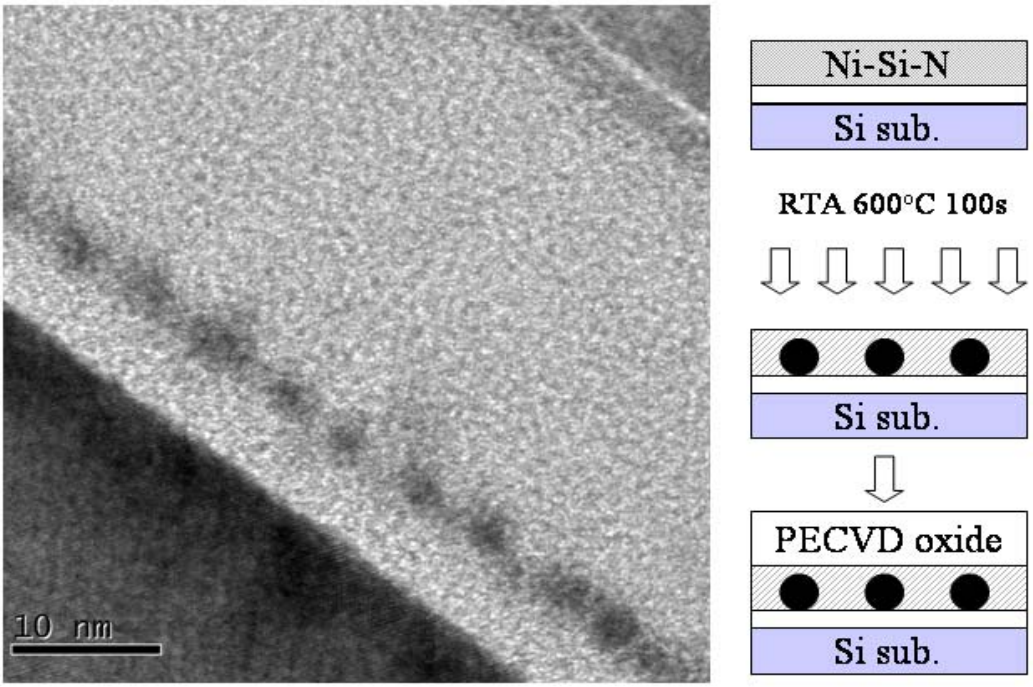


Figure 5-1 Cross-sectional transmission electron microscope and fabrication flow of NiSi NCs embedded in the nitride layer (Single-layer NCs nonvolatile memory).

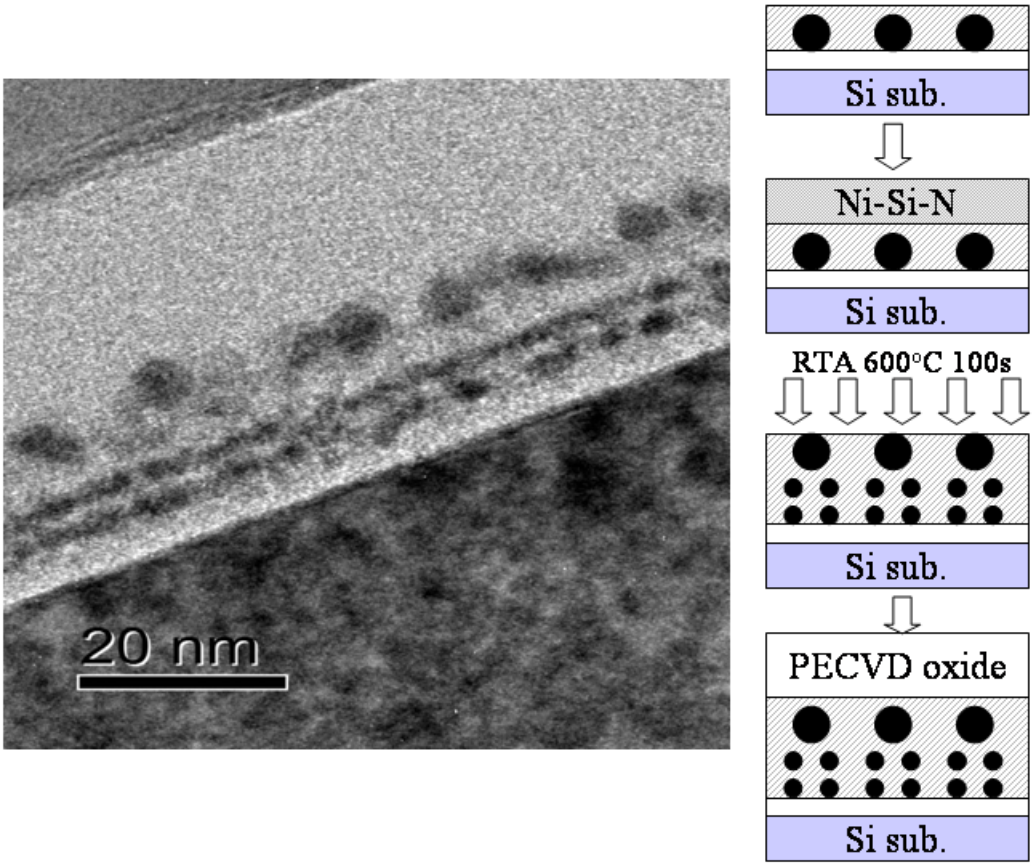
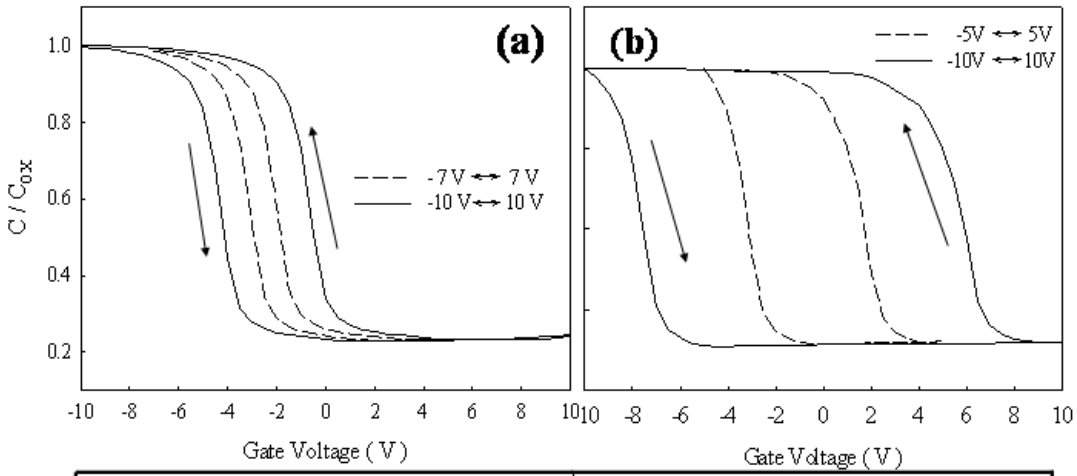


Figure 5-2 Cross-sectional transmission electron microscope and fabrication flow of NiSi NCs embedded in the nitride layer (Multi-layer NCs nonvolatile memory).



Nonvolatile Memory	Memory window under ±10V
(a) Single-layer NiSi Nanocrystals	4.0 V
(b) Multi-layer NiSi Nanocrystals	13.0 V

Figure 5-3 Capacitance-voltage (*C-V*) hystereses of memory structure with (a) single-layer and (b) multi-layer NCs. The memory windows of (a) 4.0 V and (b) 13.0 V can be obtained under ±10 gate voltage operation, respectively.

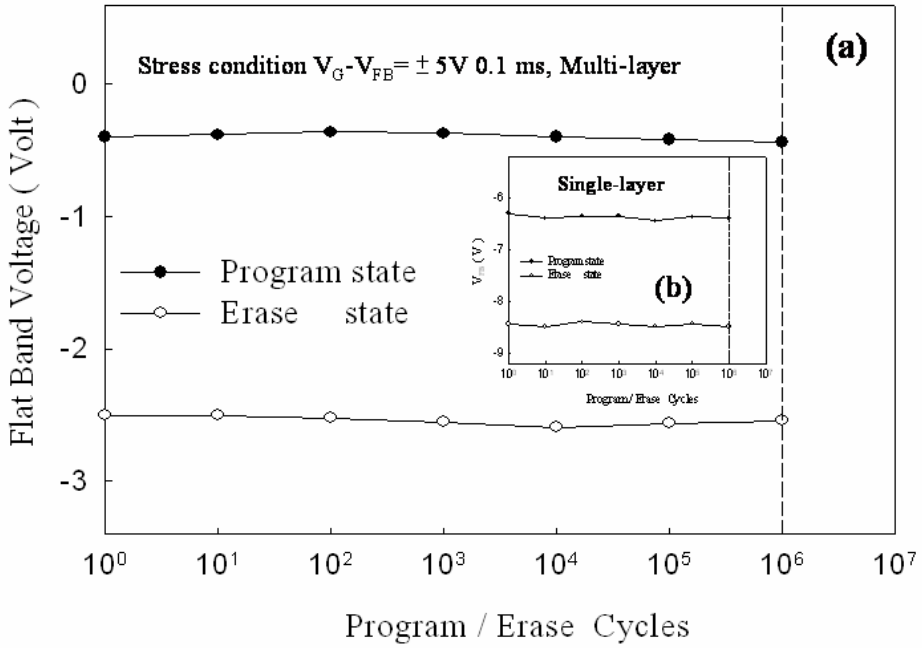


Figure 5-4 Endurance characteristics of (a) multi-layer NiSi NC memory and (b) single-layer NiSi NC memory. Pulses condition of V_G - V_{FB} = ±5 V and 0.1 ms.

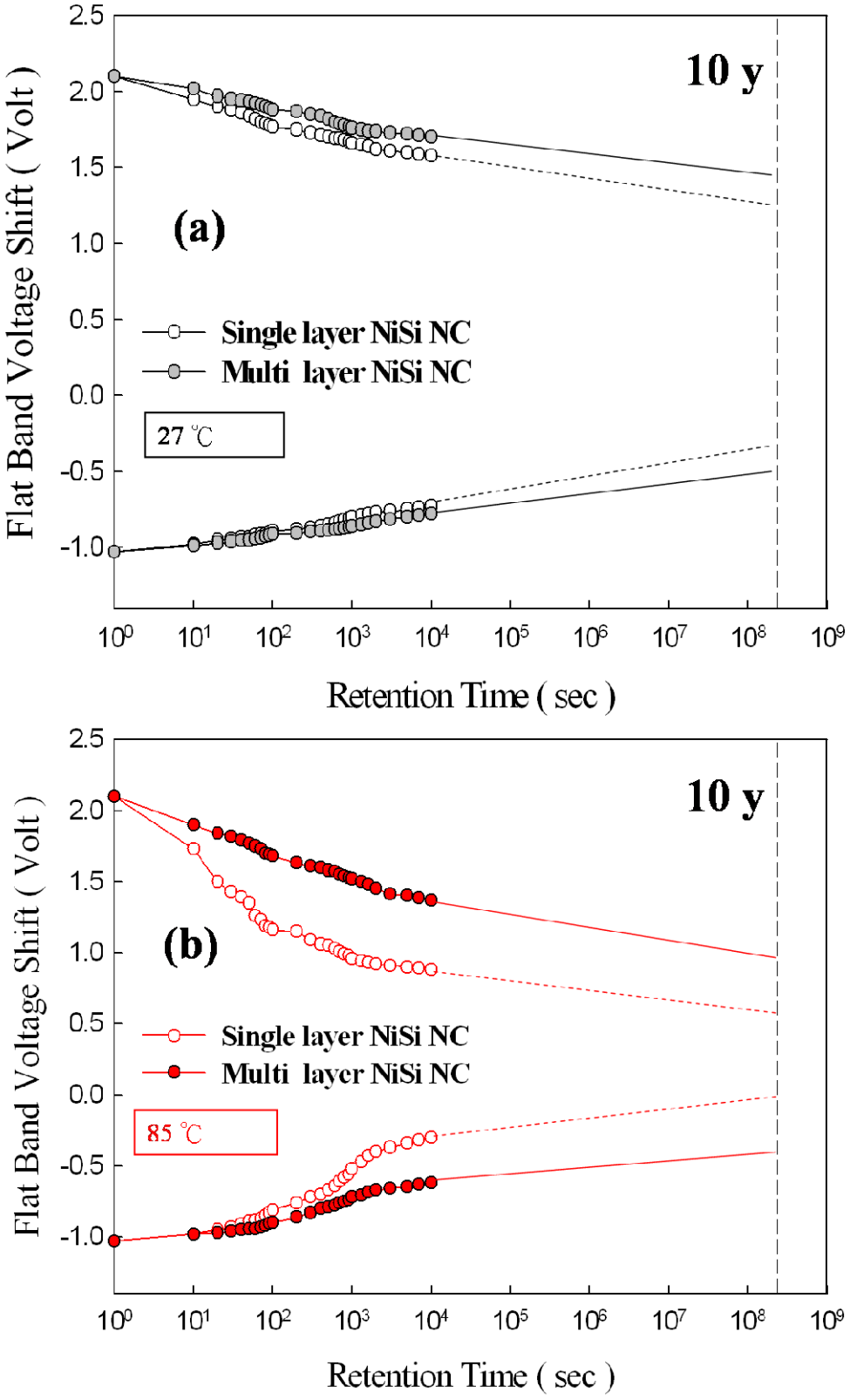


Figure 5-5 Retention characteristics of the NCs memory structure with (a) room temperature, 27°C and (b) 85°C. The dotted line and solid line are the extrapolated value of retention data after 1000 s, which this range is a steady state.

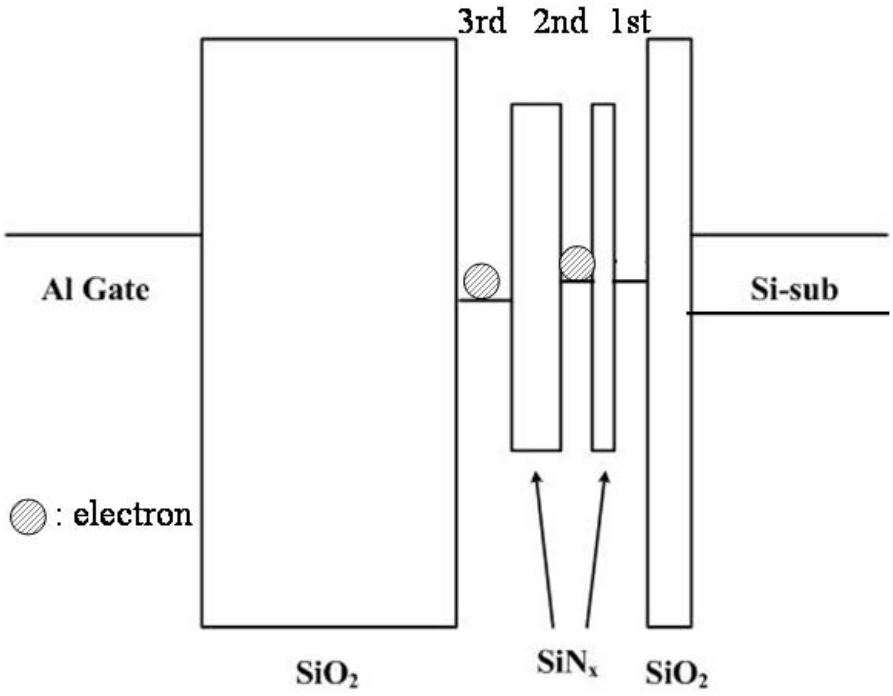


Figure 5-6 Energy bond diagram of multi-layer NiSi NCs embedded in SiN_x. The ground states of first and second layer of multi-layer structure were caused by the energy level quantization effect.

Chapter 6

Nonvolatile Memory Effect of Single-layer and Dual Layer Manganese Silicate ($MnSiO_x$) Nanocrystals

6.1 Introduction

Recently, nonvolatile memory (NVM) devices are moving toward high density cell array, low operation voltage, and good reliability. However, the conventional NVM with a floating gate (FG) structure cannot efficaciously prevent data loss in terms of reliability trials for the future scaling down process of tunneling oxide engineering [6.1]. Hence, the next-generation NVM is needed to employ discrete traps or quantum wells as charge storage media to improve retention time. The silicon-oxide-nitride-oxide semiconductor (SONOS) type and nanocrystals (NCs) memory structures have been currently proposed [6.2, 6.3]. In the past few years, many research have shown the high-k material served as charge trapping layer as the potential candidates for replacing the SiN layer [6.4] , and also demonstrated various NCs to provide the charge storage node, such as silicon (Si), germanium (Ge) and metallic NCs [6.5, 6.6]. Additionally, to use dielectric NCs with high-k material are also investigated by C. H. Chien et al., such as hafnium oxide (HfO_2) and Cerium oxide (CeO_2) NCs [6.7, 6.8]. These dielectric NCs NVMs are similar to the SONOS-type NVMs, but have more separable trap distribution due to NC structure.

Hence, in this study, we have proposed a dielectric NC, manganese silicate ($MnSiO_x$), and successfully fabricated it by a simple process flow. This $MnSiO_x$ NCs are considered that the charges are stored in the discrete traps of dielectric NCs and the distribution of storage charges are dispersed resulting in a lower Coulomb repulsive force in the charge trapping layer. Therefore, good data retention of $MnSiO_x$

NCs for the next-generation NVMs will be discussed.

6.2 Experiment

Figures 6-1 exhibits schematics of the experimental procedures. The fabrication of NCs NVM structures were started with a thermal dry oxidation at 950°C to form a tunnel oxide about 5 nm on *p*-type (100) Si wafer which had been removed native oxide and micro-particles by RCA process, and then 1-nm-thick a-Si and 9-nm-thick $Mn_{0.2}Si_{0.8}$ served as a charge tapping layer were deposited by reactive sputtering in the Ar [24 SCCM (SCCM denotes cubic centimeter per minute at STP)] ambiance at room temperature. Before the rapid thermal annealing (RTA) process at 800°C for 30 s in the O_2 ambiance, the charge trapping layer was capped by a 10-nm-thick oxide using the plasma enhanced chemical vapor deposition system at 300°C (PACO process). The RTO process was performed to cause the self-assembly of $MnSiO_x$ NCs in the charge trapping layer. After RTO process, a 20-nm-thick blocking oxide was also deposited by PECVD. This sample was denoted the sample C.

In addition, we changed the fabrication process of charge trapping layer which was deposited 1-nm-thick a-Si and 9-nm-thick $Mn_{0.2}Si_{0.8}$ by sputtering in the Ar/O_2 (24/1 SCCM) ambiance at room temperature. The RTA process at 800°C for 30 s in the N_2 ambiance was performed to cause the self-assembly of $MnSiO_x$ NCs in the charge trapping layer. According to previous studies, contrary to conventional RTO process, sputtering in the Ar/O_2 ambiance can avoid over oxidation [6.9]. After RTN process, a 30-nm-thick blocking oxide was deposited by PECVD at 300°C. This sample was denoted the sample D. The sample C and D were finally deposited Al gate electrodes to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure, as shown in Fig. 6-1. Electrical characteristics of the capacitance-voltage (*C*-*V*) hysteresis were also measured by HP4284 precision *LCR* meter with high frequency of 1 MHz.

Moreover, transmission electron microscope (TEM) and x-ray photoelectron spectroscopy (XPS) were adopted for the microstructure analysis and chemical material analysis of NCs.

6.3 Results and Discussion

6.3.1 Material and electrical characteristics of Mn silicate ($MnSiO_x$) NC NVMs

Figures 6-2(a) and (c) show the cross-sectional TEM images of NCs embedded in oxide layer of sample C and D. From the plane-view image of TEM analysis in Fig. 6-2(b), the NC diameter of sample C is approximately 8-10 nm and the density of the NCs is estimated to be about 8.09×10^{11} cm^{-2}. The crystallized NCs with obviously visible lattice images are evident in the insets. Furthermore, the average NC diameter of sample D is approximately 5-6 nm and the area density of the NCs is estimated to be about 2.33×10^{12} cm^{-2}, as shown in Fig. 6-2(c). In these cross-sectional TEM analyses, it was obviously found that less Mn atoms reacted with tunnel oxide during the RTA process due to the first deposited 1-nm-thick a-Si that protected our tunnel oxide.

In our work, the chemical composition of the NCs is demonstrated by XPS analysis using an Al Kα (1486.6 eV) x-ray radiation, as shown in Fig. 6-3. Fig. 6-3(a) exhibits the XPS Mn 2*p* core-level photoemission spectra that indicated the component is possibly $MnSiO_3$ (642.3 eV) or manganese oxide, not Mn silicide (it cannot find any signal position is lower than 640 eV) [6.10]. The O 1*s* peak shows Mn silicate centered at 531±0.2 eV from Fig.6-3(b) [6.11]. According to the previous research, Mn oxide is centered on the values below 530 eV by the XPS O 1*s* analysis [6.12]. We can believe that the main component of NCs in this trapping layer is Mn silicate (MnSiO).

In addition, we also considered Gibbs free energy, the actual value for chemical

reactions involving Mn silicate and SiO_2 formation. Here are some allowed chemical reactions to be listed below [6.13, 6.14].

$$\mathbf{Si + O_2 \rightarrow SiO_2 \quad \Delta G_{298K}^{0} = -732.94\ KJ/mol} \qquad (6\text{-}1)$$

$$\mathbf{Mn + 1/2\ O_2 \rightarrow MnO \quad \Delta G_{973K}^{0} = -615.03\ KJ/mol} \qquad (6\text{-}2)$$

$$\mathbf{MnO + SiO_2 \rightarrow MnSiO_3 \quad \Delta G_{298K}^{0} = -1244.7\ KJ/mol} \qquad (6\text{-}3)$$

$$\mathbf{MnO + 1/6\ O_2 \rightarrow 1/3\ Mn_3O_4 \quad \Delta G_{973K}^{0} = -206.34\ KJ/mol} \qquad (6\text{-}4)$$

According to these chemical reactions by Gibbs free energy analysis, Mn prefers forming MnO compound first and then MnO reacts with SiO to form the $MnSiO_3$ NC embedded in oxide.

Figure 6-4 shows capacitance-voltage (*C-V)* hysteresis of MOIOS structure for the (a) sample C and (b) D. The memory windows of two samples are nearly equal to 1 and 2.5 V under V_G-V_{FB}= ±5 V dash line and ±10 V solid line gate voltage operation, respectively. The *C-V* hysteresis slope of MOIOS structure by the sample D shows less interface damage of tunneling oxide at RTN process. For the sample C, we extrapolate a large number of oxygen diffuse into tunneling oxide and re-oxidize the surface of Si-substrate at RTO process. Here, the sample C and D all presented the same charge storage ability under *C-V* measurement.

Endurance characteristics of the sample C and D NVM structures are shown in Fig.6-5. Pulses conditions are set at $V_G - V_{FB}$= ± 10V for 10ms. From the data trend of sample C in Fig.6-5(a), it is found that the degeneration of the memory window is serious after 10^6 Program/Erase (P/E) cycles and keeps 67% compared with the initial memory window. However, the memory window of sample D can keep 86% after 10^6 Program/Erase (P/E) cycles test, as shown in Fig. 6-5(b). We consider that the endurance results are also to verify the evidence of re-oxidation of Si-substrate in RTO process for sample C.

Figure 6-6 shows charges (electron) remained rate of the sample C and D NVM structures. The charges (electron) remained rate of the sample D (52%) is better than sample C (32%). Here, we also analyzed the oxygen concentration of NCs of sample C and D whose ratios are 70% and 58% by ECSA results. Hence, it is considered that oxygen content of charge trapping center affects the trap level position in the NCs and we will discuss it by our building energy band diagram of Mn silicate NC [6.15, 6.16].

6.3.2 Energy band diagram and trapping level of Mn silicate ($MnSiO_x$) NCs

We are most concerned for the energy band diagram and trapping level position of Mn silicate ($MnSiO_x$). Hence, we used the intersection of two straight line which segments-one was fitted to the linear portion of the valence band (VB) leading edge and the other one was fitted to the background channels between the VB and the Fermi level by the Kraut's method for oxides and high k materials [6.17, 6.18]. Figure 6-7 shows the results that the valence-band spectrum of P-type Si (100), 5 nm SiO2/ P-type Si (100) and 5 nm $MnSiO_x$/ P-type Si (100) by XPS analysis. The valence band offset between $MnSiO_x$ and P-type Si (100) is estimated to be about 2.8 eV.

In the dielectric thin films, Plasmon and band to band transitions of XPS signals are appeared in the lower kinetic energy side of primary core-line peaks by the corresponding loss energy. The energy loss for the Plasmon excitation is generally much larger than the energy of excitation from the valence band maximum to the conduction band minimum. Therefore, the band gap values like the high-k dielectric can be determined from the threshold energy of the energy-loss spectrum for O1s and N 1s [6.19, 6.20]. The O 1s photoelectrons energy-loss spectra for 5 nm-thick thermal oxide and 5nm-thick $MnSiO_x$ is demonstrated in Fig. 6-8. The band-gap values of thermally grown SiO_2 and $MnSiO_x$ can be thereby determined to 8.9 eV and ~5.8 eV by using the Kraut's theory. The conduction band offset between the $MnSiO_x$ and Si

sub. is expressed as

$$\Delta E_C = E_g\,(MnSiO_x) - \Delta E_V - E_g\,(Si) \qquad (6\text{-}5)$$

where E_g (band gap of $MnSiO_x$), ΔE_V (valence band offset) and E_g (band gap of Si) are 5.8, 2.8 and 1.12 eV, respectively. Hence the conduction band offset between $MnSiO_x$ and Si is 1.9 eV, as shown in Fig. 6-8. The complete energy band diagram of $MnSiO_x$ NCs embedded in oxide NVM is presented in Fig. 6-9.

In addition, in order to extract the trap level of $MnSiO_x$ NCs, the trap-assisted tunneling model is used in this study [6.21, 6.22]. This simple model is taken into account the tunneling of electrons through traps located below the conduction band of the high permittivity gate dielectric layer. The expression of the gate current density (J_G) within this model is given by

$$J_G \propto N_t \exp[(qV_{OX} - \phi_1 + \phi_2 + \phi_t)/k_B T]. \qquad (6\text{-}6)$$

where N_t, V_{OX}, Φ_1, Φ_2 and Φ_t are trap density, oxide voltage, conduction band offset between Si sub. and oxide, conduction band offset between oxide and $MnSiO_x$, and trapping level. The gate current density J_G as a function of the voltage across the gate oxide V_{OX} for the SiO*x* /$MnSiO_x$ layer is shown in Fig. 6-10 from room temperature up to 150 °C. Figure 6-10 can transfer to Fig.6-11 which shows the current density as a function of the inverse of temperature on dot plots for a fixed gate oxide voltage of 3.1 V. The solid lines of Figs. 6-11(a) and (b) are fitted to the data using Eq. (6-6). One observes that J_G is exponentially dependent on $1/T$ and thus the experimental data are good agreement with this model. The trap levels of sample C and D are found to be about 1.26 and 1.83 eV below the conduction band of $MnSiO_x$. Here, we also used this model to extract the trap density of $MnSiO_x$ and the trap density of sample C and D were about the same, 5.4 and 6.6 $x10^{17}$ cm^{-3}. Therefore, the charge storage abilities of sample C and D were also the same.

Moreover, according to the results of trapping level of sample C and D, we can re-describe the trapping level position in our proposed energy band diagram of Fig. 6-9 and Fig. 6-12 shows the trapping levels below the conduction band of $MnSiO_x$ NCs by the sample C (blue line) and sample D (red line). This band diagram can also use to explain the retention characteristics of Fig. 6-6 and hence the escaping paths of stored charges is dominated the retention time of sample C and D, as show in Figs. 6-12(a) and (b).

Table 1 is comparisons of oxygen concentration with trapping level for the sample C and sample D by ESCA analysis. We found that the trapping level was depended on the oxygen concentration of $MnSiO_x$ due to the number of dangling band and the sample D had deeper trapping level than sample C.

6.3.3 Electrical characteristics of double layer $MnSiO_x$ NCs NVM

In the previous studies of double layer metallic NCs NVMs, they have a serious drawback for retention test which the interlayer, isolated dielectric, between two metallic NCs layers is not enough thick and that will lose to block the lateral electron migration effect, as shown in Fig. 6-13(a). Hence, we proposed a double layer $MnSiO_x$ NCs NVM to solve the above-mentioned problem. By our proposed double $MnSiO_x$ NCs structure of Fig. 6-13(b), the discrete traps in dielectric NCs can restrain lateral electron migration effect because the stored charges must overcome the barrier height of trapping level to transport in the charge trapping layer.

Figure 6-14 exhibits schematic sketch of double layer $MnSiO_x$ NCs structure procedures. The fabrication of NVM structure was started with a thermal dry oxidation at 950°C to form a tunnel oxide about 5 nm on *p*-type (100) Si wafer which had been removed native oxide and micro-particles by RCA process, and then a 1-nm-thick a-Si and 9-nm-thick $Mn_{0.2}Si_{0.8}$ served as a charge tapping layer was deposited by reactive sputtering in the Ar/ O_2 [24/ 1 SCCM (SCCM denotes cubic

centimeter per minute at STP)] ambiance at room temperature. Before the rapid thermal annealing (RTA) process at 800 °C for 30 s in the N_2 ambiance, the $Mn_{0.2}Si_{0.8}$ layer was capped by a 10-nm-thick oxide using PECVD system at 300°C. The RTN process was performed to cause the self-assembly double layer of $MnSiO_x$ NCs in the charge trapping layer. After RTN process, a 20-nm-thick blocking oxide was deposited by PECVD and then deposited Al gate electrodes to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. Here, we used the sample D fabrication condition to form the double layer NCs NVMs because of its deep trapping level. Electrical characteristics of the capacitance-voltage (*C-V*) hysteresis were also measured by HP4284 precision *LCR* meter with high frequency of 1 MHz.

The cross-sectional TEM image of MOIOS structure containing spherical and separated NCs is shown in Fig. 6-15. There is an obvious double layer of $MnSiO_x$ NCs because Mn atoms diffuse into pre-cap control oxide during RTA process. From TEM analysis, the average diameter of the NCs is approximately 6 nm. Figure 6-16 shows capacitance-voltage (*C-V)* hysteresis of single and double layers NCs memories. The memory windows of two samples are nearly equal to 1 V under V_G-V_{FB} = ± 5 V gate voltage operation. However, under V_G-V_{FB} = ±10 V gate voltage operation, the memory windows of double and single layers NCs memories are 4.5V and 2.5V respectively, as shown in Figs. 6-16(a) and (b). Fig. 6-17 shows the memory windows of single and double layers $MnSiO_x$ NCs NVMs under gate voltage sweep. From Fig. 6-17, it is found that the memory windows of single and double layers $MnSiO_x$ NCs are the same before V_G-$V_{FB} \leqq 4$ V while the double layer $MnSiO_x$ NCs has better charge storage ability than single layer NCs after V_G-$V_{FB} \geqq 4$ V. This result can be explained that the electrons are injected into the first layer NCs under a small gate voltage operation (V_G-$V_{FB} \leqq 4$ V, as show in Fig. 6-18(a)) and are injected into the second layer NCs under a high gate voltage operation (V_G-$V_{FB} \geqq 4$ V, as show in

Fig. 6-18(b)).

Figure 6-19 presents the retention characteristic of double and single layers NCs NVMs for electron storage ability. We fixed the initial flat band voltage shift, 2 V, for two kinds of NCs NVMs under 10 V stress. The charges (electron) remained rate of the double layer (64%, 1.28 V) is better than sample C (52%, 1.06 V). Simple energy band diagrams of single and double layers NCs NVMs are shown in Fig.6-20(a) and (b). According these band diagrams, if the electron is stored in the traps of the secondary NCs, it is more difficult than single layer NCs to leaks into the Si-sub. Hence, before the retention time 300s, the retention behavior of double layer is similar to single layer due to the charge loss of first NCs. We successfully fabricated the double layer $MnSiO_x$ NCs embedded in oxide for the next-generation NVM application.

6.4 Conclusion

The nonvolatile memory structure of $MnSiO_x$ NCs embedded in the SiO_x layer was fabricated by sputtering ($Mn_{0.2}Si_{0.8}$/a-Si) in an Ar/O_2 environment at room temperature. The $MnSiO_x$ NCs can be explained that the MnO react with SiO_x during RTA process. The NCs can be simple and uniform to fabricate in this study. The memory window of $MnSiO_x$ NCs enough to define “1” and “0” states is clearly observed for the NVM application. The retention and endurance characteristic are enough to be maintained after 10 ys and 10^6 P/E cycles.

XPS were adopted to identify the $MnSiO_x$ NCs. The band gap of $MnSiO_x$, VBO and CBO between the $MnSiO_x$ films and Si substrates are obtained by XPS measurements, and the values of VBO and CBO to Si are found to be about 2.8 and 1.9 eV, respectively. The analysis of the temperature dependence of the current density in $MnSiO_x$ gate stacks is allowed to estimate the energy levels responsible for

the leakage current in these layers. The estimation of these energy levels requires the knowledge of the band offsets between the different layers. In this study, the trap levels depended on the oxygen concentration of sample C and sample D are about 1.26 and 1.83 eV below the conduction band of $MnSiO_x$ by using the trap assisted tunneling model.

Double layer $MnSiO_x$ NCs memory was easily fabricated. It exhibits superior memory characteristics for the application of low-power nano-scale nonvolatile memory. The nanocrystal can be simple and uniform to fabricate in this study. The memory window of $MnSiO_x$ NCs enough to define "1" and "0" states is clearly observed for the nonvolatile memory application. The retention characteristic of Double layer $MnSiO_x$ NCs memory is better than single layer NCs NVMs to be maintained after 10 ys due to the charge storage mode under retention state.

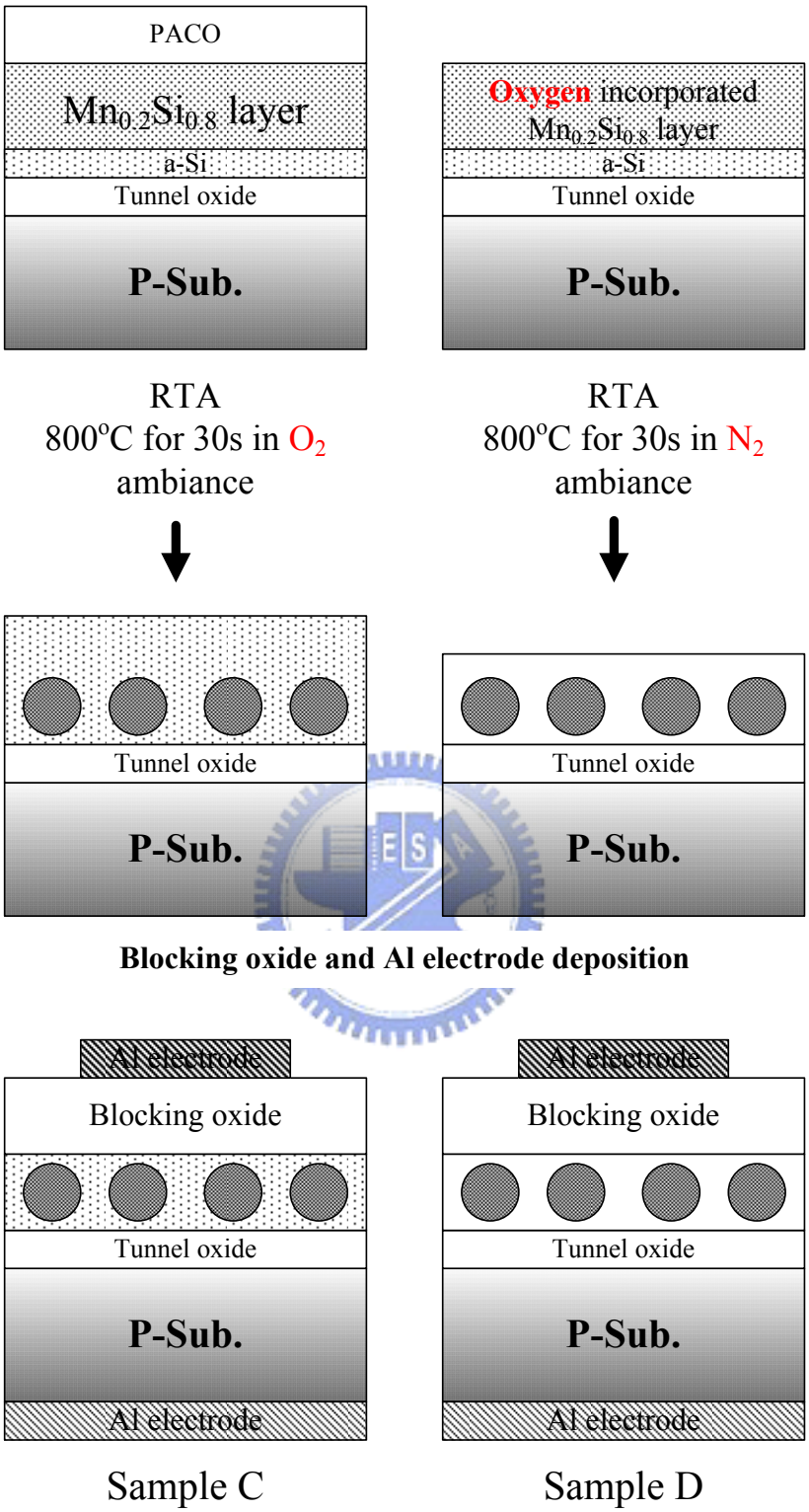


Figure 6-1 Schematic sketches of experimental procedures for manganese silicate nanocrystals embedded in oxide layer nonvolatile memories. Sample C is used the RTA process in O_2 ambiance. Sample D is used the oxygen incorporated $Mn_{0.2}Si_{0.8}$ layer as charge trapping layer.

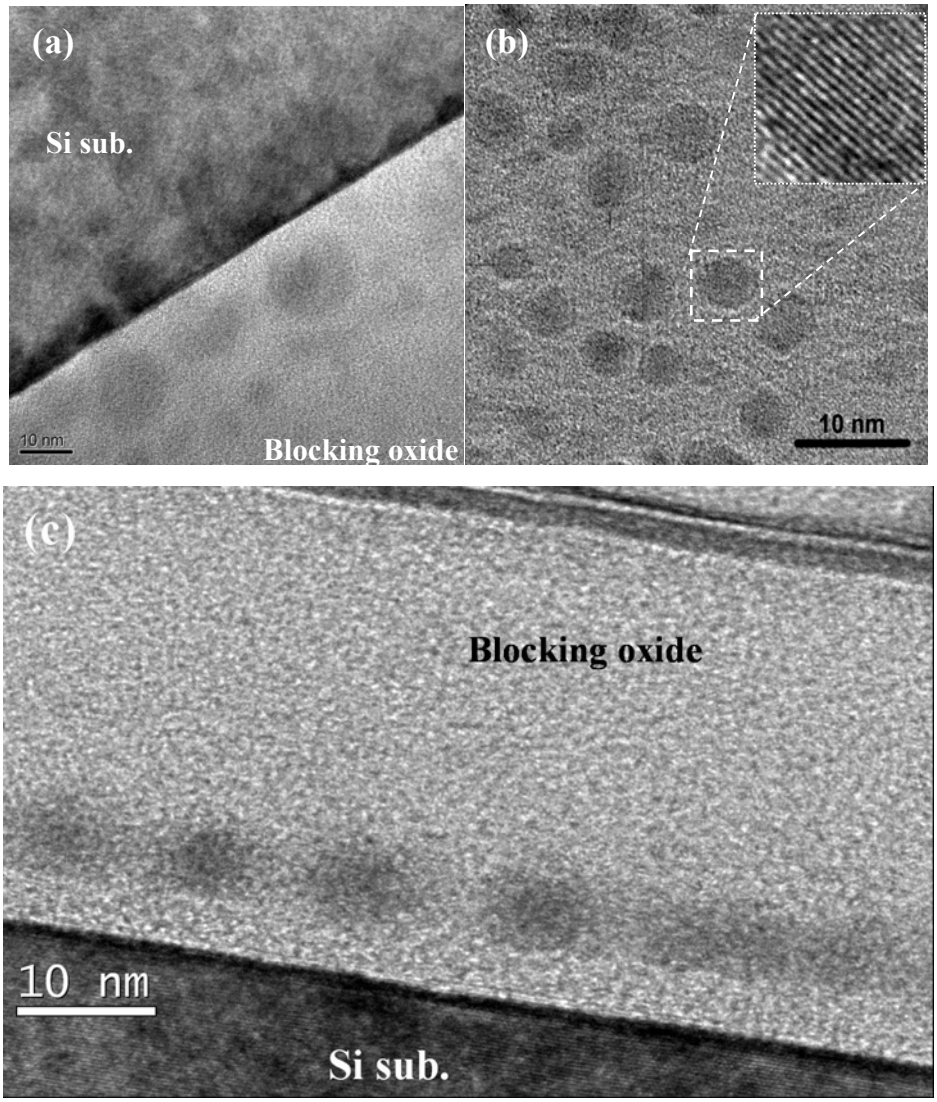


Figure 6-2 Cross-section (a) and plane view (b) TEM images of sample C. (c) Cross-section TEM image of sample D.

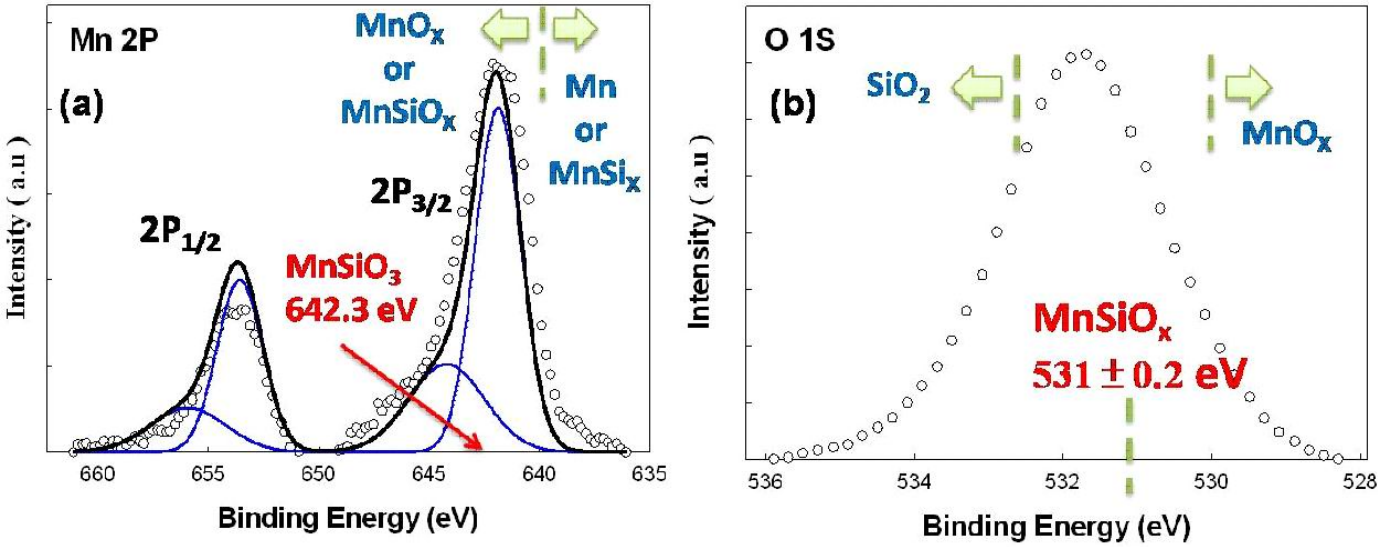
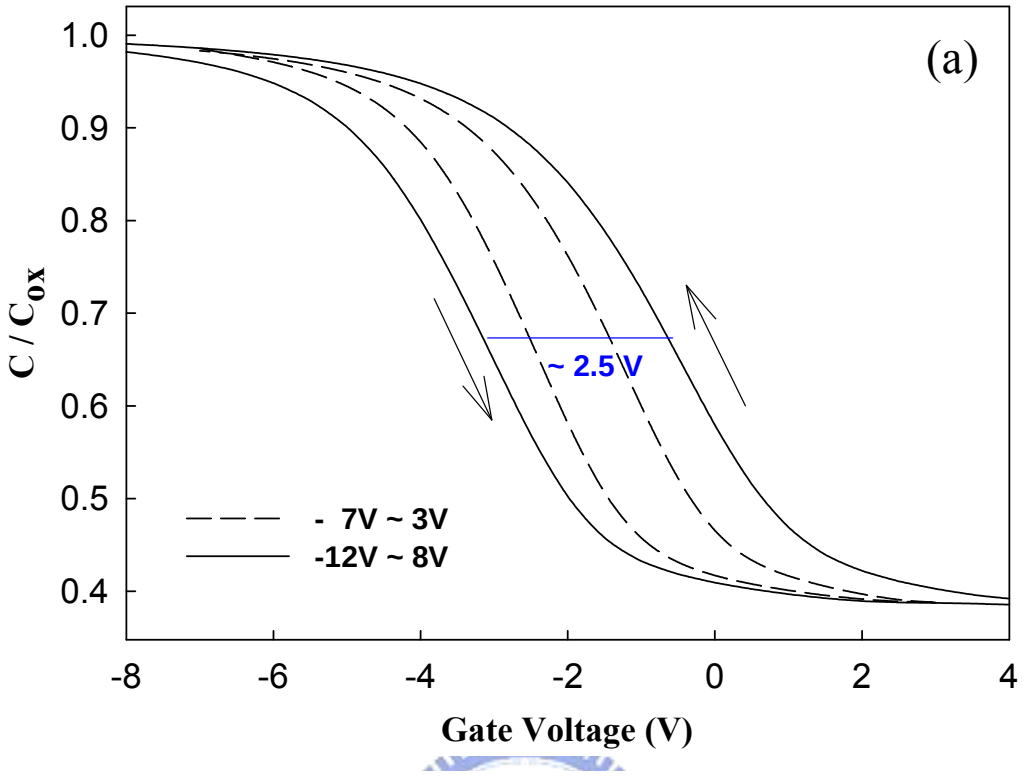


Figure 6-3 (a) Mn 2*p* and (b) O 1*s* XPS analysis of the charge trapping layer. Empty circles and straight line indicate experimental and fitting results, respectively.



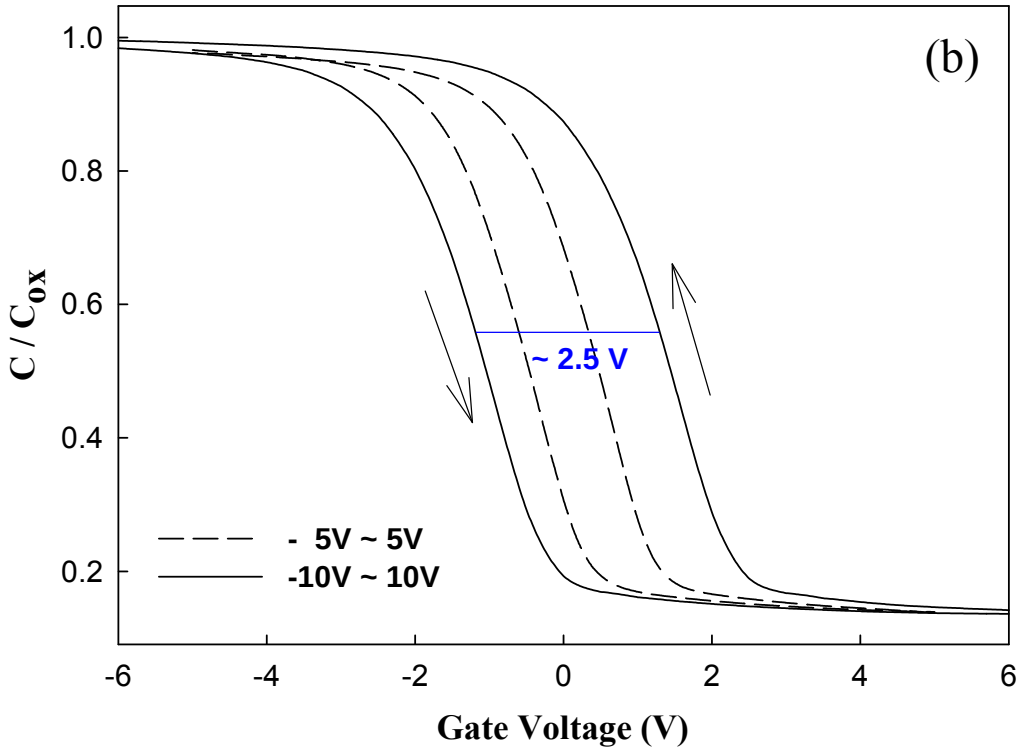
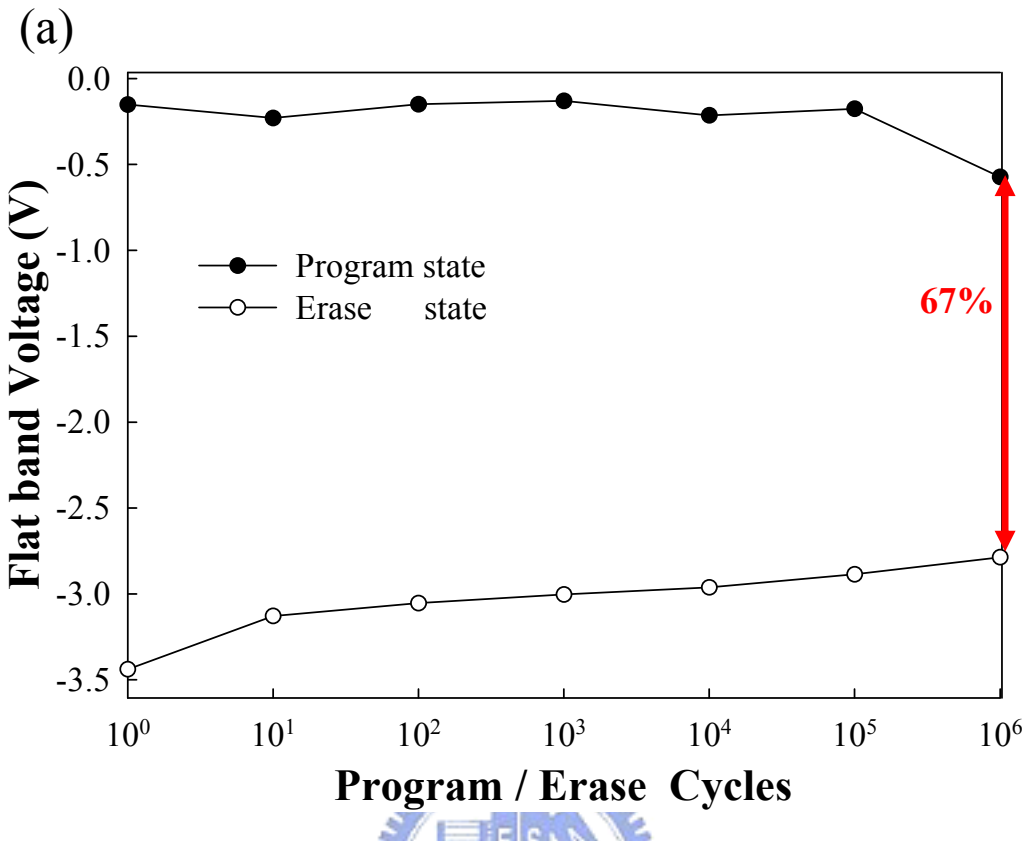


Figure 6-4 *C-V* hysteresis of MOIOS structures by (a) sample C, and (b) sample D. The memory windows of two samples are nearly equal to 1 and 2.5 V under ±5 dash line and ±10 V solid line gate voltage operation, respectively.



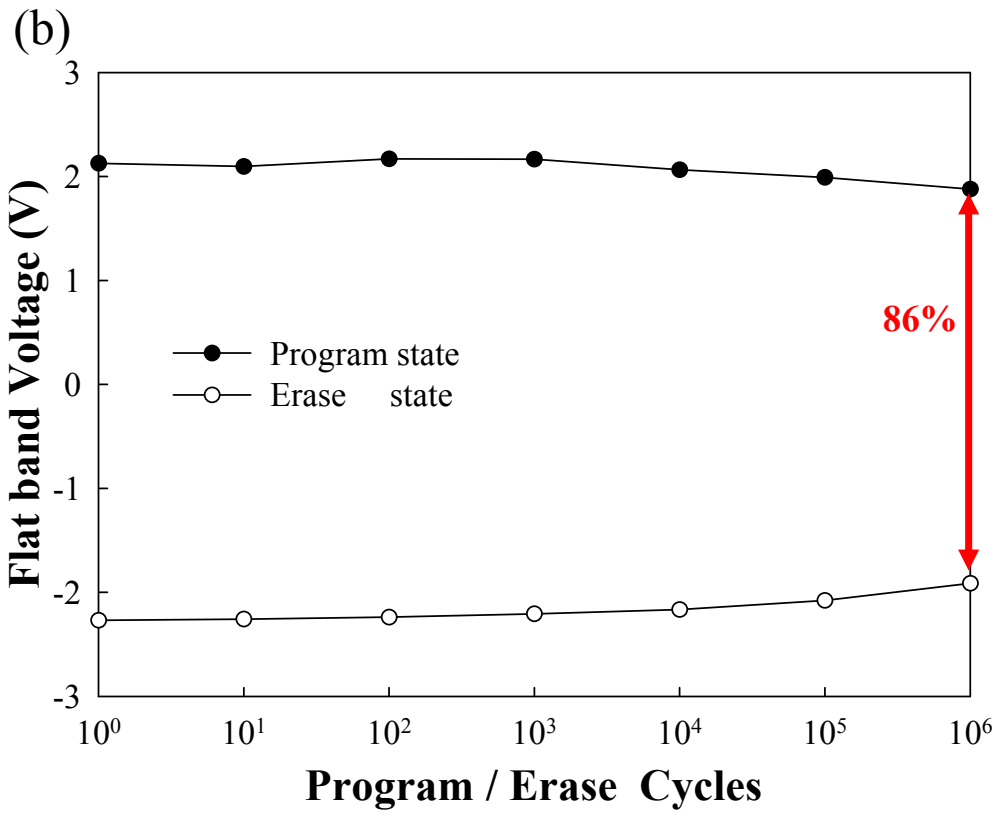


Figure 6-5 Endurance characteristics of the NCs memory structures by the (a) sample C and (b) sample D. Pulses condition of $V_G - V_{FB} = \pm 10V$ for 10 ms.

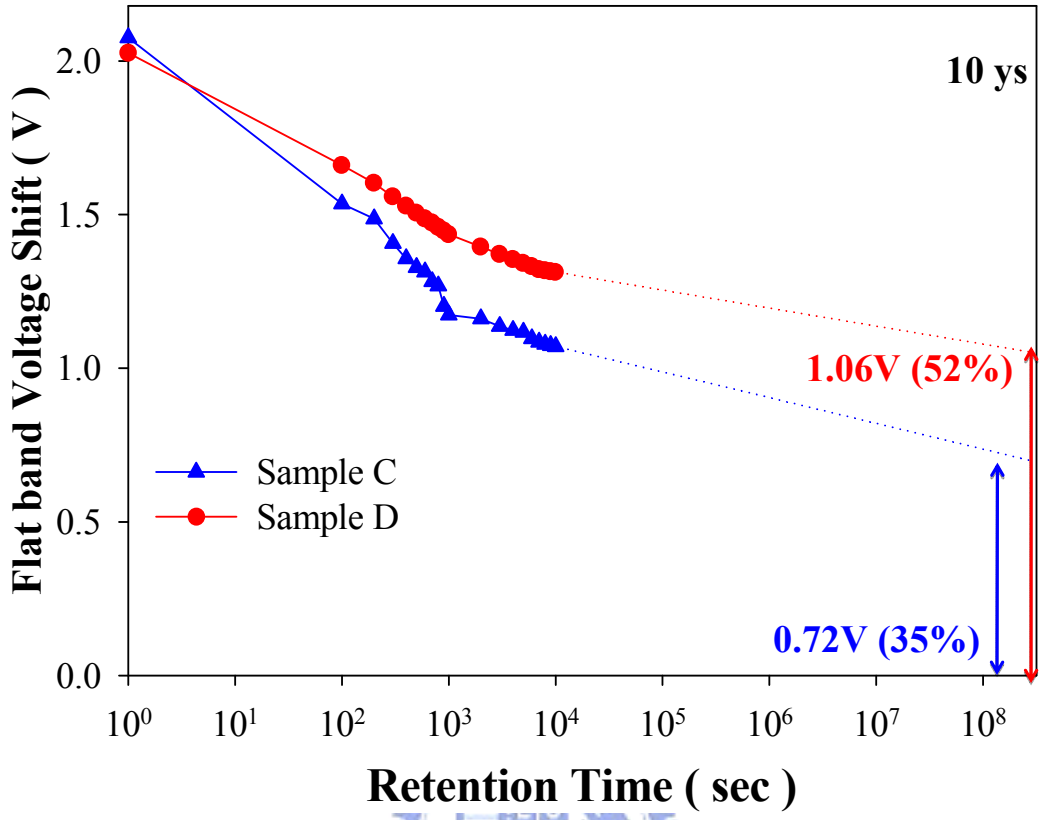


Figure 6-6 Retention characteristics of the NCs nonvolatile memory structures by the sample C and sample D. Charge holding rates of sample C and sample D are about 35% and 52% after 10 ys.

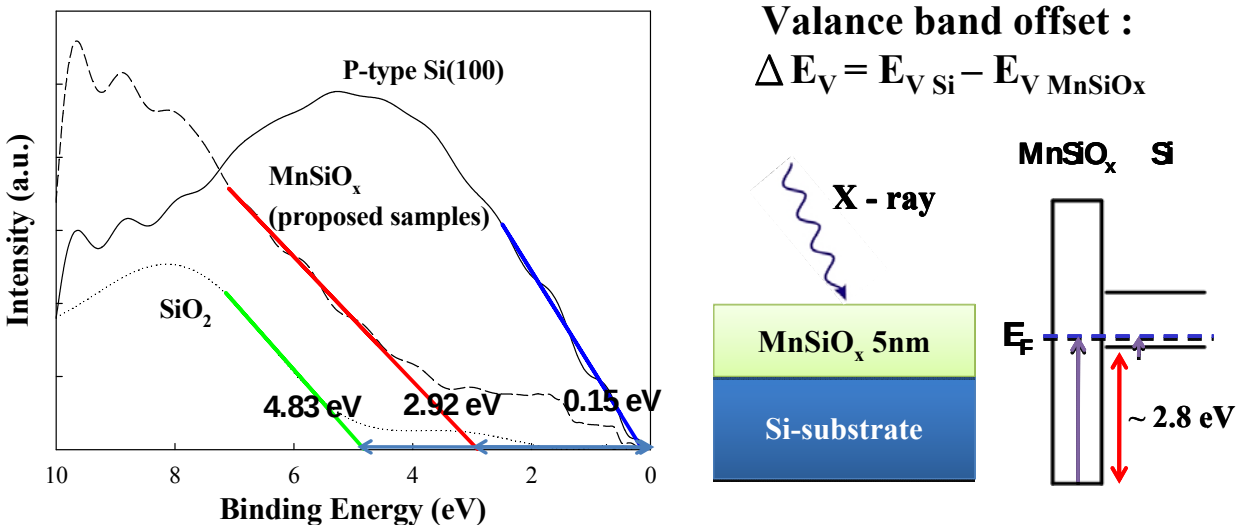


Figure 6-7 Valence band spectrum for Si-sub, 5 nm thick SiO_2/Si (100) and 5 nm thick $MnSiO_x$/Si (100) by using the XPS analyses. The valance band offset ($\triangle E_V$) of $MnSiO_x$ for our proposed sample is about 2.8 eV.

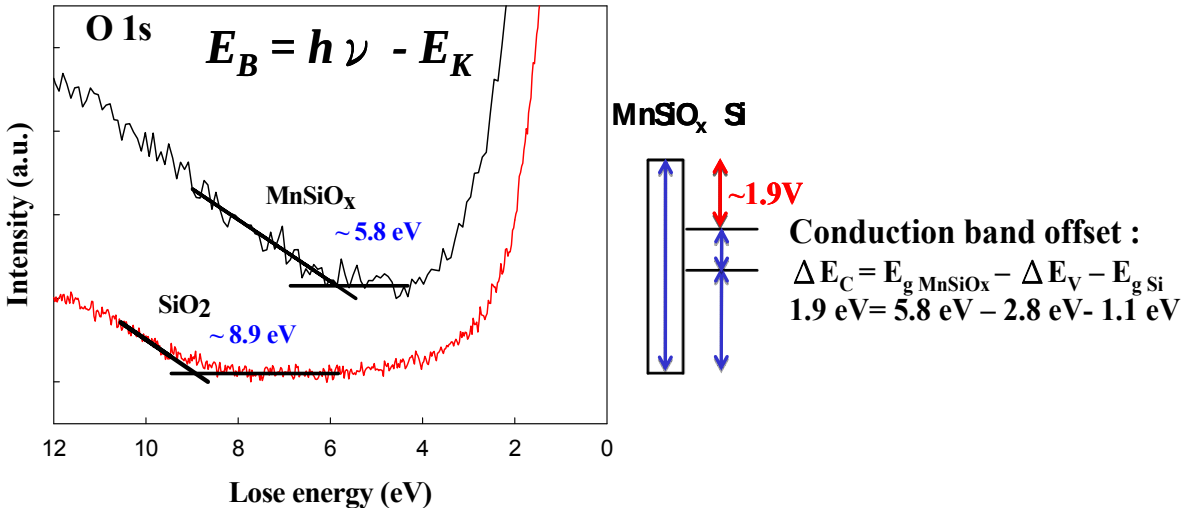


Figure 6-8 O1s energy-loss spectra for 5 nm thick thermal oxide and 5nm thick $MnSiO_x$ by using the XPS analyses. The band gap (E_g) of manganese silicate is about 5.8 eV.

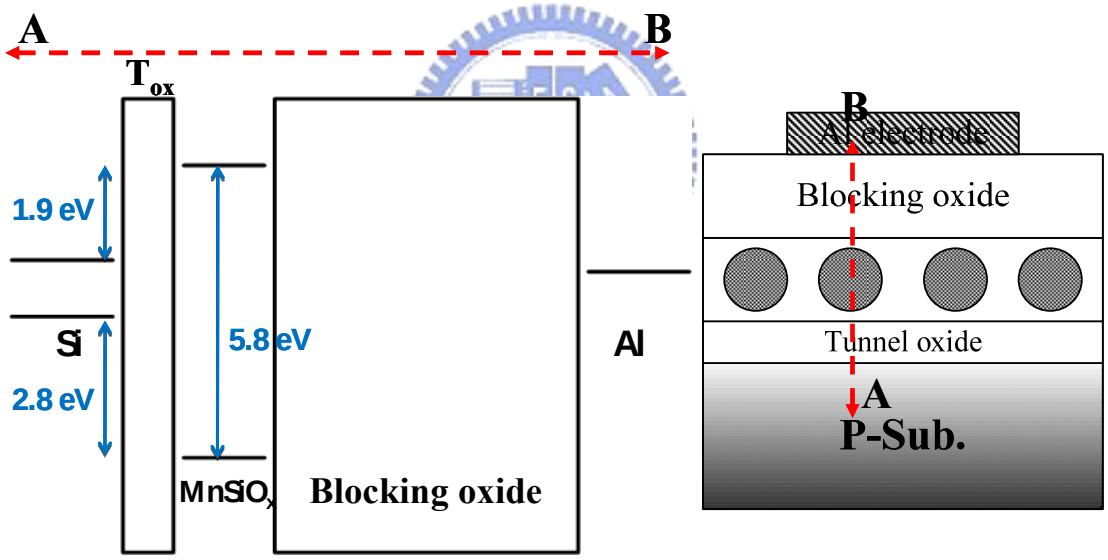


Figure 6-9 Energy band diagram of MOIOS memory cell with $MnSiO_x$ nanocrystals as charge trapping center.

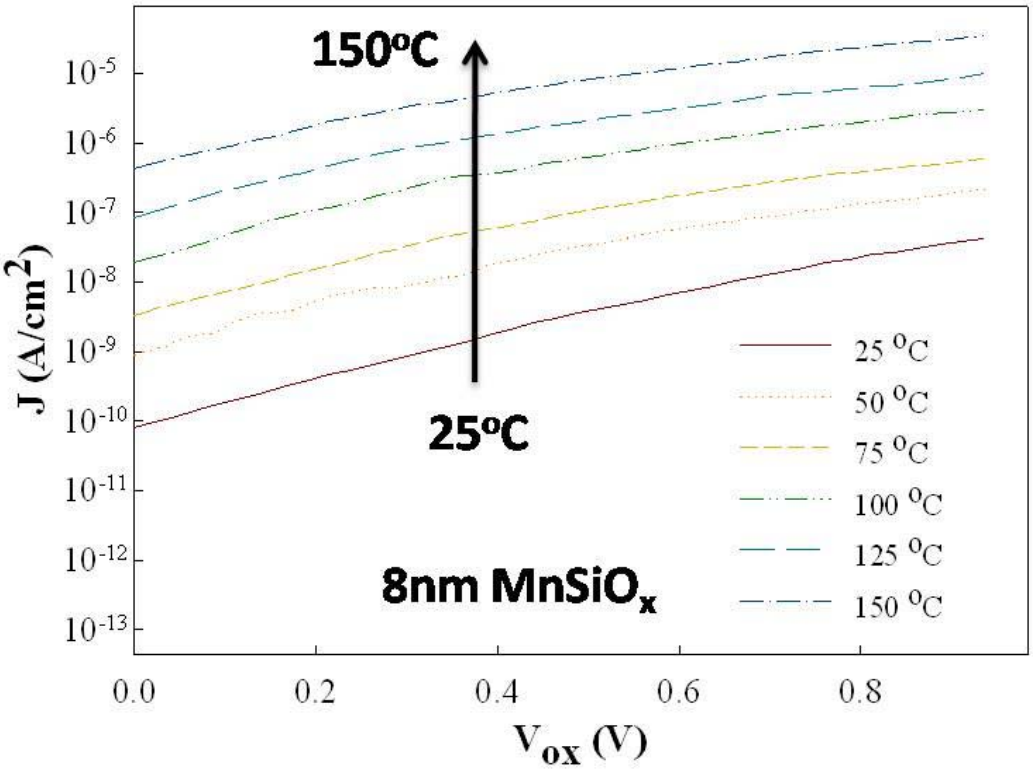


Figure 6-10 Current–density J (A/cm^2) as a function of the V_{OX} of a MOS capacitor with a $MnSiO_x$ stack dielectric layer (8 nm $MnSiO_x$) recorded from 25 to 150 °C.

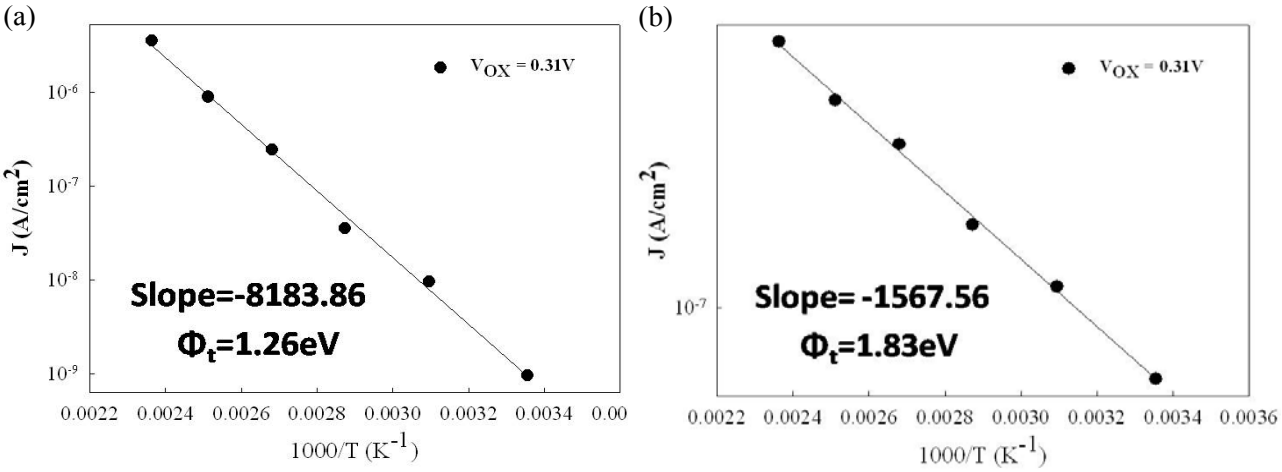


Figure 6-11 Current–density J (A/cm^2) of (a) sample C and (b) sample D as a function of the inverse temperature for $MnSiO_x$ gate dielectric stacks. The solid lines are fitted to the data by using Eq. (6-6). The Φ_t of (a) sample C and (b) sample D are about 1.26 and 1.83 eV.

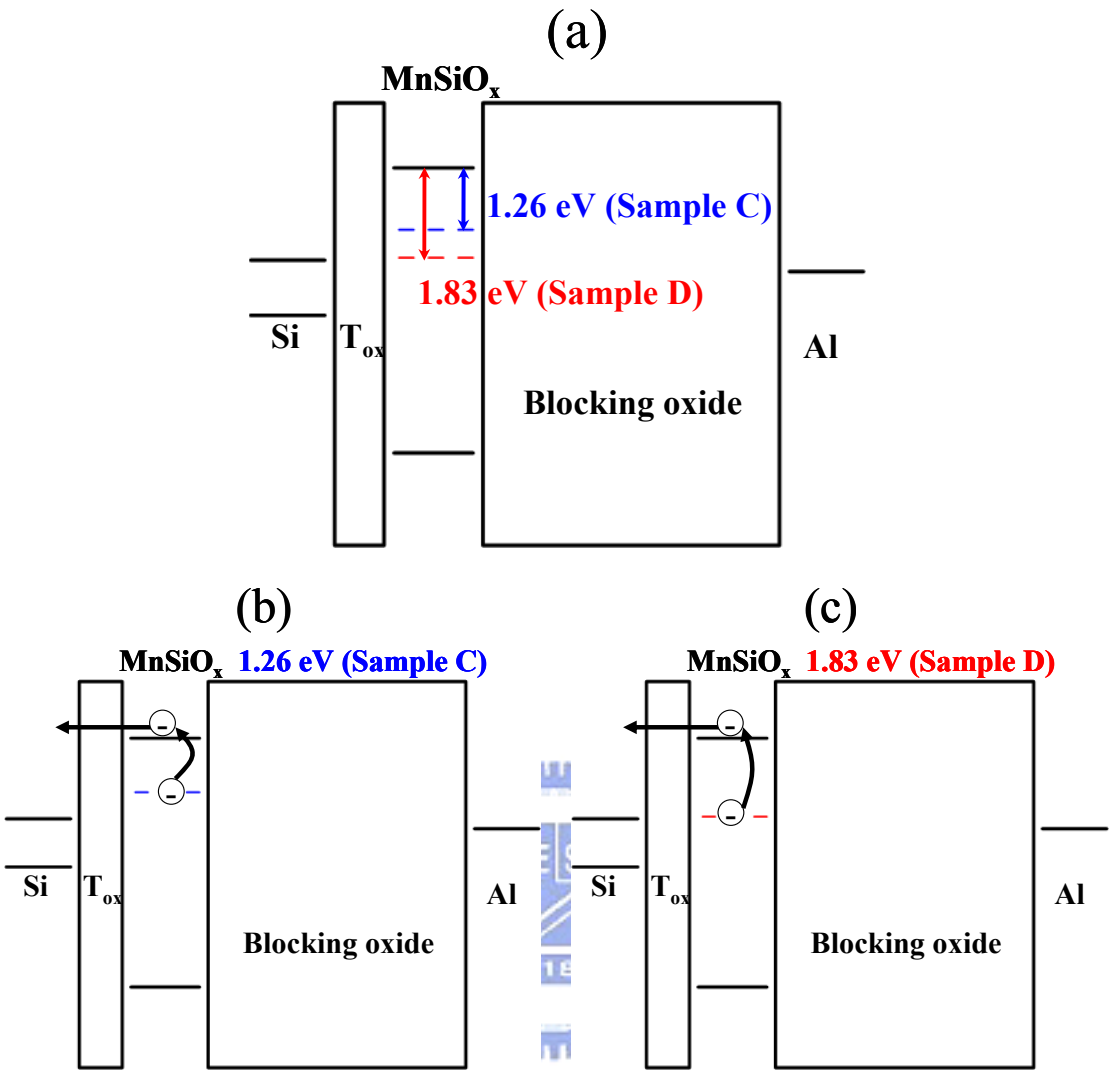


Figure 6-12 (a) Trapping levels below the conduction band of $MnSiO_x$ NCs by the sample C (blue line) and sample D (red line). Escaping paths of stored charges for the (b) sample C and (c) sample D are form the trapping level of NCs to the Si sub. under retention state.

Table 6-1 Comparisons of oxygen concentration for the sample C and sample D by ESCA analysis.

NVM structures	Oxygen concentration (%)	Trapping Level (eV)	Memory window under ± 10 V	Trap density (cm^{-3})
Sample C	70	1.26	2.5 V	5.4×10^{17}
Sample D	58	1.83	2.5 V	6.6×10^{17}

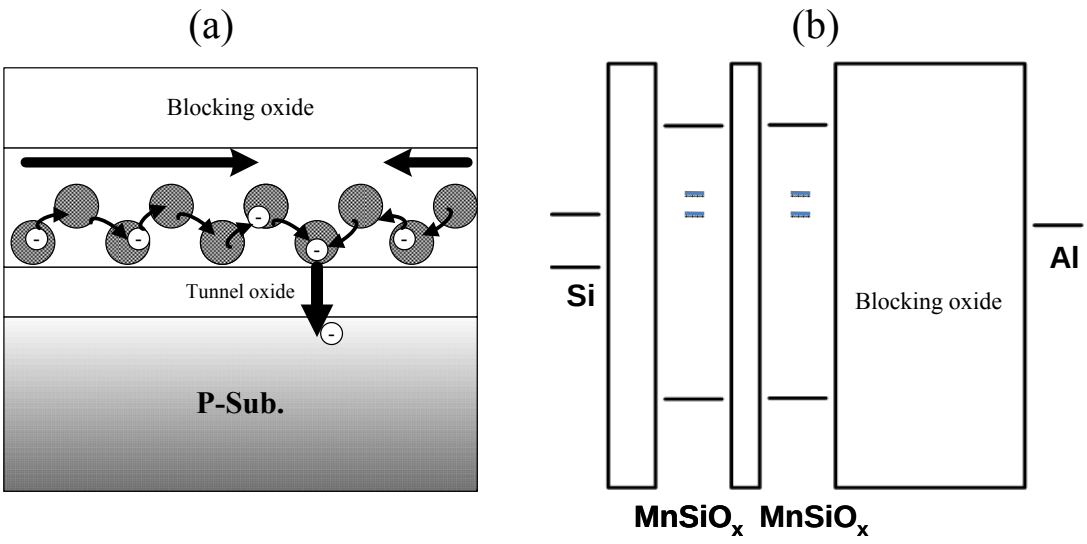


Figure 6-13 (a) Lateral leakage current phenomenon of non-ideal double metal NCs structure. (b) Our proposed double layer $MnSiO_x$ NCs structure.

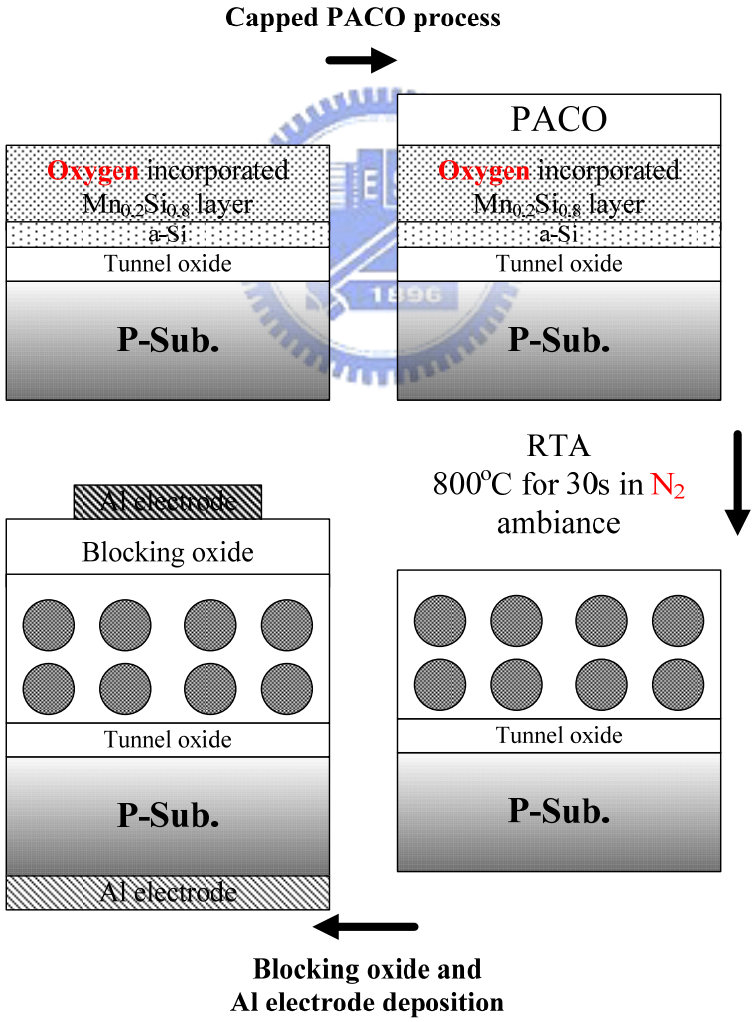


Figure 6-14 Formation flow of our proposed double layer $MnSiO_x$ NCs structure by using the self-assembled mechanism of $MnSiO_x$ NCs.

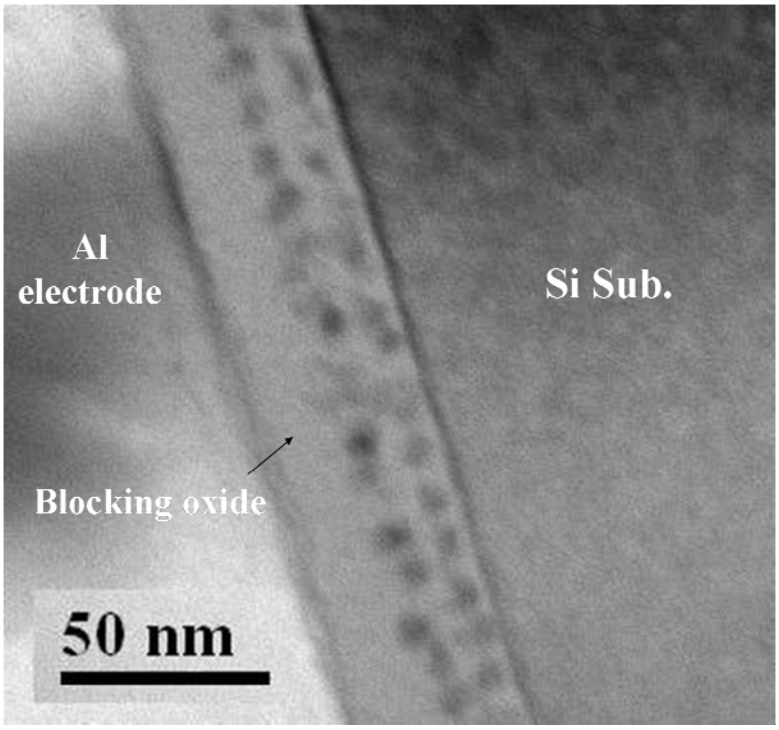


Figure 6-15 Cross-section TEM image of our proposed double $MnSiO_x$ NCs nonvolatile memory structure.

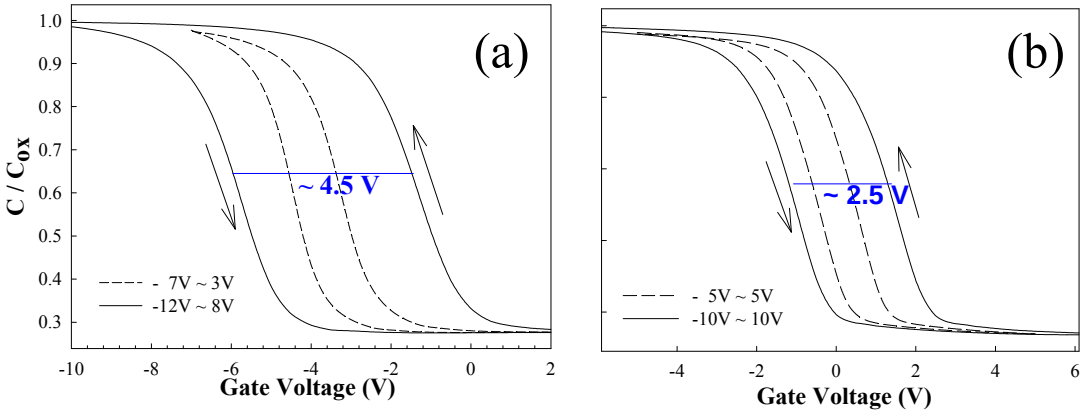


Figure 6-16 *C-V* hystereses of MOIOS structures by the (a) double layer NCs and (b) single layer NCs. The memory windows are 4.5 and 2.5 V for the (a) double layer NCs and (b) single layer NCs under V_G-V_{FB}= ± 10 V solid line gate voltage operation, respectively.

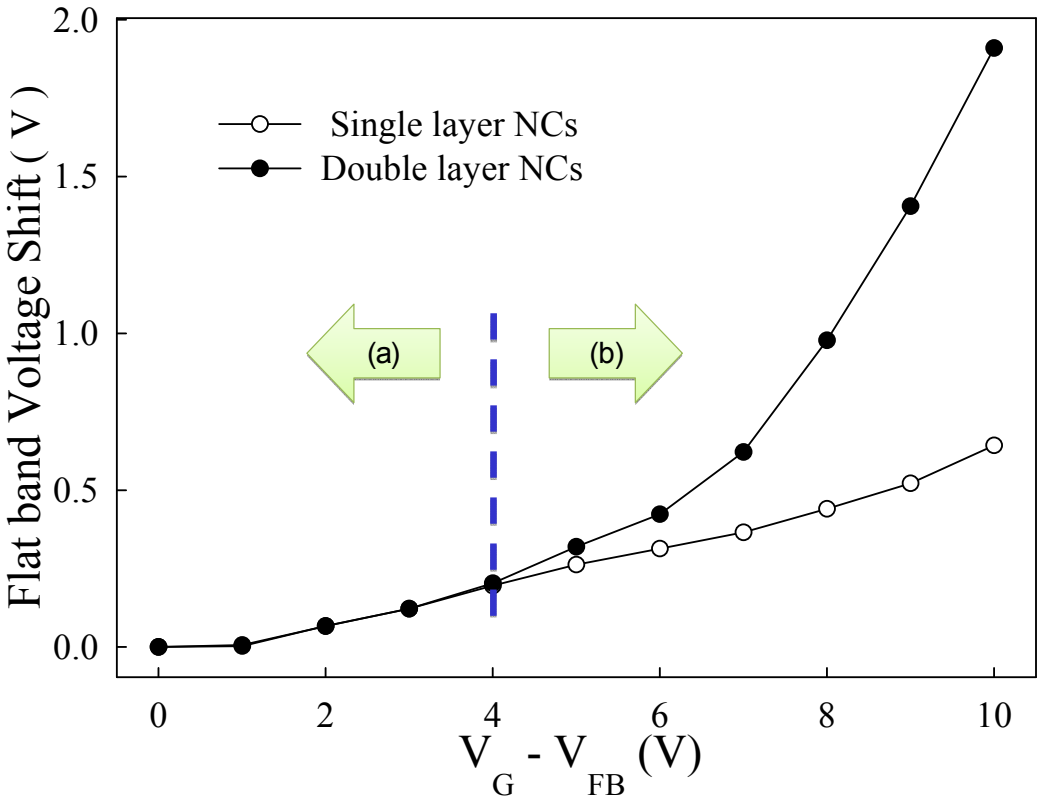


Figure 6-17 Flat band voltage shift characteristics of the double layer $MnSiO_x$ nanocrystals NVM as compared with single-layer $MnSiO_x$ nanocrystals NVM for the electron injection. The Flat band voltage shift is measured by C-V curve.

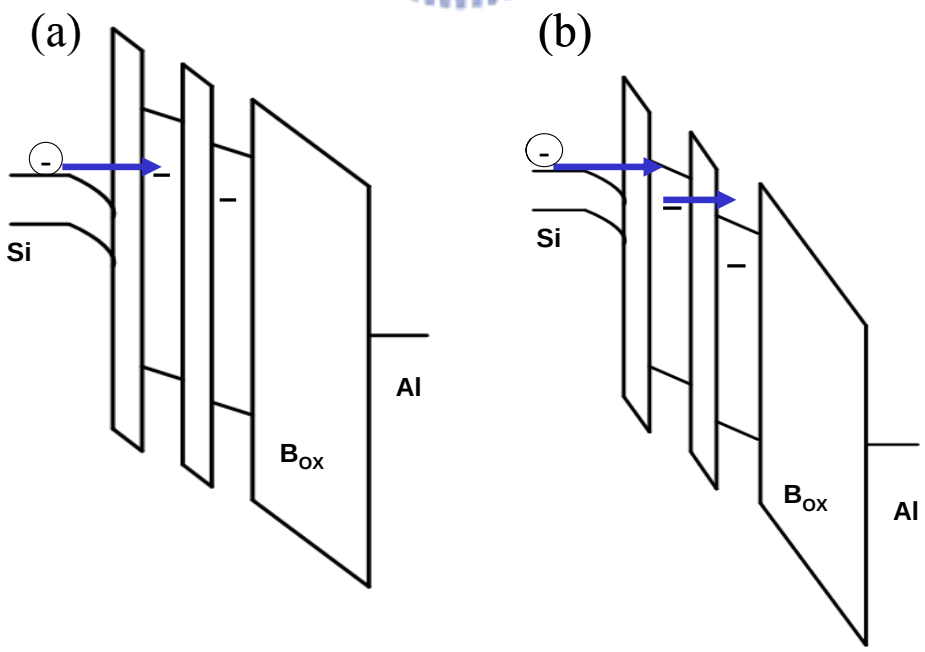


Figure 6-18 Energy band diagrams of electrons injection under (a) small gate voltage (V_G-V_{FB}≦4 V) and (b) high gate voltage (V_G-V_{FB}≧4 V) operations.

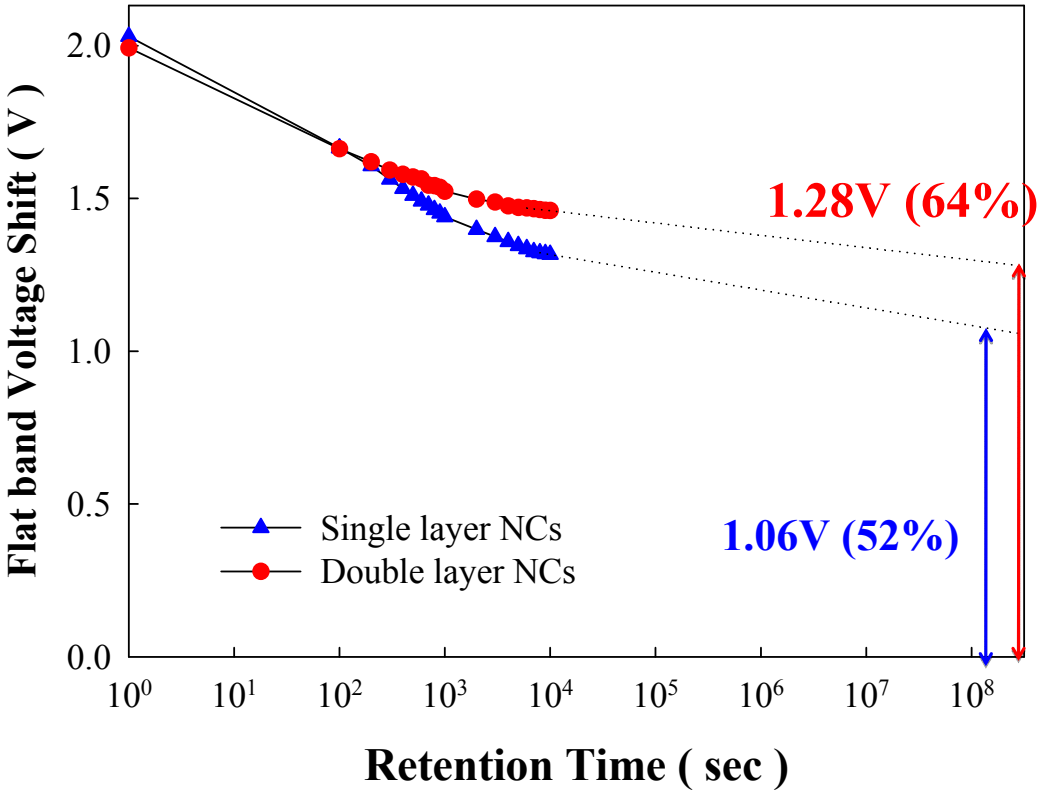


Figure 6-19 Retention characteristics of the double layer $MnSiO_x$ nanocrystals NVM as compared with single layer $MnSiO_x$ nanocrystals NVM. Charge holding rates of double layer and single layer $MnSiO_x$ nanocrystals NVMs are about 64% and 52% after 10 ys.

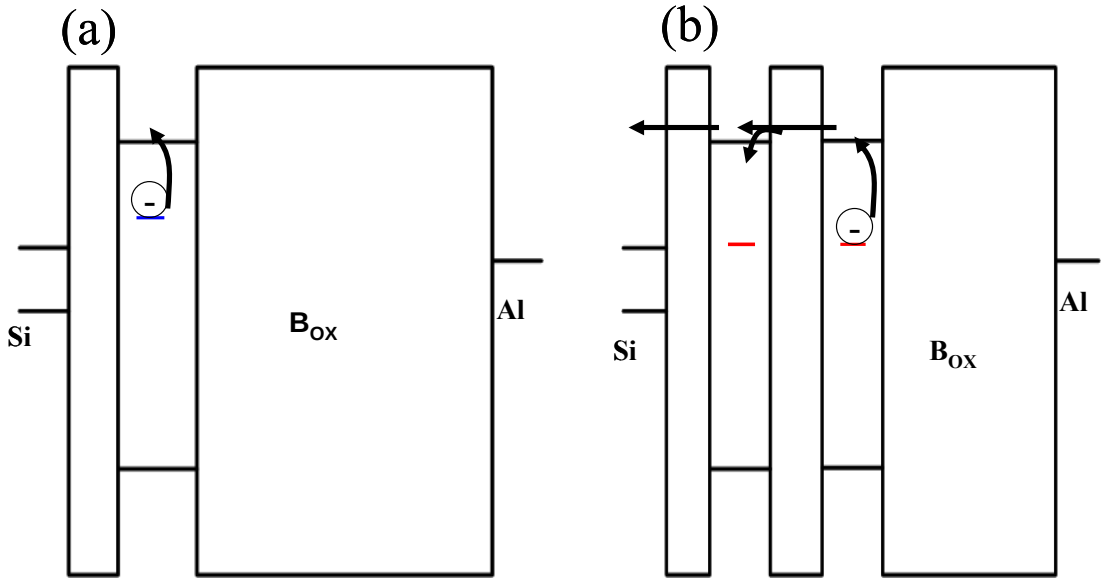


Figure 6-20 Energy band diagrams of electrons escaping paths of (a) double layer and (b) single layer $MnSiO_x$ nanocrystals NVMs under retention state.

Chapter 7

Conclusion

We successfully fabricated the Ge nanocrystals embedded in the dielectric by using the internal competition reaction characteristics of $Si_{1.33}Ge_{0.67}O_2$ and $Si_{2.67}Ge_{1.33}N_2$ in this study and also cut down thermal budget by using RTA system. The over-oxidation phenomenon of Ge nanocrystals for conventional Ge nanocrystals fabrication could be prevented through different Gibbs free energies of compounds. The Ge nanocrystals combined with SiN_x matrix shown better charge storage ability than Ge nanocrystals embedded in oxide because of the extra traps of SiN_x surrounding with nanocrystal. Moreover, due to the Coulomb blockade effect, the Ge nanocrystals embedded in nitride can keep long-term stored charges in the charge trapping layer. In addition, we also obtained the good endurance test for our proposed samples on the nonvolatile memory application.

In this thesis, novel and ease fabrication techniques of Ni-O-Si and Ni-Si-N nanocrystals were demonstrated for the application of nonvolatile memory. The nonvolatile memory structure of Ni-O-Si nanocrystals embedded in the SiO_x layer was fabricated by sputtering a commixed target ($Ni_{0.3}Si_{0.7}$) in an Ar/O_2 environment at room temperature. For the formation of nanocrystal, the oxygen plays a critical role during sputter process. The high density (~10^{12} cm^{-2}) nanocrystal can be simple and uniform to be fabricated. Another similar process for Ni-Si-N nanocrystals is also proposed by sputtering a co-mix target ($Ni_{0.3}Si_{0.7}$) in the argon (Ar) and nitrogen (N_2) mix-gas environment at room temperature. This similar fabrication was also found that high density Ni-Si-N nanocrystals embedded in the silicon nitride (SiN_x). Due to low temperature process, this technique of metal nanocrystals for the application of nonvolatile nanocrystal memory can be satisfied with requirement of low temperature

substrate and to reduce the use of Si wafer.

Furthermore, a RTA process with low temperature (500°C~600°C) and short duration (100sec) is used to improve the crystalline quality of NiSi nanocrystals and memory characteristic. During the RTA process, the metallic Ni-Silicide (NiSi) nanocrystals precipitate and show good crystalline quality by XRD analysis. The NiSi nanocrystal with good crystalline quality has higher density of states to store charge and cause larger memory window. The reliability issues, such as retention and endurance, are significantly improved after the RTA process. According the results of J-V characteristic and XPS analysis, thermal treatment (RTA) can reduce the defects (leakage path) in the SiN_x which surrounds the nanocrystals. It decreases the probability of charge escaping from the nanocrystal. The quality of dielectric is also strengthened to bear the P/E cycling stress.

The charge storage layer of nanocrystals embedded in SiN_x shows larger memory window and better reliability over nanocrystals embedded in SiO_x. The improvement of charge storage capacity is attributed to additional accessible charge trap states in the SiN_x matrix. For retention property, the stored charge can be shared among the nitride traps; the enhanced field by stored charge (Coulomb blockade) through the tunneling oxide can be reduced. This result decreases the probability of charge escaping from the nanocrystal. Moreover, charges are likely to be relaxed to the nitride traps. Leakage through the intermediate medium can also be inefficient due to Coulomb Blockade. Therefore, nanocrystals embedded in SiN_x show enhanced retention characteristics. In addition, because of high permittivity (ε) of nitride, the charges transportation is more uniform on the channel surface due to the electric field distribution by ISE TCAD simulation results. Combining NiSi nanocrystals and SiN_x as charge trapping layer can improve the endurance characteristic for P/E cycling operation.

Multi-layer NiSi nanocrystals memory was obtained layer by layer using the sputtering deposition followed by low temperature RTA process. We have demonstrated multi-layer metal nanocrystals memory has charge storage and retention improvement over single-layer metal nanocrystals. The increased number density of nanocrystals can enlarge the memory windows. The leakage of stored charges in the upper-layer nanocrystals can be suppressed by Coulomb blockade and ground state quantization from the lower-layer (small size) nanocrystals. In addition, we can get a 5 V memory window under a small ± 5V operation and the superior endurance characteristic are obtained after one million Program/Erase cycles.

In the finial chapter, the dielectric manganese silicate ($MnSiO_x$) nanocrystals nonvolatile memory structure was proposed and fabricated by sputtering ($Mn_{0.2}Si_{0.8}$/a-Si) in an Ar/O_2 environment in this study. The $MnSiO_x$ nanocrystals can be explained that the MnO react with SiO_x during RTA process. The memory window of $MnSiO_x$ NCs enough to define “1” and “0” states is clearly observed for the NVM application. In addition, the band gap of $MnSiO_x$, valence band offset and conduction band offset between the $MnSiO_x$ films and Si substrates are obtained by XPS measurements, and the values of VBO and CBO to Si are found to be about 2.8 and 1.9 eV, respectively. Moreover, the trap levels depended on the oxygen concentration of our proposed $MnSiO_x$ nanocrystals nonvolatile memory structures are about 1.26 and 1.83 eV below the conduction band of $MnSiO_x$ by using the trap assisted tunneling model. Double layer $MnSiO_x$ nanocrystals memory was also easily fabricated. It exhibits superior memory characteristics for the application of low-power nano-scale nonvolatile memory. The nanocrystal can be uniform to distribute among the charge trapping layer. The retention characteristic of double layer $MnSiO_x$ nanocrystals memory is better than single layer nanocrystals to be maintained after 10 ys due to the charge storage mode under retention state.

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Chapter 1

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Chapter 5

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Vita　　簡　　歷

姓名： 陳緯仁 (Wei-Ren Chen)

出生日期：民國 71 年 02 月 14 日 (1982/02/14)

住址：900 屏東市自立南路 157 巷 6 號

學歷：

國立中山大學 物理學系 學士

(2000.09-2004.06)

國立交通大學 電子工程研究所 碩士班

國立交通大學 電子工程研究所 博士班

(2004.09-2008.10)

論文題目：

前瞻非揮發性奈米點記憶體元件之製作與特性研究

Fabrication and Electrical Characterization of Advanced Nanocrystals Nonvolatile Memories

Publication List（著作目錄）

International Journals:

[1]. C. H. Tu, T. C. Chang, P. T. Liu, H. W. Zan, Y. H. Tai, C. Y. Yang, Y. C. Wu, H. C. Liu, **W. R. Chen**, and C. Y. Chang, "Enhanced Performance of Poly-Si Thin Film Transistors Using Fluorine Ions Implantation", *Electrochem. Solid-State Lett.*, **8**, pp. G246-G248 (2005)

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International conference:

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專利:

1. 陳緯仁、張俊彥、劉柏村、張鼎張、涂峻豪、葉睿龍，”具有奈米點之電荷儲存層的非揮發性記憶體”,(中華民國專利申請中申請案號: 096117223(2007/05/15)&美國專利送審中)
2. 陳緯仁、張俊彥、劉柏村、張鼎張、涂峻豪，”薄膜電晶體之多晶矽層的鈍化方法”，(中華民國專利申請中申請案號: 96117222(2007/05/15))
3. 陳緯仁、張俊彥、謝彥廷、張鼎張，”以四元化合物作為非揮發性記憶體儲存層的應用”，(中華民國專利申請中，申請案號: 96144787)

茂德科技合作專利

1. A novel method to form metal (W) nanocrystals for high-density non-volatile memory (中華民國專利申請中)
2. Tungsten (W) nanocrystals formed on N_2O-grown dielectric for high-reliability non-volatile memory(中華民國專利申請中)