國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

不同前處理對氮氧化鉿(鋯)閘極介電層於鍺基板之電物性研究

The Electrical and Physical Properties of Hf(Zr)-oxynitride Gate Dielectrics on Ge Substrates with Various Surface Pretreatments

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摘　要

對於四氟化碳和氨氣電漿前處理以及二矽乙烷的鈍化前處理方法，我們有系統地研究此三種表面前處理對於氮氧化鉿以及氮氧化鋯閘極介電層在鍺基板上之電物性。

我們發現高介電係數材料與鍺基板的接面和矽基板的接面有不同熱化學的特性；在矽基板與氮氧化鋯之間的接面層會因高溫處理而成長，並且有助於鋯金屬矽化物的形成。相反的，在鍺基板與氮氧化鋯之間的接面層會因高溫處理而揮發，並且抑制鋯金屬鍺化物的形成，此外，由於接面層揮發使介電層所產生的局部凹陷現象，亦會損害高介電係數材料/鍺基板元件結構的電性。

高介電係數材料/鍺基板結構會有很差的熱穩定性主要是由於低品質的鍺原生氧化層，因此沉積介電質後的熱退火處理以及沉積金屬電極後的熱

退火處理就被用來檢驗白金/高介電係數材料/鍺基板電容結構之熱穩定性。我們發現沉積介電質後的熱退火處理並不會增加鍺基板的捕捉缺陷(bulk traps)，而沉積金屬電極後的熱退火處理卻會使其增加。此外，這兩種熱退火處理都能削減接面載子捕捉密度(D_{it})與縮小等效氧化層厚度，但此二種熱處理過程卻同時增加了閘極漏電流。

四氟化碳電漿前處理會使白金/高介電係數材料/鍺基板電容結構中的遲滯寬度與閘極漏電流增大，這很可能是由於接面載子捕捉密度以及表面粗糙度的增加。另一方面，氨氣電漿前處理卻壓縮了遲滯寬度，這應該與較少的氧化鍺和接面載子捕捉密度有關，另外，此種氮化過程也能減少氧化鍺的成長以及它的揮發，因而改善白金/高介電係數材料/鍺基板電容結構的熱穩定性。

在攝氏五百五十度下熱脫附十分鐘以及接下來的二矽乙烷鈍化前處理已經成功地消除鍺的原生氧化層，因此大大縮小了遲滯的寬度，但是在高頻的電容-電壓曲線圖中，有經過二矽乙烷鈍化前處理的試片卻呈現出低頻的電容-電壓特性曲線。然而，這些表面前處理解決了遲滯現象並且改善了白金/高介電係數材料/鍺基板電容結構的熱穩定性，因此持續最佳化接面特性應能改善電性以及實現鍺基板結合高介電係數材料之元件。

The Electrical and Physical Properties of Hf(Zr)-oxynitride Gate Dielectrics on Ge Substrates with Various Surface Pretreatments

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ABSTRACT

We have systematically investigated the electrical and physical properties of HfO_xN_y and ZrO_xN_y gate dielectrics on Ge substrates with different surface pretreatments, including CF_4 plasma pretreatment, NH_3 plasma pretreatment and Si_2H_6 passivation.

We found that the interfacial layer of high-k/Si and high-k/Ge have distinct thermochemical properties; high temperature processing aided the interfacial layer growth and the formation of Zr–silicate in $ZrO_x(N_y)$/Si gate stack. On the contrary, severe interfacial layer volatilization and the inhibition of Zr–germinate were found in $ZrO_x(N_y)$/Ge system, moreover, the generated localized pits in deposited high-k films owing to the desorption of the interfacial layer might degrade the electrical properties of fabricated high-k/Ge devices.

The poor thermal stability of high-k/Ge gate stacks is due to inherent poor quality of Ge native oxide. Two thermal processes PDA and PMA are included to examine the thermal

stability of Pt/high-k/Ge capacitors. We found that the PDA process did not multiply the pre-existing bulk traps in Ge substrate but the PMA process increased them. Furthermore, both annealing processes were found to annihilate the amount of D_{it} and shrink the CET, but these thermal processed increased the gate leakage current at the same time.

The CF_4 plasma pretreatment enlarged the hysteresis width and gate leakage current of Pt/high-k/Ge capacitors, which were possibly due to the increment of D_{it} and surface roughness. On the other hand, the NH_3 plasma pretreatment compressed the hysteresis width, which was related with less GeO_x and D_{it}, moreover, this nitridation process improved the thermal stability of Pt/high-k/Ge capacitors by diminishing the formation of GeO_x and their volatilization.

The Ge native oxide was successful eliminated by thermal desorption at 550°C for 10 min and following Si_2H_6 passivation, which greatly reduced the hysteresis width of Pt/high-k/Ge capacitors, but the high frequency C-V curves of the Si_2H_6 passivation samples presented a low-frequency-like characteristic. However, those surface pretreatments solved the hysteresis effect and improved the thermal stability of Pt/high-k/Ge capacitors, thus the continuous optimization of the interface properties are expected to improve the electrical characterization and achieve the Ge device in combination with a high-k dielectric.

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Contents

Chapter 3 Post Dielectric/Metal Annealing

Chapter 4 CF_4 and NH_3 Plasma Pretreatment

Chapter 5 UHVCVD Si_2H_6 Passivation

Chapter 6 Conclusions and Suggestions for Future Work

Figure Captions

Chapter 1 Introduction

Chapter 2 The High-k/Ge Interface Properties

Chapter 3 Post Dielectric/Metal Annealing

Chapter 4 CF_4 and NH_3 Plasma Pretreatment

Chapter 5 UHVCVD Si_2H_6 Passivation

Chapter 1
Introduction

1-1 General Background

As the dimensions of complementary metal oxide semiconductor (CMOS) devices are scaled down to keep the continuous improvement on device performance, the thickness of the traditional SiO_2 gate dielectric will steadily decrease to 1.2 nm, which resulting in large leakage current and poor reliability. For n-channel MOSFET, the ideal drive current in saturation region can be expressed as

$$I_D = \frac{1}{2}\left(\frac{\varepsilon_{ox}}{t_{ox}}\right)\mu_n \frac{W}{L}\left(V_{GS} - V_T\right)^2 \tag{1.1}$$

Where ε_{ox} is the permittivity of gate oxide, t_{ox} is the gate oxide thickness, μ_n is the mobility for electrons, W is the channel width, L is the effective channel length, V_{GS} is the applied gate-to-source voltage and V_T is the threshold voltage. Besides decreasing the gate oxide thickness, it seems there are still many parameters in the above formula can be adjusted to improve the device driving capability. However, some approaches will bring about serious drawbacks. For instance, too large V_{GS} will create an undesirable high electric field across the gate oxide, which degrades the device reliability. Moreover, the reduction of V_T about 200 mV is limited because of the induced statistical fluctuations in thermal energy at a typical operation circumstance of up to 100°C. Therefore, the reduction of gate oxide

thickness and the shrinkage of the channel length are the simple ways which made the continuous improvement on device performance in the past two decades. However, scaling down of Si device's dimensions has approached to its fundamental physical limit. Therefore, new materials with higher dielectric constant and novel device structures must be developed.

Currently, the CMOS technology node of 90 nm is well developed, According to the International Technology Roadmap for Semiconductors (ITRS) [1], the equivalent oxide thickness (EOT) should be less than 1.6 nm for next generation. Figure 1-1 (a) and (b) depict the shrinking trend of equivalent oxide thickness as a function of technology node for microprocessor and low power devices. Although silicon oxy-nitride (SiON) gate dielectric has replaced SiO_2 to achieve 90 nm technology node by its better dielectric integrity and lower stress induced leakage current, the dielectric constant of SiON is not high enough for 65 nm technology node. Besides, as the thickness of SiO_2 and SiON is less than 1.2 nm, the direct tunneling effect will become a very critical issue to overcome. The resulting gate leakage current will not only degrade the device performance but increase the power dissipation. The relation between gate leakage current and EOT is shown in figure 1-2 (a) to (c) where "J_g,limit" is the gate leakage current density limit, and "J_g,simulated" is the expected value of the gate leakage current density from the simulations. Because of direct tunneling current, the leakage current limit cannot be met with using SiON after 2008 for the high-performance logic transistors. Furthermore, the J_g,simulated curve separates rapidly from

the J_g,limit curve after 2008, indicating that the gate leakage current would become completely out of specification if SiON were to continue to be used for the gate dielectric after 2008. Therefore, the high dielectric constant (high-k) material which significantly reduces gate leakage for a given EOT is clearly needed by 2008.

Recently, high-k materials such as Al_2O_3, ZrO_2, HfO_2 and their silicates [2-15] have been studied widely. Unfortunately, the dielectric constant of most high-k materials is inversely proportional to their band-gap, as shown in figure 1-3. Although the gate leakage current is suppressed by the thicker physical thickness of high-k materials at same EOT, the narrower band-gap and smaller band offset would enhance Schottky emission of carriers. Furthermore, the trap-assisted tunneling, Frenkel-Poole emission and the hopping effect are the problems remain to be solved. Consequently, there are several issues must be improved before those high-k materials take the place of SiO_2 and SiON.

(1) Thin interfacial layer.

(2) Low interface state density ($D_{it} < 10^{11}$ eV / cm^2)

(3) Thermodynamic stability in direct contact with substrate.

(4) High energy band-gap with more than 1 eV of conduction band offset to reduce carrier thermal emission.

(5) Low gate leakage current ($J_G < 1$ mA/cm^2 at $V_G = V_{FB} + 1$ V for PMOS and $V_G = V_{FB} - 1$ V for NMOS)

(6) Small hysteresis (hysteresis＜20 mV)

(7) Amorphous phase

(8) Good gate compatibility.

(9) Stable process compatibility, especially for the high temperature dopant activation of source/drain.

(10) Less mobility degradation.

On the other hand, improvements of carrier mobility can be obtained by replacing Si channel with strained Si [16]; however, a major breakthrough may be achieved if the conventional Si substrate is replaced by Ge which has high intrinsic carrier mobility. The hole mobility is four times grater than Si and electron mobility is twice as big as Si. Because of its higher low-field carrier mobility and smaller mobility band-gap for supply voltage scaling, there are many attempts to use Ge as a channel material in high-speed field-effect transistors. However, it still remains several important issues, which we have mentioned above, waiting to be solved.

1-2 Motivation

Recently, high-k materials such as HfO_2 [17] and ZrO_2 [18] have been under intense investigation for gate dielectric application into the 65 nm technology node and beyond to replace conventional SiO_2 or SiON because of the excessive leakage current and reliability

concerns. However, single oxide high-k dielectrics such as HfO_2 and ZrO_2 have been reported to be vulnerable to the diffusion of oxygen, which causes formation of a low-k interfacial layer. The incorporation of both Si and N into HfO_2 has attracted considerable interest because of its several improved features addressing those issues facing binary HfO_2, especially for the increase of crystallization temperature and the suppression of defect states caused by the oxygen vacancies in HfO_2 film. According to the report [19], Although HfSiON with optimized composition ratio remains amorphous state up to 1100°C, the dielectric constant of HfSiON is decrease to about 10, which is caused by the present of silicon oxide bonds. On the other hand, HfO_xN_y and ZrO_xN_y [20] seem to be promising for further scaling-down of EOT since incorporated nitrogen strengthen the immunity against oxygen diffusion as well as boron penetration [21] without lowering the dielectric constant.

As mentioned above, improvements of carrier mobility can be obtained by replacing Si channel with Ge channel owing to its higher intrinsic electron and hole mobility. Unfortunately, GeO_2/Ge exhibits unstable interface, poor electrical properties [22] and may be too disordered intrinsically [23], so the water–soluble and unstable germanium native oxides have been the main obstacles to Ge application. Consequently, growing high-k dielectric materials becomes a very attractive option to overcome the limitations of GeO_2 and provide alternatives to Si-based microelectronics. In this article, we investigate HfO_xN_y and ZrO_xN_y gate dielectrics on Ge substrate with different kinds of surface pretreatments to enhance

electrical properties of Ge MOS capacitor.

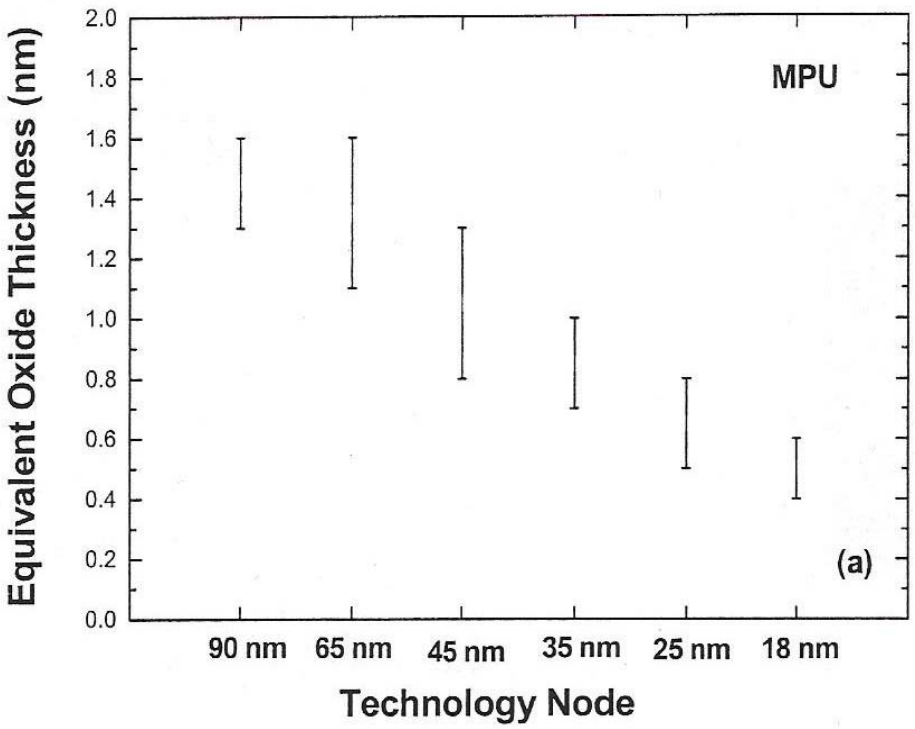
1-3 Organization of the Thesis

In chapter 2, we first studied the high-k/Ge interface properties and discussed about the thermal stability of high-k/Ge interface. We also found that the interfacial layer has distinct thermochemical properties on Ge and Si substrates. Various material analysis techniques, such as x-ray photoelectron spectroscopy (XPS), high-resolution transmission electron microscopy (HRTEM), secondary ion mass spectroscopy (SIMS) and atomic force microscopy (AFM), were performed to characterize the entire structures and surface morphology.

In chapter 3, we studied the effects of thermal processes in Pt/high-k/Ge gate stack by employing capacitance and conductance measurements. The interface properties and thermal stability of high-k/Ge gate stack which we had discussed helped us to understand the thermal mechanism of Pt/high-k/Ge capacitor.

In chapter 4 and chapter 5, we demonstrated three different kinds of surface pretreatments including CF_4 plasma pretreatment, NH_3 plasma pretreatment and Si_2H_6 passivation. These surface pretreatments were applied to solve the issues of Pt/high-k/Ge gate stack, such as hysteresis, thermal stability and frequency dispersion.

At the end of this thesis, chapter 6 gave the conclusion and suggestions for future works.



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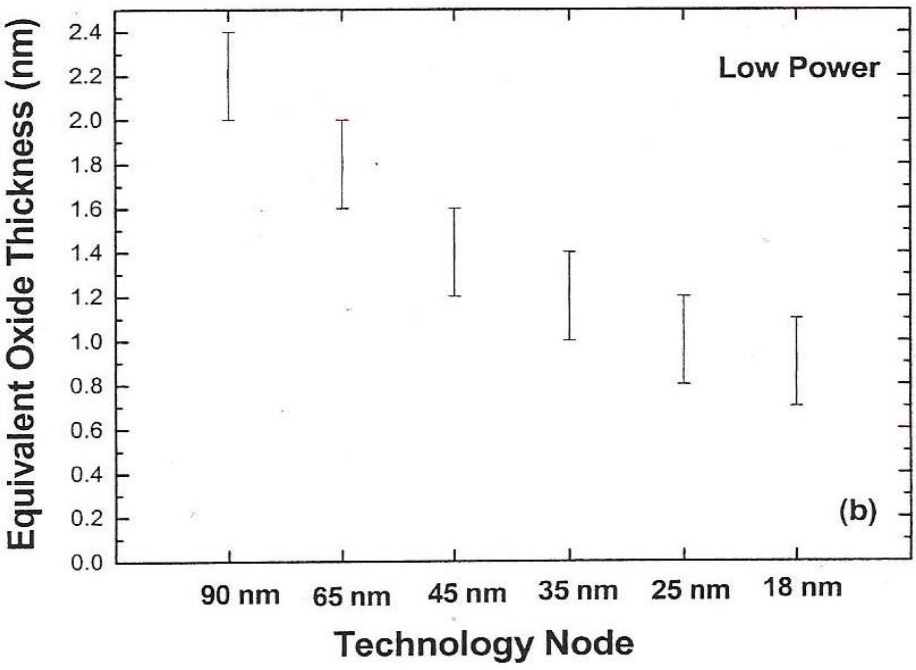

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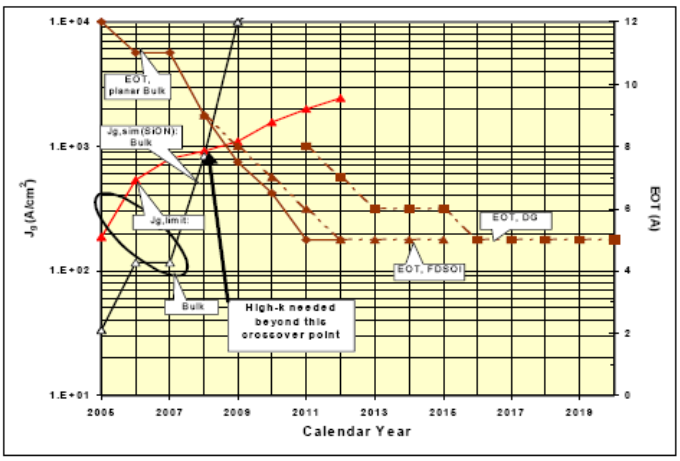
Fig. 1-1 The equivalent oxide thickness versus generation technology node for （a）microprocessor and （b）low power.



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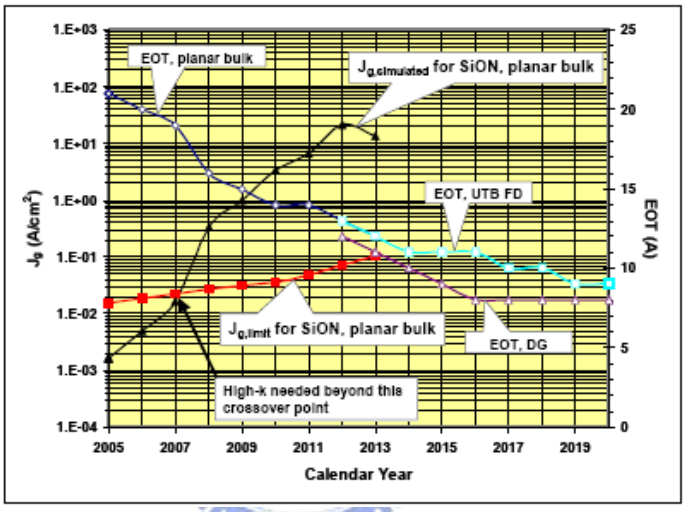

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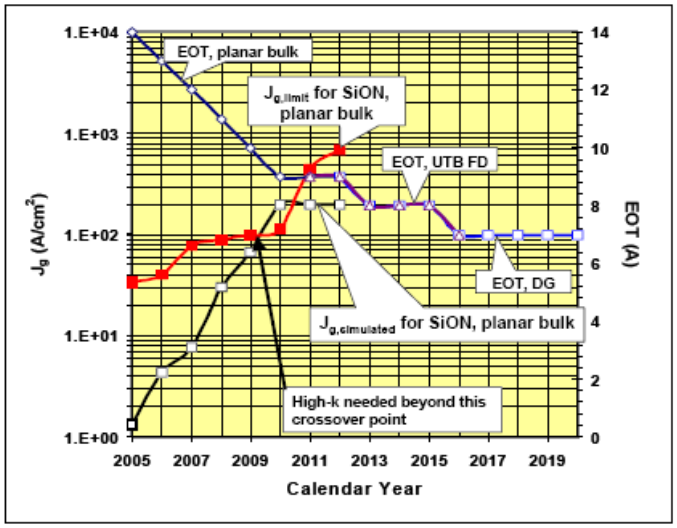


（c）

Fig. 1-2　J_g,limit versus J_g,simulated for （a）high-performance logic, （b）low-standby power and （c）low-operating power.

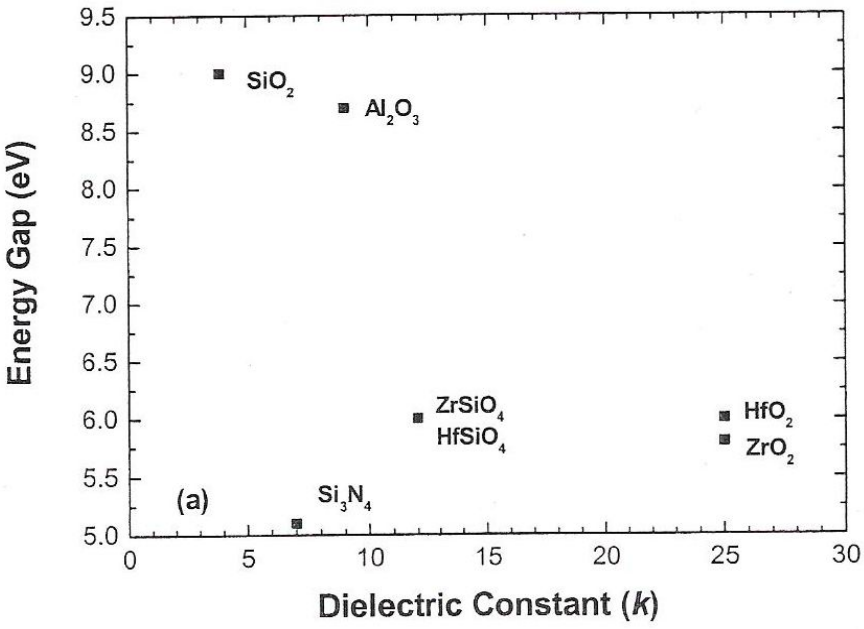


Fig. 1-3 Energy gap versus dielectric constant for SiO_2, Si_3N_4, Al_2O_3, $ZrSiO_4$, $HfSiO_4$, ZrO_2 and HfO_2.

Chapter 2
The High-k/Ge Interface Properties

2-1 Introduction

There have been extensive studies on several promising high-permittivity (high-k) candidates such as HfO_2 [24-25], ZrO_2 [26] and Al_2O_3 [27] deposited on Ge because of the application of its higher low-field carrier mobility; the admirable capacitance properties and transistor performances were continually demonstrated in recent years [28-29]. However, it seems essential to clarify what other advantages and disadvantages of Ge as a replacement of Si. For instance, the thinner lower-permittivity interfacial layer was observed in high-k/Ge system [30], which is beneficial in further scaling the equivalent-oxide-thickness (EOT) below 1 nm, meanwhile, this interfacial layer is very thermodynamically unstable which would degrade the electrical characterization seriously. This finding also implies that fundamental dissimilarities exist between the thermochemical properties of the Ge and Si. Annealing GeO_2 at 420°C results in the transformation of GeO_2 to GeO, and desorbs as GeO at higher temperatures. In contrast with SiO_2, SiO gets transformed into SiO_2 up to 780°C and decomposes to volatile SiO at higher temperatures [31]. Ge native oxide which is unstable and volatile grows easily on Ge surface when exposed to atmosphere. GeO_2 seems to play an important role in the interface of high-k/Ge system, so we need to comprehend the detailed

mechanism of high-k/Ge interface and how it affects our electrical characterization.

2-2 Experimental Procedures

(100) p-type Ge and Si wafers were subjected to a cleaning process sequence of deionized (DI) water rinse followed by diluted HF acid solution dipping for three cycles. Two different high-k thin films were then deposited by reactive sputtering chamber at 2 x 10^{-7} torr; ZrO_2 was deposited in an $Ar+O_2$ ambient [$O_2/Ar+O_2=0.2$] with a high-purity Zr target, while ZrO_xN_y was deposited in an $Ar+N_2$ ambient [$N_2/Ar+N_2=0.33$] with residual oxygen. For studying the interfacial reaction between the interfacial layer and Zr high-k dielectrics on Ge and Si substrates, we analyzed the effect of N_2 post-deposition annealing (PDA) on the chemical configuration by ex-situ x-ray photoelectron spectroscopy (XPS) using an Al Kα source (1486.6 eV). We also employed high-resolution transmission electron microscopy (HRTEM), secondary ion mass spectroscopy (SIMS) and atomic force microscopy (AFM) to characterize the entire structures and surface morphology.

2-3 Results and Discussion

2-3-1 X-ray photoelectron spectroscopy (XPS) and high-resolution transmission electron microscopy (HRTEM)

Figure 2-1 (a) to (c) display the core-level spectra of Si 2*p*, N 1*s* and O 1*s* for the ZrO_xN_y

ultra-thin films on Si substrates before and after 500°C or 600°C PDA, respectively. The binding energies of Si-Si, Si-N and SiO_2 are 99.5 eV, 102.5 eV and 103.7 eV in Si 2*p* spectrum. We observed that as the PDA temperature increases, the intensity of SiO_2 increases clearly, which corresponds to the formation of the interfacial layer as O 1*s* spectrum. Furthermore, the peak of O 1*s* spectrum shifts to higher binding energy also indicates the transition from ZrO_2 to Zr–silicate.

Figure 2-2 (a) to (c) show the core-level spectra of Ge 2*p*, Ge 3*d* and O 1*s* for the ZrO_xN_y ultra-thin films on Ge substrates before and after different PDA temperatures. The energies of Ge-Ge, GeO and GeO_2 in Ge 2*p* spectrum are 1217.6 eV, 1219.1 eV and 1220.6 eV, respectively. Dissimilarly, the intensity of GeO_2 is diminished with the increasing PDA temperatures, which indicates that thermally induced transformation of GeO_x ($x \leqq 2$) into GeO gaseous species led to severe interfacial layer desorption through the top high-k films.

As far as the loss of Ge oxide species is concerned, Ogino and Amemiya proposed two possible reaction mechanisms [32-33] as follows:

$$Ge(s) + GeO_2(s) \rightarrow 2GeO(v) \tag{2.1}$$

$$Ge(s) + \frac{1}{2}O_2(v) \rightarrow GeO(v). \tag{2.2}$$

The critical temperature, at which the chemical reduction of GeO_2 into volatile GeO takes place, was reported to range from 350°C to 550°C [34-36]. Higher temperature is believed to be able to accelerate the desorption rate via the mechanism (2.1). Besides, residual oxygen in

an N_2 ambient may diffuse through the high-k film and trigger the mechanism (2.2). Therefore, higher thermal annealing temperature leads to GeO_x volatilizes acutely, which is also evidenced by the reduced intensities of the corresponding O 1*s* spectra.

Figure 2-3 (a) and (b) show the Zr 3*d* core-level spectra of ZrO_xN_y thin films on Si and Ge substrate. We observed the spectrum of ZrO_xN_y/Si gate stacks shifting to higher binding energy and becoming almost identical after 600°C PDA; this finding indicates that high-temperature annealing tends to convert both the Zr–N and Zr–O bonds into the configuration of Zr–O–Si bond [37-38]. From the O 1*s* broad spectra in figure 2-1 (c), we confirm this tendency by observing the shifting toward higher binding energy and the increased peak intensity, which is also consistent with the findings of the Si 2*p* spectra in figure 2-1 (a). Interestingly, there is no evidence of the emergence of interfacial Zr–O–Ge bonding albeit 600°C annealing.

Figure 2-4 (a) to (c) display the core-level spectra of Si 2*p*, N 1*s* and O 1*s* for the ZrO_2 ultra-thin films on Si substrates before and after 500°C or 600°C PDA, respectively. Similar to ZrO_xN_y case, the intensity of SiO_2 increases with the PDA temperature increases, meanwhile the O 1*s* spectrum also show the transition from ZrO_2 to Zr–silicate. Deservedly, there is no Si-N signal in ZrO_2 case.

The spectra in figure 2-5 also suggest that higher annealing temperature would accelerate the desorption rate of GeO_2 whatever the high-k film is ZrO_2 or ZrO_xN_y. Figure 2-6 (a) and (b)

show the Zr 3*d* core-level spectra of ZrO_2 thin films on Si and Ge substrate. Without any thermal process, the interfacial layer tends to be Zr–silicate on Si substrate for the ZrO_2 case. After 600°C PDA, the Zr 3*d* spectrum shifted to 183.8 eV which is the same value in ZrO_xN_y case. In figure 2-6 (b), the subsequent 600°C annealing still can not prompt the occurrence of Zr–germinate, i.e., $ZrGeO_x$: indeed, the spectrum profiles even slightly move backward to lower binding energy.

The purpose of comparing these two Ge spectra (Ge 2*p* and Ge 3*d*) was due to the fact that they have significantly different sampling depths. Through the curve fitting for these two Ge core-levels with mixed Gaussian-Lorentzian line shapes, the amounts of three components (Ge, GeO and GeO_2) were extracted, as illustrated in figure 2-7; the inset displays the HRTEM image of as-deposited ZrO_2 thin film, in which an interfacial layer of ca. 22 Å can be equivocally seen, showing agreement with the estimated thickness of ca. 20 Å by XPS calculation [39]. After annealing at 600°C, the GeO_x–contained interfacial layer certainly revealed acute volatilization, which was also evidenced by the reduced intensity of the corresponding O 1*s* spectrum.

2-3-2 Secondary ion mass spectroscopy (SIMS) and atomic force microscopy (AFM)

We did not show the N 1*s* core-level spectra for Ge substrate in figure 2-2 because the

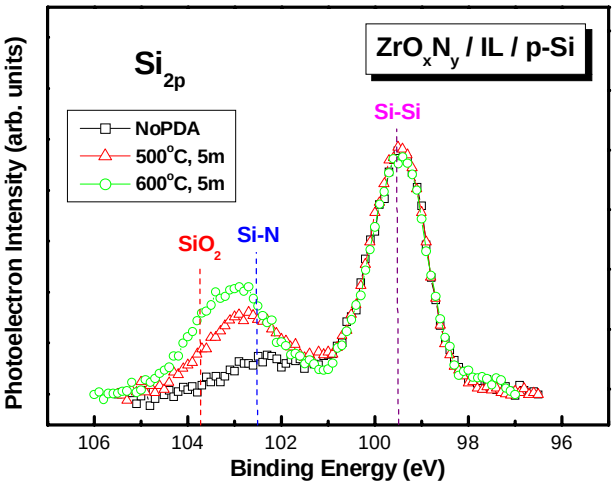
Ge-N bonds signal was too slight to be detected for XPS, where we verified it in figure 2-8 (a) again, and furthermore increasing annealing temperature would accelerate the breaks of Ge-N bonds. On the contrary, the intensity of Si-N bonds was very strong in figure 2-1, which was corresponded to the result of figure 2-8 (a). In figure 2-8 (b), we found out that Ge diffused into ZrO_xN_y after 600°C PDA, which was resembled in XPS result and severely degraded the electrical properties of fabricated high-k/Ge devices.

Figure 2-9 and figure 2-10 show the AFM images with different annealing temperatures of Ge substrate. The room-mean-square (RMS) surface roughness was increased with the higher annealing temperatures, indicating that more GeO_2 transformed into volatile GeO and left a lot of small pits and holes on the Ge substrate. Figure 2-11 is the AFM images of ZrO_xN_y/Si gate stack with and without PDA, and we observed that the surface roughness did not change apparently even after 600°C PDA. However, the surface morphology of ZrO_xN_y overlayer on Ge substrate was clearly damaged after 600°C annealing, as shown in figure 2-12 and 2-13; this in turn possibly created a considerably high defect density and then severely jeopardized the insulating properties of high-k thin film on Ge [40]. Moreover, the surface morphology of ZrO_2 overlayer on Ge substrate was damaged seriously after 600°C annealing, as shown in figure 2-14. We also noticed that the surface roughness of ZrO_2/Ge gate stack was higher than that of ZrO_xN_y/Ge gate stack, which might due to a great deal of GeO_x was formed during ZrO_2 deposition. With above examinations, we speculate that the

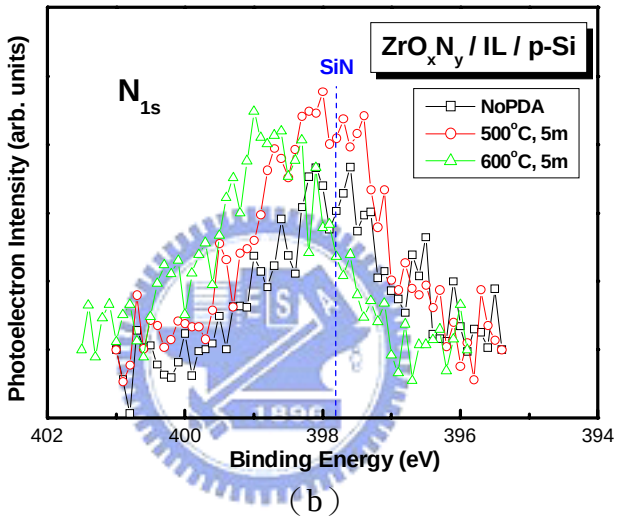
desorption of GeO_x–contained interfacial layer is the possible origin of why we did not observe the formation of Zr–germinate after high temperature annealing on Ge.

2-4 Summary

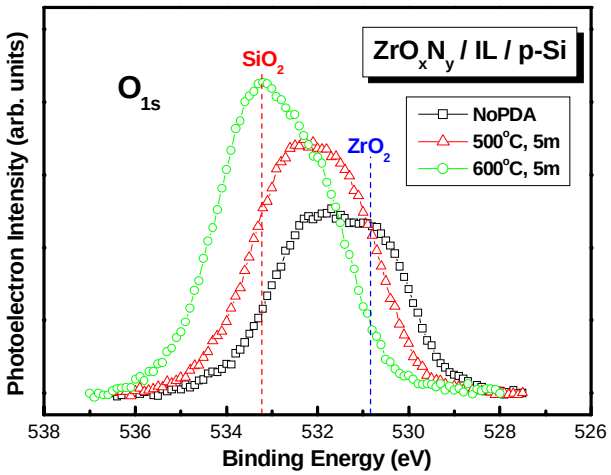
In this chapter, we have studied the high-k/Ge interface properties and discussed about the thermal stability of high-k/substrate interface on Ge is not as good as that on Si due to inherent poor quality of Ge native oxide. We found that the interfacial layer has distinct thermochemical properties on these two substrates. High temperature processing aided the interfacial layer growth and the formation of Zr–silicate in $ZrO_x(N_y)$/Si gate stack. On the contrary, severe interfacial layer volatilization and the inhibition of Zr–germinate were found in $ZrO_x(N_y)$/Ge system; these features are expected to possess a better EOT scalability with respect to $ZrO_x(N_y)$/Si system. However, the generated localized pits in deposited high-k films owing to the desorption of the underlying interfacial layer may severely degrade the electrical properties of fabricated high-k/Ge devices.



（a）

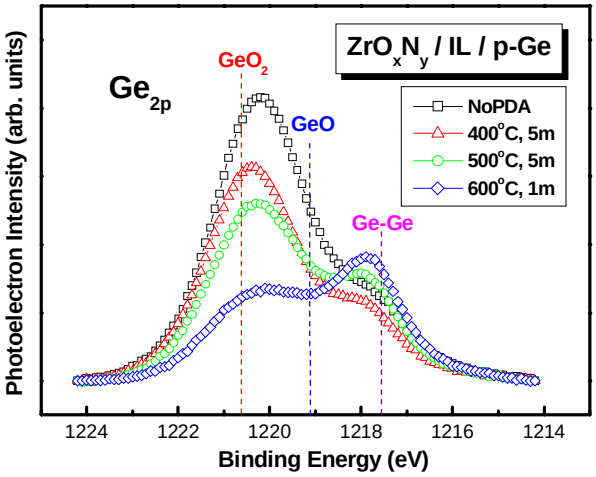


（b）

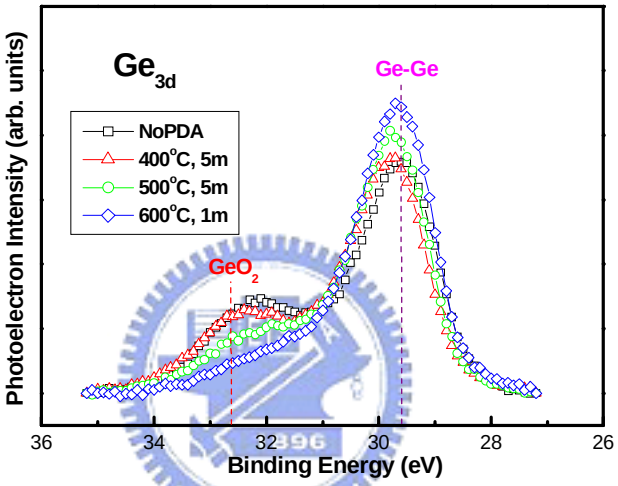


（c）

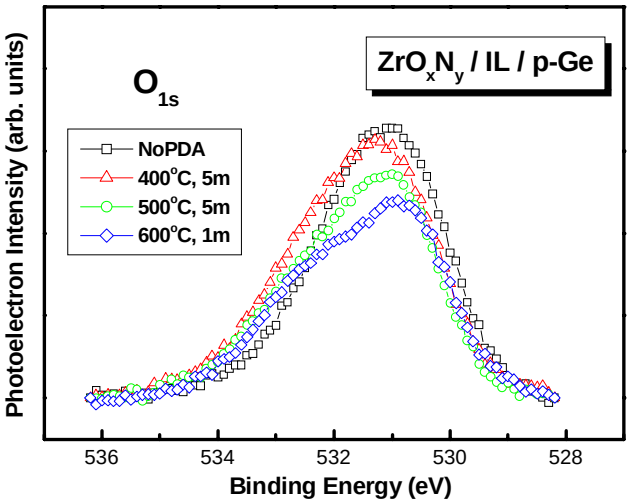
Fig. 2-1 （a）Si 2*p*, （b）N 1*s* and （c）O 1*s* core-level spectra of ZrO_xN_y thin films on Si substrates before and after different PDA temperatures.



(a)

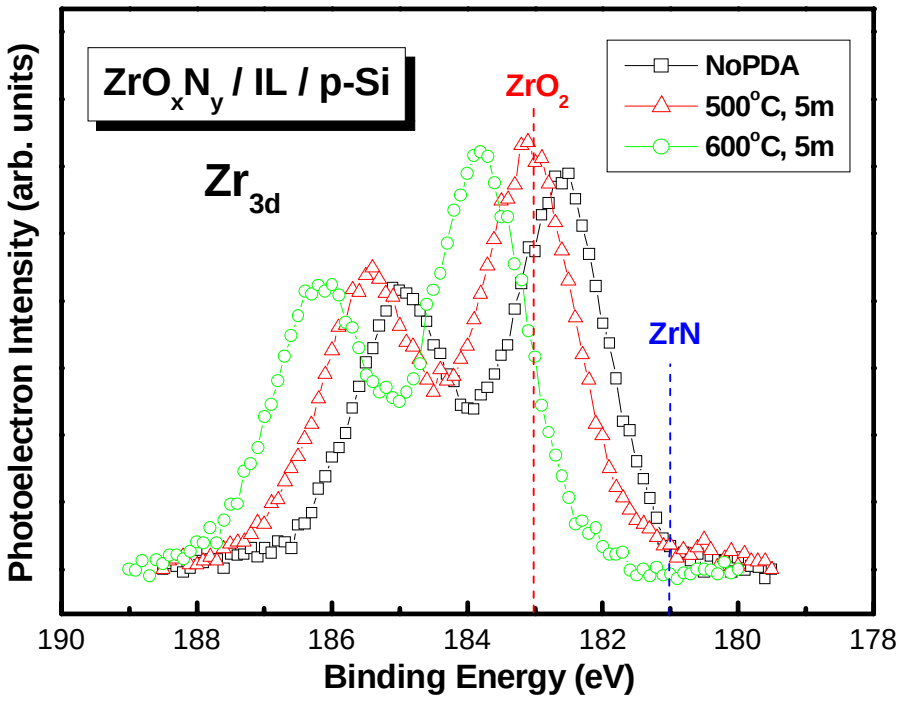


(b)

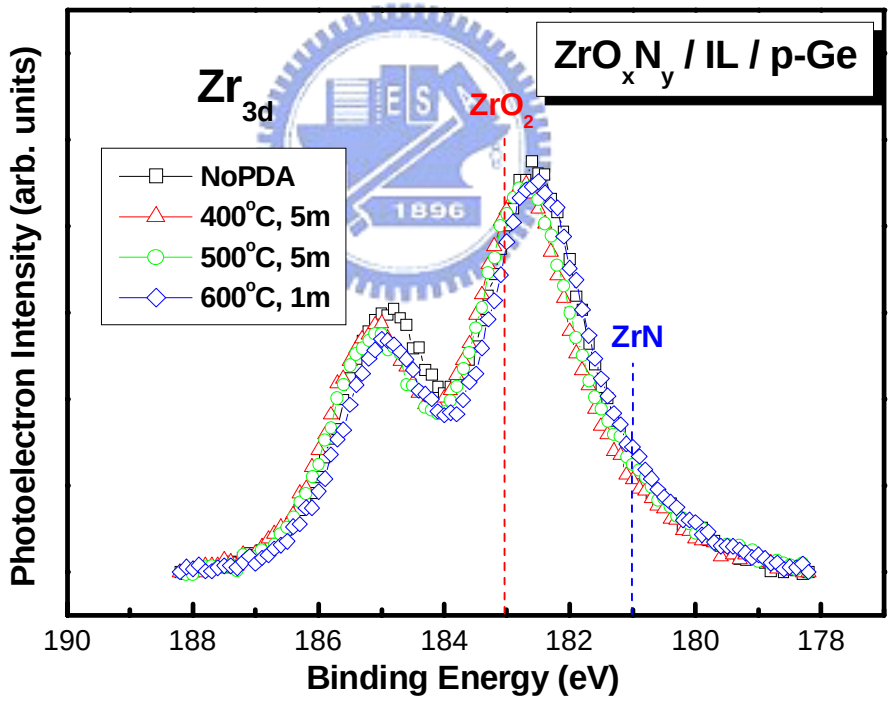


(c)

Fig. 2-2 (a) Ge 2*p*, (b) Ge 3*d* and (c) O 1*s* core-level spectra of ZrO_xN_y thin films on Ge substrates before and after different PDA temperatures.

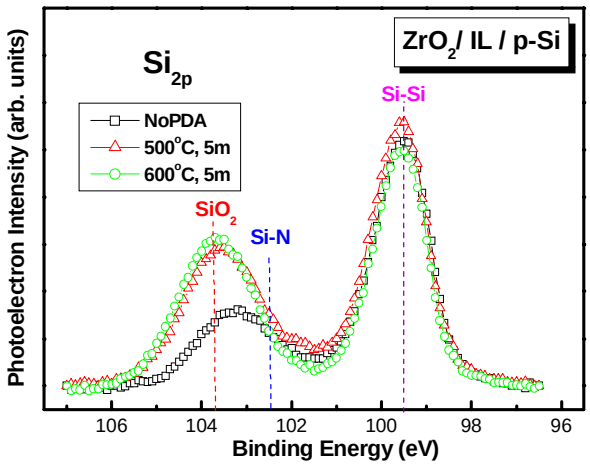


（a）

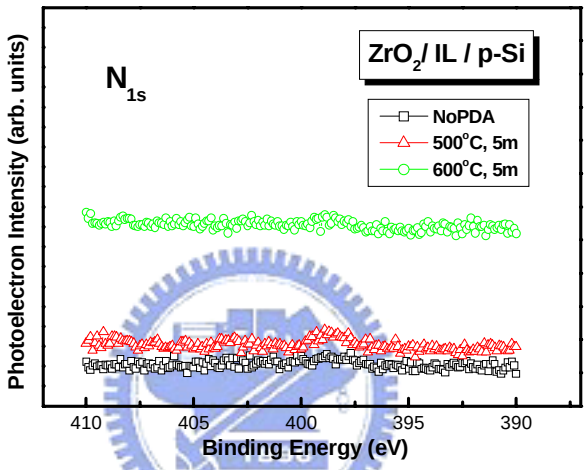


（b）

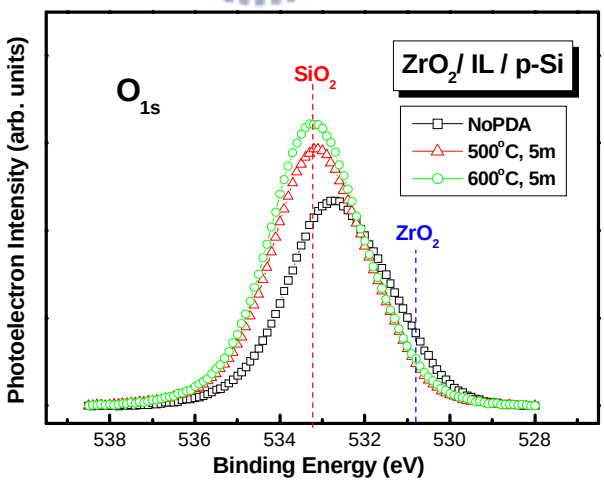
Fig. 2-3　Zr 3*d* core-level spectra of ZrO_xN_y thin films on （a）Si and （b）Ge substrates before and after different PDA temperatures.



（a）

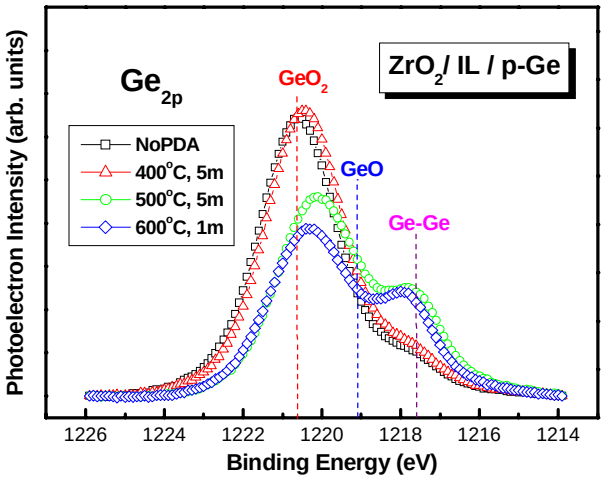


（b）

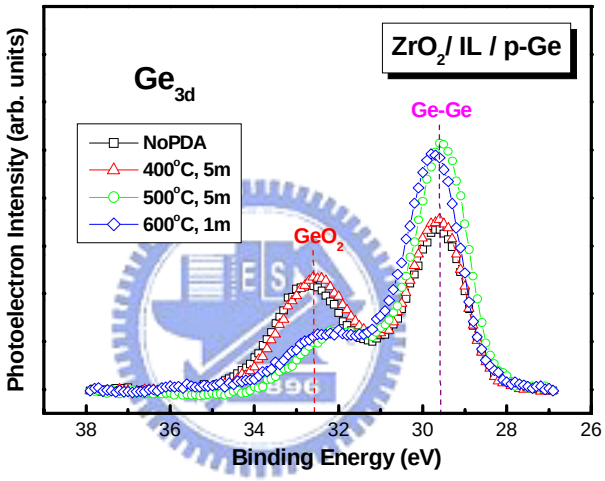


（c）

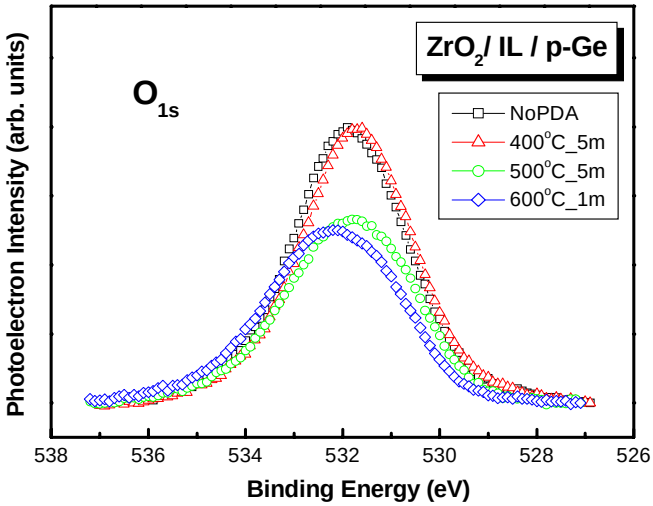
Fig. 2-4 （a）Si 2*p*, （b）N 1*s* and （c）O 1*s* core-level spectra of ZrO_2 thin films on Si substrates before and after different PDA temperatures.



（a）



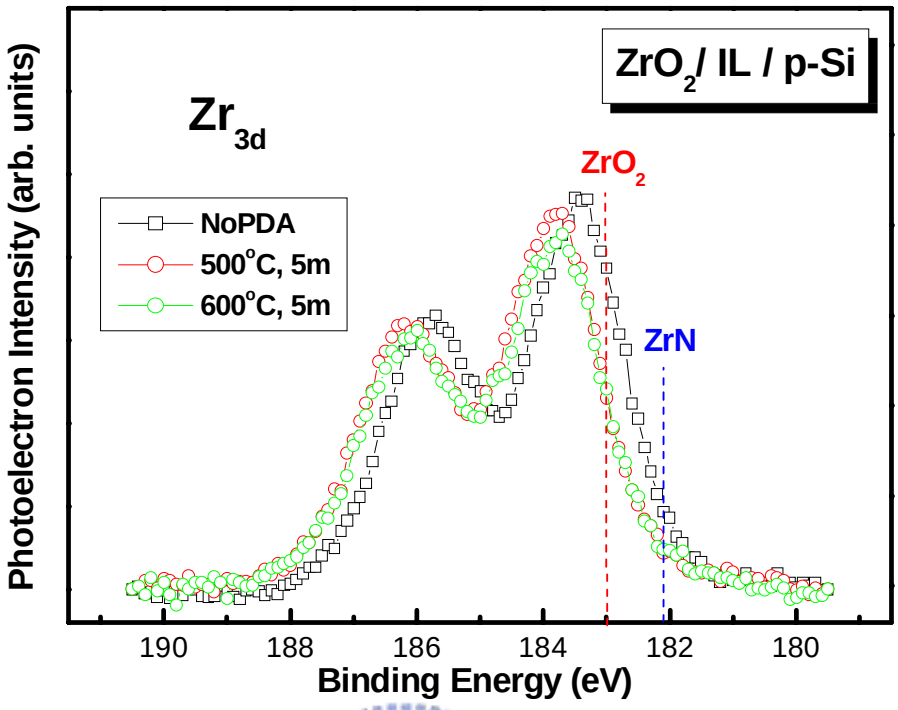
（b）



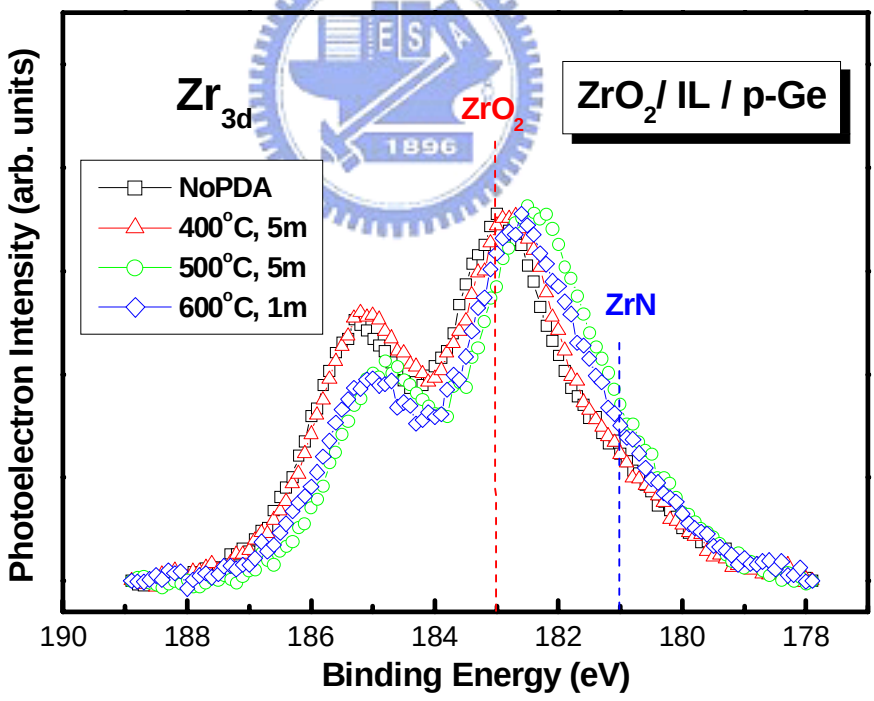
（c）

Fig. 2-5 （a）Ge 2*p*, （b）Ge 3*d* and （c）O 1*s* core-level spectra of ZrO_2 thin films on Ge

substrates before and after different PDA temperatures.



(a)



(b)

Fig. 2-6 Zr 3*d* core-level spectra of ZrO_2 thin films on (a) Si and (b) Ge substrates before and after different PDA temperatures.

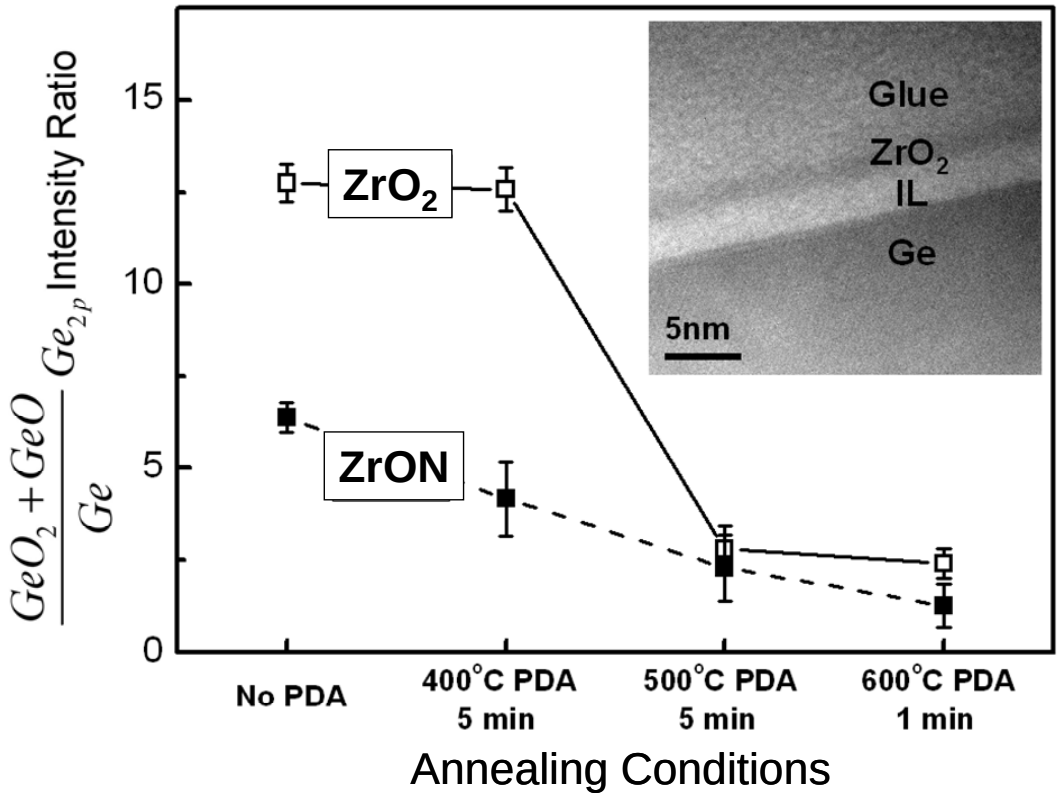
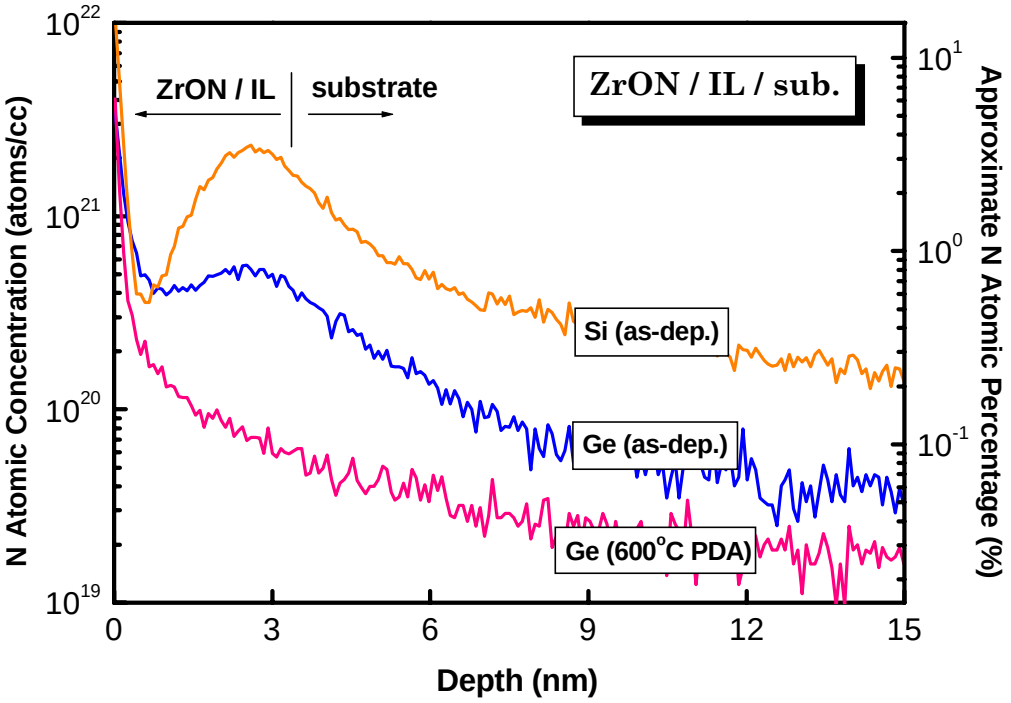
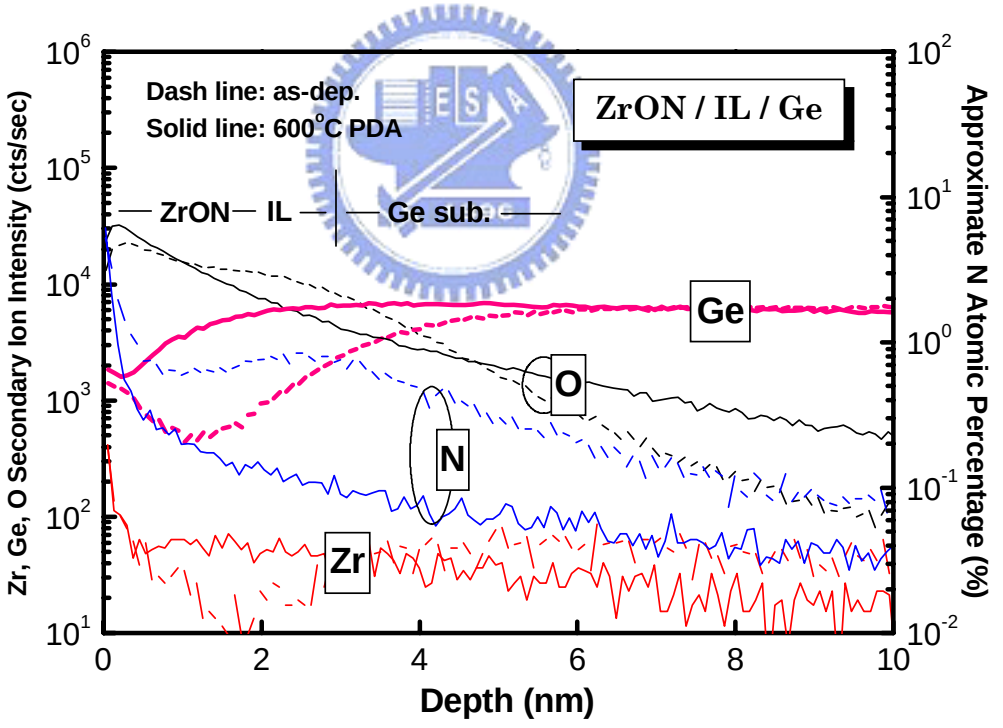


Fig. 2-7 The ratio of GeO_x to Ge substrate versus annealing conditions for ZrO_xN_y/Ge and ZrO_2/Ge gate stacks. Inset: cross-sectional TEM image of ZrO_2/Ge gate stacks before annealing.

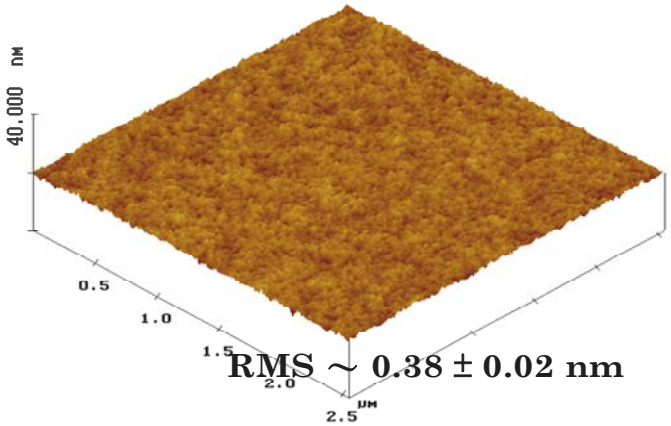


（a）

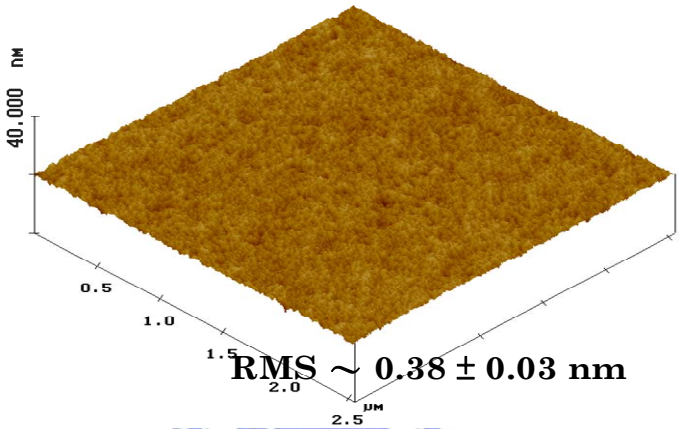


（b）

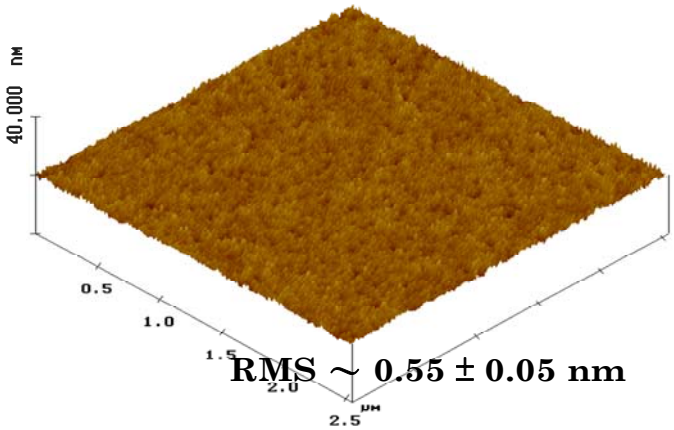
Fig. 2-8　The SIMS depth profiles for ZrO_xN_y thin films on （a）Si and Ge substrates and （b）Ge substrates before and after 600°C PDA.



（a）



（b）



（c）

Fig. 2-9　The AFM images of Ge substrate with （a）no annealing, （b）400°C annealing for 5 min and （c）500°C annealing for 5 min.

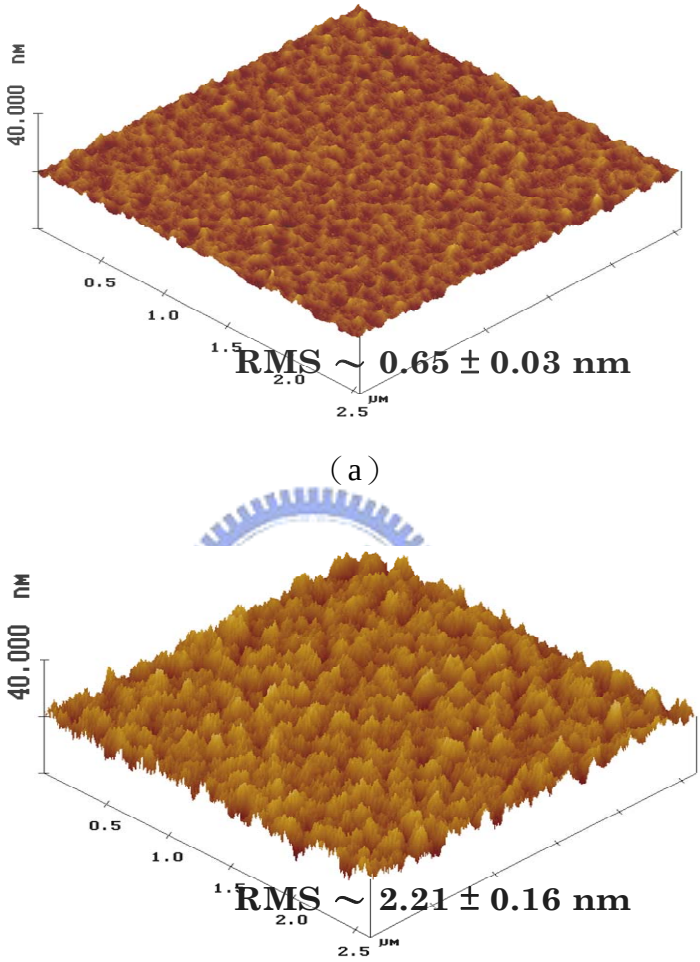
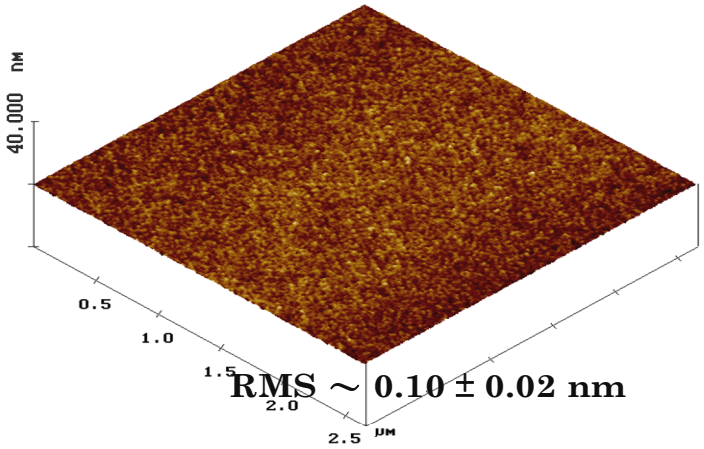
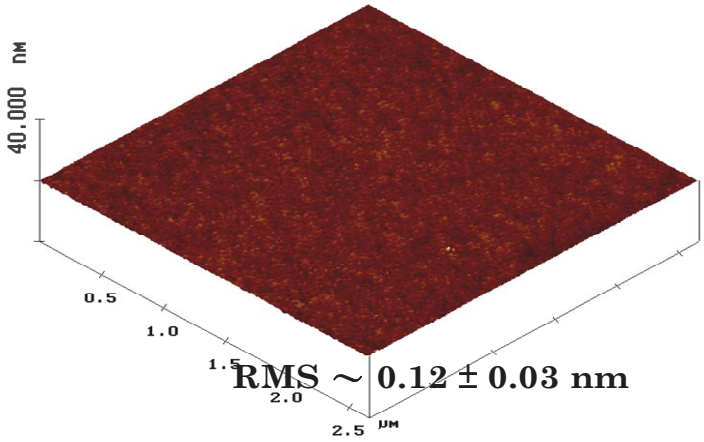


Fig. 2-10 The AFM images of Ge substrate with （a）600°C annealing for 1 min and （b）600°C annealing for 5 min.

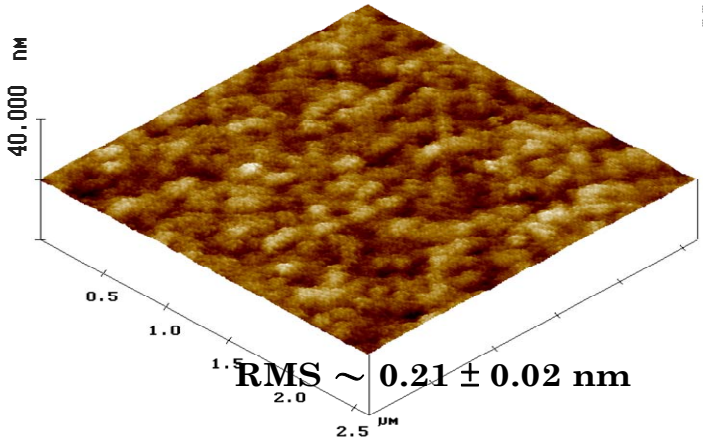


（a）

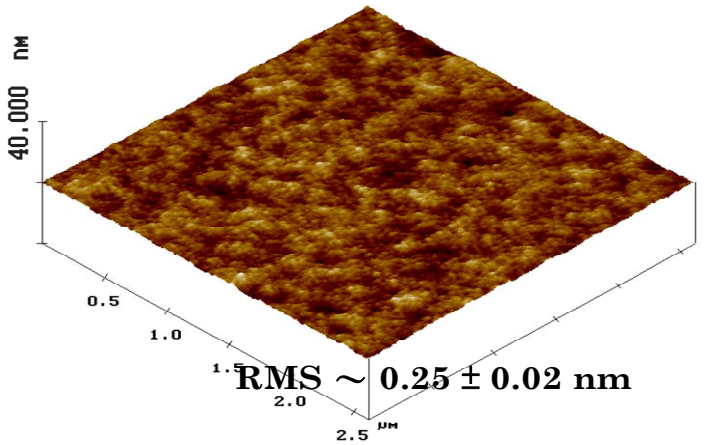


（b）

Fig. 2-11　The AFM images of ZrO_xN_y/Si gate stack with （a）as-deposited and （b）600°C PDA for 5 min.

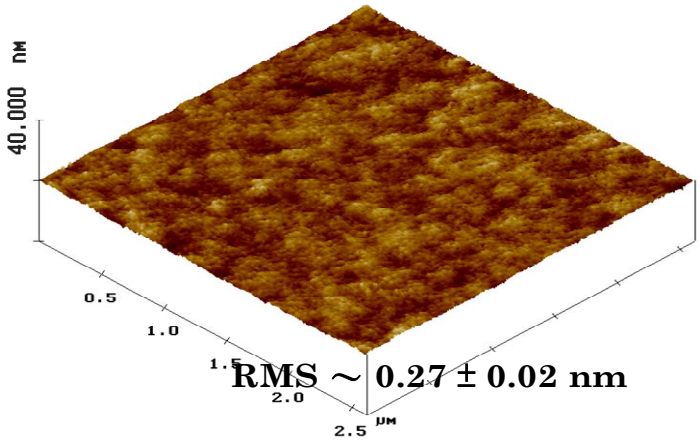


（a）

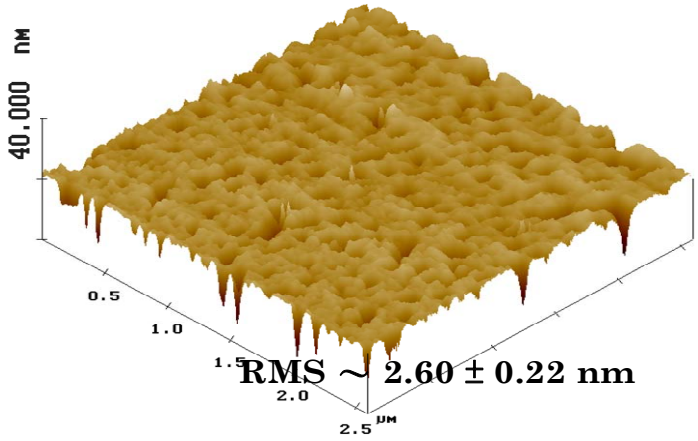


（b）

Fig. 2-12　The AFM images of ZrO_xN_y/Ge gate stack with （a）as-deposited and （b）500°C PDA for 5 min.



（a）



（b）

Fig. 2-13　The AFM images of ZrO_xN_y/Ge gate stack with （a）600°C PDA for 1 min and （b）600°C PDA for 5 min.

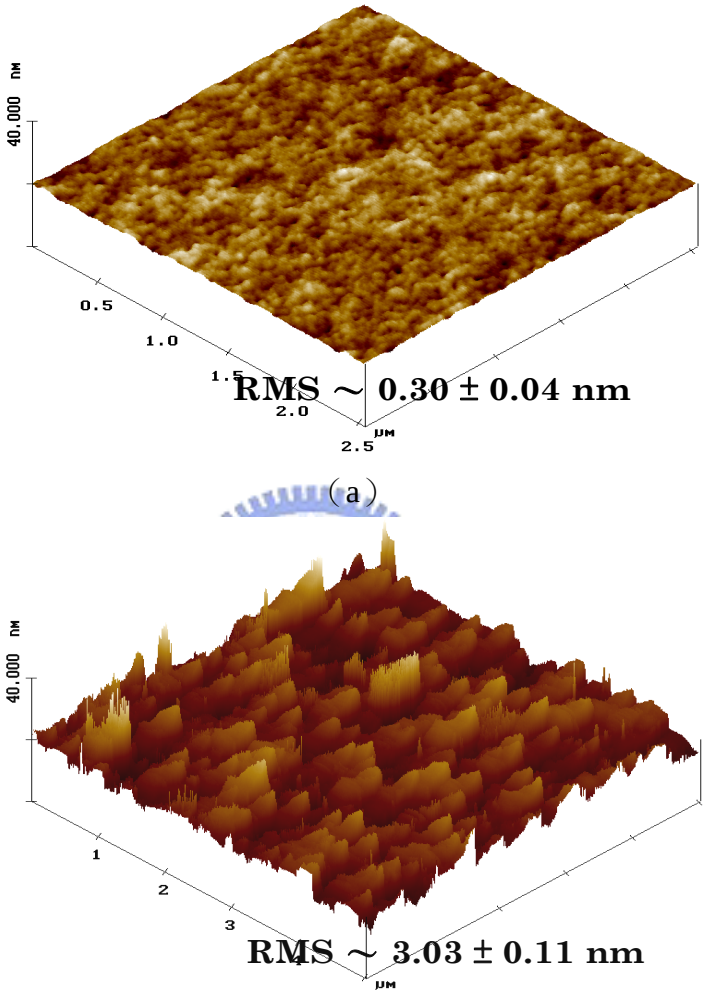


Fig. 2-14 The AFM images of ZrO_2/Ge gate stack with （a）600°C PDA for 1 min and （b） 600°C PDA for 5 min.

Chapter 3
Post Dielectric/Metal Annealing

3-1 Introduction

Silicon has been used in CMOS technology for decades due to better qualities of its native oxide such as low interface state density and good thermal stability. But, with further downscaling device dimensions and the shrinkage of gate oxide thickness to nanometer range, the leakage current density of SiO_2 is too large to be accepted. Recently, Ge-channel devices which including bulk Ge [41-42] and strained Ge [43] with the integration of high-k gate dielectrics have gained considerable research interest. Some materials which have high dielectric constant are being introduced to suppress excessive leakage concern with a thicker physical thickness while still maintaining the capacitance equivalent thickness (CET) of the scaled devices. Up to the present, HfO_2, ZrO_2 and their oxynitride are the uppermost candidates among all potential high-k dielectrics. Both Si and Ge MOSFETs with high-k gate dielectrics have shown some promising performances [44-45]. Our work presents the electrical characteristics of HfO_xN_y thin films deposited on bulk Ge substrate, and the impact of thermal anneal processing on entire capacitor structures is also studied.

3-2 Experimental Procedures

MOS capacitors were fabricated on (100) oriented n-type Ge substrates which were doped with Sb having a resistivity of 8–12 Ω·cm. Deionized (DI) water rinse followed by diluted HF acid solution dipping for three cycles in order to remove Ge native oxide. Subsequently, HfO_xN_y thin films were first deposited through reactive sputtering in an $Ar+N_2$ [$N_2/Ar+N_2=0.33$] ambient with a pure Hf target, and then annealing in N_2 gas with residual oxygen. Next, a 1000 Å layer of platinum (Pt) dot was deposited using electron beam evaporation through a shadow mask. Finally, Al was deposited on the backside of Ge wafer to reduce the contact and series resistances. For comparison, as-deposited HfO_xN_y films were annealed at the temperatures of 500°C and 600°C, respectively; same annealing conditions were employed after metallization for evaluating thermal stability of the Pt/high-k/Ge structures. The capacitance–voltage (C–V) and conductance–voltage (G–V) curves were measured using an HP4284 LCR meter, while the current–voltage (I–V) characteristics were measured using a Keithley 4200 semiconductor analyzer system. The series resistance was extracted and then applied as a correction to the measured capacitance and conductance. The interface state density (D_{it}) at the midgap is determined from G–V characteristics by using Hill's method [46].

3-3 Results and Discussion

Figure 3-1 (a) and (b) display typical 100-kHz C–V and G–V characteristics of the HfO_xN_y/Ge capacitors before and after post dielectric annealing (PDA), the sweep direction of all curves presented in our figures are from V_g = +2 V to V_g = -2 V; that is from strong accumulation to strong inversion. The CET estimated at V_g = +2 V in C–V curves was ca. 28 Å for as-deposited samples and decreased to ca. 25 Å and ca. 22 Å after annealing at 500°C for 30 sec and 5 min, respectively. The further CET scaling could be achieved by extending annealing duration or increasing the annealing temperatures. Consequently, we believe that annealing processes not only made the densification of HfO_xN_y film but also the shrinkage of interfacial layer, showing agreement with the observation in chapter 2. Furthermore, the G–V characteristics obviously revealed the energy loss peak, corresponding to the hump observed in the depletion region in C–V curves, indicating the existence of fast interface states at the HfO_xN_y/Ge interface. Another noteworthy feature was that the measured conductance in inversion showed gate-bias independence; this phenomenon is rare for traditional Si MOS capacitors. Figure 3-2 shows the C–V and G–V characteristics of the HfO_xN_y/Si capacitor at 100-kHz, the equivalent parallel conductance goes through a peak in weak inversion and immediately drops to a very low value in strong inversion. In contrast with HfO_xN_y/Ge capacitors case, the gate-bias independent conductance observed in inversion reflects the fact that the generation and recombination of minority carriers indeed contributes an energy loss in

inversion and competes with interface state loss in depletion.

Figure 3-3 (a) and (b) display typical 100-kHz C–V and G–V characteristics of the HfO_xN_y/Ge capacitors before and after post metal annealing (PMA), respectively. The lowest CET value of ca. 23 Å was achieved after PMA at 500°C for 5 min. In comparison with PDA processes, the PMA process apparently relieves the hump emerged in as-deposited sample, as evidenced by vanishing conductance peak in G–V curves. Interestingly, PMA samples depict contrasting behavior in inversion as compared to PDA ones; the measured capacitance and conductance simultaneously raise with increasing PMA temperature and time, which is a typical characteristic of the increase of bulk traps presumably caused by introducing Pt atoms during high temperature annealing, as shown in figure 3-4. Except for the contribution to more bulk traps loss, the bulky defects with energy levels near midgap in Ge, which are also responsible for the supply of minority carriers to the inversion layer, incur the onset of low-frequency-like C–V characteristic, even in the kHz range.

Figure 3-5 analyzed D_{it} with different kinds of annealing conditions. The as-deposited HfO_xN_y/Ge sample revealed a large value of the D_{it} of ca. 4 x 10^{12} $cm^{-2}eV^{-1}$, which probably associated with poor quality of the interfacial layer. However, the D_{it} reduced to ca. 2.5 x 10^{12} and ca. 1 x 10^{12} $cm^{-2}eV^{-1}$ for PDA and PMA samples, respectively. In order to figure out the charge trapping effect and the improvement of interface quality during annealing, we discussed them together with the examination of the V_{fb} in figure 3-6. The V_{fb} of as-deposited

sample was ca. 0.35 V lower than the ideal work-function difference which is ca. 0.9 eV between Pt electrode and n-Ge substrate, implying that substantial positive charges have been introduced in the gate dielectric/interfacial layer during the post-process. With increasing the annealing temperature, the value of V_{fb} undergoes a positive shift, indicating that positive charges have been remedied by high temperature annealing, otherwise, the diffusion of Ge or the volatilization of GeO would generate additional negative charges and led to the charge neutralization.

The volatilization of GeO not only made the shrinkage of interfacial layer but also created the leakage-paths in the gate dielectric, as shown in figure 3-7, the gate leakage current increased with the higher annealing temperature, which was coincided with the amount of GeO volatilization. Figure 3-8 depict the hysteresis of Pt/high-k/Ge capacitors which hysteresis was about 600 to 700 mV except PMA at 600°C for 5 min. The large gate leakage current resulted in the abrupt reduction of hysteresis of PMA 600°C sample. In contrast with Pt/high-k/Si capacitors, the negligible hysteresis was below 50mV. The detailed analysis of hysteresis will be discussed in next chapter.

3-4 Summary

In this chapter, we found that the PDA process did not multiply the pre-existing bulk traps in Ge substrate, which was conformed by corresponding G–V results, whereas the PMA

process increased them, and thus presented low-frequency-like behavior in high-frequency C–V curves. Furthermore, both annealing processes were found to annihilate the amount of D_{it} and shrink the CET, but these thermal processed increased the gate leakage current at the same time.

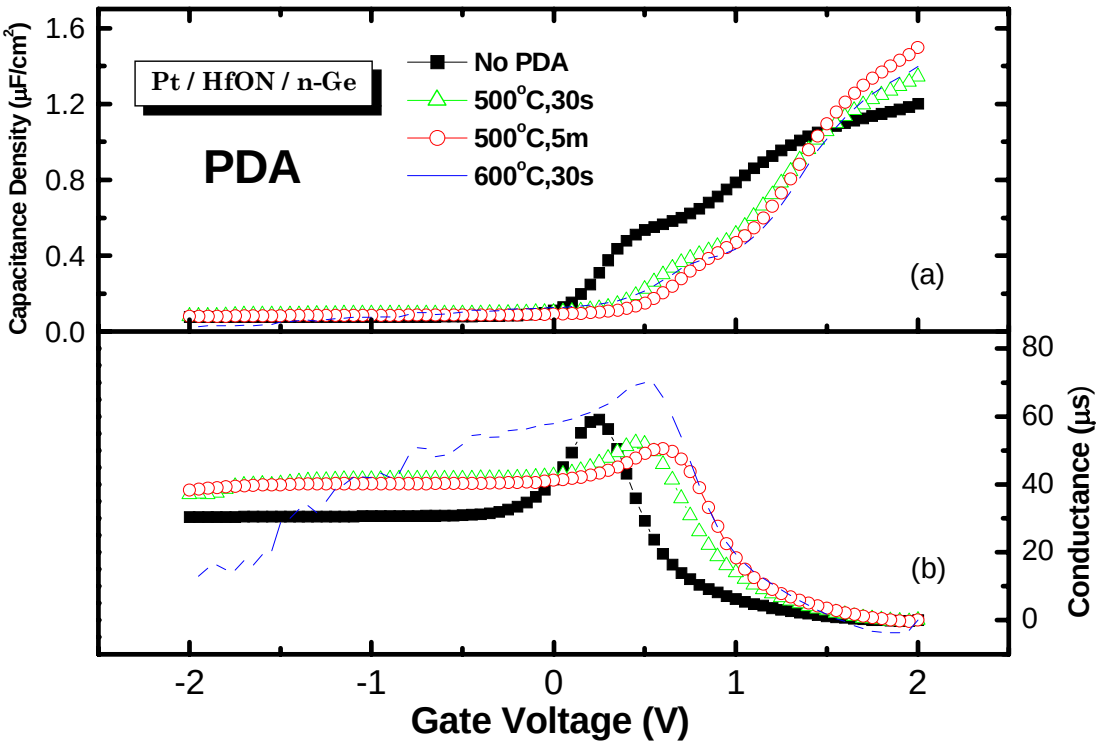


Fig. 3-1 Typical 100-kHz（a）C–V and （b）G–V curves of Pt/HfO_xN_y/n-Ge capacitors before and after PDA, respectively.

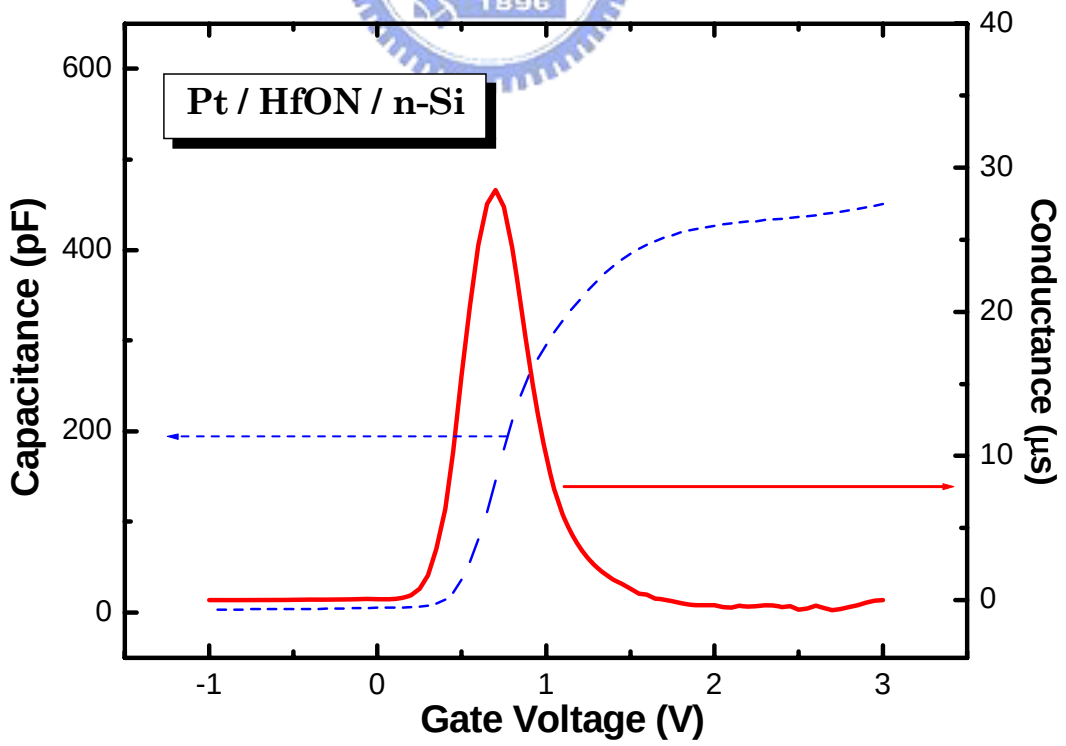


Fig. 3-2 C–V (dash) and G–V (solid) curves of Pt/HfO_xN_y/n-Si capacitors.

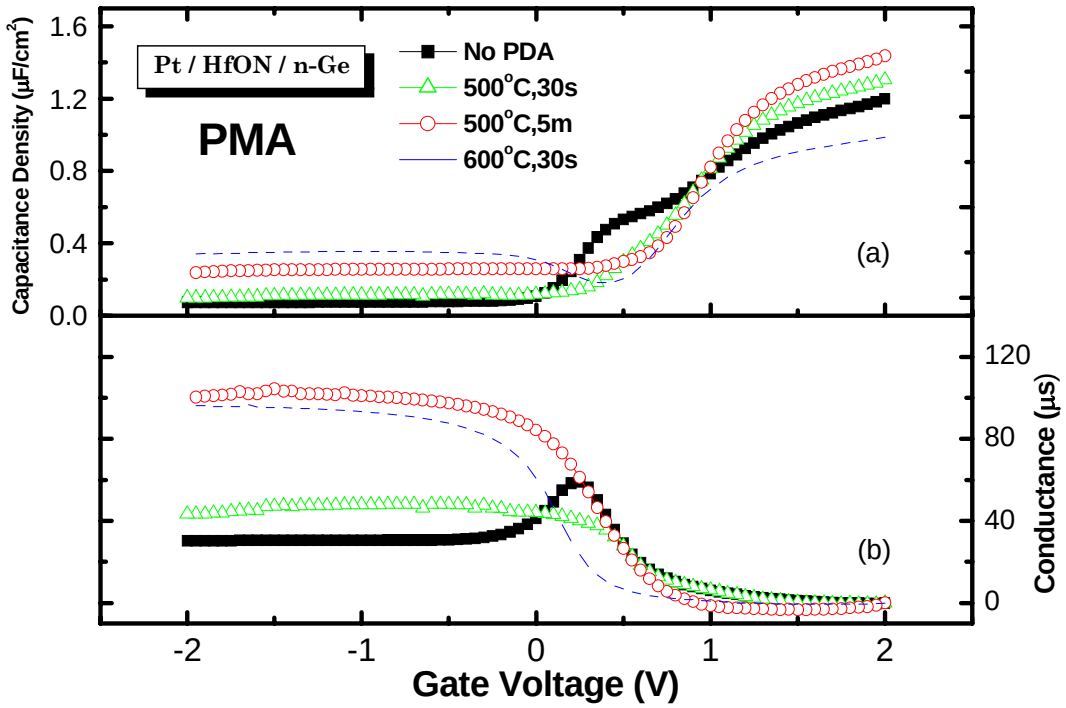


Fig. 3-3 Typical 100-kHz (a) C–V and (b) G–V curves of Pt/HfO_xN_y/n-Ge capacitors before and after PMA, respectively.

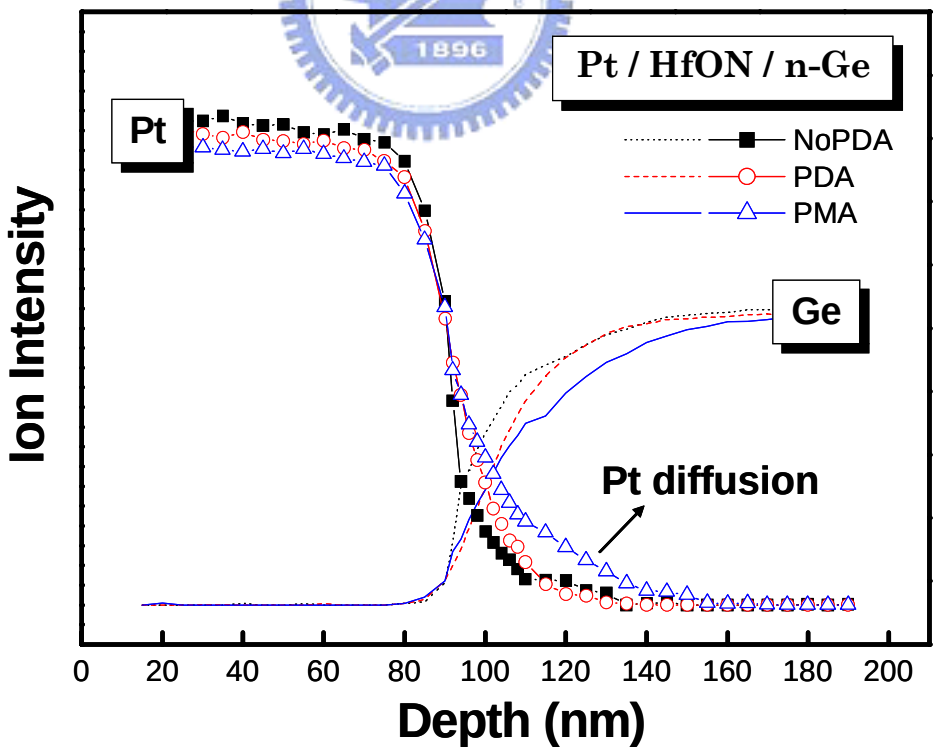


Fig. 3-4 The Auger depth profile of the Pt/HfO_xN_y/n-Ge gate stacks.

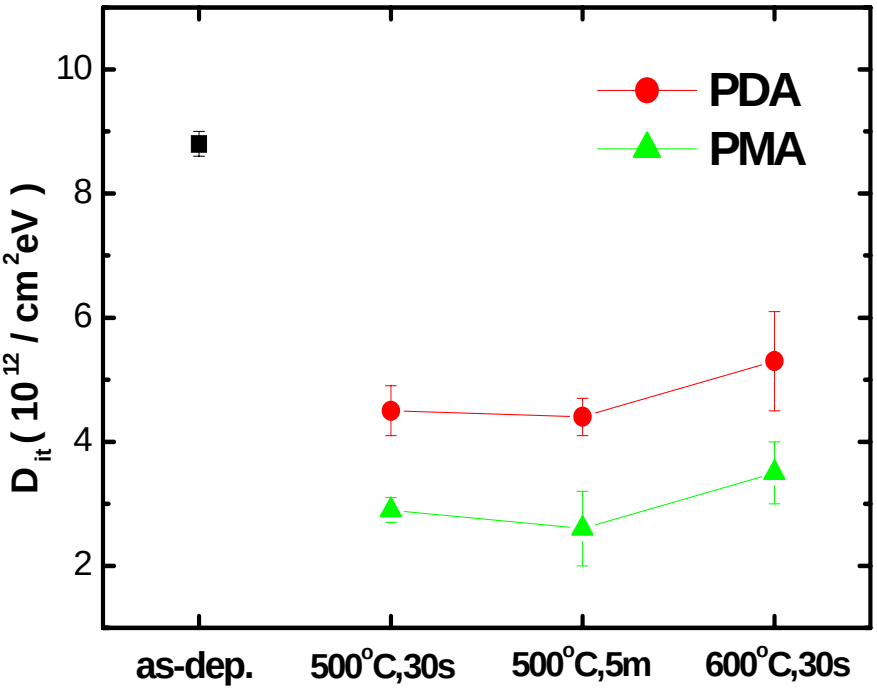


Fig. 3-5 The D_{it} of as-deposited Pt/high-k/Ge capacitors and annealed ones.

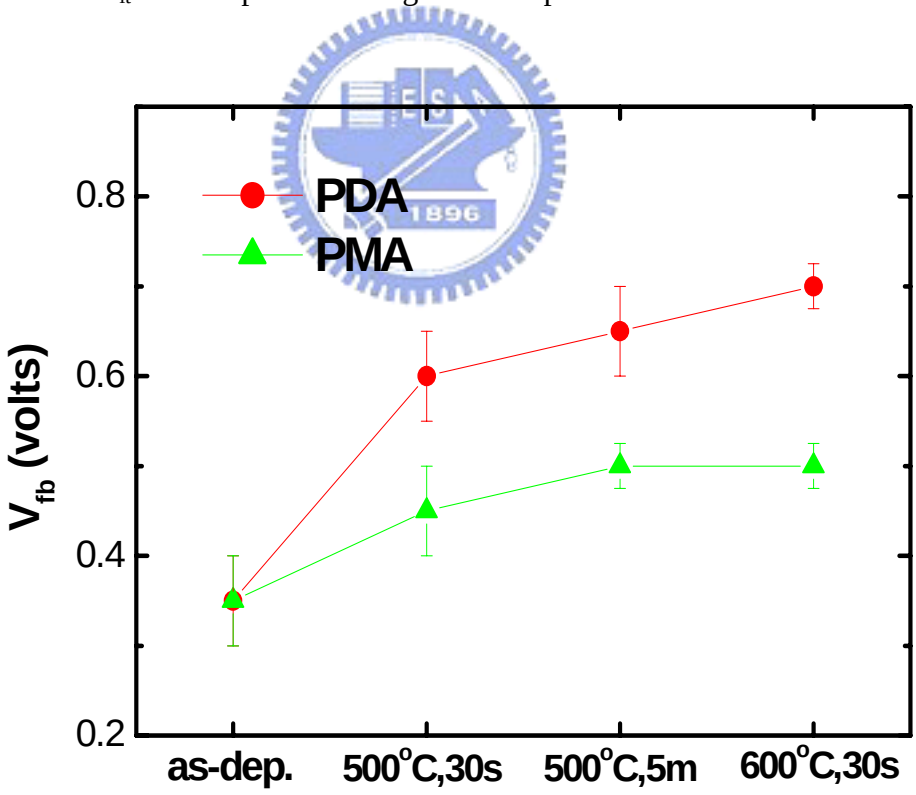


Fig. 3-6 The flat-band voltage of Pt/high-k/Ge capacitors for as-deposited and annealed ones.

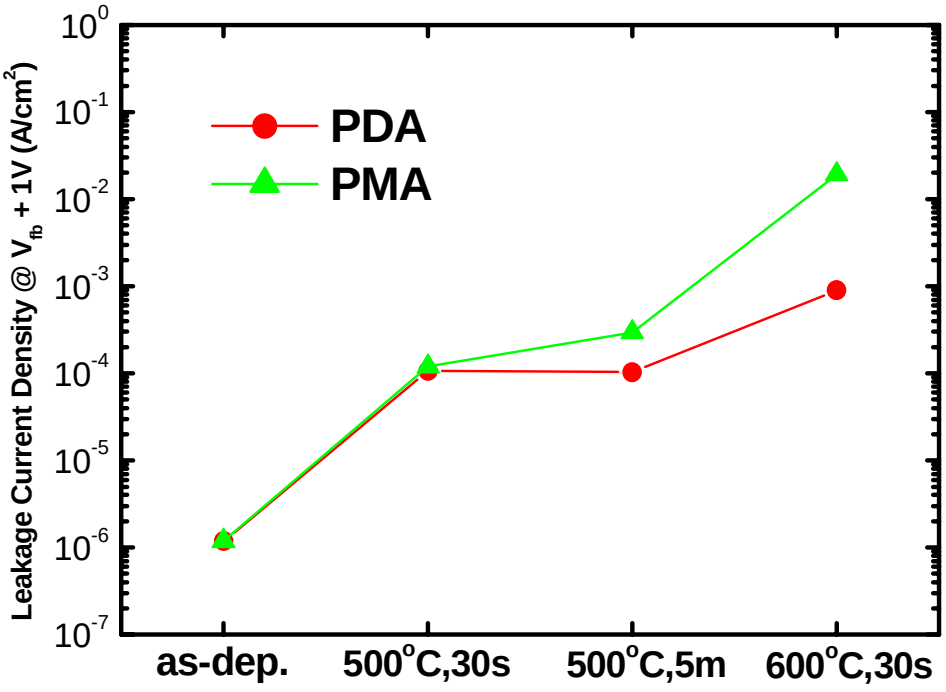


Fig. 3-7 The gate leakage current density of Pt/high-k/Ge capacitors for as-deposited and annealed ones.

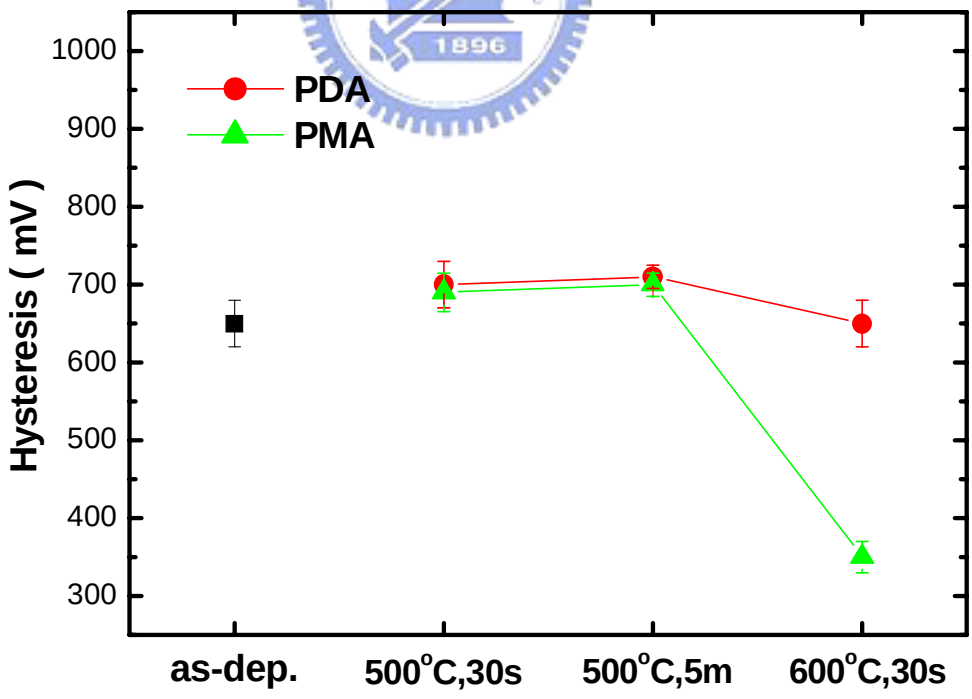


Fig. 3-8 The hysteresis of as-deposited Pt/high-k/Ge capacitors and annealed ones.

Chapter 4
CF_4 and NH_3 Plasma Pretreatment

4-1 Introduction

Ge has recently retrieved enormous attentions due to its higher hole and electron mobility than Si (4x for hole and 2x for electron). Unfortunately, GeO_2 and GeO are thermodynamically unstable and soluble to water, which retard the development of high-performance Ge-MOSFET. Therefore, looking for high-k materials such as HfO_2 or ZrO_2 to be substitute gate dielectric is in demand. The incorporation of N into both HfO_2 and ZrO_2 has attracted considerable interest because of its several improved features addressing those issues facing binary HfO_2, especially for the increase of crystallization temperature and the suppression of defect states caused by the oxygen vacancies in HfO_2 film. Moreover, HfO_xN_y and ZrO_xN_y seem to be promising for further scaling-down of EOT since incorporated nitrogen strengthen the immunity against oxygen diffusion as well as boron penetration without lowering the dielectric constant. However, it was reported that before or during the post-process, the Ge surface would be oxidized to form GeO_x and lead to the degradation of device performance [47-48]. The methods to reduce those excessive GeO_x growths and improve the electrical performance are the purpose of this chapter, which included CF_4 plasma and NH_3 plasma surface pretreatments.

4-2 Experimental Procedures

MOS capacitors were fabricated on (100) oriented n-type Ge substrates which were doped with Sb having a resistivity of 8–12 Ω·cm. Deionized (DI) water rinse followed by diluted HF acid solution dipping for three cycles. After clean process, CF_4 or NH_3 plasma was demonstrated on Ge surface in plasma-enhanced chemical vapor deposition (PECVD). Subsequently, HfO_xN_y or ZrO_xN_y thin films were first deposited through reactive sputtering in an $Ar+N_2$ [$N_2/Ar+N_2$=0.33] ambient with pure Hf or Zr target and the sputtering power was 150 W at the chamber pressure of 7.6 mTorr, and then annealing in N_2 gas with residual oxygen. Next, a 1000 Å layer of platinum (Pt) dot was deposited using electron beam evaporation through a shadow mask, subsequently, annealing in N_2 gas with residual oxygen at 400°C for 30 sec to make the densification of our metal gate. Finally, Al was deposited on the backside of Ge wafer to reduce the contact and series resistances. For comparison, the Si substrate was also demonstrated by same processes.

The capacitance–voltage (C–V) and conductance–voltage (G–V) curves were measured using an HP4284 LCR meter, while the current–voltage (I–V) characteristics were measured using a Keithley 4200 semiconductor analyzer system. We analyzed the effect of NH_3 plasma pretreatment on the chemical configuration by ex-situ XPS using an Al Kα source (1486.6 eV). We also employed atomic force microscopy (AFM) to characterize the surface morphology of CF_4 plasma samples.

4-3 Results and Discussion

4-3-1 The hysteresis of Pt/ZrO_xN_y/Ge gate stack

Figure 4-1 displays the typical 1-MHz C–V curves of Pt/ZrO_xN_y/n-Ge capacitor without any surface pretreatment, which exhibits ca. 650 mV of hysteresis width. In contrast with Pt/ZrO_xN_y/n-Si capacitor shown in figure 4-2, the negligible hysteresis is only ca. 50mV, and the frequency dispersion effect of Pt/ZrO_xN_y/Si gate stack is very slight. It stands to reason that the issues of hysteresis and frequency dispersion existed in the Pt/ZrO_xN_y/n-Ge gate stack have no relationship with our ZrO_xN_y gate dielectric and Pt metal gate.

In order to discover the origin of hysteresis of Pt/ZrO_xN_y/n-Ge capacitor, first, we fastened down the gate bias (V_g) at 0 V in inversion region and then swept from 0 V to different accumulation bias (1 V, 1.2 V, 1.4 V, 1.6 V, 1.8 V and 2 V, respectively). Oppositely, we fastened down the V_g at 1 V in accumulation region and swept from 1 V to different inversion bias (0 V, -1.2 V, -1.4 V, -1.6 V, -1.8 V and -2 V, respectively). All these results are shown in figure 4-3. Obviously, the sweep direction from V_g = +1 V to strong inversion resulted in the presence of hysteresis effect, whereas the sweep direction from V_g = 0 V to strong accumulation did not. Consequently, the hysteresis of Pt/ZrO_xN_y/Ge capacitor might result from the hole trapping effect and corresponding trapping mechanism was deduced in figure 4-4 and figure 4-5. When the capacitor was biased at strong inversion, the holes near valence band of Ge substrate tunneled from Ge surface to interfacial layer and

trapped at the inner-interface. On the other hand, when the capacitor was biased at strong accumulation, the electrons near conduction band of Ge substrate tunneled through the interfacial layer and gate dielectric ZrO_xN_y without being trapped at the inner-interface, thus contributing to the gate leakage current.

Figure 4-6 shows the gate leakage current of $Pt/ZrO_xN_y/Ge$ capacitor, the flat-band voltage is ca. 0.35 V with respect to the C-V curve (dashed line), the gate leakage current density is ca. 9×10^{-7} A·cm^{-2} and ca. 1×10^{-5} A·cm^{-2} at V_{fb} - 1 V and V_{fb} + 1 V, respectively. Apparently, the gate leakage current at strong accumulation condition is greater than the leakage current at strong inversion condition, which is coincided with the result of energy-band diagrams in figure 4-4 and figure 4-5.

4-3-2 CF_4 plasma pretreatment

Figure 4-7 displays the 1-MHz C–V curves of Pt/ZrO_xN_y/n-Ge capacitors with and without CF_4 plasma pretreatment. After CF_4 plasma pretreatment, the hysteresis width of Pt/ZrO_xN_y/n-Ge capacitors increased from 650 mV to 950 mV, whereas the 3 watt CF_4 plasma was ineffective to Pt/ZrO_xN_y/n-Si gate stack. As shown in figure 4-8, the C-V curves of Pt/ZrO_xN_y/n-Si capacitors remained identical whatever CF_4 plasma was demonstrated or not, which indicated that the power of CF_4 plasma was too small to react with Si surface. It also resulted in the consequences of gate leakage current in figure 4-9, the gate leakage current

density at V_{fb} + 1 V of Pt/ZrO_xN_y/Si capacitors was all ca. 10^{-6} A·cm^{-2} for 0 watt, 2 watt and 3 watt CF_4 plasma pretreatment. In contrast with Pt/ZrO_xN_y/Ge gate stacks, the gate leakage current increased with the uplifting CF_4 plasma power.

The enlargement of hysteresis phenomnomn after CF_4 plasma pretreatment was examined by the previous method we used; figure 4-10 demonstrated the 1-MHz C–V curves of Pt/ZrO_xN_y/n-Ge capacitor with CF_4 plasma treatment. First, we swept the gate bias from 0 V to 1 V, 1.2 V, 1.4 V, 1.6 V, 1.8 V and 2 V, respectively. And then the gate bias was swept from 1 V to 0 V, -1.2 V, -1.4 V, -1.6 V, -1.8 V and -2 V, respectively. Interestingly, the curves of sweep direction from V_g = 0 V to strong accumulation region began to shift positively and curves of sweep direction from V_g = 1 V to strong inversion region moved even more manifestly, which implied that CF_4 plasma pretreatment induced trapping centers not only near conduction band but also valence band of Ge.

Figure 4-11 shows the AFM images of Ge substrates before and after CF_4 plasma pretreatment, the room-mean-square (RMS) surface roughness is increased from 0.35 nm to 0.46 nm, which probably incurred the larger gate leakage current of Pt/ZrO_xN_y/n-Ge capacitors in figure 4-9. However, 3 watt CF_4 plasma was ineffectual to change the surface morphology of Si substrate, as shown in figure 4-12.

4-3-3 NH_3 plasma pretreatment

High-frequency (1-MHz) C–V curves of Pt/HfO_xN_y/n-Ge capacitors with and without NH_3 plasma pretreatment was shown in figure 4-13. After NH_3 plasma pretreatment, the hysteresis width of Pt/HfO_xN_y/n-Ge capacitors was reduced from 650 mV to 400 mV. On the contrary, the hysteresis width of Pt/HfO_xN_y/n-Si capacitors remained ca. 30 mV, which was independent of applied NH_3 plasma, implying that the power of NH_3 plasma was not enough to nitride the Si surface.

Figure 4-15 (a) and (b) show the core-level spectra of Ge 2*p* and Ge 3*p* for the HfO_xN_y/n-Ge gate stacks. Manifestly, NH_3 plasma pretreatment suppressed the growth of GeO_x, which restrained the electrons and holes from trapping at HfO_xN_y/IL interface and diminished the hysteresis width of Pt/HfO_xN_y/n-Ge capacitors.

As we discussed in chapter 2 and chapter 3, the volatilization of GeO would damage the gate dielectric and generate leakage-paths in it especially after high-temperature annealing. However, the NH_3 pretreatment samples reduced the gate leakage current by two orders of magnitude after PDA at 600°C for 30 sec, as shown in figure 4-16, which was attributed to the nitrided-surface and leading to a small amount of GeO volatilization.

Figure 4-17 displays the D_{it} of as-deposited Pt/high-k/Ge capacitors before and after surface pretreatment, the D_{it} was determined from G–V characteristics at the frequency of 500-kHz by using Hill's method. The CF_4 plasma pretreatment enlarged the hysteresis width

indicated an increment in charge traps possible at the interface of high-k/IL. On the other hand, the NH_3 plasma pretreatment compressed the hysteresis width implied a reduction in charge traps at the interface of high-k/IL, which was likely related to less native oxide of nitrided samples.

4-4 Summary

In this chapter, we found that the hysteresis of both Pt/ZrO_xN_y/n-Ge and Pt/HfO_xN_y/n-Ge (not shown) capacitors was due to the trapping centers at high-k/IL interface near the valence band of Ge. The CF_4 plasma pretreatment enlarged the gate leakage current and hysteresis width of Pt/high-k/Ge capacitors, which were possibly due to damage Ge surface and the increment of D_{it}. On the other hand, the NH_3 plasma pretreatment compressed the hysteresis width, which was likely related with less GeO_x and D_{it}. Moreover, the nitridation process improved the thermal stability of Pt/high-k/Ge capacitors by restraining the formation of GeO_x and their volatilization.

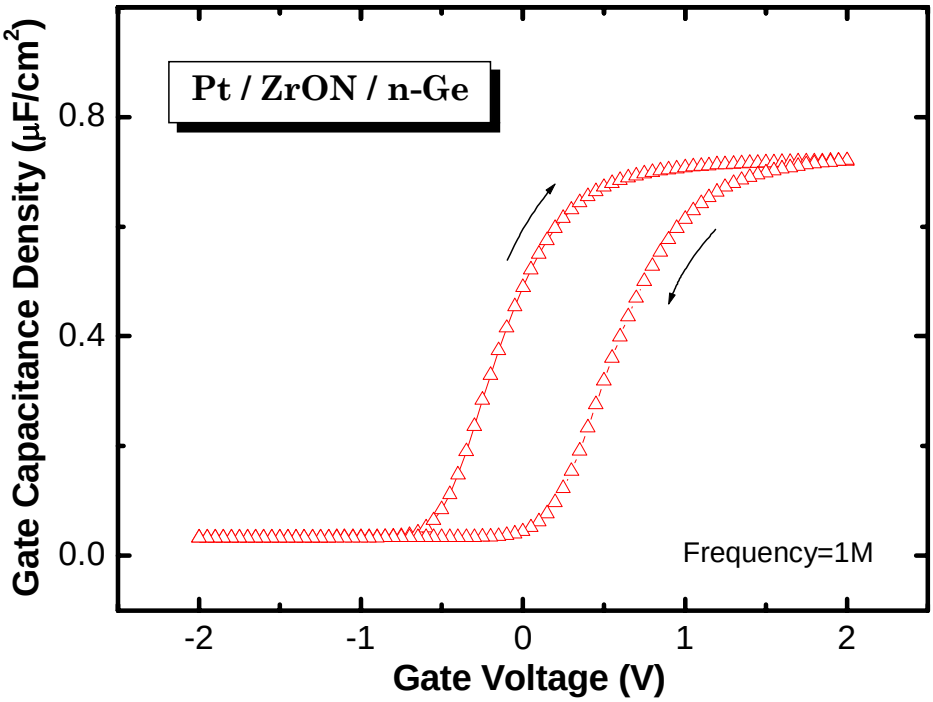


Fig. 4-1 Typical 1-MHz C–V curves of Pt/ZrO_xN_y/n-Ge capacitor without any surface pretreatment.

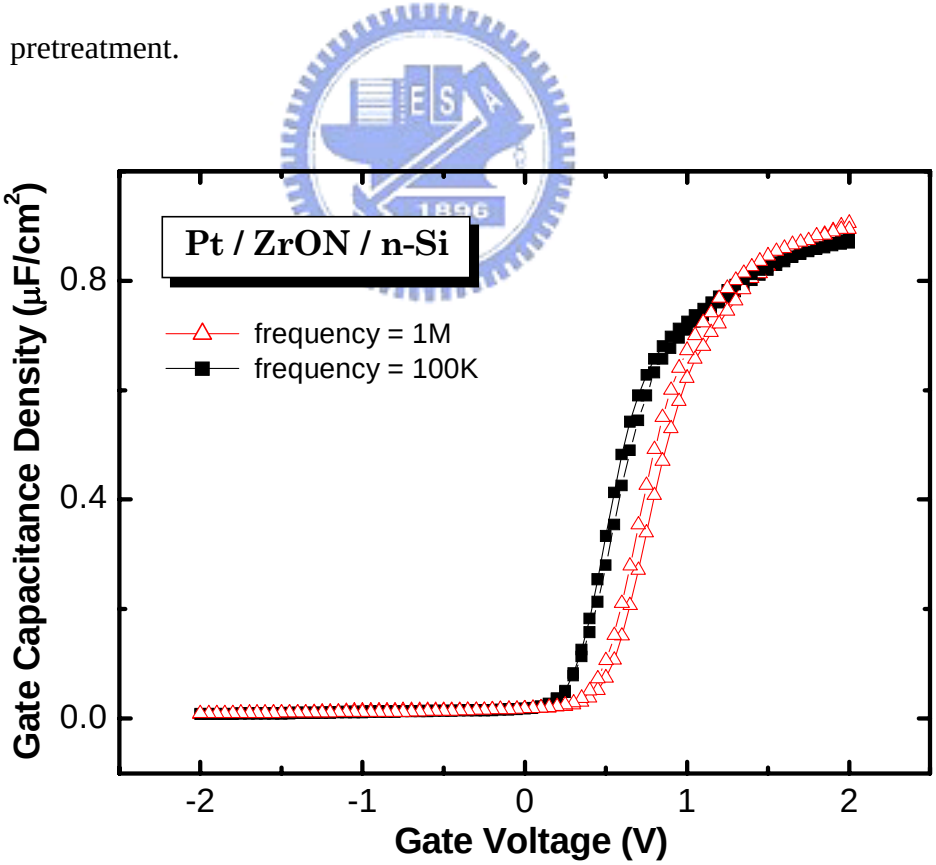


Fig. 4-2 Typical 1-MHz and 100-kHz C–V curves of Pt/ZrO_xN_y/n-Si capacitor without any surface pretreatment.

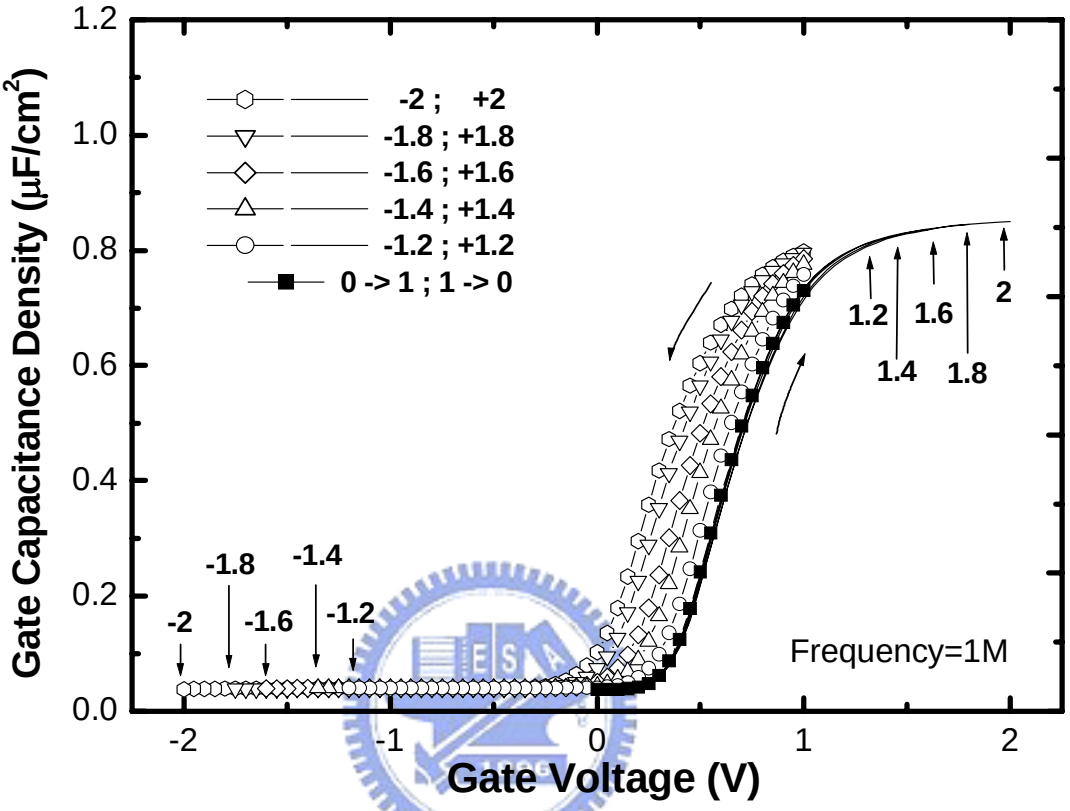


Fig. 4-3 The 1-MHz C–V curves of $Pt/ZrO_xN_y/n$-Ge capacitor (solid lines refer to the sweep-voltage from 0 V to 1 V, 1.2 V, 1.4 V, 1.6 V, 1.8 V, 2 V, respectively**;** symbol lines refer to the sweep-voltage from 1 V to 0 V, -1.2 V, -1.4 V, -1.6 V, -1.8 V, -2 V, respectively).

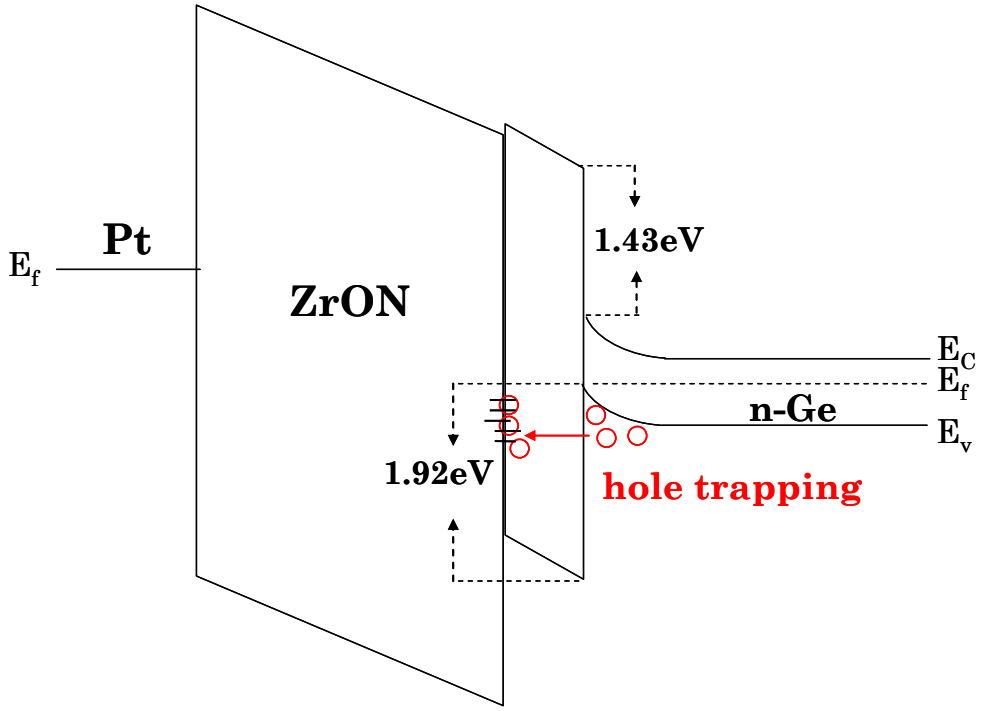


Fig. 4-4 Energy-band diagram of ZrO_xN_y/IL/n-Ge gate stack with Pt metal gate electrode under the inversion condition.

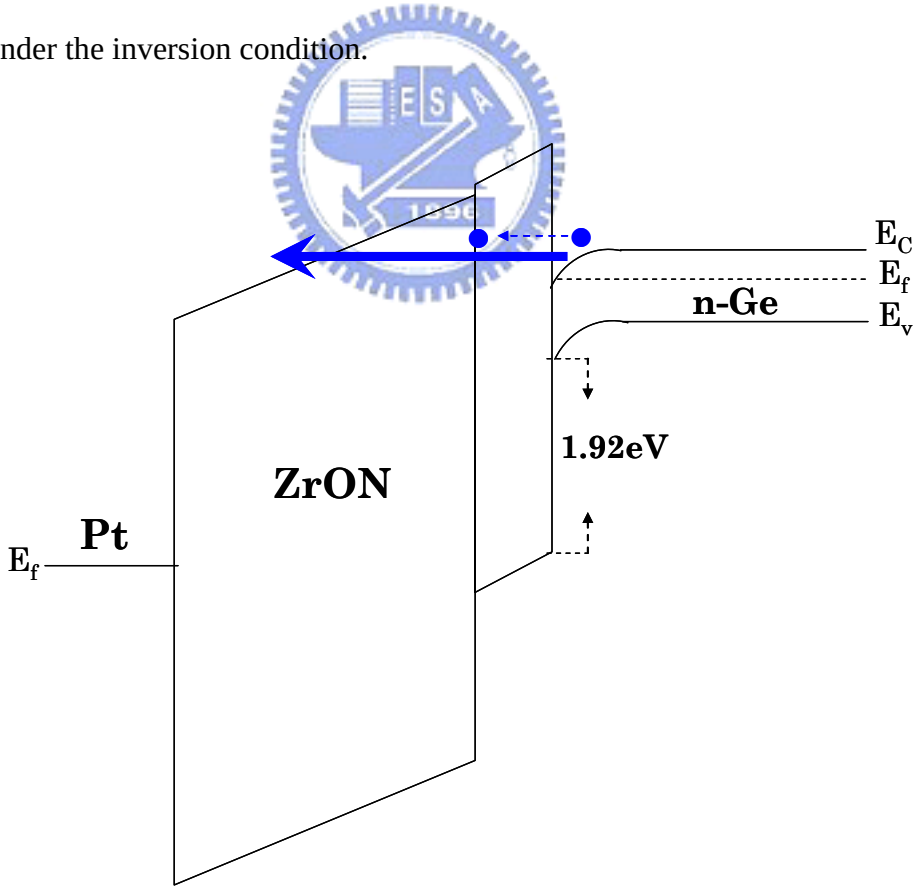


Fig. 4-5 Energy-band diagram of ZrO_xN_y/IL/n-Ge gate stack with Pt metal gate electrode under the accumulation condition.

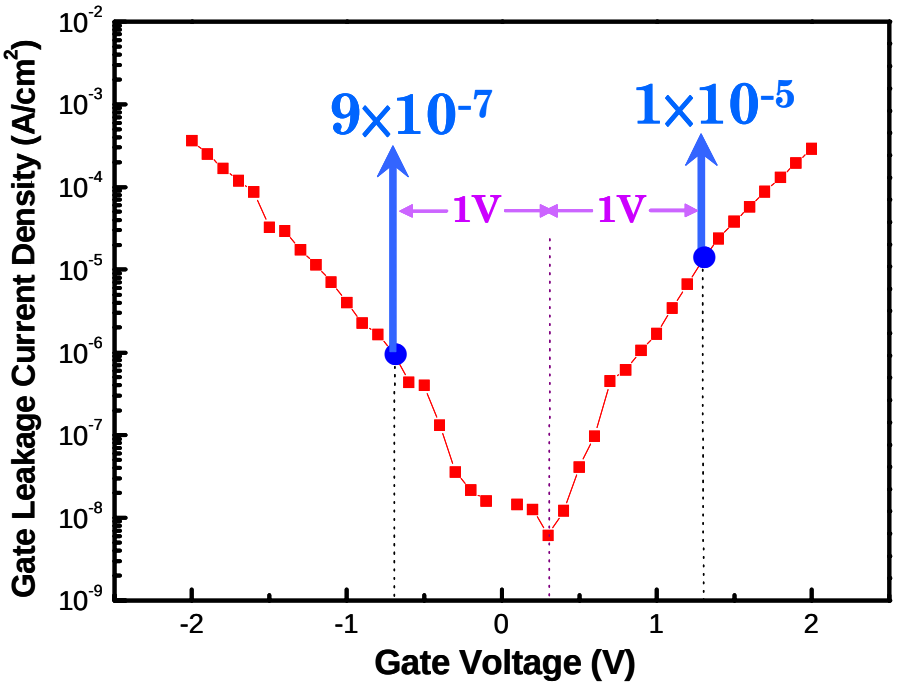


Fig. 4-6 I-V characteristics of $Pt/ZrO_xN_y/n\text{-}Ge$ gate stack (the leakage current density is ca. 9 x 10^{-7} A·cm^{-2} and ca. 1 x 10^{-5} A·cm^{-2} at V_{fb} - 1 V and V_{fb}+ 1 V, respectively).

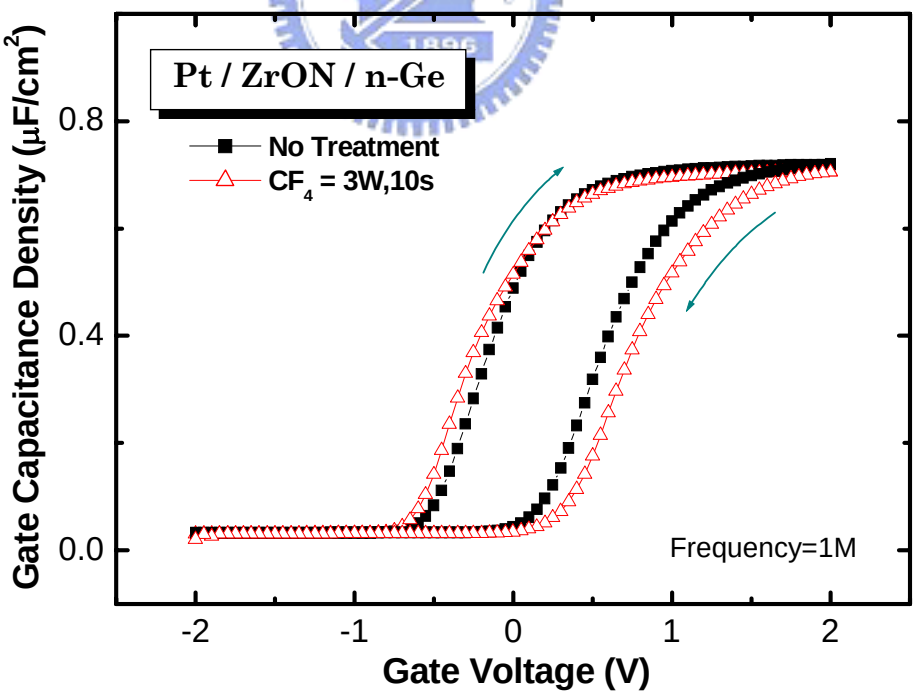


Fig. 4-7 C–V curves of $Pt/ZrO_xN_y/n\text{-}Ge$ capacitors with (open symbol) and without (solid symbol) CF_4 plasma pretreatment.

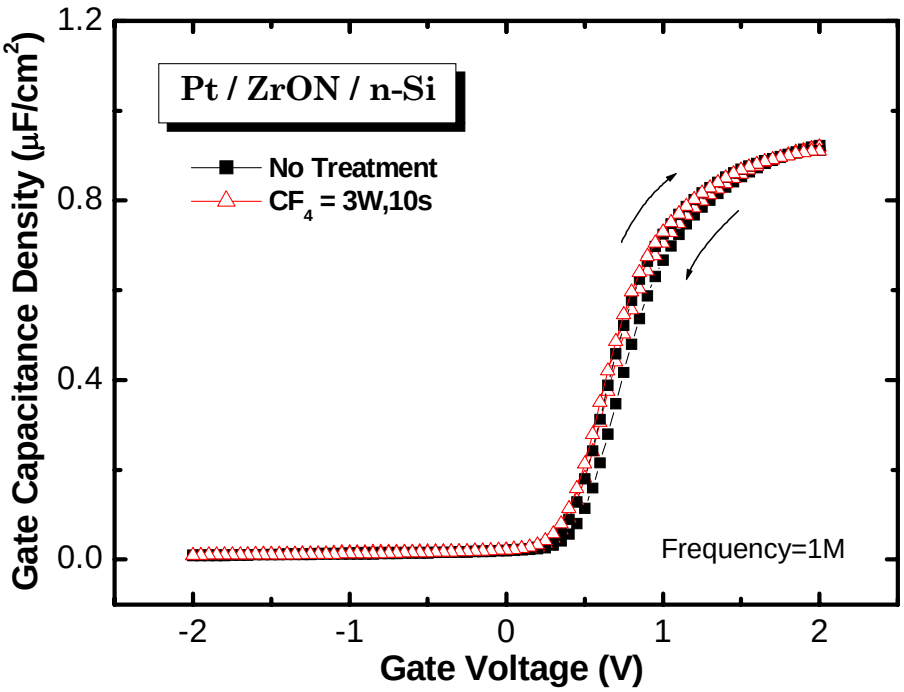


Fig. 4-8 C–V curves of Pt/ZrO_xN_y/n-Si capacitors with (open symbol) and without (solid symbol) CF_4 plasma pretreatment.

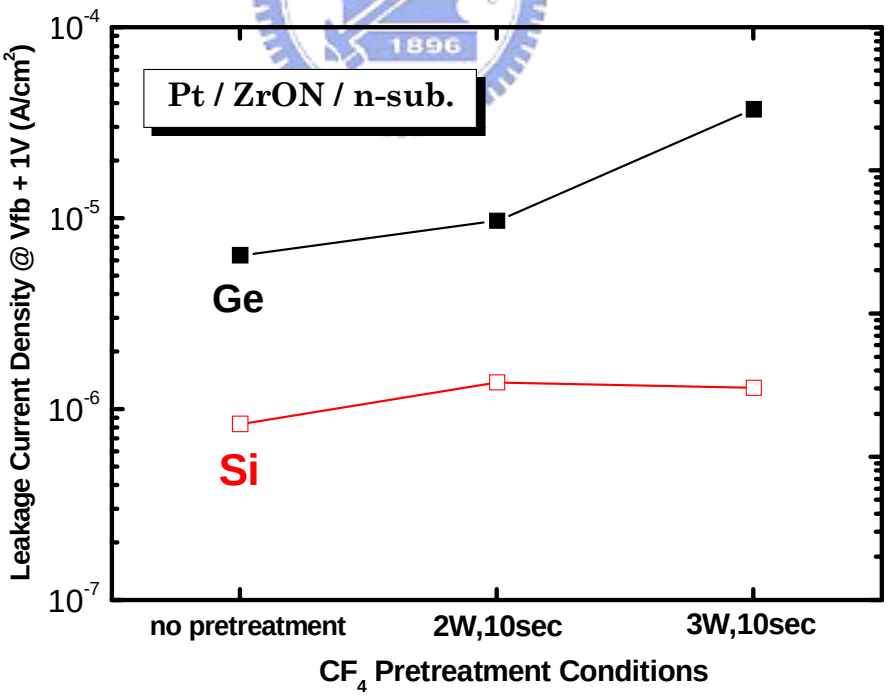


Fig. 4-9 The gate leakage current density at V_{fb} + 1 V of Pt/ZrO_xN_y/n-sub capacitors (open symbol for Si substrate; solid symbol for Ge substrate).

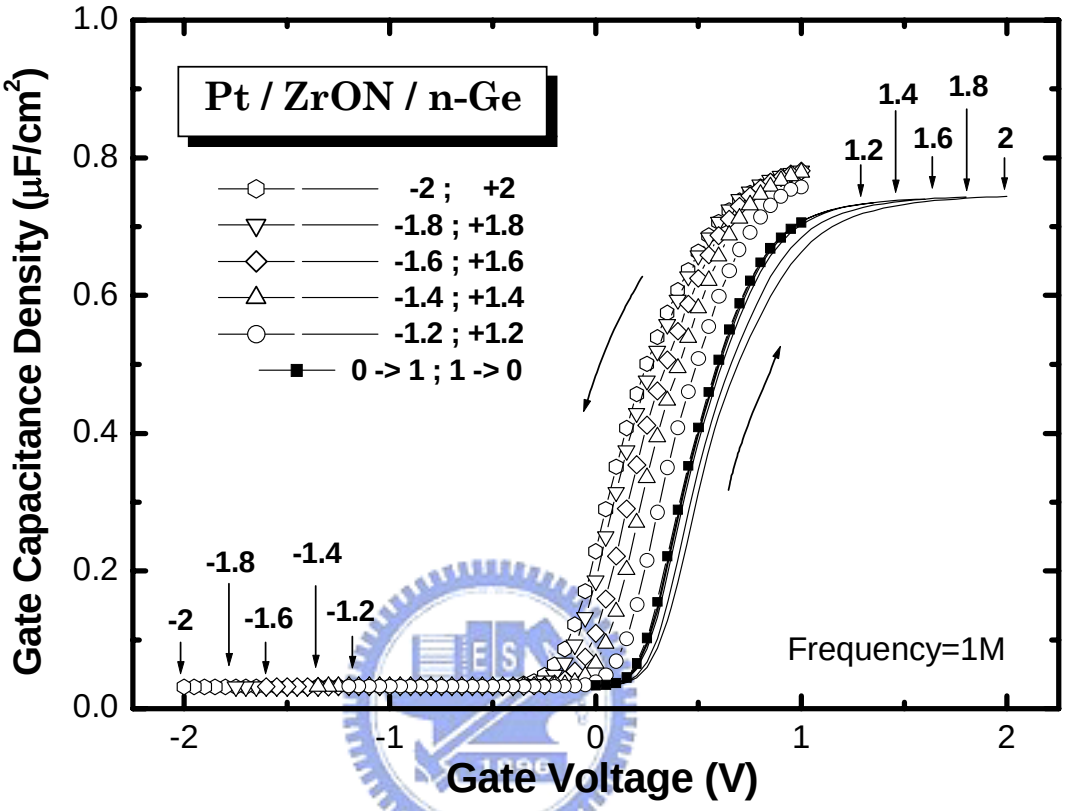
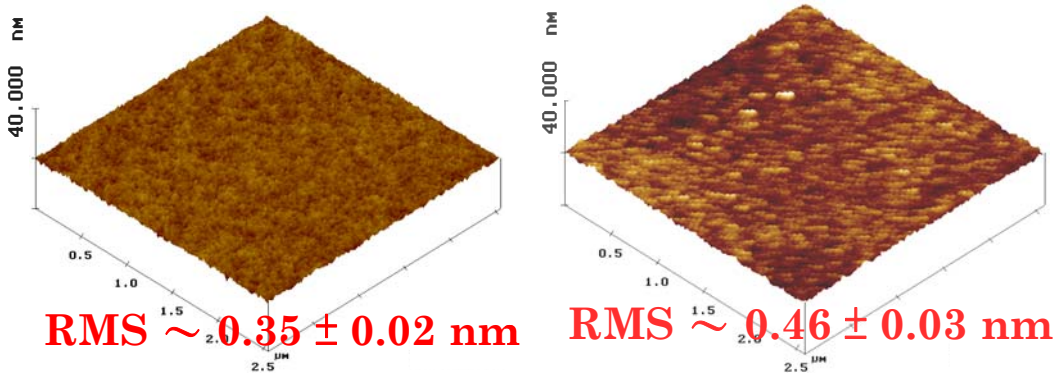
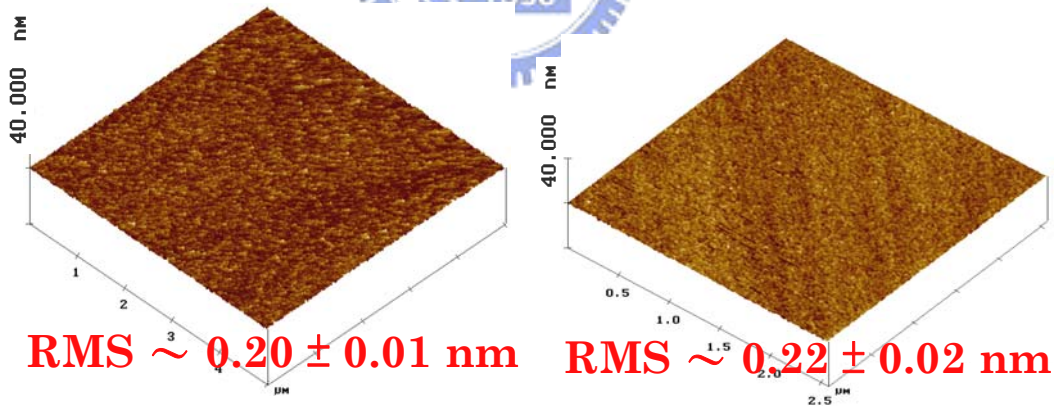


Fig. 4-10 The 1-MHz C–V curves of $Pt/ZrO_xN_y/n$-Ge capacitor with CF_4 plasma pretreatment (solid lines refer to the sweep-voltage from 0 V to 1 V, 1.2 V, 1.4 V, 1.6 V, 1.8 V, 2 V, respectively; symbol lines refer to the sweep-voltage from 1 V to 0 V, -1.2 V, -1.4 V, -1.6 V, -1.8 V, -2 V, respectively).



（a）　　（b）

Fig. 4-11　The AFM images of Ge substrate （a）before CF_4 plasma pretreatment and （b）after CF_4 plasma pretreatment.



（a）　　（b）

Fig. 4-12　The AFM images of Si substrate （a）before CF_4 plasma pretreatment and （b）after CF_4 plasma pretreatment.

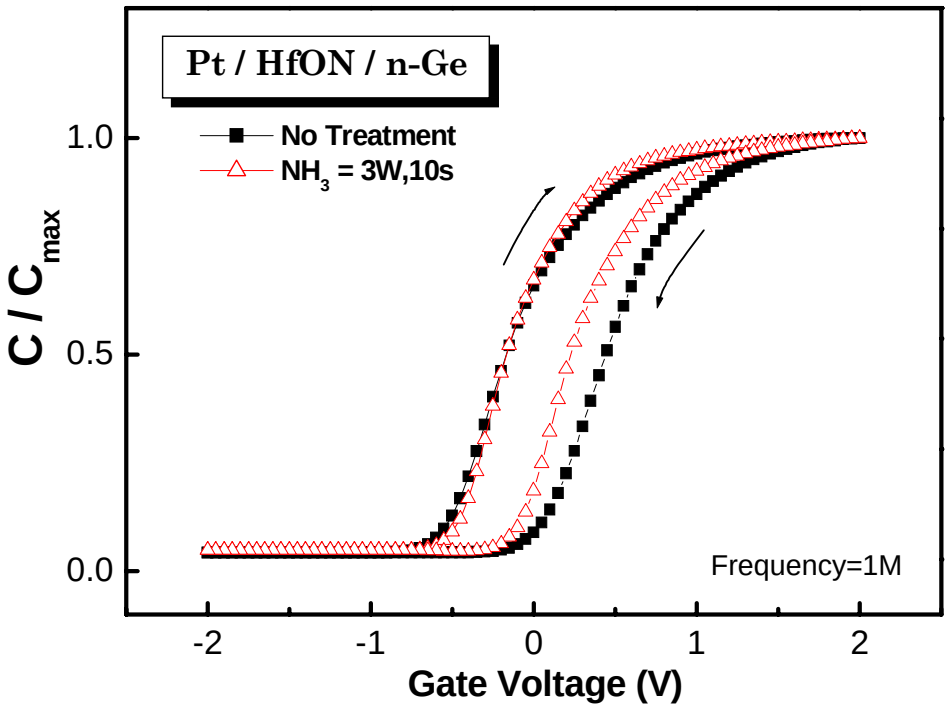


Fig. 4-13 Normalized C–V curves of Pt/HfO_xN_y/n-Ge capacitors with (open symbol) and without (solid symbol) NH_3 plasma pretreatment.

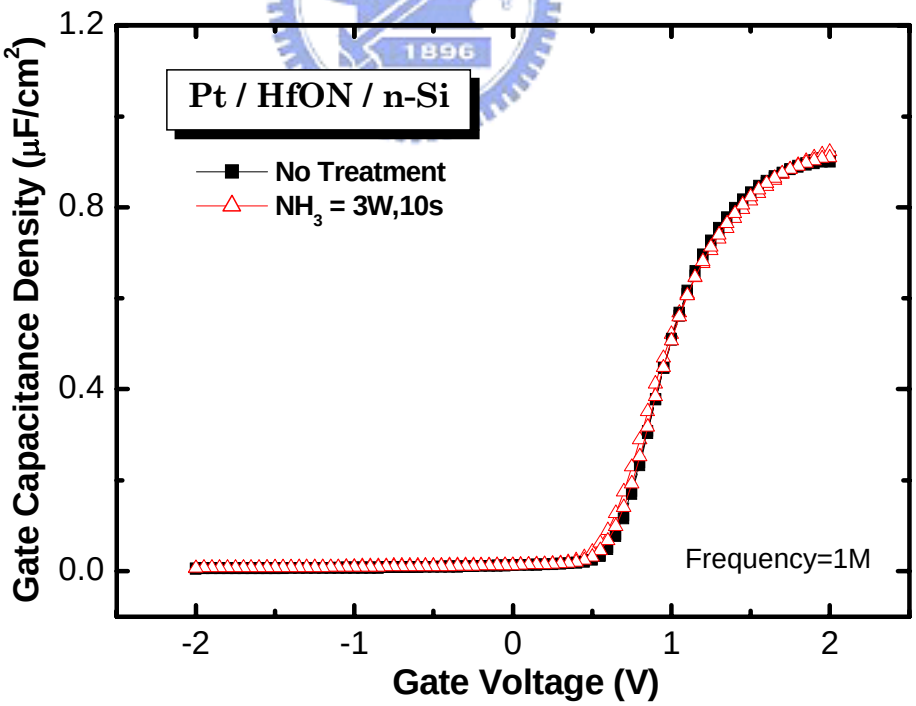
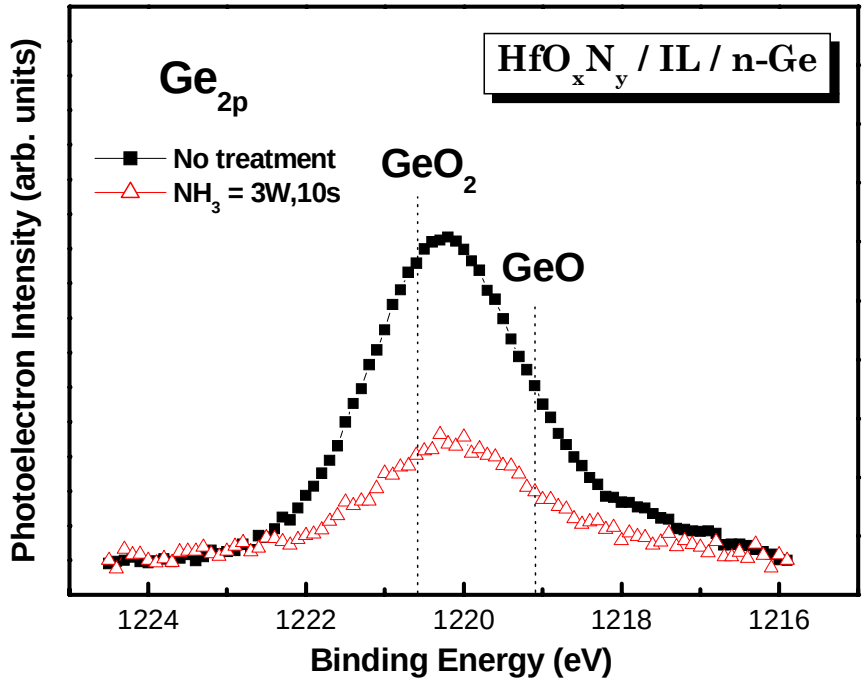
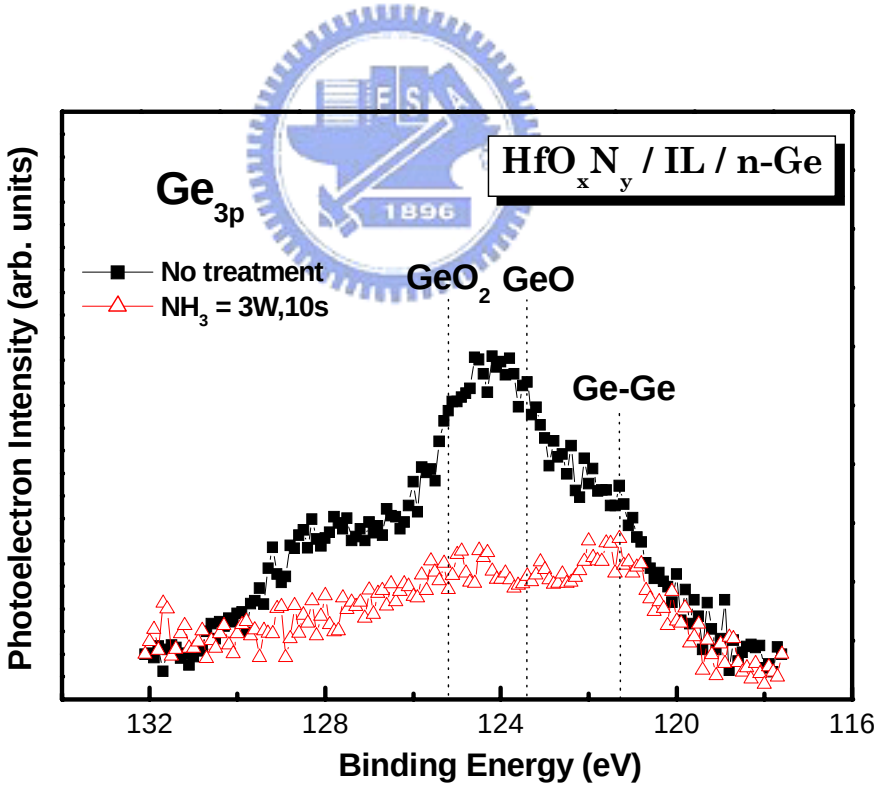


Fig. 4-14 C–V curves of Pt/HfO_xN_y/n-Si capacitors with (open symbol) and without (solid symbol) NH_3 plasma pretreatment.



（a）



（b）

Fig. 4-15 （a）Ge 2*p* and （b）Ge 3*p* core-level spectra of HfO_xN_y thin films on Ge substrates before and after NH_3 plasma pretreatment.

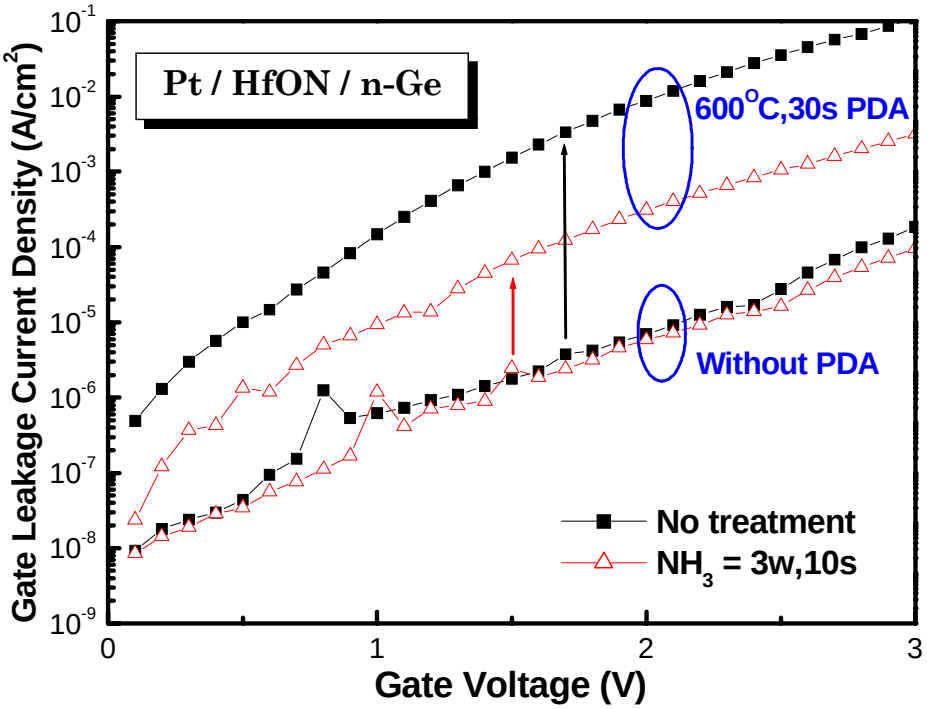


Fig. 4-16 I-V characteristics of $Pt/HfO_xN_y/n\text{-}Ge$ gate stack with (open symbol) and without (solid symbol) NH_3 plasma pretreatment.

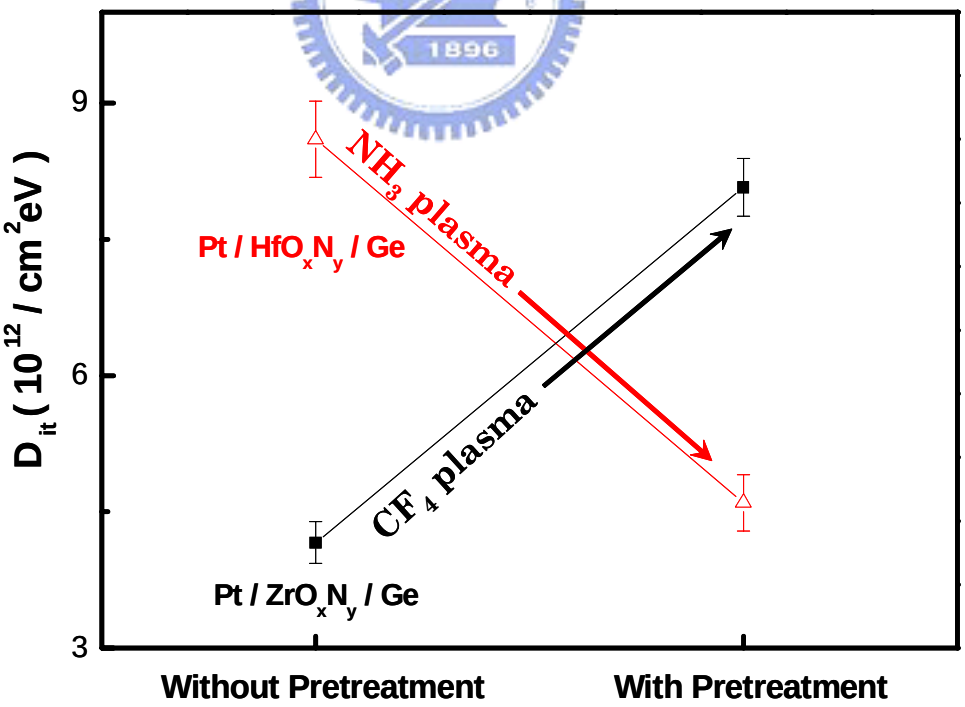


Fig. 4-17 The D_{it} of as-deposited Pt/high-k/Ge capacitors before and after pretreatments.

Chapter 5
UHVCVD Si_2H_6 Passivation

5-1 Introduction

For the past several decades, improvement of transistor performance has been principally accomplished by scaling the transistor dimensions resulting in a higher circuit speed, larger packing density and less power consumption. But, with further downscaling device dimensions and the shrinkage of gate oxide thickness to nanometer range, the leakage current density of SiO_2 is too large to be accepted. As an alternative to the scaling approach, enhancing the channel carrier mobility can promote the driving capability, which has recently led to a renewed interest in Ge because of its higher intrinsically carrier mobility [49-50]. However, Ge oxide is thermodynamically unstable and soluble to water, which retards the development of high-performance Ge-MOSFET. On the other hand, important progress has been made in the field of thin-film depositions, especially the substitute gate dielectric of high-k materials, which could enable the implementation of Ge in combination with a high-k dielectric.

NH_3 surface pretreatment had been applied on high-k/Ge system in chapter 4, which improved the electrical properties by suppressing the growth of GeO_x, but nitrogen incorporation may not be sufficient to fully passivate the dangling bonds on Ge surface and

prevent the growth of GeO_x. In this chapter, we demonstrate the Si_2H_6 passivation on Ge surface, which is expected to prohibit the growth of GeO_x by forming several monolayers of Si between gate dielectric and Ge substrate.

5-2 Experimental Procedures

MOS capacitors were fabricated on (100) oriented n-type Ge substrates which were doped with Sb having a resistivity of 8–12 Ω·cm. First, thermal desorption at 550°C for 10 min was demonstrated on Ge substrate, which was expected to remove native GeO_x on Ge surface, and then in-situ Si_2H_6 passivated in ultra high vacuum chemical vapor deposition (UHVCVD). After Si interlayer passivation on Ge substrate, DI water rinse followed by diluted HF acid solution dipping for one cycle in order to remove Si native oxide. Subsequently, HfO_xN_y or ZrO_xN_y thin films were first deposited through reactive sputtering in an $Ar+N_2$ [$N_2/Ar+N_2$=0.33] ambient with pure Hf or Zr target and the sputtering power was 150 W at the chamber pressure of 7.6 mTorr, and then annealing in N_2 gas with residual oxygen. Next, a 1000 Å layer of platinum (Pt) dot was deposited using electron beam evaporation through a shadow mask, subsequently, annealing in N_2 gas with residual oxygen at 400°C for 30 sec to make the densification of our metal gate. Finally, Al was deposited on the backside of Ge wafer to reduce the contact and series resistances. For comparison, the Si substrate was also demonstrated by same processes.

The capacitance–voltage (C–V) and conductance–voltage (G–V) curves were measured using an HP4284 LCR meter, while the current–voltage (I–V) characteristics were measured using a Keithley 4200 semiconductor analyzer system. We analyzed the effect of Si interlayer on the chemical configuration by ex-situ XPS using an Al Kα source (1486.6 eV). We also employed secondary ion mass spectroscopy (SIMS) to characterize the effect of Si_2H_6 passivation.

5-3 Results and Discussion

5-3-1 The properties and estimated thickness of Si interlayer

After Si passivation on Ge substrate, we removed Si native oxide by HF dipping for 30 sec, and immediately loaded into XPS analyzed system to examine their surface chemistry, as presented in figure 5-1 (a) to (c). Taking the use of Si 2*p*, Ge 2*p* and Ge 3*d* core-level spectra, the thickness of Si cap-layer was calculated using the following formulas [51-52]:

$$I_{2p} = I_{2p}^{\infty} e^{\frac{-d}{\lambda_{2p}\sin\theta}} \quad (5.1), \qquad I_{3d} = I_{3d}^{\infty} e^{\frac{-d}{\lambda_{3d}\sin\theta}} \quad (5.2)$$

where λ is the attenuation length, θ is the angle between surface normal and the emission direction (60^{o} in our case), I_{2p} and I_{3d} are the measured intensity of Ge 2*p* and Ge 3*d* core-level spectra, respectively. Based on the assumption of $I^{\infty}_{2p} = I^{\infty}_{3d}$, λ_{2p} and λ_{3d} are equal to 0.9 nm and 3.0 nm respectively [53-54]. Consequently, the thicknesses of Si cap-layer were estimated to be 8.7 Å and 13.0 Å for the Si_2H_6 passivation 1 and 2 min

respectively, which was coincided with the intensity of Si 2*p* spectrum.

The Ge native oxide was vanished after thermal desorption process, as shown in figure 5-1 (b) and (c). The samples without Si_2H_6 passivation displayed a broad profile in Ge 2*p* and Ge 3*d* core-level spectra, suggesting the existence of GeO_x. On the other hand, Si_2H_6 passivation samples only exhibited the Ge substrate peak without the presence of the GeO_x.

5-3-2 Electrical characteristics of Pt/high-k/Si/n-Ge capacitor

In chapter 4, we demonstrated the inner-interface trapping model of Pt/high-k/IL/Ge gate stacks. This trapping mechanism took place in high-k/IL interface, and the IL was referring to GeO_x. Figure 5-2 (a) and (b) are the high-frequency (1-MHz) C–V curves of Pt/HfO_xN_y/n-Ge capacitors with Si_2H_6 passivation for 1 and 2 min, respectively. Apparently, the hysteresis width was greatly compressed because of the absence of GeO_x, especially for the 2 min Si_2H_6 passivation sample, the hysteresis width was ca. 20mV.

The Si_2H_6 passivation was successful in eliminating the hysteresis of Pt/high-k/Ge gate stacks, and it improved the frequency dispersion effect slightly. We estimated this dispersion effect in the accumulation region (V_g = 2V) simply by the following equation:

$$dispersion = \frac{\| C(@100kHz) - C(@1MHz) \|}{C(@100kHz)}\% \qquad (5.3)$$

We obtained a negligible value of 0.4 % for Pt/HfO_xN_y/Si gate stacks, but 39.2 %, 36.5 % and 30.6 % for the Pt/HfO_xN_y/Ge gate stacks of Si_2H_6 passivation 0 min, 1 min and 2 min

respectively, as shown in figure 5-3 and figure 5-4. As far as the frequency dispersion effects of the accumulation capacitance was concerned, the series resistance (R_s) which was related to the bulk wafer resistivity and the contact resistances would be the dominated mechanism; this effect would be amplified with the measured conductance [55]. Although the Ge substrates we used had slightly higher bulk resistivity than that of Si, it only partly explained the dispersion effects. The Si_2H_6 passivation reduced the frequency dispersion effects form 39.2 % to 30.6 %, which indicated that the frequency dispersion in accumulation region was also improved by the better interface quality [56].

On the other hand, we clearly observed the anomalous low-frequency-like behavior of the high-frequency (in the kHz range) C–V curves in inversion for the capacitors on the Ge substrate but not on the Si substrate, which was resulted from the fast rate of minority carrier generation in Ge [57]. It is well known that two major mechanisms are responsible for the build-up of inversion charge, or the so-called generation current density (J_{gen}). The first mechanism is the thermal generation of electron/hole pairs via the trap levels within the space charge region, denoted as J_{scr}, and another mechanism is the diffusion of minority carriers from the bulk substrate across the space charge region, denoted as J_{diff}. Under the strong inversion condition, the following equation describes the relation between J_{scr} and J_{diff} [58].

$$J_{gen} = J_{scr} + J_{diff} = \frac{en_i w}{\tau_t} + \frac{en_i^2}{N_{maj}} \sqrt{\frac{D_{\min}}{\tau_{\min}}} \tag{5.4}$$

where e is the electronic charge, n_i is the intrinsic carrier concentration, w is the width of

space charge region, N_{maj} is the majority carrier concentration, D_{min} is the diffusion coefficient of minority carriers and τ_{min} is the generation lifetime of minority carriers. For Si substrates, J_{scr} is ca. 1×10^{-9} A/cm^2 and J_{diff} is ca. 2×10^{-12} A/cm^2. In comparison, the J_{scr} is ca. 2×10^{-5} A/cm^2 and J_{diff} is ca. 9×10^{-4} A/cm^2 for Ge substrates [40]. As a result of the larger value of n_i, J_{diff} and J_{scr} are drastically increased and consequently J_{gen} is increased by four orders of magnitude of Ge substrate. That is to say, the sufficiently larger value of J_{gen} in Ge leads to the observed minority carrier response in the C-V characteristic.

The measured capacitance and conductance simultaneously rose after Si_2H_6 passivation, as shown in figure 5-5. Similar to the effect in PMA processes, it seemed to be like a typical characteristic of the increment of bulk traps. Besides, the bulky defects with energy levels near midgap in Ge were also responsible for the supply of minority carriers to the inversion layer, incurring the onset of low-frequency-like C–V characteristic.

Figure 5-6 shows the flat-band voltage of Pt/HfO_xN_y/n-sub capacitors for as-deposited and annealed ones. After PDA at 500°C, the V_{fb} of 1 min and 2 min Si_2H_6 passivation samples were increased to ca. 1 V and ca. 1.2 V respectively, implying that positive charges which were introduced during dielectric deposition had been remedied by high temperature annealing as what we discussed in chapter 3.

The elimination of GeO_x in the HfO_xN_y/Ge interface avoided the leakage-paths caused by the volatilization of GeO. Figure 5-7 displays the leakage current density of

Pt/HfO_xN_y/n-sub capacitors for as-deposited and annealed ones, the gate leakage current of 1 min Si_2H_6 passivation sample did not apparently increased with the high annealing temperature with respect to non-passivation sample. Nevertheless, the sample with Si_2H_6 passivation for 2 min might induce large stress and dislocations in Ge substrate, hence resulting in large gate leakage current. The comparison of gate leakage current density versus the CET of Pt/HfO_xN_y/n-sub capacitors was shown in figure 5-8, after PDA at 500°C, the Si interlayer had transferred to SiO_x which resulted in the increment of CET for Si_2H_6 passivation samples.

On the other hand, we also replaced gate dielectric HfO_xN_y with ZrO_xN_y, figure 5-9 demonstrates the hysteresis of Pt/HfO_xN_y/n-sub capacitors and Pt/ZrO_xN_y/n-sub capacitors. Obviously, the hysteresis width was greatly compressed after Si_2H_6 passivation process independent of the gate dielectric we deposited, which confirmed our inner-interface trapping model in chapter 3 again. Figure 5-10 displays the gate leakage current density versus the CET of Pt/ZrO_xN_y/n-sub capacitors, and similar tendency could be concluded.

5-3-3 Physical properties of Pt/high-k/Si/n-Ge capacitor

Figure 5-11 displays the Hf 4*f* core-level spectrum of HfO_xN_y thin films on Ge substrates with and without Si_2H_6 passivation, we observed that the profiles shifting to higher binding energy after Si_2H_6 passivation; this finding was also recognized in the ZrO_xN_y/Si gate stacks

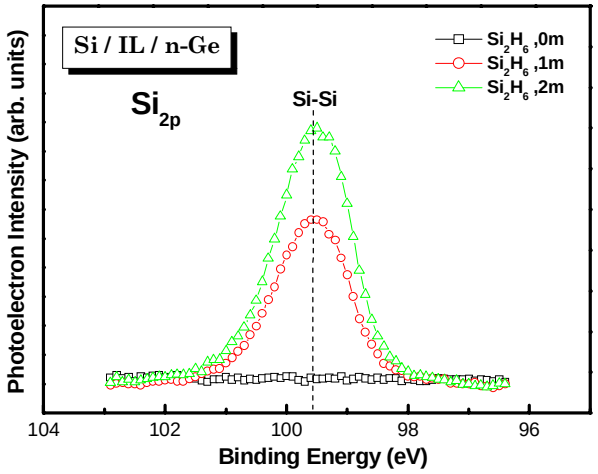
in chapter 2, which indicated that the Si interlayer formed by Si_2H_6 passivation converted both the Hf–N and Hf–O bonds into the configuration of Hf–O–Si bond. Besides, there was no evidence of the emergence of interfacial Hf–O–Ge bonding, which was consistent with the discussion in ZrO_xN_y/Ge gate stack in chapter 2.

The residual oxygen in RTA chamber could readily oxidize the entire Ge substrate and incurred the formation of volatile GeO, which resulted in the signal of GeO_x for Si_2H_6 passivation simples, as shown in figure 5-12 (a) and (b). Nevertheless, the intensity of GeO_x caused by residual oxygen was very weak with respect to the GeO_x caused by the interfacial layer desorption. Consequently, increasing annealing temperature and duration had slightly enlarged the amount of GeO_x from chamber residual oxygen which was shown in figure 5-13 (a) and (b).

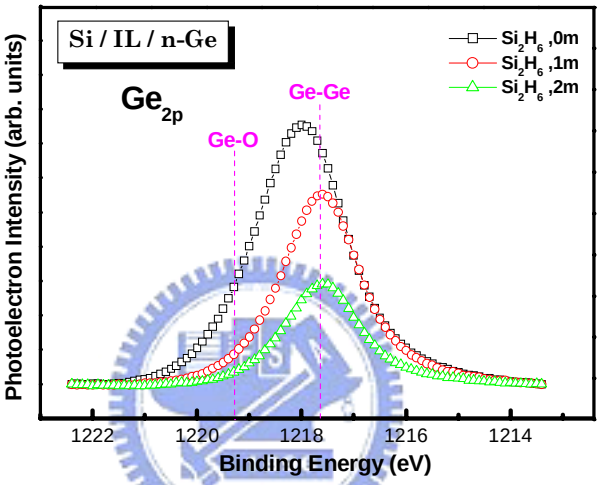
Figure 5-14 (a) and (b) show the O 1*s* and Si 2*p* core-level spectra of HfO_xN_y/n-Ge gate stacks with Si_2H_6 passivation for 1 min. The slight intensity of Si-Si bonding for as-deposed sample was observed in figure 5-14 (b), which was referred to the Si interlayer formed by Si_2H_6 passivation. After post annealing at 500°C, the Si-Si bond was naturally oxidized and thus increased the signal of SiO_x. Moreover, PDA at 500°C did not cause Ge to diffuse into high-k gate dielectric, as shown in figure 5-15 (a) and (b), which was likely contributed to the Si interlayer.

5-4 Summary

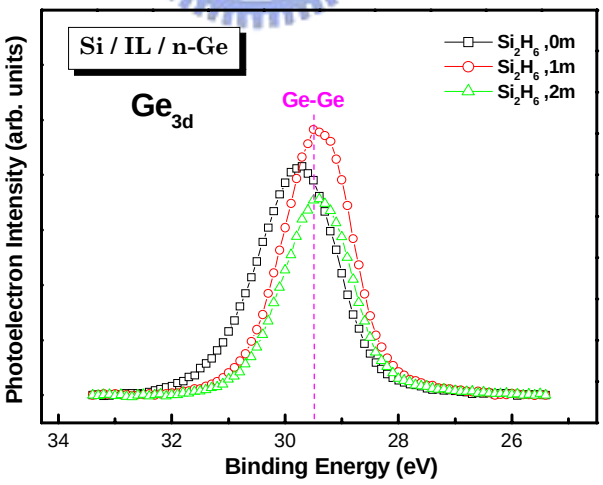
In this chapter, we have demonstrated the electrical and physical characteristics of $Pt/HfO_xN_y/Ge$ and $Pt/ZrO_xN_y/Ge$ capacitors with Si_2H_6 surface pretreatment. We found that GeO_x was successful eliminated by thermal desorption at 550°C for 10 min and following Si_2H_6 passivation, which reduced the gate leakage current and hysteresis width of $Pt/HfO_xN_y/Ge$ and $Pt/ZrO_xN_y/Ge$ capacitors. However, the high-frequency C-V curves presented a low-frequency-like characteristic after Si_2H_6 passivation, which was likely a typical characteristic of the increment of bulk traps. Besides, the bulky defects with energy levels near midgap in Ge were also responsible for the supply of minority carriers to the inversion layer, incurring the onset of low-frequency-like C–V characteristic. Nevertheless, the samples with Si_2H_6 passivation for 2 min probably induced large stress and dislocations in Ge substrate which led to the large gate leakage current.



（a）

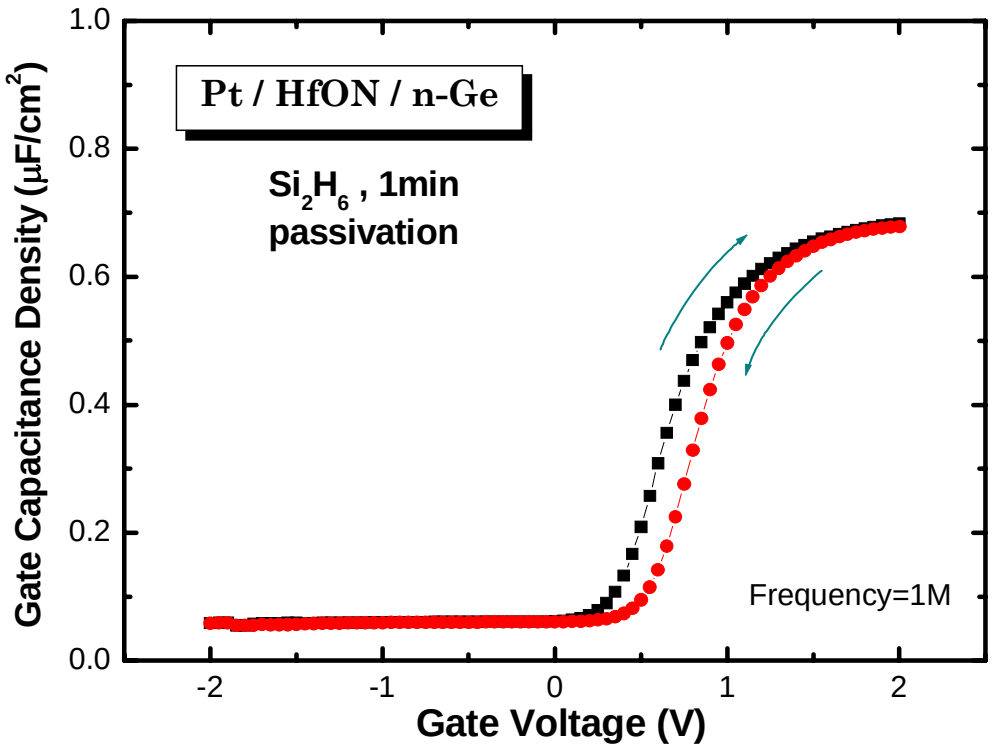


（b）

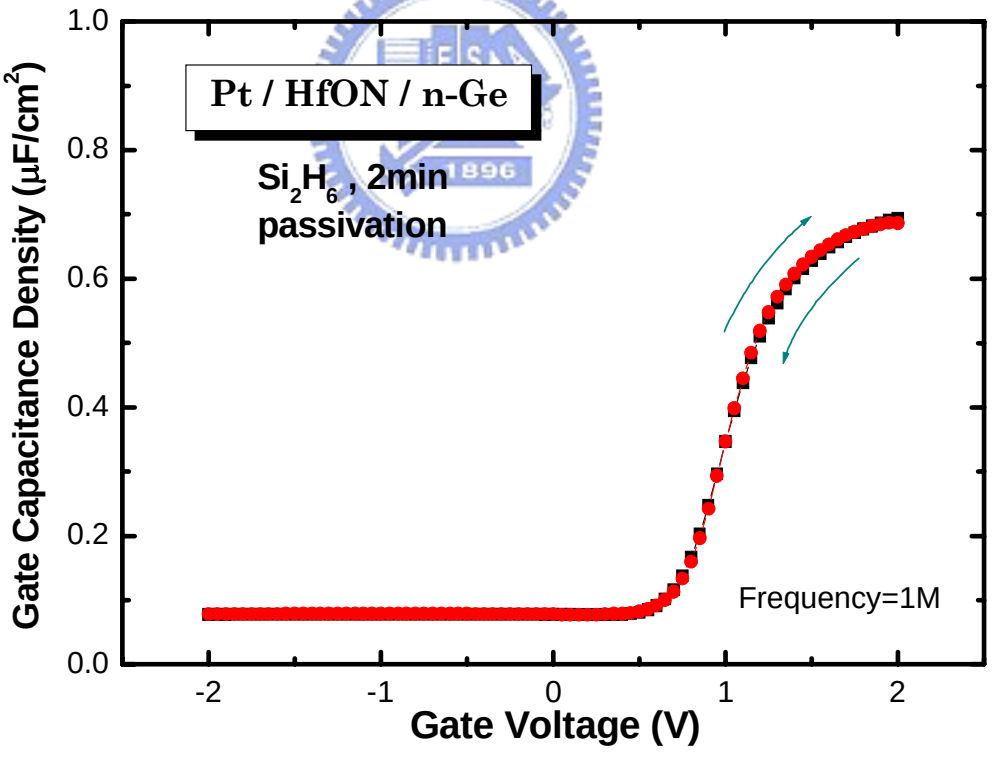


（c）

Fig. 5-1 （a）Si 2*p*, （b）Ge 2*p* and （c）Ge 3*d* core-level spectra of Ge substrates with and without Si_2H_6 passivation.

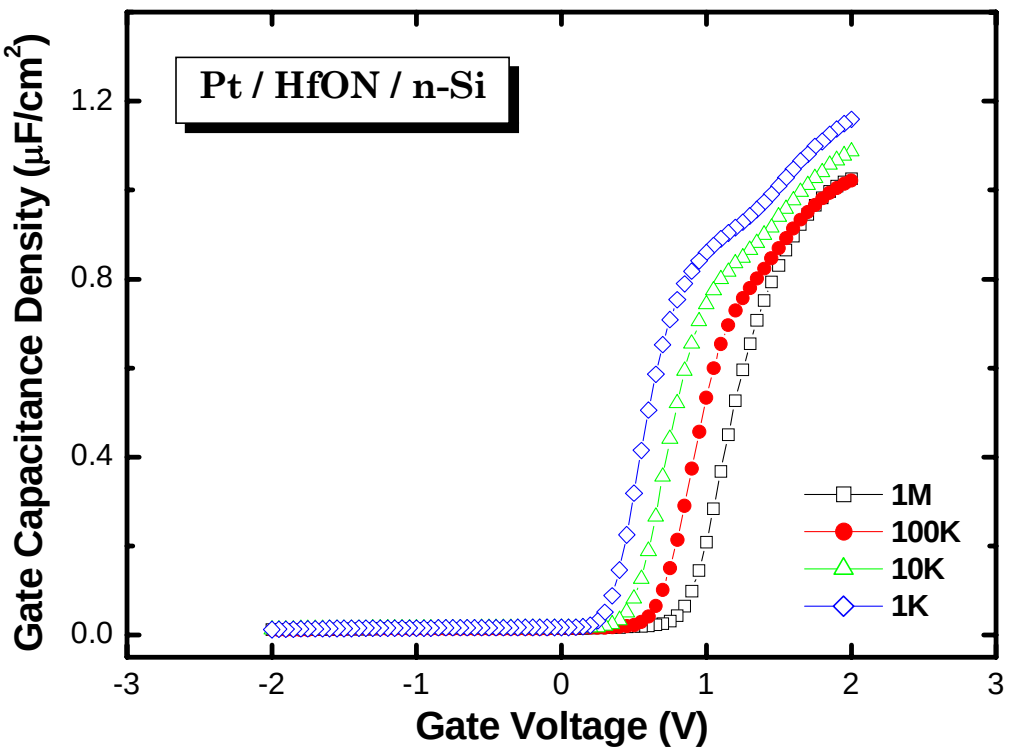


（a）

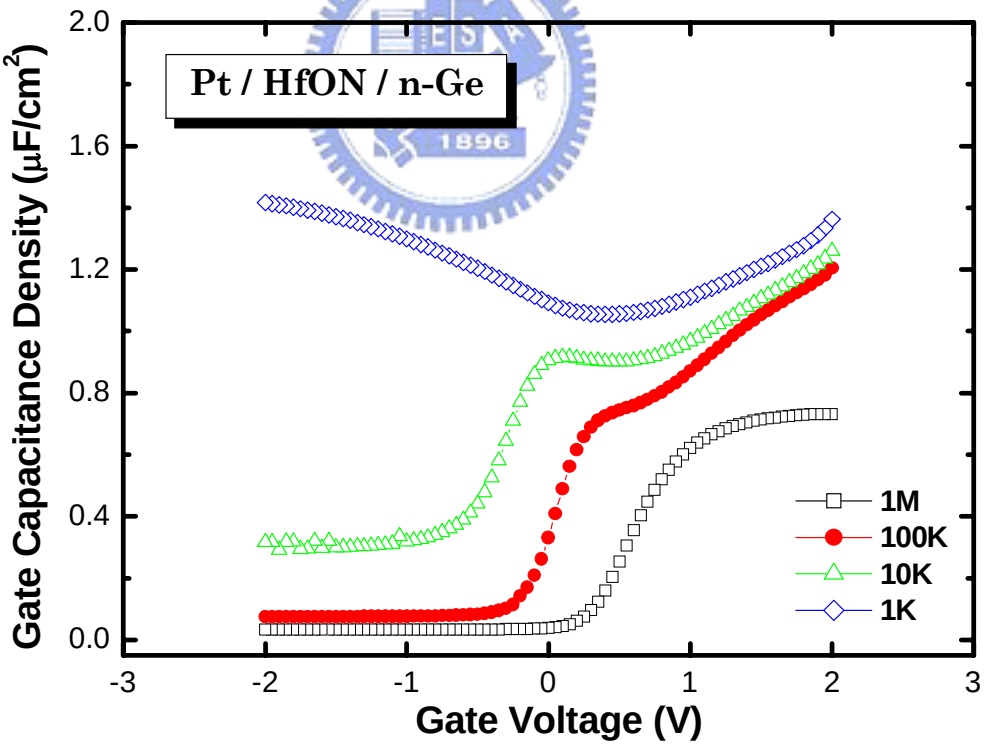


（b）

Fig. 5-2 Typical 1-MHz C–V curves of Pt/HfO_xN_y/Si/n-Ge capacitors with Si_2H_6 passivation for（a）1min and （b）2min.

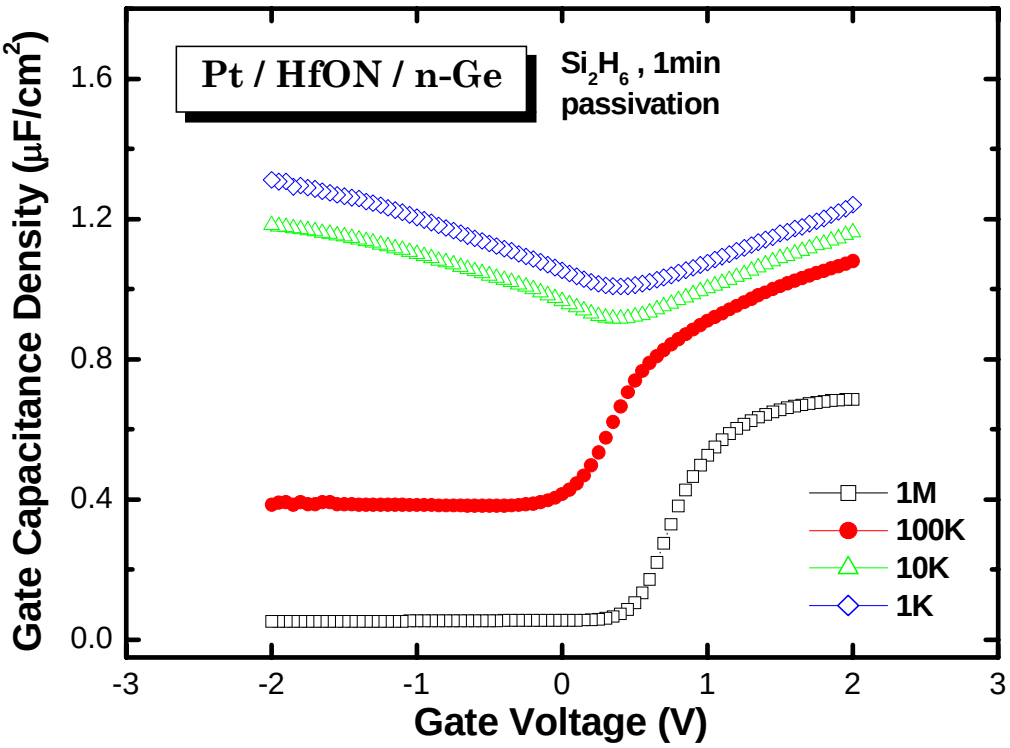


（a）

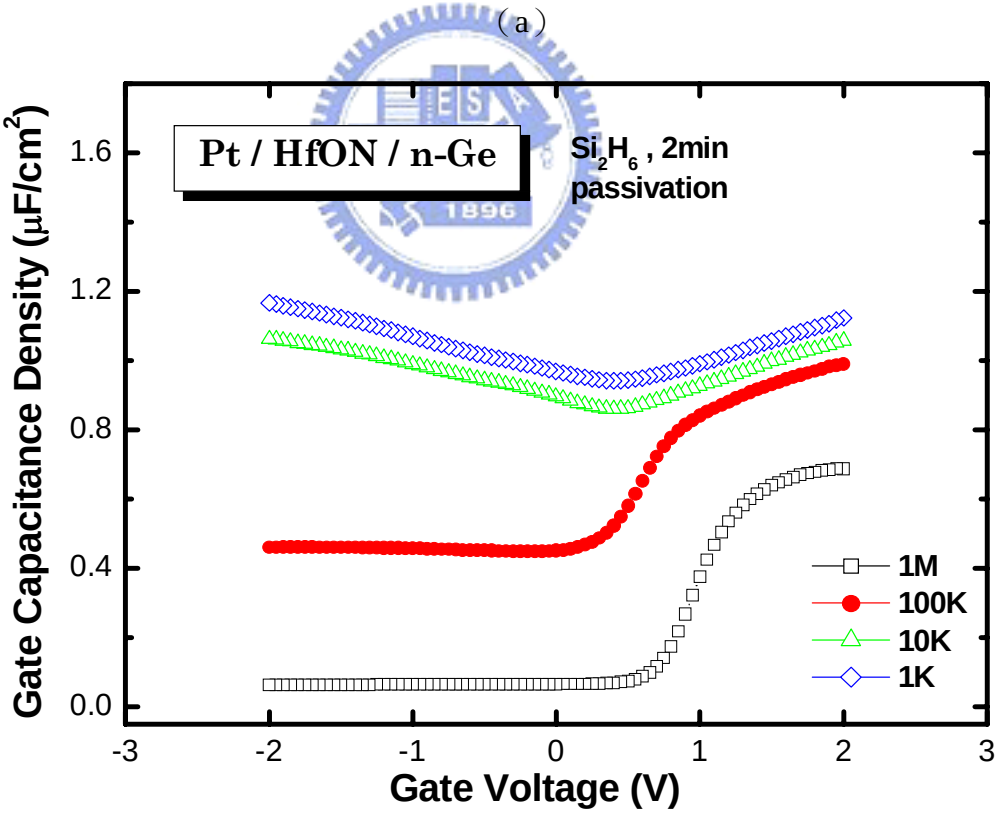


（b）

Fig. 5-3　The 1-MHz, 100-kHz, 10-kHz and 1-kHz C–V curves of（a）Pt/HfO_xN_y/n-Si and（b）Pt/HfO_xN_y/n-Ge capacitors without Si_2H_6 passivation.



（a）



（b）

Fig. 5-4　1-MHz, 100-kHz, 10-kHz and 1-kHz C–V curves of $Pt/HfO_xN_y/Si/n$-Ge capacitors with Si_2H_6 passivation for（a）1min and （b）2min.

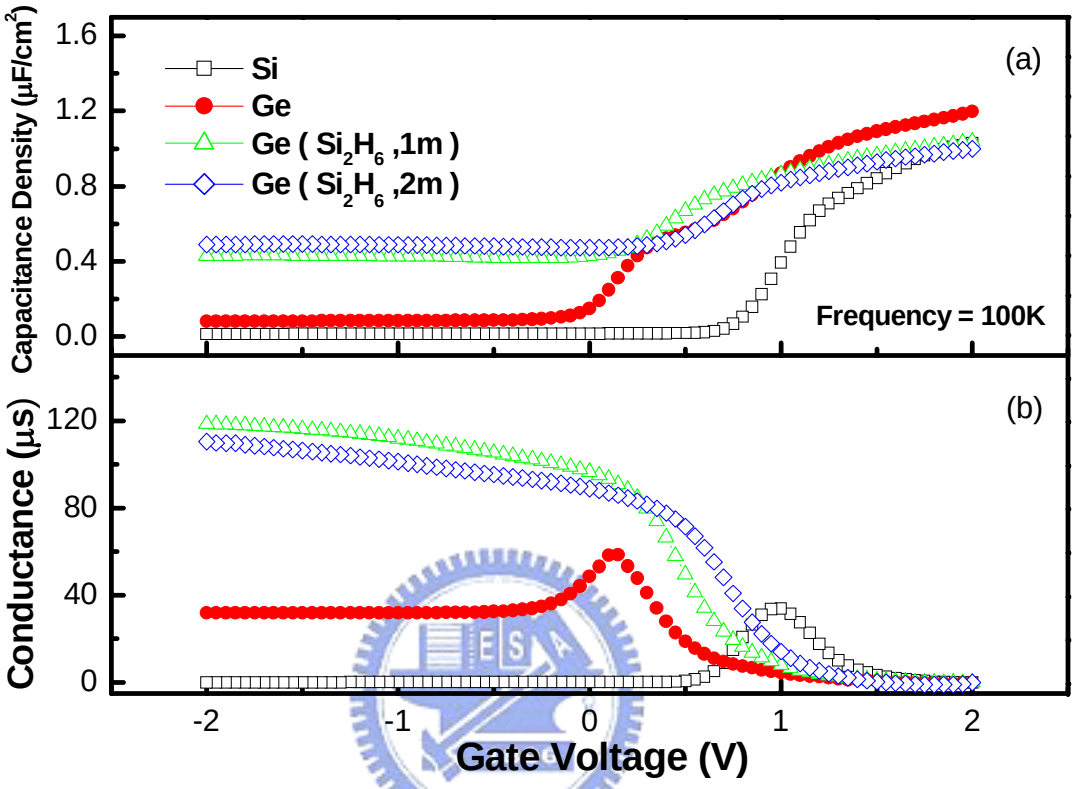


Fig. 5-5 Typical 100-kHz（a）C–V and （b）G–V curves of Pt/HfO_xN_y/n-sub capacitors with and without Si_2H_6 passivation.

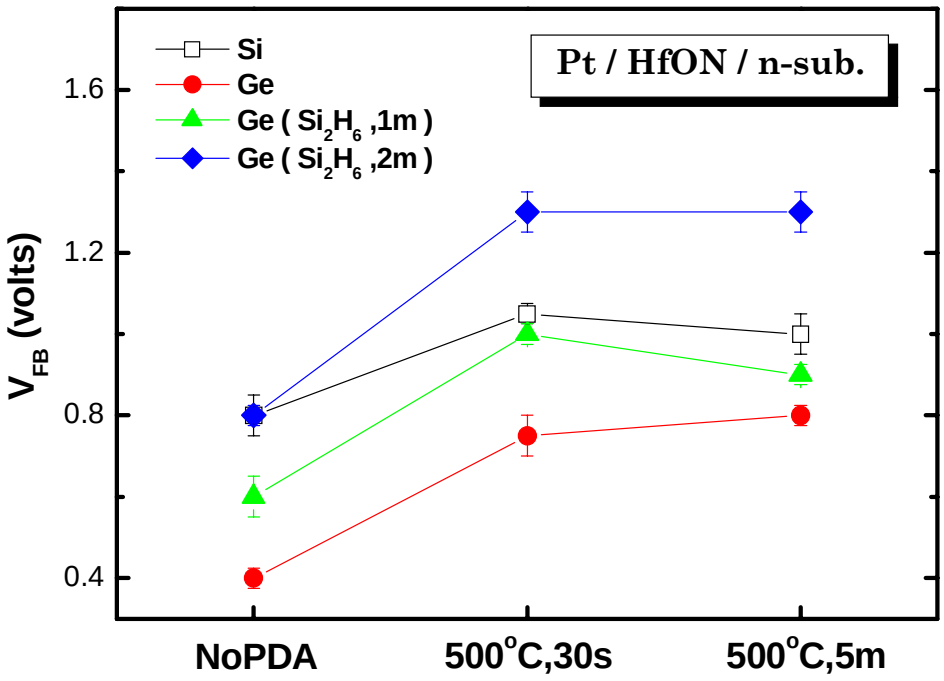


Fig. 5-6 The flat-band voltage of Pt/HfO_xN_y/n-sub capacitors for as-deposited and annealed ones.

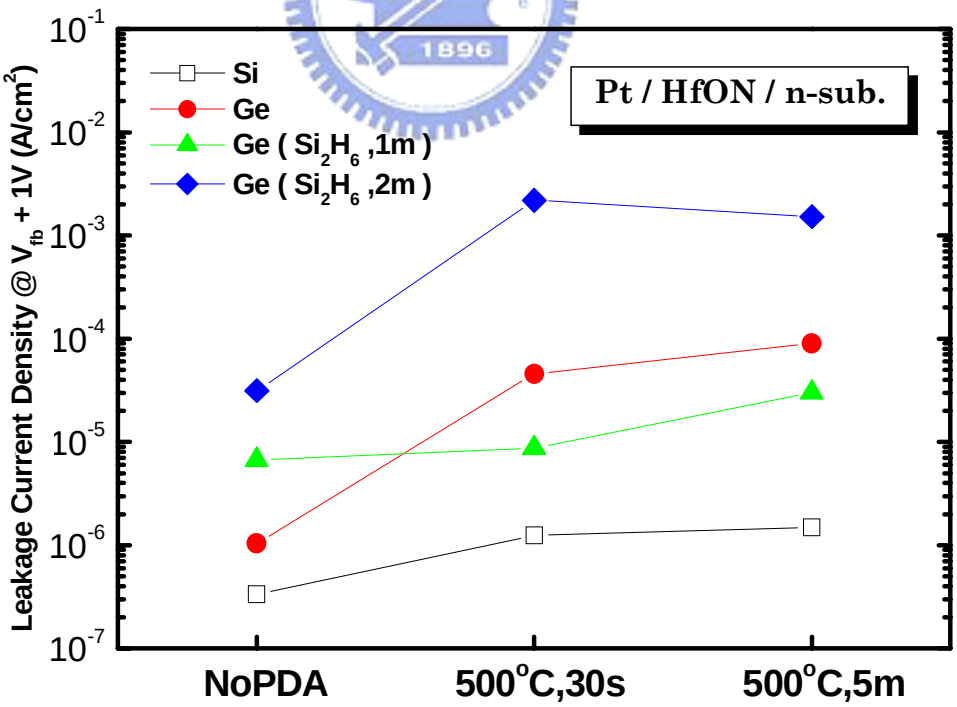


Fig. 5-7 The gate leakage current density of Pt/HfO_xN_y/n-sub capacitors for as-deposited and annealed ones.

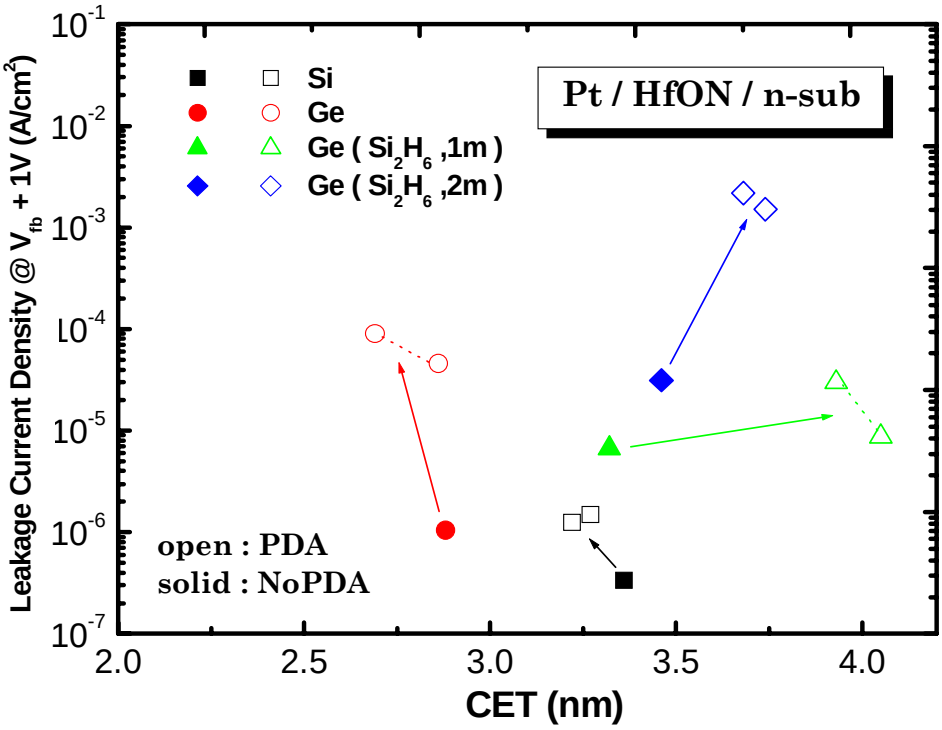


Fig. 5-8 The gate leakage current density versus the CET of Pt/HfO_xN_y/n-sub capacitors for as-deposited and annealed ones.

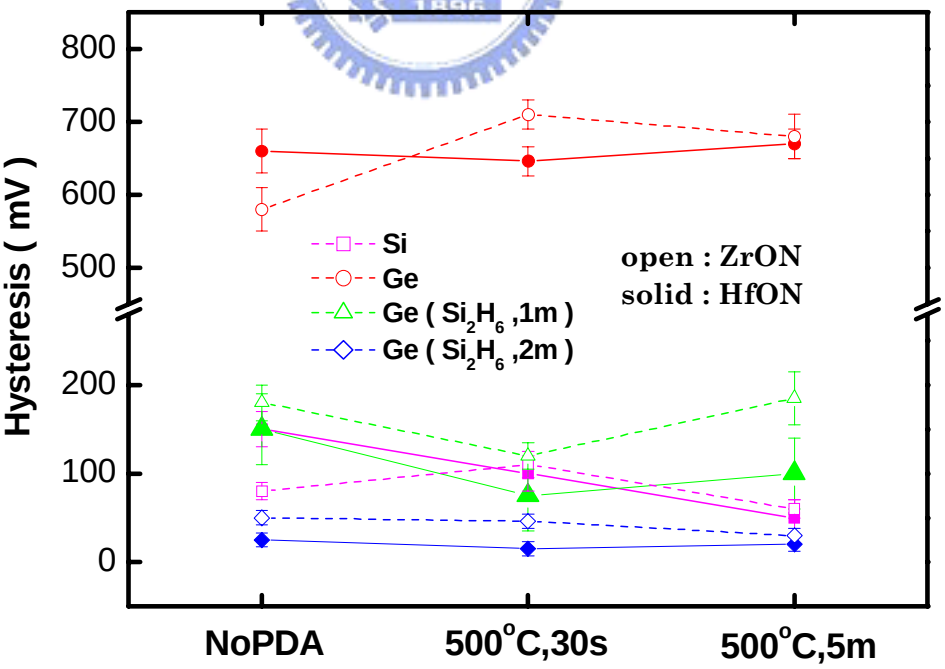


Fig. 5-9 The hysteresis of Pt/HfO_xN_y/n-sub (solid symbols) capacitors and Pt/ZrO_xN_y/n-sub (open symbols) capacitors.

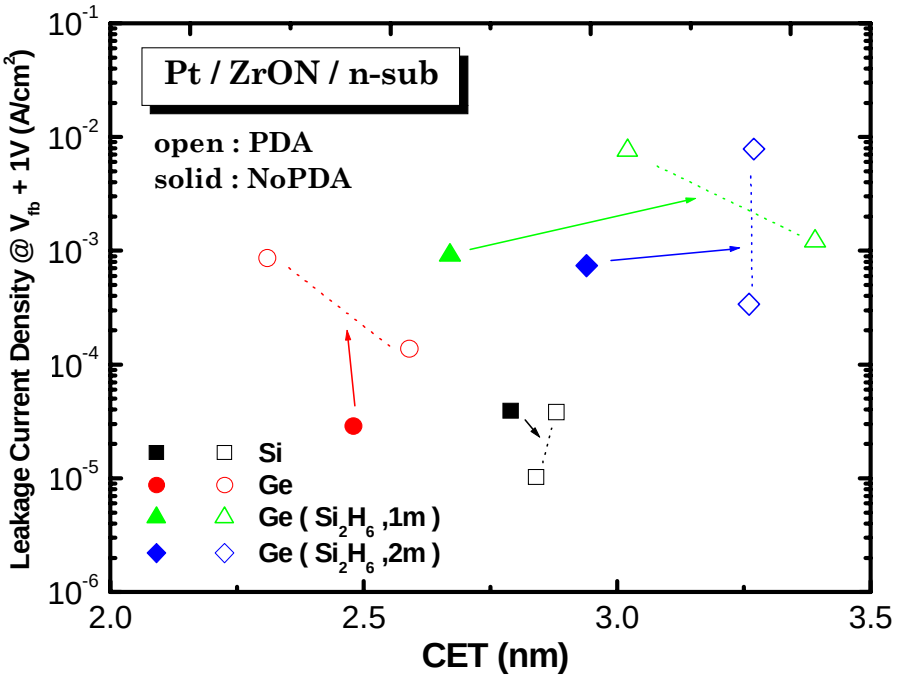


Fig. 5-10 The gate leakage current density versus the CET of Pt/ZrO_xN_y/n-sub capacitors for as-deposited and annealed ones.

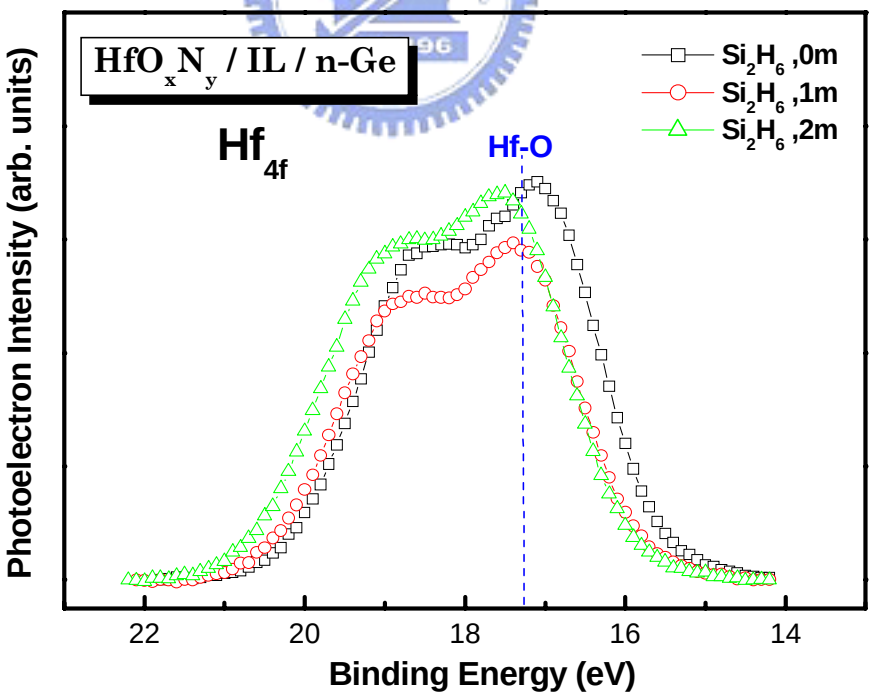
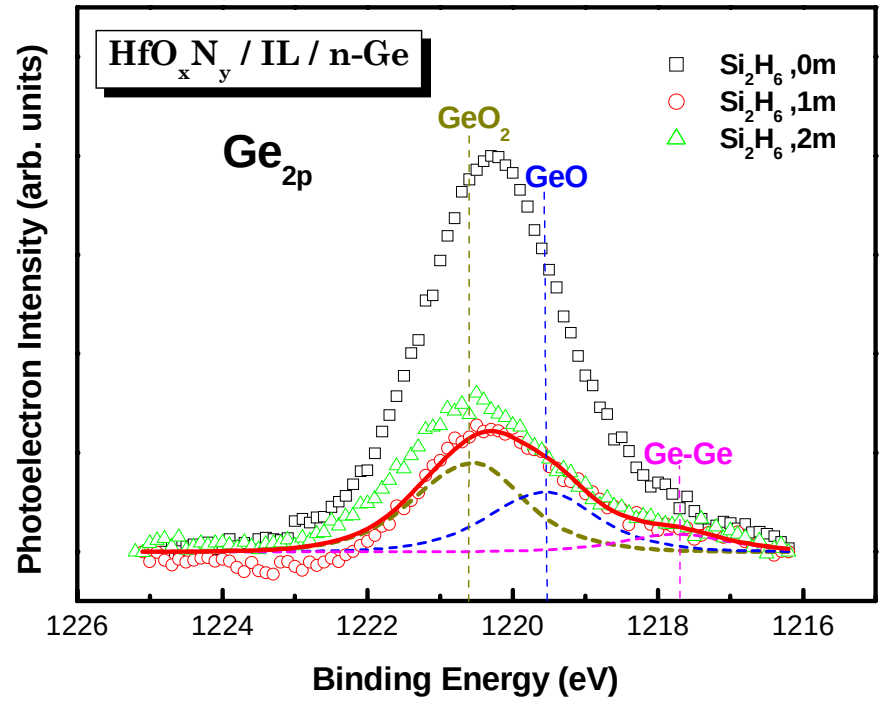
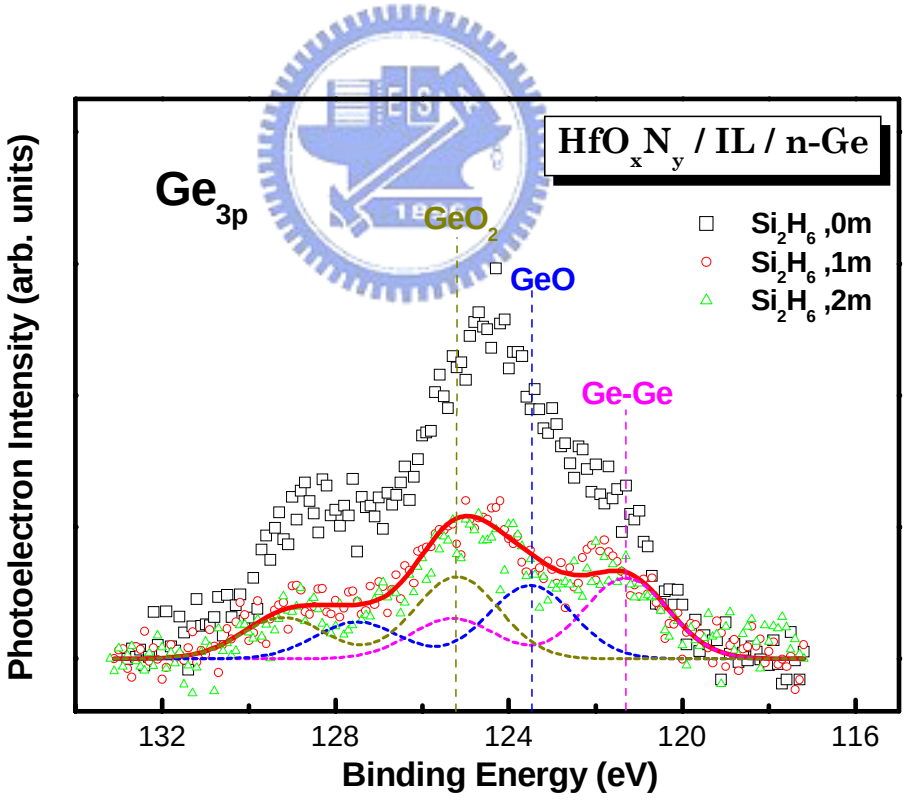


Fig. 5-11 The Hf 4*f* core-level spectrum of HfO_xN_y thin films on Ge substrates with and without Si_2H_6 passivation.

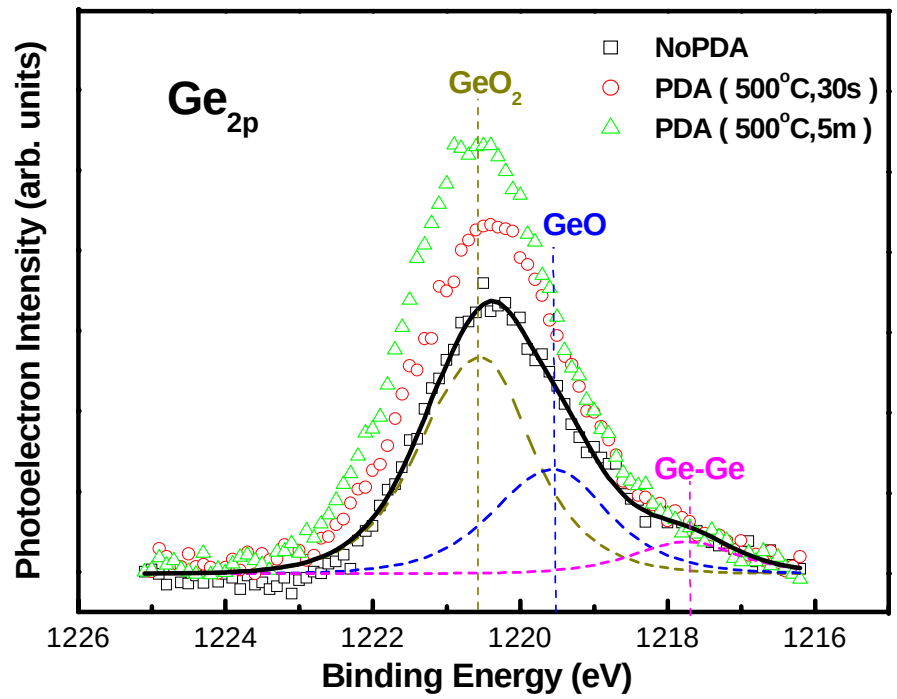


(a)

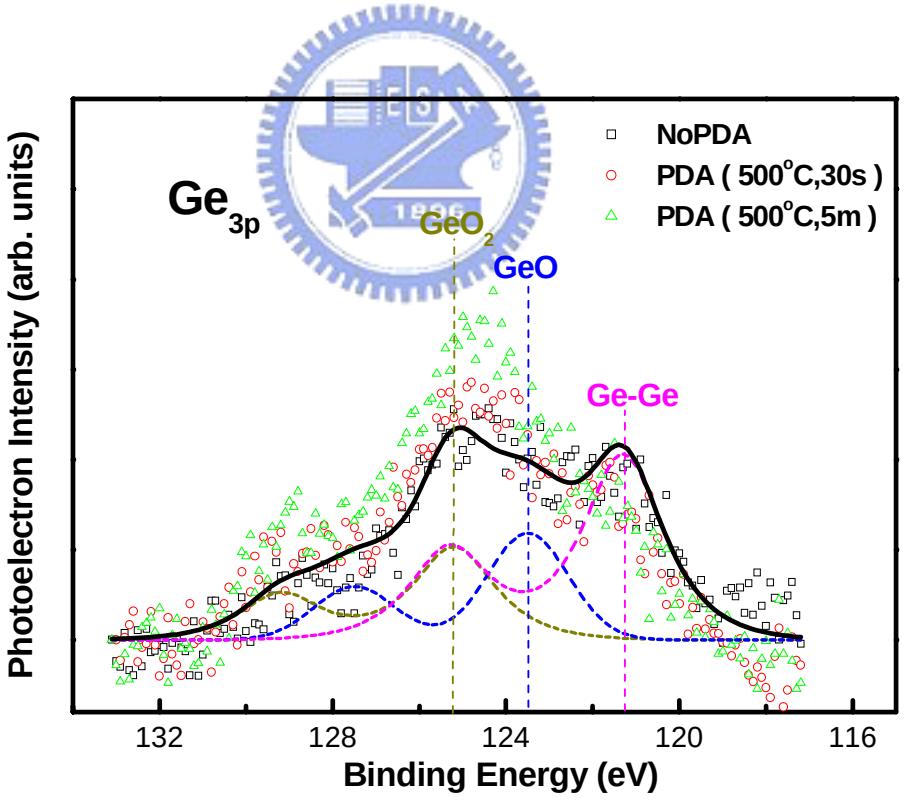


(b)

Fig. 5-12 (a) Ge 2*p* and (b) Ge 3*p* core-level spectra of HfO_xN_y thin films on Ge substrates with and without Si_2H_6 passivation.

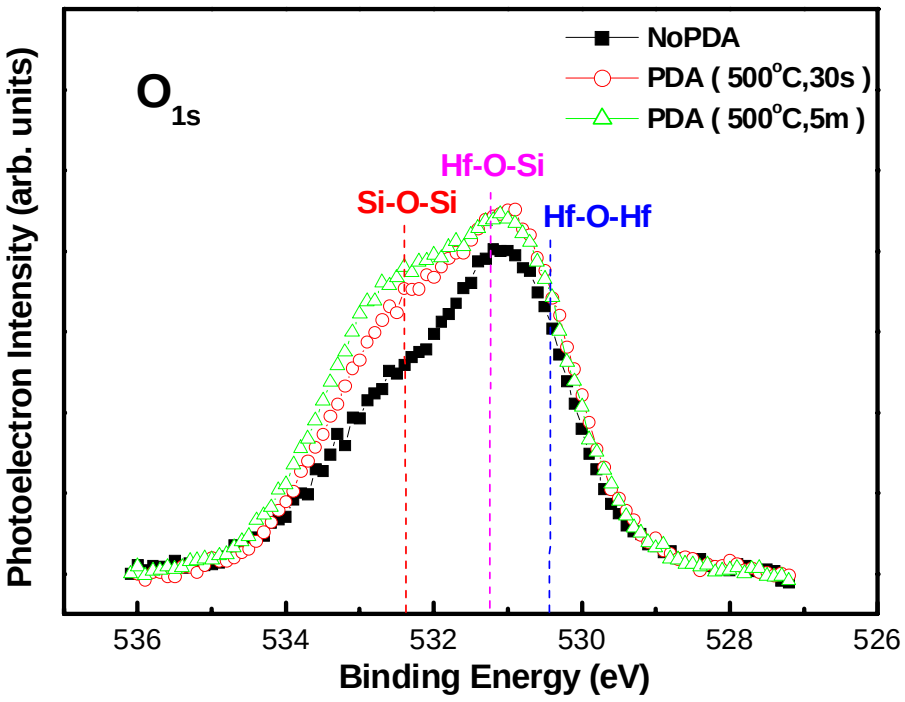


（a）

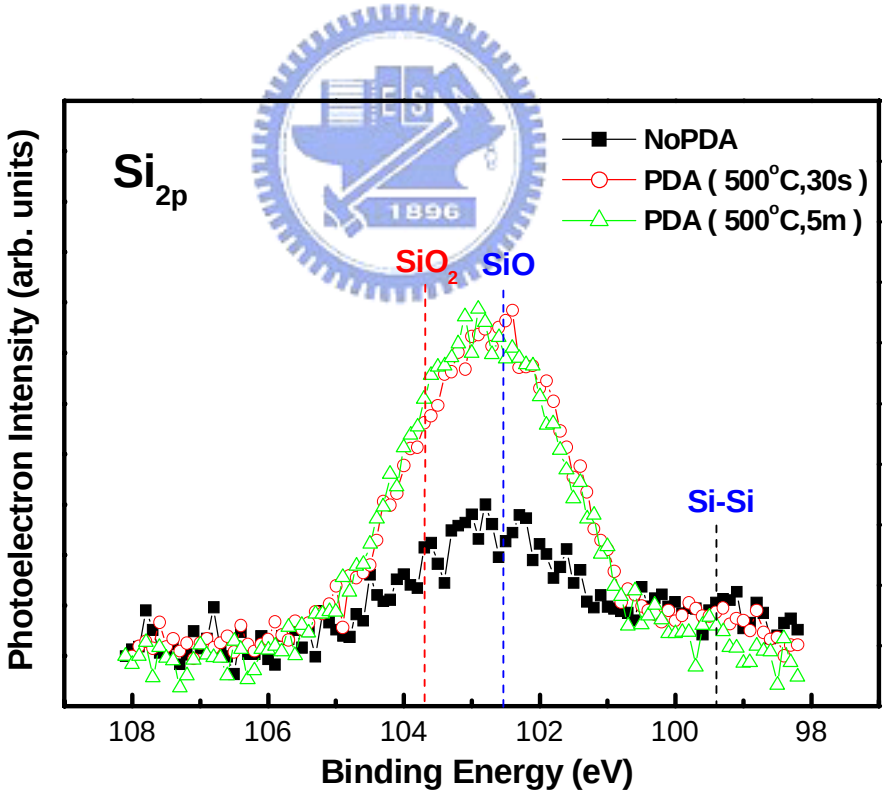


（b）

Fig. 5-13（a）Ge 2*p* and（b）Ge 3*p* core-level spectra of HfO_xN_y/n-Ge gate stacks with Si_2H_6 passivation for 1 min.

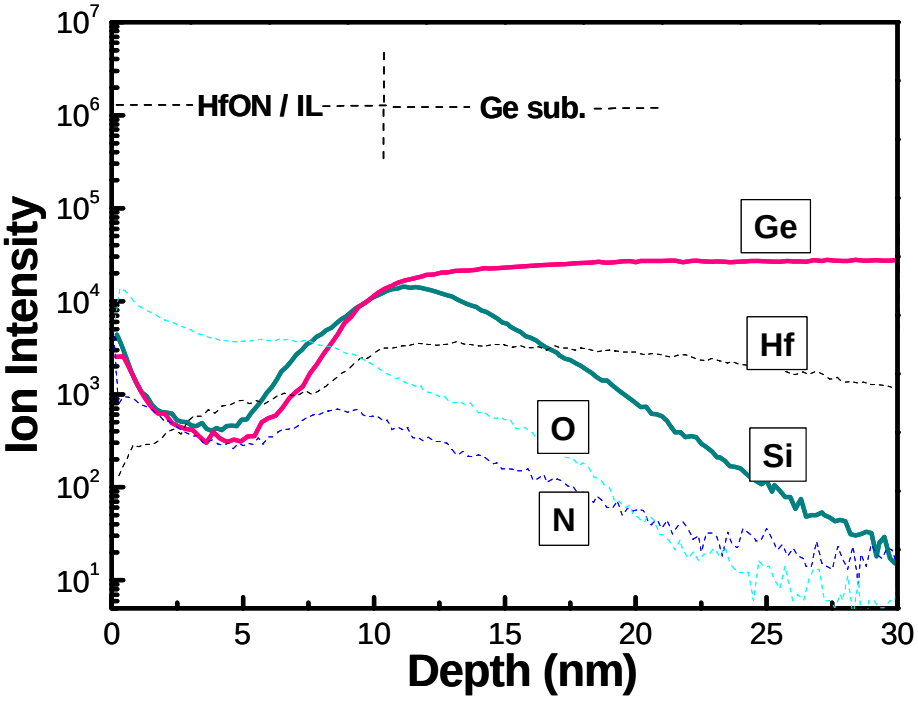


（a）

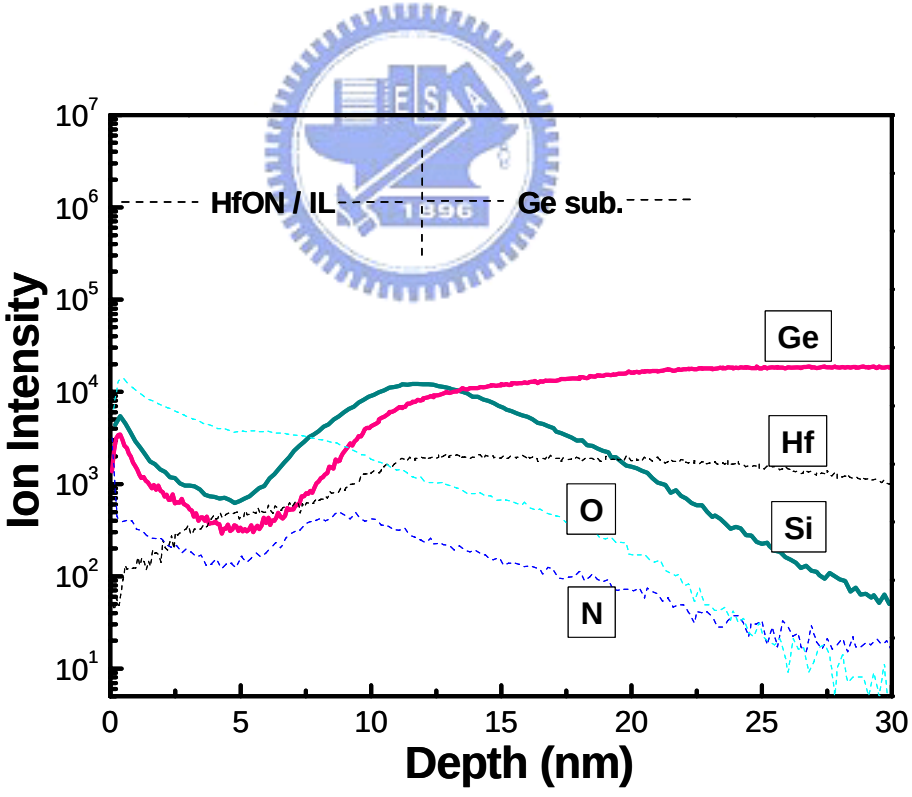


（b）

Fig. 5-14 （a）O 1*s* and （b）Si 2*p* core-level spectra of HfO_xN_y/n-Ge gate stacks with Si_2H_6 passivation for 1 min.



（a）



（b）

Fig. 5-15 The SIMS depth profiles of HfO_xN_y/n-Ge gate stacks (after 1min Si_2H_6 passivation) for （a）as-deposited and （b）500°C PDA for 5 min.

Chapter 6

Conclusions and Suggestions for Future Work

6-1 Conclusions

In this thesis, we study the electrical and physical properties of HfO_xN_y and ZrO_xN_y gate dielectrics on Ge substrates with different surface pretreatments. Firstly, we studied the high-k/Ge interface properties and discussed about the thermal stability of high-k/substrate interface on Ge is not as good as that on Si due to inherent poor quality of Ge native oxide. We found that high temperature processing aided the interfacial layer growth and the formation of Zr–silicate in $ZrO_x(N_y)$/Si gate stack. On the contrary, severe interfacial layer volatilization and the inhibition of Zr–germinate were found in $ZrO_x(N_y)$/Ge system; these features are expected to possess a better EOT scalability with respect to $ZrO_x(N_y)$/Si system. Nevertheless, the generated localized pits in deposited high-k films owing to the desorption of the underlying interfacial layer may severely degrade the electrical properties of fabricated high-k/Ge devices.

Since Ge oxide plays an important role in the interface of high-k/Ge system, two thermal processes including PDA and PMA were discussed to help us realize its impact on entire capacitor structures. We found that the PDA process did not multiply the pre-existing bulk traps in Ge substrate, which was conformed by corresponding G–V results, whereas the PMA

process increased them, and thus presented low-frequency-like behavior in high-frequency C–V curves. Furthermore, both annealing processes were found to annihilate the amount of D_{it} and shrink the CET, but meanwhile these thermal processed increased the gate leakage current.

Although proper thermal processes can reduce the D_{it} of high-k/Ge gate stack, the poor thermal stability and hysteresis effect were the major issues in our experiment. We found that the hysteresis of Pt/high-k/n-Ge capacitors was due to the trapping centers near high-k/IL interface. In order to improve the interface quality of high-k/Ge interface, CF_4 and NH_3 plasma pretreatment were applied. Unfortunately, The CF_4 plasma pretreatment enlarged the hysteresis width and gate leakage current of Pt/high-k/Ge capacitors, which were possibly due to the increment of D_{it} and surface roughness. On the other hand, the NH_3 plasma pretreatment compressed the hysteresis width, which was related with less GeO_x and D_{it}, moreover, the nitridation process improved the thermal stability of Pt/high-k/Ge capacitors by diminishing the formation of GeO_x and their volatilization.

NH_3 surface pretreatment improved the electrical properties by suppressing the growth of GeO_x, but nitrogen incorporation may not be sufficient to fully passivate the dangling bonds on Ge surface and prevent the growth of GeO_x. The Si_2H_6 passivation which was expected to prohibit the growth of GeO_x by forming several monolayers of Si between gate dielectric and Ge substrate were demonstrated. We found that GeO_x was successful eliminated by thermal

desorption at 550°C for 10 min and following Si_2H_6 passivation, which reduced the gate leakage current and effectively compressed the hysteresis width of Pt/HfO_xN_y/Ge and Pt/ZrO_xN_y/Ge capacitors. However, the high-frequency C-V curves presented a low-frequency-like characteristic after Si_2H_6 passivation, which was likely a typical characteristic of the increment of bulk traps, and the bulky defects with energy levels near midgap in Ge were also possibly resulted in the supply of minority carriers to the inversion layer, incurring the onset of low-frequency-like C–V characteristic. The research in further details of low-frequency-like C-V characteristic needs more investigation and other physical analyses are still in study.

6-2 Suggestions for Future Work

The hysteresis effect of Pt/high-k/n-Ge capacitors is due to the trapping centers near high-k/IL interface, and we have suggested the inner-interface trapping model of Pt/high-k/IL/Ge gate stacks, but the detailed distribution of those trapping centers is waiting to be solved.

The low-frequency-like C–V characteristic appears in the PMA and Si_2H_6 passivation samples, which was speculated resulting from a typical characteristic of the increment of bulk traps and the bulky defects with energy levels near midgap in Ge. However, we need more valid evidence to figure out the mechanism of minority carrier behavior.

The experiment of Si_2H_6 passivation indicated that GeO_x was successful eliminated by thermal desorption at 550°C for 10 min, therefore, thermal desorption processes prior to in-situ high-k deposition seems a better method to improve the electrical properties of high-k/Ge gate stack. Moreover, atomic layer deposition (ALD) substitute for reactive sputtering of high-k deposition techniques is particularly attractive in terms of precise thickness control and near-perfect conformality for ultra thin high-k formation.

Finally, fabricating Ge MOSFET structure is necessary to perform complete evaluation of the implementation of Ge in combination with a high-k dielectric.

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The Electrical and Physical Properties of Hf(Zr)-oxynitride Gate Dielectrics on Ge Substrates with Various Surface Pretreatments