Chapter 2

Low Temperature Process of OTFTs with LPD SiO_2 as Gate Insulator

2.1 Introduction

Organic Thin Film Transistors(OTFTs) allow fabrication of electronic circuits and active-matrix displays on various substrates, such as Si, glass, polymide [21.],[2.2],[2.3], PEN, PET, and polycarbonate. In the future, OTFTs will be fabricated on clothes or paper substrate for flexible application. Organic thin film such as P3HT, pentacene, and α-sexithiophene can be deposited below 150℃, but the gate insulator of OTFT is hardly deposited with high quality at low temperature . Consequently, we need to develop a low temperature process for gate insulator of OTFTs. Among most commonly used deposition techniques, e-beam evaporation and sputtering are potential candidates for low temperature process. But the quality of SiO_2 deposited by e-beam evaporation and sputtering is not good enough that we have to deposit thicker SiO_2 to avoid large gate leakage current [2.4],[2.5],[2.6]. Other materials for gate insulator of OTFTs are organic dielectrics such as PVP and polyimide [2.7],[2.8].But the required thickness of organic dielectrics are thicker than SiO_2 due lower dielectric constant than SiO_2.To provide higher quality SiO2 than those deposited by e-beam evaporation and sputtering, we deposit SiO_2 by Liquid-Phase Deposition(LPD), a room temperature process.

2.2 Chemical Vapor Deposition(CVD) and Liquid-Phase Depotition(LPD)

Chemical Vapor Deposition(CVD) is the most common method to deposit SiO_2 at low temperature. SiO_2 can be deposited at atmospheric pressure with high deposition rate by atmospheric pressure CVD(APCVD), which was firstly used in the

microelectronics industry,. However, APCVD is susceptible to gas phase reactions, and the films typically exhibit poor step coverage. Since APCVD processes are generally conducted in the mass transport limited regime, the reactant flux to substrate in the reactor must be precisely controlled. By low pressure CVD(LPCVD), SiO_2 can be deposited at 650~750℃ by decomposing tetraethoxysilane(TEOS). LPCVD TEOS is useful for depositing insulators on poly-silicon gate, but the high deposition temperature precludes its use over aluminum process. The advantages of LPCVD TEOS deposition are excellent uniformity, conformal step coverage, and good film properties. The disadvantage is the requirement of high temperature process. Not alike APCVD and LPCVD, plasma enhanced CVD(PECVD) uses an rf-induced glow discharge to transfer energy into the reactant gases, allowing the substrate to maintain at lower temperature. Lower substrate temperature is the major advantage of PECVD. However, the properties of PECVD SiO_2 are not stoichiometric because the deposition reactions are complicated. Moreover, by-products and incidental species are easily incorporated into the resulting films, especially hydrogen and nitrogen. Excessive incorporation of these contaminants may lead to out-gassing and concomitant bubbling, cracking or peeling during later thermal cycling, and threshold voltage shifts in CMOS circuits.

Liquid-Phase Deposition(LPD) technology was first proposed by Nagayama et al. in 1988[2.9]. At first, SiO_2 was depotited by LPD on glass substrate to prevent the alkali ions from migrating in the glass substrate. Homma et al. found that SiO_2 could be selectively deposited by LPD between tungsten wiring [2.10],[2.11]. Furthermore, LPD was developed and applied to VLSI technology [2.12],[2.13]. From 1993, Yeh's research group applied SiO_2 deposited by LPD as gate insulator to fabricated Low Temperature Poly-Si Thin-Film Transistors (LTPS-TFTs) and MOSFETs[2.14],[2.15].

From the above mention, although several CVD methods can be used to deposit

SiO_2 at low temperatire, the processes are complicated and the costs of equipments are high. As to SiO_2 deposited by LPD, there are two main advantages in comparison with other CVD methods. First, the substrate temperature during deposition can be greatly reduced, because LPD SiO_2 can be deposited at room temperature. Second, the apparatus are much simpler and cheaper. The characteristics of LTP SiO_2 include room-temperature deposition, cheap apparatus, large coverage area application, selective deposition, and dielectric constant 3.9(fluorine incorporated).

2.3 Mechanism of LPD

The schematic diagram of the apparatus for liquid-phase deposition technology is illustrated in Fig. 2-1. First, 75 g of silica (SiO_2) powder with high purity of 99.999% was mixed with 1200 ml of hydrofluorosilicic acid (H_2SiF_6, 4 mol/l) and then the solution was stirred in the "saturation tank" at 23°C for 18 ~ 24 hr. The temperature of the LPD solution was controlled precisely by a water chiller. After stirring for tens of hours, the hydrofluorosilicic acid became saturated, which can be represented by the following equation:

$$5H_2SiF_6 + SiO_2 + 6H_2O \rightarrow 4SiF_6^{2-} + 2Si(OH)_4 + 6HF + 8H^+$$

Before starting the deposition process, the pipes, filters, valves, and pumps (driven by compressed dry air, CDA) should be cleaned by diluted HF and D.I. water rinse for several times to ensure the cleanness. This process can be performed automatically through the programmable control of the LPD apparatus. Next, the saturated H_2SiF_6 solution was pumped out of the left saturation tank, filtered through two PTFE filters with pore size of 0.5 μm/0.1 μm respectively to remove the undissolved SiO_2 particles, and then flow into the right "deposition tank." The temperature of the deposition tank was also controlled by the water chiller at 23°C or 25°C.

When the samples were ready for deposition LPD-SiO_2, we added D.I. water into

the saturated H_2SiF_6 solution and thus the equilibrium condition was altered, contributing to a super-saturated state of silicic acid $Si(OH)_4$. After immersing the samples, the $Si(OH)_4$ molecules would react with the hydrophilic surface, that is, the surface full of OH bonds, and then the $Si(OH)_4$ dehydrate into SiO_2 at deposition rate about 25nm/hr under an acid catalytic polymerization process. For those hydrophobic surfaces such as photo resist or metals (e.g. Ta), the SiO_2 will not deposit on them and an extraordinary selectivity can be obtained. Finally, the two PTFE filters were cleaned again to remove the SiO_2 following the standard cleaning process of LPD apparatus.

2.4 Experimental Detail

2.4.1 Process flow of OTFTs based on P3HT with SiO_2 as gate insulator by PECVD and LPD

OTFT based on P3HT with bottom-contact structure is fabricated on a silicon substrate as shown in Fig. 1-4(a). The process flow is described in detail as following. At first, an n-type bare silicon wafer was cleaned by the standard RCA clean process. After RCA clean, phosphorus atoms were diffused into an n-type silicon wafer by $POCl_3$ to form a common gate electrode. Then we used dilute HF to remove SiO_2 and measured its sheet resistance(3~5Ω/□) .Before we deposited SiO_2 as gate insulator, the n+ silicon wafer must be cleaned by the standard RCA clean process again. An insulating layer of 120nm SiO_2 is deposited on the silicon substrate by PECVD using TEOS and O_2 source gas at 350℃ and LPD. Afterwards, source and drain regions were defined through the photo lithography process followed by e-beam evaporation of a 20-nm thick layer of Ti as an adhesion layer and a 100-nm thick layer of Pt as a contact material. Later, the wafer was then immersed in acetone to lift-off the photo resist and to form the source/drain regions. A comb geometry, as depicted in Fig.

1-4(b) for the source/drain contacts, is adopted to minimize the device area and the associated gate to source/drain leakage current. A typical channel width W was in the range of 100 ~ 10,000 μm and a channel length was 10 ~ 50 μm. The samples after S/D patterning were treated with 3 minute IPA clean and 5 minute D.I water clean. Next, oxide surfaces were treated with hexamethyldisilazane (HMDS) to improve the adhesion between the polymer chain and the oxide surface. After treating SiO_2 surface with HMDS, the hydroxyl groups at the oxide surface would be replaced by methyl groups and the apolar nature of these groups apparently attract the hexyl side chains of P3HT, favoring lamellae with an edge-on orientation [2.16]. P3HT of 0.3 wt.% dissolved in chloroform was deposited by the spin-coating method to form the active layer. P3HT solution was filtered by a 0.2-μm pore-size PTFE filter and then spun onto the wafer surface. The detail spin-coating parameters is: 200RPM for 10s, 500RPM for 25s and 2000RPM for 25s. Finally, the sample was cured at 120℃ for 3 minutes. Process flow is shown in Fig2-2. Before measuring electric characteristics, the sample was stored in vacuum for 2 days to let the oxygen atoms out-diffuse. The electric characteristics of OTFTs were measured by HP4156.

2.4.2 Process flow of OTFTs based on P3HT with SiO_2 as gate insulator and isolation layer by LPD

The quality of SiO_2 deposited by LPD as gate insulator for OTFT without thermally annealing is poorer than that deposit by PECVD [2.17]. The gate leakage current of OTFTs with LPD SiO_2 insulator are larger than that of previous experiment. In order to suppress the leakage current, we demonstrated a stacked structure which addtional SiO_2 was deposited by Selective LPD(S-LPD) as an isolation layer under source and drain electrodes. Comparing to the same structure in [2.18], the isolation layer need only one lithography process because the selectively deposition properties of LPD method. Process flow is shown in Fig. 2-3. After substrate doping, LPD SiO_2

depositing as gate insulator, and patterning photo resistance, a 200-nm thick layer of SiO_2 as isolation layer was deposited by LPD selectively. Source and drain regions were defined through the photo lithography process followed by e-beam evaporation of a 20-nm thick layer of Ti as an adhesion layer and a 100-nm thick layer of Pt as a contact material. Later, the wafer was then immersed in acetone to lift-off the photo resist and to form the source/drain regions. The samples after S/D patterning were treated with 3 minute IPA clean and 5 minute D.I water clean. Next, oxide surfaces were treated with hexamethyldisilazane (HMDS) to improve the adhesion between the polymer chain and the oxide surface. P3HT of 0.3 wt.% dissolved in chloroform was deposited by the spin-coating method to form the active layer. P3HT solution was filtered by a 0.2-μm pore-size PTFE filter and then spun onto the wafer surface. The detail spin-coating parameters is: 200RPM for 10s, 500RPM for 25s and 2000RPM for 25s. Finally, the sample was cured at 120℃ for 3 minutes. Before measuring electric characteristics, the sample was stored in vacuum for 2 days to let the oxygen atoms out-diffuse. The electric characteristics of OTFTs were measured by HP4156.

2.5 Electrical Characteristics of OTFTs based on P3HT

2.5.1 Measurement

Current-voltage characteristics of OTFT were measured in the air with a semiconductor parameter analyzer HP4156. All measurements were carried out in an electrically shielded box. The drain-source current, I_{DS}, was measured as a function of the drain-source voltage, V_{DS}, to observe FET-like characteristics. And I_{DS} was also measured as a function of the gate voltage, V_G, at small drain-source voltage, which was constructed to determine the gate bias modulation of the FET conductive channel.

Three parameters were extracted from the experimental I-V curves: (1) threshold voltage (V_T), (2) current modulation (the ratio of the current in the accumulation

mode over the current in the depletion mode, also referred to as ON-OFF current ratio), and (3) field effect mobility (μ). The detail extraction method will be discussed in the following section.

2.5.2 Threshold Voltage and OFF Current Definition

Inorganic semiconductors, such as Si or Ge, can be operated in three modes: depletion mode, accumulation mode, and inversion mode. For organic semiconductors such as OTFTs based on P3HT, they can not be operated in the inversion mode. Therefore, OTFTs based on P3HT were turned ON in the accumulation mode (V_G<0, see Fig1-5(b)) and were turned OFF in the depletion mode (V_G>0, see Fig1-5(c)).

Because OTFTs based on P3HT are normally ON devices, we defined that when the current is smaller than a certain value, it was called OFF-current. The corresponding gate voltage (V_G) was defined as threshold voltage (V_{th}). Therefore, we define the normalized off current (I_{OFF}) is 10^{-12} Amp and off current is I_{OFF} *W/L. The magnitude of off current with different channel length and different channel width is listed Table2-1

2.3.3 The Extraction Method of Mobility

OTFT based on P3HT is PMOS like FET. Therefore, the field effect mobility in the linear regime can be obtained by the calculation described below. At low drain voltage (V_D), source-drain current (I_{DS}) increases linearly with V_D (linear regime) and is approximately determined from the following equation (2-1):

$$I_{DS} = \frac{W}{L}\mu C_i (V_G - V_{th} - V_D/2)V_D \qquad \text{as } V_D << V_G - V_{th} \qquad \text{[Equation 2-1]}$$

where L is the channel length, W is the channel width, Ci is the capacitance per unit area of the insulating layer, V_{th} is the threshold voltage, and μ is the field effect mobility, which can be calculated in the linear regime from the transconductance,

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \frac{WC_i}{L}\mu V_D \qquad \text{[Equation 2-2]}$$

by plotting I_{DS} versus V_G at a constant low V_D, with $-V_D << -(V_G - V_T)$, and equating the value of the slope of this plot to g_m. We can compute the linear regime mobility from equation 2-2

2.6 Results and Discussion

2.6.1 Characteristics of LPD SiO_2

High frequency C-V curve of LPD SiO_2 in this experiment is shown in Fig 2-4. The heavy n-type doping results in Si substrate becoming degenerate n-type semiconductor, and high frequency C-V characteristics of LPD SiO_2 showed the M-I-M(metal-insulator-metal)-like properties. The dielectric constant of LPD SiO_2 is lower than 3.9 due to fluorine incorporated. The C/Cox is kept at a steady value from -40 V to 40 V and the dielectric constant is about 3.7 after conversion. Typical I-V curves of MOS capacitors with LPD SiO_2 as dielectric was shown in Fig 2-5. The leakage current density is about $20nA/cm^2$ at the electric-field of 4MV/cm. Comparing to that of PECVD SiO_2, the leakage current density of LPD SiO_2 is higher about one order.

2.6.2 Characteristics of OTFTs with LPD SiO_2 as gate insulator

The gate leakage current of OTFTs with LPD SiO_2 and PECVD SiO_2 are shown in Fig 2-6,wich are calculated by subtract measured drain current I_D and source current I_S. The profile is dissymmetrical because P3HT film is a normally-on semiconductor. When applying positive bias, charge will reject form the interface between the insulator and P3HT. Then the depletion region will form and the gate leakage area is only the patterned source/drain region as shown in Fig 2-7(a). When a negative bias is applied to the gate electrode, the voltage is dropped over the insulator and over the semiconductor near insulator/semiconductor interface and accumulates more positive charge in the accumulation region. The accumulation positive chare

region will form the additional gate leakage path and enlarge the gate leakage area as shown in Fig 2-7(b). Gate leakage current at the negative gate bias is larger than at positive gate bias at the same voltage value. Comparing to OTFTs with PECVD SiO_2 as gate insulator, the gate leakage current of OTFTs with LPD SiO_2 is larger about two order at -30V and only 2 times at +30V. The quality of gate insulator determines the magnitude of gate leakage current at negative gate bias. At positive gate bias, the interface state between P3HT and insulator and the defect in the insulator will affect the gate leakage current greatly because of the large leakage area. The area of gate leakage will dominate the magnitude of gate leakage current in negative gate bias. The importance of gate insulator quality is relatively slight in this condition, so the gate leakage current of OTFTs with LPD SiO_2 is only 2 times larger than that with PECVD SiO_2 at negative bias.

The transfer characteristics I_S-V_G of OTFTs with LPD SiO_2 and PECVD SiO_2 as gate insulator is shown in Fig 2-8. We can find the gap of driving current I_S is large at -30V gate bias, but it reduces greatly when applying gate electrode of 30V. When applying negative bias at gate electrode, the device is operated at off-state and the slight driving current I_S will be affected enormously by the gate leakage current. The poorer quality of LPD SiO_2 results in the large off-state leakage current and huge power consumption. When the device is operated at on-state, the effect of gate leakage current is relatively smaller because of the large driving current. Although the gate leakage current is great larger when applying positive gate bias, the increase rate of gate leakage current comparing to that of driving current is negligible.

The field-effect mobility of OTFTs with LPD SiO_2 is 1.8×10^{-3} and I_{ON}/I_{OFF} is 9.5×10^{3} respectively. Comparing to OTFTs with PECVD SiO_2, the value of OTFTs with LPD SiO_2 as gate insulator is slightly increased due to gate leakage current.

2.6.3 Characteristics of OTFTs with LPD SiO_2 as gate insulator and isolation layer

The gate leakage current of OTFTs with and without LPD SiO_2 as isolation layer is shown in Fig 2-9. We can easily find that gate leakage current is reduced about one order because of the additional isolation dielectric layer. The reduction of gate leakage current when applying negative bias to gate electrode and device operated at depletion mode, as shown in Fig 2-7(a), is attributed to the thicker isolation dielectric layer between source/drain metal and gate electrode. When applying positive bias to gate electrode, the gate leakage path is not only the isolation dielectric layer between source/drain metal and gate electrode but also accumulation layer area through the thin gate oxide between accumulation layer and gate electrode. The thick isolation dielectric layer reduces the leakage current by thicker dielectric thickness states forward. The other role played by isolation dielectric layer is modification of electric field distributed between source/drain metal and the semiconductor channel and thereby enhancing charge injection. The additional layer redistributes the electric field falling on the semiconductor near the area connecting to gate electrode.

The output characteristics I_S-V_G of OTFTs with and without LPD SiO_2 as isolation layer is shown in Fig 2-10. The off-state leakage current is reduced about one order by the additional isolation dielectric layer. The smaller on-state driving current of OTFTs with isolation dielectric result from not only reduced gate leakage, but also isolation dielectric layer resulting in lager series resistance. The field-effect mobility of OTFTs with isolation dielectric layer is 1.5×10^{-3} and I_{ON}/I_{OFF} is 6.34×10^{3} respectively. Those data including field-effect mobility, off-state leakage current and I_{ON}/I_{OFF} were summarized in Table 2-2. We can find the additional isolation dielectric structure effectively reduces the off-state leakage current but still shows larger off-state leakage current than OTFTs with PECVD SiO_2 as gate insulator. The larger series resistance of OTFTs with additional isolation dielectric structure results in slightly lower field-effect mobility and I_{ON}/I_{OFF} than that with PECVD SiO_2 as gate

insulator. The output characteristics I_S-V_D of OTFTs with and without LPD SiO_2 as isolation layer is shown in Fig 2-11and Fig 2-12. The other reason reducing on current is extra channel due to isolation dielectric layer. The lower dielectric constant (k~3.7) is also a parameter affecting the performance of OTFTs but not conspicuous in this experiment due to the gate leakage current effect.

2.7 Summry

We developed a new process for OTFTs with LPD SiO_2 as gate insulator. The advantage of this process includes low temperature process, large area application, inexpensive apparatus, and good insulator quality. The gate leakage properties of OTFTs are investigated and discussed. The performance of OTFTs with LPD SiO_2 as gate insulator is useable and the field-effect mobility is 1.8×10^{-3}, I_{ON}/I_{OFF} is 9.5×10^{3} ,which is comparable to OTFTs with PECVD SiO_2 as gate insulator. The off-state leakage current of OTFTs with LPD SiO_2 as gate insulator is relatively large and need to be improved further.

Next, we deposit a thick isolation dielectric layer under the source/drain region to reduce the gate leakage current. The LPD method can save one lithography process when fabricate this device due to selective deposition property. The OTFTs with isolation dielectric structure can reduce the gate leakage current and off-state current about one order in magnitude. The field effect mobility of OTFTs with isolation dielectric is 1.5×10^{-3} and I_{ON}/I_{OFF} is 6.4×10^{3}. Because of lager series resistance and extra channel , the field-effect mobility and I_{ON}/I_{OFF} is slightly lower than that with PECVD SiO_2.

The process of OTFTs with LPD SiO_2 as gate insulator and isolation dielectric layer is developed. It provided a solution to fabricate the OTFTs on plastic, clothes and paper substrate.

Stacked isolation dielectric layer under source/drain region can reduce the gate leakage current but shows lower field-effect mobility and I_{ON}/I_{OFF}. It can be optimized by adjusting the thickness of gate insulator and isolation dielectric. The structure of stacked isolation dielectric under source/drain region of OTFTs is similar to the LDD structure of conventional MOSFETs that can reduce leakage but increase series resistance and channel length. This structure which maybe can raise the reliability of OTFTs needs further work to investigate.

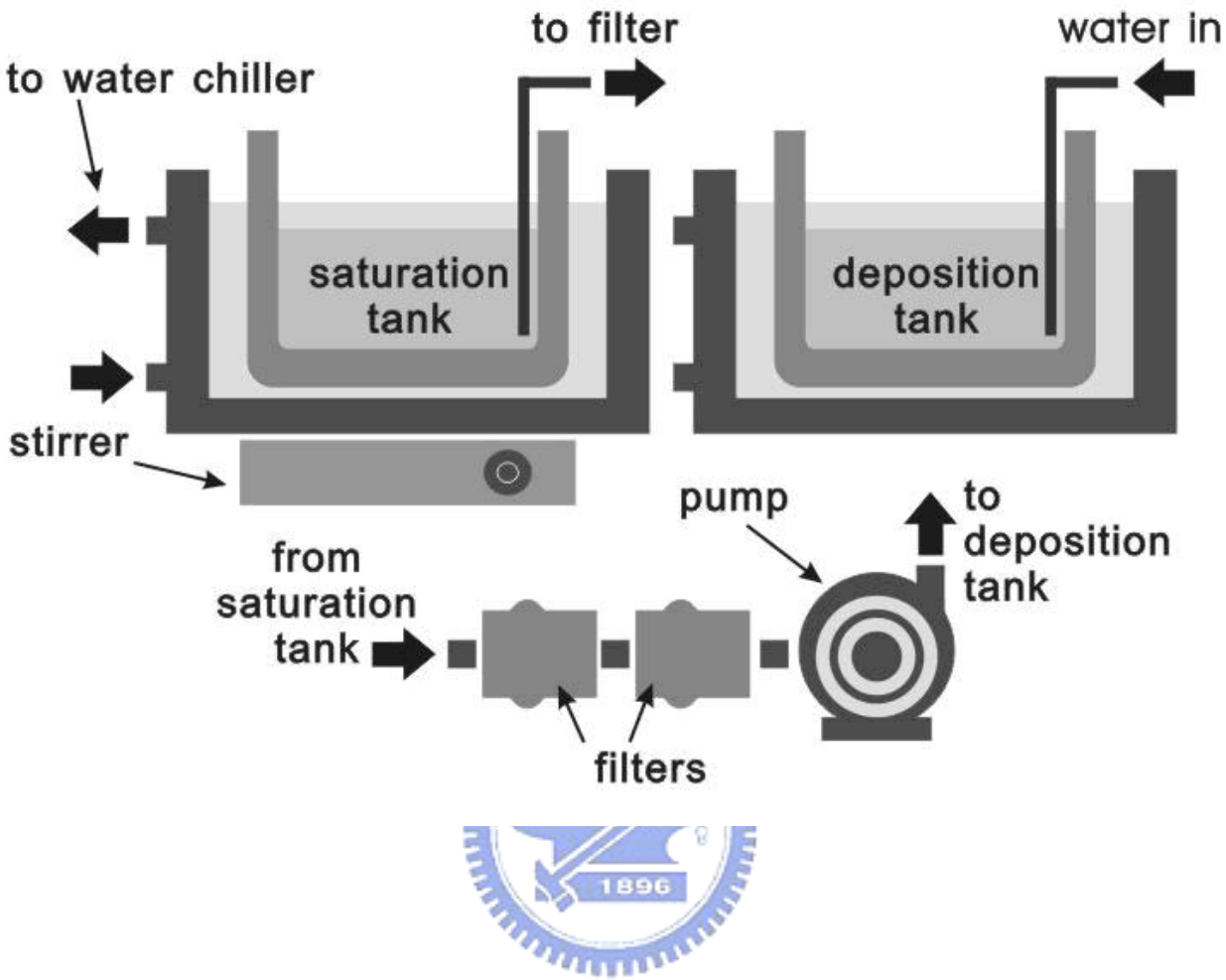


Figure 2-1 The schematic diagram of the apparatus for LPD

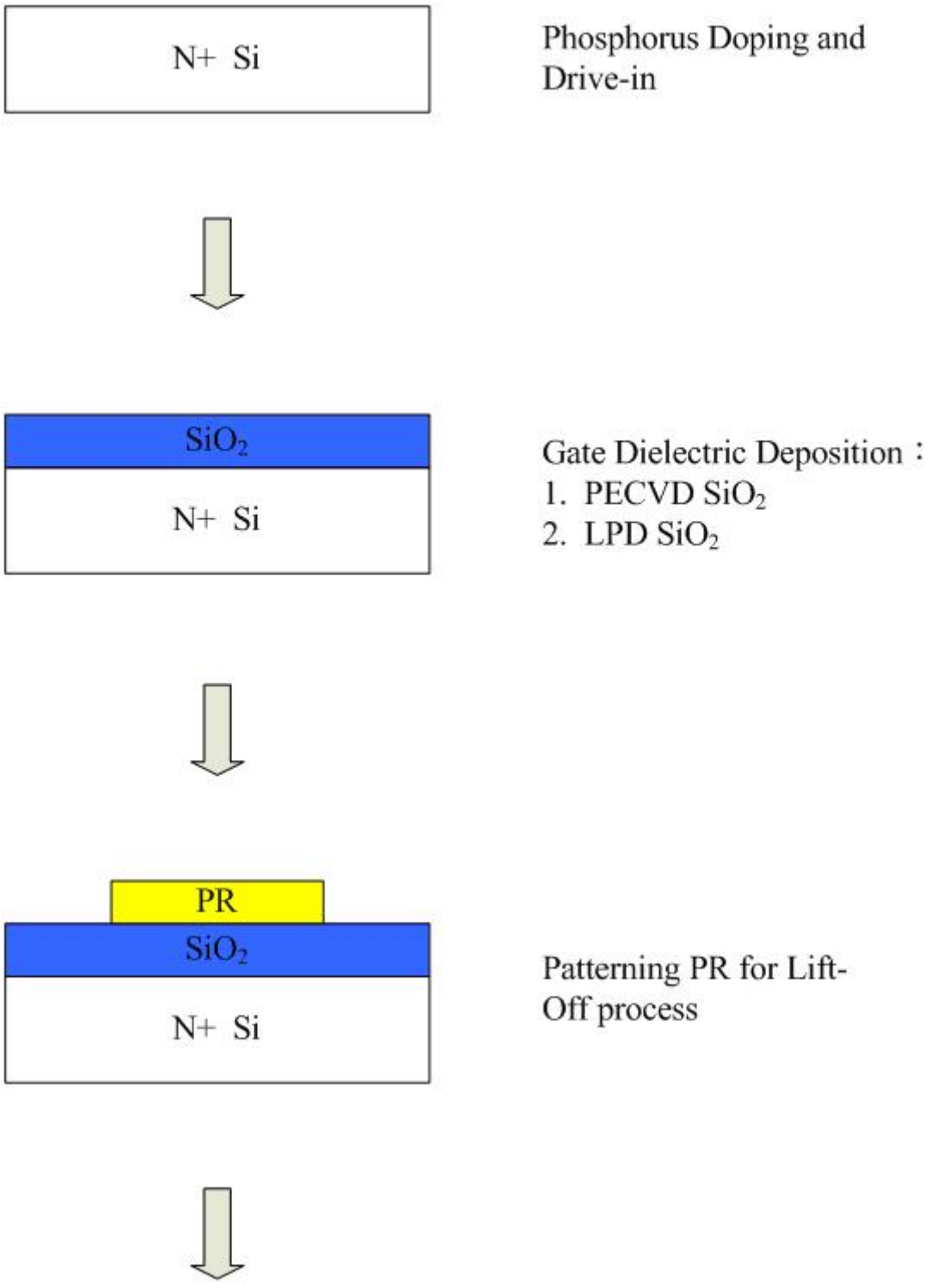


Figure 2-2 Process flow of OTFTs based on P3HT with SiO_2 as gate insulator by PECVD and LPD.(continue)

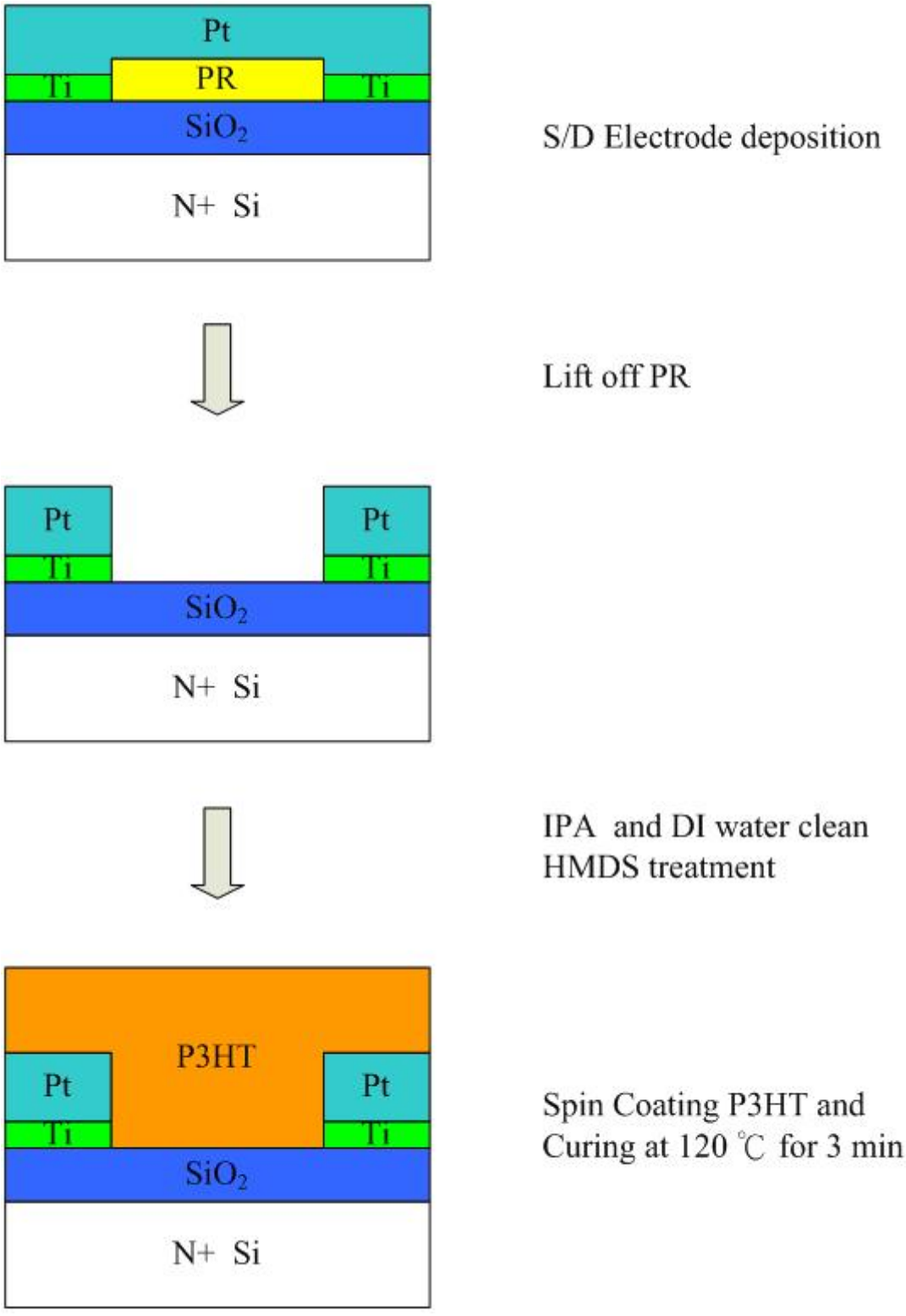


Figure 2-2 Process flow of OTFTs based on P3HT with SiO_2 as gate insulator by PECVD and LPD.

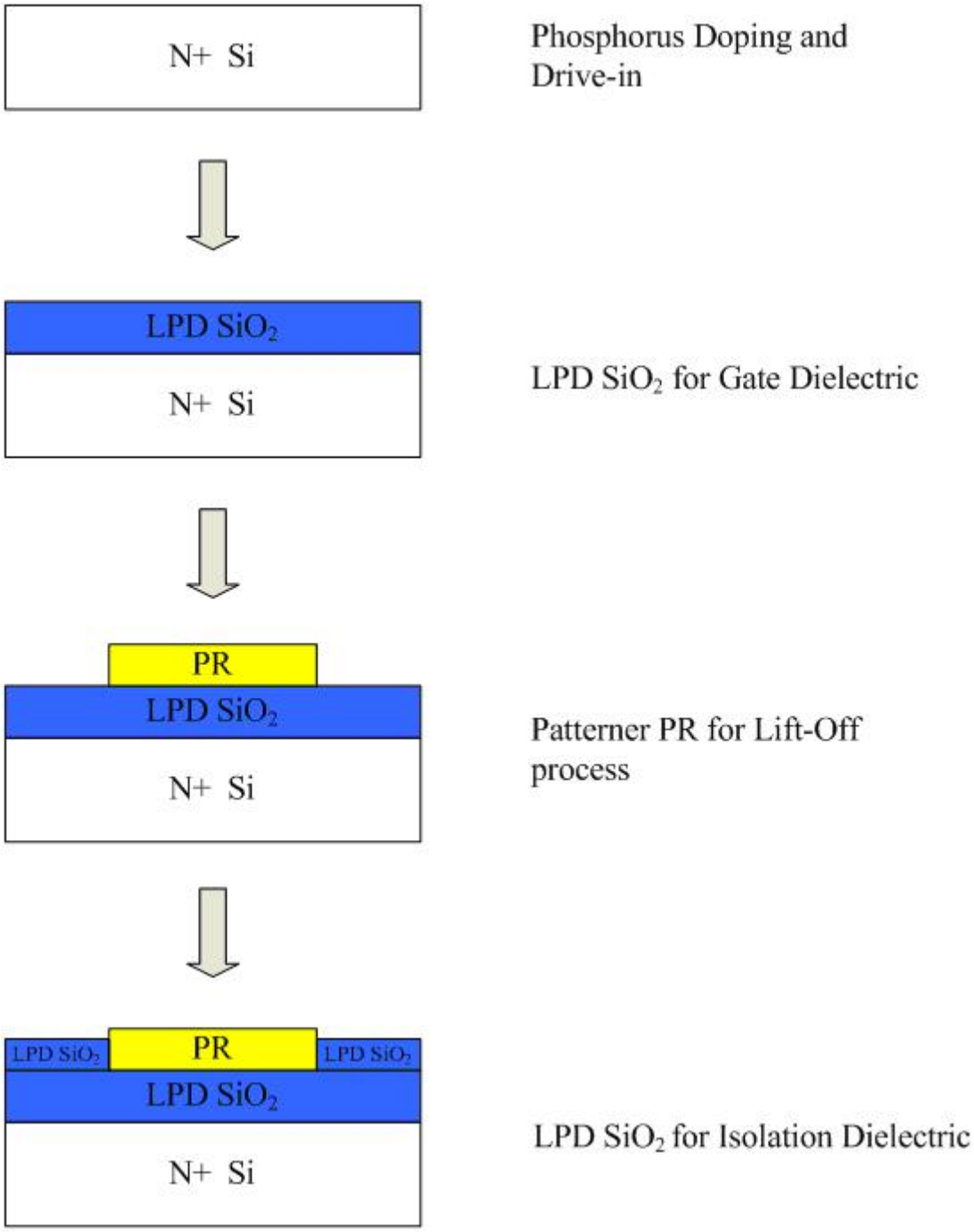


Figure 2-3 Process flow of OTFTs based on P3HT with SiO_2 as gate insulator and isolation layer by LPD.(continue)

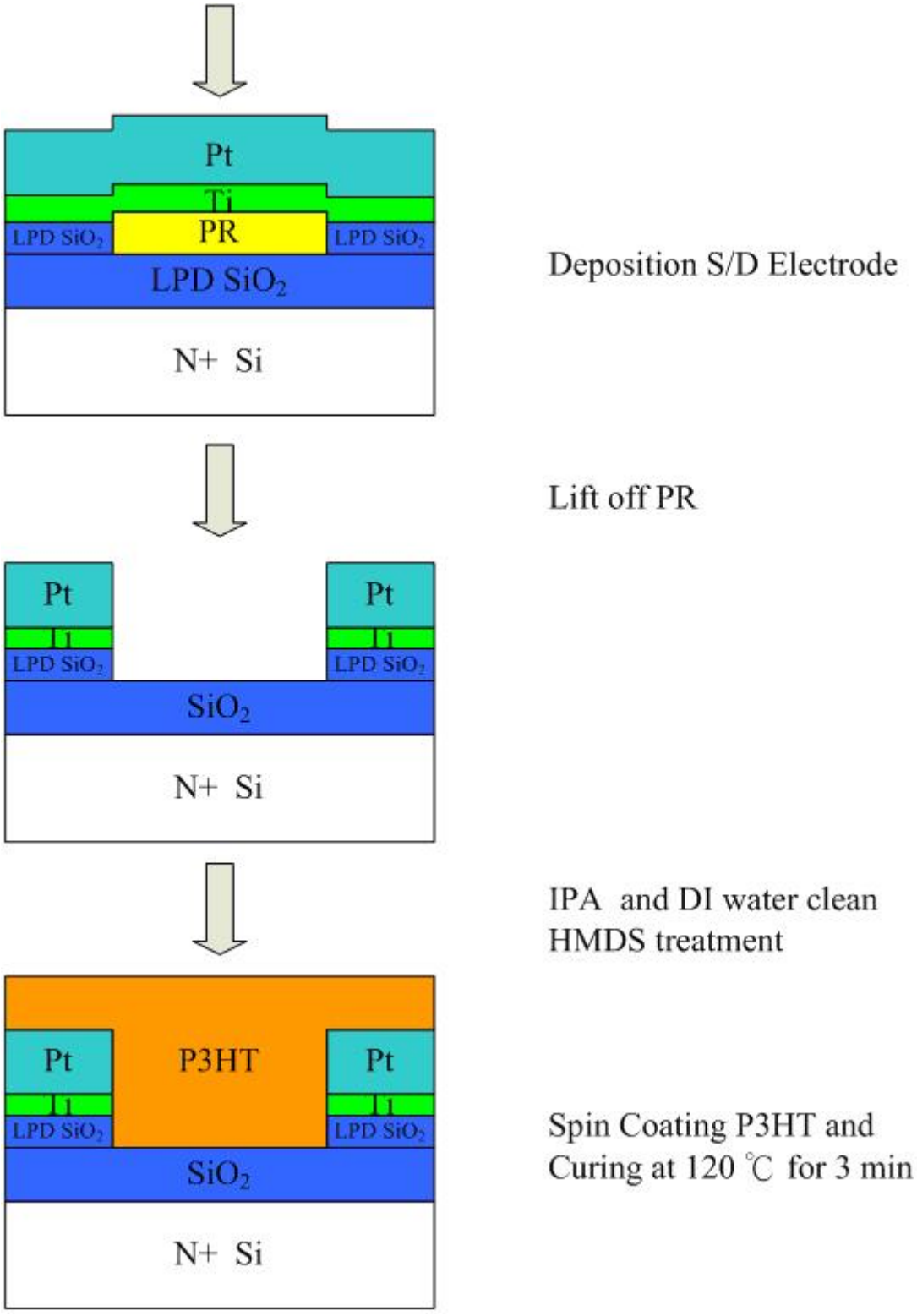


Figure 2-3 Process flow of OTFTs based on P3HT with SiO_2 as gate insulator and isolation layer by LPD.

W/L	I_{NO}(Amp)	I_{OFF}(Amp)
W/L=10000/10 μm	1×10^{-12}	1×10^{-9}
W/L=5000/10 μm	1×10^{-12}	5×10^{-10}
W/L=1000/10 μm	1×10^{-12}	1×10^{-10}
W/L=1000/15 μm	1×10^{-12}	6.6×10^{-11}
W/L=1000/25 μm	1×10^{-12}	4×10^{-11}
W/L=1000/35 μm	1×10^{-12}	2.8×10^{-11}
W/L=1000/50 μm	1×10^{-12}	2×10^{-11}
W/L=500/10 μm	1×10^{-12}	5×10^{-11}
W/L=500/15 μm	1×10^{-12}	3.3×10^{-11}
W/L=500/25 μm	1×10^{-12}	2×10^{-11}
W/L=500/35 μm	1×10^{-12}	1.4×10^{-11}
W/L=500/50 μm	1×10^{-12}	1×10^{-11}
W/L=300/35 μm	1×10^{-12}	8.5×10^{-12}

Table2-1 The magnitude of I_{OFF} with different channel length and different channel width

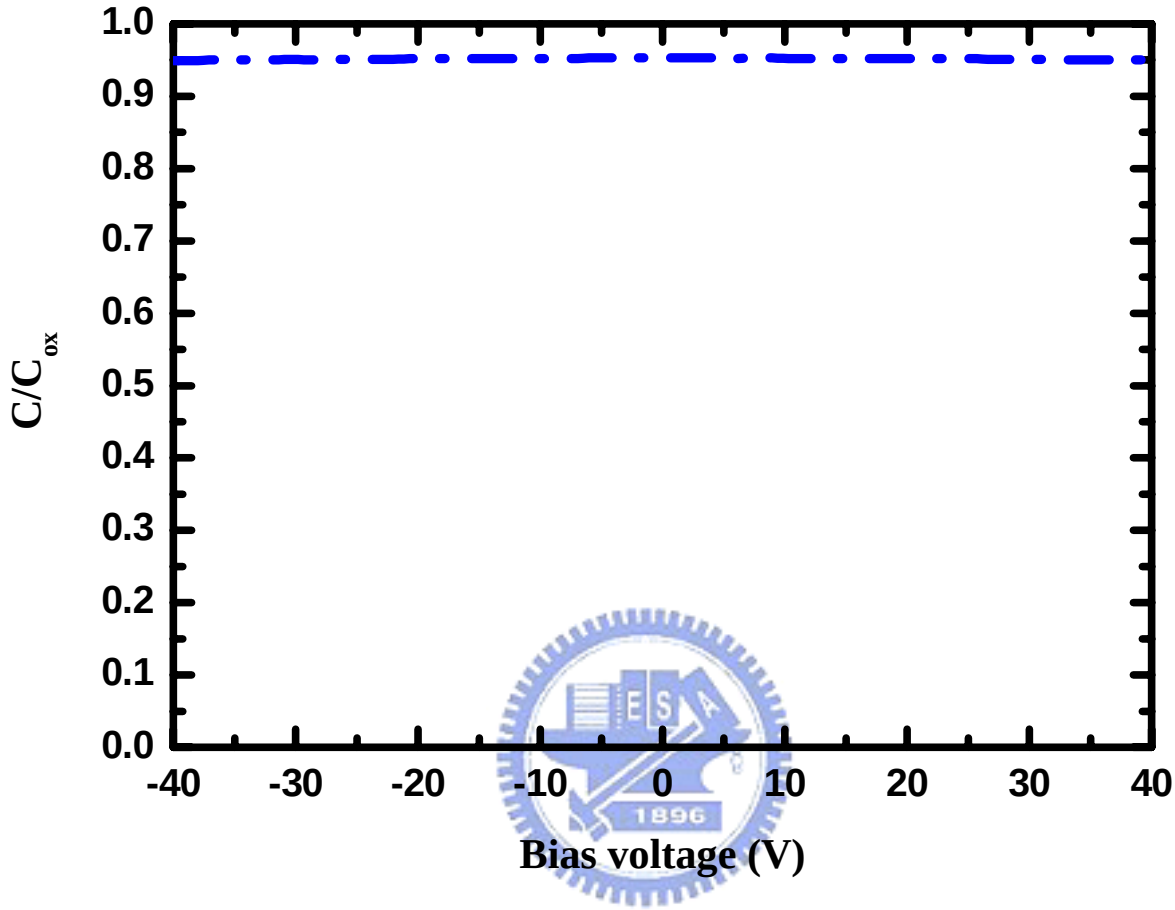


Figure 2-4 High frequency of C-V curve of LPD SiO_2

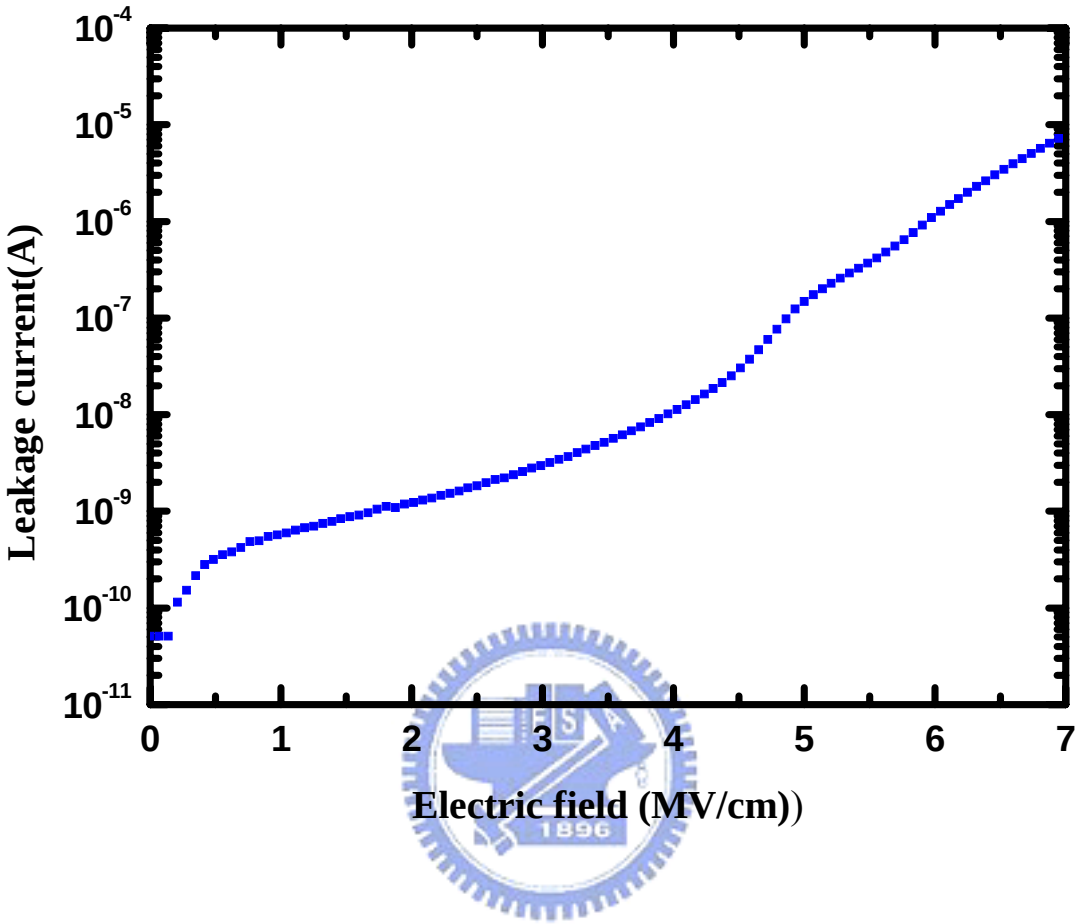


Figure 2-5 I-V curve of MOS capacitors with LPD SiO_2

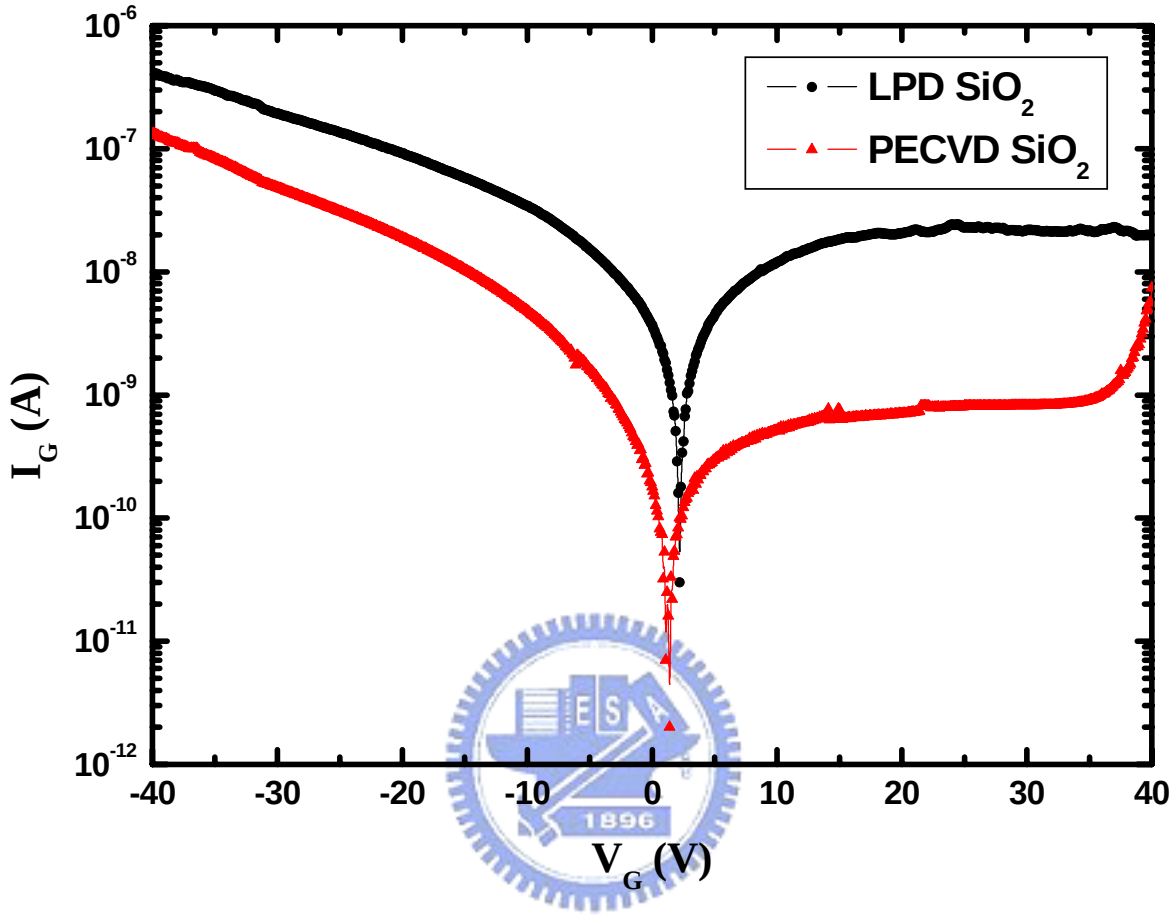
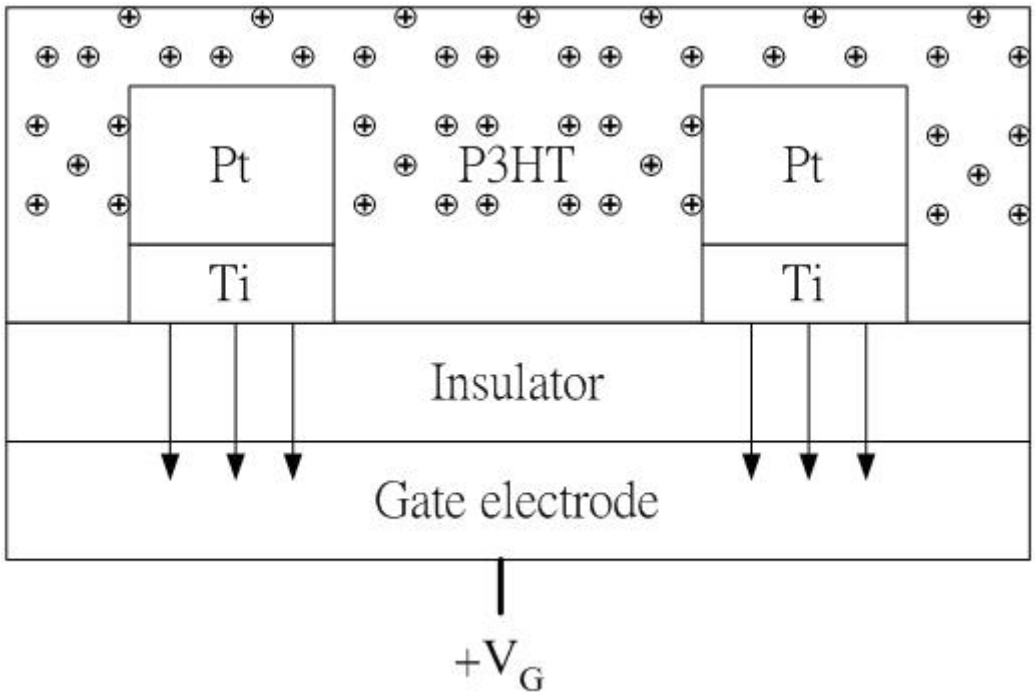


Figure 2-6 Gate leakage current of OTFTs based on P3HT with LPD SiO_2 amd PECVD SiO_2

(a)



(b)

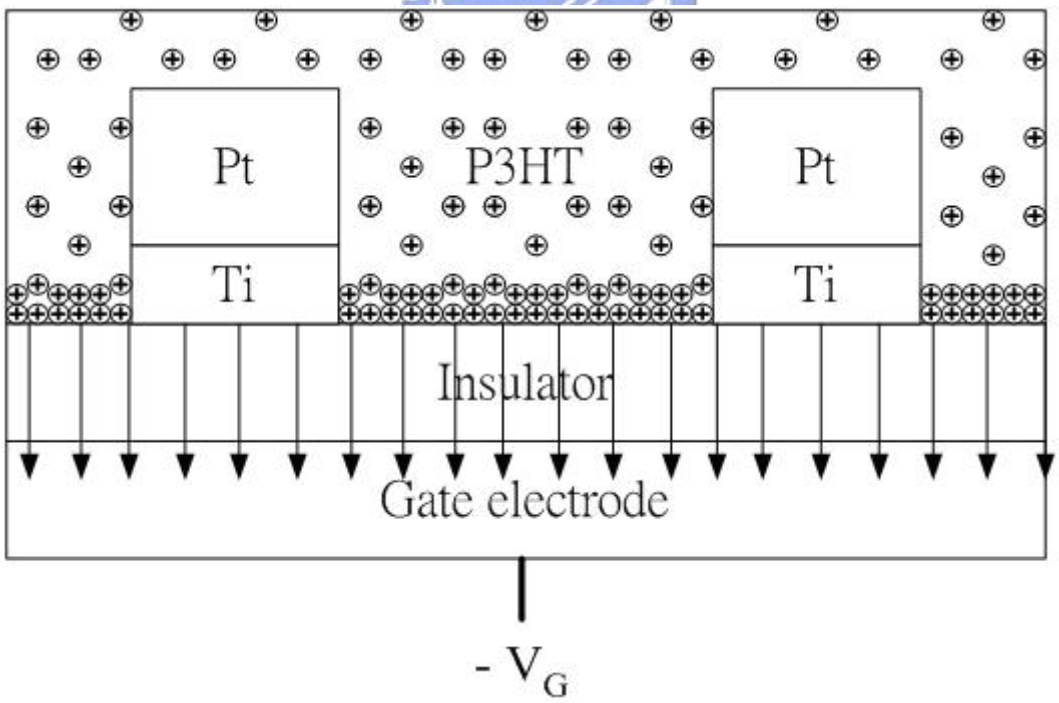


Figure 2-7 Gate leakage path of OTFTs at (a)positive gate bias (b) negative gate bias.

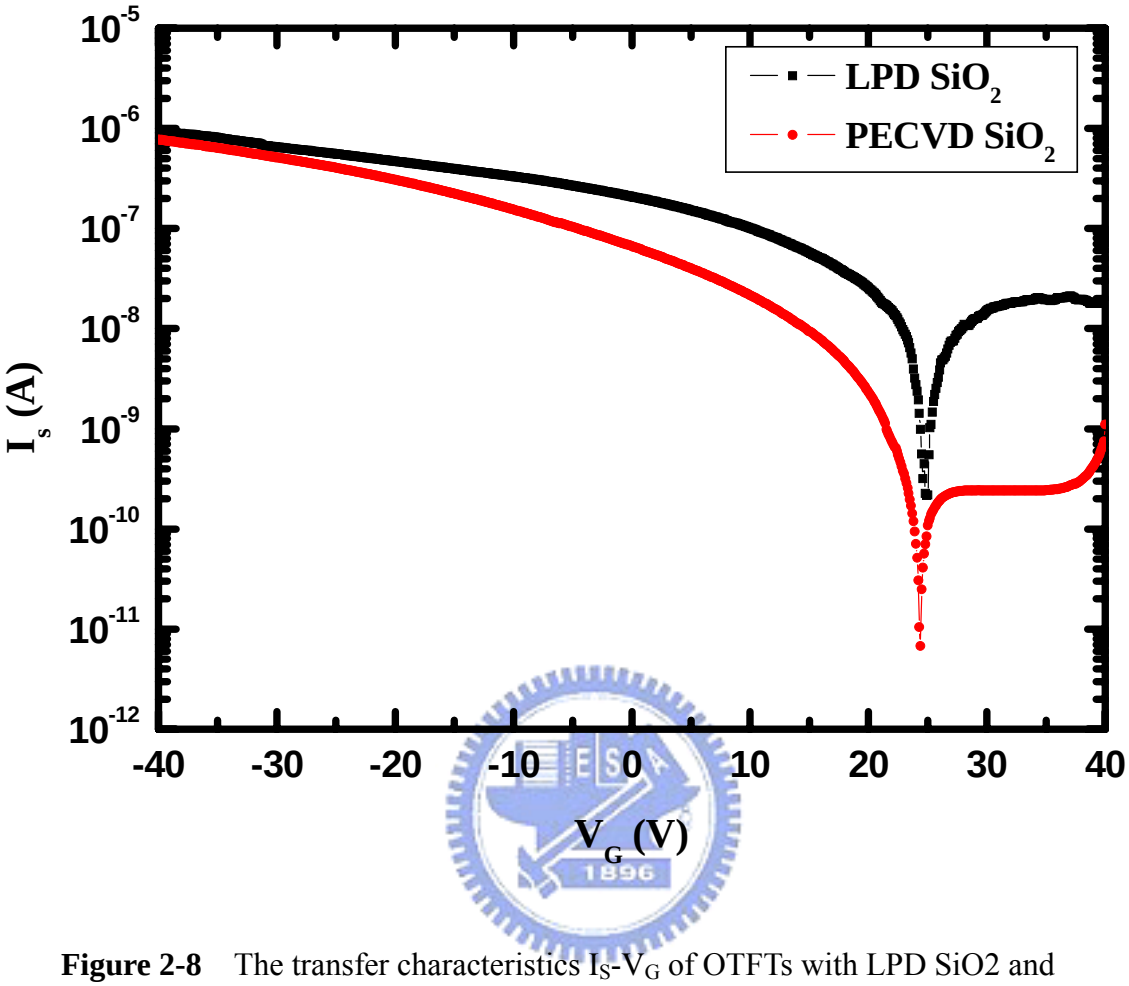


Figure 2-8 The transfer characteristics I_S-V_G of OTFTs with LPD SiO2 and PECVD SiO2 as gate insulator

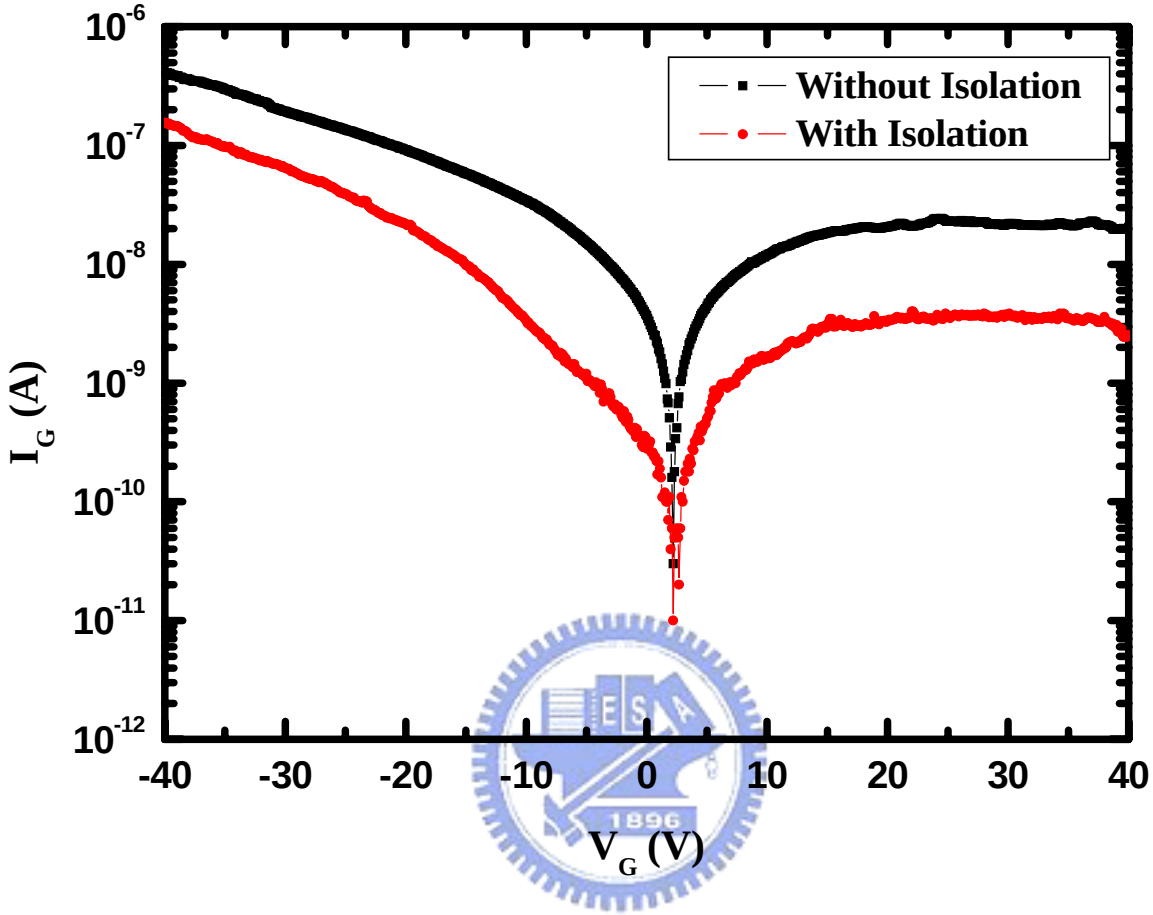


Figure 2-9 The gate leakage current of OTFTs with and without LPD SiO2 as isolation layer

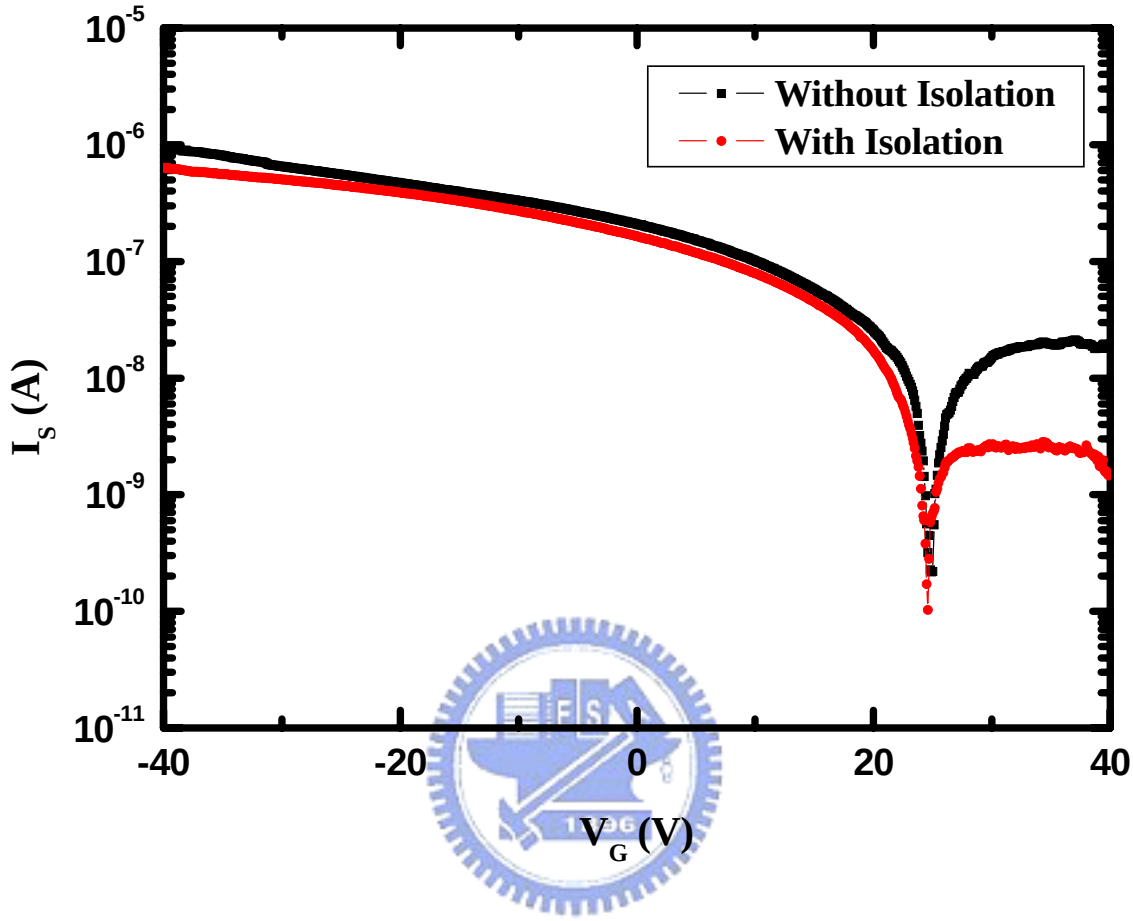
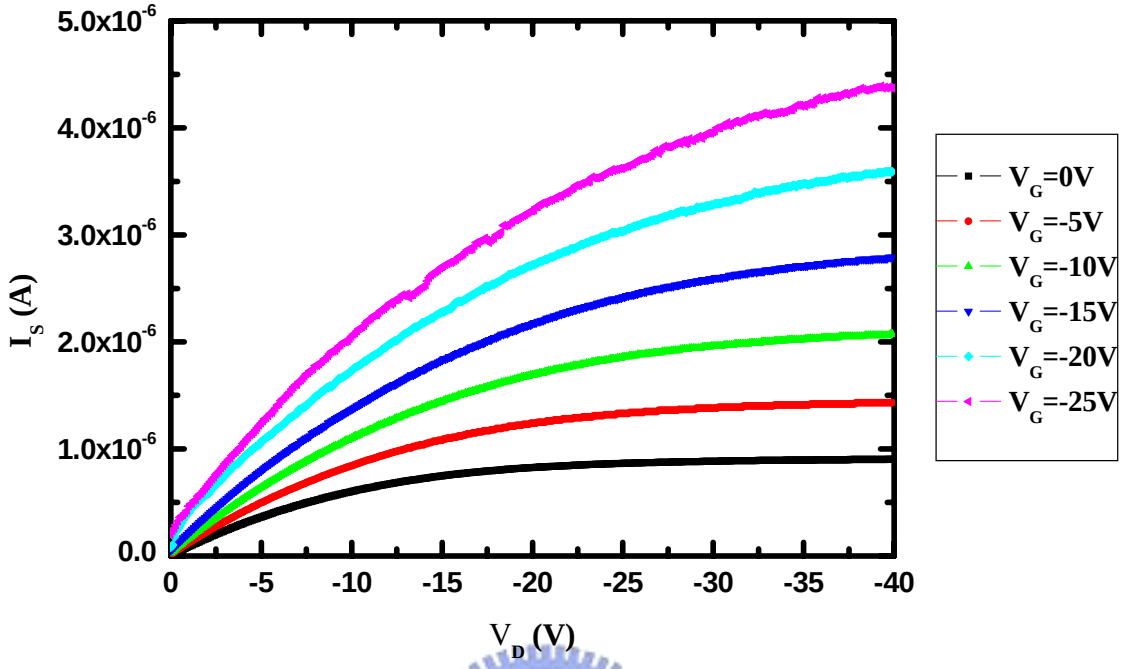


Figure 2-10 The output characteristics I_S-V_G of OTFTs with and without LPD SiO_2 as isolation layer

(a)



(b)

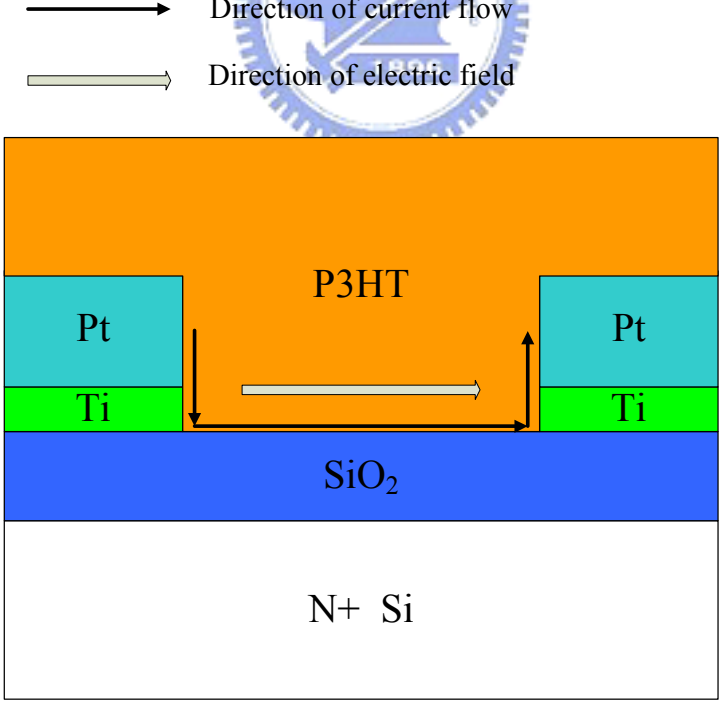
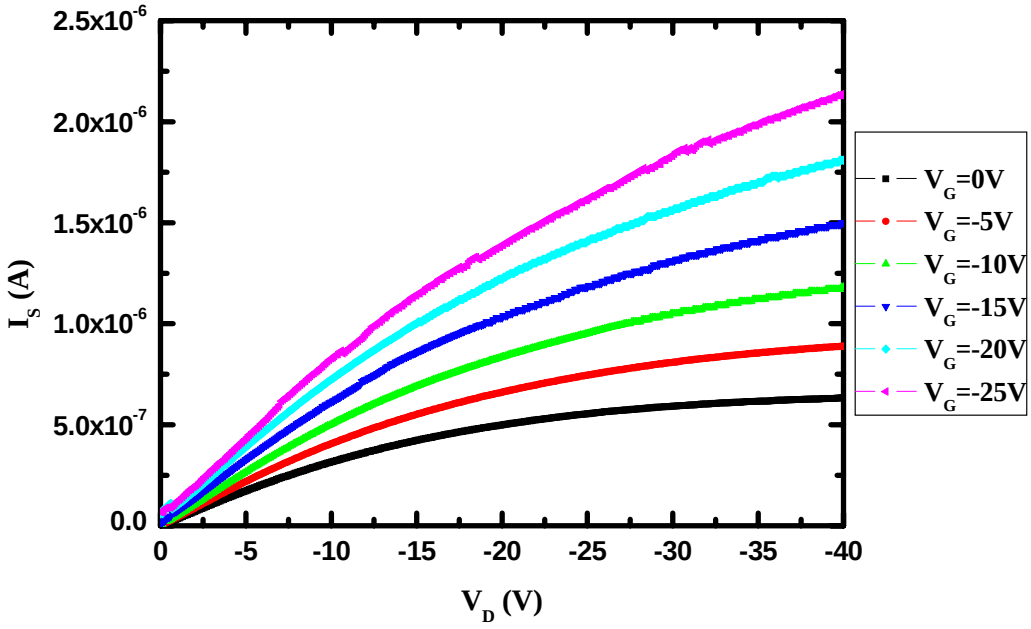


Figure 2-11 (a) The output characteristics I_S-V_D of OTFTs without isolation layer (b)current path of OTFTs without isolation layer

(a)



(b)

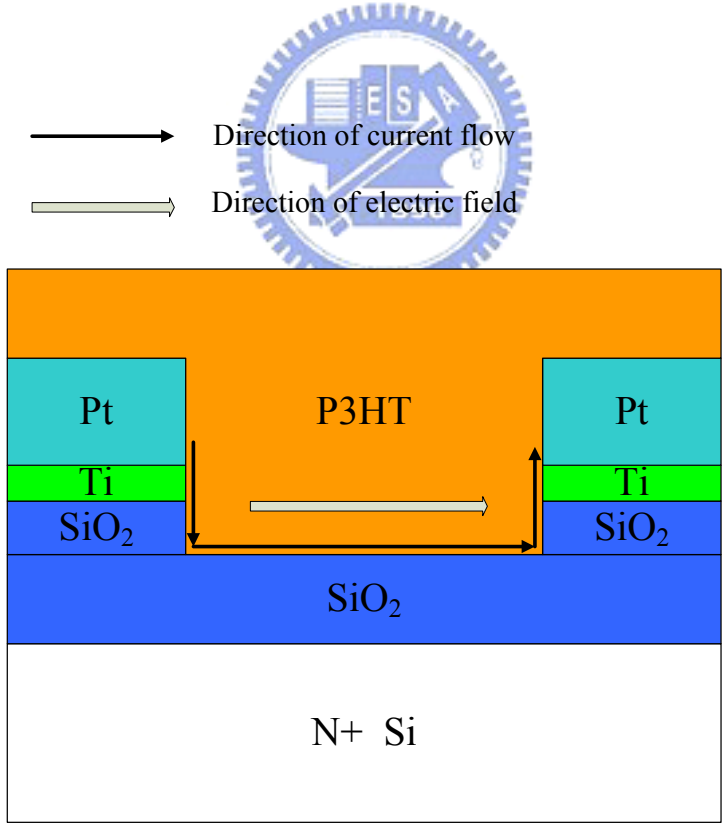


Figure 2-12 (a) The output characteristics I_S-V_D of OTFTs with LPD SiO_2 as isolation layer (b)current path of OTFTs with isolation layer

	PECVD SiO_2	LPD SiO_2	LPD SiO_2 with isolation
Mobility (cm/V-s)	1.6×10^{-3}	1.8×10^{-3}	1.5×10^{-3}
I_{ON}/I_{OFF}	7.8×10^{3}	9.5×10^{3}	6.4×10^{3}
Off state leakage	8.4×10^{-10}	2×10^{-8}	2.6×10^{-9}

Table 2-2 Field-effect Mobility, Off state leakage and I_{ON}/I_{OFF} of OTFTs with PECVD SiO_2, LPD SiO_2 and LPD SiO_2 with isolation dielectric layer.