Chapter 4

Conclusion and Future work

4.1 Conclusions

The feasibility study of Spin-Coating technique, physical and the electrical characteristics of P3HT OTFT are investigated. Here, we conclude our study into two parts: Low Temperature Process of OTFTs with LPD SiO_2 as Gate Insulator and Plasma Treatment Effects On OTFTs.

4.1.1 Low Temperature Process of OTFTs with LPD SiO_2 as Gate Insulator

We applied a new process of OTFTs with LPD SiO_2 as gate insulator. The advantages of this process include low temperature process, large area application, inexpensive apparatus, good oxide quality. The gate leakage property of OTFTs were investigated and discussed. The performance of OTFTs with LPD SiO_2 as gate insulator is useable and the field-effect mobility is 1.8×10^{-3}, I_{ON}/I_{OFF} is 9.5×10^{3} , which is comparable to OTFTs with PECVD SiO_2 as gate insulator. The off-state leakage current of OTFTs with LPD SiO_2 as gate insulator is relatively large and needs to be improved further.

Next, we deposited a thick isolation dielectric layer under the Source/Drain region to reduce the gate leakage current. The LPD method can save one lithography process because of selective deposition property to fabricate this device. The OTFTs with isolation dielectric layer can reduce the gate leakage current and of-state current about one order in magnitude. The field-effect mobility of OTFTs with isolation dielectric layer is 1.5×10^{-3} and the I_{ON}/I_{OFF} is 6.4×10^{3}. Because of lager series resistance and extra channel length, the field-effect mobility and I_{ON}/I_{OFF} is slightly lower than that with PECVD SiO_2 as gate insulator. The process of OTFTs with LPD SiO_2 as

gate insulator and isolation dielectric layer was developed. It provided a solution to fabricate the OTFTs on plastic, clothes and paper substrate. Stacked isolation dielectric under Source/Drain region can reduce the gate leakage current but lower the field-effect mobility and I_{ON}/I_{OFF}. It can be optimized by adjusting the thickness of gate insulator and isolation dielectric layer. The structure of stacked isolation dielectric under Source/Drain region of OTFTs is similar to the LDD structure of conventional MOSFETs. It can reduce leakage but increase series resistance and channel length. This structure which maybe improve the reliability of OTFTs needs further work to investigate.

4.1.2 Plasma Treatment Effects on OTFTs

The performance of OTFTs is closely related to the surface of gate insulator because the active layer as channel is the interface of SiO_2/P3HT. Various methods have been investigated to improve the performance of OTFTs by modification of surface state. Not alike HMDS which can enhance the adhesion of P3HT onto SiO_2, plasma treatments can remove residual contaminant and decrease the interface charges. In our experiments of plasma treatment, we found OTFTs with plasma treatments showed better performance than those with HMDS treatment. We also got the optimum condition for OTFTs with O_2 plasma treatment for 5 min. Under the optimum condition, the mobility and threshold voltage of OTFTs are 0.042 cm^2/V-s and 57 V respectively.

4.2 Future work

4.2.1 A new method to deposit P3HT thin film

There are three methods to deposit P3HT thin films: (1) spin-coating (2) dip-coating (3) drop-casting. In our experiment, we made use of spin-coating method to deposit P3HT thin films and obtained optimized deposition parameters for fabricating P3HT thin films. However, among the three methods to deposit P3HT thin films, the best method is drop-casting. Therefore, in the

future we will make use of drop-casting to deposit P3HT thin films, and study the deposition parameters of drop-casting.

4.2.2 Thermal stability of P3HT OTFTs

In addition to investigations of device lifetime and stability of P3HT in different environments, thermal stability is another important topic for OTFTs. First, poly (3-hexylthiophenes) devices will be likely exposed to elevated temperatures during the fabrication process, due to the annealing requirements of other layers. Second, thermal cycling studies provide crucial insights into device lifetime and stability. [4.1]

4.2.3 An in-situ pacivation layer for protecting the P3HT film

From our experimental results, P3HT OTFTs are sensitive to ambient conditions. Protection from the environment by encapsulation is critical to the stability of P3HT OTFTs. Therefore, using a suitable material as pacivation to protect P3HT film from environmental effect is another important topic.

4.2.4 New gate insulator materials for P3HT OTFTs

From the performance point of view, the most important parameters are charge carrier mobility, ON-OFF current ratio and the operational voltage range. However, the operating voltages of P3HT OTFT required to produce such performance were impractically high, around 50~60V. Although decreasing the thickness of SiO_2 could reduce the operating voltages of P3HT OTFT, the gate leakage current would increase with decreasing the thickness of SiO_2 and affect the performance of P3HT OTFT. Therefore, the use of high dielectric gate insulator materials is possible for reducing operating voltages of P3HT and gate leakage current. [4.2], [4.3], [4.4]