國　立　交　通　大　學

電子工程學系　電子研究所碩士班

碩　士　論　文

高功率元件-CoolMOS™ 的元件模擬與電性研究

A Study of Device Simulation and Electrical Properties for High Power Device-CoolMOS™

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中華民國 九十五年 九 月

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摘　要

本論文主要利用 ISE-TACD 的模擬軟體來探討 superjunction MOSFET (CoolMOS^{TM})功率元件的物理機制與電性討論。對於 Saturation 與 Quasi-saturation 發生時所以表現的電性現象利用 2D 的數理參數來加以解釋。同時對於 superjunction 所引入的 pillar 在慘雜濃度匹配與不匹配的情況下進一步探討電性的影響以及所誘發的物理機制。

在此研究中，不僅觀察到摻雜濃度對元件的電性有重大影響，也明顯看到 CoolMOS^{TM} 一些操作特性，例如，在低汲極電壓時快速 saturation 的發生與在高閘極電壓、汲極電流下的 Quasi-saturation 現象等。

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Abstract

This study simulates and discusses the superjunction MOSFET power devices (CoolMOS™) by means of ISE-TCAD simulator, which contains processing simulation, device simulation, and circuit integrated simulation. Saturation and Quasi-saturation occurring in the CoolMOS are also explanted by 2D physical parameters. At the same time, the doping concentration balance and imbalance in the pillar region affecting the electric characteristic and physic mechanism of the superjunction power devices are also be simulated and discussed.

In this paper, we can observe that the doping concentration has large influence on the device electric characteristics and CoolMOS operating phenomenon. For example, the saturation occurs in the low drain voltage and gate voltage, and the quasi-saturation is in the high gate voltage and drain current level.

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Chapter 1
Introduction

1.1 Overview of Power Devices

In the recent years, power devices have been developed with smart power technology and widely studied because of their potential application in automotive field, industrial segment, consumer segment, computer market, and car-radio field. Such as home automation network nodes, motors power supply bridge, dense energy control units, hard disk drivers, motherboards, and graphics cards etc [1]-[4].

There also have a wider range of applications through the use of SOI wafers with high frequency, high speed and high blocking voltage capabilities for radio frequency (RF) power amplifiers [5], plasma display panel (PDP) scan driver IC [6], and RF power supply [7]. Recently, there is a great interest to study the power integrated circuits (PICs) and high voltage thin film transistors (HVTFTs) in order to achieve the goals of system-on-a- chip (SOC) and system-on-a-panel (SOP)[8]-[10].

An ideal power device is difficult to be fabricated, because it is usually limited in the current conducting of the on-state and voltage blocking of the off-state in a number of ways. So, it is not surprising that no single device can support and cover all capability in power device applications, because there have wide requirements in the blocking

voltage, driving current, and switching speed.

Additionally, the cost and complexity will significantly determine the device performance in the overall circuit and focus a particular application aspect like device types, control, and protective circuitry function. Thus, designers will only depend on their need to design the device and frequently the cost and physical size restrict the device usefulness. The power device will be designed with the limited performance and only can work in some fields of function.

Designers try to enhance the blocking voltage by modified junction arrangement and develop new devices to overcome some limitation in previous device types using novel structures or materials. The advent material—such as silicon-carbon (SiC) can provide the high voltage, high frequency, and high temperature robustness for power devices [11]-[15]. But, the power devices are still widely fabricated with the material of silicon (Si) because that can achieve the excellent compromise among the semiconductor properties, material cost, and easy fabrication in today foundry.

1.2 Silicon Power Switching Devices

Faster switching characteristics for low-medium power levels can be obtained using bipolar junction transistors (BJTs) or metal oxide semiconductor field effect transistors (MOSFETs). Power electronic systems have benefited greatly during the past ten years from the revolutionary advance that have occurred in discrete power devices. The

power MOSFETs in the 1970s and the insulated gate bipolar transistors (IGBTs) in the 1980s enabled design of very compact high-efficiency systems due to the greatly enhanced power gain resulting from the high input impedance of these structures [16].

Power metal oxide semiconductor field effect transistors (MOSFETs) have evolved from MOS integrated circuit technology and have been developed to overcome performance limitations of BJTs. Such as, switching speed has been greatly increased and drive power requirements considerably reduced. The power MOSFETs are unipolar devices having an excellent forward biased safe operating area (FBSOA) and not liable to second breakdown. In order to make efforts towards optimizing the structure, design, and process, the double-diffused MOS (DMOS), V-shaped groove MOS (VMOS), U-shaped groove MOS (UMOS) and trench structures with improved specific on-resistance have been developed (Fig. 1.1). Although the power MOSFETs have lots of merits, they are not suitable for high voltage applications. The reason is that the power MOSFETs suffers from the rapid increase in specific on-resistance of the drift region in order to increase the breakdown voltage.

In 1982, a new device which combined bipolar and MOSFET technologies was introduced. The insulated gate bipolar transistor (IGBT) has the drive requirements of a power MOSFET combined with the voltage and current handling capabilities of the bipolar device [17]. The IGBT structure consists of a wide-base p-n-p transistor driven by an integrated short channel MOSFET (Fig. 1.2). This combination produces a very high power gain because of the high input impedance resulting from the MOS-gate structure, and the low no-state voltage drop resulting

from high level injection of minority carriers in the drift region. Additionally, the MOS-gate oxide insulates the gate electrode so that there is no power dissipation in the control gate. But, the switching speed is limited by the stored charge in the base region, which is generated from carrier injection, and this minority carrier lifetime will determine the turn-off time during the transient characteristics [18].

Recently, significant improvements in the performance of silicon power MOSFETs have been achieved by using innovative vertical structures with charge coupled region. Meanwhile, silicon IGBTs continue to dominate the medium and high voltage application space due to scaling of their voltage rating and refinements to their gate structure achieved by using very large scale integration (VLSI) technology and trench gate regions [19].

1.3 CoolMOS

CoolMOS is a novel power MOSFET with a “superjunction” for its drift region, which results in a vastly improved relationship between the on-resistance and breakdown voltage [20].

Power MOSFETs are commonly used as switches in power electronic circuits, and they should have minimal resistance when the device is conducting and sustain high voltage when it is off. For a higher breakdown voltage, power MOSFETs are usually fabricated as a vertical double-diffused structure with a lightly doped epitaxial drift layer to sustain the voltage. The breakdown voltage (V_B) of the device is

increased by reducing the doping concentration and increasing the thickness of the drift layer. However, this results in an increase of the on-resistance (R_{on}). It can be shown that R_{on} is proportional to $V_B^{2.5}$ [21], which means that increasing V_B will result in a significant increase in R_{on}, causing higher conduction losses. The CoolMOS is evolved from a conventional DMOS structure but it breaks the more than square law dependence in the case of standard DMOS with the linear voltage relationship in specific on-resistance. CoolMOS is a novel power MOSFET projected as the latest milestone in high-voltage MOSFET devices. In the CoolMOS, the drift region of the conventional DMOS is replaced by a "superjunction"—a combination of n^- and p^- strips in parallel (Fig. 1.3).

When the device is on, the n^- strip conducts the drain current. When it is off, a drain voltage (V_D) is applied, and it appear as a reverse bias between the n^- and p^- strips. A depletion region forms, and a relatively small value of V_D fully depletes the drift layer. Subsequently, the behavior of the drift region is similar to that of an intrinsic layer. For an example, based on the new device concept of charge compensation the R_{on} area product of 600 V transistor has been reduced by a factor of 5 [22].

CoolMOS shows no bipolar current contribution like the well known tail current observed during the off-state of the IGBTs. CoolMOS virtually combines the low switching losses of a MOSFET with the on-state losses of an IGBT. Moreover, while the donor and acceptor charge reach the balance state in their depletion regions, the superior breakdown voltage can be achieved well than any stat-of-the-art power

MOSFETs. Additionally, it also can be attempted to develop lateral superjunction structure into silicon-on-insulator (SOI) to increase their voltage blocking capability (Fig. 1.4) [23].

Chapter 2
Device Physics of the CoolMOS

2.1 CoolMOS in the Off-State

The behavior of the CoolMOS transistor in the off state is dominated by the characteristics of the superjunction drift layer. Here, first explain, with the help of simulation results, why the breakdown voltage is higher in the superjunction structure. We will then discuss how the doping density of the n^- and p^- strips can be chosen to achieve the minimum on resistance.

To understand how the superjunction drift layer improves the breakdown voltage in the CoolMOS transistor, the superjunction (SJ) is simulated here alone (i.e., without the MOS structure) and compare it with the drift region of a conventional power MOSFET, which is simply a lightly doped (LD) layer without any p-n junction. Fig. 2.1 shows the two simulated structures. The n^+ and p^+ contact regions are heavily doped ($N_d=N_a=3\times10^{19}cm^{-3}$), the n^- and p^- strips, and the n^- layer of the LD structure are lightly doped ($N_d=N_a=3\times10^{15}cm^{-3}$). The p^+ contact is grounded, and a positive voltage is applied to the n^+ contact. The superjunction structure was found to break down at 300 V, while the LD

structure could sustain only 130 V [24].

In Fig. 2.2, we have plotted the electric field for the LD structure. As this is effectively a one-dimensional (1-D) structure, there is no variation in the x direction. In Fig. 2.3, the net electric field for the SJ structure along the outer edge of the n^- strip is plotted. This field is also vertical because of symmetry. For the LD structure, the field profile is triangular, with constant slope, and advancing toward the n^+ contact, as the applied voltage increases. Note that, in this structure, the depletion region expands gradually as the voltage increases. For the SJ structure, on the other hand, the n^- and p^- strips become completely depleted (which is indicated by the field becoming nonzero) at a relatively low voltage, about 50 V for this example. The field profile for larger voltages retains its relatively flat shape, with steep variations only near the contacts.

The following two observations, along with the field profiles, will explain the superior V_B of the SJ structure: (i) The voltage difference between the contacts in both LD and SJ structures is simply the area under the field profiles plotted in Fig. 2.2 and 2.3. This is because the electric field is vertical in both the structures, as that has pointed out. (ii) For the SJ structure, the field is maximum at the junctions along the two edges (and these two values are equal in our device because of symmetry) [25]. Thus, in each of the two structures, LD and SJ, the breakdown voltage is simply the area under the field profile when the maximum field reaches a critical value. Now, looking at the shape of the field profiles, it is easy to see that V_B will always be higher for the SJ structure than that for the LD structure, because the area is larger in the SJ case.

When the height of the superjunction region was increased from 15 μm to 25 μm, without changing any other parameter, V_B increased from 300 to 500 V. The field profiles at breakdown for the SJ structure for these two heights are seen to coincide almost exactly for 15 μm (Fig. 2.4). Since R_{on} has also increased in the same proportion as the height of the SJ region, the linear relationship between R_{on} and V_B for the SJ structure has been proved by this result.

2.2 CoolMOS in the On-State

The on-resistance of the conventional high voltage Power MOSFET is dominated by the resistance of the voltage sustaining drift layer. The blocking capability of this region is determined by its thickness and the doping [26] [27]. In order to increase the blocking voltage the doping must be simultaneously reduced and the layer thickness increased. The resistance of the transistor therefore increases disproportionately strongly as a function of its blocking capability. Accordingly the drift layer causes over 95% of the total on-resistance in e.g. a 600V transistor [28]. The main emphasis in improving the transistors performance must therefore be directed towards reducing this drift region resistance.

CoolMOS in the on state, electrons flow from the source, under the gate electrode (i.e., through the MOSFET channel), through the drift region (i.e., the n^- part of the superjunction), to the drain terminal (Fig.

2.5). We can therefore consider the device to be made up of an “intrinsic” MOSFET and a drift region. We have simulated the device in the on state, by applying a positive bias to the gate. The transfer characteristics are similar to those of a conventional power MOSFET. The device turns on at the threshold voltage of the “intrinsic” MOSFET, and the current rises with V_G initially and saturates when the resistance of the drift region starts dominating. The characteristics saturate after a small increase in V_G (less than 1 V) in the simulated device, indicating a high drift region resistance, as compared to that of the intrinsic MOSFET.

The I_D–V_D characteristics show two distinct regimes (Fig. 2.6). For lower values of V_G, saturation in the conventional sense is observed; i.e., as V_D becomes high, the intrinsic MOSFET saturates. For higher values of V_G, the current does not saturate completely, but undergoes a “partial” saturation and rises slowly with V_D. It is also seen that, in this region, there is hardly any increase in the current with increasing V_G (between V_G = 10 V and 30 V). This implies that some mechanism other than the usual MOSFET saturation must be responsible for this “quasi” saturation of current at large gate voltages. The quasi-saturation was thought to be due to degradation of mobility, as the electric field increases [29] [30]. To test the validity of this conjecture, the device was simulated with a constant mobility, and it was found that saturation indeed ceases to occur in this condition. This confirms that quasi-saturation is related to mobility degradation. We can conclude from some study that at higher gate voltages, saturation of the I_D–V_D curve occurs due to velocity saturation in the drift region, first in the neck region, and then, at higher drain voltages, also in the pillar region. When quasi-saturation occurs, the

depletion region stops advancing further into the n^- region and the electron density in the n^- regions increases slightly above its equilibrium value.

The situation at lower gate voltages (e.g., V_G = 7.5 V for the simulated structure) is different. The saturation of the I_D–V_D curve in this case is caused by the usual saturation of the intrinsic MOSFET. When V_D was made more than 50 V, however, we observed that velocity saturation occurred in the drift region. As the intrinsic MOSFET is in saturation, this does not reflect on the I_D–V_D curve.

2.3 Analyses of the Drift pillar, the Current, and the Specific On-Resistance

The "pillar" portion of the n^- drift region of the CoolMOS transistor is not present in conventional power MOSFETs, as we pointed out previously. Analytical modeling of this region was therefore undertaken, considering it to be equivalent to the JFET-type structure shown in Fig. 2.7, as suggested by the observed depletion region behavior. The gate, source, and drain terminals are defined for this JFET as shown in Fig. 2.7. Using the depletion approximation, we can write, assuming $N_a = N_d = N$

$$\omega(y) = (\varepsilon_{si} V_G / qN)^{1/2} \quad (1)$$

The total current at a given y is

$$I = -zh(y)/\rho \cdot dV/dy \quad (2)$$

Where $h(y) = cp/2 - \omega(y)$ (cp/2 being the width of the n^- pillar W_n) can be shown to be

$$h(y) = cp/2\,[1 - (V(y) - V_G / V_p)^{1/2}] \quad (3)$$

V_p in Eq. (3) is the pinch-off voltage $V_p = q \cdot (cp/2)^2 \cdot N / \varepsilon_{si}$. Now, integrating over the length of the structure, the current can be obtained as

$$I = G_0 \cdot V_p[V_{DS} / V_p + 2/3(-V_{GS} / V_p)^{3/2} - 2/3(V_D - V_G / V_p)^{3/2}] \quad (4)$$

with $G_0 = cp \cdot z / 2\rho \cdot t_{epi}$. It can be seen that (4) is similar to that for a conventional JFET [24].

For the device to block maximum voltage, the charge (Q) in the n^- and p^- pillars should be exactly balanced and chosen such that the pillars are compietely depleted before breakdown (i.e. $Q < \varepsilon_{si}E_C / q$). This ensures that the electric field profile is flat (and not triangular as in the standard MOSFET case) and the breakdown is dependent just on the epilayer thickness and independent of the doping concentration. Assuming a perfectly flat electric field profiIe and $W_n = W_p = cp/2$, the V_B and Q are given by

$$V_B = E_C \cdot t_{epi} \quad (5)$$

$$Q = N_d \cdot cp / 2 = \varepsilon_{si} \cdot E_C / q \quad (6)$$

where E_C, is the critical electric field strength, t_{epi} is the thickness of the epitaxial layer (height of the pillars), N_d is the doping concentration of the n^- pillar and cp is the cell pitch. Using (5) and (6) in the R_{on} equation

$$R_{on} = t_{epi} / q \mu_n N_d \quad (7)$$

leads to

$$R_{on} = cp \cdot V_B / 2q \mu_n E_C Q = cp \cdot V_B / 2 \mu_n \varepsilon_{si} E_C^2 \quad (8)$$

Equation (8) clearly shows that the relation between the V_B and R_{on} of the CoolMOS is linear, unlike the power law relationship

$$R_{on} = 6 \cdot 10^{-9} V_B^{2.5} \quad (9)$$

of the conventional DMOS device, thereby giving the CoolMOS a huge advantage over conventional MOSFETs. Equation (8) also points out that R_{on} is inversely proportional to Q and hence Q should be kept as high as passible to get the lowest on-resistance. It may also be noted that R_{on} of the CoolMOS is directly proportional to the cell pitch and hence it is extremely important to make the tall pillars as narrow as possible [31]-[34].

Chapter 3
Simulation Process

3.1 Simulation Software

Several software packages are available to arrive at a realistic and satisfactory simulation. Integrated Systems Engineering Technology Computer Aided Design (ISE-TACD) tools is one such package (Fig. 3.1). This software comprises several modules, such as MESH-ISE for grid generation, DESSIS-ISE for device and circuit simulation, FLOOPS-ISE for process simulation, MDRAW-ISE, one structure and mesh information display, and visualization tools like INSPECT and TECPLOT-ISE.

In the simulation package ISE-TCAD, the basic semiconductor equations (e.g. Poisson's and electron-hole continuity equations) are numerically solved on the mesh points mapped over the device structure. The numerical solution converges in accordance with the defined criteria for analysis. The typical input consists of structure of the device, mesh size, impurity profiles in different regions, and physical effects and models for performing the simulation. The input is given in the form of files, the mesh boundary file for defining the geometry of the device under examination; the mesh command file for impurity profiles in the structure and mesh refinements to focus at the critical regions of the

device; and the dessis command file for specifying the voltages and currents applied on the electrodes of the device, physical models to be used in the simulations, the permissible errors in the parameters, the number of iterations to be done, and the method of solving Poisson's equation, along with the approach to problem solving, whether transient, quasi-stationary, and so on. "Quasi-stationary command" is used to ramp a device from one solution to another by modifying its boundary conditions (e.g. ramping of the voltage at an electrode). "Transient command" is used to run a transient solution.

On the other words, we utilize FLOOPS-ISE to simulate the process, and MDRAW-ISE to produce the mesh of the device. DESSIS-ISE is used to result the behaviors of the device at several conditions. After that, INSPECT tool can show voltages and currents curves, and TECPLOT-ISE is utilized to display electric field, electric potential, current density distribution, etc.

3.2 Super-Junction Structure Simulation

First, we utilize FLOOPS to simulate the process of the SJ structure. Process flow and condition are defined as:

(a) Set up the substrate with n-type (100)-oriented silicon wafer ($N_d=3\times10^{19}cm^{-3}$).

(b) Grow epitaxial layer 0.25 μm with doping phosphorous ($N_d = 3\times10^{15}\ cm^{-3}$).

(c) Annealing 15 second at 550 ℃.

(d) Etch the left-half of the epi-layer.

(e) Utilize selective growth to fill the left-half with doping boron epitaxion ($N_a=3\times10^{15}\ cm^{-3}$).

(f) Annealing 15 second at 550 ℃.

(g) Repeat (b)~(f) 60 times to achieve a 15 μm pillar.

(h) Deposit a 3 μm layer with doping boron ($N_a=3\times10^{19}\ cm^{-3}$) as upper side.

(i) Contact upper and lower electrode.

And then, we put the structure (Fig. 3.2) into DESSIS-ISE to simulate its electrical properties. Here, we set up the across voltage from 10 V to 300 V.

3.3 The Simulation of the Complete Structure of the CoolMOS

By observing the SJ structure simulation, we can confirm that our device simulation is practicable. Then, we will proceed to accomplish the CoolMOS structure complete:

(A) Continuing using previous flow for SJ structure simulation, we let the pillar grows to 20 μm - namely repeat (b)~(f) 80 times.

(B) Etch a 3 μm trench for p-base.

(C) Fill the trench with doping boron deposition (N_a=5.5×$10^{16}$$cm^{-3}$).

(D) Use implantation to define the source region (N_d=3×$10^{19}$$cm^{-3}$).

(E) Grow a 0.1 μm oxidation layer for gate oxide.

(F) Contact the source, gate, and drain electrodes.

Fig. 3.3 shows the complete structure, and we could find that the tools spread impurities diffusion out distinct. Furthermore, during simulation process, we pay attention on impact ionization effect. Namely, avalanche breakdown function has been pondered over. At next section, we will list all simulative conditions in detail.

3.4 Simulative Conditions in Detail

From reference papers, we know that the drift region (the pillar) controls the greater part characteristics of the device. Above all, we take a focus on the doping concentration of the region.

In the first instance, we dominate the concentrations at n- and p-region equilibrium, and set up three different values to observe the influences:

$$N_a = N_d = 3 \times 10^{15},\quad 6 \times 10^{15},\quad 9 \times 10^{15}\quad cm^{-3}$$

Having fabrication element in mind, we deliberately let the

concentrations imbalance with the standard condition of $N_a = 6 \times 10^{15}$ cm^{-3}:

(1) n^- region raises up 5 % and 10 % to $N_d = 6.3 \times 10^{15}$ and 6.6×10^{15} cm^{-3} ;

(2) n^- region cuts down 5 % and 10 % to $N_d = 5.7 \times 10^{15}$ and 5.4×10^{15} cm^{-3} ;

And then, we discuss the cases of $N_a \neq N_d$. By the same way, letting $N_a = 6 \times 10^{15}$ (cm^{-3}) to be the standard condition, we change that :

$N_d = 6 \times 10^{14}$, 3×10^{15} , 9×10^{15} , and 1.2×10^{16} cm^{-3} .

Chapter 4
Results and Discussions

4.1 About the Super-Junction Structure

From Fig. 4.1, it shows the result that is similar to other studies. When the pillar is not depleted completely, the electric field distribution of that is a triangular form. Otherwise, this shape is rectangle like. So, in the same length and critical electric field, this structure has higher breakdown voltage indeed. This result takes a good few confidence in the following simulation.

4.2 Doping Concentration inside the Pillar Region for Balance Condition

Under balance conditions, the electric field and electron density at off-state (Vg = 0) are shown in Fig. 4.2 ~ 4.4 for the doping concentration of 3×10^{15}, 6×10^{15} and 9×10^{15} cm^{-3} respectively, inside the pillar regions. The electron density curves indicate that it is more difficult to deplete completely as the doping concentration is heavier. Hence, higher voltage drop occurs at the neck region. Generally, heavier doping concentration easily reaches the critical electric field strength of the

material ($E_c \fallingdotseq 3 \times 10^5$ V/cm for silicon). As the decease in the pillar doping concentration, the electric field curve shows more flattening, and it can be manifested that the lighter doping pillar is capable of sustaining higher breakdown voltage.

As shown in Fig. 4.5, the driving force of current increases, and as everyone knows, the on-resistance decreases with the doping concentration increasing. As stated above, doping concentration should not be increased randomly. There is one optimal pillar doping concentration for choice within the safe operating area (SOA). In Fig. 4.6, the transfer characteristics are similar to those of a conventional power MOSFET. Although CoolMOS cannot improve the rapid saturation at low voltage level, it does not sway the good manifestation of the device at high voltage level.

Quasi-saturation is seen obviously at the I_d-V_d curves (Fig. 4.7~4.9), and it is improved with concentration increasing. However, the Fig. 4.10 shows that there is an optimal pillar doping concentration to alleviate quasi-saturation effect. This result might occur by that the concentration is near the level of the p-base (5.5×10^{16} cm^{-3}).

Fig. 4.11 provides another view to probe the locations with breakdown occurrence. In the p-n junction, the peak value of the electric field strength always presents. Fig. 4.12 is a 2-D map of the electric field distribution, and it points apparently out that is not think so, this peak value is lower than the value at the neck region a lot. Perhaps it is necessary to take some focus on the p-n junction, we want to improve the problem of the breakdown voltage.

4.3 Comparison between General Saturation and Quasi-saturation

In the quasi-saturation state, the space charge distribution are presented in Fig. 4.13 with different drain voltages at Vg of 15 (V) for the pillar doping concentration of 9×10^{15} (cm^{-3}). The depletion region inside the n-pillar begins to advance the pillar center part as drain voltage increasing and then expands difficultly to the n pillar region. However, as the increasing of the drain voltage, the space charge gradually makes the p-pillar to be full depletion. The extra carrier density generated in the current path as shown in Fig. 4.14 can explant this phenomenon.

Fig. 4.15 and Fig. 4.16 show the variations of space charge and electric field within general saturation for the pillar doping concentration of 3×10^{15} (cm^{-3}). The depletion regions inside the n-pillar and p-pillar both expand uniformly with increasing of the drain voltage, and the current path is clipped from top to bottom. The electric field distributes in the p-n junction and the neck region uniform. Indeed, Fig. 4.17 shows the current path has no extra carrier density like that within quasi-saturation. By the same way, to observe the variation of space charge and electric field within quasi-saturation (Fig. 4.18, 4.19), not only the depletion region expands difficultly into the current path, but also that is clipped from bottom to top. The electric field density masses at the neck region and the bottom of the p-n junction.

Finally, taking a conclusion for the comparison between general-

and quasi-saturation, we let the drain voltage in the same level (Fig. 4.20). The region under the gate, its potential is zero within quasi-saturation, but that is not within general saturation. This shows that the channel at p-base is pinched off just like an “intrinsic” MOSFET, when the device is at saturation. However, the large enough gate voltage causes an accumulation layer near the p-base channel, and this phenomenon makes the area between the region under the gate and the source region like a short circuit. The electron current directly flows from source to the top of the current path without decay, and then drifts towards the bottom of the device by drain voltage pulling in. So that, the quasi-saturation effect lets the device to be like a large resistance.

4.4 Doping Concentration inside the Pillar Region for Imbalance Condition

In this section, the doping concentration inside the pillar region is set up imbalance deliberately to observe the variation of the quasi-saturation effect. It is assumed that the charge is within ± 5 % and ± 10 % related to the doping concentration of p-pillar ($N_a = 3\times10^{15}\ cm^{-3}$). As the N_d decreasing, the quasi-saturation effect is more obvious at the same voltage.

Fig. 4.22 shows the I_d-V_d curve at V_g = 15 V that it has large different doping concentrations between the n- and p-pillar regions. It has a larges slope in imbalance-mean a smaller resistance within

quasi-saturation. As shown in Fig. 4.23~4.25, it has a wider current path, when the doping concentration inside the n-pillar is larger.

Chapter 5
Conclusion and Future Works

5.1 Conclusion

This study has successfully simulated the operating mode of CoolMOS by the working environment of ISE-TACD. Meanwhile, observations have been made on the distribution properties of space charge and electric field. Through these observations, it has been discovered that, at the time of quasi-saturation, accumulation layers appear near p-base below gate. This distinguishes apparently the electric properties of devices at the time of quasi-saturation from those at the time of general saturation. Imbalance of doping concentration also affects electric properties. Yet, a useful conclusion has been drawn from the examination of concentration imbalance. That is: quasi-saturation is closely correlated to the doping concentration of the n-pillar.

5.2 Future Works

Of course, mastering simulation software is the initial and fundamental step. In the future, thorough examination on CoolMOS by ISE-TACD will continue to be engaged. At present, one preliminary plan has been conceived. This plan involves including thermal effect and

various kinds of particle effects into the conditions of device simulation so that the simulative results obtained can approximate the reality to the greatest extent. This done, more precise observation of the breakdown mechanism can be undertaken. If the timing and location of breakdown occurrence can be precisely identified, device properties can be improved more efficiently, or even more advanced device structures can be developed.

And then, we will go deep into observing the quasi-saturation effect to find out its complete mechanism. High frequency operating mode might be one of the future works for us.

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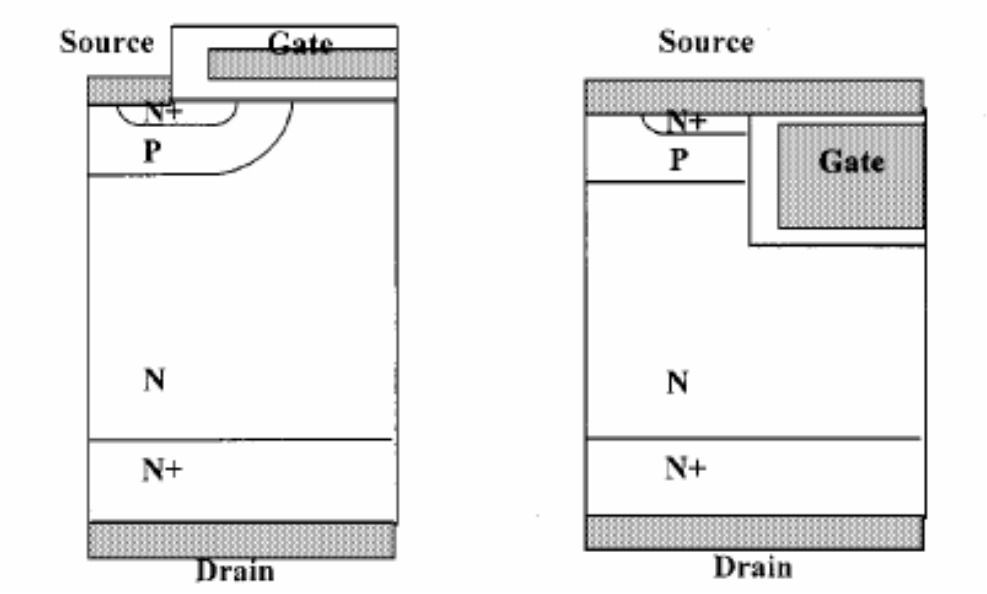


(a) DMOS (b) UMOS

Fig. 1.1 silicon power MOSFET structures

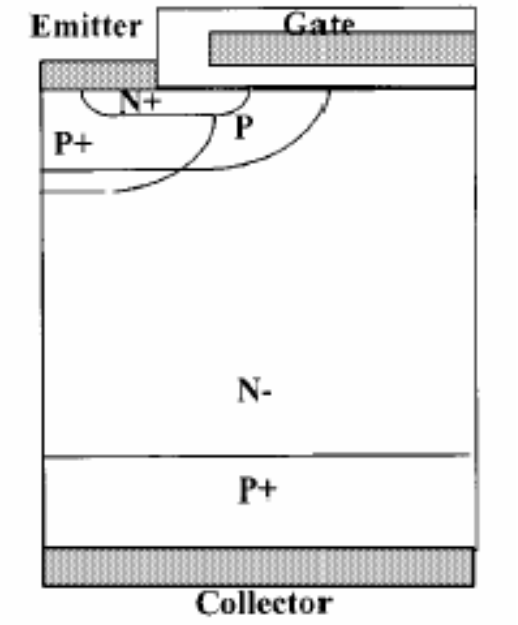


Fig. 1.2 Insulated gate bipolar transistor (IGBT) structure

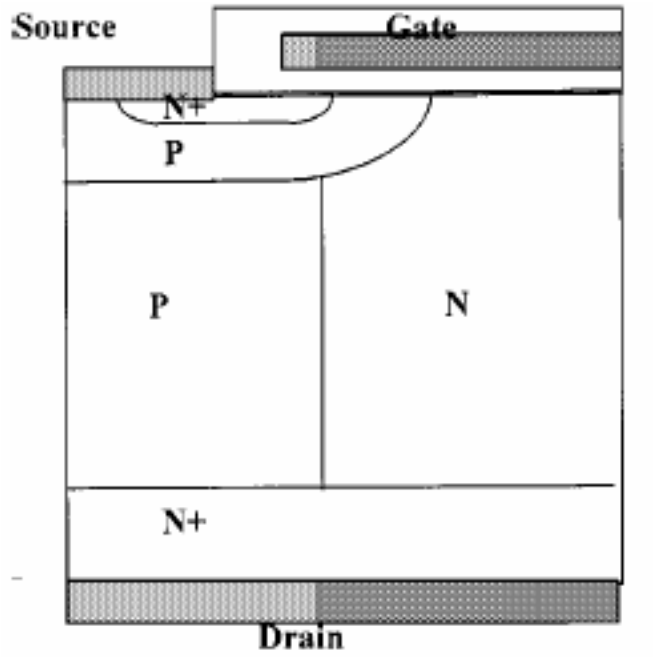


Fig. 1.3 Cross section of the CoolMOS

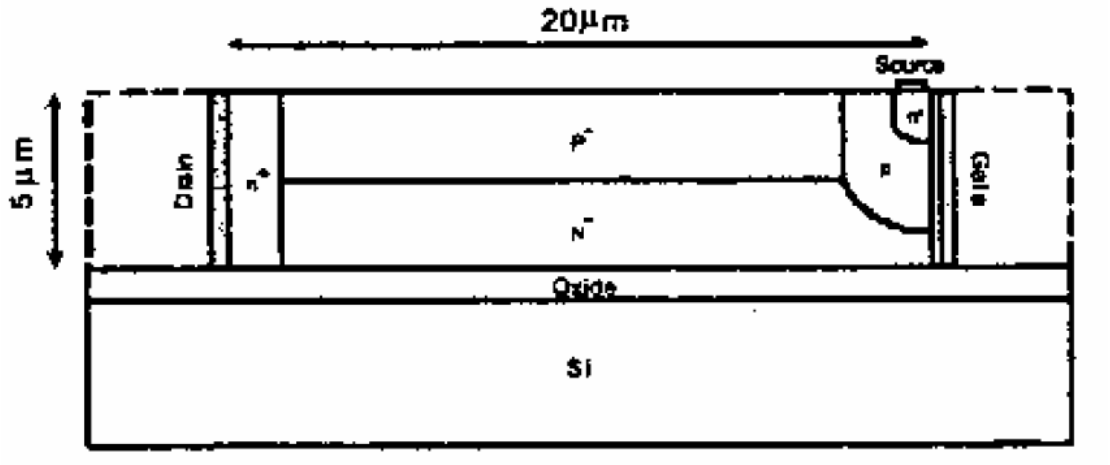


Fig. 1.4 COOLMOS™ on SOI wafer

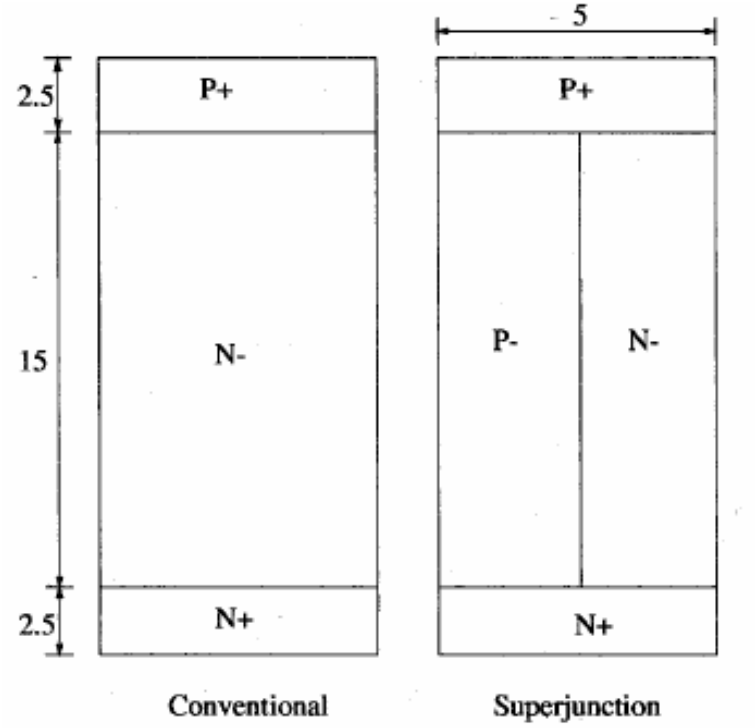


Fig. 2.1 simulation of drift layer structures

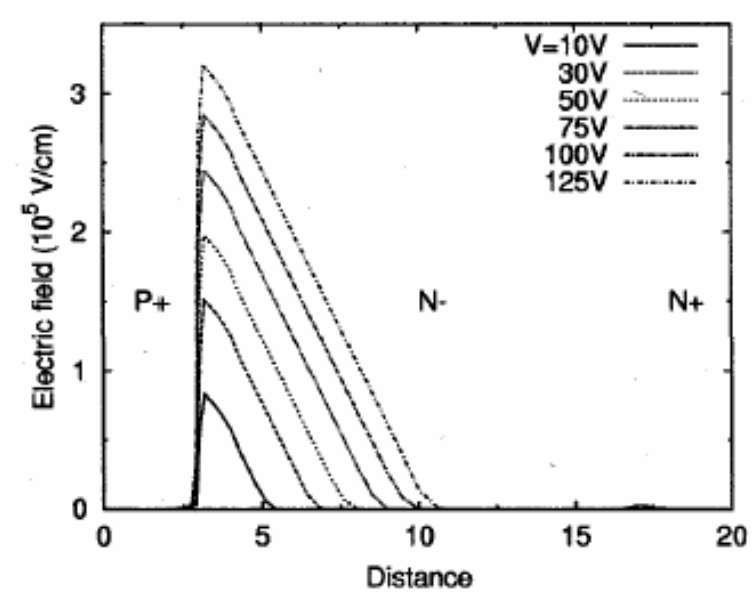


Fig. 2.2 Electric field at conventional drift region

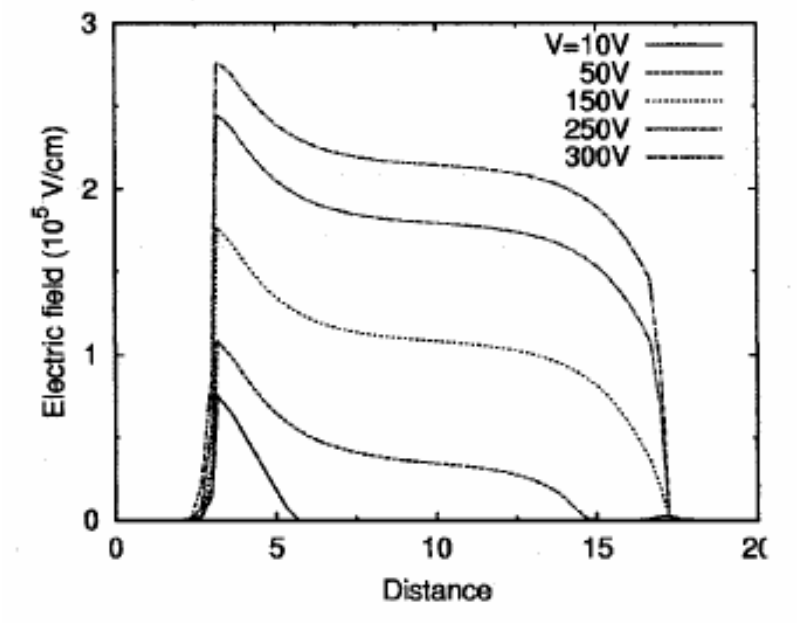


Fig. 2.3 Electric field for SJ structure

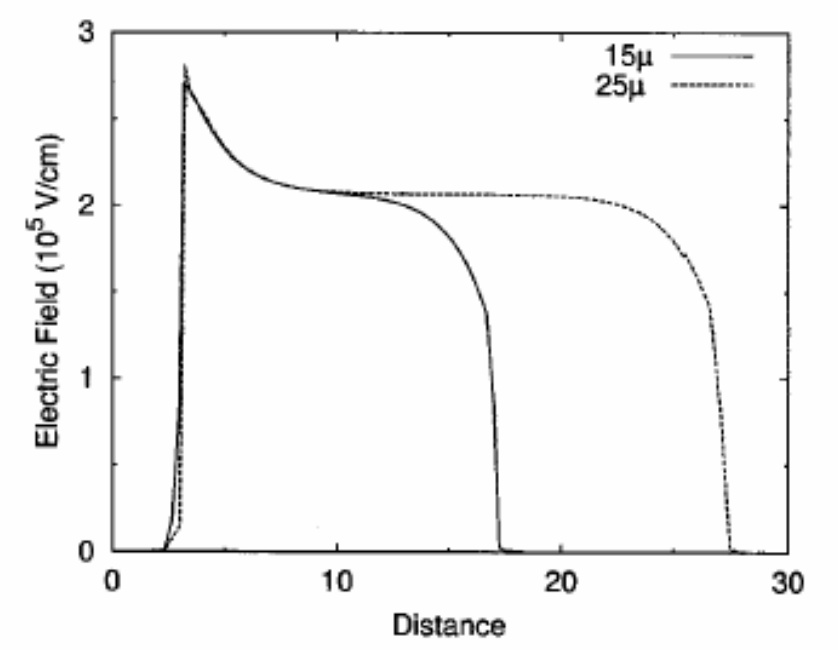


Fig. 2.4 Electric field profile along the right of the device, for SJ structures of heights 15 μm and 25 μm

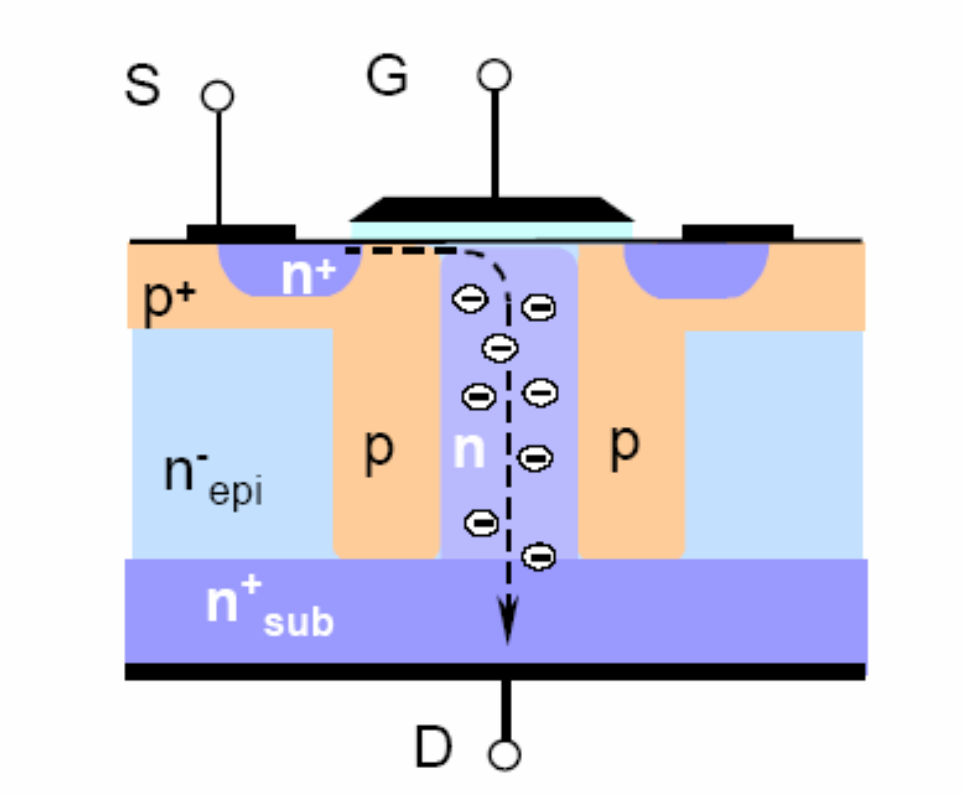


Fig. 2.5 The sketch map of the CoolMOS in the ON-state

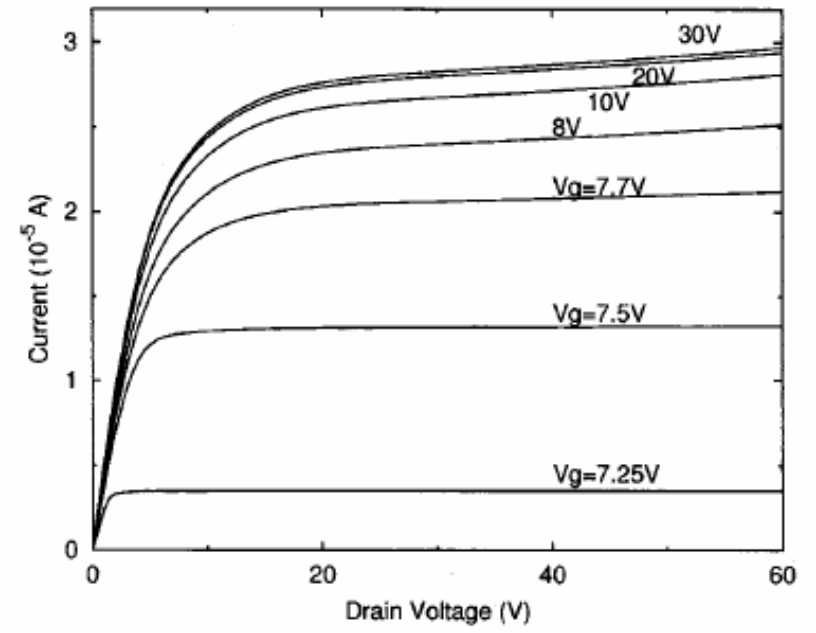


Fig. 2.6 Output characteristics of the CoolMOS™ transistor

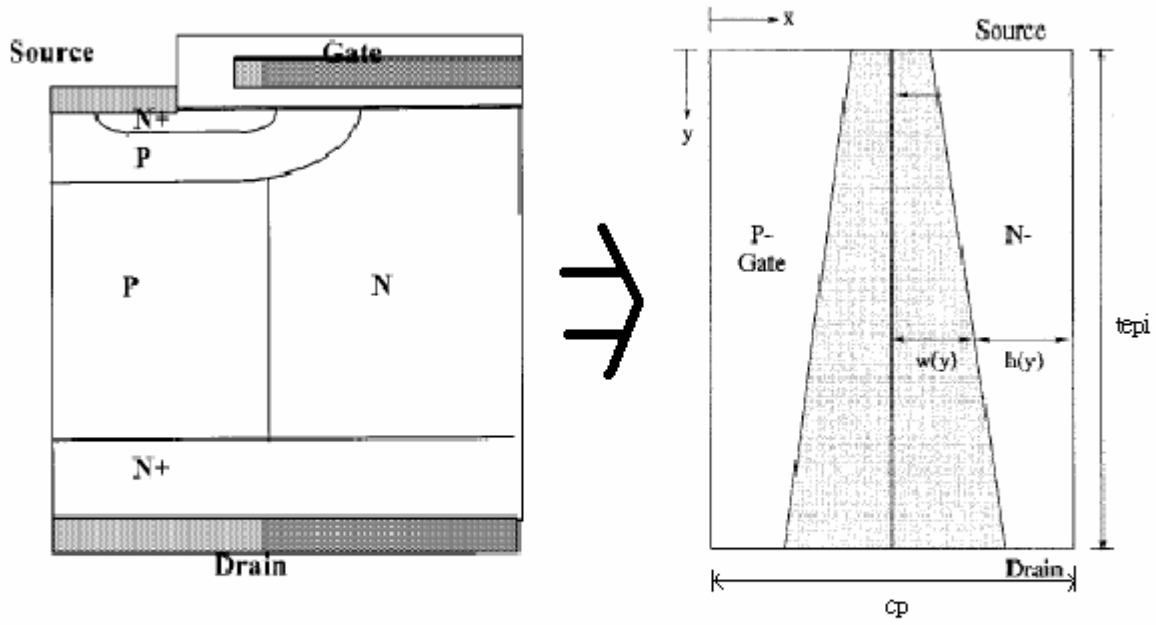


Fig. 2.7 structure identical to the pillar region

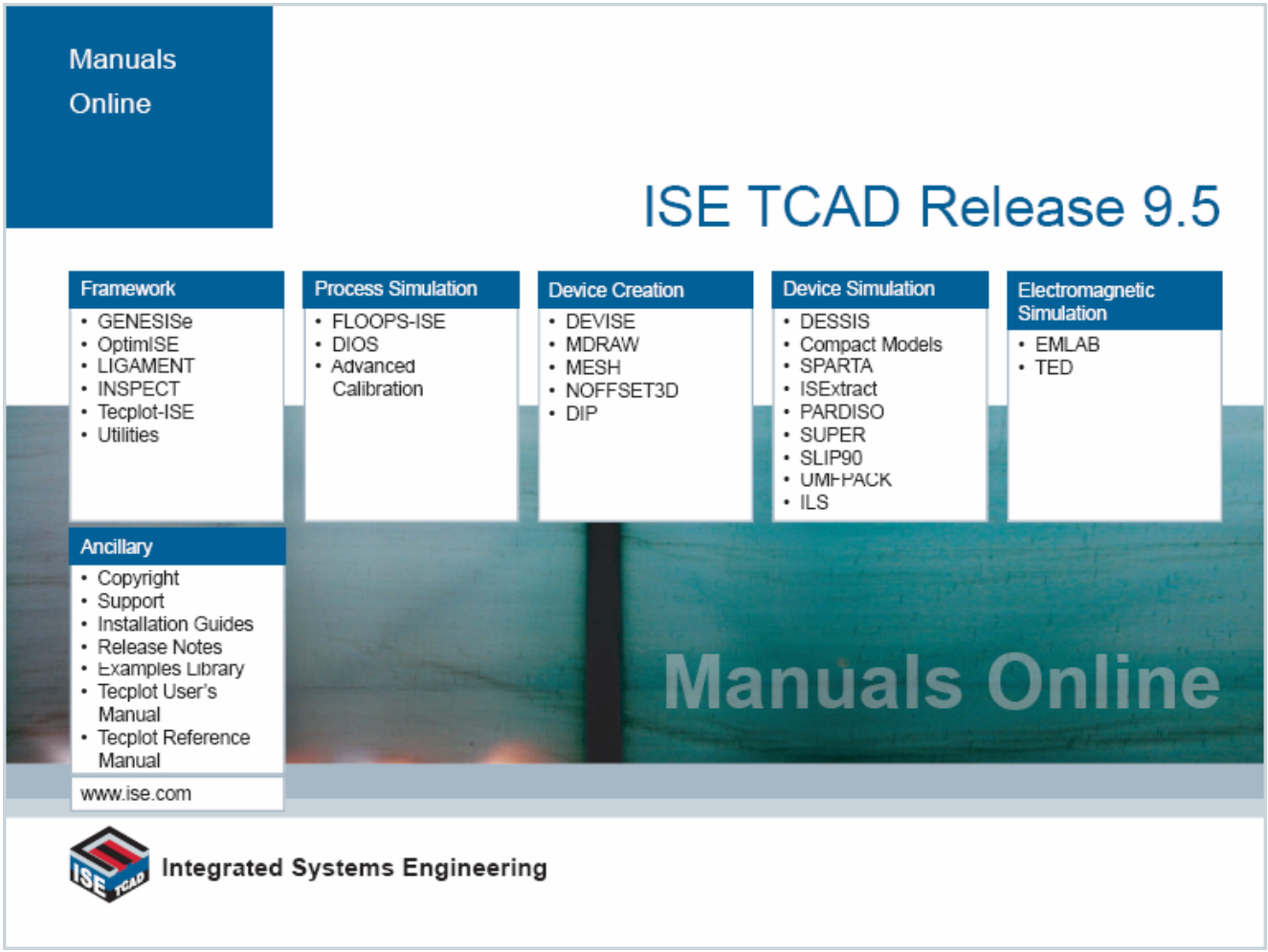


Fig. 3.1 The manuals of ISE-TACD

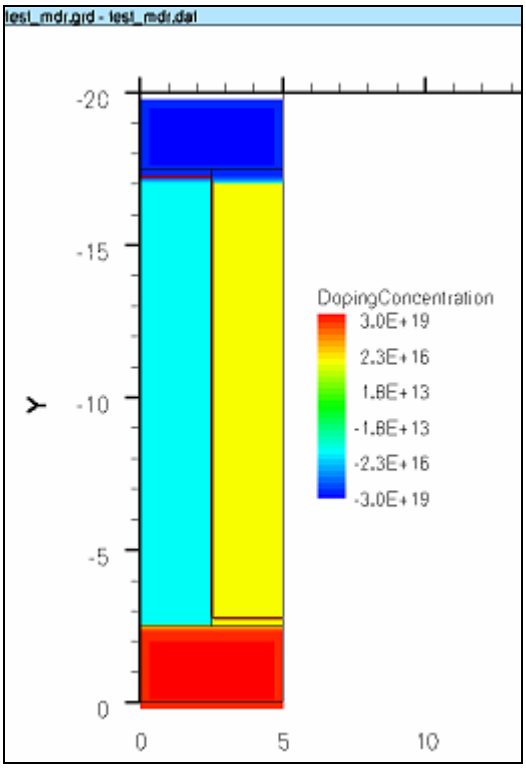


Fig. 3.2 The simulated shape of the SJ structure

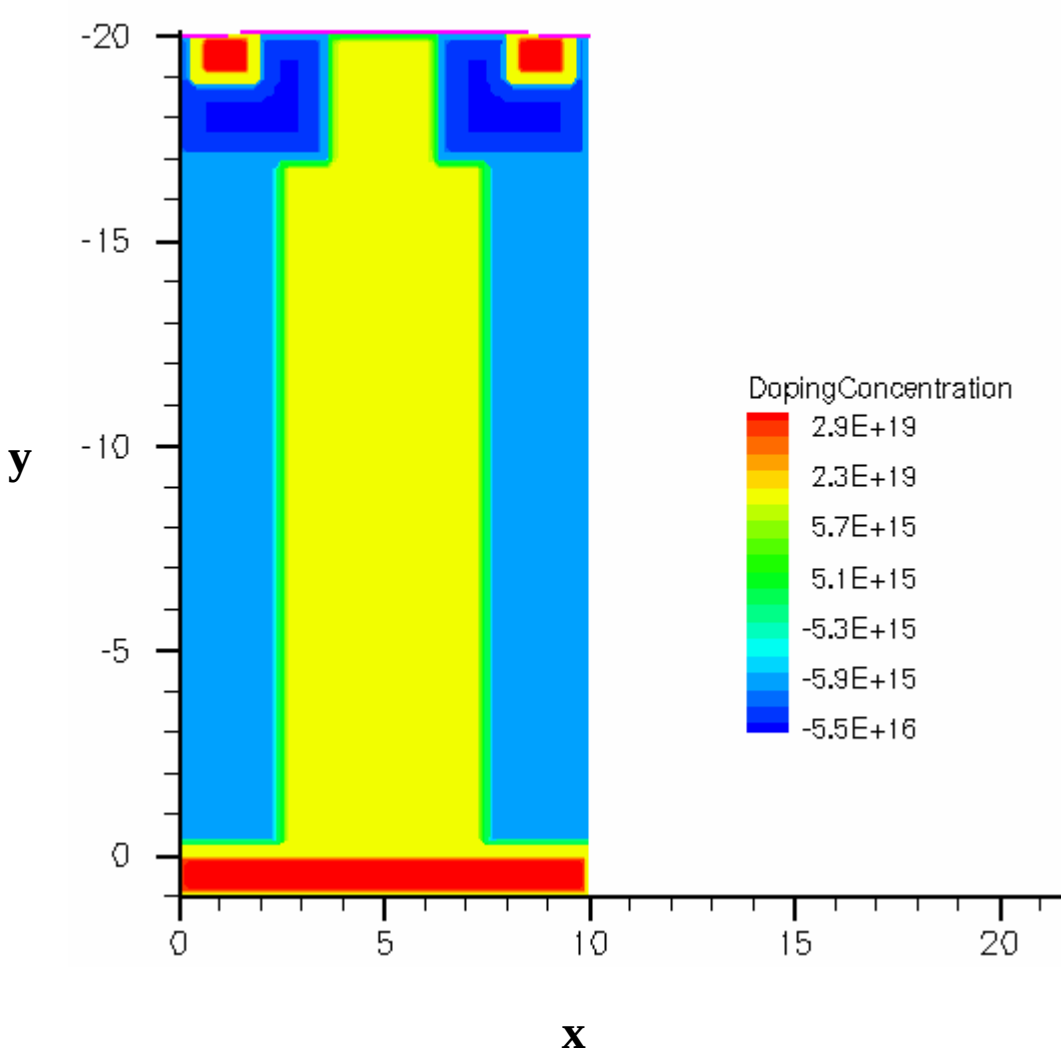


Fig. 3.3 The simulated shape of the CoolMOS structure

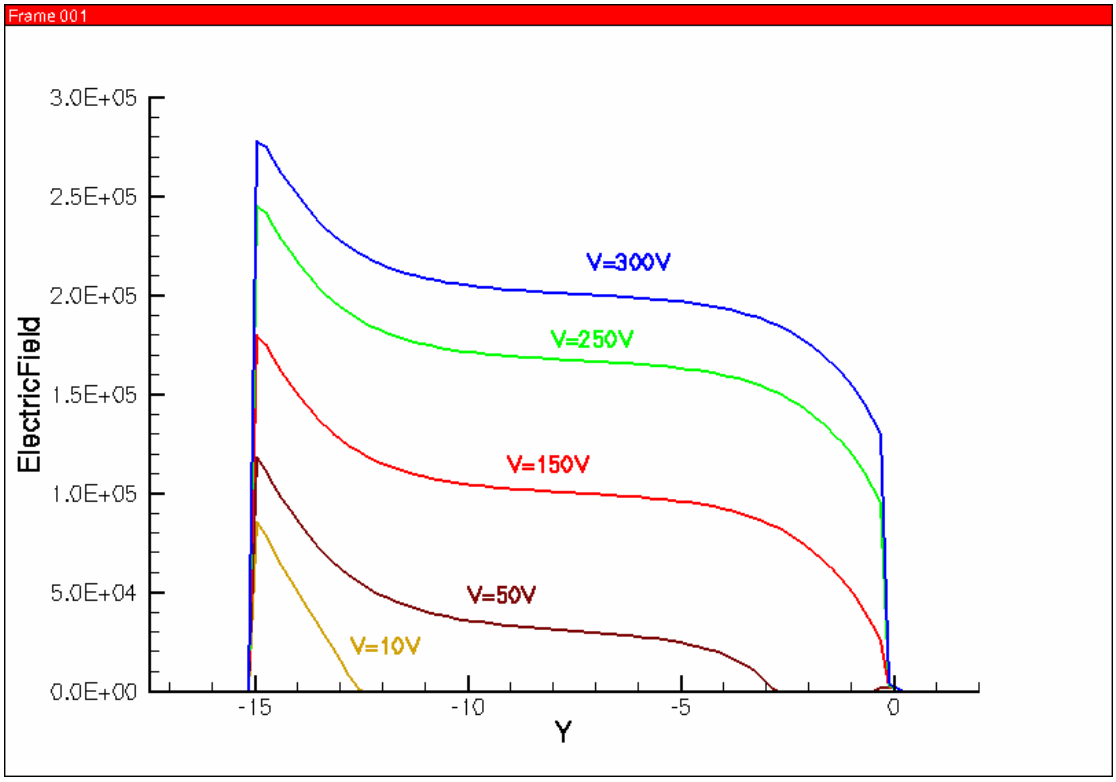


Fig. 4.1 Electric field distribution for SJ structure

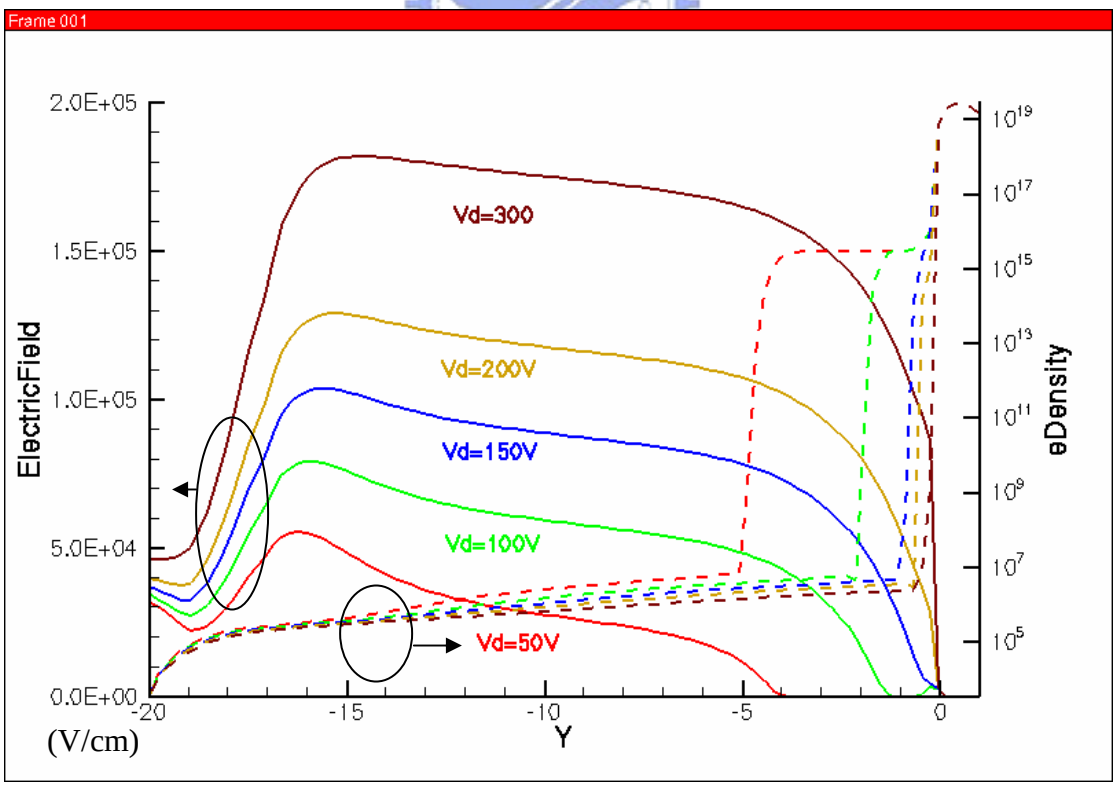


Fig. 4.2 The electric field and electron density for $N_a = N_d = 3 \times 10^{15}$ at off-state (Vg = 0) in x=5

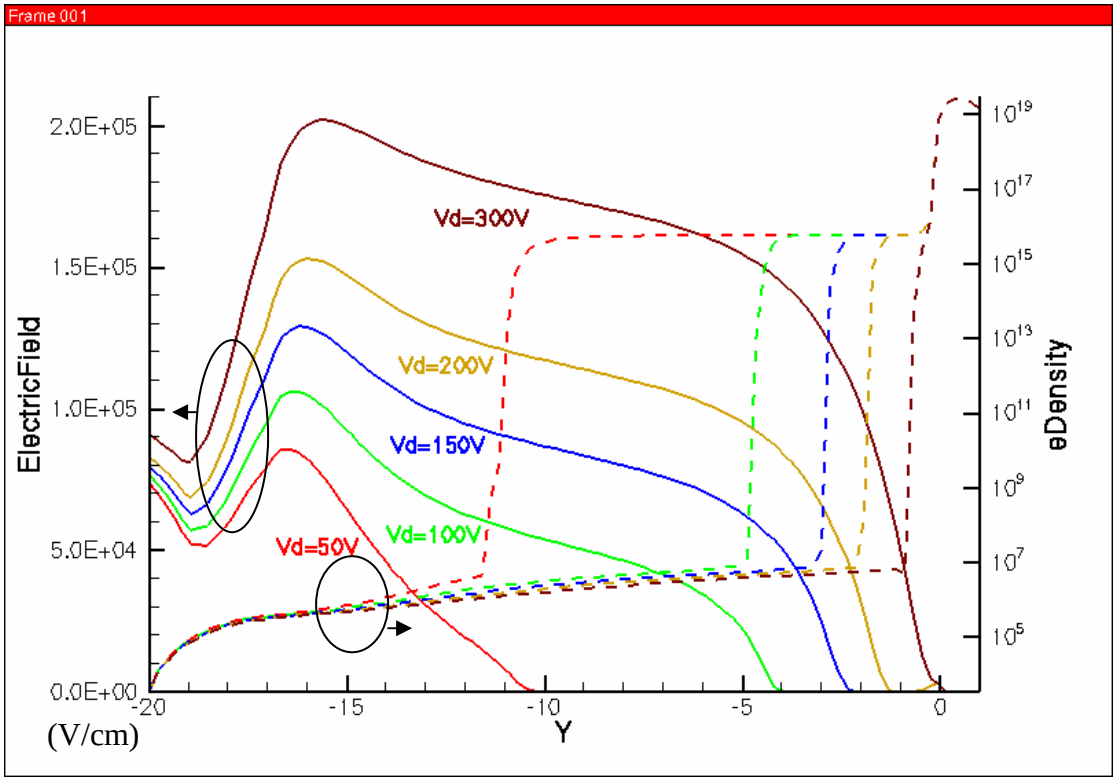


Fig. 4.3 The electric field and electron density for $N_a = N_d = 6 \times 10^{15}$ at off-state (Vg = 0) in x=5

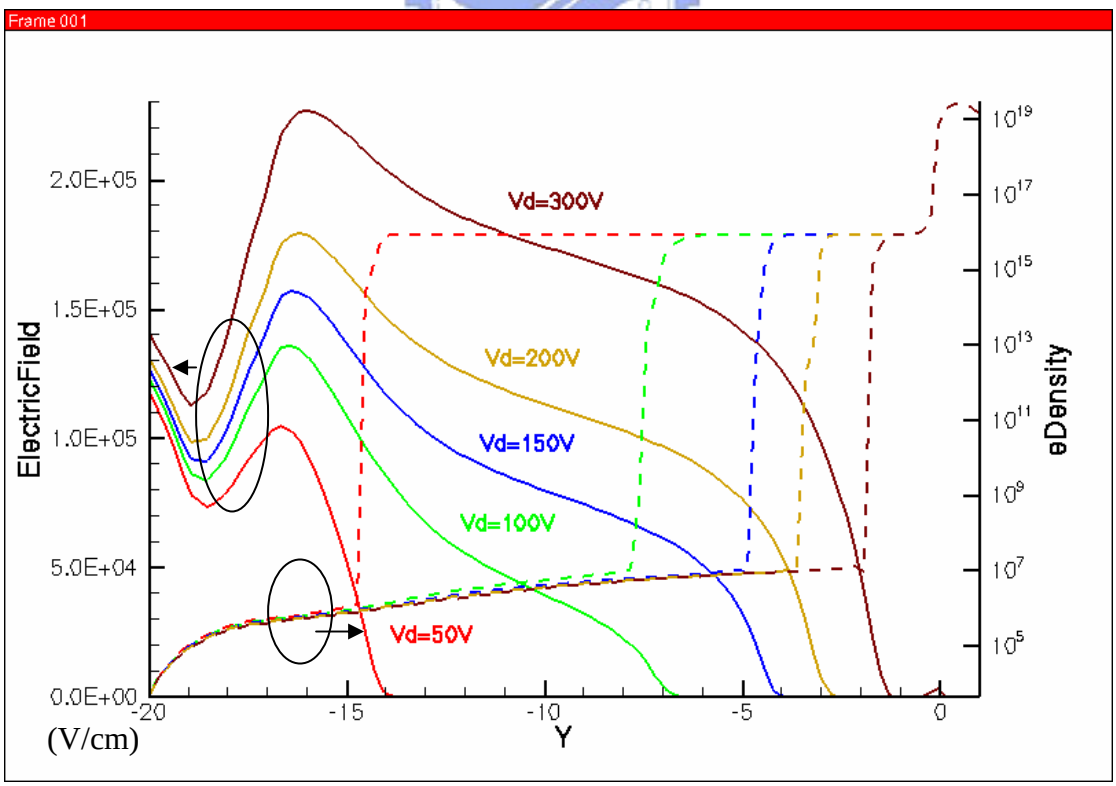


Fig. 4.4 The electric field and electron density for $N_a = N_d = 9 \times 10^{15}$ at off-state (Vg = 0) in x=5

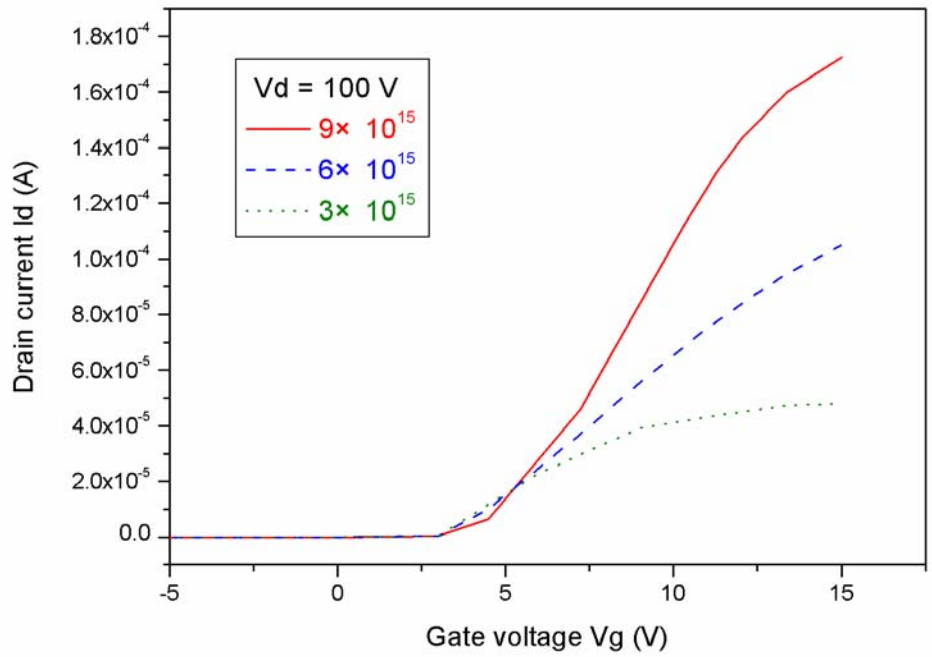


Fig. 4.5 The I_d-V_g curve at V_d =100 V with different pillar concentrations

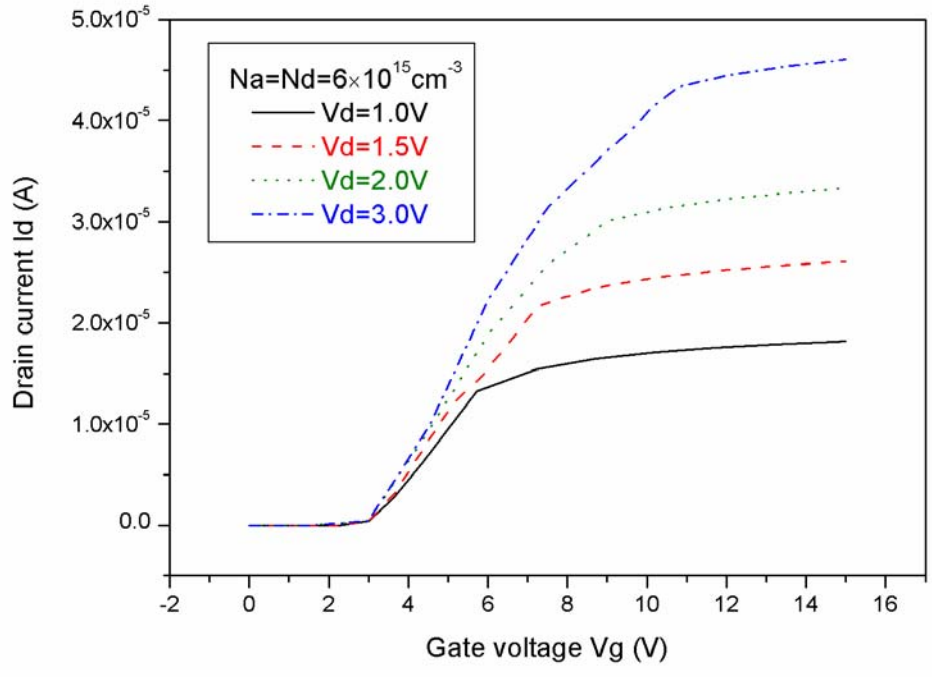


Fig. 4.6 Id-Vg curve at low Vd for N_{pillar}=6×10^{15} cm^{-3}

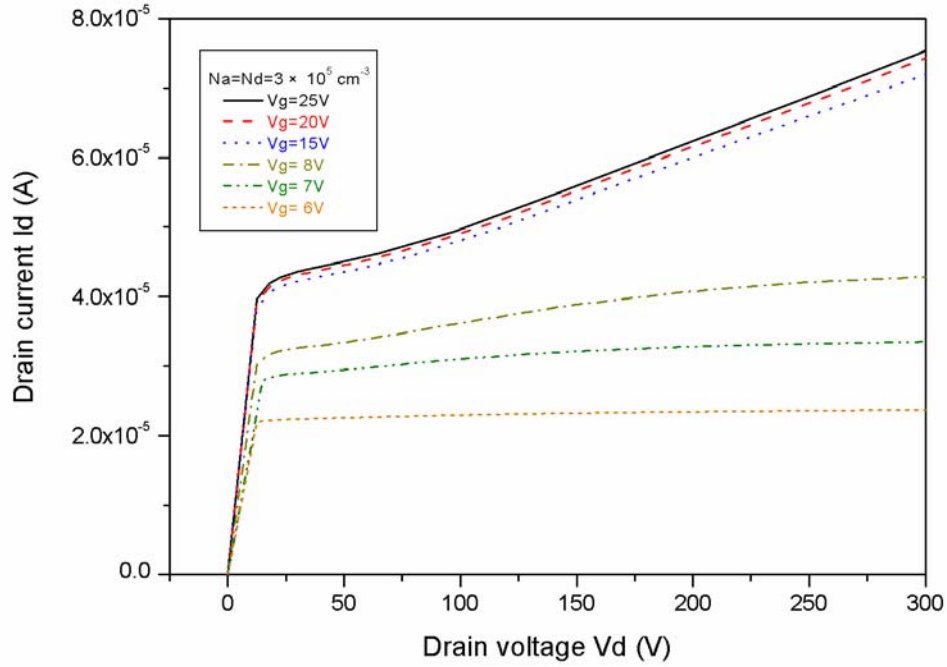


Fig. 4.7 The I_d-V_d curve for N_{pillar}=3×10^{15} cm^{-3}

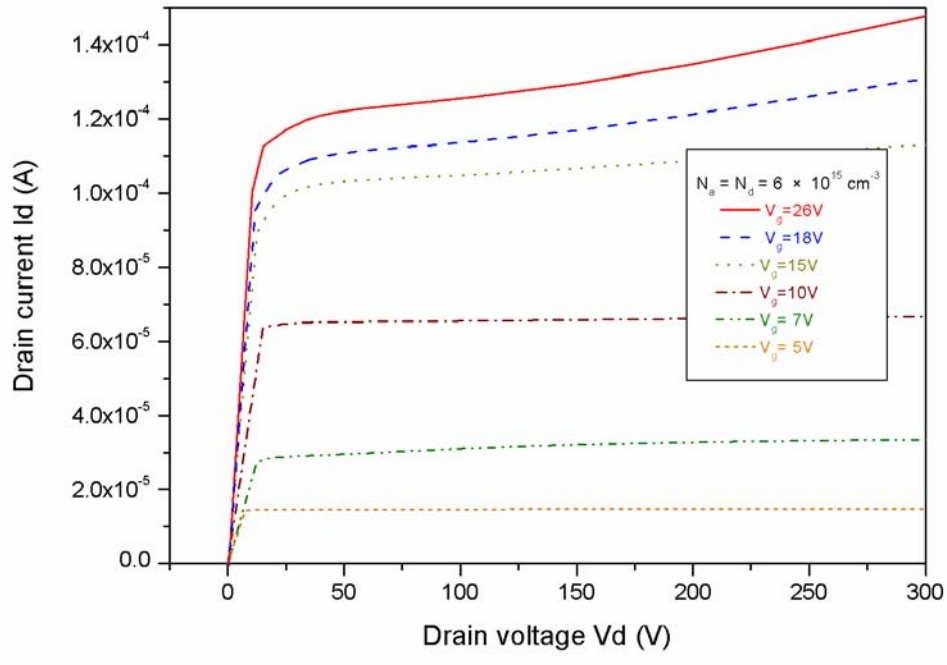


Fig. 4.8 The I_d-V_d curve for N_{pillar}=6×10^{15} cm^{-3}

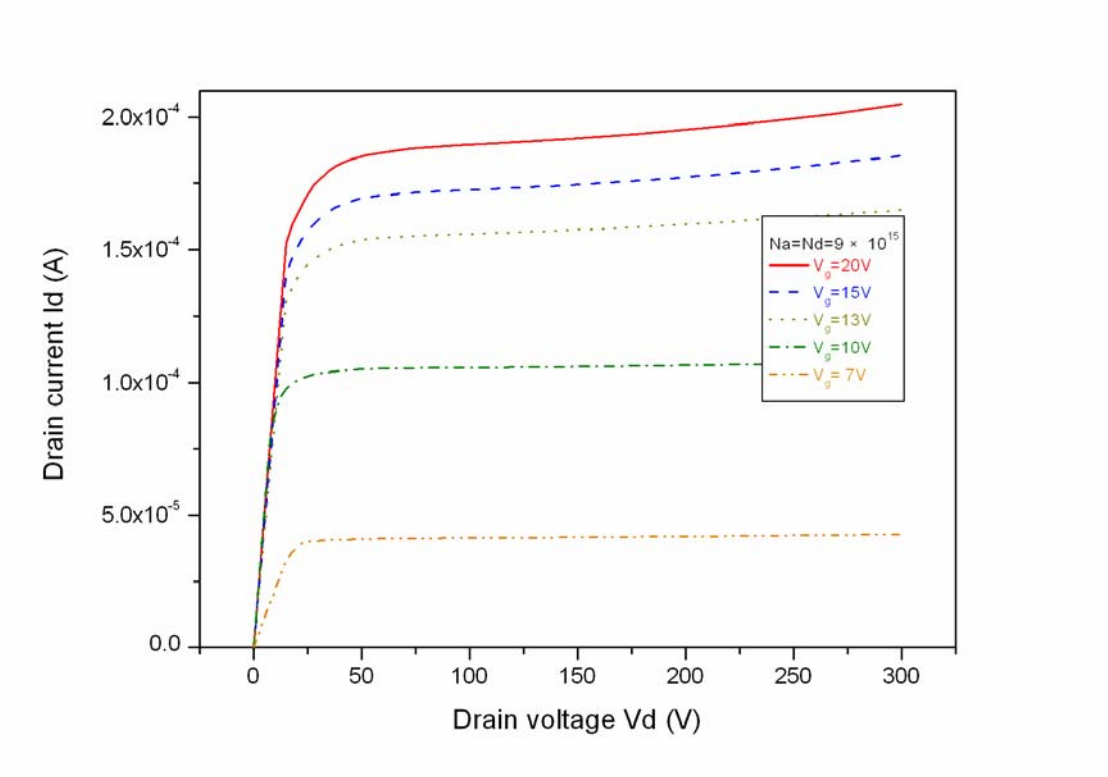


Fig. 4.9 The I_d-V_d curve for $N_{pillar}=9\times10^{15}$ cm^{-3}

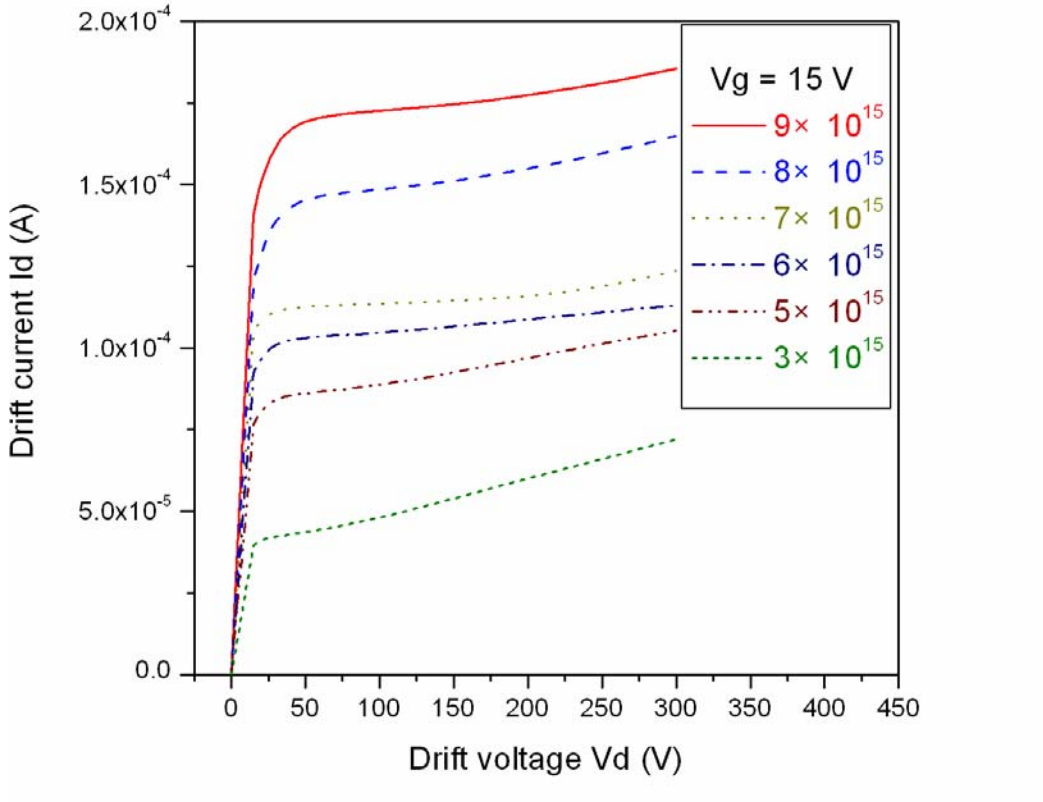


Fig. 4.10 The Id-Vd curves for multiple pillar concentrations

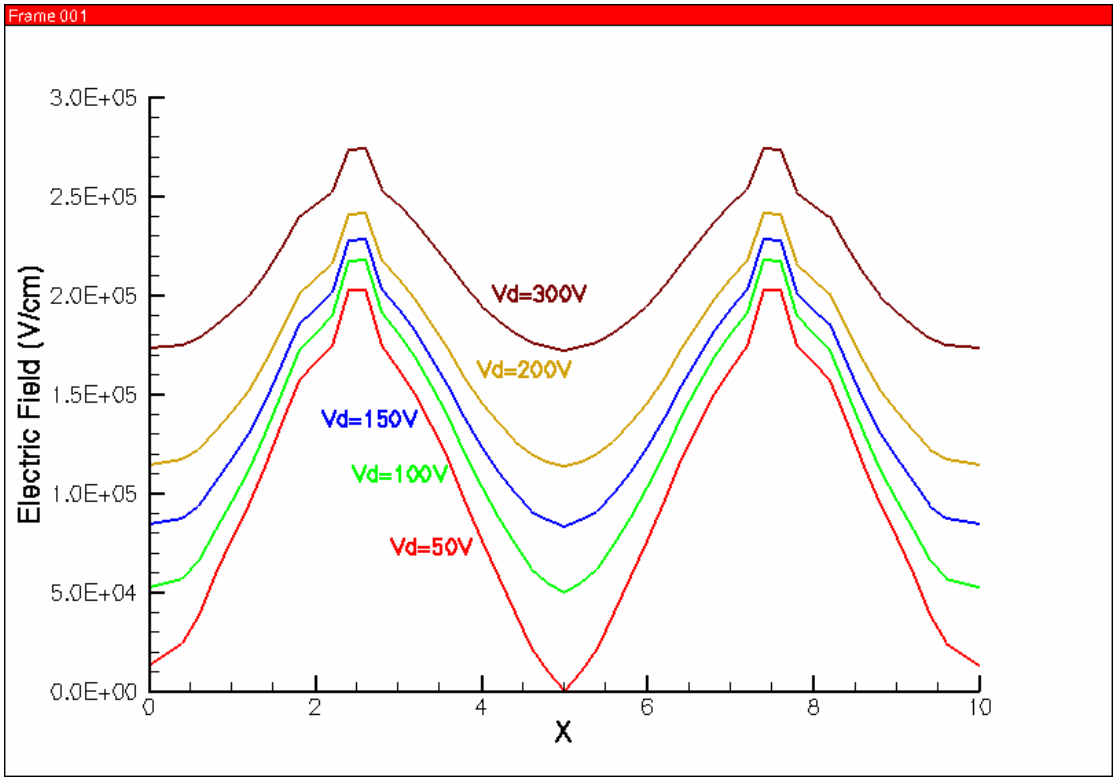


Fig. 4.11 The electric field distribution in off-state at Y=-9 for $N_{pillar}=6\times10^{15}\ cm^{-3}$

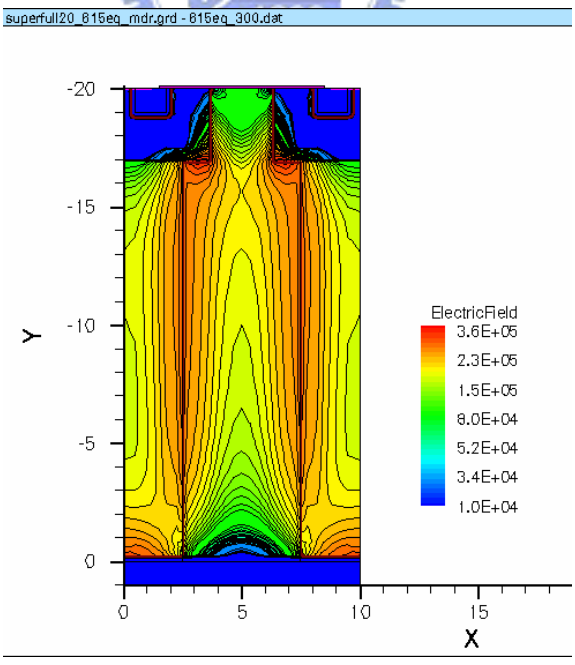


Fig. 4.12 The 2-D map of the electric field distribution in off-state at $V_d=300V$ for $N_{pillar}=6\times10^{15}\ cm^{-3}$

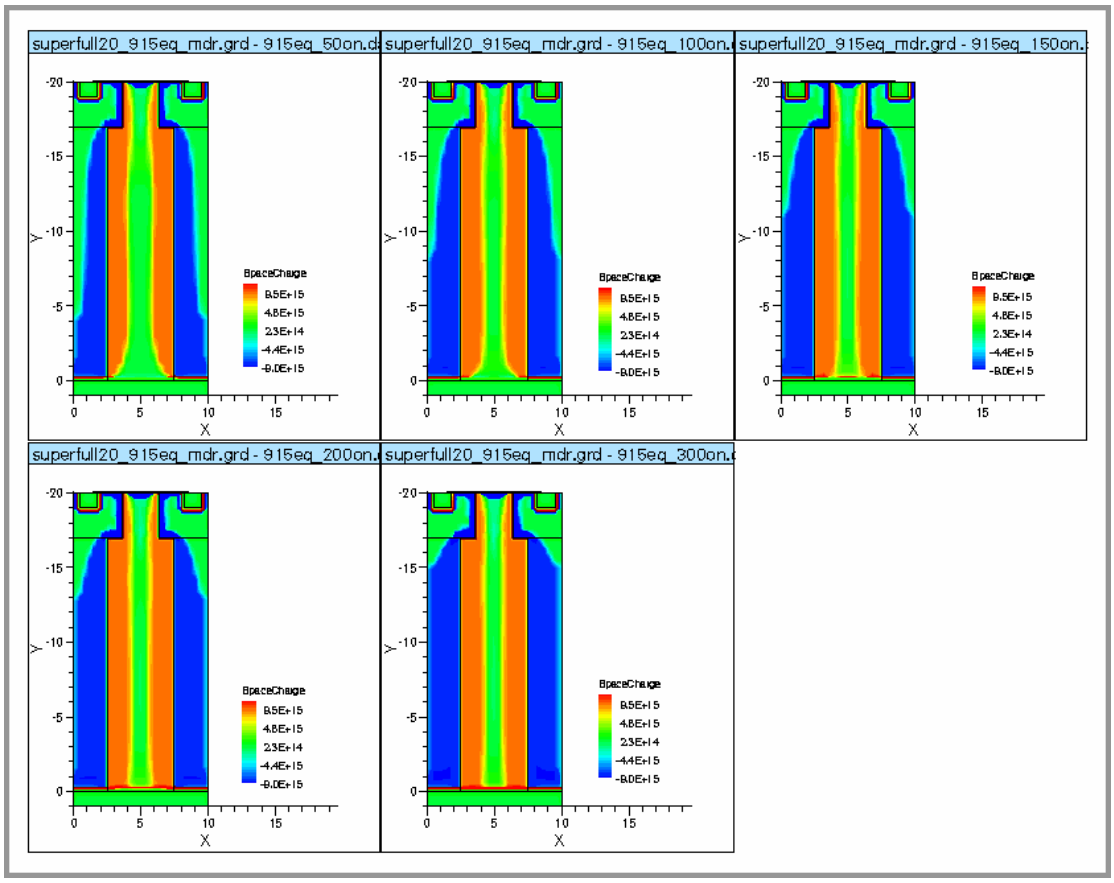


Fig. 4.13 The 2-D map of the space charge distribution in on-state at 50V, 100V, 150V, 200V, and 300V for $N_{pillar}=6\times10^{15}$ cm^{-3}

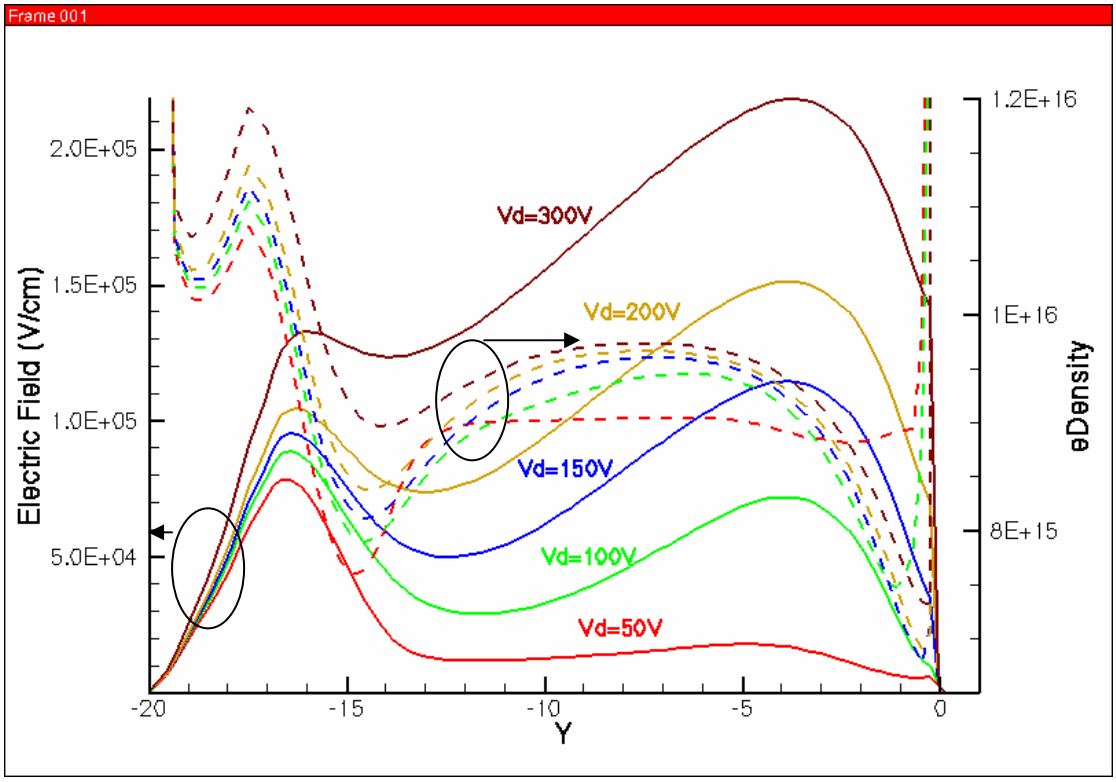
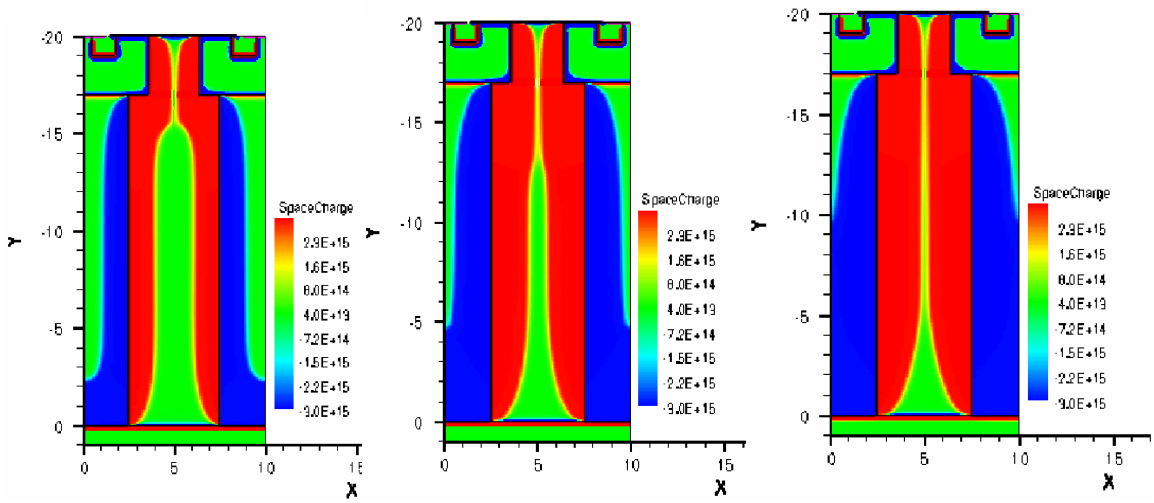
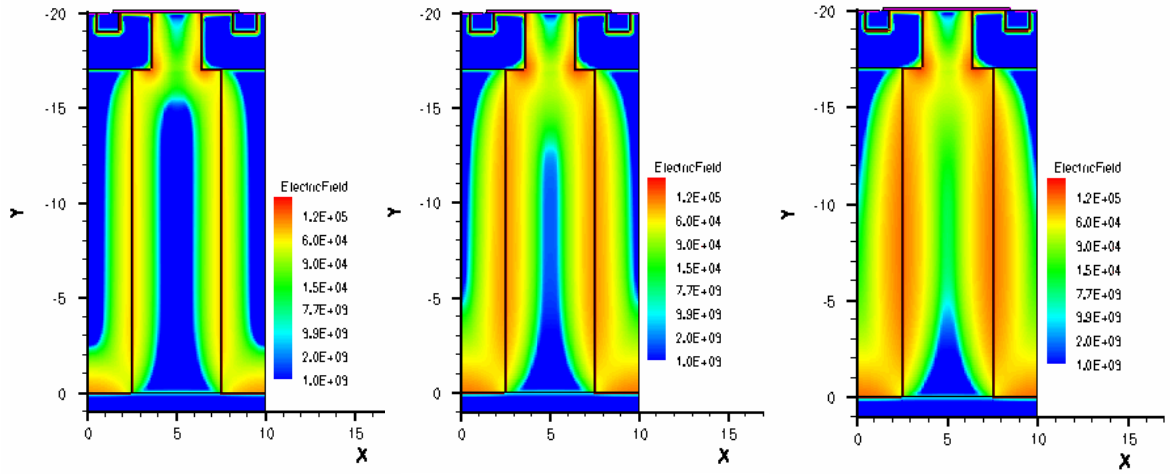


Fig. 4.14 The electric field and electron density for $N_a = N_d = 9\times10^{15}$ at on-state (Vg = 15) in x=5



V_d =10 V V_d = 20 V V_d = 30 V

Fig. 4.15 The Space charge (cm^{-3}) distribution for Vg = 5 V



V_d =10 V V_d = 20 V V_d = 30 V

Fig. 4.16 The Electric Field (V/cm) distribution for Vg = 5 V

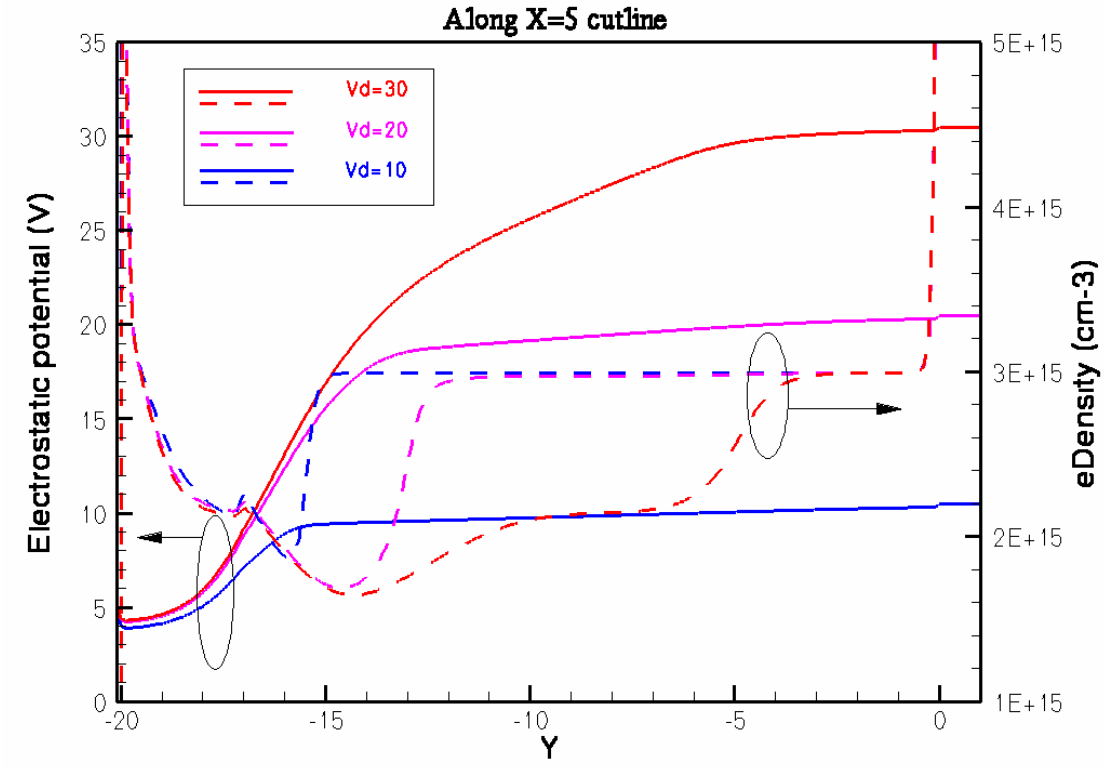
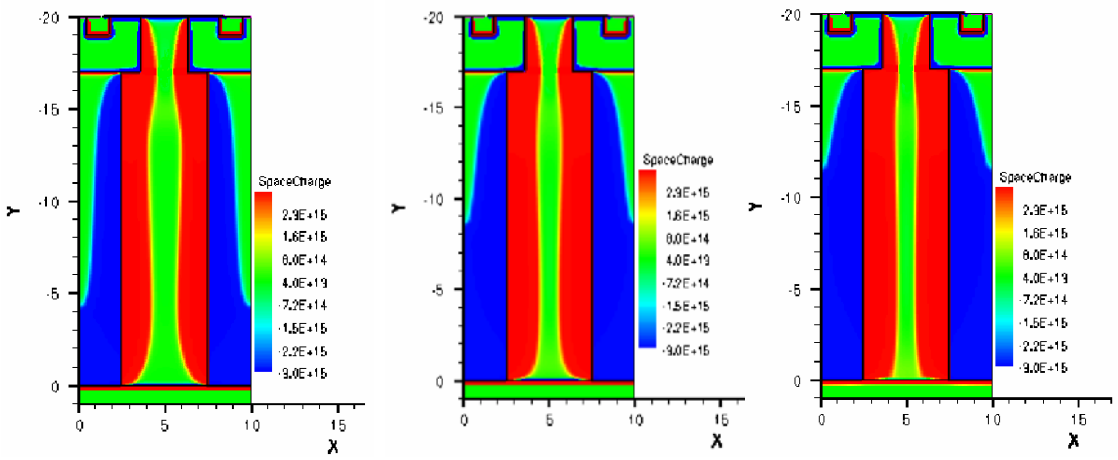
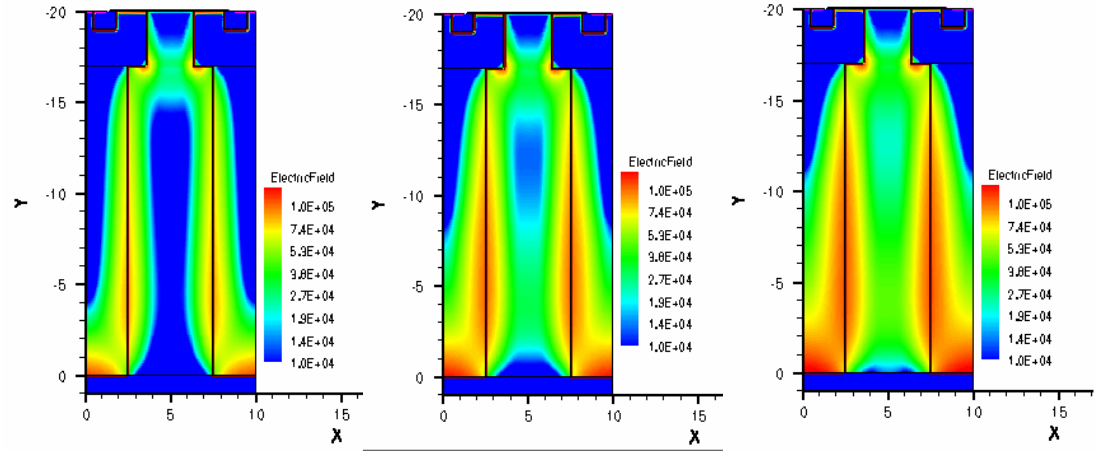


Fig. 4.17 Electron density along x = 5 within saturation condition



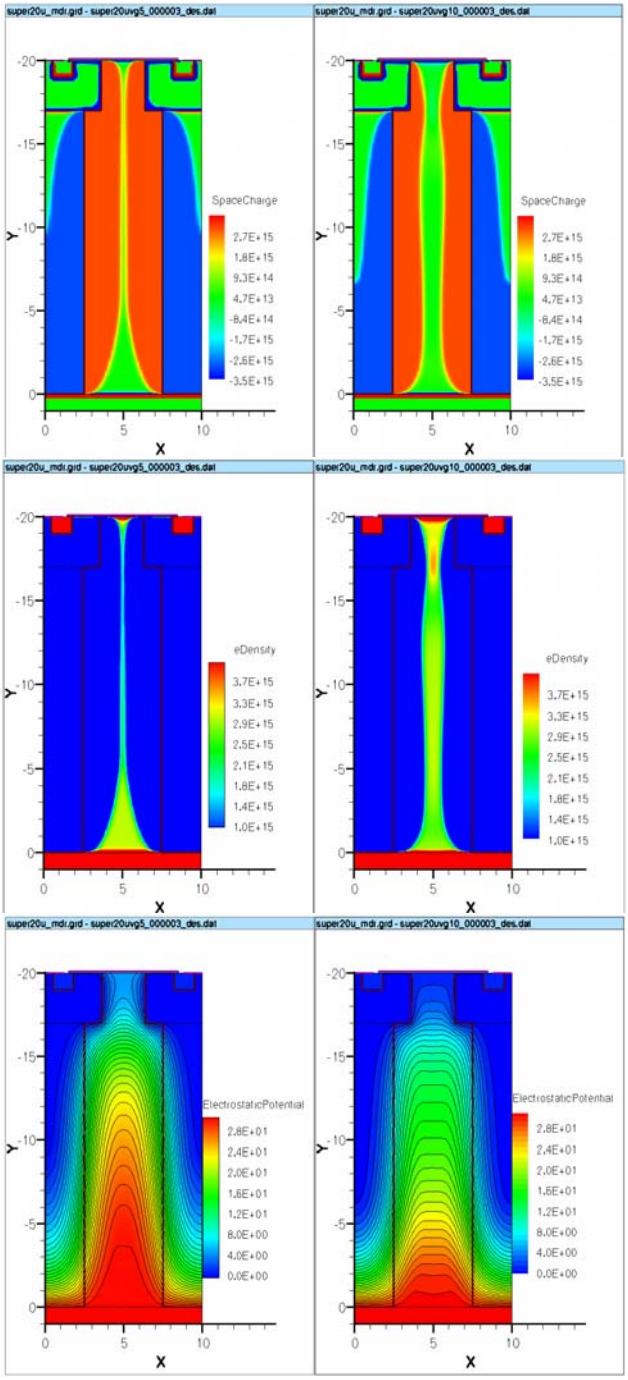
V_d =20 V **V_d = 40 V** **V_d = 60 V**

Fig. 4.18 The Space charge (cm^{-3}) distribution for Vg = 10 V



V_d =20 V **V_d = 40 V** **V_d = 60 V**

Fig. 4.19 The Electric Field (V/cm) distribution for Vg = 10 V



V_g = 5 V **V_g = 10 V**

Fig. 4.20 The space charge, electron density and potential distribution at V_d = 30 V

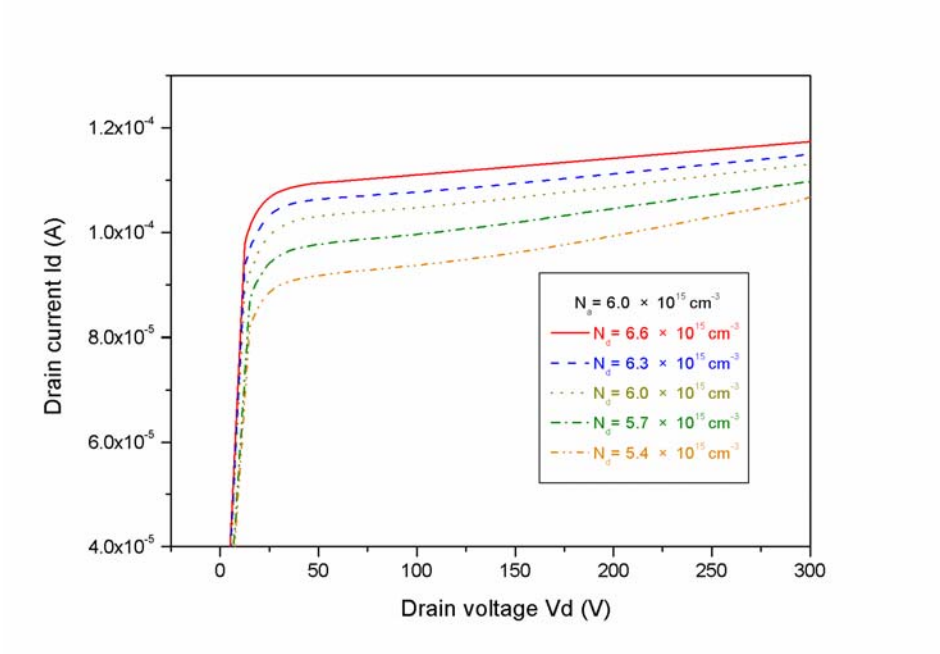


Fig. 4.21 The I_d-V_d curves at V_g = 15 V for pillar concentration imbalance

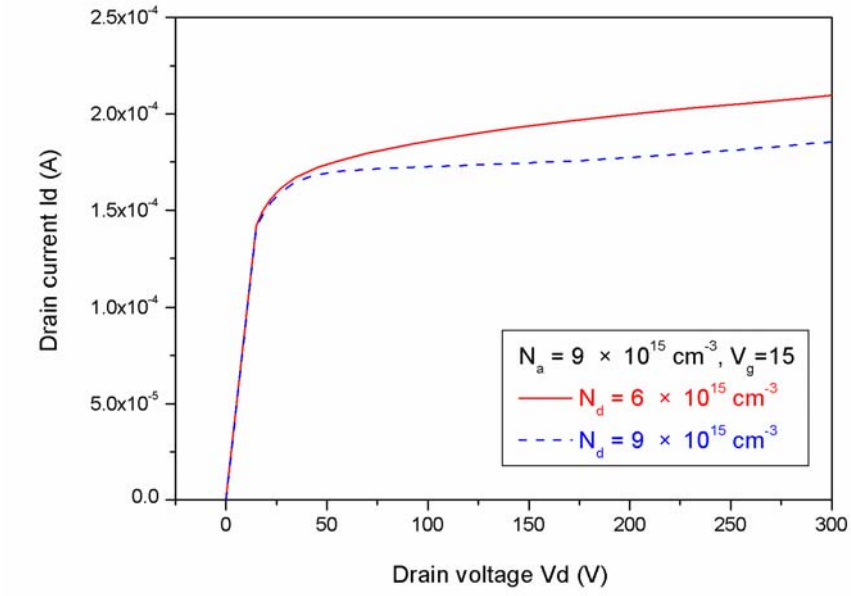


Fig. 4.22 The I_d-V_d curves at V_g = 15 V for pillar concentration different

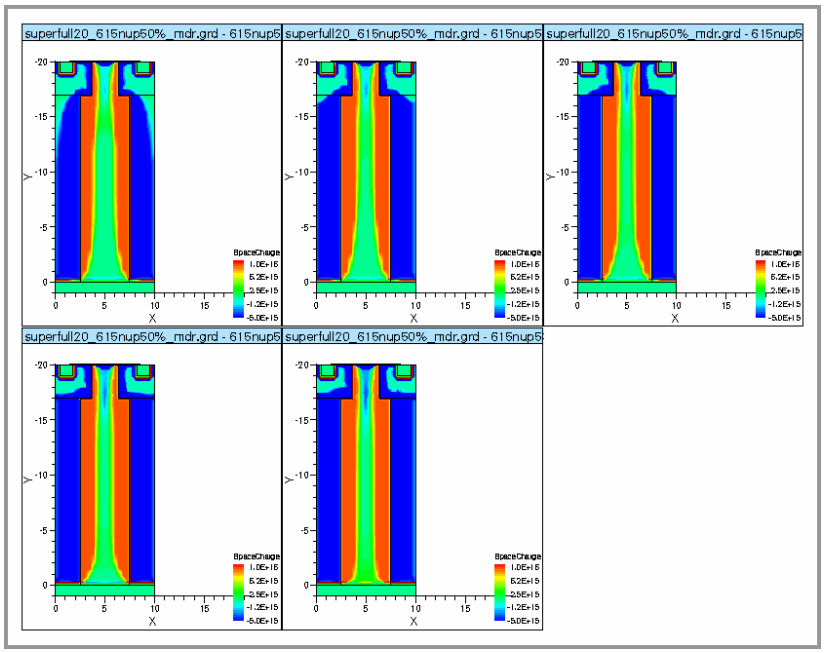


Fig. 4.23 The 2-D map of the space charge distribution at Vg = 15V for $N_a = 9\times10^{15}$ cm^{-3} and $N_d = 6\times10^{15}$ cm^{-3}

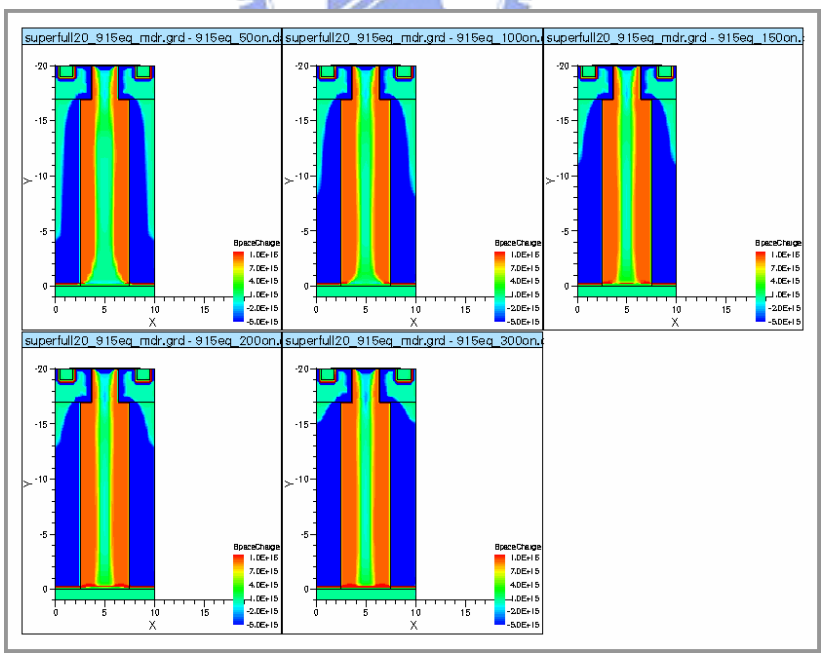


Fig. 4.24 The 2-D map of the space charge distribution at Vg = 15V for $N_a = 9\times10^{15}$ cm^{-3} and $N_d = 9\times10^{15}$ cm^{-3}

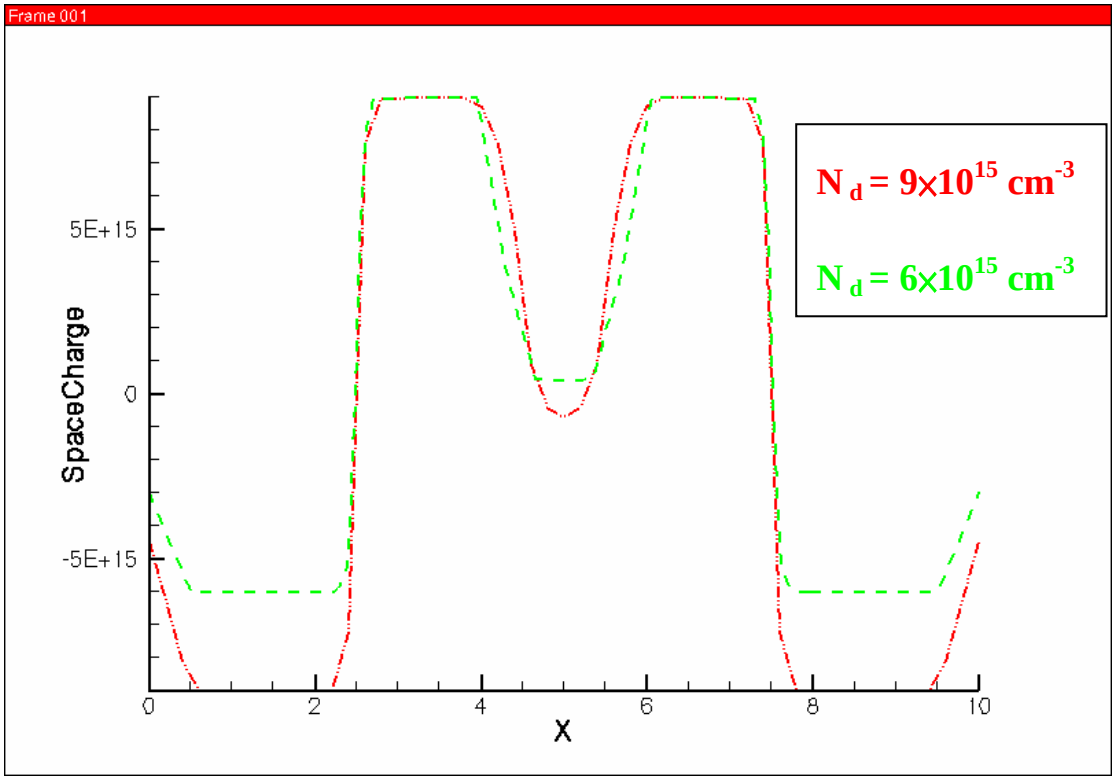


Fig. 4.25 Space charge distribution along y = -9 at V_d = 300 V

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