國 立 交 通 大 學

電子工程學系　電子研究所

碩 士 論 文

應用於超寬頻3.1-10.6GHz無線接收端之疊接回授架構與低功率電流再使用架構之低雜訊放大器之設計

Design of a cascode feedback and a low power current-reused LNA for Ultra-wideband 3.1 to 10.6GHz Wireless Receivers

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摘要

本論文研製一個應用於超寬頻 3.1-10.6 GHz 的低雜訊放大器是採用電阻-電容疊接回授架構分別為回授 1 與回授 2，以及低功率高增益的電流再使用架構。本研究是以 0.18 微米互補式金氧半製程實現。在回授 1 架構中，所量測到的平均順向增益為 5dB，逆向隔離為-32dB 以下，S11 為-7.5dB 以下，S22 約為-10dB 以下，而平均雜訊指數約為 8dB。在回授 2 架構中，所量測到的平均順向增益為 9dB，逆向隔離為-45dB 以下，S11 為-7.2dB 以下，S22 約為-8.2dB 以下，而平均雜訊指數約為 5.5dB。回授 1 與回授 2 架構均消耗功率 18mW。在電流再使用架構中，所量測到的平均順向增益為 9dB，逆向隔離為-50dB 以下，S11 為-8.6dB 以下，S22 約為-8dB 以下，而平均雜訊指數約為 5.2dB。此電路消耗功率僅為 9.4mW。

Design of a cascode feedback and a low power current-reused LNA for Ultra-wideband 3.1 to 10.6GHz Wireless Receivers

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Abstract

A 3.1-10.6GHz low noise amplifier is applied for ultra-wideband, it introduces by the cascode R-C feedback in feedback1 and feedback2 structure and a low power, high gain current-reused structure. This research is fabricated in 0.18-μm CMOS process. In feedback1 structure, the average forward S_{21} is 5dB, the reverse isolation S_{12} is under -32dB, the S_{11} is under -7.5dB, the S_{22} is under -10dB, and the noise figure is 8dB. In feedback2 structure, the average forward S_{21} is 9dB, the reverse isolation S_{12} is under -45dB, the S_{11} is under -7.2dB, the S_{22} is under -8.2dB, and the noise figure is 5.5dB. They all consume 18mW. In current-reused structure, the average forward S_{21} is 9dB, the reverse isolation S_{12} is under -50dB, the S_{11} is under -8.6dB, the S_{22} is under -8dB, and the noise figure is 5.2dB. The circuit power consumption is only 9.4mW.

誌謝

本論文得以完成,首先要感謝我的指導老師 荊鳳德 教授，在兩年的碩士研究生涯裡，給予我豐富的指導與照顧，不論是研究上與生活裡都讓我在這兩年裡獲得許多的收穫。

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最後，我要對我的父母獻上最高的敬意與謝意，感謝父母對我的栽培、支持與鼓勵，以及家人的陪伴，才讓我有機會能接觸這一切並且完成我的學業與研究。

Contents

Figure Captions

Chapter 1 Introduction

Chapter 2 Noise and Nonlinear effect in RF Design

Chapter 3 Design of UWB LNA with cascode feedback structure

Chapter 4 Design of a low power UWB LNA with current-reused structure

Chapter 5 Summary

Chapter 1

Introduction

1.1 Motivation

The allowance of the FCC regarding frequencies between 3GHz and 10GHz for Ultra-Wideband (UWB) applications has led to an increased level of interest and scope of research on this band and its various applications. The availability of such high bandwidth would allow higher data throughput up to 500Mbps in possible short distance, which is desirable for HDTV and other wireless multimedia applications. Apart from higher data rates, the other main features of UWB are lower cost and higher level of integrations. Several different approaches were proposed to establish a universal standard for this application [5].

LNA is the first stage in the receiver, after antenna in the receiver block of a communication system. It is widely used in the front-end of narrow band communication system. For UWB application, the criteria to judge its performances are slightly different. Whereas in narrowband systems there is tight requirement on linearity, this parameter is relaxed in UWB wireless systems, which ranges from 3.1GHz to 10.6GHz, because transmitted power spreads over a wide range and is restricted to be less than -41.3dBm per MHz, The most important requirement for UWB applications are input impedance match, low power consumption, low noise

performance, enough gain to suppress noise of the next stages and small size.

For the overwhelming majority DSP chips, most designer introduces the CMOS process to achieve system on chip (SOC). But for analog and radio frequency chips, due to the electricity, noise and other parameters have strict demands. In order to achieve the specification of the products, different communication systems have different demands in process. In the past, due to GaAs process has excellent high frequency parameters, so most designer introduces the GaAs process to design theirs products. But the deep sub-micro CMOS process has acceptable high frequency parameters. Recently there are designers introduce 0.18 micrometer, 0.13 micrometer or 0.09 micrometer CMOS process to design radio frequency transceivers. Because CMOS process's cost is less expensive than other process's. And that radio frequency transceiver introduces CMOS process is facile integration with base-band circuit. Achieving perfection of the SOC is feasible in future.

In the second section, we will analyze the noise effect and the nonlinear effect in the ratio frequency integrated circuit design. In the section three, a cascode R-C feedback structure will be introduced. Then, the forth section, is another structure, a low power current-reused LNA. It consumes very low power, in the LNA core only 7mW. It also has good input matching and high gain. Finally, in the section five, we will summarize a conclusion to our study.

Chapter 2

Noise and Nonlinear effect in RF Design

2.1 Noise

Noise is usually generated by the random motions of charges or charge carriers in devices and materials. Because the noise process is random, one cannot identify a specific value of voltage at a particular time, and the only recourse is to characterize the noise with statistical measures, such as the mean-square or root-mean-square values. Because of having various noise sources in the circuit, we need to simplify calculation of the total noise at the output [2]. Obviously, the output-referred noise does not allow a fair comparison of the performance of different circuits because it depends on the gain. According the circuit theory, we can use the input-referred noise of circuits to represent the noise of behavior in the circuits. To overcome the above confusion, we specify the “input-referred noise” of circuits. Illustrate conceptually in Fig. 2-1. To represent the effect of all noise sources in the circuit by a single noise source. The input-referred noise and the input signal are both multiplied by the gain as they are processed by the circuit. Thus, the input-referred noise indicates how much the input signal is corrupted by the circuit’s noise. The input-referred noise is a spurious quantity in that in cannot be measured at the input of the circuit. The two circuits of Figs. 2-1(a) and (b) are equivalent in mathematics but the real physical

circuit is still that in Fig. 2-1(b). The noise of a two-port network can be modeled by two input noise sources: a series voltage source and a parallel current source.

Generally, the correlation between the two sources must be taken into account. The situation is shown in Fig. 2-2, where a two-port network containing noise sources is represented by the same network with internal noise sources removed and with a noise voltage and current source connected at the input. It can be shown that this representation is valid for any source impedance, provided that correlation between the two noise sources is considered [3].

The signal-to-noise ratio (SNR), defined as the ratio of the signal power to the total noise power, is an important parameter. In RF circuit, most of the front-end receiver blocks are characterized in terms of their "noise figure" rather than the input-referred noise. Noise figure has many different definitions. The most commonly accepted definition is

$$\text{noise figure} = \frac{SNR_{in}}{SNR_{out}}, \tag{1}$$

Noise figure is a measure of how much the SNR degrades as the signal passes through a circuit. If a circuit has no noise source, the $SNR_{out} = SNR_{in}$, regardless of the gain.

The noise figure of a two-port amplifier is given by

$$F = F_{\min} + \frac{r_n}{g_s}\left|y_s - y_{opt}\right| \tag{2}$$

where $r_n = R_n / Z_0$ is the equivalent normalized noise resistance of the two-port, $y_s = R_n / Z_0 = g_s + jb_s$ represents the normalized source admittance, and $y_{op\ t} = g_{opt} + jb_{opt}$ represents the normalized source admittance which results in the minimum noise figure, called F_{min}.

If we express y_s and y_{opt} in terms of the reflection coefficients Γ_s and Γ_{opt}.

$$y_s = \frac{1-\Gamma_s}{1+\Gamma_s} \tag{3}$$

$$y_{opt} = \frac{1-\Gamma_{opt}}{1+\Gamma_{opt}} \tag{4}$$

Substitute (3) and (4) into (2) results in the relation

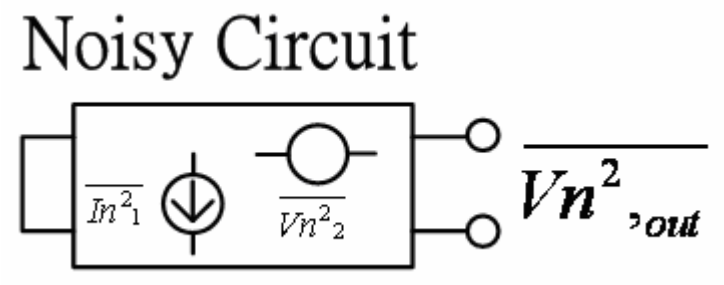
$$F = F_{\min} + \frac{4r_n\left|\Gamma_s - \Gamma_{opt}\right|^2}{(1-\left|\Gamma_s\right|^2)\left|1+\Gamma_{opt}\right|^2} \tag{5}$$

When $\Gamma_s=\Gamma_{opt}$ occurs, the value of F is equal to F_{min}. F_{min} is a function of the device bias current and operating frequency [4].

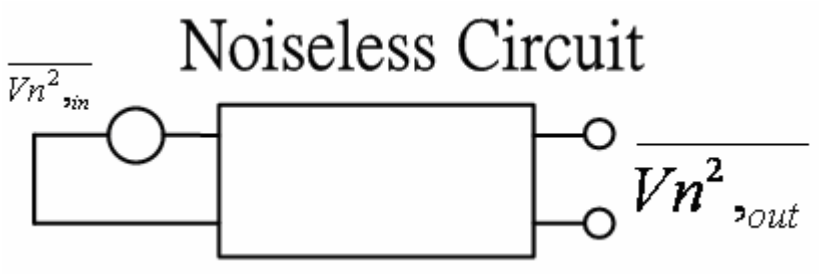
For a cascade of stages, the overall noise figure can be obtained in terms of the NF and gain of each stage. For m-stages, the NF_{tot} is equal to

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1}\cdots A_{p(m-1)}} \tag{6}$$

where A_{pm} is the available power gain of the m-th stage. This is called the Friis equation. The Friis equation indicates that the noise contributed by each stage decreases as the gain preceding the stage increases, implying that the first few stages in a cascade are the most critical [1].

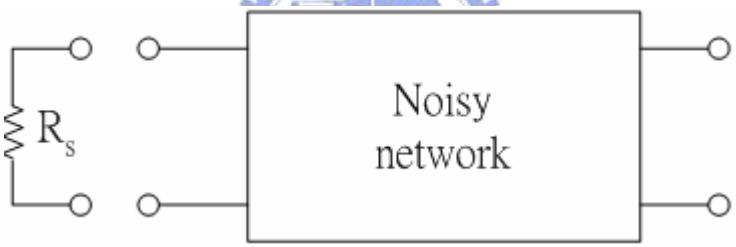


(a)

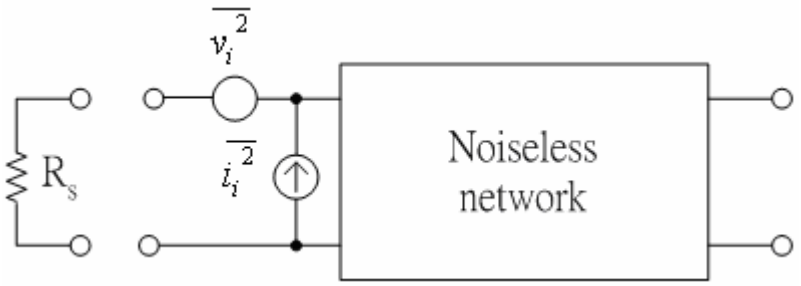


(b)

Fig. 2-1 Determination of input-referred noise voltage.



(a)



(b)

Fig. 2-2 Representation of noise in a two-port network by equivalent input voltage and current sources.

2.2 Nonlinear effect

While many RF circuits can be approximated with a linear model to obtain their response to small signals, nonlinearities often lead to interesting and important phenomena. For simplicity, we assume that

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{7}$$

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. If $x(t) = A\cos\omega t$, then

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t \tag{8}$$

$$= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \tag{9}$$

In Eq. (9), then term with the input frequency is called the "fundamental" and the higher-order terms the "harmonics." The amplitude of the *n*th harmonic consists of a term proportional to A^n.

In (9) this occurs if $\alpha_3 < 0$. Written as $\alpha_1 + \frac{3\alpha_3 A^2}{4}$, the gain is therefore a decreasing function of A. In most circuits, the output is a "compressive" or "saturating" function of the input; that is, the gain approached zero for sufficiently high input levels. This effect is quantified by the "1-dB compression point," defined as the input signal level that causes the small-signal gain to drop by 1 dB. If plotted on a log-log scale as a function of the input level, the output level falls below its ideal

value by 1 dB at the 1-dB compression point.

When two signals with different frequencies are applied to a nonlinear system, the output in general exhibits some components that are not harmonics of the input frequencies. Called intermodulation (IM), this phenomenon arises from multiplication of the two signals when their sum is raised to a power greater than unity. We assume that

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \tag{10}$$

Thus,

$$y(t) = \alpha_1 (A_1 \cos\omega_1 t + A_2 \cos\omega_2 t) + \alpha_2 (A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^2 + \alpha 3 (A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^3 \tag{11}$$

Expanding the left side and discarding DC terms and harmonics, we obtain the intermodulation products:

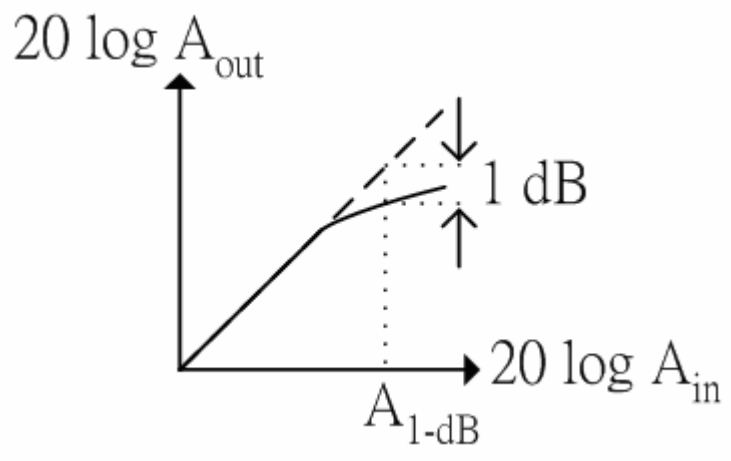
$$\omega \to 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^{\,2} A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^{\,2} A_2}{4} \cos(2\omega_1 - \omega_2)t \tag{12}$$

$$\omega \to 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_2^{\,2} A_1}{4} \cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_2^{\,2} A_1}{4} \cos(2\omega_2 - \omega_1)t \tag{13}$$

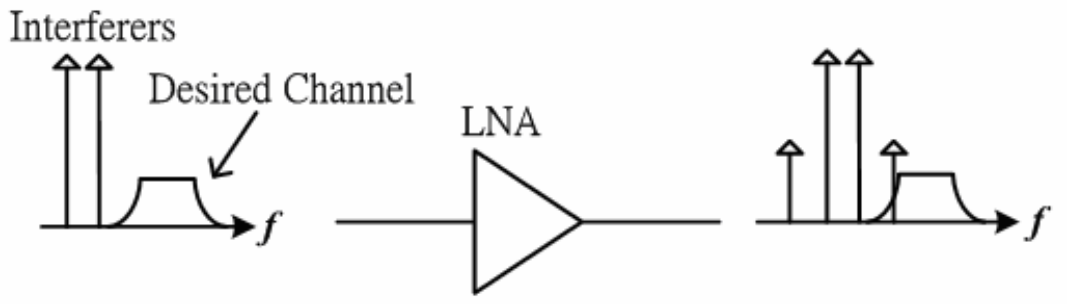
Because the difference between ω_1 and ω_2 is small, the components at $2\omega_1$-ω_2 and $2\omega_2$-ω_1 appear in the vicinity of ω_1 and ω_2. In a typical two-tone test, A_1=A_2=A, and the ratio of the amplitude of the output third-order products to α_1A defines the IM distortion. If a weak signal accompanied by two strong interferers experiences third-order nonlinearity, then one of the IM products falls in the band of

interest, corrupting the desired component.

Use IP_3 to characterize this behavior. Called the “third intercept point” (IP_3), this parameter is measured by a two-tone test in which A is chosen to be sufficiently small so that higher-order nonlinear terms are negligible and the gain is relatively constant and equal to α_1. The third-order intercept point is defined to be at the intersection of the two lines [1].



(a)



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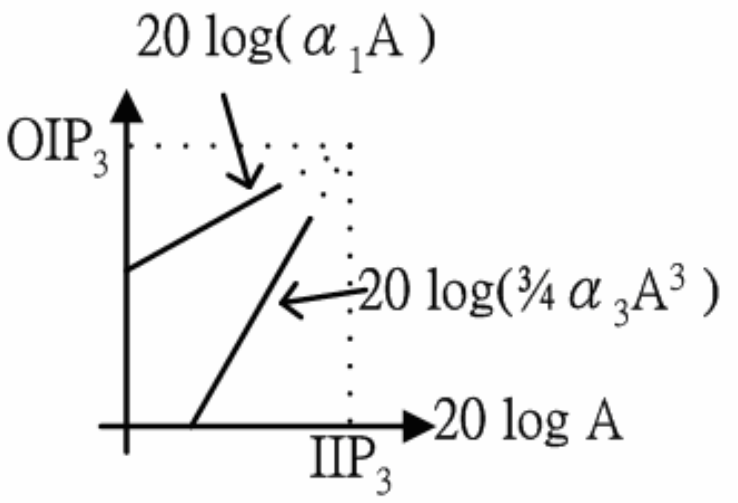


(c)

Fig. 2-3 (a) Definition of the 1-dB compression point, (b) Corruption of a signal due to intermodulation, (c) The third-order intercept point.

2.3 Cascaded Nonlinear Stages

Since in RF systems, signals are processed by cascaded stages, it is important to know how the nonlinearity of each stage is referred to the input of the cascade. Consider two nonlinear stages in cascade. As shown in Fig.2-4. Assuming that the input-output relationship is

$$y_1(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{14}$$

$$y_2(t) = \beta_1 y_1(t) + \beta_2 y_1{}^2(t) + \beta_3 y_1{}^3(t) \tag{15}$$

Substitute (14) into (15) results in the relation

$$y_2(t) = \alpha_1\beta_1 x(t) + (\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1{}^3\beta_3)x^3(t) \tag{16}$$

If we consider only the first- and third-order terms, then

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1\beta_1}{\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1{}^3\beta_3}\right|}. \tag{17}$$

From equation (17) can be simplified if the two sides are inverted and squared:

$$\frac{1}{A^2_{IP3}} = \frac{1}{A^2_{IP3,1}} + \frac{3\alpha_2\beta_2}{2\beta_1} + \frac{\alpha_1{}^2}{A^2_{IP3,2}}, \tag{18}$$

where $A_{IP3,1}$ and $A_{IP3,2}$ represent the input IP_3 points of the first and second stages, respectively. From the above result, we note that as α_1 increases, the overall IP_3 decreases. This is because with higher gain in the first stage, the second stage senses larger input levels, thereby producing much greater IM_3 products [1].

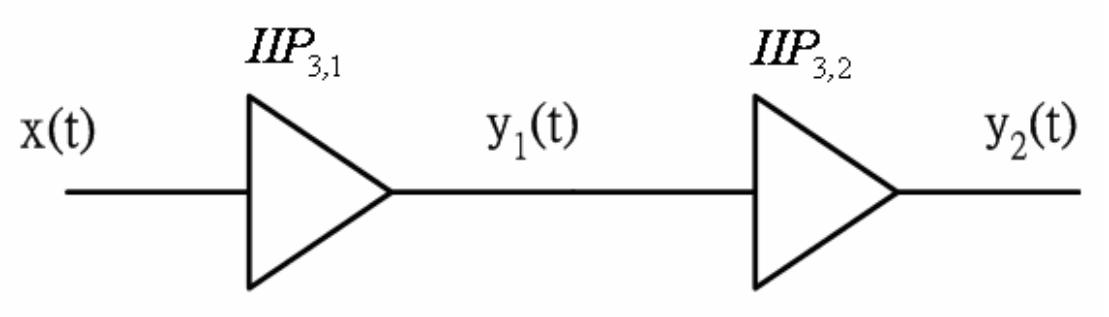


Fig. 2-4 Cascaded nonlinear stages.

Chapter 3

Design of UWB LNA with cascode feedback structure

3.1 Circuit topology

In designing a broadband amplifier, feedback and distributed configuration are most widely used. In the chapter, feedback configuration was used instead of distributed configuration because it is more adequate for integration due to better uniformity and stability at frequencies below 12GHz. In addition, the cascode structure has been considered as the best topology for wideband applications because of its advantages [11].

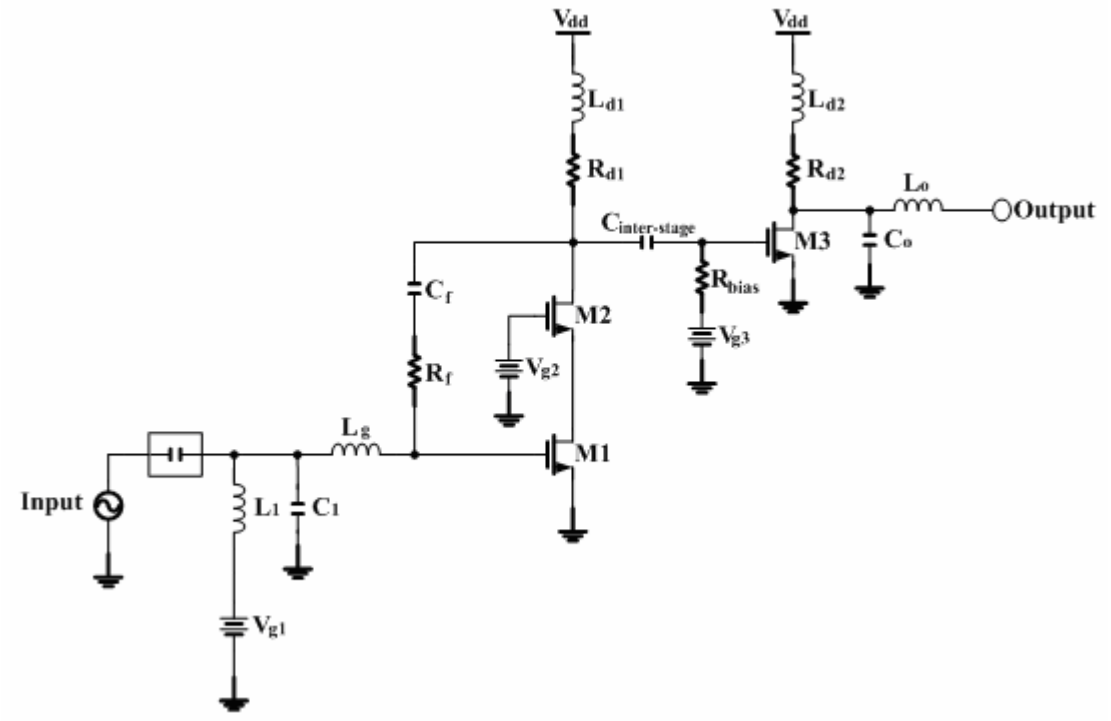
We design UWB LNA with cascode R-C feedback structure. There are two types in this structure. The feedback1 structure is the R-C feedback connected between Lg and MOS1's gate, like Fig. 3-1(a). The feedback2 structure is the R-C feedback connected between input and Lg, like Fig. 3-1(b).

From Fig. 3-1 (a) and (b), we can observe that they are two stage low noise amplifier. First stage used the cascode R-C feedback structure. The advantages of cascode structure are high gain, wider bandwidth, better stability and reverse isolation. The cascode configuration is being used to reduce the high frequency roll-off of the input devices due to the Miller effect [11]. It can also be performed the input/output matching independently. The R-C feedback (R_f & C_f) in cascode circuit improves the

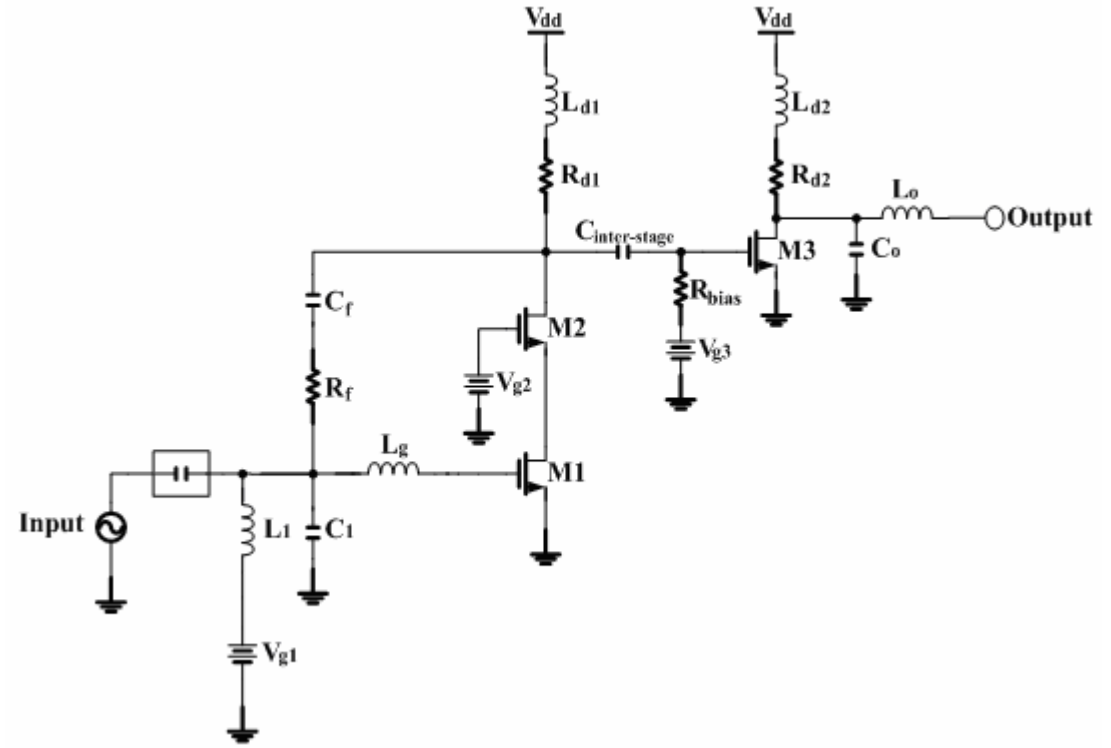
S11 of the circuit and stabilizes the common-gate without reducing the gain. Above all, it can satisfy the requirements of wideband system for both noise and power simultaneously by carefully feedback resistance.

The MOS M1 dominates the noise performance. These two MOS (M1 and M2) have little effects with each other.

The two LNA (feedback1 and feedback2) for UWB applications were designed using TSMC 0.18um RF CMOS technology.



(a)



(b)

Fig. 3-1 Proposed UWB LNA schematic (a) feedback1, (b) feedback2.

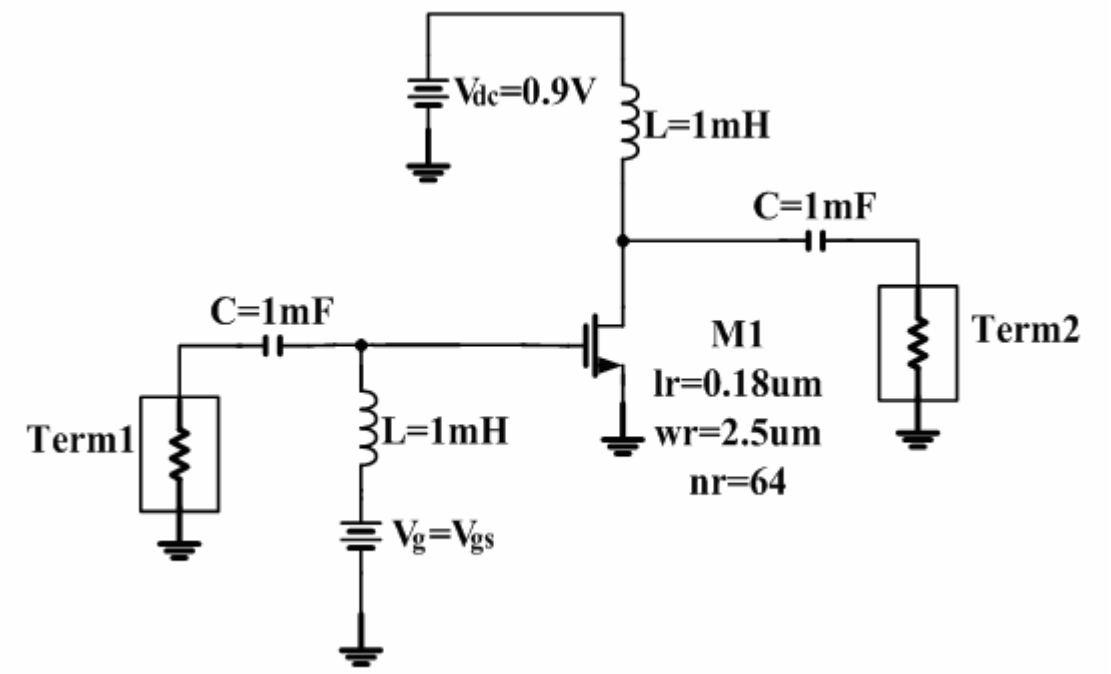
3.2 Design procedures

3.2.1 Transistor sizing and bias condition

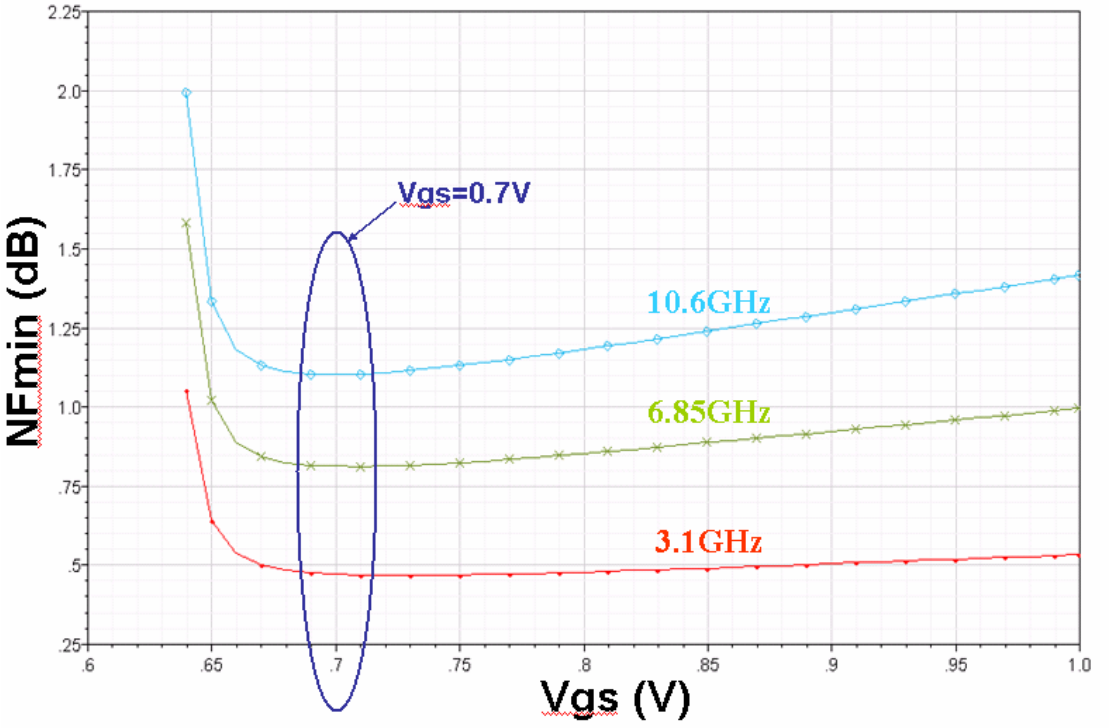
Since the size of transistor and bias condition determine the power dissipation, it is often recommended to decide them with a certain power budget. However, we should evaluate the size of the transistor versus bias condition carefully, because they are also related to the impedance seen by the input gate. Thus, the first choice is to determine the size and bias condition that satisfies both impedance and noise matching with limited bias current.

Fig. 3-2(a) shows a simulation circuit of MOS NFmin. In Fig. 3-2(a), the input transistor M1 (W/L = 160/0.18 um) is chose and is biased at 7.5mA. In Fig. 3-1(a) and (b), the size of the cascode transistor M2 (W/L = 64/0.18 um) is decided considering a trade-off between gain (S_{21}) and -3dB bandwidth. The size of the second stage transistor M3 is W/L = 64/0.18 um. The total power consumption is 18.8mW.

Fig. 3-2(b) shows the Vgs versus NFmin at 3.1GHz, 6.85GHz and 10.6GHz. From Fig. 3-2(b), we can observe that when Vgs = 0.7V, the transistor M1 has the minimum noise figure. Thus, the bias condition is decided to Vgs = 0.7V.



(a)



(b)

Fig. 3-2 (a) Simulation circuit of MOS NFmin, (b) Vgs v.s. NFmin at 3.1GHz、6.85GHz and 10.6GHz.

3.2.2 Noise analysis

The noise performance of the R-C cascode feedback topology is determined by three main contributors: the feedback resistor Rf, the gate inductor Lg and the noise of the amplifying device M1. The optimization of the noise contribution from M1 relies on the choice of its width for a given bias current.

MOS transistor noise sources are shown in Fig. 3-3(a). The noise generator $\overline{i^2_d}$ is

$$\overline{i^2_d} = 4kT\left(\frac{2}{3}g_m\right)\Delta f + k\frac{I^a{}_D}{f}\Delta f \tag{19}$$

where $4kT\left(\frac{2}{3}g_m\right)\Delta f$ is thermal noise component, and $k\frac{I^a{}_D}{f}\Delta f$ is flicker noise component. And noise generator $\overline{i^2_g}$ is

$$\overline{i^2_g} = 2qI_G\Delta f \tag{20}$$

The input-referred in a conventional way and replaced with two correlated noise generators, as shown in Fig. 3-3(b), because the current gain of the source degeneration is $\beta(j\omega) = \frac{\omega_T}{j\omega}$, and the cutoff frequency is $\omega_T \approx \frac{g_m}{C_{gs}}$, so the $\overline{i^2_{ia}}$ is

$$\overline{i^2_{ia}} = \overline{i^2_g} + \frac{j\omega C_{gs}}{g_m}\overline{i^2_d} \tag{21}$$

and $\overline{v^2_{ia}}$ is

$$\overline{v^2_{ia}} = \frac{\overline{i^2_d}}{g_m} \tag{22}$$

Fig. 3-4(a) and (b) show the equivalent circuit of the input stage for noise calculation.

In Fig. 3-4(a), the feedback1 topology:

$$v_{ib1} = v_{ia} \tag{23}$$

$$i_{ib1} = i_{ia} + i_f \tag{24}$$

Then,

$$v_{i1} = v_{ib1} + i_{ib1} \cdot R_{Lg} + v_{Lg} = v_{ia} + i_{ia} \cdot R_{Lg} + v_{Lg} + i_f \cdot R_{Lg} \tag{25}$$

$$i_{i1} = i_{ib1} = i_{ia} + i_f \tag{26}$$

Thus, the total equivalent noise voltage and current of feedback1 is

$$\overline{v^2_{i1}} = \overline{v^2_{ia}} + \overline{v^2_{Lg}} + \overline{i^2_{ia}} \cdot {R_{Lg}}^2 + \overline{i^2_f} \cdot {R_{Lg}}^2 \tag{27}$$

$$\overline{i^2_{i1}} = \overline{i^2_{ia}} + \overline{i^2_f} \tag{28}$$

In Fig. 3-4(b), the feedback2 topology:

$$v_{ib2} = v_{ia} + i_{ia} \cdot R_{Lg} + v_{Lg} \tag{29}$$

$$i_{ib2} = i_{ia} \tag{30}$$

Then,

$$v_{i2} = v_{ib2} = v_{ia} + i_{ia} \cdot R_{Lg} + v_{Lg} \tag{31}$$

$$i_{i2} = i_{ib2} + i_f = i_{ia} + i_f \tag{32}$$

Thus, the total equivalent noise voltage and current of feedback2 is

$$\overline{v^2_{i2}} = \overline{v^2_{ia}} + \overline{v^2_{Lg}} + \overline{i^2_{ia}} \cdot {R_{Lg}}^2 \tag{33}$$

$$\overline{i^2_{i2}} = \overline{i^2_{ia}} + \overline{i^2_f} \tag{34}$$

where

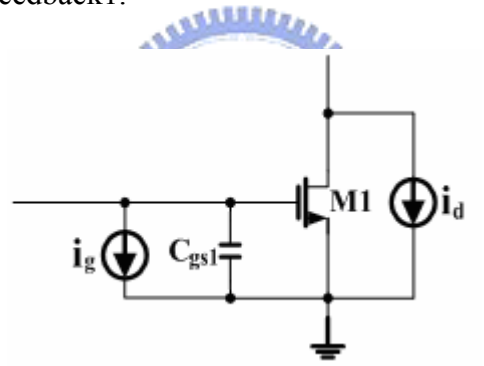
$$\overline{i^2{}_f} = 4kT\frac{1}{R_f}\Delta f \tag{35}$$

$$\overline{v^2{}_{Lg}} = 4kTR_{Lg}\Delta f \tag{36}$$

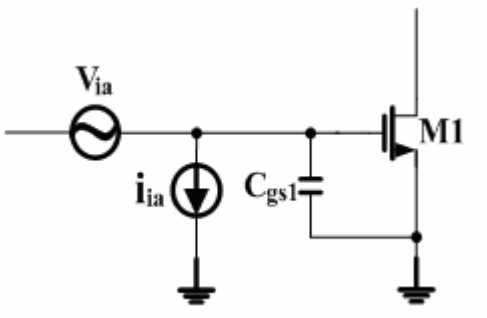
The noise factor is

$$F = 1 + \frac{\overline{v^2{}_i}}{4kTR_S\Delta f} + \frac{\overline{i^2{}_i}}{4kT\frac{1}{R_S}\Delta f} \tag{37}$$

From equation (27) and (33), we can observe that the total noise of feedback1 is greater than feedback2 due to the $\overline{i^2{}_f} \cdot R_{Lg}{}^2$ item. Fig. 3-5 shows the noise figure: feedback1 versus feedback2. We can observe that the noise figure of feedback2 topology is better than feedback1.



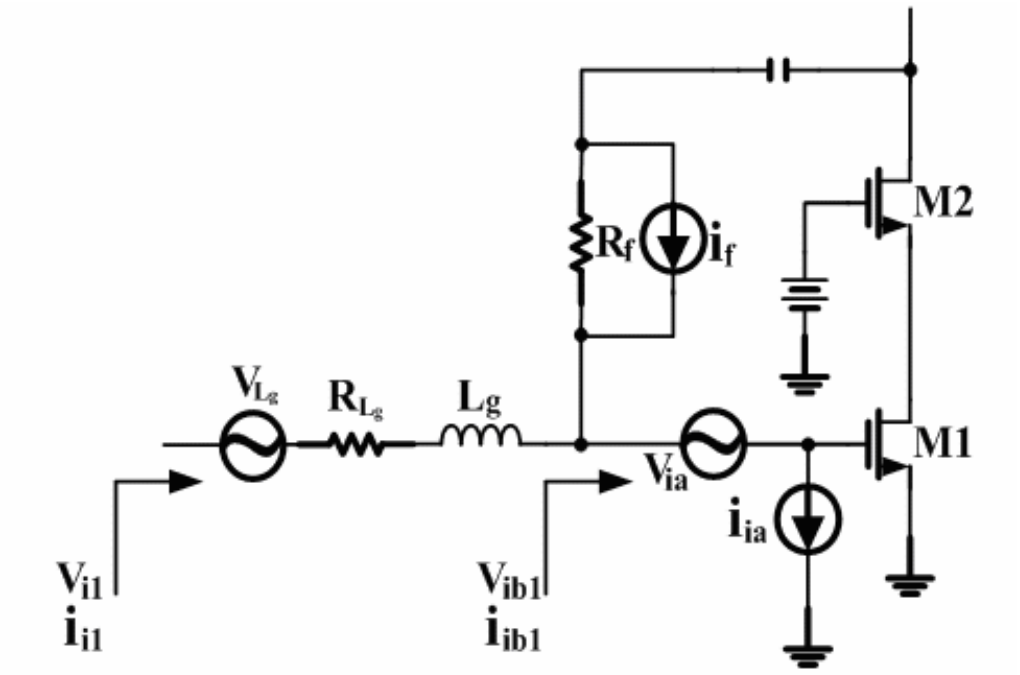
(a)



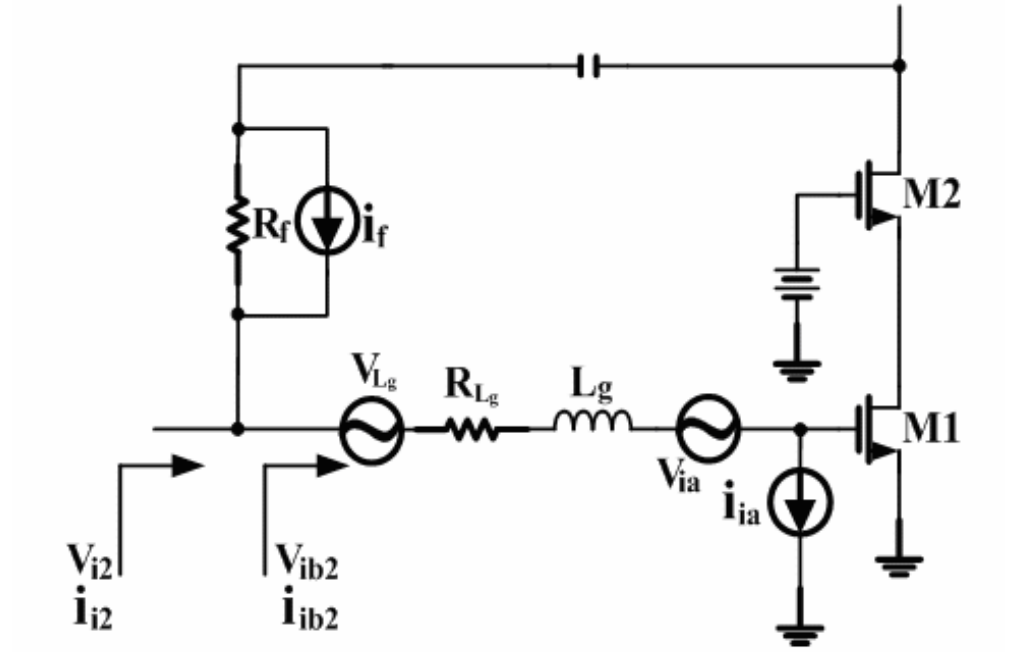
(b)

Fig. 3-3 Noise model for the amplifying transistor M1 (a) M1 noise sources,

(b) Input-referred equivalent noise generators.



(a)



(b)

Fig. 3-4 Equivalent circuit of the input stage for noise calculation

(a) feedback1, (b) feedback2.

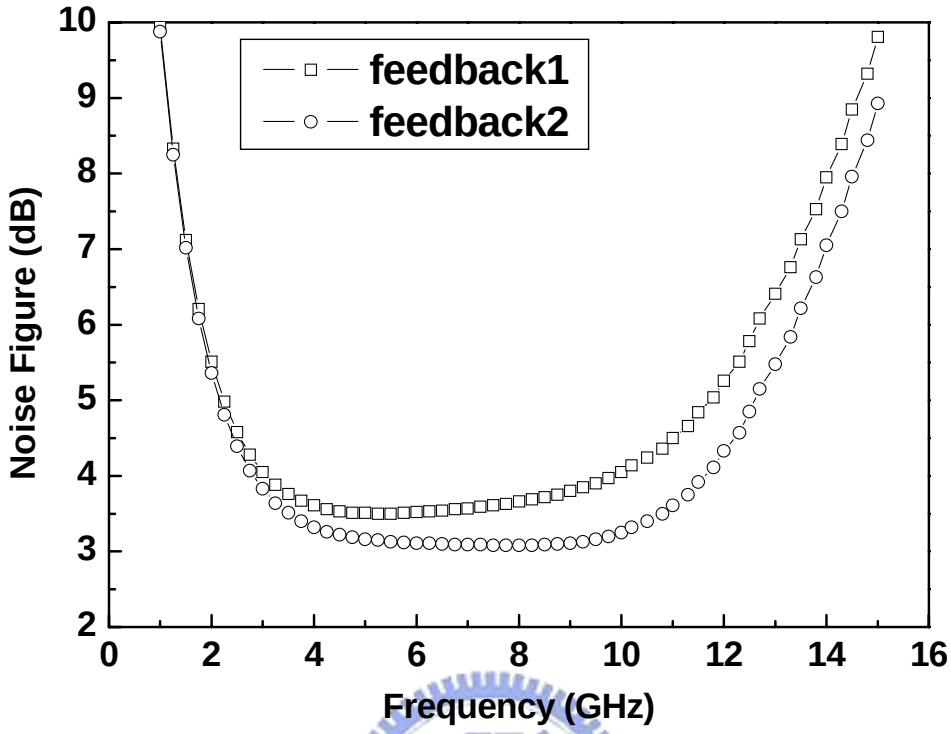


Fig. 3-5 Noise figure: feedback1 v.s. feedback2.

3.2.3 Input and output match

Input matching:

In feedback1 topology, the small signal equivalent is shown in Fig. 3-6(a), where

$$Z'_{in} = 1/sC_{gs1} \tag{38}$$

$$Z_1 = sL_1 // 1/sC_1 \tag{39}$$

$$Z_2 = sL_g \tag{40}$$

$$g_{m,eff} \cong g_{m1} \times 1 = g_{m1} \tag{41}$$

$$Z_L = R_{d1} + sL_{d1} \tag{42}$$

$$Z_f = R_f + 1/sC_f \tag{43}$$

For this configuration, the input impedance and the gain can be calculated to be

$$Z_{in1} = \left[\frac{Z'_{in} \cdot Z_f}{Z_f + (A_V - 1) \cdot Z'_{in}} + Z_2 \right] // Z_1 \tag{44}$$

$$A_{V1} = \frac{Z_L + g_{m,eff} \cdot Z_f \cdot Z_L}{Z_L - Z_f} \tag{45}$$

And in feedback2 topology, the small signal equivalent is shown in Fig. 3-6(b), where

$$Z'_{in} = sL_g + 1/sC_{gs1} \tag{46}$$

Z_1, Z_L, Z_f and $g_{m,eff}$ are the same with feedback1. For this configuration, the input impedance and the gain can be calculated to be

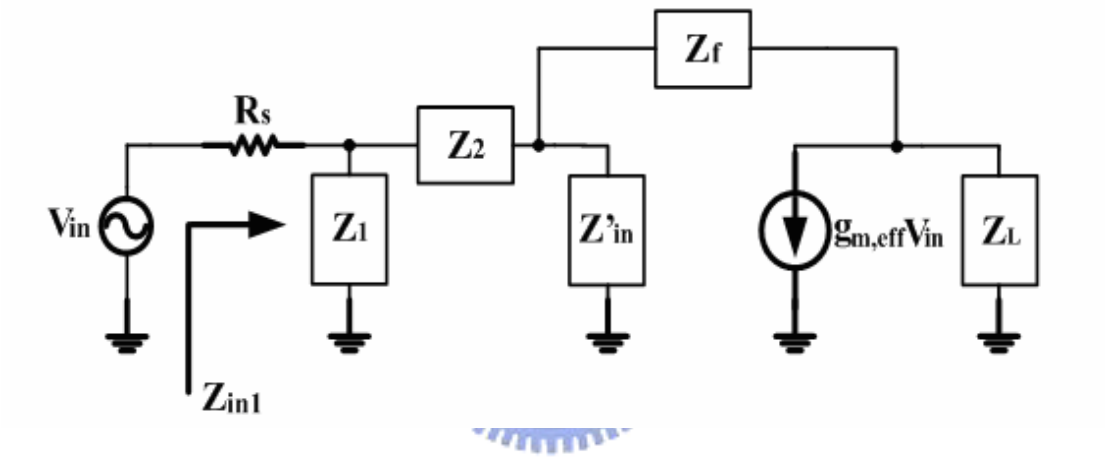
$$Z_{in2} = \left[\frac{Z'_{in} \cdot Z_f}{Z_f + (A_V - 1) \cdot Z'_{in}} \right] // Z_1 \tag{47}$$

$$A_{V2} = \frac{Z_L + g_{m,eff} \cdot Z_f \cdot Z_L}{Z_L - Z_f} \tag{48}$$

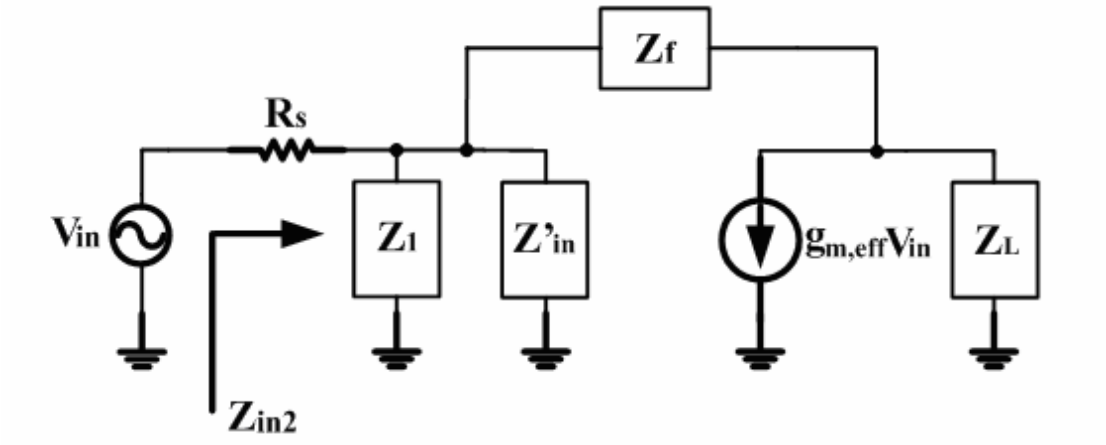
Since the circuit parameters Z'_{in} and A_V are frequency dependant, the characteristics of Z_f will vary accordingly over the frequency band. Thus, select Z_f and combination of R、C components，perfect matching and gain can be achieved.

Output matching:

The second stage is decided to use L-C section for output match.



(a)



(b)

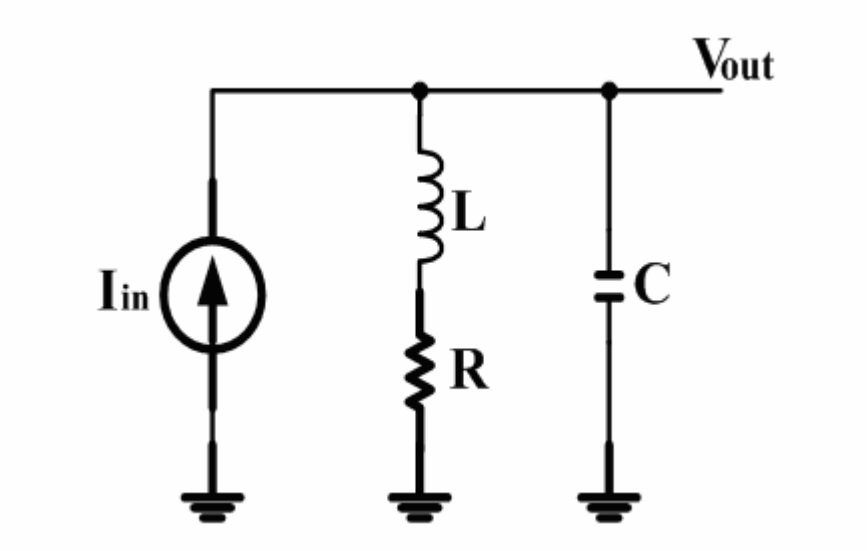
Fig. 3-6 (a) Feedback1 configuration, (b) Feedback2 configuration.

3.2.4 Shunt peaking

A model of shunt peaking amplifier is shown in Fig. 3-7(a). The capacitance *C* may be taken to represent all the loading on the output node, including that of a subsequent stage. The resistance *R* is the effective load resistance at that node and the inductor provides the bandwidth enhancement. It's clear from the model that the transfer function v_{out}/i_{in} is just the impedance of the *RLC* network, so it should be straightforward to analyze. The addition of an inductance in series with the load resistor provides an impedance component that increases with frequency, which helps offset the decreasing impedance of the capacitance, leaving net impedance that remains roughly constant over a broader frequency range than that of the original *RC* network. The impedance of the *RLC* network may be written as

$$Z(s) = (sL + R) // \frac{1}{sC} = \frac{R[s(L/R)] + 1}{s^2 LC + sRC + 1} \tag{49}$$

The load is designed to achieve flat gain over the whole bandwidth. The choice of L_d is determined by two opposite requirements: L_d must be sizable to have large gain and must be small so that it resonates C_{out} out of band [9]. R_d is chosen to place the zero frequency ($\omega_z = R_d/L_d$) as close as to the lower edge of the band to improve the gain. We choose $R_d = 90\Omega$ and $L_d = 1.7nH$ so that $\omega_z \cong 8.5GHz$. The shunt peaking is shown in Fig. 3-7(b).



(a)

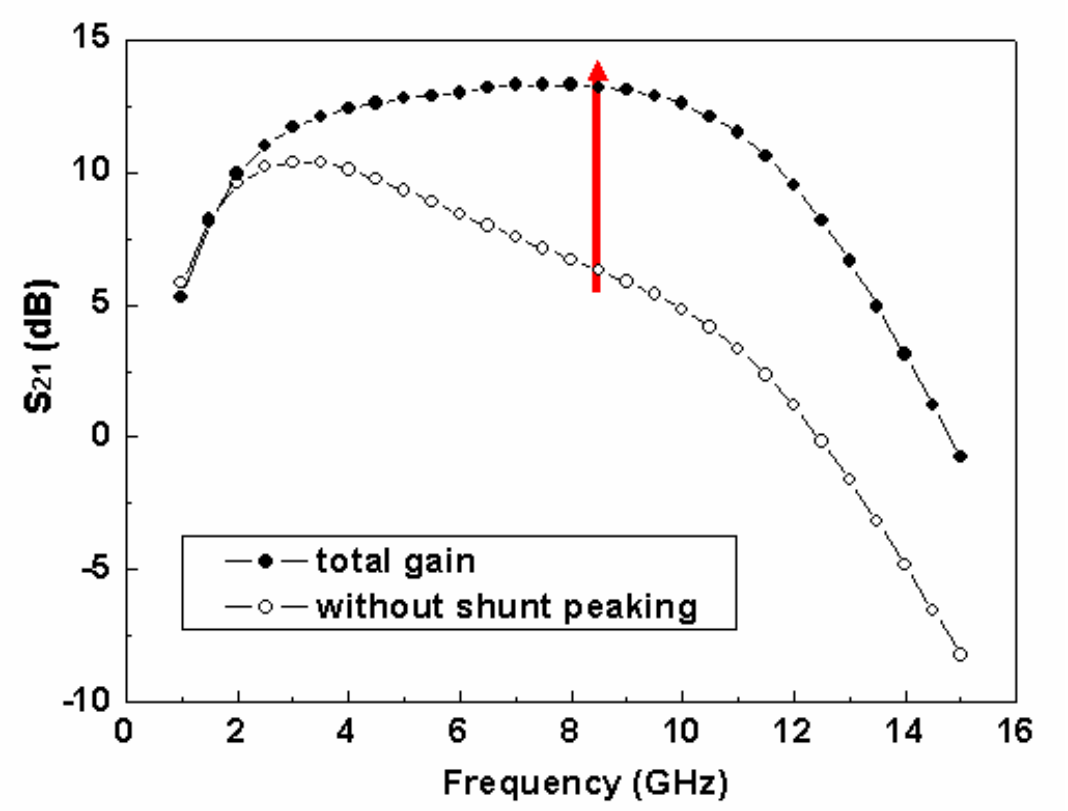


Fig. 3-7 (a) Model of shunt-peaked amplifier, (b) Gain compare with shunt-peaking.

3.3 Simulation and Measurement Result

Fig. 3-8 shows the s-parameters of simulation and measurement in feedback1 and feedback2. Fig. 3-9 shows the noise figure and Fig. 3-10 shows the linearity. Fig. 3-11 is the die photo.

In feedback1, the forward gain (S_{21}) is less than simulation about 5dB due to the L1 without connecting bypass capacitors and process variation. When measured, the Vg1 dc probe without bypass capacitors may cause signal loss and have parasitical effects so that the gain is less than simulation. And, the ripple in 3 to 6GHz is due to the M2's gate bypass capacitor layout which cause parasitic inductor and capacitor resonated in 3 to 6GHz. The reverse isolation (S_{12}) is below -32 dB. The magnitude of S_{11} is below -7.5dB and S_{22} is below -10dB in entire operation frequency band. The S_{12}, S_{11} and S_{22} are very close to the simulation result. The average noise figure is about 8dB and the minimum noise figure is 6.7dB at 5GHz. The IIP3 is 2dBm at 5.5GHz. The total power consumption is about 18mW with a power supply of 1.8 volts. And the die area including the pads is 0.77 mm^2.

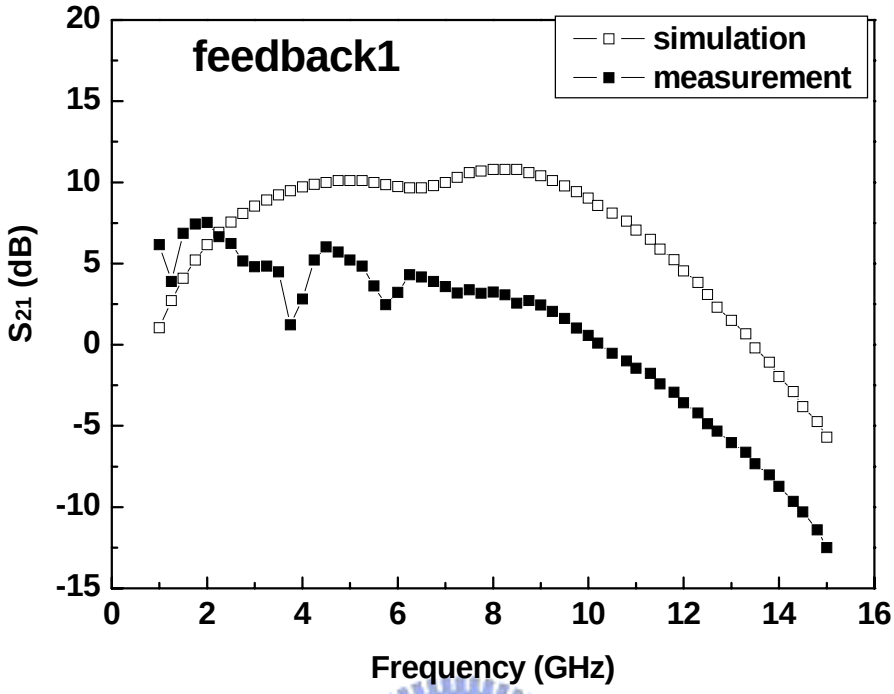
In feedback2, the forward gain (S_{21}) is less than simulation about 2dB due to the L1 without connecting bypass capacitors. The reason is the same with feedback1. And, the ripple in 3 to 6GHz is also the same, because their basic structure and layout are slightly different. The reverse isolation (S_{12}) is below -45 dB. The magnitude of S_{11} is

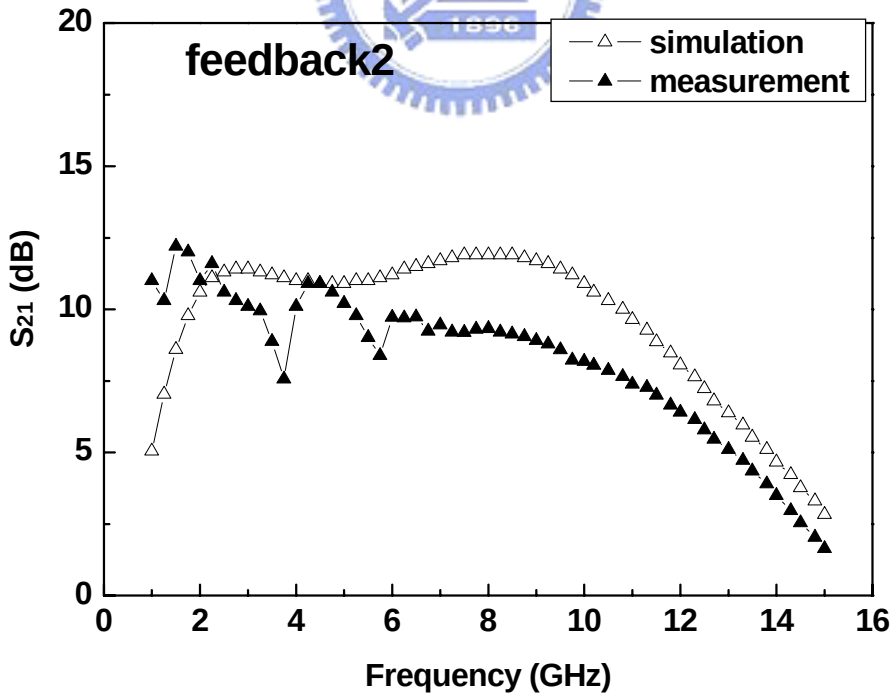
below -7.2dB and S_{22} is below -8.2dB in entire operation frequency band. The S_{12}, S_{11} and S_{22} are very close to the simulation result. The noise figure is very flat about 5.5dB and the minimum noise figure is 4.55dB at 9GHz. The IIP3 is -2dBm at 5.5GHz. The total power consumption is about 18mW with a power supply of 1.8 volts. And the die area including the pads is 0.77 mm^2.

From feedback1 and feedback2 structure, we can observe that the noise figure in feedback2 is better than feedback1 and the gain is also better. By the feedback2 structure, a low power, low noise amplifier can be achieved.

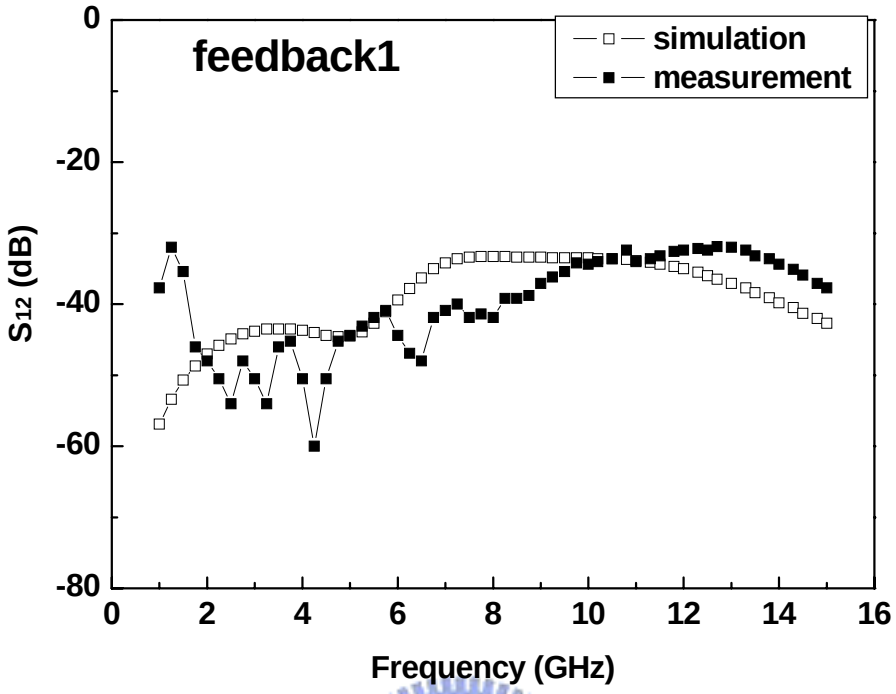
3.1~10.6 (GHz)	**Gain (dB)**	**NF (dB)**	**S_{11} (dB)**	**S_{22} (dB)**	**IIP3 (dBm)**	**Pdc (mW)**
Feedback1	5	8	<-7.5	<-10	2	18
Feedback2	9	5.5	<-7.2	<-8.2	-2	18

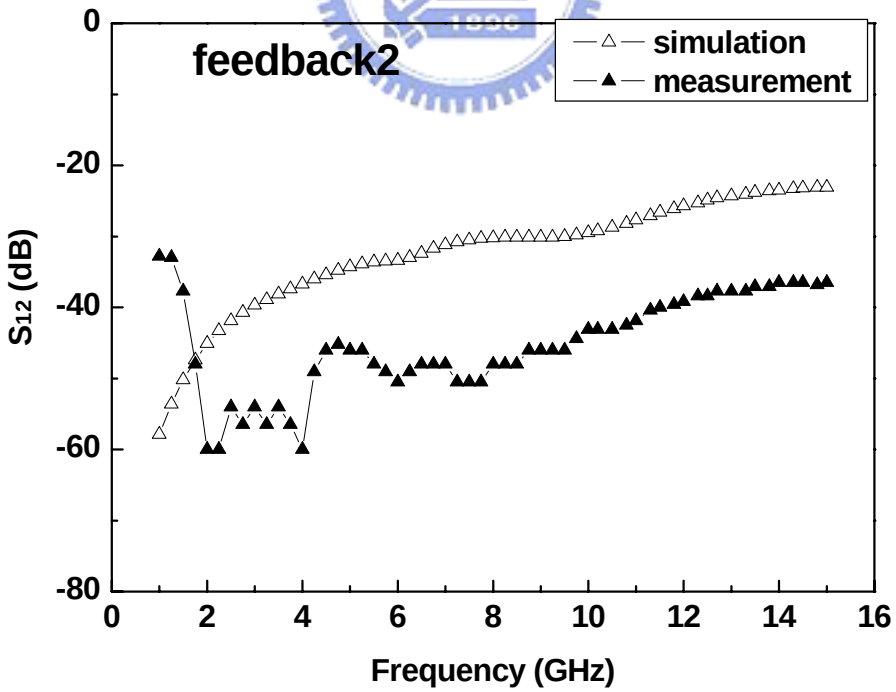
Table 3.1 Measurement results summary.


feedback1
simulation
measurement
S21 (dB)
Frequency (GHz)
20
15
10
5
0
-5
-10
-15
0
2
4
6
8
10
12
14
16

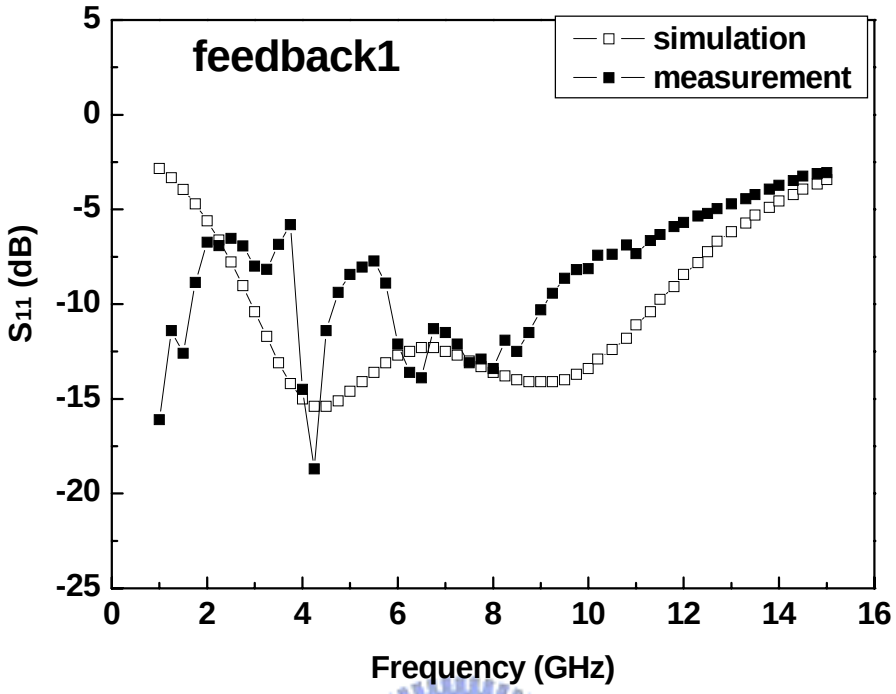

feedback2
simulation
measurement
S21 (dB)
Frequency (GHz)
20
15
10
5
0
0
2
4
6
8
10
12
14
16

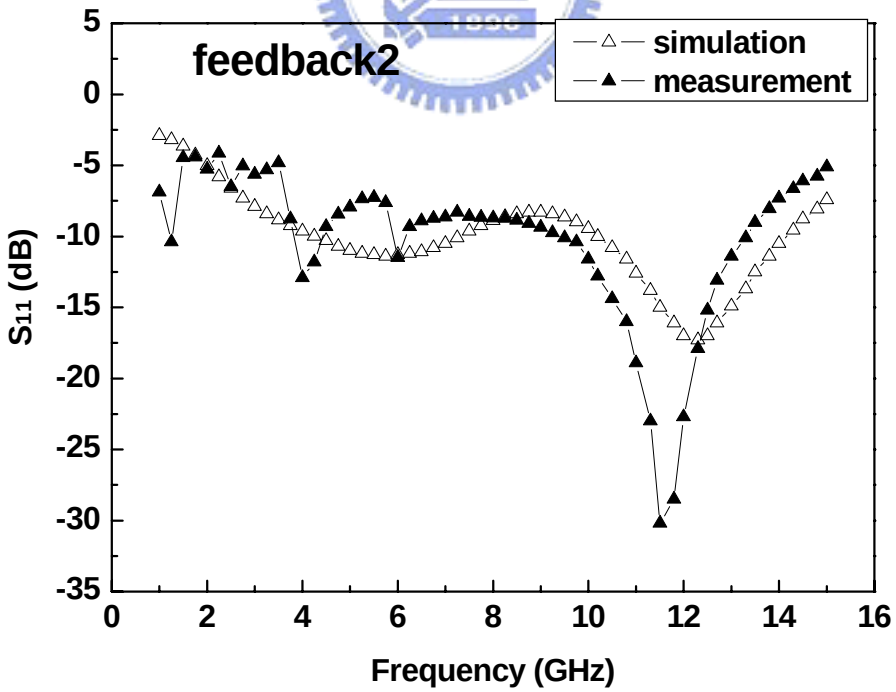
(a)


feedback1
simulation
measurement
S12 (dB)
0
-20
-40
-60
-80
0
2
4
6
8
10
12
14
16
Frequency (GHz)

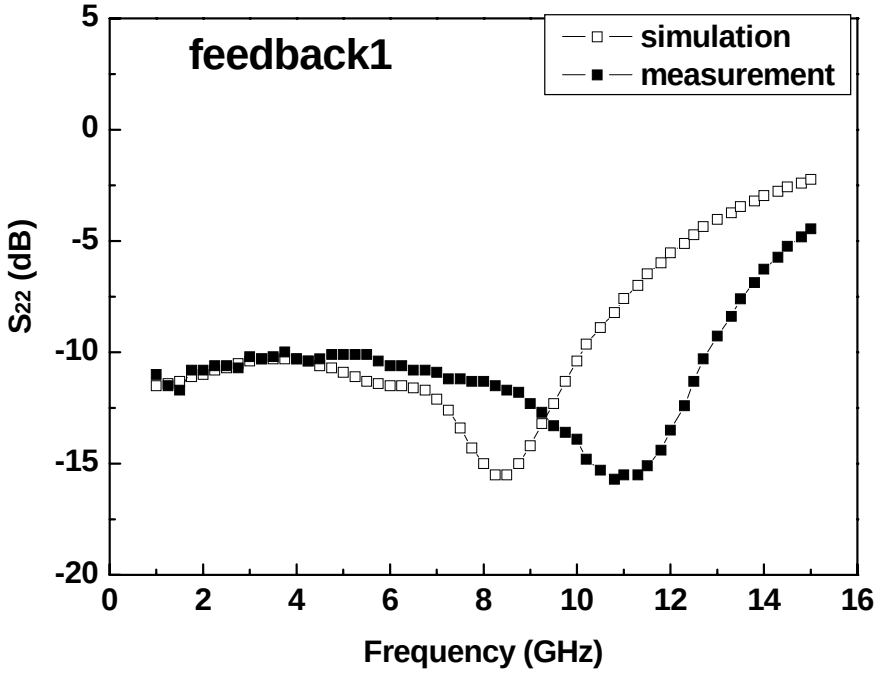

feedback2
simulation
measurement
S12 (dB)
0
-20
-40
-60
-80
0
2
4
6
8
10
12
14
16
Frequency (GHz)

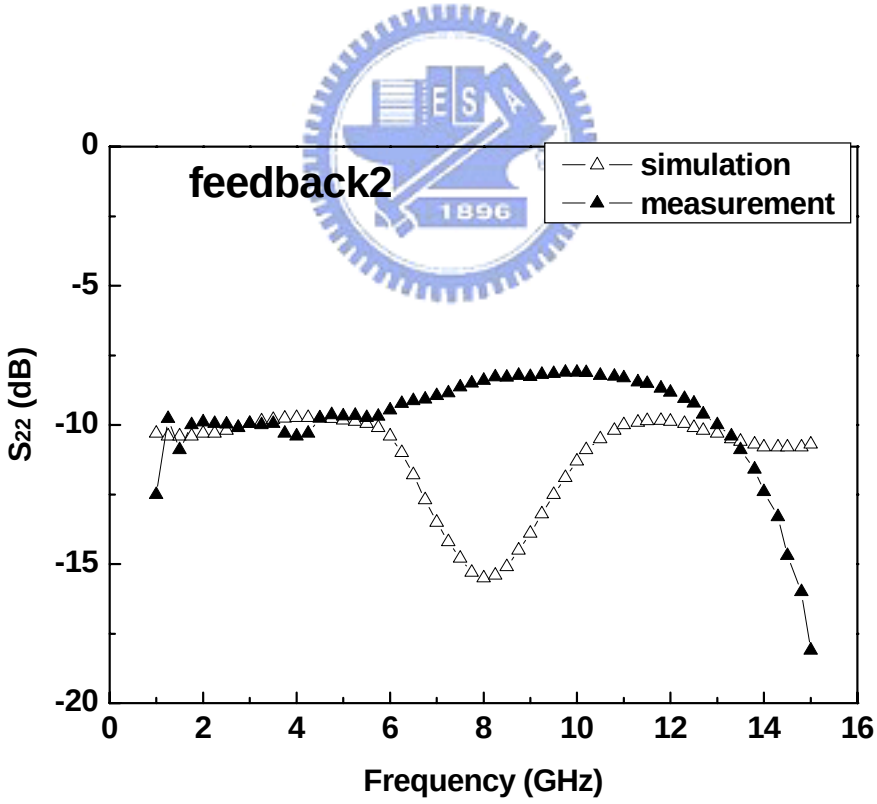
(b)


feedback1
simulation
measurement
S11 (dB)
Frequency (GHz)
5
0
-5
-10
-15
-20
-25
0
2
4
6
8
10
12
14
16


feedback2
simulation
measurement
S11 (dB)
Frequency (GHz)
5
0
-5
-10
-15
-20
-25
-30
-35
0
2
4
6
8
10
12
14
16

(c)





(d)

Fig. 3-8 S-parameters of feedback1 and feedback2 (a) S_{21}, (b) S_{12}, (c) S_{11}, (d) S_{22}.

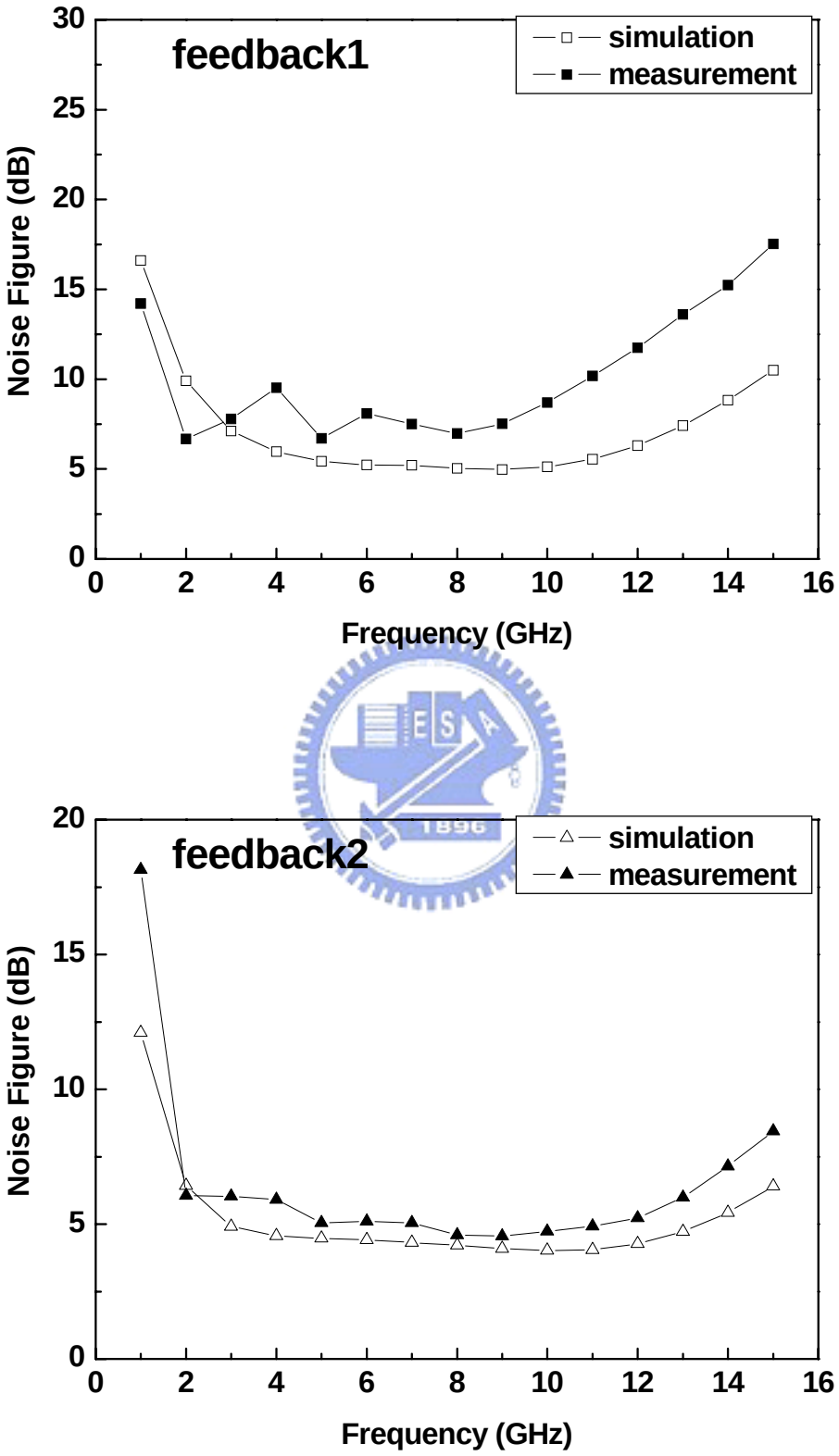


Fig. 3-9 Noise figure of feedback1 and feedback2.

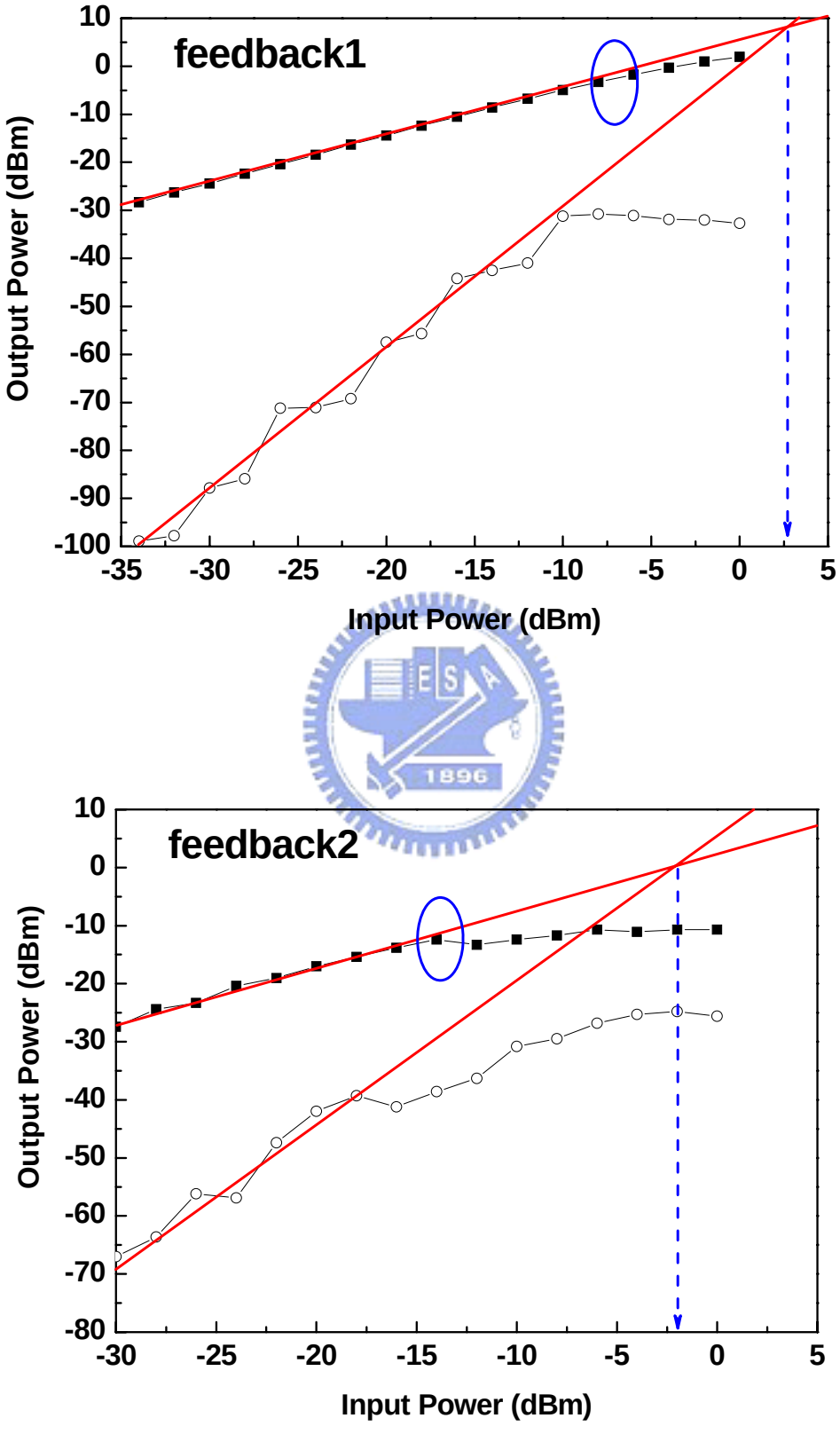
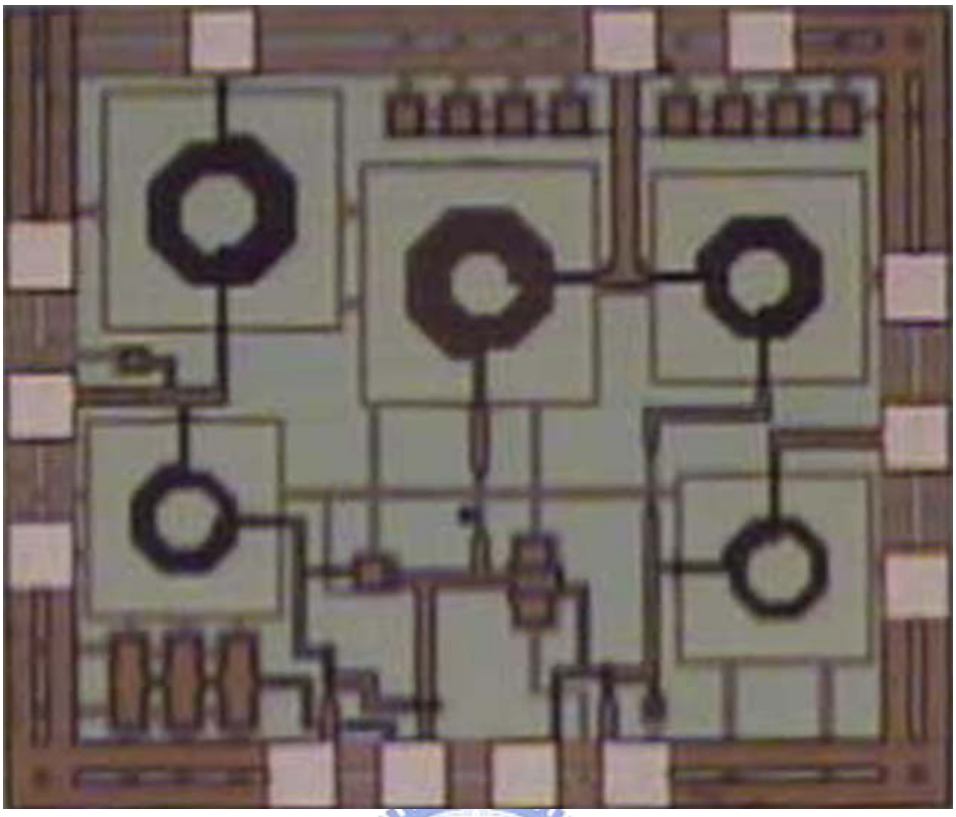
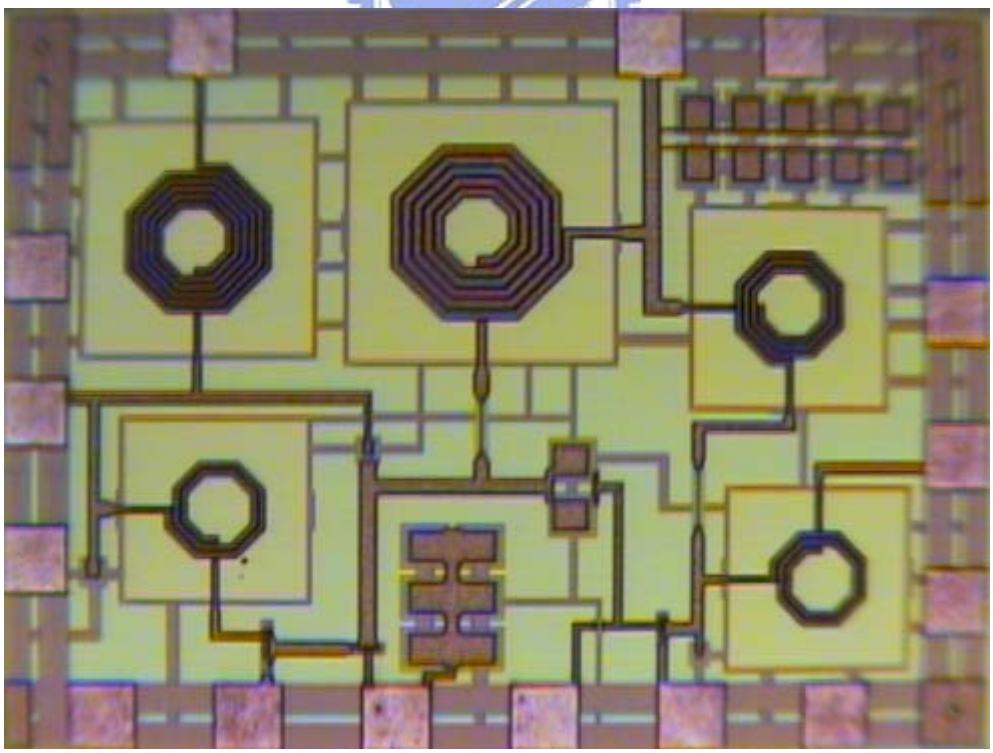


Fig. 3-10 Linearity of feedback1 and feedback2.



(a)



(b)

Fig. 3-11 Die photo (a) feedback1, (b) feedback2.

Chapter 4

Design of a low power UWB LNA with current-reused structure

4.1 Circuit topology

Fig. 4-1 shows the proposed current-reused high gain two stage amplifier topology. In Fig. 4-1, R_{d1}、L_{d1} and L_{d2} are the loads for each common-source amplifier, C_{g2} is the coupling capacitor, C_{bypass} is the bypass capacitor, and R_{bias} is the bias resistor. The proposed amplifier is the current-reused cascaded common-source amplifier with capacitive inter-stage coupling except the extra inductor L_{g2}. In Fig. 4-1, the value of L_{g2} is adjusted for the series resonance with the input capacitance of the second stage. Accordingly, the first stage is designed to resonate at the lower bound of the frequency band. The second stage, on the other hand, resonates at the higher bound of the frequency band.

To achieve the goal of power saving, the second stage is stacked on top of the first stage. A coupling capacitor and a bypass capacitor are required for this topology. The capacitor C_{g2} provides signal coupling between the two stages and the capacitor C_{bypass} functions as an ac ground at the source of transistor M2. The capacitance of capacitor C_{bypass} is chosen to be as large as possible to provide ideal ac ground in conventional narrow band designs as well.

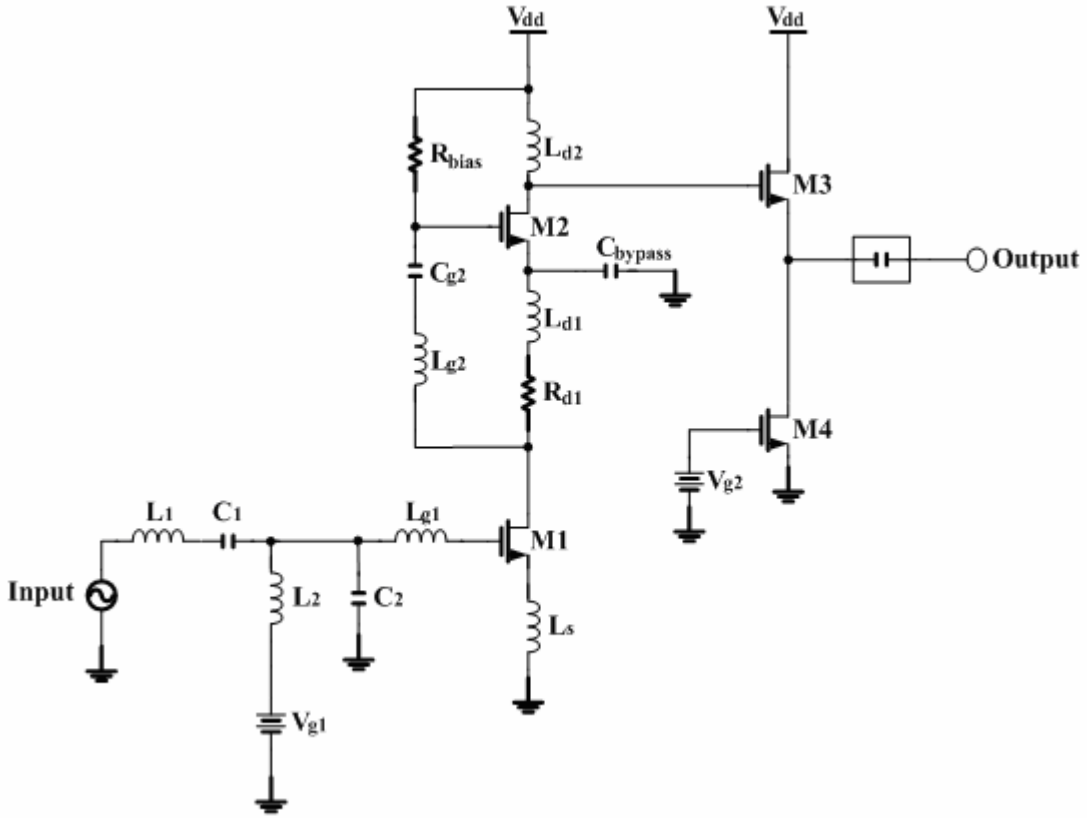


Fig. 4-1 Proposed UWB LNA schematic.

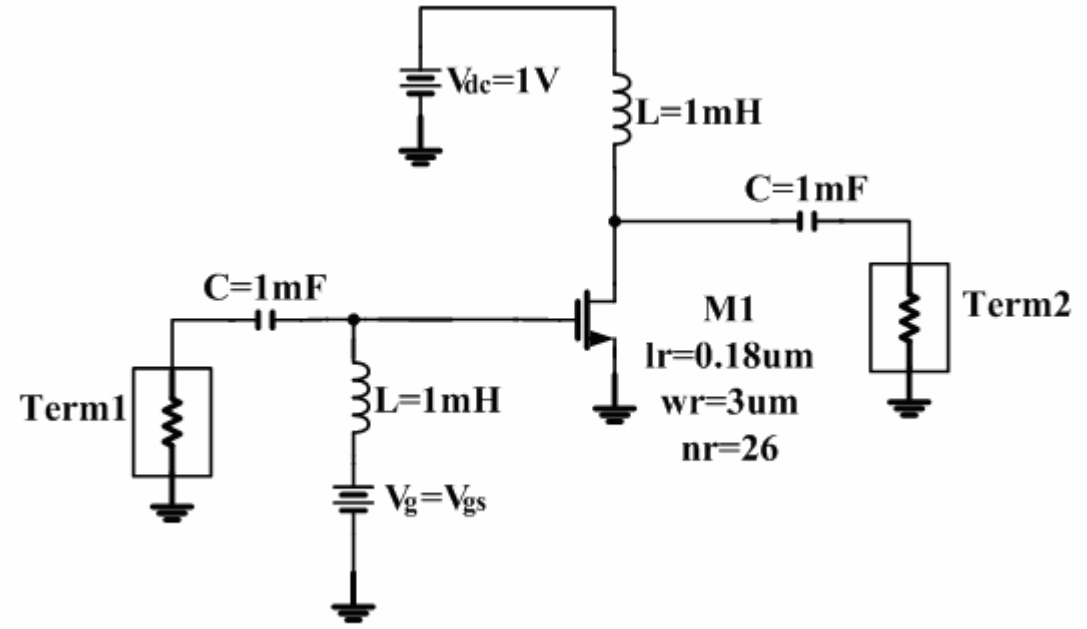
4.2 Design procedures

4.2.1 Transistor sizing and bias condition

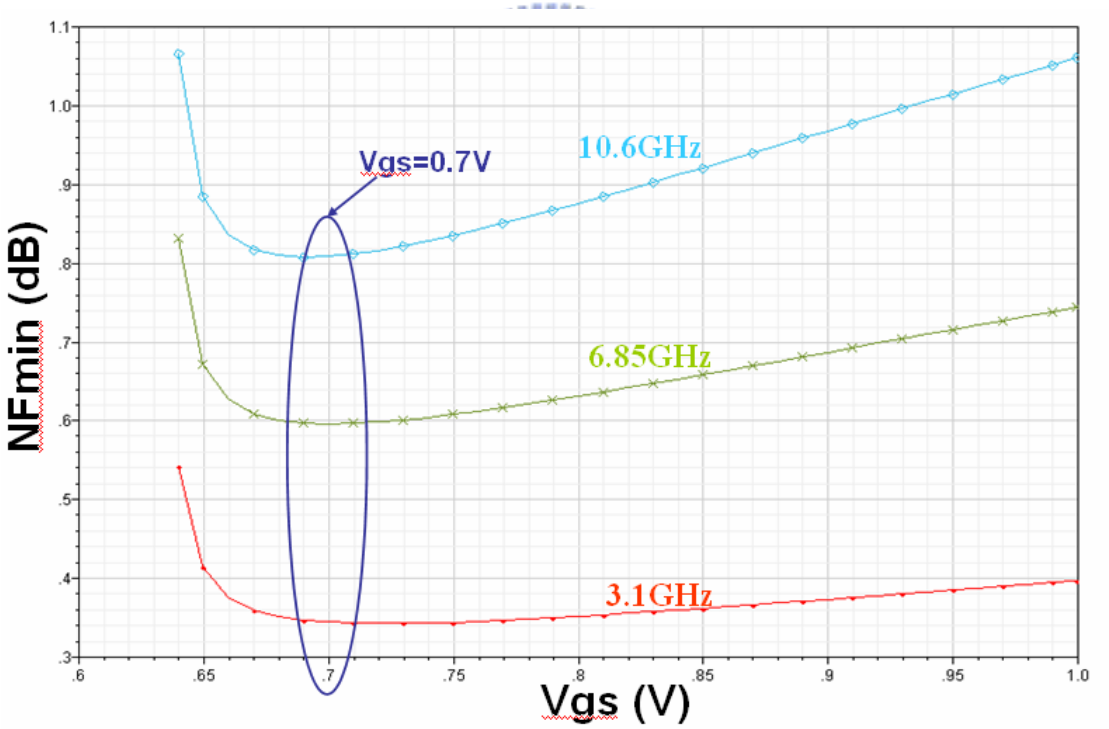
Since the size of transistor and bias condition determine the power dissipation, it is often recommended to decide them with a certain power budget. However, we should evaluate the size of the transistor versus bias condition carefully, because they are also related to the impedance seen by the input gate. Thus, the first choice is to determine the size and bias condition that satisfies both impedance and noise matching with limited bias current.

Fig. 4-2(a) shows a simulation circuit of MOS NFmin. In Fig. 4-2(a), the input transistor M1 (W/L = 78/0.18 um) is chose and is biased at 3.89mA. In Fig. 4-1, the size transistor M2 (W/L = 80/0.18 um) is decided. The bias current for M3 is selected to be 1.2mA and the width of M3 is 88 um. The transistor used to implement the current source is 24 um width. The total power consumption is only 9.1mW.

Fig. 4-2(b) shows the Vgs versus NFmin at 3.1GHz, 6.85GHz and 10.6GHz. From Fig. 4-2(b), we can observe that when Vgs = 0.7V, the transistor M1 has the minimum noise figure. Thus, the bias condition is decided to Vgs = 0.7V.



(a)



(b)

Fig. 4-2 (a) Simulation circuit of MOS NFmin, (b) Vgs v.s. NFmin at 3.1GHz、6.85GHz and 10.6GHz.

4.2.2 Input and output match

Input matching:

Fig. 4-3 shows the small signal model of the input impedance. The passive components L_1、C_1、L_2、C_2、L_{g1} and L_S are adopted for matching network at the input to resonate over the entire frequency band. The source inductor L_S is used to generate a real term for input impedance matching.

$$g_{m1}L_S / C_{gs1} = R_S = 50\Omega \tag{50}$$

The input impedance is derived as

$$Z_{in} = Z_1 + \frac{Z_2(Z_3 + \omega_T L_S)}{Z_2 + Z_3 + \omega_T L_S} \tag{51}$$

where

$$Z_1 = sL_1 + \frac{1}{sC_1} \tag{52}$$

$$Z_2 = sL_2 // \frac{1}{sC_2} \tag{53}$$

$$Z_3 = s(L_3 + L_S) + \frac{1}{sC_{gs1}} \tag{54}$$

$$\omega_T = \frac{g_{m1}}{C_{gs1}} \tag{55}$$

Output matching:

Fig. 4-4 shows the output matching network. The buffer must drive a 50Ω external load. The buffer is independently biased by means of a current source made up of two transistors in current mirror configuration.

$$\frac{1}{g_{m3}} = 50\Omega \tag{56}$$

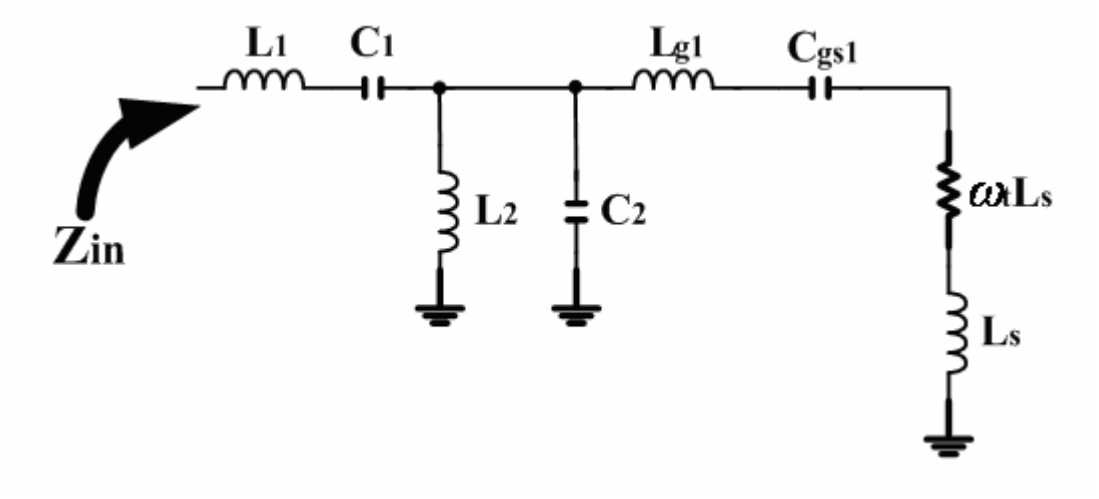


Fig. 4-3 Small signal model of the input impedance.

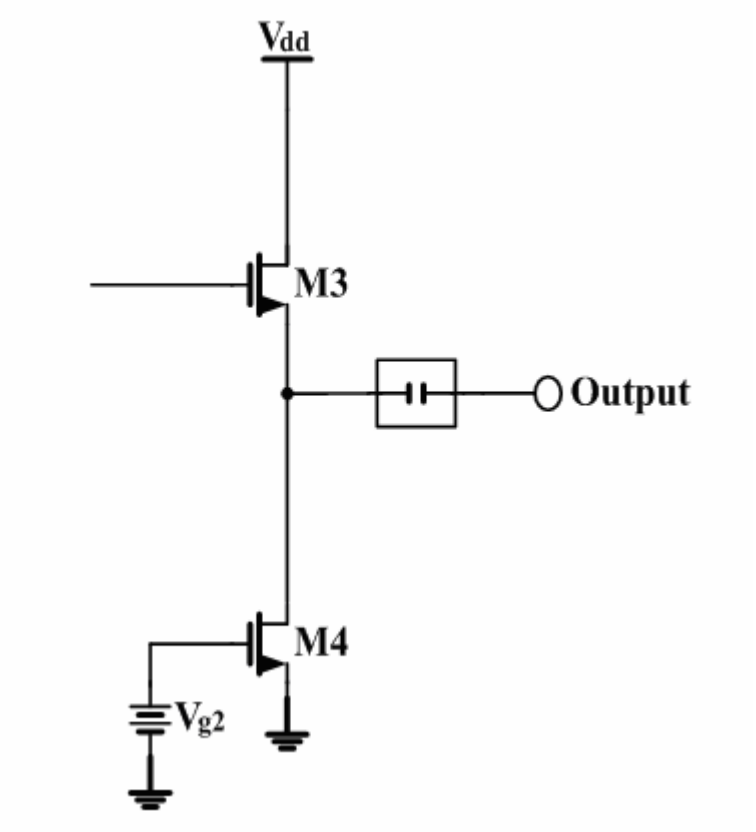


Fig. 4-4 Output matching network.

4.2.3 Gain analysis

Fig. 4-5(a) shows the current-reused two stage cascade amplifier with series inter-stage resonance. In Fig. 4-5(a), the value of L_{g2} is adjusted for the series resonance with the input capacitance of the second stage.

Fig. 4-5(b) shows the small signal equivalent circuit for the portion of the circuit enclosed by the dashed box in Fig. 4-5(a) in order to estimate the current gain from the drain of M1 to that of M2. In Fig. 4-5(b), Z_{d1} represents the load of M1 equal to R_{Lg2} is the parasitic series resistance of L_{g2}. The V_{gs2} and g_{m2} represent the gate-to-source voltage and the transconductance of M2.

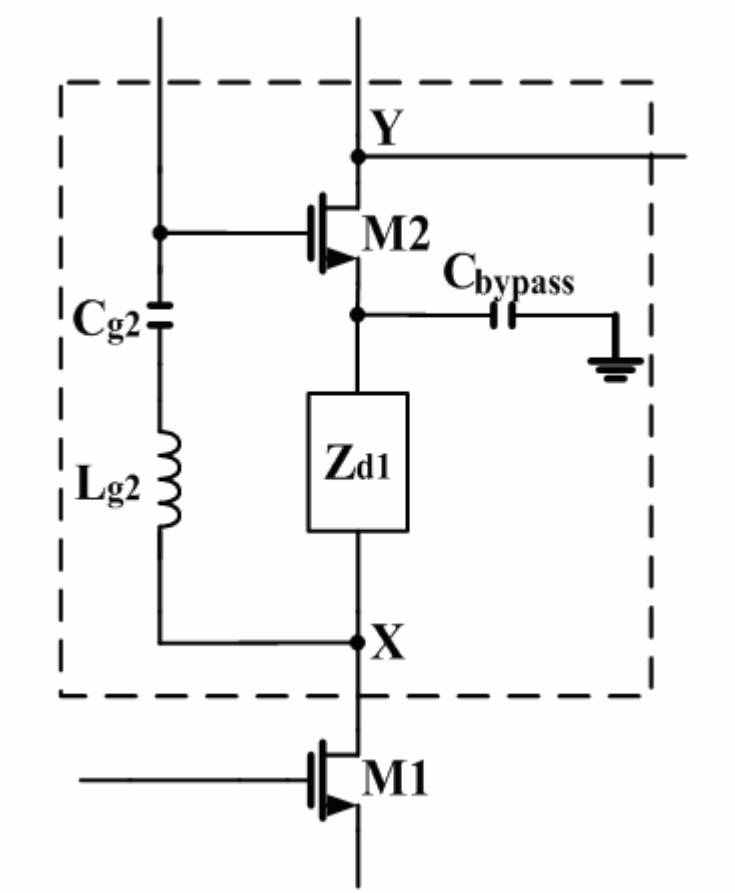
The current-amplifying characteristic of the series inter-stage resonated amplifier can be understood by analyzing the circuit shown in Fig. 4-5(b). From Fig. 4-5(b), the current gain id_2/id_1 can be expressed as

$$\frac{id_2}{id_1} = \frac{g_{m2}}{sC_{gs2}} \times \frac{Z_{d1}}{Z_{d1} + sL_{g2} + (1/sC_{g2} + 1/sC_{gs2}) + R_{Lg2}} \tag{57}$$

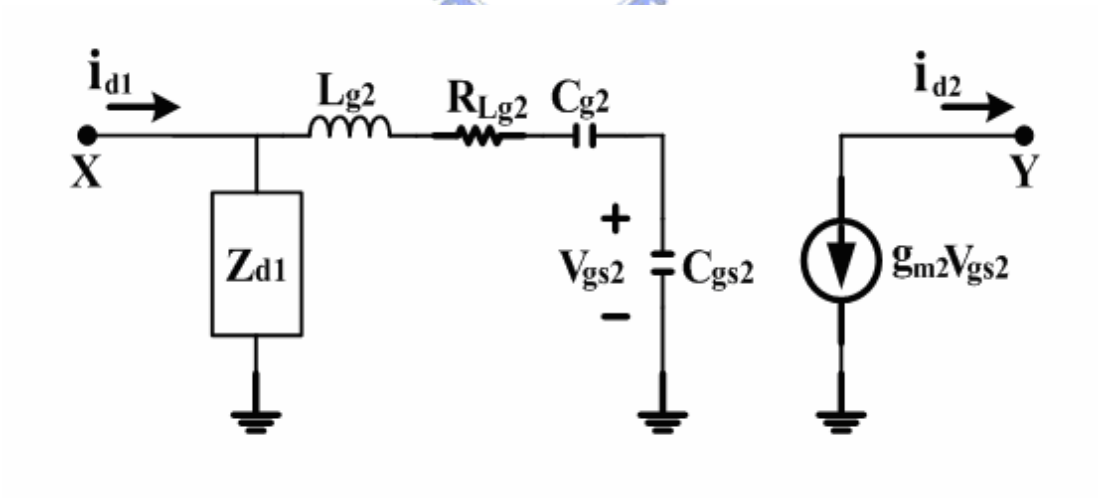
From equation (57), L_{g2} resonates with $1/sC_{g2} + 1/sC_{gs2}$ at high frequency band. If Z_{d1} provides sufficiently high impedance, $Z_{d1} >> R_{Lg2}$, then, $id_2/id_1 \cong g_{m2}/sC_{gs2}$, equation (1) can be approximated as

$$\frac{id_2}{id_1} \cong \frac{g_{m2}}{sC_{gs2}} \cong \frac{\omega_T}{\omega} \tag{58}$$

where ω_T is M2's cutoff frequency, ω is the frequency of operation.



(a)



(b)

Fig. 4-5 (a) Current-reused two stage cascade amplifier with series inter-stage resonance, (b) Small signal equivalent representation of the circuit from node X to Y.

4.2.4 Shunt peaking

The load inductor of the first stage, L_{d1}, is chosen to resonate at 3GHz with the R_{d1} at the drain node of the transistor M1. The load of inductor of the second stage is chosen to generate a resonance at 10 GHz. As shown in Fig. 4-6, a flat frequency response can be obtained by the combination of the resonance of the first and second stages ($\omega_{z1} \cong 3GHz$ and $\omega_{z2} \cong 10GHz$). To fit the frequency bands of UWB applications, the -3dB bandwidth is designed to cover 3.1 – 10.6 GHz.

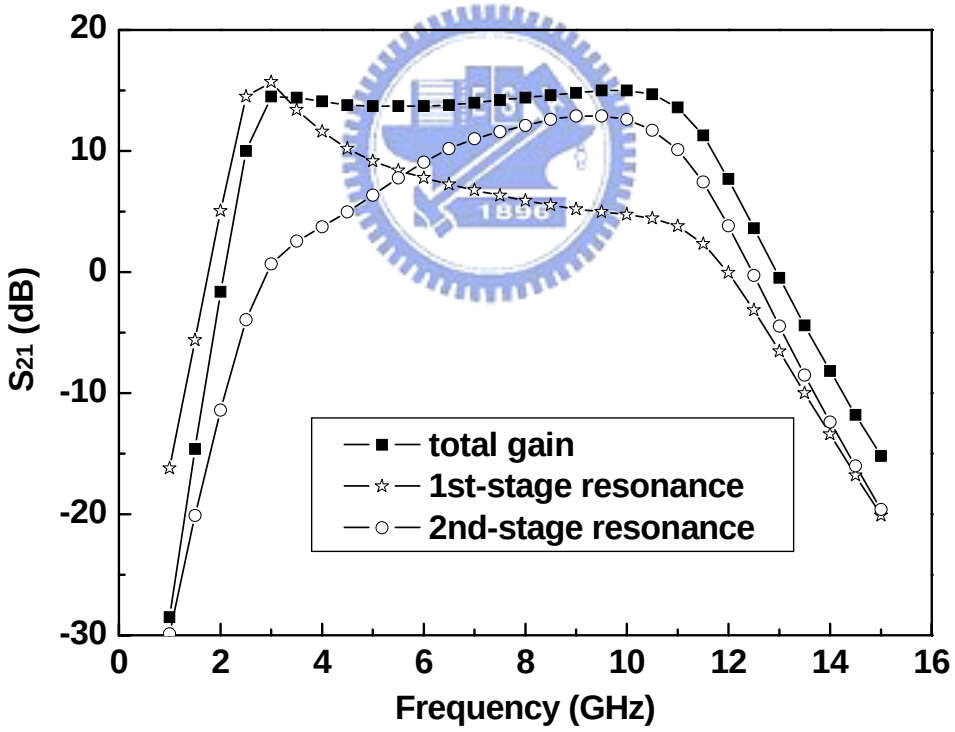


Fig. 4-6 1st-stage and 2nd-stage resonance contribute to gain.

4.3 Simulation and Measurement Result

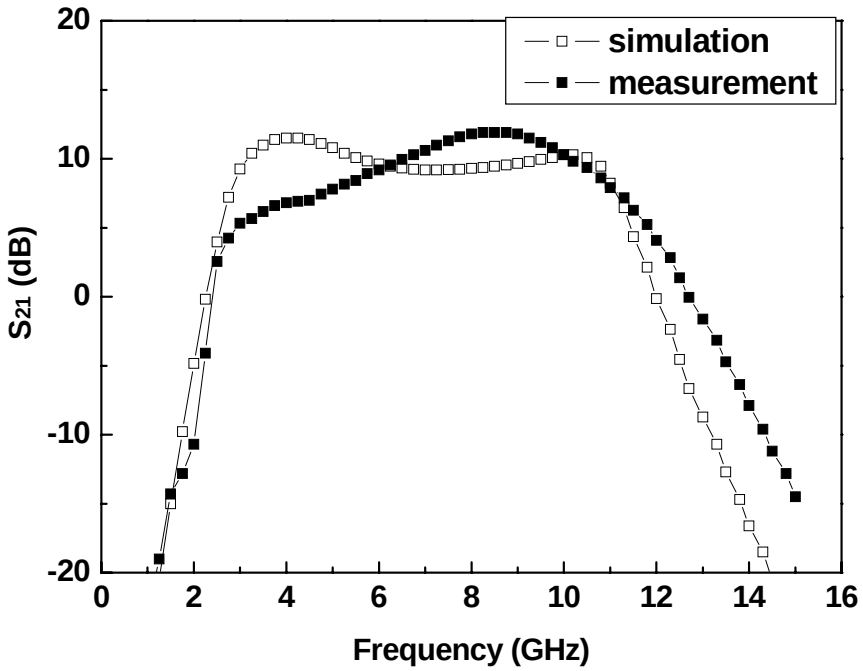
Fig. 4-7 shows the s-parameters of simulation and measurement. Fig. 4-8 shows the noise figure and Fig. 4-9 shows the linearity. Fig. 4-10 is the die photo.

In the current-reused structure, the forward gain (S_{21}) is less than simulation about 2dB due to the L2 without connecting bypass capacitors. When measured, the Vg1 dc probe without bypass capacitors may cause signal loss and have parasitical effects so that the gain is less than simulation. The reverse isolation (S_{12}) is below -50 dB. The magnitude of S_{11} is below -8.6dB and S_{22} is below -8dB in entire operation frequency band. The S_{12} , S_{11} and S_{22} are very close to the simulation result. The average noise figure is about 5.2dB and the minimum noise figure is 4.87dB at 8GHz. The IIP3 is -13dBm at 5.5GHz. The total power consumption is only 9.4mW with a power supply of 1.8 volts. And the die area including the pads is 0.98 mm^2.

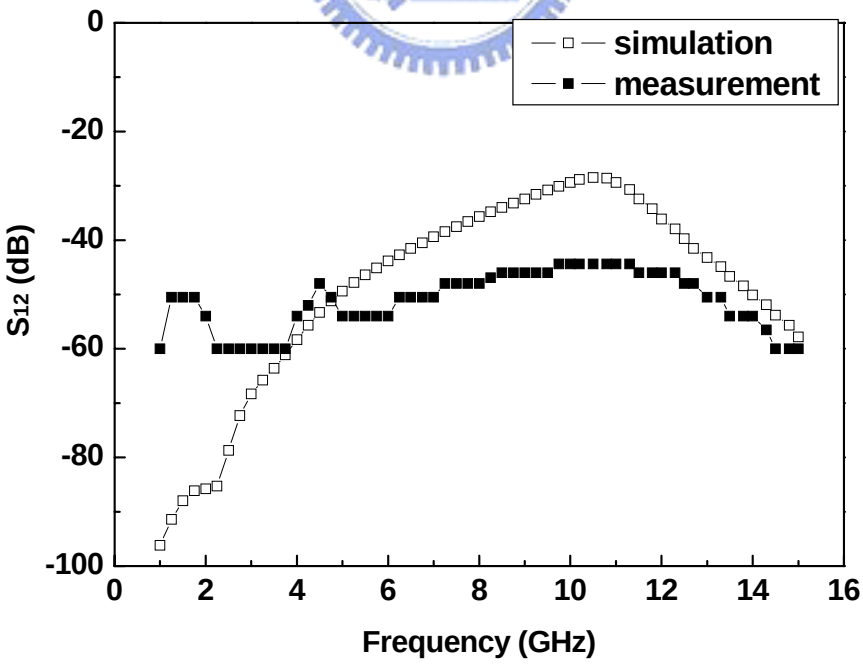
By current-reused method, a high gain, low power, low noise amplifier can be achieved. It only consumes 9.4mW.

3.1~10.6 (GHz)	**Gain (dB)**	**NF (dB)**	**S_{11} (dB)**	**S_{22} (dB)**	**IIP3 (dBm)**	**Pdc (mW)**
Current-reused	9	5.2	<-8.6	<-8	-13	9.4

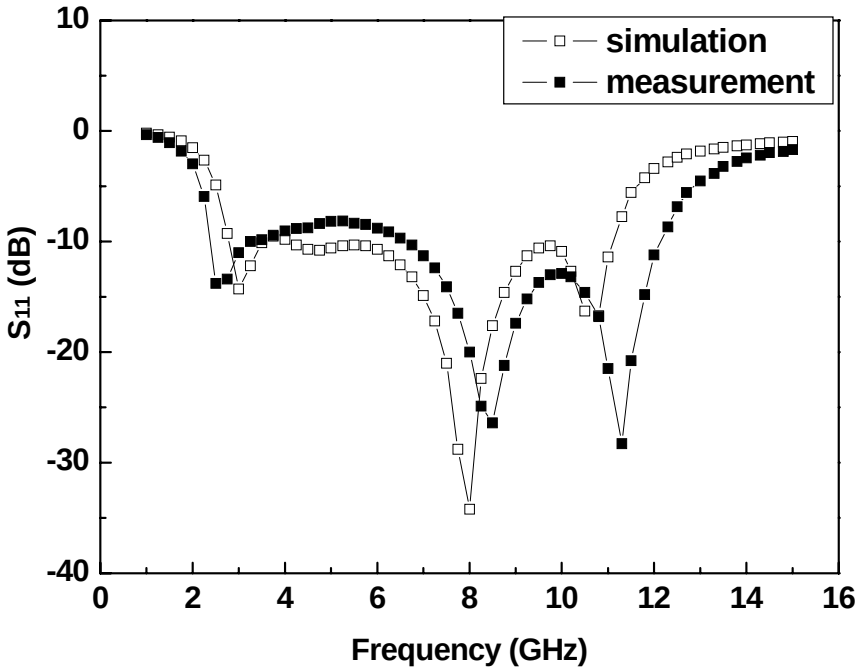
Table 4.1 Measurement results summary.


simulation
measurement
S21 (dB)
Frequency (GHz)
20
10
0
-10
-20
0
2
4
6
8
10
12
14
16

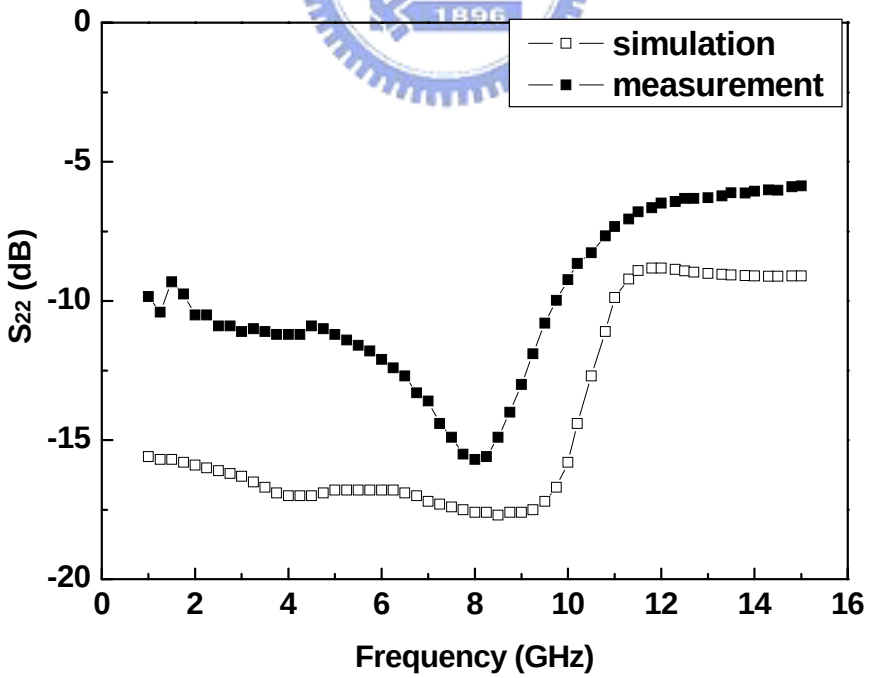
(a)


simulation
measurement
S12 (dB)
Frequency (GHz)
0
-20
-40
-60
-80
-100
0
2
4
6
8
10
12
14
16

(b)



(c)



(d)

Fig. 4-7 S-parameters (a) S_{21}, (b) S_{12}, (c) S_{11}, (d) S_{22}.

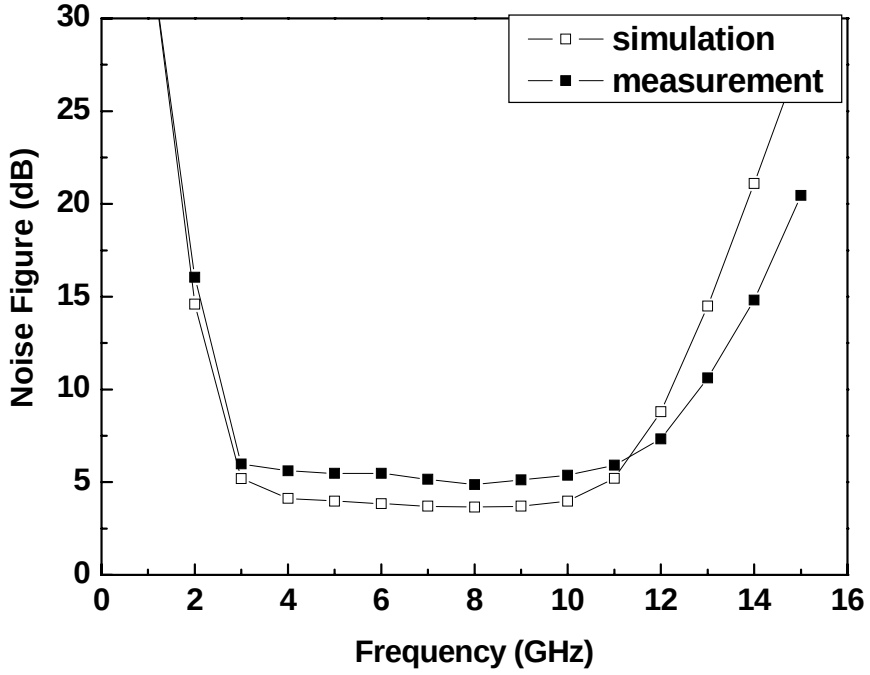


Fig. 4-8 Noise figure.

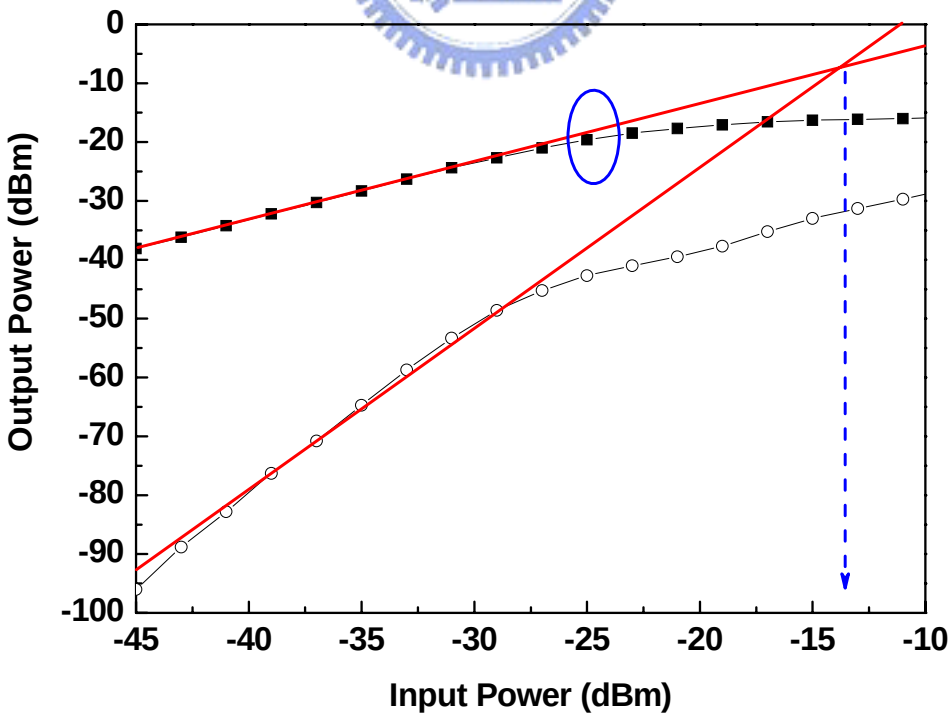


Fig. 4-9 Linearity.

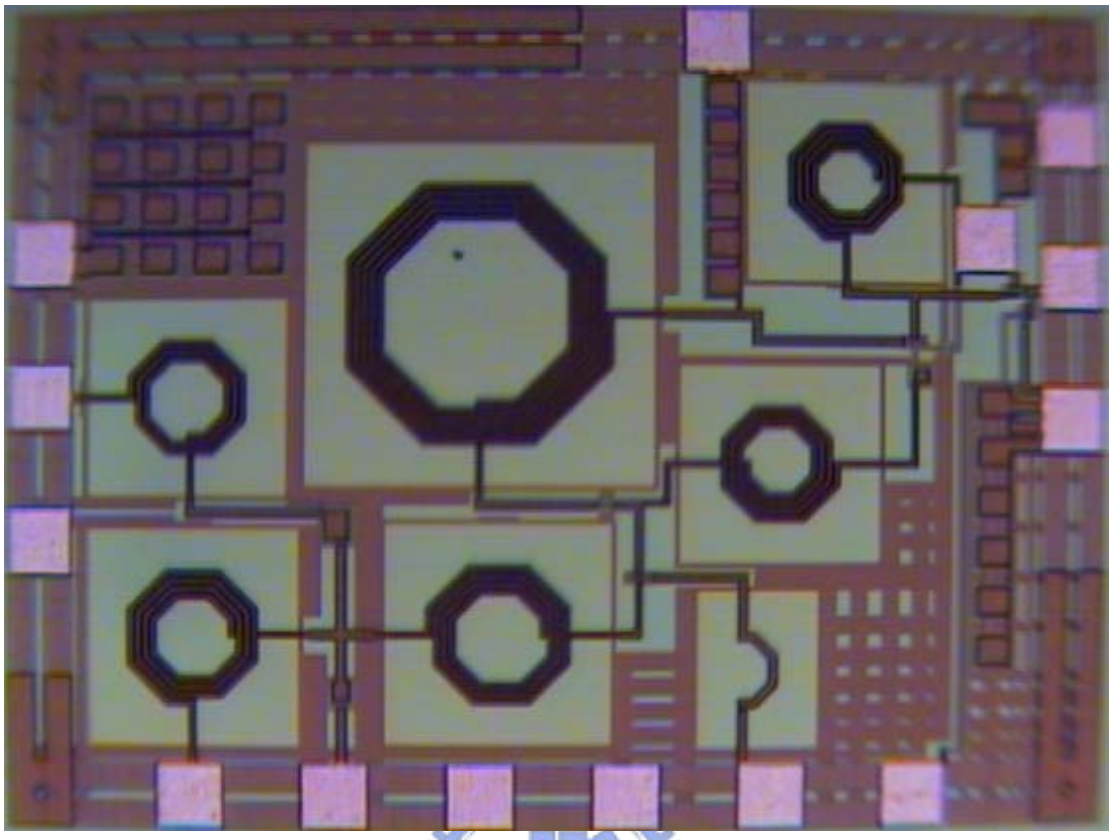


Fig. 4-10 Die photo.

Chapter 5

Summary

We design UWB LNA with R-C feedback structure in feedback1 and feedback2 and a low power current-reused structure. From measurement results, we can observe that feedback2 has better noise performance than feedback1 and current-reused structure is not only low power but also has good noise performance.

Table 5-1 is the comparison of broadband LNA performance. We can find out feedback2 has good noise performance and current-reused structure has very low power consumption and good noise figure.

Ref.	**B.W. (GHz)**	**Gain (dB) (max)**	**NF (dB) (average)**	**S11 (dB)**	**S22 (dB)**	**IIP3 (dBm)**	**Pdc (mW)**	**Tech. CMOS**	**year**
[9]	2.4~9.5	9 (9.3)	4~9 (6.5)	< -9	< -20	-6.7	18 *9	.18	2004
Feedback1	3.1~10.6	5 (6)	7.7~8.7 (8)	< -7.5	< -10	2	18	.18	2006
Feedback2	3.1~10.6	9 (10.5)	5.9~4.8 (5.5)	<-7.2	<-8.2	-2	18	.18	2006
Current-reused	3.1~10.6	9 (11.9)	5.6~5 (5.2)	< -8.6	< -8	-13	9.4 *7	.18	2006

Table 5.1 Comparison of broadband LNA performance * LNA core only

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（93年9月入學）

論文題目：

應用於超寬頻3.1-10.6GHz無線接收端之疊接回授架構與低功率電流再使用架構之低雜訊放大器之設計

(Design of a cascode feedback and a low power current-reused LNA for Ultra-wideband 3.1 to 10.6GHz Wireless Receivers)