應用於切換式直流至直流轉換器之
高性能互補金氧半控制器

HIGH PERFORMANCE CMOS CONTROLLERS FOR SWITCHING-MODE DC–DC CONVERTERS

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摘要

本論文針對切換式直流至直流轉換器提出數種創新之高性能控制器。為了要達到快速暫態反應、高效率、穩定運作以及固定的切換頻率等需求，新型控制器的分析與設計在本論文裡有完整的探討，並利用 CMOS 類比及數位混合式積體電路技術實現控制電路。

現存之自由運行控制電路具有架構簡單和反應極為快速之優點，然而切換頻率不固定，因此無法運用在對電磁干擾敏感的裝置中，同時相關的論文質與量皆相當缺乏，在理論分析方面仍有進一步探討的空間。在本論文中對於常見的兩種自由運行控制型式--漣漪控制和固定開啟時間控制進行理論研究，並針對缺點提出改進的電路架構。

在固定開啟時間控制方面，設計可依據輸入輸出電壓調整開啟時間的電路，因此切換頻率幾乎不隨輸入輸出電壓以及負載電流變動。在論文中探討自由運行控制的不穩定

現象，容易被回授信號上的雜訊干擾，因此提出創新的補償電路，可改善頻率響應以及雜訊免疫能力，利用內建積分器產生的斜坡信號用來觸發比較器，具有良好的雜訊免疫能力，可以達到穩定且快速的動作。控制電路利用 1 微米的互補式金氧半導體積體電路技術來實現，包含輸入輸出接腳的面積為 5.2 毫米平方，實驗結果顯示暫態反應十分快速，在輸入電壓 5 伏特，輸出電壓 2.476 伏特，負載電流 10 毫安培至 3 安培的情況下，效率可達 86 %至 93 %，負載穩壓度和線穩壓度分別為 0.032 %/A 和 0.034 %/V，均優於傳統電壓模式和電流模式的脈寬調變控制方式。

在漣漪控制方面，提出了嶄新的方法，利用相鎖迴路調整延遲，用以鎖定切換頻率，並針對 buck 和 boost 兩種功率級分別提出電壓模式與電流模式之漣漪控制器。穩態反應分析、輸出電壓電流轉換函數、切換頻率函數以及頻率響應函數在論文中有推導及分析，根據頻率響應設計出補償網路，分析漣漪控制之各種特性。同時，將切換頻率與延遲的關係線性化之後，可得到一個線性模型，根據此模型，我們可以設計迴路參數和分析相鎖迴路的穩定度。穩壓器電路經由 SPICE 模擬，buck 穩壓器在輸入 20 伏特輸出 1.5 伏特的情況下，穩態切換頻率鎖定 300 kHz，負載穩壓度和線穩壓度分別為 0.0046 %/A 和 0.028 %/V；boost 穩壓器在輸入 2.4 伏特輸出 3.3 伏特的情況下，穩態切換頻率鎖定 300 kHz，負載穩壓度和線穩壓度分別為 0.96 %/A 和 0.75 %/V，其他模擬結果也包含在本論文內。

傳統之類比式控制器存在調整困難，容易隨製程參數與外在環境漂移之缺點，數位式控制器則受限於電路數量較多與成本較高，針對此一問題，提出一種混合式控制電

路，利用比例式電流回授技術加速電源穩壓器之暫態反應，配合特別電路設計，簡化類比數位轉換與數位運算電路，具有架構簡單與高性能之優點，且容易調整控制參數。一般數位類比混合電路多利用電晶體等級的模擬分析系統的時域反應，在本論文中利用行為模型模擬系統的時域反應，可以大幅減少模擬的時間。控制電路利用 0.6 微米的互補式金氧半導體積體電路技術來實現，包含輸入輸出接腳的面積為 1.8 乘 1.8 毫米平方。當輸出電流由 2 安培增加至 20 安培時，輸出電壓最多降低 150 毫伏，並於 100 微秒內回到靜態容忍的界線內，大電流暫態反應符合嚴格的電源需求，並且與模擬的結果相符。

HIGH PERFORMANCE CMOS CONTROLLERS FOR SWITCHING-MODE DC–DC CONVERTERS

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Abstract

Several high performance controllers for switching-mode DC–DC converter are proposed. In order to achieve fast transient response, high efficiency, stable operation, and low switching noise, analysis and circuit design of the controllers are comprehensively investigated in this dissertation. Controllers are realized by CMOS analog and digital mixed-mode integrated circuits techniques.

Free-running control is the simplest among all control topologies of switching power supply. However, the switching frequency depends on the operating conditions and power filters. Thus, the use is limited in noise sensitive devices. Besides, only few related literatures provide analytical insights into this kind of control. Two common free-running control

topologies, ripple control and constant on-time control, are investigated. Circuits architectures are proposed to improve these controllers.

Switching frequency of the constant on-time regulator can be also stabilized by adjusting the on time according to input and output voltages. Unstable operation of free-running control due to noise on feedback signal is discussed. A novel compensation circuit is proposed to improve the frequency response and noise immunity of constant on-time control. This compensation circuit uses a built-in integrator to generate a ramp signal to trigger the comparator. Therefore, it is less susceptible to noise. Stable operation and fast response are obtained. The proposed control circuits are realized in a 1 μm CMOS technology with area of 5.2 μm^2 including the I/O pads. Experimental results showed fast response during load and line transients. Efficiency from 86 % to 93 % is obtained over a load range from 10 mA to 3 A under 5 V input voltage and 2.476 V output voltage. The load and line regulations are 0.032 %/A and 0.034 %/V that are superior to conventional current-mode and voltage-mode PWM control.

Switching frequency of the ripple control regulator can be synchronized by a novel method that uses a phase-locked loop to lock the switching signal with an input clock. Voltage-mode and current-mode control circuits are presented for the buck and boost power stages, respectively. Both steady-state response and small-signal model are discussed. Derived transfer functions are useful for designing the control loop and compensation network. By

taking linearization of the relationship of switching frequency and delay, a linear model is obtained for loop parameter design and PLL stability analysis. The proposed regulators were simulated in transistor level using SPICE. Input voltage and output voltage are 20 V and 1.5 V respectively for the buck regulator. During the steady state, the switching frequency was locked at 300 kHz. Load regulation is 0.0046 %/A and line regulation is 0.028 %/V. Input voltage and output voltage are 2.4 V and 3.3 V respectively for the boost regulator. During the steady state, the switching frequency was locked at 300 kHz. Load regulation is 0.96 %/A and line regulation is 0.75 %/V. More simulation results are also shown in this dissertation.

Analog controllers are sensitive to noise, process, temperature and component variations. Tuning these controllers is quite complicated as well. The uses of digital controllers are limited by their complex circuits and higher cost. In this thesis, the proportional current feedback technique is proposed to accelerate transient response of the voltage-mode switching regulators. With this technique, the complexity of analog-to-digital conversion circuits and digital computation circuits is greatly reduced. Performance can be easily tuned by adjusting the parameters. Instead of transistor-level simulation, a Matlab behavior model is build to simulate time-domain system response. Fast and accurate results can be obtained from this model. The proposed control circuits are realized in a 0.6 μm CMOS technology with area of $1.8\times1.8\ \mu m^2$ including the I/O pads. Experimental results showed the output voltage dropped 150 mV and recovered to static tolerance in 100 μs during a load transient from 2 A to 20 A.

The performance of the regulator met strict requirements and verified the simulation results.

誌謝

> Imagination reaches out repeatedly trying to achieve some higher level of understanding, until suddenly I find myself momentarily alone before one new corner of nature's pattern of beauty and true majesty revealed. That was my reward.
>
> — *Richard Feynman*

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左仲先

*2004*年*10*月


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Chapter 1

Introduction

1.1 Background

The rapid advances in computer, communications, and consumer electronics technology are having a major impact on our everyday lifestyle. This trend has been largely due to recent advances in emerging VLSI and ULSI semiconductor technology. While the brain of an electronic system is usually referred to the CPU, the heart of the system is the power supply. The CPU processes data and the power supply processes electric power. Due to various voltage and current requirements of different applications, design of power supply has become an important issue. Power conversion usually refers to the process of converting different forms of power supply such as AC–AC (frequency changers, cyclo-converters), AC–DC (rectifiers, off-line converters), DC–AC (inverters), or DC–DC conversion.

The role of DC–DC power conversion becomes more important in these years. Electronics products need to provide high-performance capabilities at low-power dissipation levels in compact packages at affordable prices. In order to achieve faster and more efficient circuit operations, signal swing inside integrated circuits should be as low as possible.

One dominant part of the power consumption in a CMOS circuit is the dynamic power consumption:

$$P_d \propto f \times V_{DD}^2 \tag{1.1}$$

where f is the operating frequency and V_{DD} is the supply voltage. It is clear from the above equation that reducing the supply voltage V_{DD} can reduce power consumption greatly due to their squaring relationship. In analog integrated circuits, voltage reduction also provides an effective mean to reduce the power consumption if the performance degradation is accepted or compensated.

The demands for higher functionality, smaller device size, and lower power dissipation have brought new technological issues. They can be resolved using more advanced semiconductor processes to implement the so-called system-on-a-chip (SOC). The processes have been improved from 0.35 μm to 0.25 μm, 0.18 μm, 0.13 μm, 90 nm and smaller for commercial products. By utilizing these advanced processes, more circuits can be implemented into one single chip and system size and complexity are greatly reduced. As the dimension of transistor continues to shrink, the gate oxide thickness of MOSFET also becomes thinner. To prevent electric breakdown, the maximum allowable supply voltage has dropped with each generation of semiconductor technology. For example, it is 3.3 V for 0.35 μm technology and 1.8 V for 0.18 μm technology. The operating voltage of an integrated circuit requires to scale down in order to maintain the reliability.

Another reason to perform DC voltage conversion is supply voltage boosting in portable equipments. Small-size and light-weight portable equipments such as MP3 players, cellular phones, pagers, and personal digital assistants (PDAs) provide convenient entertainment,

communication, and data access functions. The size and weight limitations restrict the number of battery cells. Thus, the input voltage provided by the batteries is usually lower than the chip supply voltage. Step-up voltage conversions are required in these systems.

As a result, it is a trend to drive high performance chips with an optimum operating voltage. Voltage regulators have to convert supply voltage provided by either standard system supply or batteries to various chip supply voltages. For example, in a personal computer (PC) system, there are several supply voltages required for different circuits such as 1.5 V for CPU and chipset, 2.5 V for memory module, 3.3 V and 5 V for standard logic chips.

Elementary switching-mode converters have been well known since the 1970's [2–7]. They can provide a wide range of output voltages; no matter lower or higher than the input voltage. Another feature, also the most important one, of a switching-mode converter is its dramatic improvement in weight and efficiency compared to dissipative regulators. The efficiency can often be higher than 80 % compared to 60 % (maximum) of a 5 V-to-3 V linear regulator. The efficiency of a linear regulator decreases as the difference between input and output voltage increases. Therefore, the switching-mode converter is a major choice for most power systems.

1.2 Trends and Challenges of Power Supply Design in Microelectronic Era

In this microelectronic era, high performance, long operating time, compact size and low cost are essential factors of a successful electronic product. For example, it is expected a third generation (3G) cellular phone can process extensive multimedia data with standby

time of a week and size of the palm [8–10]. These requirements challenge traditional power supply control techniques and converter design. In this section, trends of power supply design in microelectronic era are described.

1.2.1 High Efficiency

While transistor numbers inside a single chip continues to double every 18 months as Moore's Law predicts, energy density of batteries has increased little. Conversion efficiency is particularly important in battery-powered equipments. Low heat production also saves space for heat ventilation. Advanced power management techniques and converter circuits design will help to extend battery life and shrink device size.

1.2.2 Low Output Voltage and Low Noise

In portable and high performance systems, electronic systems are designed to operate at the optimal supply voltage [11, 12]. Low operating voltage of new generation integrated circuits has set tight tolerance of converter's output. Communication and audio circuits are also sensitive to noise interference. Low output ripple and low noise are essential. Fast transient response is required to prevent large output deviation during step load transient. In addition, fixed frequency operation of switching-mode converters is favorable, because it is easier to filter out switching noise.

1.2.3 Compact Size

Generally, switching-mode converters are composed of many discrete components that occupy large space. Since physical size minimization is a major design objective in portable devices, reductions of external component counts and size are trends of switching-mode

converter design [13, 14]. Significant energy is dissipated in the parasitic impedances of external interconnection and components [15]. Therefore, integrating external components decreases energy loss. Higher switching frequency can reduce the required sizes of filter inductor and capacitor and also improve efficiency [16]. Further physical size minimization can be made by integrating controller with microprocessor or other circuits [17, 18].

1.2.4 Fast Transient Response

Microprocessors today exhibit much heavier load and faster current slew rate. Advanced power management techniques are usually adopted. When the system is in sleep mode, some circuits are shut down and operating voltage is scaled down in order to minimize standby current. The most challenging issue comes from step load transients when the system transits from sleep mode to full loading mode. These two modes correspond to minimum and maximum loading conditions respectively. The regulator has to maintain output voltage within tight tolerance during this fast slew-rate transient. These power requirements have become new challenges [8, 19–23].

1.2.5 Wide Duty Ratio Range

Many portable devices are powered by multiple input sources such as AC adapter and batteries. Under these conditions, range of duty ratio variation is quite large. Unstable operations are observed when using traditional PWM control especially at very low duty ratio. Wide load range also causes duty ratio to change significantly.

1.2.6 Digital Control

Switching-mode converters are one of the few analog parts in today's electronic system. Due to cost and some practical issues, digital control of switching-mode converters has not been widely used. Digital control [24–37] provides versatile functions that enable more powerful features of switching-mode power supply. Sophisticated control schemes, converter status monitoring, and system integration can be easily implemented in the digital way. Fast design cycle of digital circuits is another attractive advantage. It is also less sensitive to noise, process, temperature and component variations. As the cost per transistor continuing drop with the advance of semiconductor process, above advantages have made digital control a more attractive choice for today's switching-mode power supply.

1.3 Motivation

A desirable controller regulates output voltage tightly in the presence of input voltage and load current variations. Voltage-mode PWM control scheme is commonly used in switching-mode power supplies. Design of this control scheme is simple and straightforward. The output voltage is controlled by directly changing the PWM duty ratio. Therefore, this control scheme is also called direct duty control. However, its application is limited because of slow response. Another popular control scheme is current-mode PWM control, which is also called current-programmed control and current-injected control, was introduced in 1978 [38–43]. This control scheme utilizes dual loops to control both output voltage and inductor current. It effectively eliminates the phase lag of the fil-

ter inductor and makes loop compensation easier. However, current sensing elements not only require additional circuitry but also reduce efficiency. Moreover, switching noise can easily corrupt the sensed current signal. Therefore, instability caused by noise is common in a current-mode system [44, 45]. Instability problem also occurs at very low duty ratio caused by high input voltages and low output voltages, which is encountered in notebook computer systems.

Variable-frequency control, also called free-running control [46, 47], includes constant on-time, constant off-time control [39, 48–51], and ripple control [26, 52–57]. Free-running control is the simplest among all control topologies of switching power supply. It performs tightest control over output voltage (voltage mode) or inductor current (current mode). Main advantages of the free-running control are fast transient response and wide duty cycle range. It also eliminates the need of external compensation parts, resulting in compact size and low cost. However, the switching frequency depends strongly on the operating conditions and power filters. Thus, the use is limited in noise sensitive devices. Besides, only few related literatures provide analytical insights into this kind of control. There exist many subjects to be investigated, such as loop gain transfer function and noise immunity.

Switching-mode converters have shown their advantage in conversion efficiency. Severe system requirements for future DC–DC converters demand new control schemes. Traditional methods will not yield acceptable results. Control circuit design techniques of switching-mode DC–DC converters are main concerns of this dissertation. Free-running control is a strong candidate for a high performance DC–DC converter. Switching fre-

quency stabilization, loop gain compensation, and noise immunizing techniques of free-running control are important topics worthy of further investigation. Digital PWM control is another topic in this dissertation. Digital control of switching-mode converters has become a popular topic in these years. The uses of digital controllers are limited by their complex circuits and higher cost. It is desirable to build a simple and integrable digital controller to provide a high performance operation.

1.4 Research Goals and Contribution

The goals of this research are to design and analyze high performance CMOS integrated circuits for switching-mode DC–DC converters. Fast response, tight regulation, high stability, fixed frequency, and compact size are key factors of a high performance converter. Several achievements have been worked out in this research and are highlighted below:

- Developed a simple and fast response digital PWM controller that utilizes proportional current feedback technique to speed up load transient responses. Novel A/D Converter design and control circuits reduce system complexity. It is particularly suitable for system integration.

- Derived loop gain of free-running control. Improved noise immunity and loop gain by utilizing a novel error amplifier. Low switching noise and low output ripple make proposed regulator suitable for low voltage applications.

- Developed improved ripple control regulators with fixed output frequency. This frequency synchronizing technique extends the application of ripple control regulators to noise-sensitive systems. Circuit design considerations and PLL analysis were

presented.

1.5 Thesis Organization

Chapter 2 introduces basic terms of the switching regulators. Some fundamental specifications and requirements of switching regulators are introduced such that limitations and trade-offs for designing can be understood easily.

Chapter 3 demonstrates a digital PWM controller for high current applications. Proportional current feedback technique is introduced to achieve fast load transient response and good load regulation.

Chapter 4 investigates unstable phenomenon of free-running control. A novel error amplifier is introduced to improve noise immunity and stability of the constant on-time controller. Complete control circuits are built on a single chip to verify proposed technique.

Chapter 5 presents improved ripple control regulators. Ripple control regulators are simple and effective. However, their switching frequency is varying with operating conditions. Techniques to obtain frequency-synchronized operations are proposed. Analysis and simulation results are shown in this chapter.

Chapter 6 concludes this dissertation.


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Chapter 2

Switching Regulator Basics

2.1 Voltage Regulators

2.1.1 Linear Regulators

Linear regulator is a simple, widely used DC–DC voltage regulator. Figure 2.1 illustrates a common linear power supply circuit. To provide the precise output voltage, the linear voltage regulator behaves as variable resistance between the input and the output. The linear regulators have many desirable characteristics such as low output ripple, good line and load regulation, fast transient response and low EMI. However, low efficiency limits their application. The linear device must drop the difference in voltage between the input and output. Therefore, the power dissipation is $(V_{in} - V_{out}) \times I_{out}$. The needs of heat sinks and good ventilation make them occupying more space.

2.1.2 Switching Regulators

The switching-mode converter, also called switching regulator, consists of switching devices repetitively on and off, together with energy storage components (capacitors and inductors) to generate an output voltage. Regulation is achieved through the adjustment of duty ratio based on fed-back sample signals of the output stage. In fixed-frequency

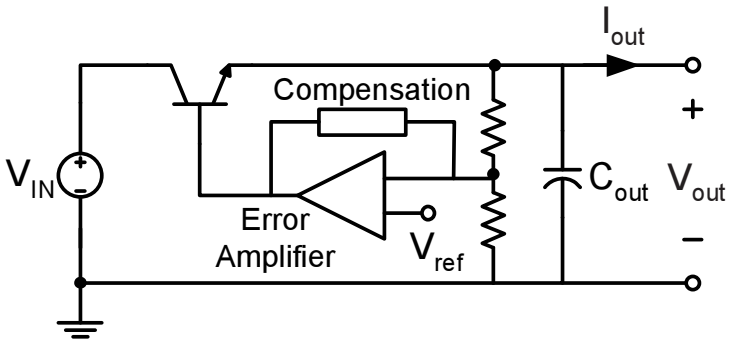


Figure 2.1: Linear regulator.

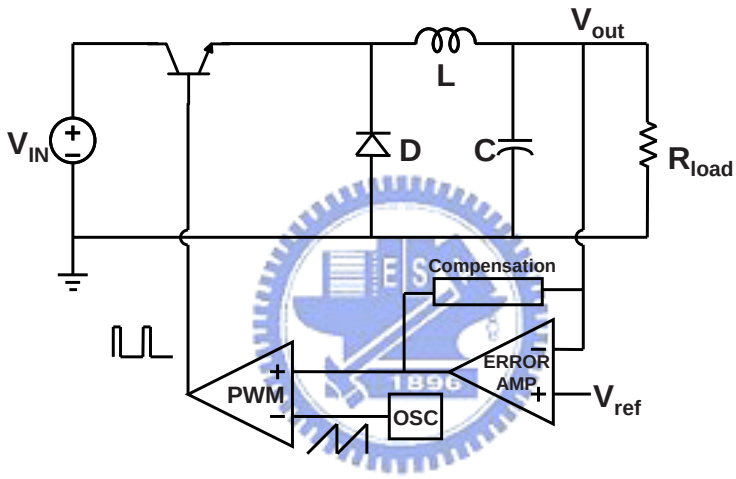


Figure 2.2: Switching regulator.

regulators, the switching signal is adjusted through modulation of the pulse width with a fixed-frequency clock signal — this is known as pulse-width modulation (PWM) control. A PWM buck regulator is shown in Fig. 2.2. In pulse-skipping modulated (PSM) regulators, the switch pulse width and frequency are kept constant, but the output switch is gated on or off by the feedback control; while in pulse-frequency modulated (PFM) regulators, the pulse width and frequency are varying with load.

Depending on the arrangement of switches and energy storage components, output voltages can be generated that are greater than or less than the input voltage. Compared

Table 2.1: Linear vs. switching regulators. (typical)

Specification	**Linear**	**Switching**
Line Regulation	0.02%–0.05%	0.05%–0.1%
Load Regulation	0.02%–0.1%	0.1%–1.0%
Output Ripple	0.5 mV–2 mV RMS	10 mV–100 mV_{P-P}
Efficiency	40%–55%	60%–95%
Power Density	0.5 W/cu. in.	2 W–10 W/cu. in.
Transient Recovery	50 μs	300 μs
EMI	None	High

with the linear regulator, PWM converter is superior in efficiency, size, and weight. With proper components, the power efficiency can be higher than 90%. This high efficiency feature makes it a popular choice in many applications. However, due to the switching operations, large ripples up to 100 mV can be observed at output. Large voltage and current swings also induce electromagnetic interference (EMI). These disadvantages make it less favorable for some applications such as communication and audio equipments. Additionally, control circuit for switching-mode power supply is usually more complex than linear regulator's. External components such as filter inductor and capacitor are also required. In addition, transient response is slower due to the limit of the switching frequency. Table 2.1 lists some typical values of linear and switching regulators [4, 58].

In summary, switching-mode regulator is suitable for medium to high power applications. In low power applications, linear regulator is a proper choice because of its low cost. The cross point of cost-versus-power curves of switching-mode regulator and linear regulator is around 3 to 10 watts [22]. The boundary continues to decrease with the advances of technology.

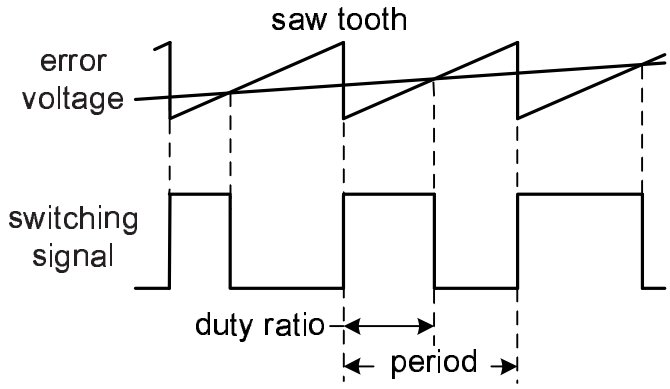


Figure 2.3: Switching signal of pulse-width modulation.

2.2 Modulation Techniques

2.2.1 Pulse-Width Modulation (PWM)

The pulse-width modulation, or PWM, control technique maintains a constant switching frequency and varies the duty ratio according to output voltage and load current. Switching signal of PWM is shown in Fig. 2.3. The error voltage is modulated by a sawtooth waveform generated by an oscillator. The switching frequency is determined by the oscillator and the pulse width is controlled by the voltage error. This technique provides high efficiency at medium to high load conditions. At light load condition, reverse inductor current and switching losses degrade efficiency. Because the switching frequency is fixed, the noise spectrum is relatively narrow, allowing simple low-pass filter techniques to greatly reduce the peak-to-peak voltage ripple. For this reason, PWM is popular with telecom applications where noise interference is of concern.

2.2.2 Pulse-Skipping Modulation (PSM)

One of the simplest modulation techniques used for controlling a DC–DC Converter is pulse-skipping modulation (PSM). As shown in Fig. 2.4, in a PSM system, the switching

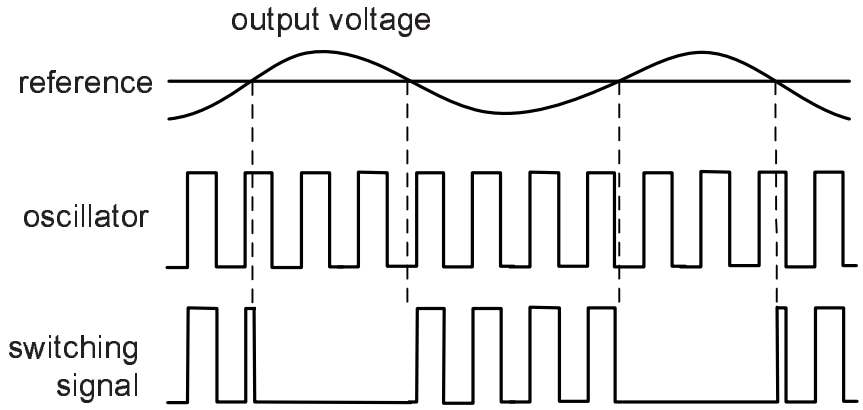
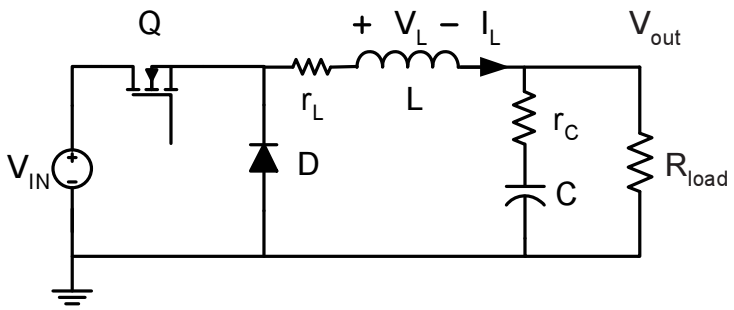


Figure 2.4: Switching signal of pulse-skipping modulation.

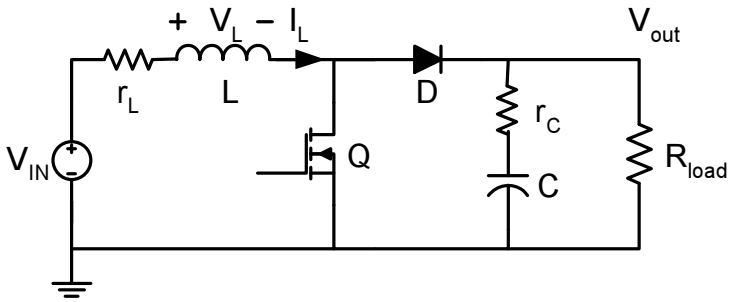
signal has a fixed pulse width, as well as period. As long as the converter output is below the reference voltage, the PSM pulses continue to run the converter switch. Once the converter output reaches or exceeds the target, the PSM pulse is skipped. This operation will result in decreasing pulse density as the converter output reaches its target, or as the output loading decreases. When the converter output falls below the target, or as the output loading increases, the PSM pulse density will increase. However, the inductor selection is complicated, the peak-to-peak voltage ripple can be quite high, and the noise/ripple spectrum will vary greatly with the load.

2.2.3 Pulse-Frequency Modulation (PFM)

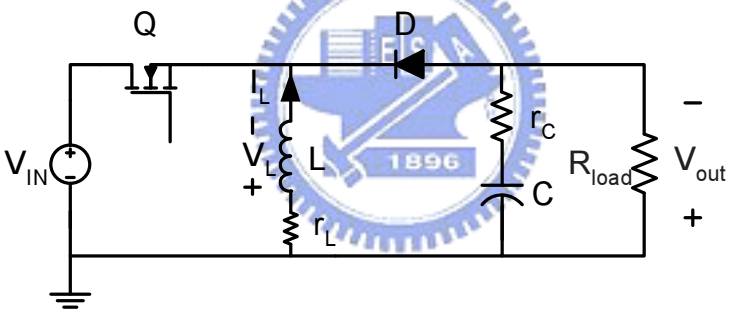
Pulse-frequency modulation is somewhat different from pulse-skipping modulation. The pulse width is variable and the pulse repetition rate is varied in accordance with load current and input/output voltages. As soon as the output voltage goes out of regulation, the switch turns on until the inductor current reaches the peak current limit [59] or until the predetermined time is up. The major drawback of PFM control is its varying switching frequency. Constant on-time control is a kind of PFM, which will be discussed



(a) Buck converter (down converter).



(b) Boost converter (up converter).



(c) Buck-boost converter (up-down converter).

Figure 2.5: Three basic converter topologies.

in Chap. 4. Switching frequency stabilizing technique of constant on-time control will be also presented in that chapter.

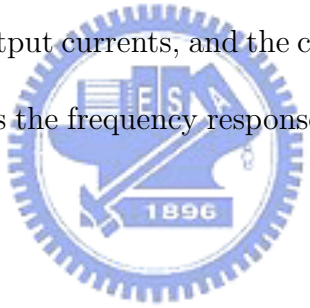
2.3 Basic Converter Topologies

In this section, three basic converter types are described: the buck, boost, and buck-boost. Figure 2.5 depicts these converters. They all consist of an inductor, a capacitor, and a diode. There is also an electronic switch that is driven on and off at a high frequency (e.g.

Table 2.2: Converter characteristics.

Topology	**Voltage Gain**	**Conversion Type**
Buck	$\frac{V_{out}}{V_{IN}} = D$	Step-down
Boost	$\frac{V_{out}}{V_{IN}} = \frac{1}{1-D}$	Step-up
Buck-boost	$\frac{V_{out}}{V_{IN}} = -\frac{D}{1-D}$	Step-up or step-down

5 kHz–1 MHz). These topologies differ in the ways that these elements are connected. Each topology has unique properties, including the steady-state voltage conversion ratios, the nature of the input and output currents, and the character of the output voltage ripple. Another important property is the frequency response of the duty-cycle-to-output-voltage transfer function.



The output filtering capacitor C in each circuit is used to smooth out the ripple component of the output voltage due to high-frequency switching. By adding a feedback circuit (not shown in the figures), the output voltage of the converter can be regulated. In each of the converter shown in Fig. 2.5, the energy-storage inductor L can be chosen to be so large that the current in it is substantially smoothed. The buck converter, shown in Fig. 2.5(a), is characterized by a smoothed output current i_{out} but a pulsating input current i_{in}. The boost converter, shown in Fig. 2.5(b), is characterized by a smoothed input current but a pulsating output current. The buck-boost converter shown in Fig 2.5(c) has both pulsating input and output currents. Table 2.2 lists characteristics of these converters.

2.4 Performance Specifications

While designing an electronic system, output voltage and current rating are usually specified to the power supply. However, many other parameters are required to evaluate the performance of a power supply [2, 60]. In this section, some terms and definitions are described such that it will be easier to design or to evaluate a switching regulator.

2.4.1 Efficiency

The efficiency of a power supply is defined as the ratio of the output power and input power and is calculated as follows:

$$\text{Efficiency} = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} \times 100\% \tag{2.1}$$

Efficiency can be regarded as the ratio of delivered power P_{out} to total consumed power P_{in}. Total power is the sum of the followings: (1) quiescent power: the quiescent current is the current flows into the chip. It is a goal of the chip designer to minimize this kind of power dissipation; (2) parasitic power: parasitic resistance in the output current path also dissipates power; (3) dynamic power: during the switching period, power is dissipated by charging/discharging gate capacitance of switching MOSFETs. It is a function of gate capacitance C_g, switching frequency f_{SW}, and driving voltage V_{dr}. The relationship is shown below:

$$P_d = C_g \times V_{dr}^2 \times f_{SW} \tag{2.2}$$

; (4)output power: power delivered to the load. An efficient power supply should transfer as much input power to the output as possible. An inefficient regulator has two major disadvantages. First, energy is wasted. This is particularly important in a battery-

powered system. Second, large heat sinks and good ventilation are required, which add to the size and weight of the regulator.

2.4.2 Load Regulation

Output voltage regulation is a regulator's ability to maintain its output voltage within the specified tolerance under various load disturbances. A measure of this ability is output impedance of the regulator. There is usually a feedback path in a regulator to compensate for such changes and keep the output close to the nominal value. Load regulation is the percentage change in the steady state output voltage when the load current changes from its minimum value to the fully rated current. Load regulation is defined as:

$$\text{Load Regulation} = \frac{\Delta V_{out}/V_{nom}}{\Delta I_{load}} \times 100\% \tag{2.3}$$

where V_{nom} is the nominal output voltage.

2.4.3 Line Regulation

Similar to the definition in the load regulation sub-section, line regulation is a measure of the effect of changes in the input voltage on the output voltage. The small signal line-to-output transfer function is called audio susceptibility. In some systems, input voltage may change as largely as 10 V. For example, in a notebook computer, the input voltage is 19 V provided by an AC adapter while it is around 8 V when battery power is used. There is a variety of methods used to specify line regulation; however, a common definition is:

$$\text{Line Regulation} = \frac{\Delta V_{out}/V_{nom}}{\Delta V_{IN}} \times 100\% \tag{2.4}$$

The specification of line regulation is usually given by %/V between maximum and minimum input voltages and at a specified loading condition.

2.4.4 Transient Response

The transient response is a switching regulator's response to sudden changes in load current. It is measured by the magnitude of output voltage drop and the time of recovery. The transient response relates to the bandwidth of switching regulator, output capacitor, equivalent series resistance (ESR) of output capacitor and the load current.

A wide bandwidth regulator exhibits fast transient response. Limited by the bandwidth of switching frequency, switching-mode regulators are slower than linear regulators. Loop crossover frequency is typically limited to 1/5 to 1/10 of the switching frequency. Therefore, a large output filter is required to compensate slow transient response. In order to reduce overshoot and ringing in output voltage, an adequate phase margin must be obtained. Control scheme also affects loop bandwidth, for example, the current-mode control provides faster response than the voltage mode.

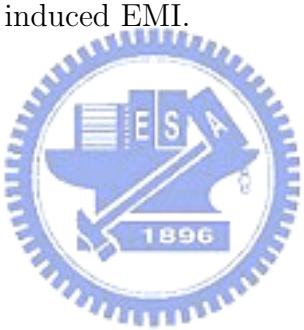
If the output is suddenly switched from light load to full load, the shortage of the output current will cause a fall in output voltage. On the other hand, if the load is switched off, excess output current will cause a rise in the output voltage. The transient response is normally specified together with a recovery time and is stated as:

$$\frac{V_{dev}}{V_{nom}} \times 100\% \tag{2.5}$$

where V_{dev} is the maximum deviation from nominal output voltage V_{nom} at a full load transient.

2.4.5 Electromagnetic Interference (EMI)

Electromagnetic interference (EMI) is a potential problem for the circuit designer. The switching process of a regulator produces voltage spikes resulting in EMI that interferes with proper operations of sensitive electronic equipments. The EMI spectrum begins at the switching frequency and often extends over 100 MHz that falls within the frequency bands commonly allocated for communications, such as low-frequency (LF), high-frequency (HF), and very-high frequency (VHF) bands. One obvious advantage of a fixed-frequency regulator is that the switching frequency and its harmonics are fixed which makes it easier to filter induced EMI.

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Chapter 3

A Compact Digital Buck Controller with Proportional Current Feedback

3.1 Introduction

While most of the switching-mode controllers today are implemented by analog circuits, digital controllers begin to play important roles in this area. Although in its initial stage, digital switching regulator control provides obvious advantages over traditional analog control such as complex control algorithm and more interaction with the microprocessor. In this chapter, a digital voltage-mode PWM DC–DC converter with error-integration algorithm is presented. This architecture requires only a compact nonlinear A/D converter and few digital circuits. Components usually used by normal digital controllers such as microprocessor, DSP, and linear A/D converter are greatly reduced. Therefore, the compactness of the controller makes it feasible to integrate with other digital circuits. However, this integrator-based controller is inherently slow during load transients and is not able to meet regulation specifications of contemporary microprocessors. To improve the performance, a novel architecture using proportional current feedback is used. Although inductor current is sampled as a feedback signal, this controller is essentially a

voltage-mode controller. In addition, the simple fashion of circuit realization is kept in this architecture. In the following section, general digital control for switching-Mode DC–DC Converter is firstly reviewed. In Sec. 3.3, the proposed control algorithm of proportional current feedback is presented. In Sec. 3.4, circuit implementation of the controller is discussed. A time domain system model that is used to simulate circuit behavior is presented in Sec. 3.5. The control chip is fabricated in a 0.6 μm digital CMOS process. In Sec. 3.6, experiment results are presented. Fast transient response proves effectiveness of the proportional current feedback technique.

3.2 Digital Control for Switching-Mode DC–DC Converter

An analog PWM controller consists of analog circuit components such as error amplifier, comparator, and saw tooth generator. Additional components are required to compensate the two poles in the control loop caused by the buck filter. The saw tooth generator runs at a fixed frequency. Its output is compared with the error amplifier's output. A PWM signal is generated by the comparator. Its duty ratio depends on the error amplifier's output and its frequency is the same as the saw tooth generator. Analog controllers are sensitive to noise, process, temperature and component variations. The switching action itself is the main source of noise that pollutes the feedback signal. Tuning these controllers is quite complicated as well.

While most of the controllers are designed using analog circuits, digital controllers [24–37] have become more popular nowadays. Benefiting from their programmability, digital controllers are smarter and more versatile than analog controllers are. Moreover,

they are less sensitive to noise and environment variations [27]. They are not limited in functions and complex computations can be performed. While most circuits in an electronic system are digital, it is much easier for a digital controller to integrate and communicate with other circuits. Further, design cycle of digital circuits is much faster than analog ones. Digital controllers are usually implemented with microprocessors or DSPs [24, 25]. In addition, A/D converters are required to convert controlled quantity, typically output voltage and inductor current. As the regulation tolerances are getting tighter, digital controllers may suffer from excessive cost and silicon area due to high resolution. Their costs are higher as compared with analog counterparts. Efforts have been made to reduce hardware complexity by exploiting a simplified A/D structure [33–36]. This kind of A/D converter will be introduced in this chapter.

3.3 Proportional Current Feedback

3.3.1 Voltage-Mode and Current-Mode Control

The voltage-mode control is a common approach used for switching regulator design [2]. The output voltage is controlled by comparing the output voltage with a reference voltage and using the resulting error to adjust the duty ratio D. Figure 3.1(a) shows a voltage-mode PWM DC–DC converter with a synchronous buck filter. There is a single voltage feedback path. This negative feedback path keeps output voltage V_{out} track to the reference V_{ref}. The amplified error voltage $A_v \times V_{err}$ is then pulse-width modulated to drive the buck filter. Pulse width modulation is done by comparing the amplified error voltage with a saw-tooth waveform generated by an oscillator. The two MOSFETs conduct currents to charge and discharge node LX, respectively. During non-overlapping period

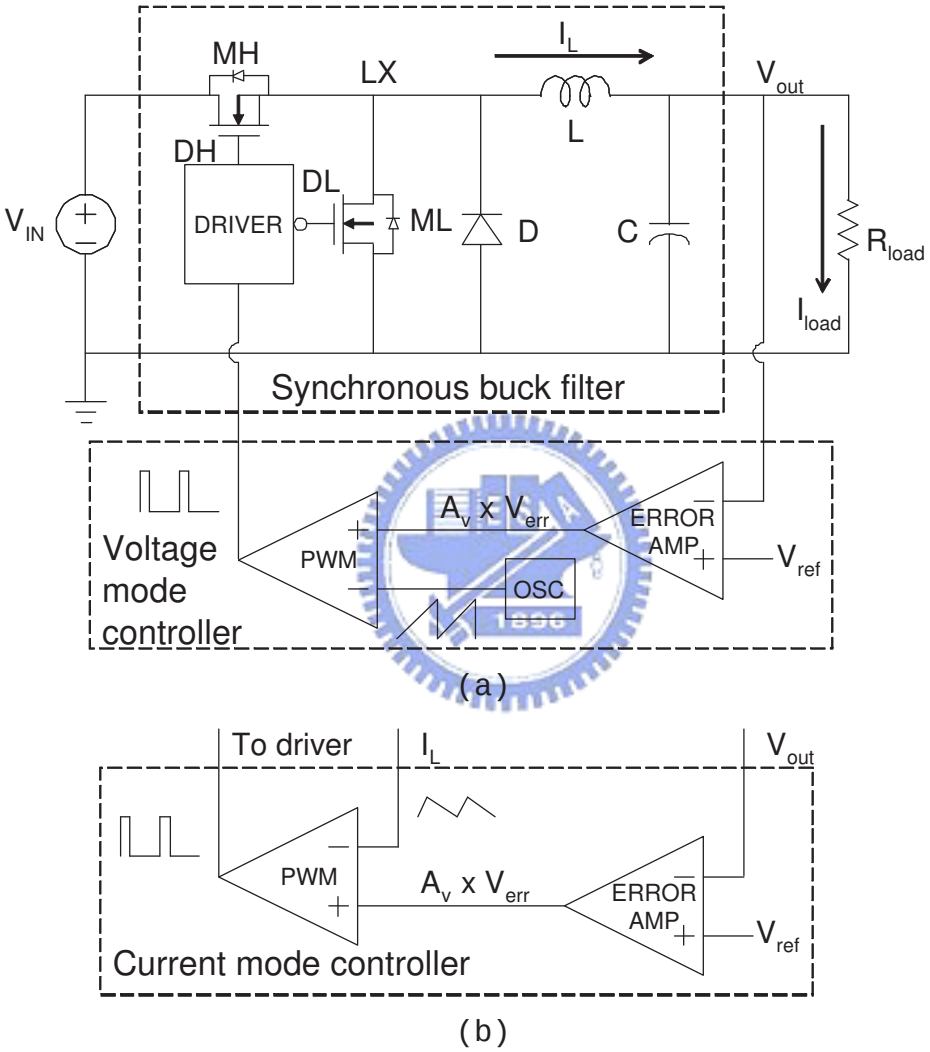


Figure 3.1: (a) Voltage-mode PWM DC–DC converter with a synchronous buck filter. (b) Current-mode controller.

of driver's output, the diode provides the inductor current a continuous path. A square wave with large current driving capability is obtained at node LX. Large inductor and capacitor filter the square wave into a nearly DC voltage. Assuming all filter components are ideal, V_{out} would be directly proportional to D.

$$V_{out} = D \cdot V_{IN} = \frac{t_{on}}{T_S} \cdot V_{IN} \tag{3.1}$$

where V_{IN} is the input supply voltage, T_S is the period of the switching frequency, and t_{on} is the on time of the PWM signal. Thus, this filter can transform the DC input voltage V_{IN} down to DC output voltage V_{out} very efficiently.

The major advantages of the voltage-mode control are simple feedback loop design and good noise margin. The PWM signal is generated from a large-amplitude saw-tooth waveform. However, any change in line or load is treated as an error of output voltage and must be corrected through the feedback loop. This means both slow line and load transient responses. Loop gain variation caused by the change in line also complicates the feedback compensation. The output filter consisting of an inductor and a capacitor adds two poles to the control loop. Thus, either dominant pole compensation or an added zero is required in the compensation. Voltage feed-forward is used to solve poor line regulation of the voltage-mode control. This is done by making the slope of the saw-tooth waveform proportional to input voltage. Therefore, the duty ratio responds to line variation immediately and loop gain is kept constant. However, application of voltage-mode control is still limited by its slow load transient response.

The introduction of current-mode control alleviates major drawbacks of voltage-mode control. Figure 3.1(b) depicts a typical diagram of current-mode controller. A voltage

signal proportional to output inductor current is used to replace the saw-tooth waveform in voltage-mode control. Because the error voltage represents the inductor current instead of output voltage, the effect of the output inductor is eliminated by the inner current control loop. Since there is only a single pole contributed by the output filter, simpler compensation and higher gain bandwidth are obtained. Fast line transient response is another advantage of the current-mode control. The rising slope of the inductor current is proportional to $V_{IN} - V_{out}$, the duty ratio responds instantaneously to the change in input voltage. This attains to both fast response and invariable control gain with line voltage changes.

Although current-mode control exhibits better dynamic performance over conventional voltage-mode control, there exists several drawbacks to a peak-sensing current-mode converter. First, open loop instability above 50 % duty ratio must be solved by slope compensation. Second, because the saw-tooth waveform derived from inductor current is small, noise will be easily inserted to the control loop, corrupting the stability. Therefore, current-mode control is not suitable for light load and wide line input/output load conditions.

3.3.2 Converter Load Transient Response

In a real condition, transistors MH and ML in Fig. 3.1(a) act as switches but their on-state resistance R_{ON} are not zero. Figure 3.2 shows an actual waveform of LX when R_{ON} is not zero. During the on time of DH, the inductor current I_L flows through MH and causes a voltage drop $I_L \cdot R_{ON} = V_{NMOS}$ across MH. At this time, voltage at LX is $V_{IN} - V_{NMOS}$. During the off time of DH, I_L flows through ML and voltage at LX is $-V_{NMOS}$. The

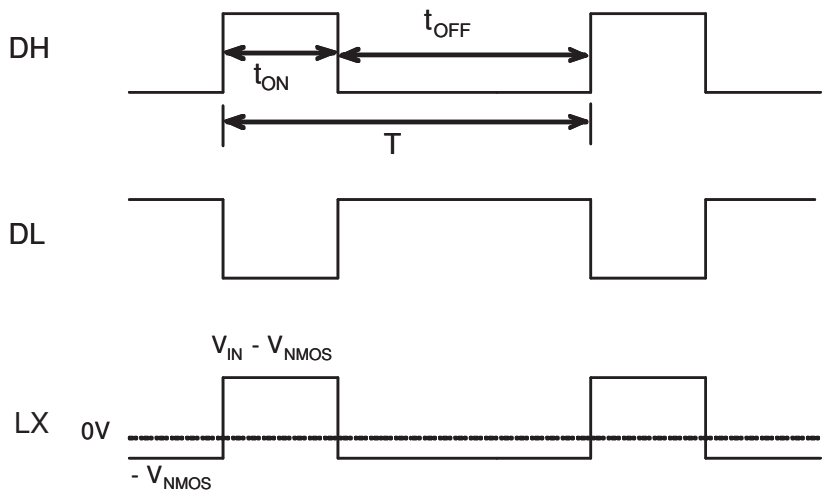


Figure 3.2: Actual waveform of LX when R_{on} of MOSFET is not zero.

output voltage is the average voltage at LX. Equation 3.1 is modified to the following equation:

$$\begin{aligned} V_{out} &= \frac{1}{T_S}[(V_{IN}-V_{NMOS})\cdot t_{ON}+(-V_{NMOS})\cdot t_{OFF}] \\ &= \frac{t_{ON}}{T_S}\cdot V_{IN}-V_{NMOS} \end{aligned} \tag{3.2}$$

From Eq. (3.1) and (3.2), assume NMOS $R_{ON} = 10$ mΩ and $V_{IN} = 5$ V, when $I_{load} = 0$:

$$D_0 = \frac{t_{ON,0}}{T} = \frac{V_{out}}{V_{IN}} \tag{3.3}$$

When $I_{load} = 20$ A:

$$\begin{aligned} D_{20A} &= \frac{t_{ON,20\ A}}{T} = \frac{V_{out}}{V_{IN}} + \frac{V_{NMOS}}{V_{IN}} \\ &= \frac{t_{ON,0}}{T} + \frac{20\ A\cdot 10\ m\Omega}{V_{IN}} \\ &= D_0 + 0.04 \end{aligned} \tag{3.4}$$

Even though there is a large increase in I_{load} from 0 to 20 A, the duty ratio D only increases by 4 %. The steady state duty ratio is mainly determined by V_{out}/V_{IN}. This

is one of the important features of the PWM regulator. From this point of view, the controller of a voltage-mode PWM regulator only have to make a small change in duty ratio when I_{load} increases from 0 to 20 A. However, owing to the nature of the LC filter, there are complicated operations between these two steady load conditions. Figure 3.3 shows transient responses of the average inductor current and the output voltage during a load transient. In the beginning of the transient, the output capacitor supplies extra current to the load because the inductor cannot provide sufficient current in a sudden. Output voltage drop V_1 caused by equivalent series resistance (ESR) of the output capacitor is proportional to the load increment. Output voltage will continue to drop until the inductor current equals to the output current ($t = T_1$). Dashed line represents output voltage of a slow response converter. Voltage drop V_2 is deeper in the slow converter. In voltage mode, a change in load is treated as an error in output voltage. The output voltage will settle to a final value after several iterations through the control loop. The longest delay in the control loop is the LC time constant. Therefore, voltage-mode control is slow because the duty ratio is all determined by V_{out}.

3.3.3 Control Architecture

In this dissertation, a simple implementation of digital voltage-mode controller is proposed. The duty ratio ($D\,[k]$) is generated from integral of error voltage (V_{err}), which is stated below:

$$D[k] = \sum_{n=0}^{k} (K_v \times V_{err}[n]) \tag{3.5}$$

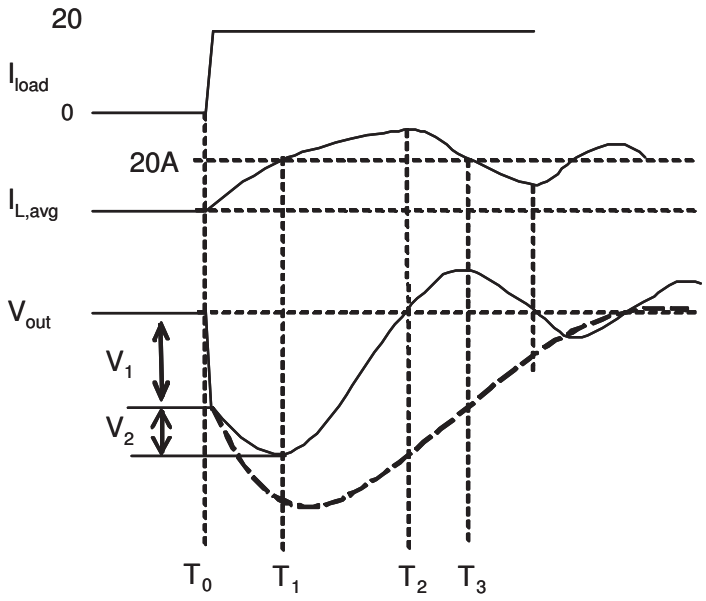


Figure 3.3: Transient responses of the average inductor current ($I_{L,avg}$) and the output voltage during a load transient.

where K_v is a constant. For comparison, duty ratio of conventional digital voltage-mode control is stated below:

$$D[k] = K_v \times (V_{ref} - V_{out}[k]) \tag{3.6}$$

There are two differences between Eqs. 3.5 and 3.6. First, $K_v \times V_{err}$ is equivalent to $K_v \times (V_{ref} - V_{out})$ mathematically, but they differ in hardware realization. In Eq. 3.6, ADC input range of V_{out} must cover the entire input voltage that is usually 5 V because V_{ref} may vary with application. Moreover, the resolution of the ADC must be at least 8 bits to obtain sufficient duty ratio accuracy. However, if V_{err} is digitized instead of V_{out}, ADC input range of V_{err} only has to cover the vicinity of zero, for example ± 1 V. Second, because $D[k]$ is an integral of V_{err}, the ADC resolution can be reduced with the magnitude of V_{err}, i.e. the resolution is decreased with increasing magnitude of V_{err} and vice versa. An example quantization table used in this design is shown in Fig. 3.4. The

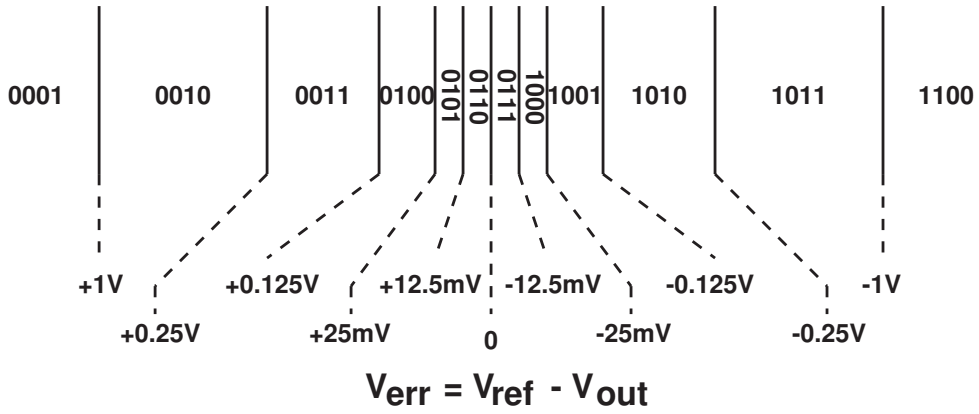


Figure 3.4: Quantization table of error voltage.

integrator together with the feedback loop will settle the output voltage to the final value V_{ref} without losing accuracy. Because the controller is composed of a simplified ADC and an integrator, it requires less hardware as compared to conventional voltage-mode controllers.

Owing to the high DC gain of the integrator-based controller, load regulation and line regulation of regulator are excellent. And the integration operation is insensitive to high frequency noise. However, this controller is inherently slow. It suffers from slow transient response. Therefore, proportional current feedback technique is proposed to improve the dynamic response. The proportional current feedback technique can be expressed as the following equation:

$$\begin{aligned} D[k] &= \sum_{n=0}^{k} (K_v \times V_{err}[n]) \\ &\quad + I_L[k] \times K_{cfb} \times V_{err}[k] \end{aligned} \tag{3.7}$$

Equation 3.7 includes two terms: The first integration term is the same as Eq. 3.5; the second term represents the proportional current feedback. Inductor current is sensed as a feedback signal. When the inductor current rises, the duty ratio will increase as well.

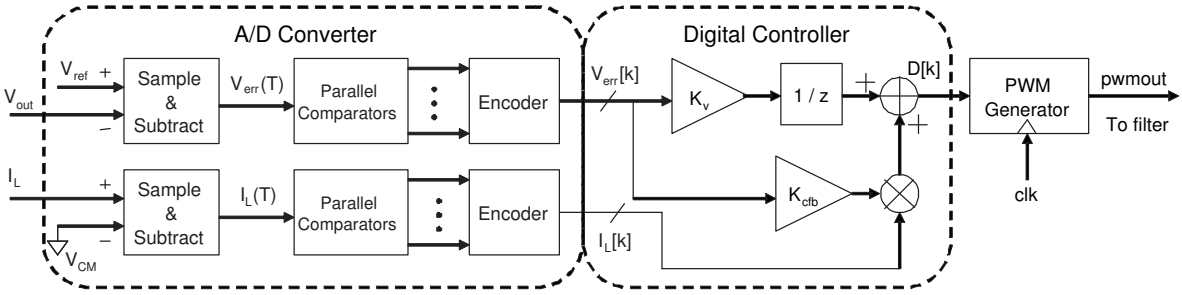


Figure 3.5: Proposed block diagram consists of: A/D converter, digital controller, and PWM generator.

Proportional current feedback means the amount of current feedback is proportional to V_{err}. The more V_{out} drops, the more amount of current feedback is added to duty cycle. As discussed in the above text, while the output current increase from 0 to 20 A, the steady state duty ratio only increases by 4 %. However, during the load transient, variation of the duty ratio should be very large to prevent deep output voltage drop. Proportional current feedback accelerates recovery rate in two ways: First, inductor current variation directly affects the duty ratio. Second, voltage drop caused by the ESR is compensated by the error voltage proportional feedback. Therefore, dynamic response is improved by the proportional current feedback. When V_{out} approaches to V_{ref}, the amount of current feedback is reduced gradually to keep the system stable. At the final state, the duty ratio contributed by the proportional current feedback is reduced to zero. The small duty ratio increment needed from one loading condition to another is generated by the voltage loop. This proportional feature helps the system to attain both fast transient response and stable steady state response.

3.4 Circuit Design

Figure 3.5 shows the block diagram of the proposed digital PWM DC–DC converter which consists of three parts: A/D converter, digital controller, and PWM generator.

3.4.1 A/D converter

This block samples V_{err} and I_L and transforms them into digital codes. Most of the digital controllers use linear A/D converters to convert V_{out} to digital codes. Error voltage V_{err} is obtained by subtracting digitized V_{out} to the reference V_{ref}. For future microprocessor voltage regulator module (VRM) applications, load current slew rates are more than 50 A/μs and regulation tolerances are less than 2 % [12]. A/D converters with high resolution and fast sampling rate are required to meet tight regulation tolerances and fast switching frequency. Although high resolution can be obtained from multistage A/D converters (pipeline and sigma-delta topology), their high conversion latency seems not suitable for real-time control. Flash topology can achieve a very high speed, low latency A/D conversion. However, its cost and power consumption grow exponentially with resolution. It is beneficial to avoid using these high power and expensive A/D converters. In this dissertation, a more simplified A/D conversion topology is proposed. Because V_{err} is the actual signal to evaluate proper duty ratio, the subtraction of V_{ref} and V_{out} is done by analog circuits. V_{err} is then converted into digital codes. Instead of using a full-range ADC, input range of the A/D conversion only covers the vicinity of zero. The resolution is not uniform for the input range. The mapping of V_{err} is partitioned into different sizes of region. As shown in Fig. 3.4, resolution is higher in the central region and lower when the error voltage is large. The basic idea is: when the error voltage is large, only the direc-

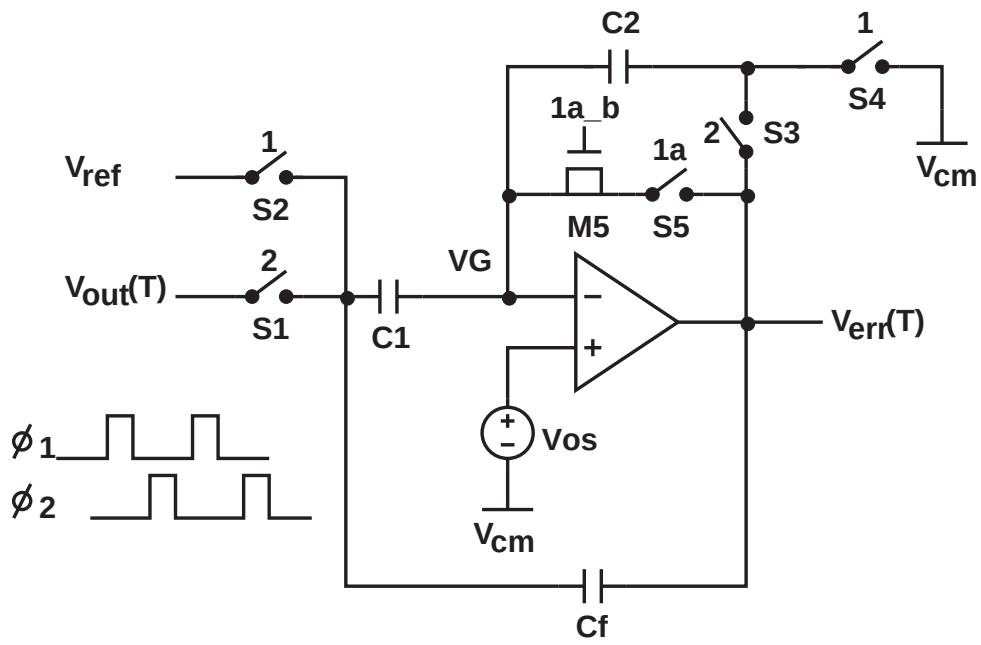


Figure 3.6: Sampling and subtraction circuit for V_{out}.

tion and rough magnitude need to be measured. Higher resolution is needed to compute precise results only when V_{out} is close to V_{ref}. In general cases, when V_{out} is the signal to be converted, minimum discriminable difference of 12.5 mV at $V_{IN} = 5$V corresponds to 8–9 bits A/D conversion resolution. In addition, static and dynamic tolerances of target application determine the partition of quantization table. Therefore, large area is saved using this topology. I_L is encoded in 5-bit. Because I_L is used to reflect its extent of change, the resolution of I_L need not be high.

Figure 3.6 shows the sampling and subtraction circuit for V_{out}. During each sampling period, it samples V_{out} and generates V_{err} by subtracting V_{out} from V_{ref}. Low frequency errors such as OPAMP offset and flicker noise are canceled with the correlated double sampling (CDS) technique. The CDS technique has originally been introduced to reduce the noise produced in charged-coupled devices (CCD's) [61]. It is widely used in sampled-

data systems and particularly in switched-capacitor (SC) circuits [62]. Assume clock phase ϕ_1 and ϕ_2 are non-overlapping and ϕ_{1a} is an early phase of ϕ_1. At time $t = t_1$, $\phi_1 = 1$:

$$V_{err}(t_1) = V_{os}(t_1) \tag{3.8}$$

And at time $t = t_2 = t_1 + T_s/2$, $\phi_2 = 1$:

$$\begin{aligned} V_{err}(t_2) &= -\frac{C1}{C2}(V_{out} - V_{ref}) \\ &\quad + (1 + \frac{C1}{C2})[V_{os}(t_2) - V_{os}(t_1)] \end{aligned} \tag{3.9}$$

where T_s is the period of the clock. Therefore, if V_{os} doesn't change with time, the second term would be eliminated. Then V_{err} will be only proportional to the difference between V_{out} and V_{ref}. NMOS switch is used for S5 to reduce parasitic capacitance in the negative input node of the opamp (VG). At the moment S5 is open, its channel charge will flow into VG and produces error voltage at output. Consequently, M5 is used to compensate this excess charge. Because both source and drain of M5 are tied together, size of M5 should be half of that of S5. To prevent channel charge of S2 to be stored in C1, VG should be floating when S2 is open. Thus, S5 should be open earlier than S2. Cf provides the OPAMP a feedback path when both $\phi 1$ and $\phi 2$ are low. Subtraction error can be as low as tenths of 1mv even when large offset exists. With careful layout techniques, matching accuracy between C1 and C2 can be better than 0.1 % [63]. This ensures adequate subtraction precision to obtain correct A/D conversion results.

Parallel comparators are used to convert V_{err} and I_L to digital codes because their resolutions are relatively low. Low conversion latency of this "flash" conversion is desirable to reduce control latency which is especially important when the response speed is a major consideration.

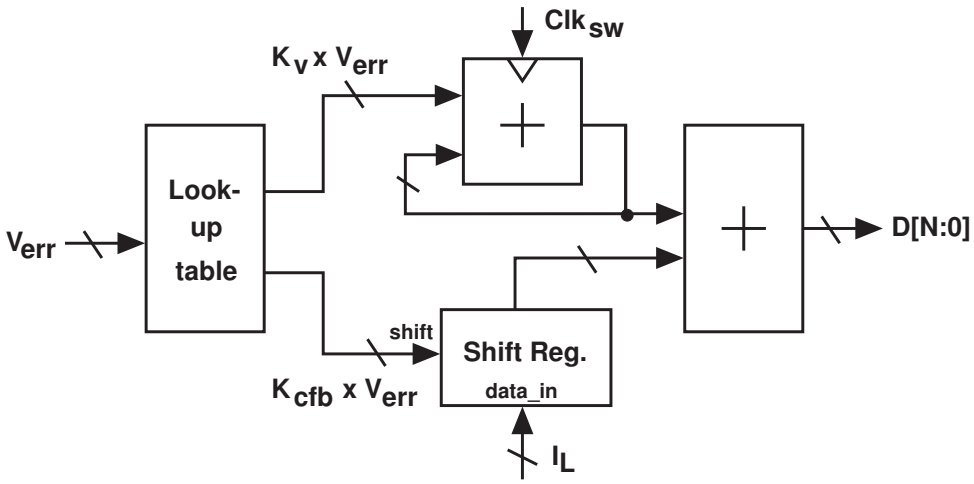


Figure 3.7: Circuit diagram of the digital controller.

3.4.2 Digital Controller

The digital controller performs duty ratio calculations in Eq. 3.7 which involve integration, multiplication, and addition. These numerical computations are usually performed by microcontrollers or DSPs. However, since V_{err} is partitioned into few regions and K_v is a constant, duty ratio increments ($K_v \times V_{err}$) can be pre-calculated and stored on chip or in an external memory device. The term $K_{cfb} \times V_{err}$ can be also pre-calculated. These data will only occupy little memory space. An accumulator is used as the integrator. Increments are accumulated in each switching cycle. Multiplication of $K_{cfb} \times V_{err}$ with I_L can be simplified to bit-wise shift of I_L if we choose $K_{cfb} \times V_{err}$ to be integer power of 2. Circuit diagram of the digital controller is shown in Fig. 3.7. An example of duty ratio calculation is shown below. Assume output resolution of duty ratio is 8 bits, we set V_{err} = 0.1 V, $K_v = 8$, and $K_{cfb} = 128$. According to Fig. 3.4, V_{err} is in the region between 25 mV and 125 mV. Average of this region ((25 mV + 125 mV)/2 = 75 mV) is used to calculate $K_v \times V_{err}$ and $K_{cfb} \times V_{err}$. That is, $K_v \times V_{err}$ and $K_{cfb} \times V_{err}$ are 0.6 and 9.6

respectively. $K_{cfb} \times V_{err}$ is approximated to 8 that is an integer power of 2. Therefore, duty ratio $D[k]$ is generated as follows:

$$\begin{aligned} D[k] &= \sum_{n=0}^{k} (K_v \times V_{err}[n]) + I_L[k] \times K_{cfb} \times V_{err}[k] \\ &= \left(\sum_{n=0}^{k-1} (K_v \times V_{err}[n]) + K_v \times V_{err}[k] \right) \\ &\quad + I_L[k] \times K_{cfb} \times V_{err}[k] \\ &= \left(\sum_{n=0}^{k-1} (K_v \times V_{err}[n]) + 0.6 \right) + I_L[k] \times 8 \end{aligned} \tag{3.10}$$

The first term is generated by the integrator and the second term is generated by the proportional current feedback. In the next cycle, assuming V_{err} is in the same region ($V_{err}[k] = V_{err}[k+1]$), $D[k+1]$ will be:

$$\begin{aligned} D[k+1] &= \sum_{n=0}^{k+1} K_v \times V_{err}[n] \\ &\quad + I_L[k+1] \times K_{cfb} \times V_{err}[k+1] \\ &= \sum_{n=0}^{k} K_v \times V_{err}[n] + K_v \times V_{err}[k+1] \\ &\quad + I_L[k+1] \times K_{cfb} \times V_{err}[k+1] \\ &= \sum_{n=0}^{k} K_v \times V_{err}[n] + I_L[k] \times K_{cfb} \times V_{err}[k] \\ &\quad + K_v \times V_{err}[k+1] \\ &\quad + I_L[k+1] \times K_{cfb} \times V_{err}[k+1] \\ &\quad - I_L[k] \times K_{cfb} \times V_{err}[k] \\ &= D[k] + 0.6 + (I_L[k+1] - I_L[k]) \times 8 \end{aligned} \tag{3.11}$$

Because $K_v \times V_{err}$ and $K_{cfb} \times V_{err}$ are obtained from a look-up table, only addition and bit-wise shift are performed by the control circuit. Both size and complexity of the

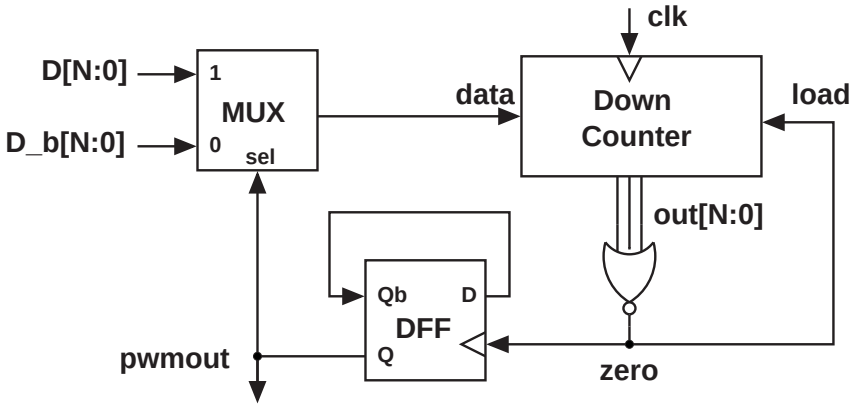


Figure 3.8: N-bit counter based PWM generator.

controller are greatly reduced and can be integrated with other circuits. For flexibility in different loading conditions, tuning is done by simply changing the gain parameters stored in an external memory device.

Internal resolution of the controller is higher than the PWM generator by several bits. It achieves finer control without losing fast response when duty increments per switching cycle are less then 1 LSB.

3.4.3 PWM Generator

The PWM generator receives duty ratio from the digital controller and modulates it to PWM signal. An N-bit counter based PWM generator is shown in Fig. 3.8. In the beginning of a switching cycle, the counter loads new duty ratio $D[N:0]$ and counts down. After D clock cycles, zero is detected at the output of counter. The PWM output is reset and the counter loads one's complement of the duty ratio (D_b). After D_b clock cycles, the PWM output is set and the switching cycle ends. Therefore one switching period equals $(D+1)+(D\_b+1) = 2^N+1$ clock cycles. Different from general counter based PWM generators, only one counter is used to count both ON and OFF duration.

Switching frequency of PWM output (f_{SW}) depends on the duty ratio resolution (N bits) and the input clock frequency (f_{clk}). Their relationship is stated below:

$$f_{SW} = \frac{f_{clk}}{2^N + 1} \tag{3.12}$$

Higher resolution means better control over the duty ratio. There are two reasons for the need of a high-resolution PWM generator. First, resolution of the PWM generator must be higher than the A/D converter in order to eliminate the limit cycles effect [36]. Limit cycles refer to steady-state periodic oscillations of the output voltage that are not due to the PWM switching activity. Second, since the differentiation of inductor's current is proportional to the voltage across it, gradual change of duty ratio is needed to avoid large peak current. However, clock frequency must be doubled to increase resolution by one bit if switching frequency is kept the same. Thus, 8-bit resolution is moderate if switching frequency is around 200 kHz. For an 8-bit system with a 40 MHz clock, the duty ratios range from 1/257 to 256/257 and the switching frequency f_{sw} is 155.6 kHz.

3.5 Time Domain System Modelling and Simulation

3.5.1 Behavior Modelling

System response of the proportional current feedback technique stated in Eq. (3.7) can be analyzed by mathematic tools. However, the circuit implementation described in the previous section usually requires transistor level simulation. To examine the system response in time domain, using transistor level simulation is precise but time consuming. A behavior model that describes circuit operations is necessary. Behavior model of the system is shown in Fig. 3.9. Functions of the blocks are to simulate real circuit behavior.

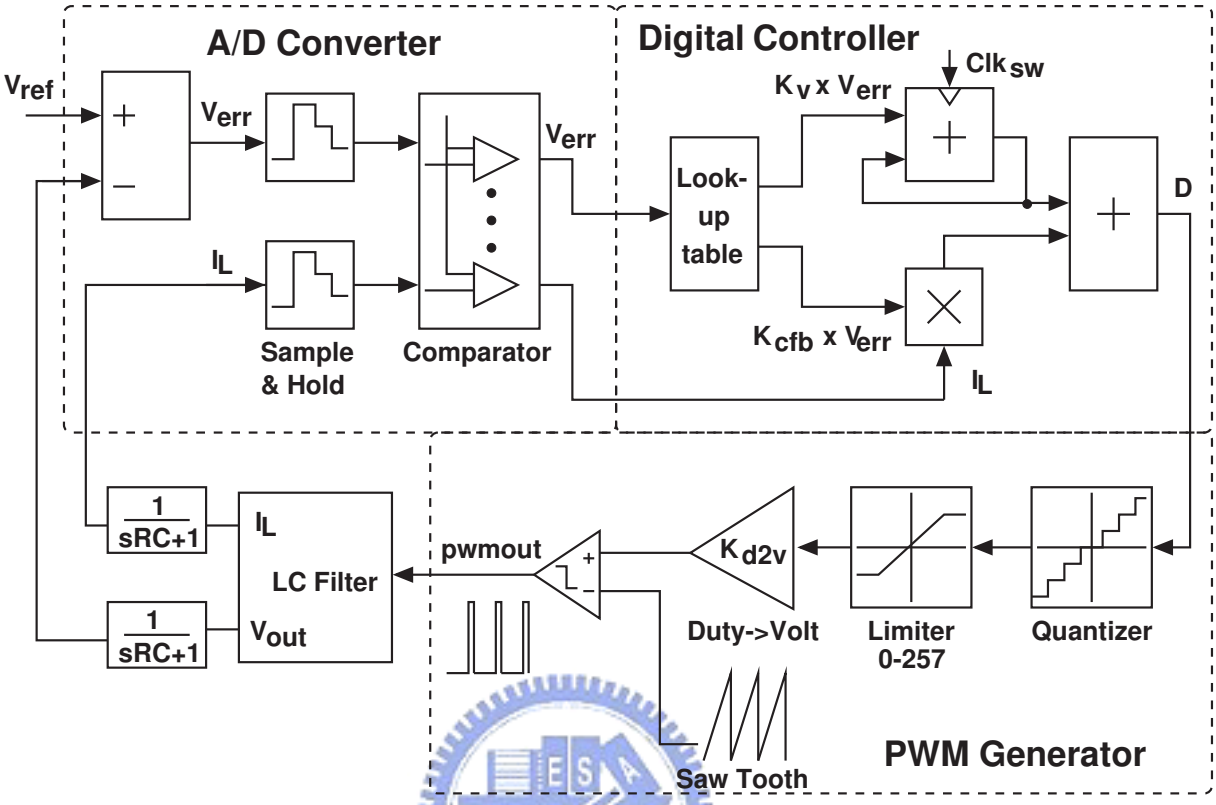


Figure 3.9: Behavior model for MATLAB simulation.

Fast and accurate results can be obtained from this model.

In the A/D converter model, two sample and hold blocks are used to convert V_{err} and I_L to discrete-time analog signals. The following comparators quantize these signals to digital codes according to the encoding table shown in Fig. 3.4. The corresponding values of $K_v \times V_{err}$ and $K_{cfb} \times V_{err}$ are read from the look-up table and then send to the algorithmic blocks. The blocks in the PWM generator modulate the duty ratio D calculated by the digital controller. The quantizer and the limiter are to simulate real behavior of the circuit. The quantizer cuts the duty ratio to integers and the limiter avoids over range conditions. The LC filter block contains an LC low pass filter. R_{ON} of the switch MOSFET and ESR of the inductor and capacitor are also included. Two

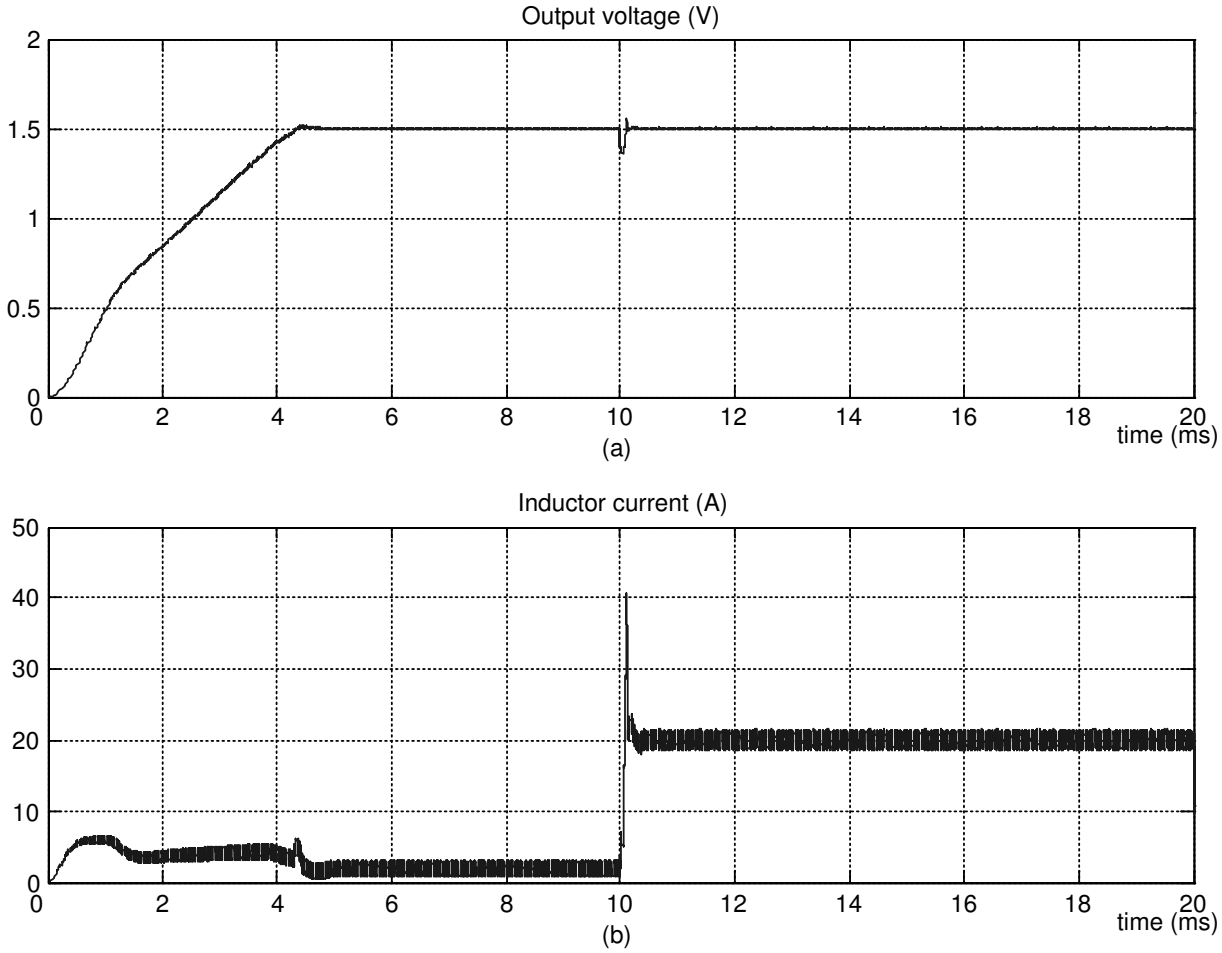


Figure 3.10: Step load transient response. Parameters are listed in Table 3.1. (a) Output voltage. (b) Inductor current.

low pass filters after the LC filter block are used to obtain average value of the inductor current and output voltage.

3.5.2 Simulation Result

Circuit model of the system has been simulated using the MATLAB mathematical simulator. Parameters are listed in Table 3.1. Values of K_v and K_{cfb} are for the 8-bit arithmetic operations, in which duty ratio values are from 0 to 255. Step load response is shown in Fig. 3.10. V_{IN} is 5 V and V_{ref} is 1.5 V. Switching frequency of PWM signal is 155.6 kHz.

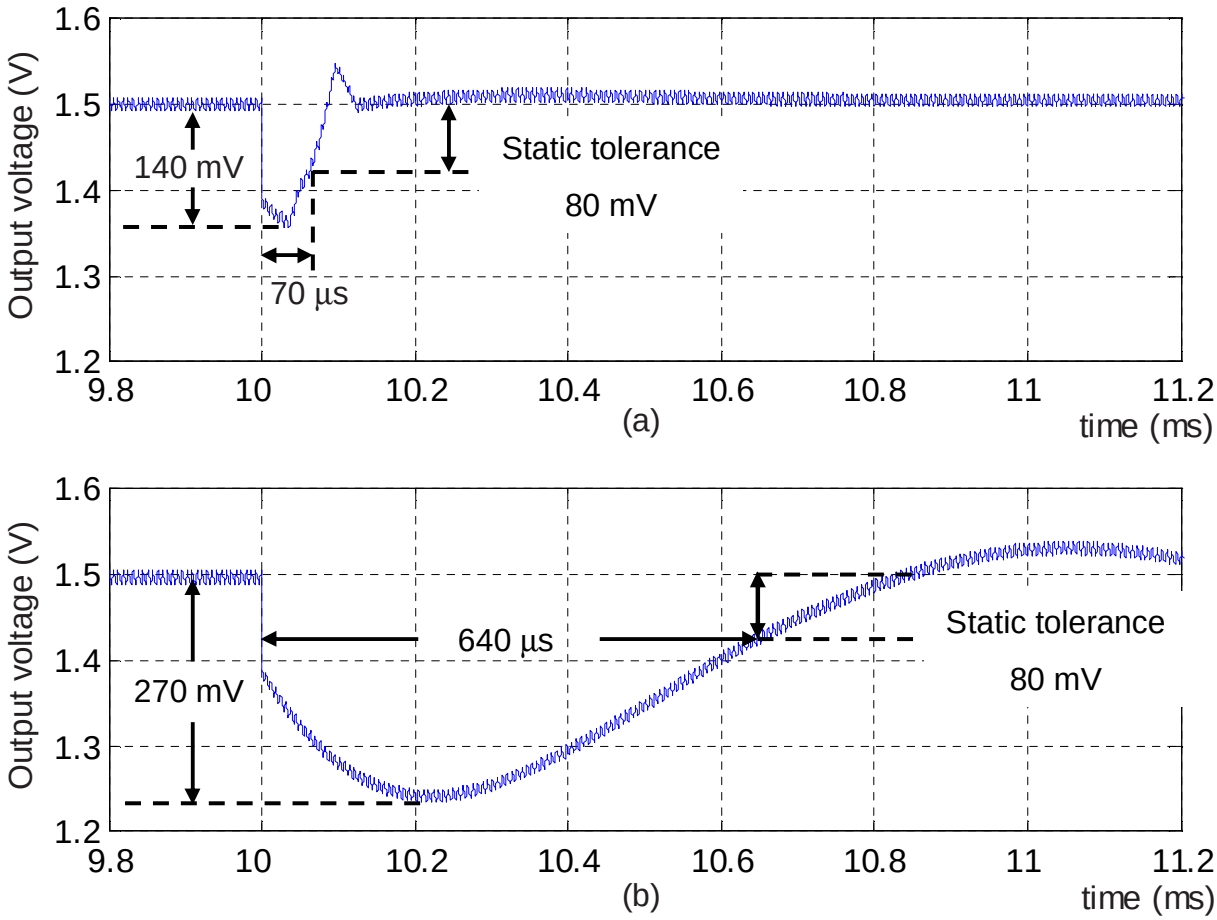


Figure 3.11: Zoomed waveforms of output voltage response. (a) With proportional current feedback, V_{out} dropped about 140 mV and returned to within static tolerance in less than 70 μs. (b) Without proportional current feedback, output voltage response didn't meet the requirement.

Before time = 5 ms, the system was in the soft-start mode. Rising rate of the output voltage is limited to prevent inductor current spike. This is done by reducing voltage gain K_v and breaking the proportional current feedback loop. According to the encoding table shown in Fig. 3.4, duty ratio increments in the same region are the same. Therefore, the output voltage exhibited uniform rising rate in the same region. Transition points can be observed at 0.5 V and 1.25 V. When the output voltage is close to the V_{ref}, the system will switch to normal mode. At t = 10 ms, a load transient occurred from 2 A to 20 A with a slope of 20 A/μs, which simulates maximum load condition when a microprocessor awakes from sleep mode to active mode. According to VRM 8.4 [8], output voltage deviation should be less than 130 mV and should not exceed static tolerance (80 mV) for longer than 100 μs. As Fig. 3.11(a) shows, V_{out} dropped less than 140 mV and went back to static tolerance in 70 μs. Note that ESR of the output capacitor can cause an output voltage drop of 120 mV, which can be calculated from the product of r_C (6.67 mΩ) and ΔI_{load} (20 A − 2 A = 18 A). V_{out} drop caused by the controller that corresponds to V_2 in Fig. 3.3 was 20 mV. To illustrate the effectiveness of the proportional current feedback, the output voltage response without proportional current feedback is shown in Fig. 3.11(b). The maximum deviation of V_{out} was 270 mV and recovery time was 640 μs. Performance did not meet the requirements.

3.6 Experiment Results

The circuits described in Sec. 3.4 are implemented to verify system responses. Figure 3.12 shows the photomicrograph of the system fabricated in a 0.6 μm digital CMOS process. Die size is 1.8 × 1.8 mm^2 including I/O pads. Digital circuits including the digital

Table 3.1: Parameters.

Filter inductor, L	3 μH
Filter capacitor, C	9 mF
DCR of inductor, r_L	10 mΩ
ESR of capacitor, r_C	6.67 mΩ
On-state resistance of MOSFET, R_{ON}	10 mΩ
Switching frequency, f_{sw}	155.6 kHz
Input voltage, V_{IN}	5 V
Reference voltage, V_{ref}	1.5 V
Voltage gain, K_v	8 (in 8 bit)
PCF gain, K_{cfb}	128 (in 8 bit)
Duty ratio resolution, N	8 bit

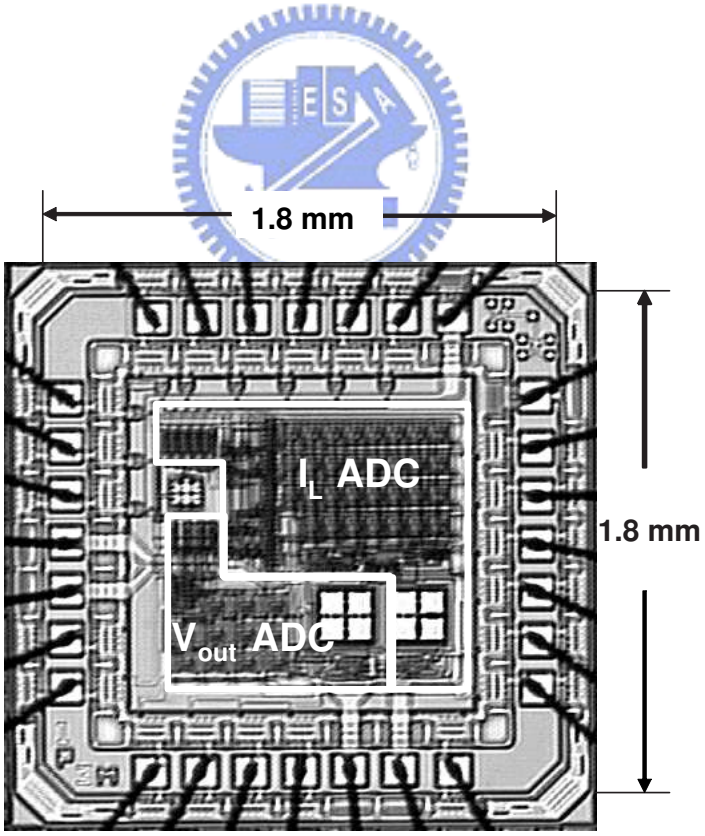


Figure 3.12: Photomicrograph of the implemented chip.

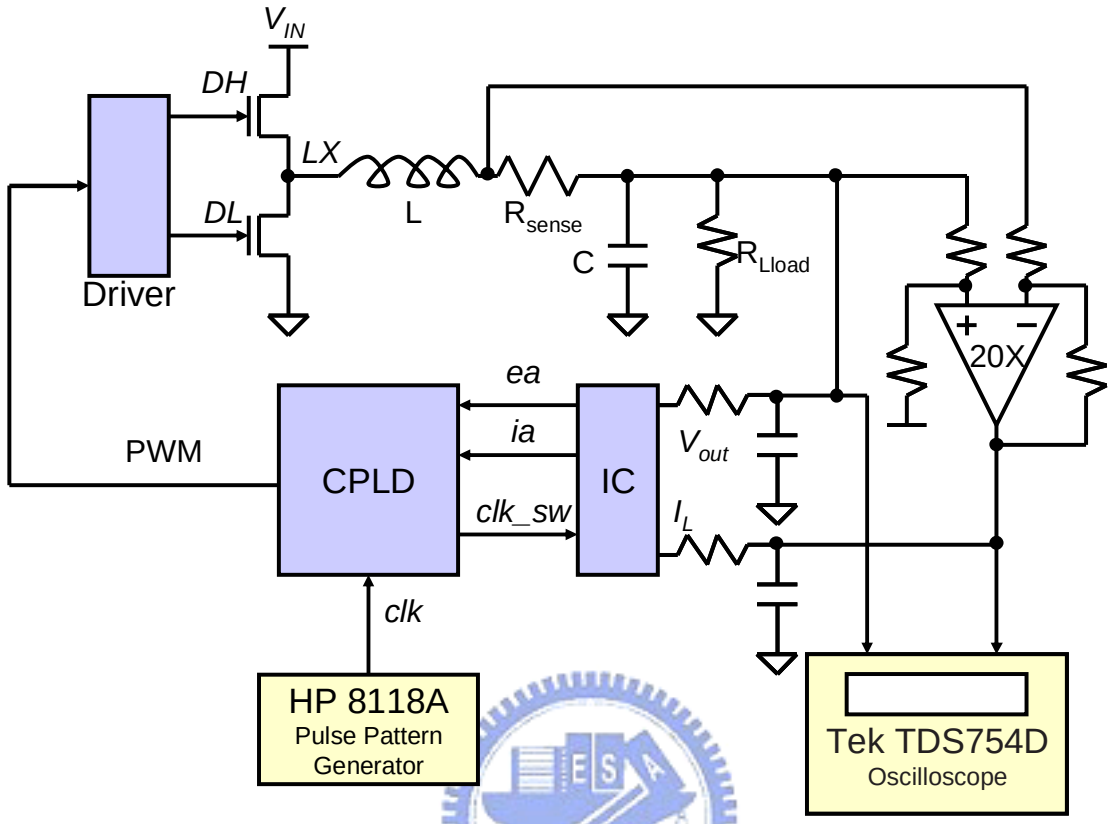


Figure 3.13: Experiment setup.

controller and the PWM generator are not implemented on the chip for programmability. Experiment setup is shown in Fig. 3.13. A complex programmable logic device (CPLD) was used to implement digital circuits in the experiment. Trace resistance in the inductor current path was used to obtain the value of inductor current. The resistance was about 4 mΩ. Before converted to a 5-bit digital signal, voltage across the trace resistance is amplified by twenty times. The ADC input range of the inductor current is from 2 V to 4 V. Signal filters of V_{out} and I_L are used to reduce voltage spikes and high frequency noise caused by switching operation.

Measured step response of this chip is shown in Fig. 3.14. Measured step response without proportional current feedback is shown in Fig. 3.15. Test conditions are the same

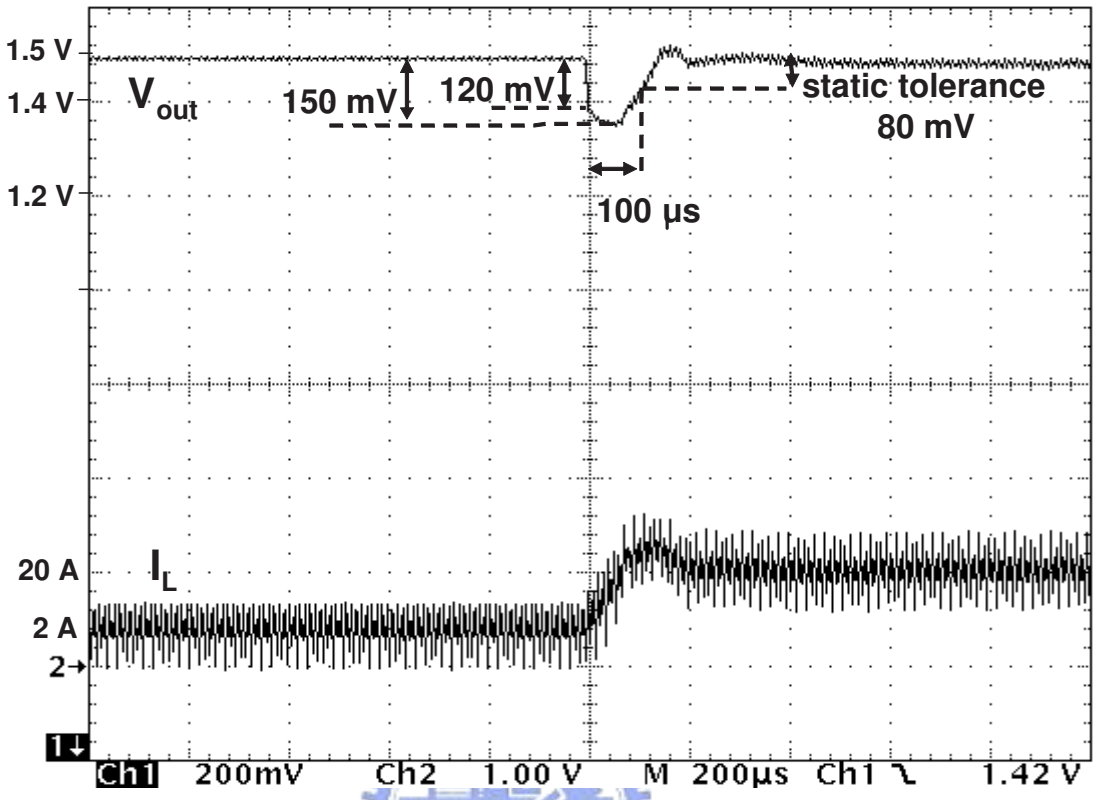


Figure 3.14: Measured step responses *with* proportional current feedback technique. Top: output voltage. Bottom: inductor current.

as those in simulation. When the load current rose from 2 A to 20 A, V_{out} dropped 150 mV and recovered to within static tolerance in 100 μs. ESR of the output capacitor caused an output voltage drop of 120 mV. Output voltage drop caused by the controller was 30 mV. Without the proportional current feedback, V_{out} dropped 230 mV and recovered in 550 μs. Experimental results showed similar performance predicted by the behavior model. Performance is greatly improved with the aid of proportional current feedback technique.

Efficiency of the converter was measured at 2 A load. As shown in Fig. 3.16, most the energy was dissipated in external components. A 12 V supply was used to drive MOSFET switches. The power consumption of the driver was 240 mW. The CPLD consumed 1.4 W

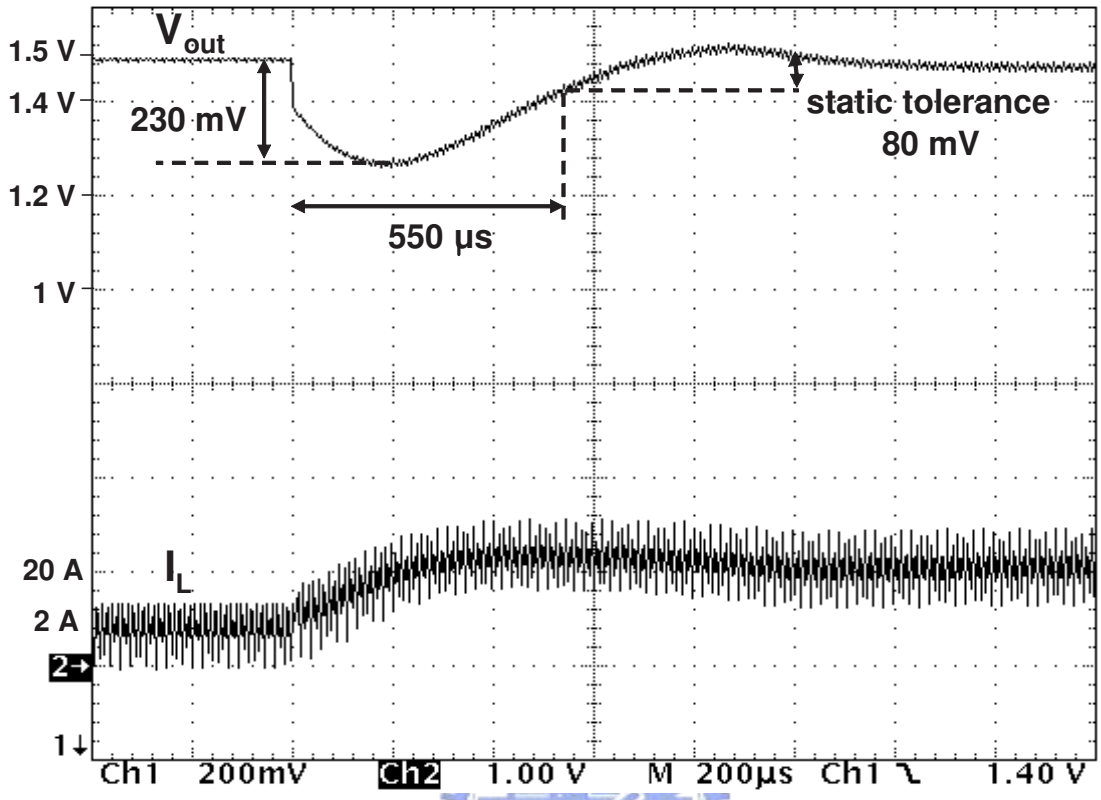


Figure 3.15: Measured step responses *without* proportional current feedback technique. Top: output voltage. Bottom: inductor current.

of power, which was one of the major energy loss in the system. The lack of transistor efficiency of CPLD compilation, high operating frequency of the counter (40 MHz), and inter-chip transmission of the switching signal might be the causes of low efficiency. The 5 V input voltage consumed 4 W of power in which 3 W was sent to the 1.5 V output. The excess power consumption was due to conduction loss, differential amplifier, and combinational logic gates for generation of synchronous gating signals. The power consumption of the control chip was only 20 mW. The measured efficiency at 2 A was 53 %. A digital controller has been reported that uses similar PWM generation approach and more complex control algorithm [64]. The power consumption of the reported controller is on the order of milliwatts. Therefore, it is possible to greatly improve the efficiency by

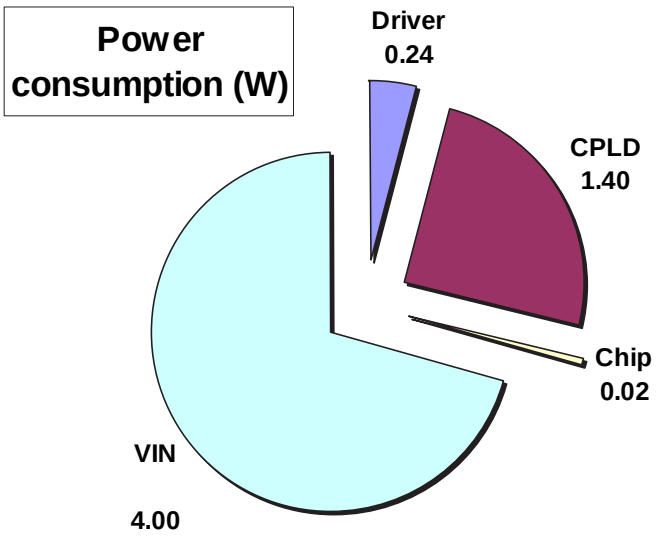


Figure 3.16: Measured power consumption at 2 A load.

integrating driver and digital circuits into the control chip.

3.7 Summary

The importance of PWM DC–DC converters is much emphasized in recent years because of their high efficiency and power packing density. Voltage-mode control is a simple topology, and therefore a popular choice in many applications. However, slow dynamic response is its major disadvantage. Current-mode control exhibits better load transient response and is widely used in applications where fast dynamic response is needed. However, noise may lead to instability when the current is small.

This dissertation has presented a simple control topology of digital PWM DC–DC converter using proportional current feedback. It retains the advantages of voltage-mode control, but has the fast load transient response like the current mode control. The proportional current feedback technique accelerates transient recovery rate and the integrator-based voltage loop achieves low DC error and stable operation. Novel circuit designs are

proposed to implement to control chip. A non-linear A/D converter with low latency and minimized cost and power consumption is presented. In addition, compact circuits design of the control law eliminates system complexity.

As shown in the results from behavior model simulation and experiments, the output voltage dropped 150 mV and recovered to static tolerance in 100 μs during a large load transient from 2 A to 20 A. Its dynamic response has been shown to meet the requirements of current applications with minimum hardware. The controller can be easily integrated on a small size chip. To adapt to different load conditions, system response can be adjusted by changing parameters in the external memory. Therefore, it is a competitive choice to current-mode control and a better solution in system integration.

Chapter 4

A Frequency Stabilized Constant On-Time Controller with Low Noise Susceptibility

Classified by switching frequency variability, common control methods for switching regulators include (a) fixed-frequency control, such as voltage-mode PWM control and current-mode PWM control; (b) variable-frequency control, also called free-running control [46], such as constant on-time, off-time control [48–50], and ripple control [26, 52–57]; and (c) quasi-fixed frequency control, which is first brought out by [51].

Generally, fixed frequency regulators are preferred because the switching frequency is selectable to avoid sensitive regions, which simplifies electro-magnetic interference (EMI) shielding in electronics equipments. In this chapter, a frequency stabilized constant on-time controller is presented. Novel error amplifier design provides loop stability compensation and improved noise immunity.

4.1 Constant On-Time Control and Frequency Stabilization Technique

Constant on-time control is a type of free-running control schemes [39, 47, 51]. Other types of free-running control are ripple control and constant off-time control. In contrast to fixed-frequency controller that uses an oscillator, free-running controller operates in a self-oscillating way. In general, performance of free-running types is better than fixed-frequency types no matter in voltage mode or current mode. Main advantages of free-running control are:

- Fast loop response.
- The tightest control over output voltage (voltage mode) or inductor current (current mode).
- Open-loop stability over full range of duty ratio without slope compensation.
- Low audio susceptibility.

Voltage-mode free-running control architecture is simpler than current-mode. It relies on the output capacitor's ESR to act as the current sensing resistor. The output ripple voltage developed across the ESR provides a ramp signal for PWM operation. As will be discussed in Subsection 5.2.4, output voltage is in phase with inductor current if the ESR is large enough.

Figure 4.1 shows the block diagram of a constant on-time buck regulator. Output voltage is compared directly with the reference voltage. The high-side MOSFET is turned on for a fixed interval determined by a one-shot timer. When the top MOSFET is turned

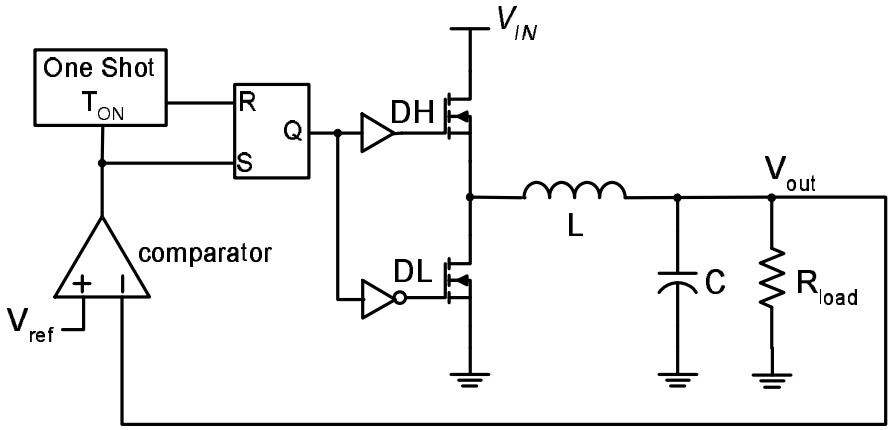


Figure 4.1: Constant on-time buck regulator block diagram.

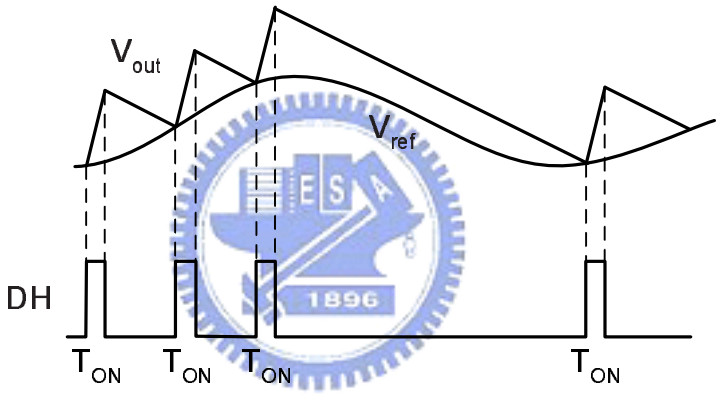


Figure 4.2: Constant on-time modulation waveform.

off, the bottom MOSFET is turned on until the output voltage falls below the reference voltage. The one-shot timer is triggered again, starting the next cycle. As shown in Fig. 4.2, the on-time pulse is fixed and the off-time pulse is varying with the reference. As a result, switching frequency is a function of operating conditions.

Many applications require stabilized or synchronized switching frequency to prevent electro-magnetic interference. In a switching converter operating in continuous conduction mode (CCM), duty ratio is mainly varied with V_{IN} and V_{out} and is affected secondarily by inductor current and temperature. These secondary factors affect parasitic voltage

drop in the inductor current path. Therefore, switching frequency of a constant on-time regulator can be stabilized by adjusting the on time according V_{IN} and V_{out} [1, 51]. If the one-shot timer generates an on time that is proportional to the duty ratio, the switching frequency is approximately constant with changes in V_{IN} and V_{out}. This feed-forward frequency stabilization technique keeps the benefits of free-running control without causing additional instability.

Instability caused by very low duty ratio has been an issue when designing a voltage regulator module for notebook computers. This problem is originated from the high input voltage (typical 9 V to 19 V) and low CPU supply voltage. This low V_{out}/V_{IN} ratio causes the instability problem to conventional PWM controllers because the on time is too short for the circuits. Constant on-time control solves this problem by generating on-time using a one-shot timer instead of monitoring output voltage or inductor current. The on-time pulse can be as short as 100 ns. Therefore, constant on-time control is stable at very low and very high duty ratios.

4.2 Stability Issues of Free-Running Control

Although constant on-time control is simple and fast, unstable operations are observed at the output. Sometimes it is a harmless perturbation. Sometimes, oscillation after load transients will trigger over- or under-voltage protection that shuts the whole system down. In this section, stability issues of constant on-time control are discussed.

4.2.1 Noise Induced Instability

All voltage-mode free-running controllers monitor the output voltage waveform as the triggering signal. In traditional voltage-mode control, averaged output voltage is sensed by the error amplifier. In constant on-tome control, however, unfiltered signal must be sent to the comparator. If the sensed output voltage is too small to be corrupted by noise, the trigger point will drift away from correct position. False triggering occurs due to noise on the output voltage or small output ramp caused by a low ESR value. In other cases, false triggering indicates the presence of loop instability. Insufficient ESR makes the output voltage at most 90 degree falls behind the inductor current, which can result in oscillations at the output after line or load perturbations. Figure 4.3 shows output voltage waveform when false triggering occurs. Arrows mark the presence of instability. DH and LX waveforms at the bottom also indicate early triggering right after the minimum off time. Ripple magnitude of output voltage and inductor current is a tradeoff in free-running control. Large ripple is required by the controller for better noise immunity and less comparator power/delay; but small ripple is always desirable especially in low voltage applications.

4.2.2 Loop Gain of Free-Running Regulator

Modulation gain of ripple control can be derived from Fig. 4.4. Consider a ripple controller without hysteresis, the output voltage charges and discharges alternately with a delay t_d. A disturbance ΔV on reference voltage causes time changes on both rising and falling ramps, those are ΔT_r and ΔT_f respectively. ΔT_r is determined by the rising slope of

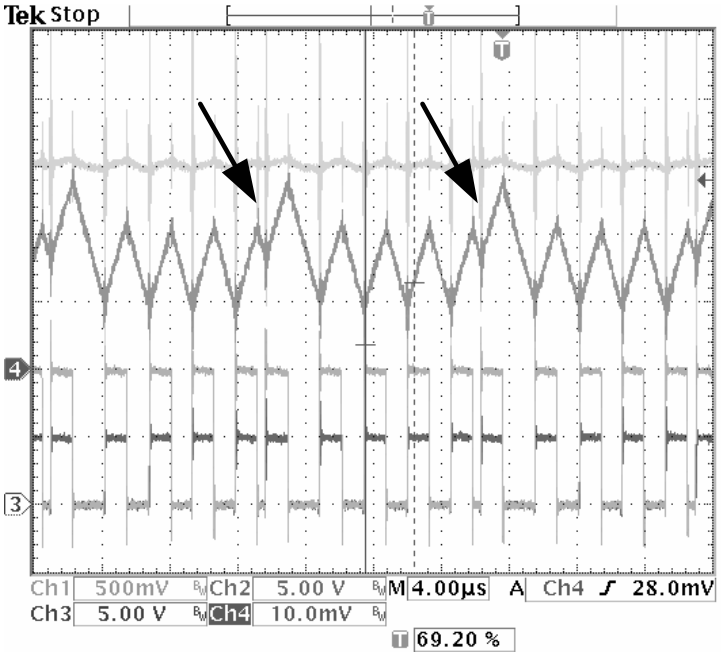


Figure 4.3: False triggering.

inductor current and ESR, r_C:

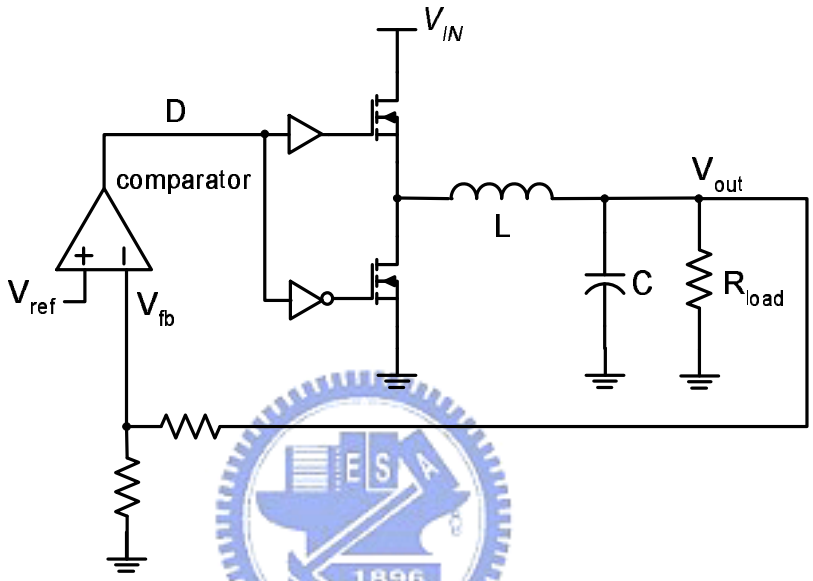
$$\begin{aligned}\Delta T_r &= \frac{\Delta V}{\frac{dV_{fb}}{dt}} = \frac{\Delta V}{r_C \frac{V_{ref}}{V_{out}} \frac{dI_L}{dt}} \\ &= \frac{\Delta V}{r_C \frac{V_{ref}}{V_{out}} \frac{(V_{IN}-V_{out})}{L}} \\ &= \frac{L}{r_C (V_{IN} - V_{out})} \frac{V_{out}}{V_{ref}} \Delta V \end{aligned} \tag{4.1}$$

where V_{ref}/V_{out} is feedback network gain. Similarly, ΔT_f is:

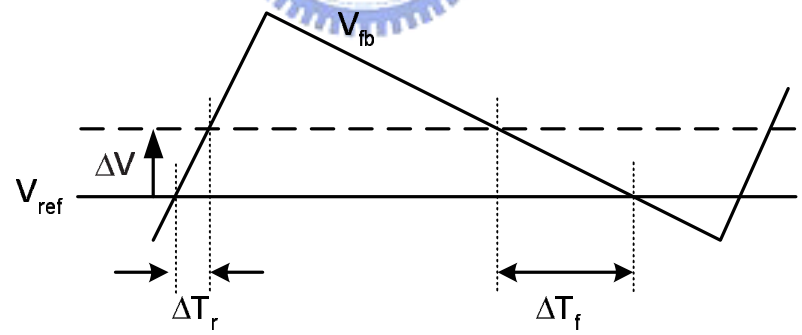
$$\Delta T_f = \frac{L}{r_C V_{out}} \frac{V_{out}}{V_{ref}} \Delta V \tag{4.2}$$

Duty ratio variation due to ΔT is:

$$\begin{aligned}\Delta D &= \frac{(\Delta T_r + \Delta T_f)}{T} \\ &= \frac{L}{r_C} \frac{V_{IN}}{V_{ref} (V_{IN} - V_{out})} \frac{1}{T} \Delta V \end{aligned} \tag{4.3}$$



(a) Regulator block diagram.



(b) Modulation waveform.

Figure 4.4: Ripple control regulator and modulation waveform.

Thus the modulation gain of ripple control, F_m, is:

$$F_m = \frac{\Delta D}{\Delta V} = \frac{L}{r_C} \frac{V_{IN}}{V_{ref}\left(V_{IN} - V_{out}\right)} \frac{1}{T} \tag{4.4}$$

Loop gain is the product of modulation gain and duty-to-output transfer function of buck filter:

$$\begin{aligned} T(s) &= F_m V_{IN} H(s) \\ &= \frac{L}{r_C} \frac{V_{IN}^2 f_{SW}}{V_{ref}\left(V_{IN} - V_{out}\right)} H(s) \end{aligned} \tag{4.5}$$

where $H(s)$ is LC filter transfer function. Since the modulation gain depends on the ripple slopes, loop gain can be compensated by changing ripple slopes.

In order to verify Eq. 4.5, loop gain of the ripple control regulator was obtained from circuit simulation. Analog modulation scheme [65, 66] has been widely used in loop gain measurement of switching regulators. As Fig. 4.5 shows, a sinusoidal modulating signal, V_{ac}, is injected in the feedback loop. The transformer blocks the modulating signal from propagating through the loop but allows switching signal's passing. Loop gain can be determined by measuring magnitude and phase response of the forward signal, V_x, to the returned signal, V_y.

In the proposed constant on-time control, there are two feedback path of the output voltage. One is for voltage regulation, another is to generate proper on time for frequency stabilization. There exist measurement problems in real condition if the loop is broken at the output point. However, accurate results can be still obtained from simulation. Loop gains of ripple control and constant on-time control regulators are simulated using analog modulation scheme. Conditions are the following: L = 2.2 μH, C = 940 μF, ESR =

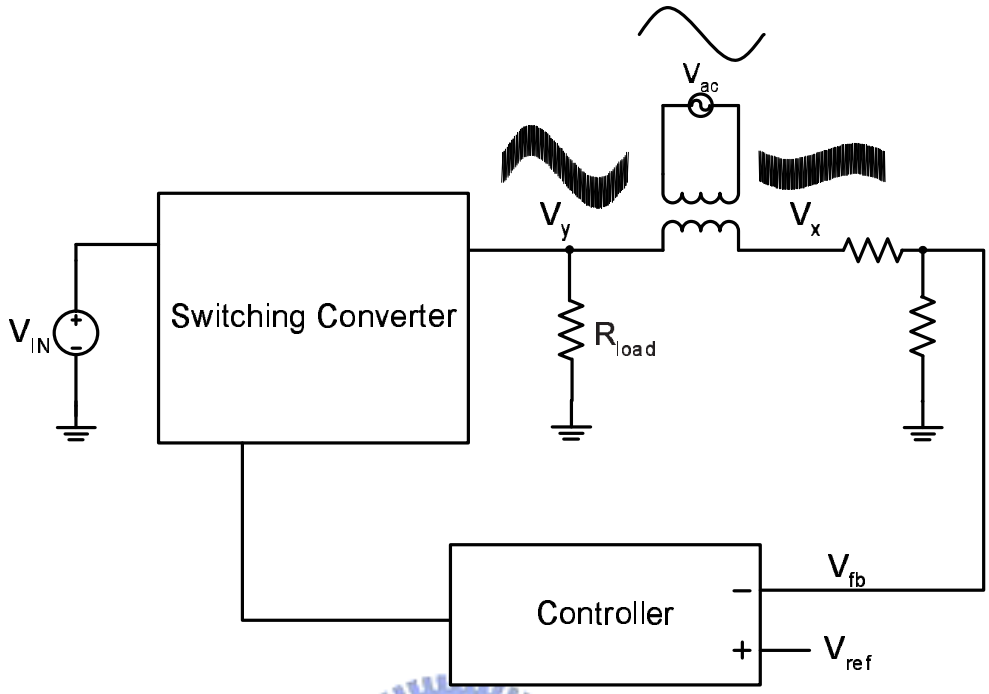


Figure 4.5: Loop gain measurement of switching regulator.

15 mΩ, V_{IN}= 20 V, V_{out} = 1.8 V, f_{SW} = 300 kHz. As shown in Fig. 4.6 and Fig. 4.7, unity-gain frequencies of both regulators are far beyond the switching frequency which is around 300 kHz. High frequency noise would pass through the loop at higher amplitude. Therefore, free-running regulators are very sensitive to noise.

In summary, the disadvantages of free-running control are:

- Sensitive to noise. Requires large output voltage and inductor current ripple.
- (In voltage mode,) Large capacitor ESR is required to keep output voltage in phase with in inductor current.
- Requires a fast, high-gain, and power-consuming comparator to amplify small output ripples.

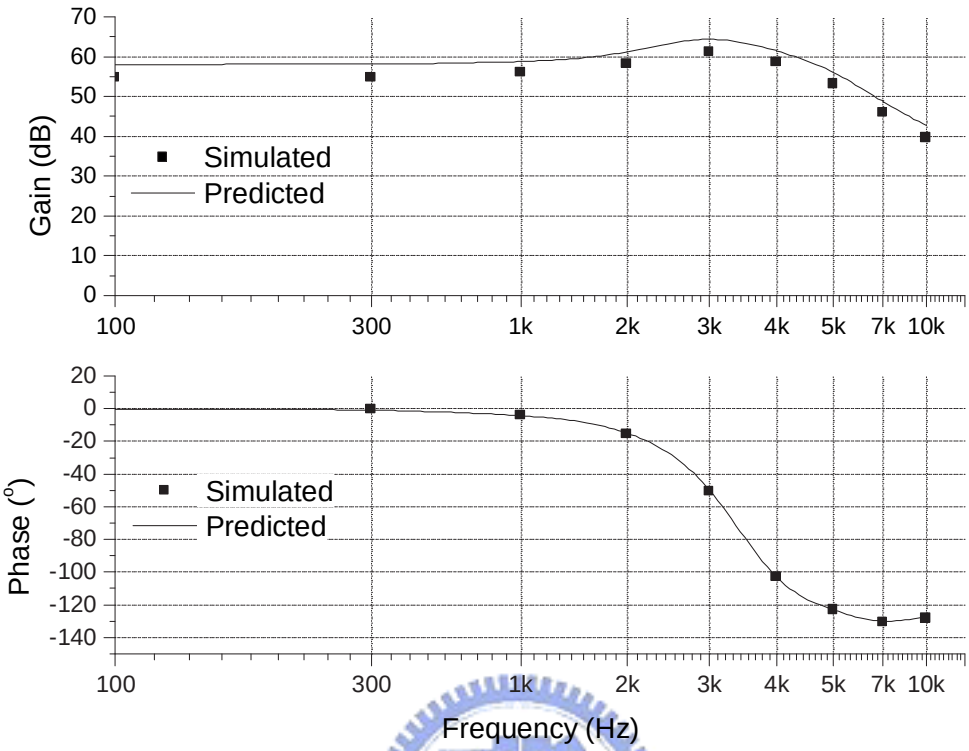


Figure 4.6: Loop gain of ripple control buck regulator.

- Loop bandwidth is too wide, which will cause instability.

- Switching noise spreads over wide spectrum.

4.3 Compensation and Circuits Implementation

From the discussions in the last section, instability of constant on-time control can be improved in two ways: 1. Create an inductor current waveform as the ramp signal instead of using output voltage. 2. Add compensation to make the unity-gain frequency of the loop gain to fall below switching frequency.

If output voltage is sensed as an average value, better regulation can be achieved by smoothing out output ripple with low ESR filter capacitor or large filter inductor. As a result, the ramp signal must be generated from inductor current. Among all inductor

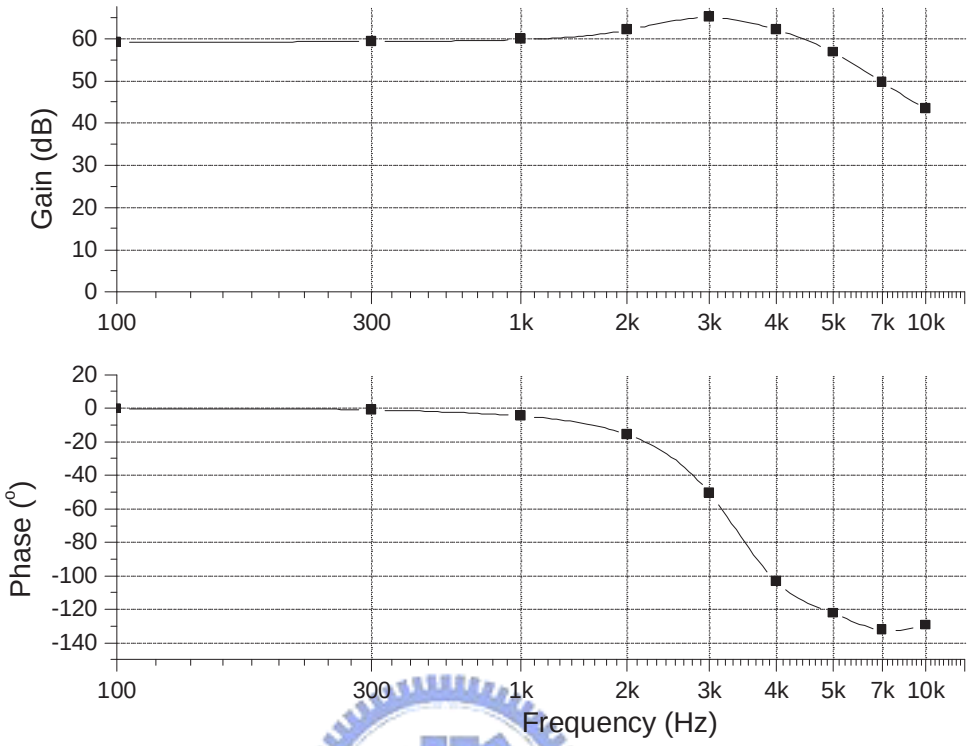


Figure 4.7: Loop gain of constant on-time control buck regulator.

current sensing techniques, integration techniques that were used in one-cycle control [67] and sensorless current-mode control [68,69] have more advantages over traditional counterparts. One-cycle control extracts voltage information by integrating LX signal. Sensorless current-mode control recreates inductor current waveform by integrating inductor voltage, $LX - V_{out}$. Since LX is a large signal and the integration acts as a low-pass filter, these techniques are less susceptible to noise. However, load regulation of one-cycle control is poor because of the lack of voltage regulation mechanism in this feed forward scheme. Moreover, one-cycle control requires additional negative supply voltage. Integration overflow will occur in sensorless current-mode because current information is constructed by integration without a resetting mechanism. These will be difficulties to implement by integrated circuits because the supply voltage is limited.

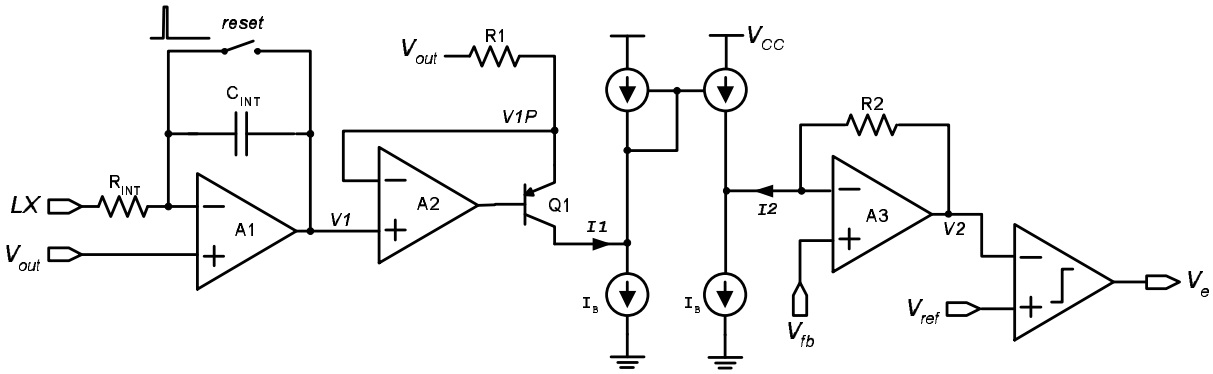
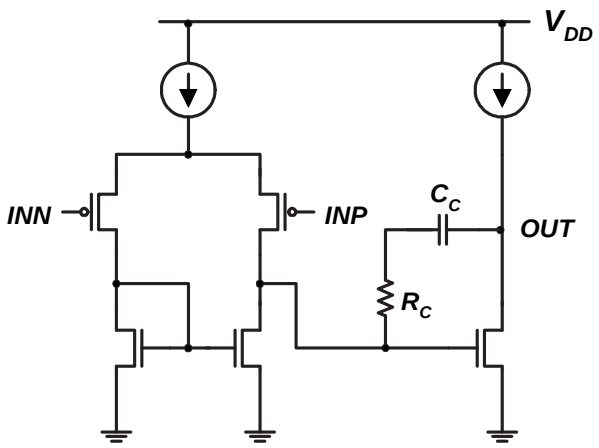


Figure 4.8: Gain compensated error amplifier.

In this section, the circuit implementation of the proposed loop gain compensated constant on-time controller is presented. Emphasis will be put on the design and loop gain analysis of the error amplifier. In the proposed design, current signal is constructed from integration of $LX - V_{out}$. Resetting mechanism and output error correcting loop are built in the error amplifier. Peripheral circuits such as timing circuits, pulse-skipping select circuit, and soft start circuit will also be addressed.

4.3.1 Error Amplifier

Figure 4.8 shows schematic of the error amplifier. Figure 4.9 shows schematic and specifications of the operational amplifier used in the error amplifier. $V1$ is negative integral of $LX - V_{out}$. At the beginning of the on state, a short pulse resets $V1$ to V_{out}. During on state, $V1$ ramps down from V_{out} with a slope proportional to $V_{out} - V_{IN}$. During off state, $V1$ ramps up with a slope proportional to V_{out}. A2 and Q1 generate a current flowing through R1 and the magnitude is $(V_{out} - V1)/R1$. This current is proportional to the AC component of V1 and can be seen as the reconstructed inductor current ripple. If the current mirrors I_B are matched, $I2$ equals to $I1$. A voltage, $V2$, contains the information



DC gain	79 dB
-3 dB freq.	500 Hz
Unity freq. (11 pF load)	4.3 MHz
Phase margin (11 pF load)	43°
Unity freq. (1 pF load)	10 MHz
Phase margin (1 pF load)	92°
Rc	30 kΩ
Cc	0.5 pF
Power consumption	100 μW

Figure 4.9: Opamp schematic and specifications.

of both inductor AC current and output voltage DC error is obtained by forcing $I2$ to flow through R2 and is described below:

$$V2 = V_{fb} - \frac{R2}{R1}(V1 - V_{out}) \tag{4.6}$$

The DC error feedback is used to achieve good voltage regulation. Loop gain compensation is done by changing $V2$'s AC ripple that is proportional to RC values. The use of lateral PNP bipolar transistor Q1 extends the output voltage range to as low as one $V_{be(sat)}$ (0.6 V). The lateral PNP transistor is available in CMOS process by exploiting parasitic device that exists in PMOS structure.

Waveforms of error amplifier are shown in Fig. 4.10. $V2$ is compared with the reference voltage. If $V2$ falls below V_{ref}, the comparator will trigger a new cycle. The positive edge of V_e triggers the one-shot timer that generates on-time pulses. Because the ripple is constructed from integration of large signal, LX, the modulation is much less sensitive

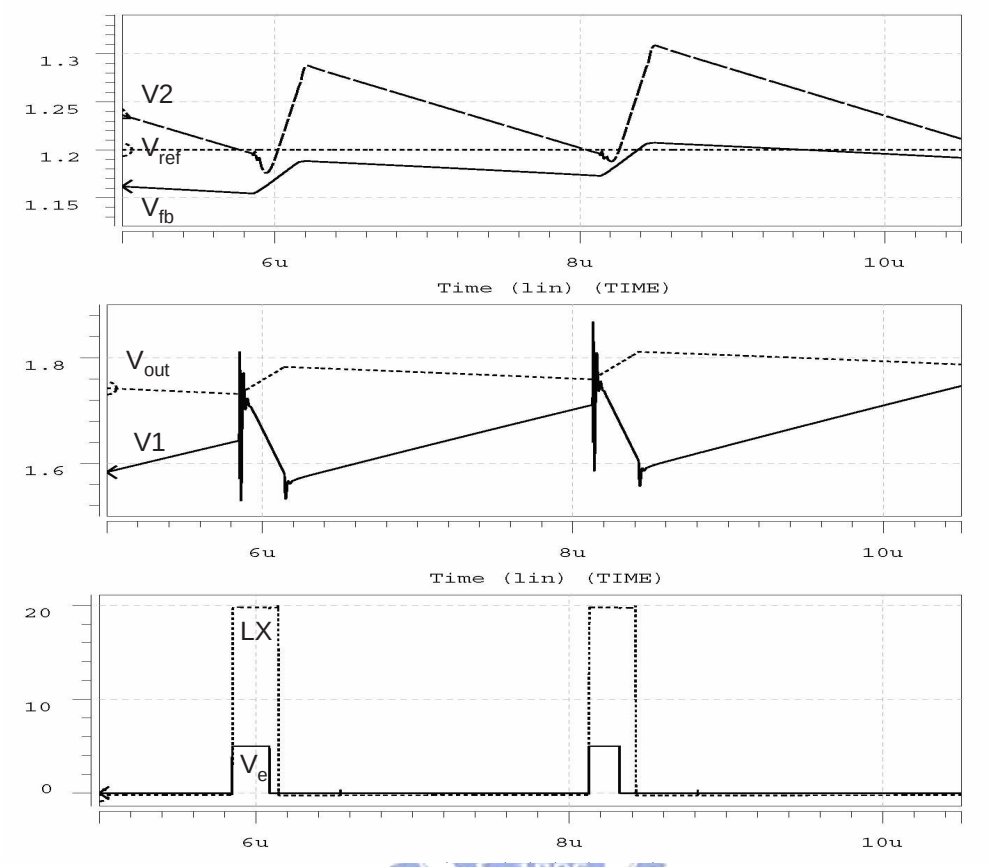


Figure 4.10: Simulated waveforms of error amplifier.

to noise as compared with traditional constant on-time control. Due to large amplitude of the input signal, strict requirements of comparator are alleviated. A comparator with lower power and slower speed can be used here. Because the output voltage is used as an average value instead of a modulating ripple, output ripple of the converter can be further reduced. Therefore, the proposed design is suitable for low voltage applications.

As discussed in Sec. 4.2.2, modulation gain is inversely proportional to ramp slope. Loop gain of constant on-time controller can be compensated by adjusting integrator's RC value in error amplifier. Proposed modulation waveforms are shown in Fig. 4.11. A disturbance ΔV on reference voltage causes a change in switching period ΔT. Because

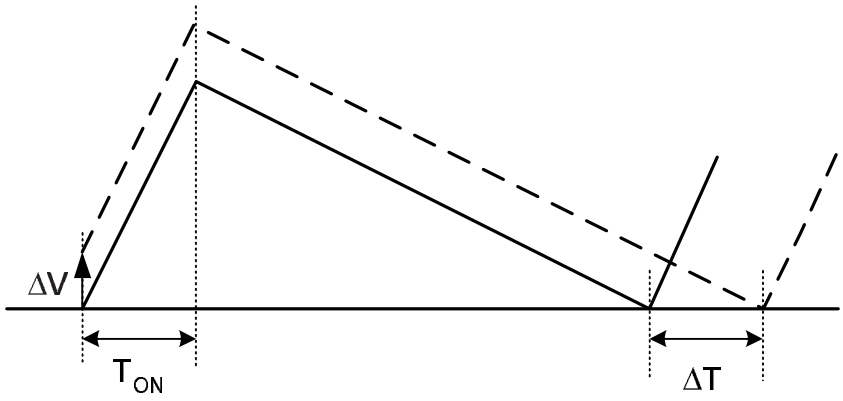


Figure 4.11: Proposed constant on-time modulation.

on time is fixed, ΔT is determined by the slope of $V2$ during off time:

$$\Delta T = \frac{\Delta V}{\frac{dV2}{dt}} = \frac{\Delta V}{\frac{R2}{R1}\frac{dV1}{dt}} = \frac{R1}{R2}\frac{R_{INT}C_{INT}}{V_{out}}\Delta V \tag{4.7}$$

In steady state, the relationship between output voltage and input voltage is:

$$V_{out} = \frac{T_{ON}}{T}V_{IN} \tag{4.8}$$

New output voltage due to ΔT is:

$$\begin{aligned} V'_{out} &= \frac{T_{ON}}{T+\Delta T}V_{IN} \\ &= \frac{T_{ON}}{T\left(1+\frac{\Delta T}{T}\right)}V_{IN} \\ &= \frac{T_{ON}}{T}V_{IN}\left(1-\frac{\Delta T}{T}\right) \\ &= V_{out}\left(1-\frac{\Delta T}{T}\right) \end{aligned} \tag{4.9}$$

By combining Eqs. 4.7 and 4.9, the change in output voltage is:

$$\Delta V_{out} = V'_{out} - V_{out} = V_{out}\frac{\Delta T}{T} = \frac{R1}{R2}\frac{R_{INT}C_{INT}}{T}\Delta V$$

Therefore, loop gain is the product of $\Delta V_{out}/\Delta V$, feedback network gain V_{ref}/V_{out}, and

Table 4.1: DC loop gain of buck regulator using proposed error amplifier.

V_{IN}	V_{out}	$f_{SW} = 1/T$	L	$R1/R2$	$R_{INT}C_{INT}$	Loop Gain	Predicted
20 V	1.8 V	300 kHz	2.2 μH	2	24 μs	10.2	9.6
8 V	1.8 V	300 kHz	2.2 μH	2	24 μs	10.1	9.6
8 V	2.5 V	300 kHz	2.2 μH	2	24 μs	7.27	6.91
20 V	1.8 V	300 kHz	4.4 μH	2	24 μs	11.1	9.6
20 V	1.8 V	600 kHz	2.2 μH	2	24 μs	20.2	19.2
20 V	1.8 V	300 kHz	2.2 μH	2	48 μs	20.0	19.2

LC filter transfer function $H(s)$:

$$T(s) = \frac{V_{ref}}{V_{out}} \frac{R1}{R2} \frac{R_{INT}C_{INT}}{T} H(s) \tag{4.10}$$

where V_{ref} is bandgap reference voltage 1.2 V. According to Eq. 4.10, Table 4.1 lists simulated DC loop gains under different conditions. Simulation reveals the same relationship as was predicted. DC loop gain is independent of ESR, input voltage, and inductor value. Therefore, output ripple can be reduced by choosing larger inductor and lower ESR values, which may cause instability in traditional constant on-time control. Figure 4.12 plots simulated loop gain versus the results predicted from Eq. 4.10 with parameters listed in the first row of Table 4.1 and a 940 μF filter capacitor with 15 mΩ ESR.

DC gain of the compensated regulator is about 20 dB. In common voltage-mode PWM converters, DC gains are usually set at 40–60 dB as a rule of thumb. High loop gain reduces load regulation error but decreases phase margin. However, in free-running control, load regulation is not directly related to DC gain. Figure 4.13 illustrates relationship of duty ratio and load current in constant on-time control. Refer to Fig. 3.2 , an increase in load current is effectively a decrease in input voltage, which is described below:

$$\Delta V_{IN} = -\Delta I_{load} \times R_{ON} \tag{4.11}$$

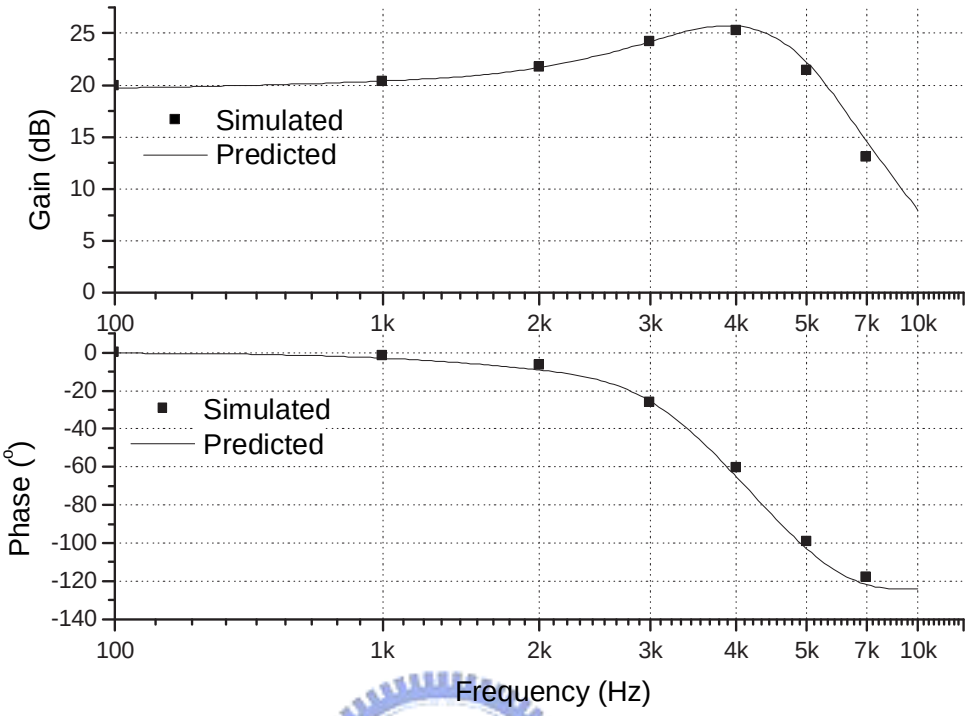


Figure 4.12: Loop gain of proposed constant on-time buck regulator.

Because rising slope of output voltage is directly proportional to $V_{IN} - V_{out}$, the rising slope of output voltage with higher load current, V'_{out}, is smaller. Because T_{ON} is fixed, V'_{out} increases less than V_{out} during on time. During off time, falling slopes of both V'_{out} and V_{out} are the same. As a result, period becomes shorter and duty ratio becomes larger with increasing load current. The increased duty ratio compensates for the increased loading. Therefore, load regulation is good in proposed control in despite of its low DC gain.

4.3.2 Timing Circuits

In an ideal buck converter without parasitic resistance in the output current path, on time is inversely proportional to V_{IN} and directly proportional to V_{out}. Therefore, if the on time, T_{ON}, of the constant on-time control is fixed, the switching frequency will vary with V_{IN} and V_{out}.

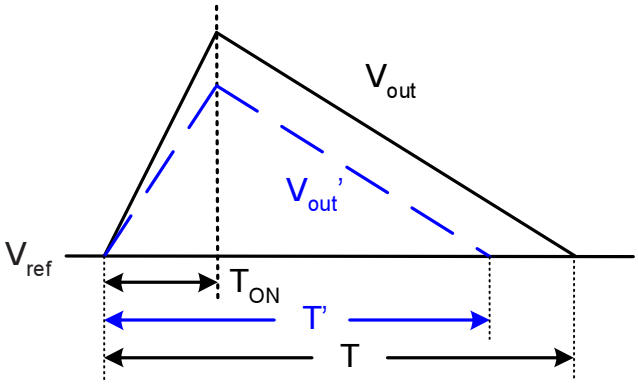


Figure 4.13: Duty ratio at different load currents of proposed constant on-time regulator.

On the other hand, if T_{ON} is made to be inversely proportional to V_{IN} and proportional to V_{out}, it can be described below:

$$T_{ON} = K_{ON}\frac{V_{out}}{V_{IN}} \tag{4.12}$$

where K_{ON} is a constant. The system operates at an approximately constant switching frequency, f_{SW}, without a clock source.

$$\begin{aligned} f_{SW} &= \frac{D}{T_{ON}} \\ &= \frac{V_{out} + I_L R_S}{T_{ON} V_{IN}} \\ &= \frac{V_{out} + I_L R_S}{K_{ON} V_{out}} \\ &\cong \frac{1}{K_{ON}} \end{aligned} \tag{4.13}$$

where R_S is the sum of the parasitic resistance in the inductor current path. Equation. 4.13 is only valid in continuous conduction mode (CCM). Frequency will be lower in discontinuous conduction mode (DCM) and is strongly dependent on load current.

A minimum off time is required to constant on-time controllers during start up and load transient. It prohibits the switching signal from turning on immediately after the

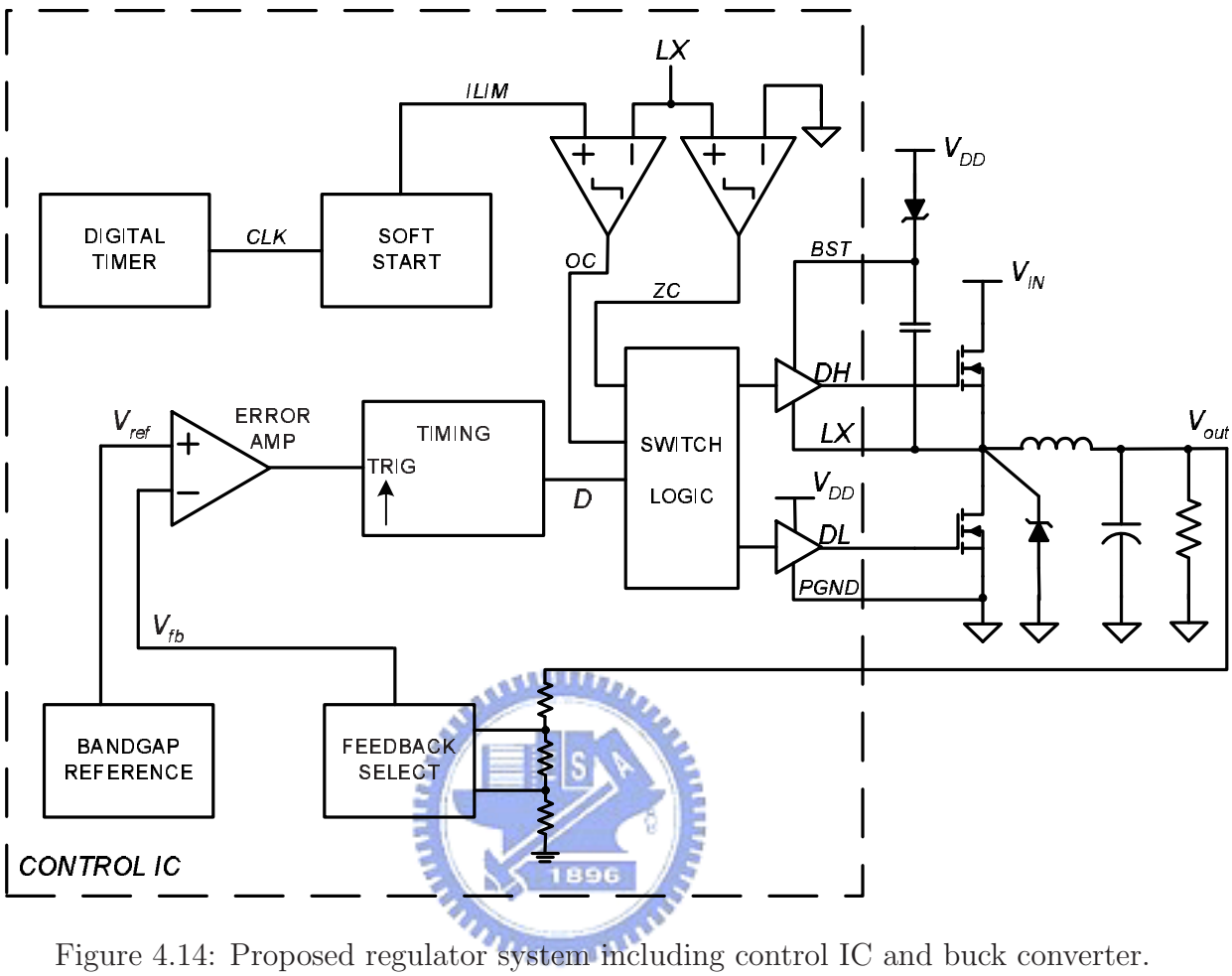


Figure 4.14: Proposed regulator system including control IC and buck converter.

T_{ON} has expired. Therefore, it prevents output voltage from high frequency oscillation.

4.3.3 Regulator System

Synchronous topology uses low on-resistance MOSFET as the low-side switch to reduce conduction loss during off time. However, at light loads, there is a possibility of reverse inductor current when using synchronous topology. Inductor current reversal can be prevented by using skip mode. An external pin enables skip mode where the low-side MOSFET turns off when zero crossing is detected at LX. Therefore, the regulator enters pulse-skipping mode automatically at light loads. Pulse skipping provides high efficiency

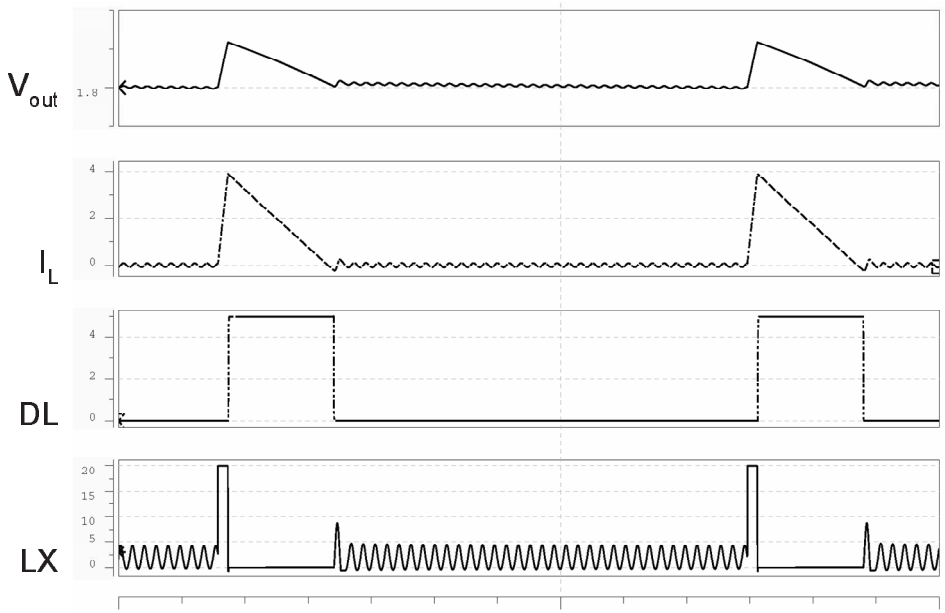


Figure 4.15: Waveforms in skip mode.

operation at light loads but also causes high frequency oscillation at LX and asynchronous operation at output. Figure 4.15 shows waveforms in skip mode. The low-side MOSFET is turned off because the inductor current has been discharged to zero. Energy stored in filter inductor and parasitic capacitance at LX causes oscillation. Trade-offs of light load efficiency and noise are made by varying the inductor value [1].

The controller uses low-side MOSFET as the current sensing element for over-current protection. As shown in Fig. 4.14, the over-current protection function is implemented by comparing LX signal with internal generated over-current threshold, $ILIM$. This kind of current limiting is called valley current limit. If the inductor current reaches the over current threshold, the low-side MOSFET will be forced to turn on and the high-side MOSFET will be forced to turn off. New cycle will not start until the over current signal is released. The peak inductor current would be the current limit threshold plus the peak

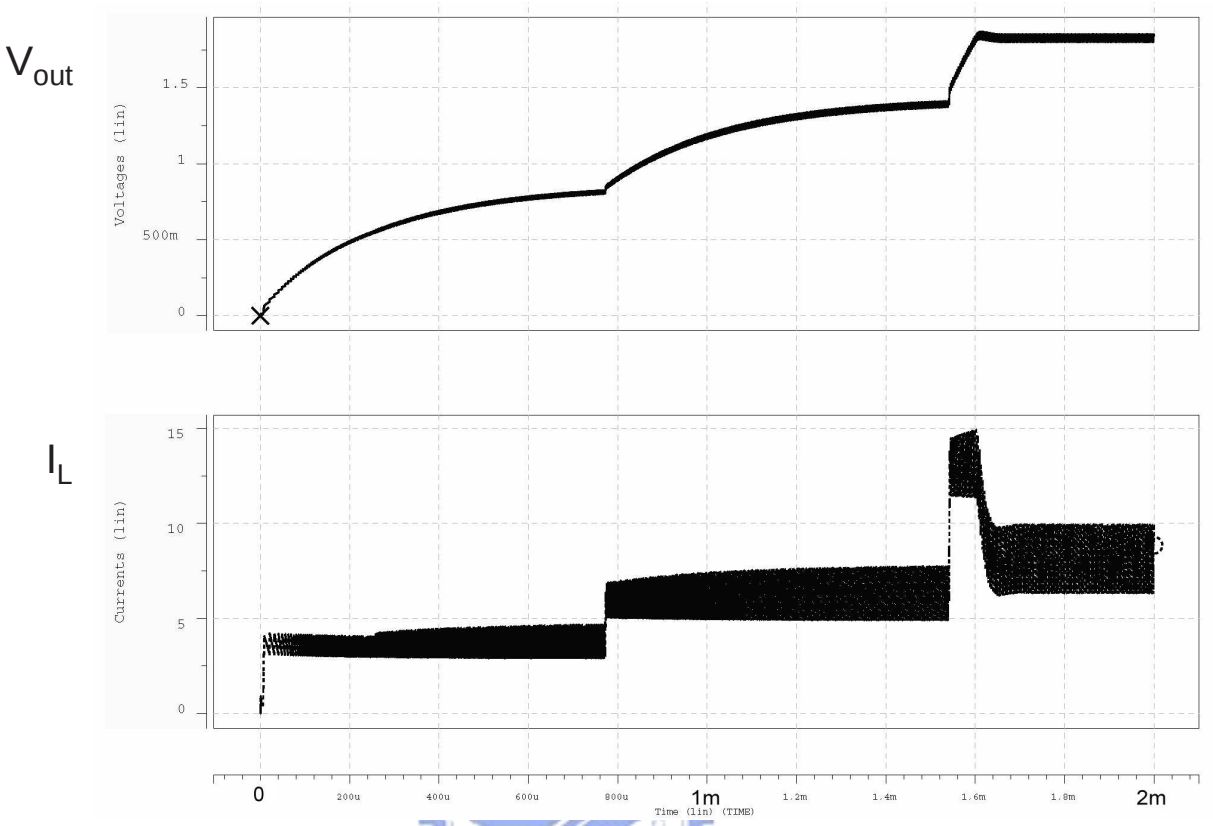


Figure 4.16: Simulation result of digital soft-start operation.

ripple current.

After power-on reset procedure, a soft start counter is enabled to provide step current limiting over a predetermined time. The progressive current threshold, $ILIM$, occurs in three steps, which can be observed in Fig. 4.16. The soft-start operation limits the slew rate of the output voltage.

4.4 Simulation and Experiment Results

The control chip was fabricated in a 1 μm 40 V CMOS process. The chip photomicrograph is shown Fig. 4.17. The chip area including pads is 5.2 mm^2, effective area is 4.6 mm^2. Experiment setup is illustrated in Fig. 4.14. The parameters used in simulation are listed

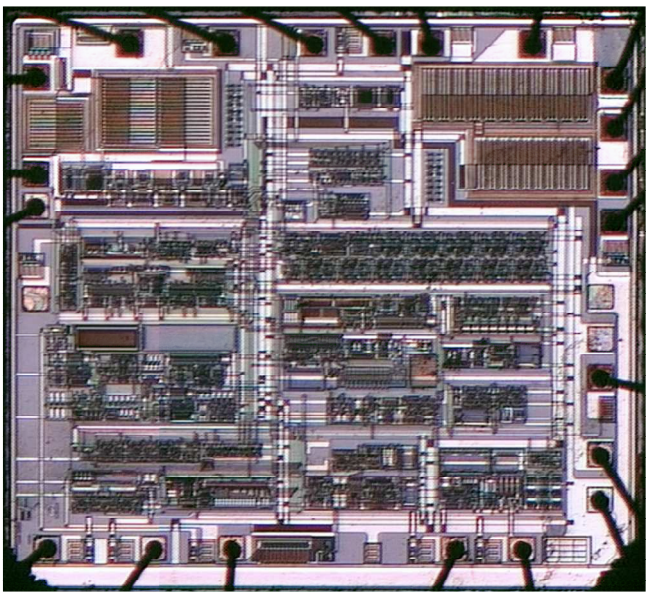


Figure 4.17: Chip photomicrograph of constant on-time controller.

Table 4.2: Parameters.

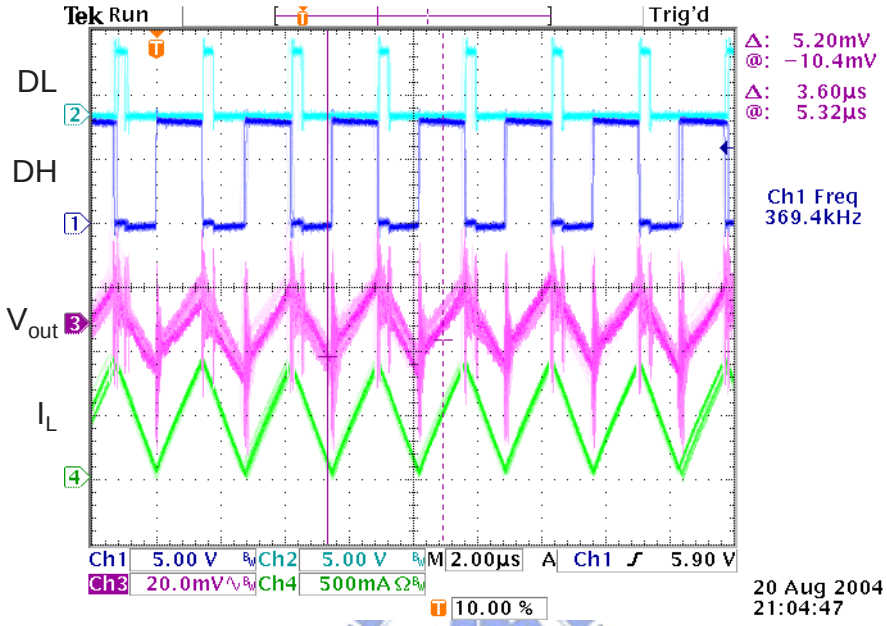
Target output voltage, V_{out}	1.8 V
Input voltage, V_{IN}	20 V
Filter inductor, L	1.5 μH
Filter capacitor, C	940 μF
DCR of inductor, r_L	2 mΩ
ESR of capacitor, r_C	15 mΩ
On-state resistance of MOSFET, R_{ON}	12 mΩ
Error amplifier resistor ratio, $R1/R2$	2
Error amplifier integrator RC, $R_{INT}C_{INT}$	24 μs
Target switching frequency, f_{SW}	300 kHz
Chip supply voltage, V_{CC}	5 V

in Table 4.2. Some values used in experiment are different and will be noted. The target input range of the regulator is from 8 V to 28 V and the regulated output range is from 1.2 V to 3.3 V.

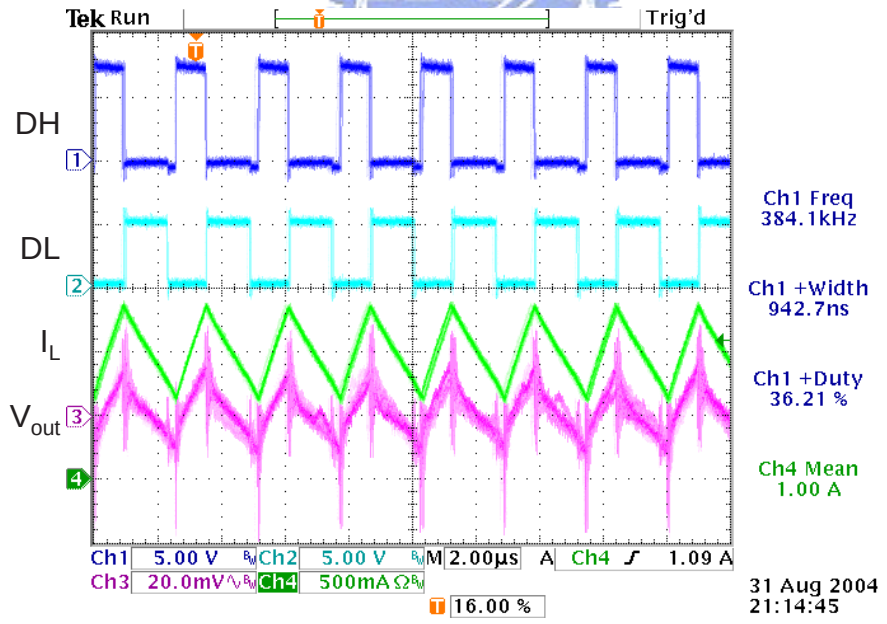
4.4.1 Steady State

In steady state, fabricated controller operated normally with inductor currents below 1.2 A. Measured steady state waveforms at 450 mA and 1 A with V_{IN} = 5 V and V_{out} = 1.71 V are showed in Fig 4.18. Target switching frequency is 300 kHz and measured frequency is 370 kHz. In Fig 4.18(a), DL is not exactly in inverse phase of DH. DL turns off earlier than normal because zero crossing current limit is too high. As described in Sec. 4.3.3, the low-side MOSFET will be turned off to prevent reverse inductor current if zero crossing is detected. Measured zero crossing current limit shown in Fig. 4.19 is about 650 mA. Incorrect current limit might be caused by inaccurate inductor current sensing. This might be also the cause of abnormal operations at high load currents. As long as the loading exceeded 1.2 A, the output voltage dropped. Figure 4.20 shows the relationship of stability versus load current from simulation. Since effect of load variation (0 and 8A) on converter loop gain is not significant, abnormal operations at high loading might be caused by other circuits such as over-current protection circuits.

Figure 4.21 shows measured efficiency of the regulator versus load current in skip mode. An efficiency of over 86 % is achieved over a load range from 10 mA to 3 A with 5 V input voltage and 2.476 V output voltage. The discontinuity of efficiency around 700 mA indicates the transition point of continuous conduction mode and discontinuous conduction mode. In skip mode, the low-side MOSFET switch will be forced off when a zero crossing of inductor current is detected to prevent current reversal. Therefore, the transition point is located at about half of the inductor current ripple. However, it is raised due to inaccurate current sense.



(a) 450 mA.



(b) 1 A.

Figure 4.18: Steady state waveforms at different load currents with V_{IN} = 5 V and V_{out} = 1.71 V.

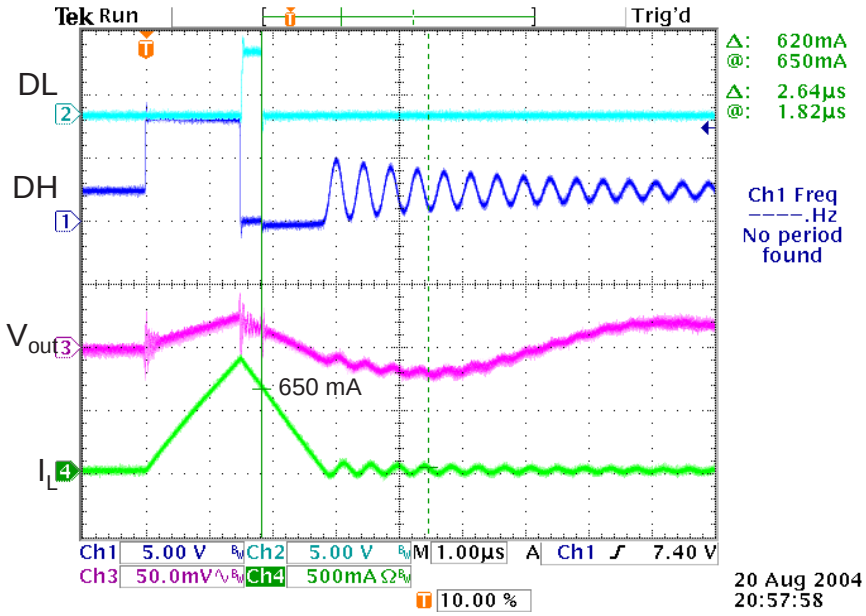


Figure 4.19: Zero crossing point of inductor current at 5 mA load current.

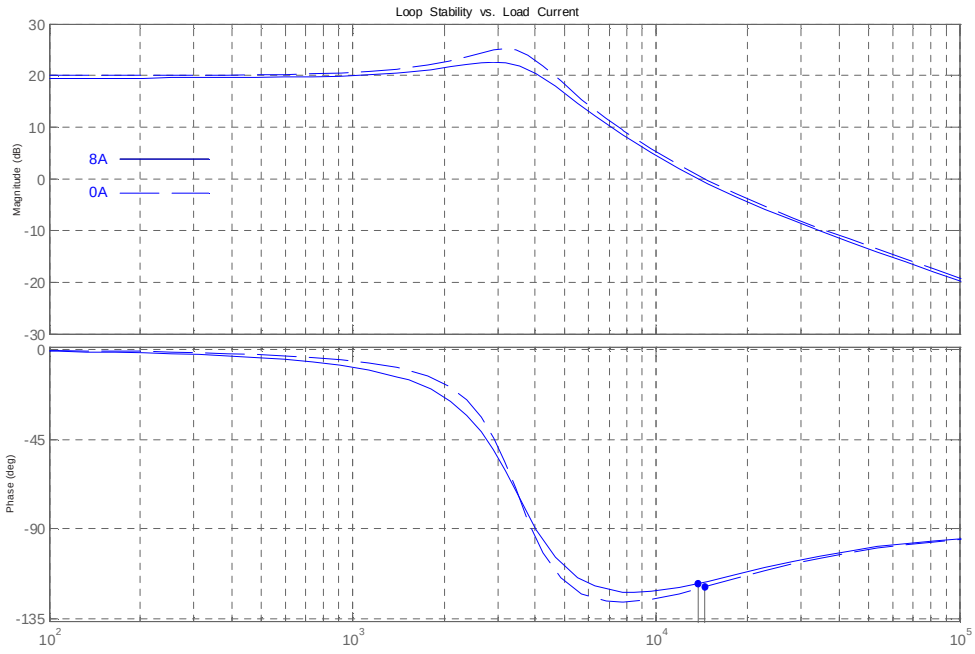


Figure 4.20: Converter loop gain versus loading.

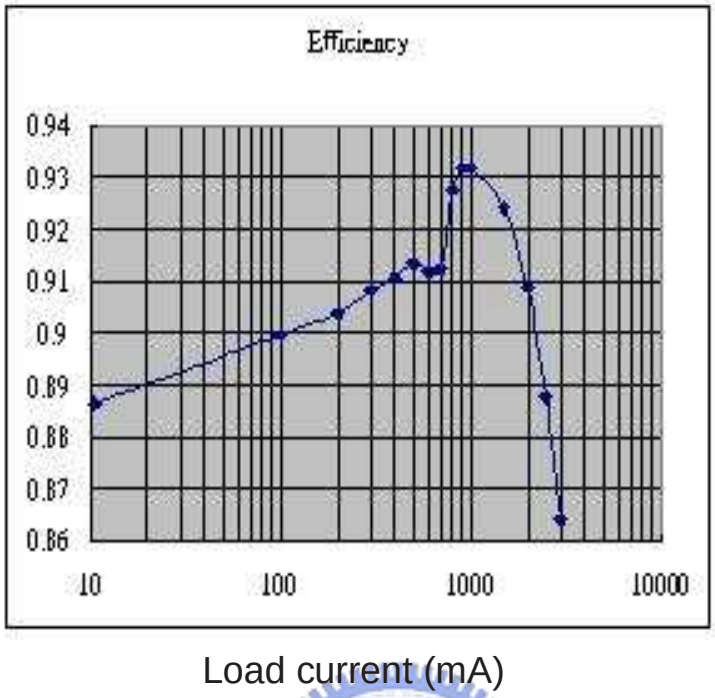
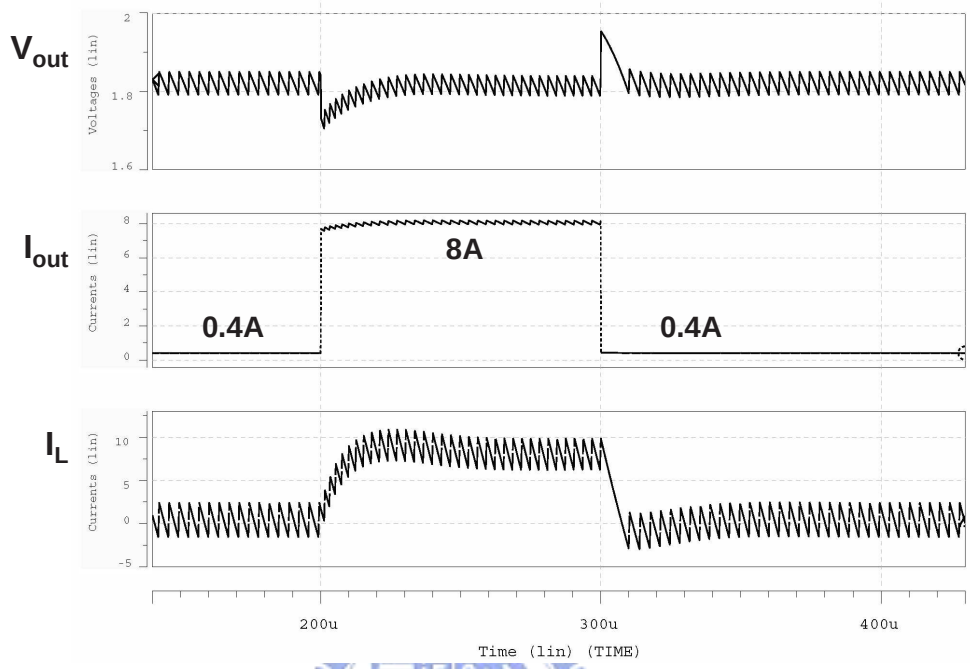


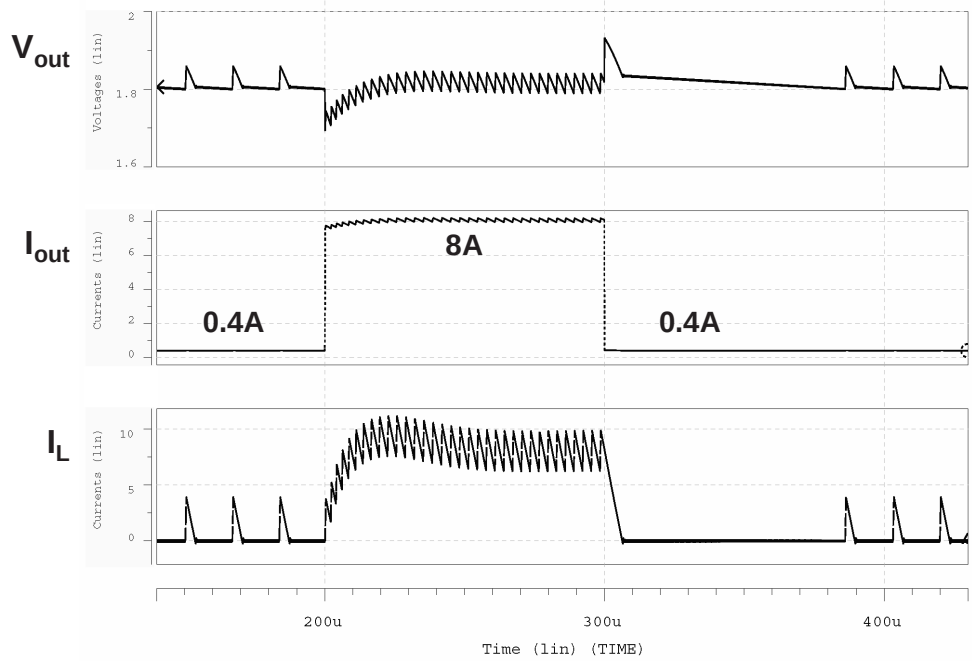
Figure 4.21: Measured efficiency versus load current with $V_{IN} = 5$ V and $V_{out} = 2.476$ V.

4.4.2 Load Transient Response

Simulated load transient responses are shown in Fig. 4.22. Load current was switched between 0.4 A and 8 A. The regulator can operate in either skip mode or forced-PWM mode. In forced-PWM mode, low-side switch remains turned on even though the inductor current has reversed. Thus, the switching frequency is almost fixed regardless of the load current level. Forced PWM is most useful for eliminating audio frequency noise at the cost of efficiency. In skip mode shown in Fig. 4.22(b), lower bound of inductor current is bound to zero. Output voltage will not be charged by the T_{ON} pulse unless it falls below reference. Pulse-skipping mode achieves high efficiency at light loads. However, the switching frequency drops dramatically with the load current. The load regulation is 0.032 %/A that is superior to conventional current-mode and voltage-mode PWM control.



(a) Forced-PWM mode.



(b) Skip mode.

Figure 4.22: Simulated load transient response.

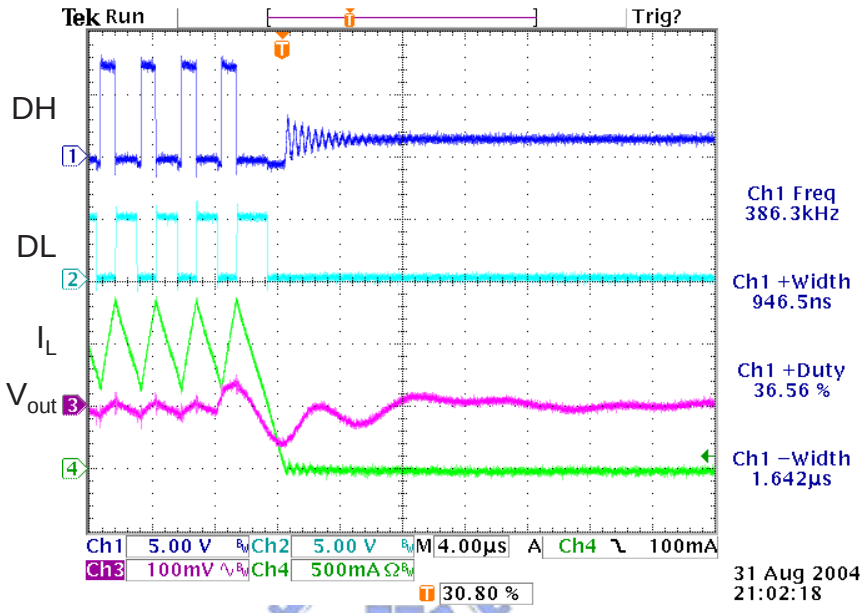
Measured load transient responses in skip mode are shown in Fig. 4.23. Load current was switched between 5 mA and 1 A with $V_{IN} = 5$ V and $V_{out} = 1.71$ V. Response time is close to the simulation result.

4.4.3 Line Transient Response

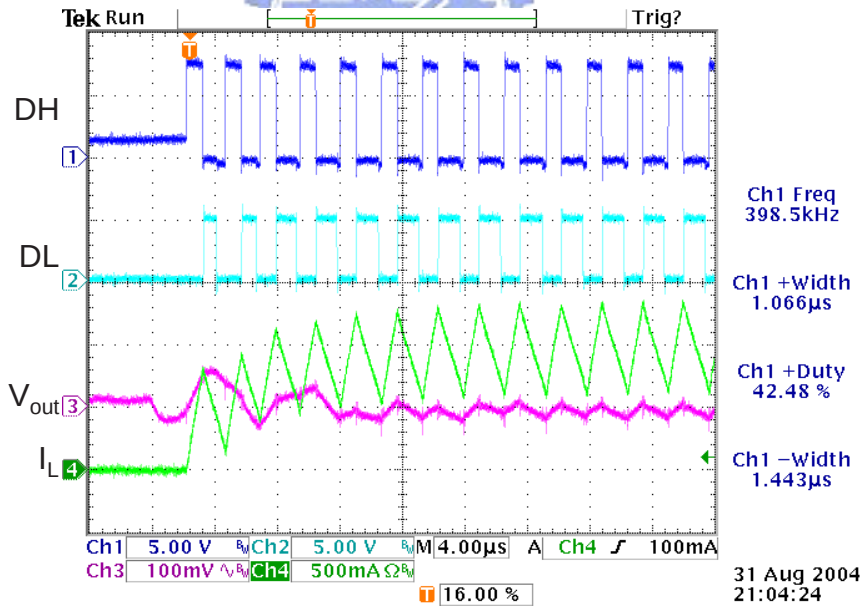
From the line regulation simulation results shown in Fig. 4.24, fast line transient response is exhibited. Line voltage was switched between 20 V and 8 V which are adaptor voltage and battery voltage respectively. Similar to other free-running controllers, the change in line is immediately responded to the duty ratio. Excellent line regulation is expected for the proposed regulator. Line regulation is 0.034 %/V from simulation. The input voltage was limited to 5 V due to voltage withstanding problem of the chip. Line regulation was not measured.

4.5 Summary

Table 4.3 summarizes performance of this work and compares with other commonly used control schemes. Current mode is less power efficient because of the current sensing resistor. Because of the integration techniques that were used in one-cycle control and sensorless current-mode control, they are superior in efficiency and noise susceptibility to traditional current-mode control. However, load regulation of one-cycle control is poor because of the lack of voltage regulation mechanism. Without the limit of clock frequency, free-running types and proposed design are faster than constant frequency types. In addition to better line and load regulation, proposed design exhibits improved noise susceptibility and EMI. Because output voltage is sensed as an average value, small



(a) 1 A to 5 mA



(b) 5 mA to 1 A

Figure 4.23: Measured load transient response in skip mode with $V_{IN} = 5$ V and $V_{out} = 1.71$ V.

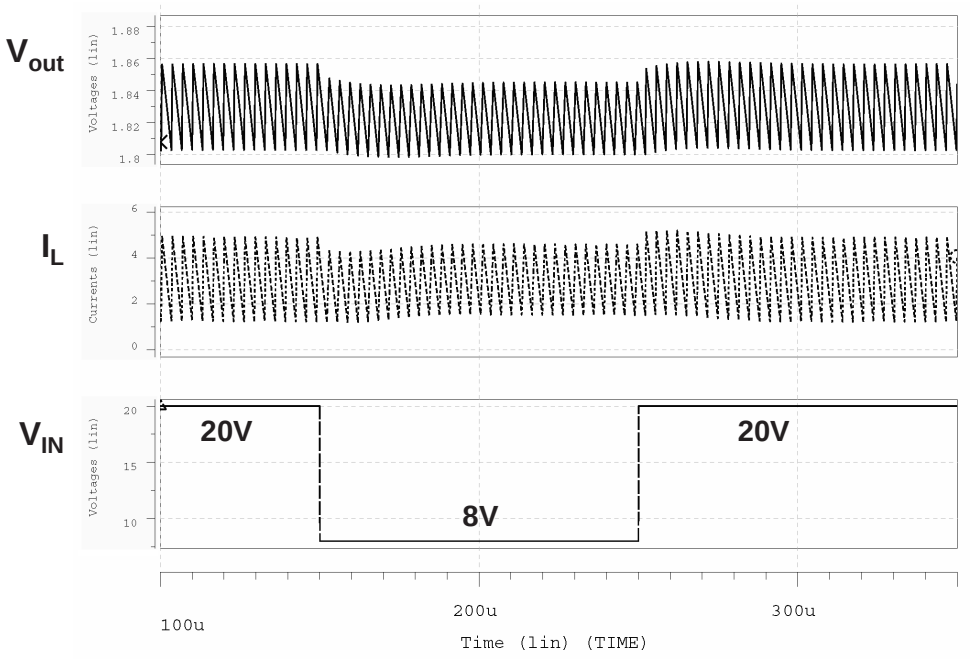


Figure 4.24: Simulation result of line transient.

output ripple of proposed design is suitable for low voltage applications.

Table 4.3: Performance summary and comparisons with other control schemes.

	This work	Free running	Current mode/Sensorless	Voltage mode	One-cycle control
Efficiency	86.5 %∼93.2 % (High)	High	Fair/High	High	High
Line transient response	Fast	Fast	Fast	Slow	Fast
Line regulation (from 8 V to 20 V)	0.034 %/V (Excellent)	Excellent	Fair	Good	Excellent
Load transient response	Fast	Fast	Fast	Slow	N/A
Load regulation (from 0.4 A to 8 A)	0.032 %/A (Excellent)	Excellent	Fair	Good	Poor
Noise immunity	Good	Poor	Poor/Good	Good	Good
EMI	Low	High	Low	Low	Low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Chapter 5

Frequency Synchronized Ripple Controllers

5.1 Introduction

The ripple control is the simplest among all switching regulators. The intrinsic advantage of the ripple regulator is the small number of parts, resulting in high reliability and low cost. Main advantages of the ripple regulator, like other variable frequency regulators, are fast transient response and wide range of output/input voltages. However, the switching frequency depends on the operating conditions and power filter. Quasi-fixed frequency control, which is introduced in Chap. 4, was brought up based on the idea of controlling the on time that is directly proportional to the output voltage and inversely proportional to the input voltage, thus an approximately fixed switching frequency is achieved. However, the switching frequency still varies with second-order effects in the switching regulator. In this chapter, methods and circuits are proposed to implement frequency synchronized ripple control regulators. Both advantages of fixed and non-fixed frequency regulators are therefore obtained.

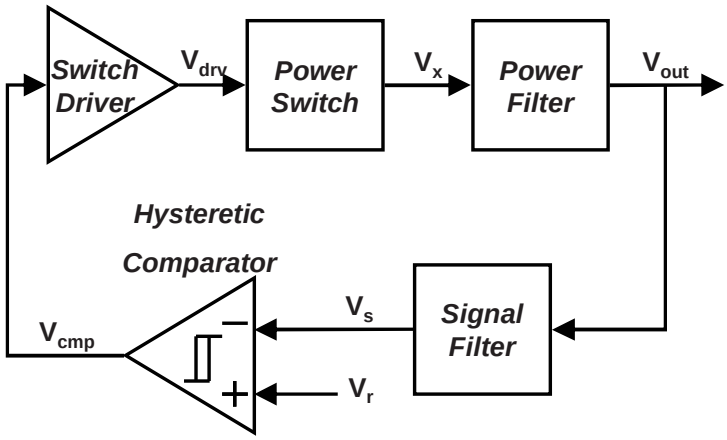


Figure 5.1: Ripple control regulator block diagram.

5.2 Voltage-Mode Ripple Control Buck Regulator with Fixed Output Frequency

Ripple control is well known for simple structure, wide conversion range, and fast response. However, switching frequency of the conventional ripple control regulator is a function of circuit delay, ESR of the output capacitors, and many other parameters. Varying switching frequency can cause EMI problem in a system. In this section, we present a frequency synchronization technique for the voltage-mode ripple control buck regulator.

5.2.1 Voltage-Mode Ripple Control Buck Regulators

Figure 5.1 shows the ripple control regulator block diagram. It uses a comparator-based voltage control loop. The sensed voltage V_s is fed to a comparator, which drives the power switch on and off to regulate the output voltage V_{out}. Hysteresis is usually added to limit switching frequency, but is not necessary. System internal delay caused by the comparator and the switch driver also limits switching frequency. The control loop keeps V_{out} within a small region around the desired voltage. Once there is a voltage drop caused

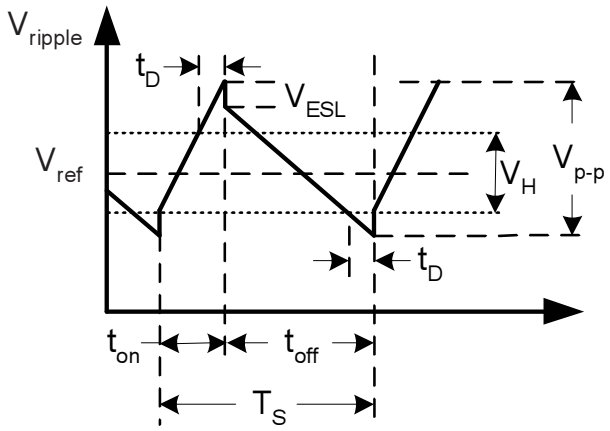


Figure 5.2: Output ripple of the voltage-mode ripple control regulator.

by a load transient, V_{out} recovers as quickly as the power filter allows. In addition to its fast transient response, this control scheme provides a simple and reliable design.

In the buck converter, three elements of the output capacitor contribute to output voltage ripple:

$$V_{ripple} = V_C + V_{ESR} + V_{ESL} \tag{5.1}$$

where V_C is capacitance voltage, V_{ESR} and V_{ESL} are voltages induced by ESR and ESL of the capacitor respectively. The switching frequency of the ripple control regulator can be calculated from the formula derived in [56]:

$$f_{SW} = \frac{V_{out}}{V_{IN}} \times \frac{(V_{IN} - V_{out}) \times (r_C - t_D/C)}{V_{IN} \times r_C \times t_D + V_H \times L - l_C \times V_{IN}} \tag{5.2}$$

where r_C is ESR of the output capacitor C, t_D is internal delay, V_H is the comparator hysteresis window, L is the inductor of the buck filter, l_C is ESL of the buck filter capacitor. The output frequency is significantly influenced by these factors. Figure 5.3(a) and (b) estimate the switching frequency variations against V_{IN} with different V_{out} and r_C. Parameters used are the followings: C=940 μF, V_H=20 mV, L=2.2 μH, t_D=200 ns, l_C=1 nH.

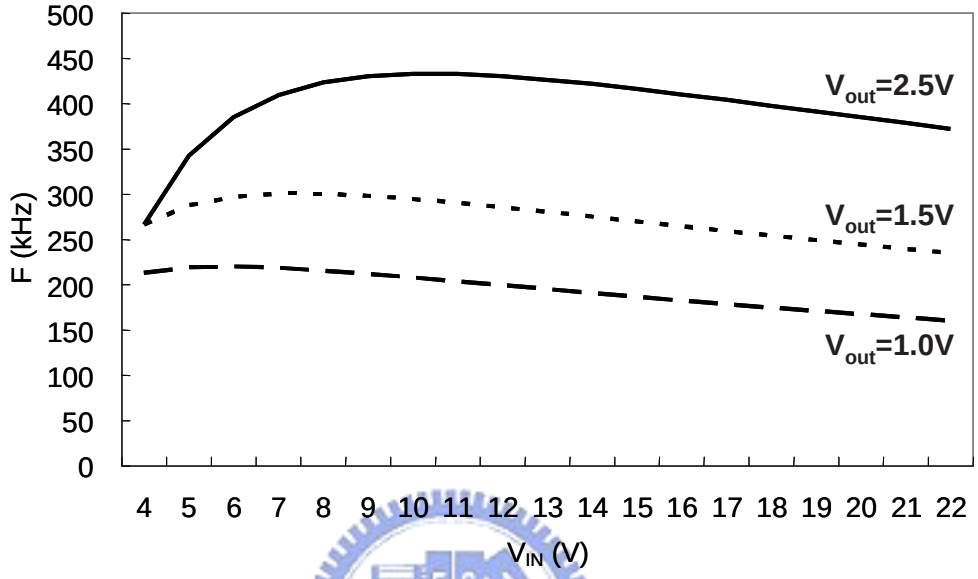
For a certain application, desired switching frequency can be obtained by tuning these parameters. However, the ESR of a capacitor changes with material, temperature, and age. Practical ESR variations can easily lead to a frequency variation by one to three times, which makes EMI shielding almost impossible. It would be desirable to automatically synchronize switching frequency of a ripple control regulator.

5.2.2 Circuit Design for Fixed Switching Frequency

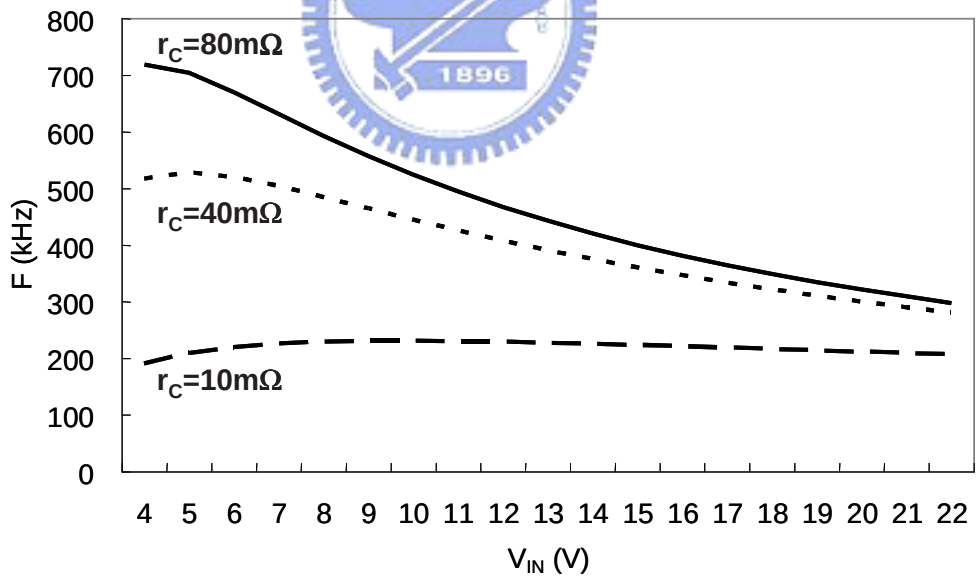
From Eq. (5.2), it is observed that the switching frequency is a function of internal delay which resides within the comparator and the switch driver. If total delay of the controller is controllable, the switching frequency is controllable as well. Refer to Eq. (5.2), hysteresis window, V_H, and filter inductance, L, limit the highest attainable switching frequency. Below the limit, it is possible to fix the frequency by inserting appropriate system delay.

To control the switching frequency precisely, one straightforward approach is to calculate the total delay from Eq. (5.2) and subtract it to the internal delay. However, the drift of the switch driver delay and the comparator delay with supply voltage and temperature make this method impractical. The inserted delay value must be determined automatically by some mechanism.

Figure 5.4 shows the proposed control loop derived from the ripple control regulator. A comparator with hysteresis is used to avoid false crossing detections caused by the noise. Different from conventional ripple controllers, a delay element is placed after the comparator. A negative feedback loop that uses a phase-frequency detector (PFD) is also added to determine the accurate delay value. The delay time caused by the delay element is directly proportional to V_{TH}. The PFD is widely used in phase-locked loop (PLL)



(a) Frequency vs. input voltage with different output voltages. (r_C=15 mΩ)



(b) Frequency vs. input voltage with different ESRs. (V_{out}=1.5 V).

Figure 5.3: Frequency variations of the ripple control regulator.

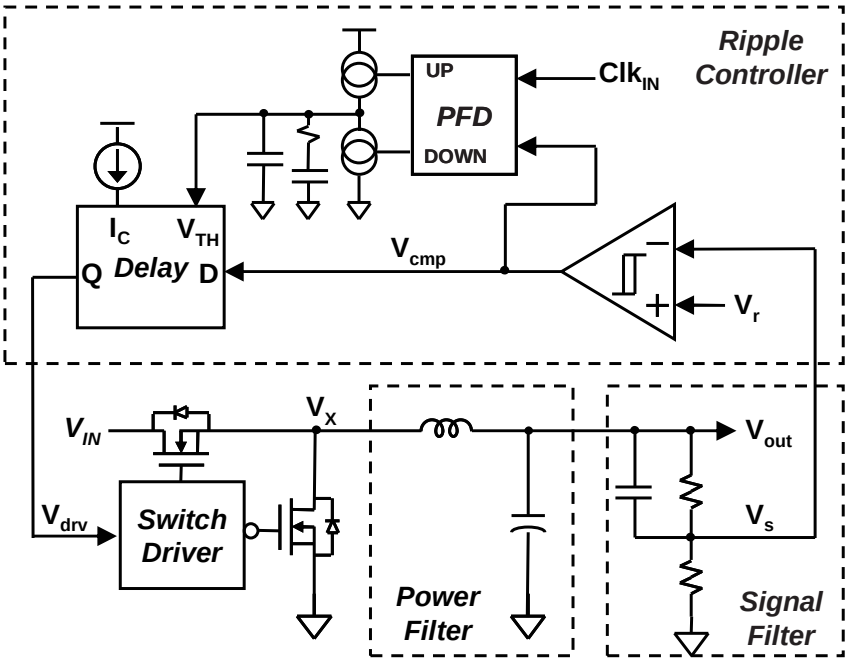


Figure 5.4: Proposed ripple control buck regulator.

circuits. It detects the phase/frequency differences between the clock input CLK_{IN} and the switching signal. If the switching signal runs slower than CLK_{IN}, the PFD will control the low-side charge pump to discharge V_{TH}. Because delay is directly proportional to V_{TH}, decreasing V_{TH} is effectively increasing the frequency. If the switching signal is faster, it will pump V_{TH} to increase the delay. With this mechanism, the switching frequency will be exactly the same as the clock input.

In the following paragraphs, we proceed to detail circuit design of each block in Fig. 5.4. In order to obtain accurate system characteristics, most of the circuits are constructed by transistors.

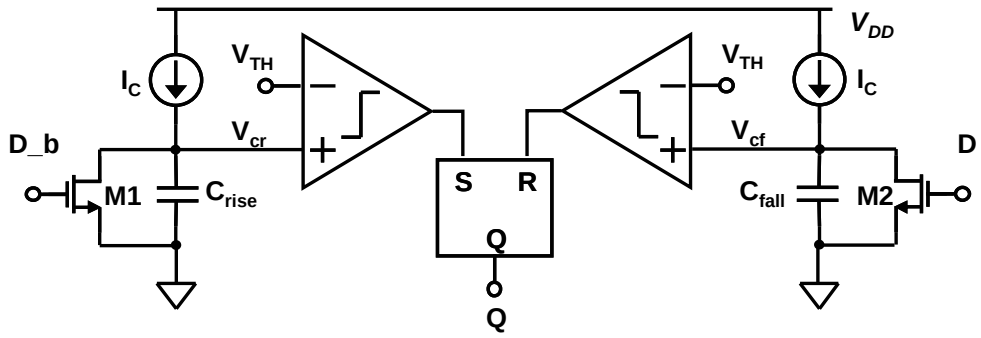


Figure 5.5: Delay element.

Delay Element

A CMOS delay element is shown in Fig. 5.5. The delay value can be varied over a wide range by changing the control signals I_C and V_{TH}. The left side of the Fig. 5.5 is triggered by the rising edge of the input signal D and the right side is by the falling edge. Once the rising edge of D is detected, I_C starts to charge C_{rise}. When the ramp voltage V_{cr} exceeds the threshold voltage V_{TH}, the S-R flip-flop sets the output Q to logic high. Operations of the falling edge can be understood similarly. A delayed waveform of D is generated with identical duty ratio. The delay time, t_D, is determined by I_C, C, and V_{TH}:

$$t_D = \frac{C \times V_{TH}}{I_C} \tag{5.3}$$

Assume $I_C = 10$ μA ,$C = 10$ pF, and $V_{TH} = 1$ V, then we have $t_D = 1\mu s$. Reasonable delay time to keep a fix-frequency operation at 150 kHz–600 kHz is from 100 ns to 1 μs.

Large voltage swings are expected in V_{cr} and V_{cf}. In order to suppress the effect of channel-length modulation, cascode current sources are used. Detail circuits will be shown with the charge pump. In order to reduce charge sharing effect at node V_{cr} and V_{cf}, the current is steered to the switch during the reset mode. Small-size NMOS transistors

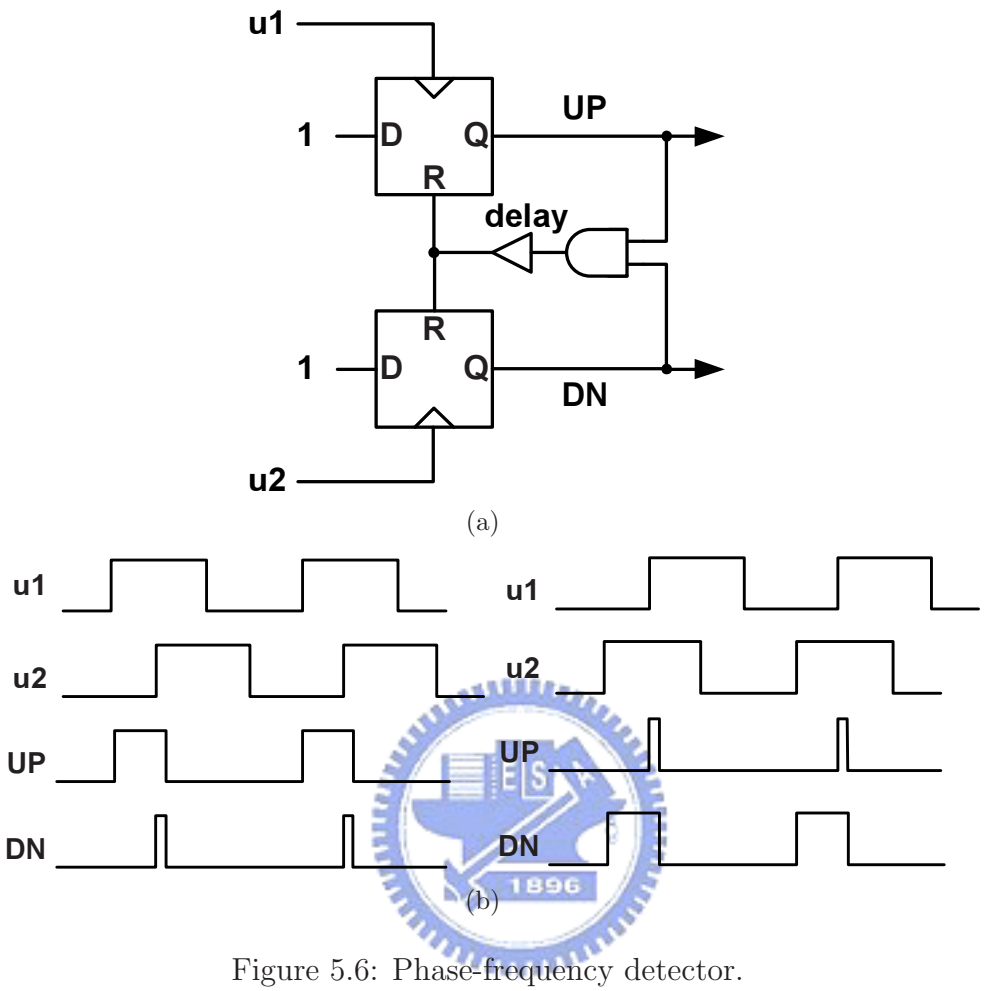


Figure 5.6: Phase-frequency detector.

are recommended to implement the switches. Although smaller switches exhibit larger resistance, only capacitor discharging time is affected. It is not critical in this design.

The Charge-Pump Phase-Frequency Detector

Figure 5.6 shows the phase-frequency detector (PFD) used in the controller. The PFD comprises two D flip-flops and some resetting logic gates. The PFD is triggered by positive edges, the duty ratios of $u1$ and $u2$ are irrelevant. Thus, it is suitable for comparing PWM signals. An early arriving positive edge of $u1$ will set UP to high. On the other hand, an early arriving positive edge of $u2$ will set DN to high. Output will reset after a positive

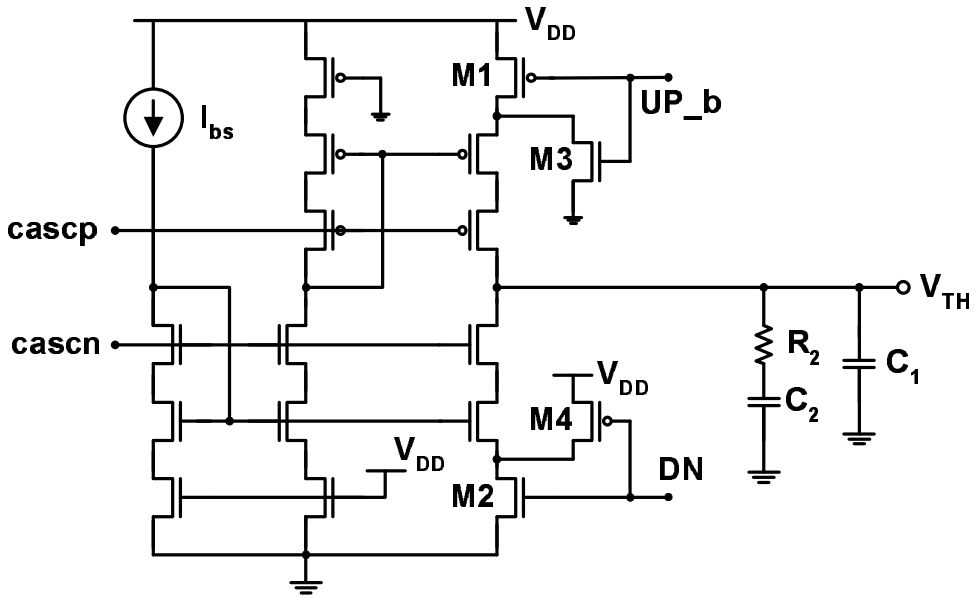
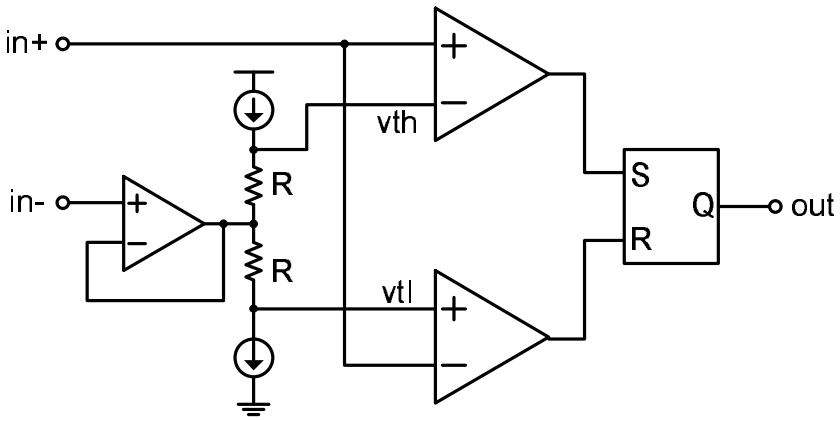


Figure 5.7: Charge pump and loop filter.

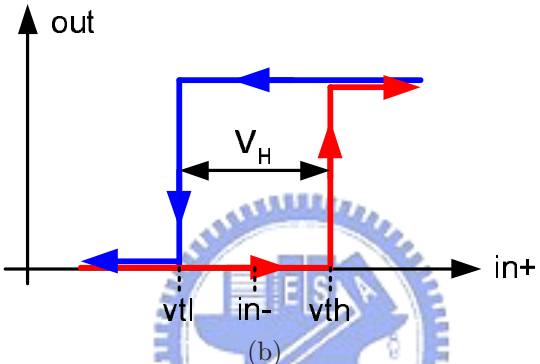
edge of another input signal has arrived. A small delay is added in the reset path to eliminate the dead zone [70]. The dead zone is a non-ideal effect of PFD and charge pump. The charge pump will inject no current to the loop filter if phase error is too small. To solve this problem, UP and DN are simultaneously set high for a short time.

Figure 5.7 shows the charge pump circuit and the loop filter. The charge pump consists of two switched current sources that inject charge into or out of the loop filter and is driven by the PFD. If UP is high, the top current source charges the loop filter. If DN is high, the bottom current source discharges the loop filter. Thus, if $u1$ leads $u2$, the charge pump continues to charge the loop filters and V_{TH} rises.

Parasitic capacitance at the drains of $M1$ and $M2$ causes charge-sharing problem that adds to static phase offset for PFD's input [71]. To solve this problem, charge removal transistors $M3$ and $M4$ are placed to eliminate charge sharing.



(a)



(b)

Figure 5.8: Hysteretic comparator.

Hysteretic Comparator

The hysteretic comparator circuit is shown in Fig. 5.8(a). Two comparators are used to compare positive input with two threshold voltages vth and vtl. These two voltages constitute top and bottom threshold of the hysteresis. An opamp is used to buffer the negative input, $in-$. The threshold voltages are generated from the voltages across the two resistors in series. Therefore, the two threshold voltages track the negative input closely. If the positive input, $in+$, is higher than vth, the output is set high. If $in+$ is lower than vtl, the output is set low.

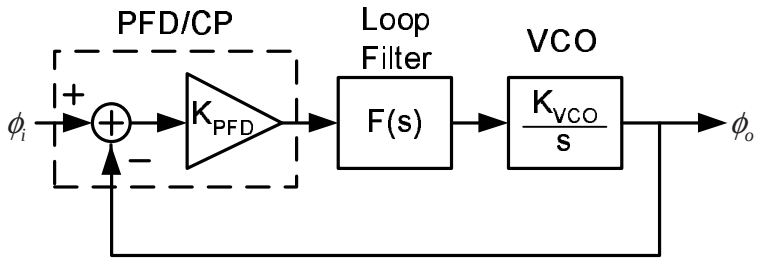


Figure 5.9: Linear model of a PLL.

Switch Driver and Power Stage

The switch driver controls the power switches. Two N-channel MOSFETs are used as the power switches. The advantages of using an N-channel MOSFET are its low conduction resistance $R_{DS(on)}$ and low cost (compared to a P-channel MOSFET with the same $R_{DS(on)}$). However, a driving voltage higher than the input voltage is required to fully turn on the high-side NMOS. Bootstrap is a common technique to obtain a high driving voltage by pumping the input voltage [1]. In addition, a dead time must be inserted between on-times of the high-side and low-side driving signals to prevent short current. Real MOSFET models from the vendors are used in the simulation. The switch driver is not implemented and is modeled by an ideal voltage-controlled voltage source with finite output resistance and internal delay.

5.2.3 Phase-Locked Loop Analysis

In the last section, the PLL circuit is used for synchronizing switching frequency. Much work has been done for the PLL stability analysis [70, 72–74]. It would be desirable to apply the same analysis procudure to the PLL of the ripple control.

The PLL itself is a non-linear system. However, it can be linearized by taking aver-

ages of each cycle. Figure 5.9 shows a linear model of the PLL along with the transfer function of each block. The model is to provide the overall transfer function for the phase, $\phi_o(s)/\phi_i(s)$. The major difference between the PLL block diagram and proposed ripple control regulator is the voltage-controlled oscillator (VCO). Therefore, if the switching behavior of the regulator can be modeled as a VCO, PLL analysis techniques can be applied to the proposed system.

VCO

As mentioned in the beginning of this section, the free-running control regulator is a self-oscillating system with a frequency controlled by many factors. In steady state, the relationship of switching frequency and delay can be derived from Eq. 5.2. With V_{IN} = 20 V, V_{out} = 1.5 V, and V_H = 20 mV, the switching frequency is inversely proportional to the delay, as shown in Fig 5.10. Linear characteristics can be obtained by choosing an operating point around typical delay values, which is stated below:

$$f_{SW} = f_0 + K_{SW} t_D \tag{5.4}$$

Here, f_0 represents the intercept corresponding to $t_D = 0$ and K_{SW} denotes the gain of delay to frequency. As shown in Eq. 5.3, t_D is directly proportional to V_{TH} with a gain of C/I_C. By combining Eqs. 5.3 and 5.4, we have:

$$\begin{aligned} f_{SW} &= f_0 + K_{SW}\frac{C}{I_C}V_{TH} \\ &= f_0 + K_{VCO}V_{TH} \end{aligned} \tag{5.5}$$

The above equation shows that the relationship of the switching frequency and V_{TH} can be characterized as a VCO. Because the output quantity of the analysis is the phase of

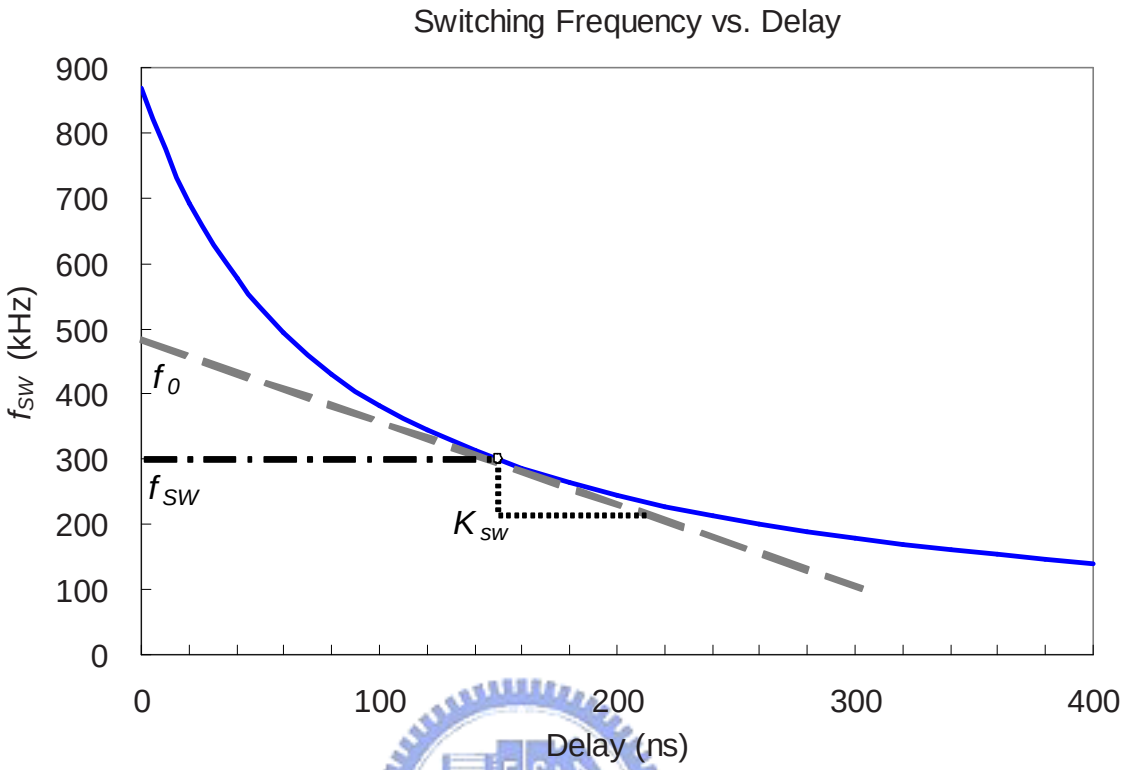


Figure 5.10: Switching frequency versus delay of ripple control buck regulator.

the VCO and phase is the integral of rad frequency, the transfer function of the VCO is:

$$\frac{\phi_o}{V_{TH}}(s) = \frac{K_{VCO}}{s} \tag{5.6}$$

PFD and Charge Pump

The combination of PFD and charge pump is not a linear system. In order to quantify their behavior, the approximation of this discrete-time system by a continuous-time system has been made [70, 72]. The response of a PFD/charge pump to a phase step, $\Delta\phi$, is a linear ramp if the loop filter is a capacitor. The transfer function from $\Delta\phi$ to current injected into the loop filter, I_{out}, is:

$$\frac{I_{out}}{\Delta\phi}(s) = \frac{I_P}{2\pi} \tag{5.7}$$

where I_P is the charge pump current.

Loop Filter

A second-order filter is used in this design. The current injected from the charge-pump develops control voltage of the VCO. Refer to Fig. 5.7, the transfer function of the loop filter is:

$$\begin{aligned} F(s) &= \frac{sC_2R_2+1}{s\left(sC_1C_2R_2+C_1+C_2\right)} \\ &= \frac{1}{C_1+C_2}\frac{sT_2+1}{s\left(sT_1+1\right)} \end{aligned} \tag{5.8}$$

where

$$T_1 = R_2\frac{C_1C_2}{C_1+C_2}, T_2 = R_2C_2$$

The loop filter creates a pole at the origin, another pole at $\omega_p = T_1^{-1}$, and a zero at $\omega_z = T_2^{-1}$. The loop filter gains some phase boost in the frequency between the pole and zero. Therefore, the crossover frequency of total open-loop gain is usually placed here to obtain good phase margin.

PLL

The open-loop transfer function of PLL is equal to:

$$\begin{aligned} G(s) &= K_{PFD}F(s)\frac{K_{VCO}}{s} \\ &= \frac{I_P}{2\pi}\left(\frac{1}{C_1+C_2}\frac{sT_2+1}{s\left(sT_1+1\right)}\right)\frac{K_{VCO}}{s} \end{aligned} \tag{5.9}$$

Denote crossover frequency of $G(s)$ to be ω_c, and phase margin to be ϕ_P. The double poles at the origin can be compensated by properly placing the pole and zero of the loop filter. Let the ratio ω_c/ω_z to be equal to $\omega_p/\omega_c = \gamma$, phase margins with various values of γ are listed in Table 5.1 [7]. It was proved that if a crossover frequency and a phase

Table 5.1: Phase margins with various values of γ.

γ	ϕ_P
1	0
2	36.9°
3	53.1°
4	61.9°
5	67.4°
6	71°

margin are specified, T_1, T_2, C_1, C_2, and R_2 can be obtained as followed:

$$\begin{aligned} T_1 &= \frac{\sec\phi_P - \tan\phi_P}{\omega_c} \\ T_2 &= \frac{1}{\omega_c^2 T_1} \\ C_1 &= \frac{T_1}{T_2}\frac{K_{PFD}K_{VCO}}{\omega_c^2}\sqrt{\frac{1+(\omega_c T_2)^2}{1+(\omega_c T_1)^2}} \\ C_2 &= C_1\left(\frac{T_2}{T_1}-1\right) \\ R_2 &= \frac{T_2}{C_2} \end{aligned} \tag{5.10}$$

Sampling theory shows that f_c must be less than half the switching frequency for the loop to be stable. In order to get good linear approximation of PLL circuits and to avoid interference with transient responses of the voltage regulation, the crossover frequency of PLL is set at tenth of the switching frequency, i.e. $f_c = f_{SW}/10$. Therefore, the PLL is used to synchronize switching frequency in steady state. During the load/line transient, the frequency is still variable like a normal ripple control regulator. The frequency response of PLL is shown in Fig 5.11. C_2 is set to $20C_1$ for a 65° phase margin. The parameters are listed in Table 5.2.

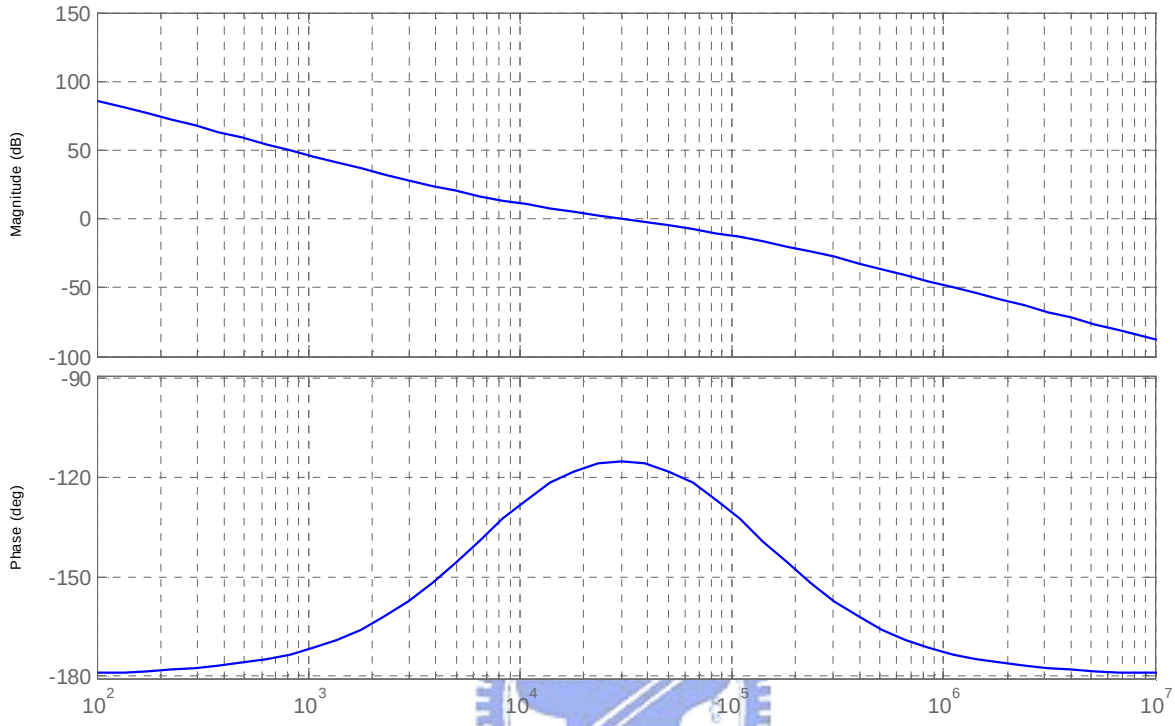


Figure 5.11: Frequency response of PLL.

Table 5.2: Parameters of PLL.

K_{PFD}	100 $\mu/2\pi$
K_{VCO}	0.83 M
f_c	30 kHz
T_1	1.19 μ
T_2	23.7 μ
C_1	83 pF
C_2	1.58 nF
R_2	15 kΩ

5.2.4 Design Considerations

In the previous subsection, we have demonstrated a feasible circuit configuration to realize fixed frequency operations. However, there are some prerequisites for the proposed technique to work properly. In this subsection, design considerations are investigated for a robust design. A design margin must be made to adapt component variations with manufacturing inaccuracy, aging and temperature.

Switching Frequency

The choice of switching frequency is a trade-off between size and efficiency. The value of the switching frequency determines the external components used in the converter, the frequencies of noise generated by the converter, and affects the performance of the converter. Refer to Eq. 2.2, the dynamic power dissipation is proportional to the switching frequency. However, sizes of the filter inductor and capacitor could be smaller by choosing a higher switching frequency. A well-performing high-frequency converter also has faster transient response than one of a low frequency. Table 5.3 lists frequency selection guidelines for voltage regulator in notebook computers [1]. The boundary between high and low frequency is technology dependent. Advances in power MOSFETs improve current capability and switching efficiency thus extends the application toward higher frequencies.

Filter Capacitor

In fixed frequency regulators, the filter capacitor is selected to limit ripple voltage below the tolerance required by the specification. In a voltage-mode ripple control regulator, the output ripple is limited by the comparator hysteresis window. According to Eq. 5.2,

Table 5.3: Frequency selection guidelines [1].

Frequency (kHz)	Typical Application	Comments
200	4-cell Li+ notebook	Use for absolute best efficiency.
300	4-cell Li+ notebook	Considered mainstream by current standards.
450	3-cell Li+ notebook	For lighter load or where size is key.
600	+5 V input	Allows the minimum possible size.

the filter capacitor's ESR and ESL are the most critical parameters.

To calculate the ESR requirement, assume that the output voltage change due to the capacitor's capacitance is much smaller than the voltage change due to the ESR, and that the capacitor's ESL is negligible. In order to limit output voltage change within 100 mV due to a 6.5 A load step, the required ESR is:

$$r_C \leqslant \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{100\text{ mV}}{6.5\text{ A}} = 15.4\text{ m}\Omega \tag{5.11}$$

The output capacitance must have sufficiently low ESR to meet output ripple and load-transient requirements. However, to maintain a fixed switching frequency, the ESR should be sufficiently high. Therefore, the switching frequency sets a minimum value of the ESR. Assume capacitance voltage is negligible, the output voltage ripple is mainly composed of voltages across ESR and ESL. Before the delay is inserted to the control loop, the switching frequency must be higher than the target frequency. Assume the system delay is zero, from Eq. 5.2, the minimum ESR is:

$$r_C \geqslant \frac{f_{SW} \times V_{IN} \times (V_H \times L - l_C \times V_{IN})}{V_{out} \times (V_{IN} - V_{out})} \tag{5.12}$$

For example, minimum required ESR of the proposed design at 300 kHz is:

$$r_C \geqslant \frac{300\ \text{kHz} \times 20\ \text{V} \times (20\ \text{mV} \times 2.2\ \mu\text{H} - 1\ n\text{H} \times 20\ \text{V})}{1.5\ \text{V} \times (20\ \text{V} - 1.5\ \text{V})} = 5.2\ \text{m}\,\Omega \tag{5.13}$$

This ESR value can be obtained by using low ESR electrolytic or Tantalum capacitors in parallel. An ESR value close to the maximum value defined in Eq. 5.11 is suggested to ensure sufficiently high switching frequency. The actual capacitance value required relates to the physical size needed to obtain required ESR. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value. In addition, the capacitance must be high enough to absorb the inductor energy going from a full-load to no-load condition without causing a large overshoot.

ESL of the filter capacitor is another important parameter in a ripple control regulator. The switching frequency equation Eq. 5.2 strongly depends on ESL and this parameter must be reduced to the following level:

$$l_C < (r_C \times t_D + V_H \times L \times D/V_{out}) \tag{5.14}$$

Otherwise, the voltage step across the ESL during switching exceeds the hysteresis window, and the switching frequency becomes too high and uncontrollable. Typical ESL value of an SMD capacitor is around 1 nH.

Filter Inductor

In fixed frequency regulators, the choice of inductor value provides trade-offs between size and efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output ripple. In the voltage-mode ripple control regulator, the ripple current is governed by the output voltage hysteresis and the filter

capacitor's ESR. The inductor value affects the switching frequency. It limits how fast the output voltage traverses through the hysteresis window. As the inductance decreases, the output voltage changes faster, resulting in higher switching frequencies. Therefore, the inductor value is fairly critical and should be stable over the expected load and temperature range.

The minimum required inductance is one that causes the circuit to operate at the edge of critical conduction. In the buck power stage, the average output current is equal to the average inductor current, i.e. $I_{out(avg)} = I_{L(avg)}$. At the edge of critical conduction, the average output current is equal to half of the peak-to-peak inductor current:

$$I_{out(avg)} = \frac{1}{2} \times \Delta I = \frac{V_{IN} - V_{out}}{2 \times L} \times D \times T_S \tag{5.15}$$

Therefore, the minimum required inductance is obtained with a given minimum output current, $I_{out(\min)}$:

$$L \geqslant \frac{V_{IN} - V_{out}}{2 \times I_{out(\min)}} \times D \times T_S \simeq \frac{V_{out} \times (V_{IN} - V_{out})}{2 \times V_{IN} \times I_{out(\min)} \times f_{SW}} \tag{5.16}$$

The maximum required inductance is determined by the hysteresis at a specified switching frequency. With an inductance larger than the maximum value, the switching frequency will fall below the specified value. From Eq. 5.2, the output voltage ripple is equal to the hysteresis window with maximum inductance:

$$V_H = \frac{l_C \times V_{IN}}{L_{\max}} + \frac{V_{out} \times (V_{IN} - V_{out}) \times r_C}{V_{IN} \times L_{\max} \times f_{SW}} \tag{5.17}$$

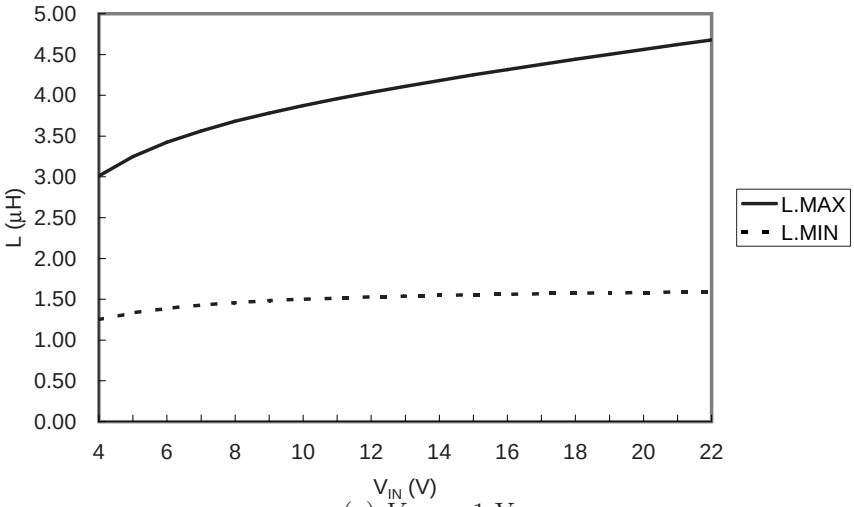
The first term is caused by the ESL and the second term is caused by the ESR. Rearrange above equation, we have:

$$L \leqslant \frac{l_C \times V_{IN}}{V_H} + \frac{V_{out} \times (V_{IN} - V_{out}) \times r_C}{V_{IN} \times V_H \times f_{SW}} \tag{5.18}$$

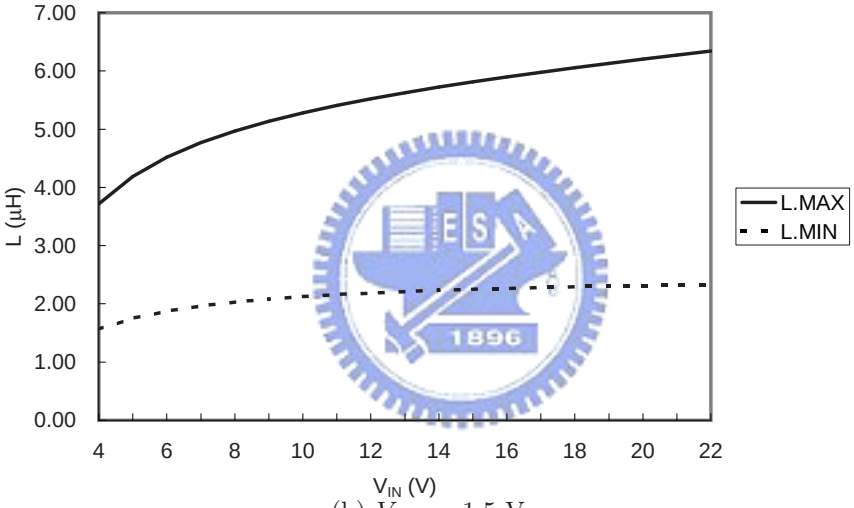
The maximum allowable inductance is inversely proportional to V_H. Assume $l_C = 1$ nH, $V_H = 20$ mV, $r_C = 15$ mΩ, $I_{out(\min)} = 1.5$ A, Figures 5.12 to 5.15 plot the required maximum and minimum values of the filter inductance at different switching frequencies.

The inductance value must be chosen between the lowest maximum value and the highest minimum value over the possible input voltage range at the specified switching frequency. The minimum allowable inductance is determined by the minimum output current, $I_{out(\min)}$. Lower $I_{out(\min)}$ requires higher inductance to avoid entering discontinuous conduction. $I_{out(\min)}$ is usually specified by the application. Therefore, the minimum allowable inductance is not adjustable. The maximum allowable inductance is determined by the hysteresis window, V_H, and the capacitor ESR, r_C. Decreasing V_H lifts the upper limit of inductance but reduces noise immunity. Increasing r_C also lifts the upper limit but increases the output voltage drop during a load transient. These two parameters should be adjusted with caution.

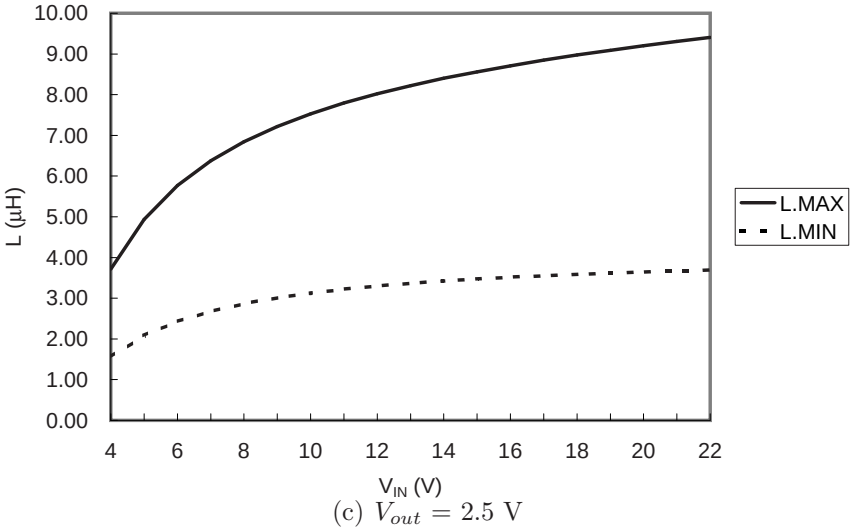
A small V_{IN}-to-V_{out} ratio also limits the choice of inductance. Refer to Fig. 5.15(c), when $V_{out} = 2.5$ V, the range of allowable inductance becomes very small if V_{IN} extends below 6 V. To solve this problem, increasing capacitor ESR is a possible approach because the load current is usually smaller at higher output voltage. A comparison of allowable inductance range with different ESR is shown in Fig. 5.16. If ESR is increased from 15 mΩ to 30 mΩ, maximum allowable inductance is increased. ESR can be adjusted by changing capacitance of the same material or by choosing different material.



(a) $V_{out} = 1$ V

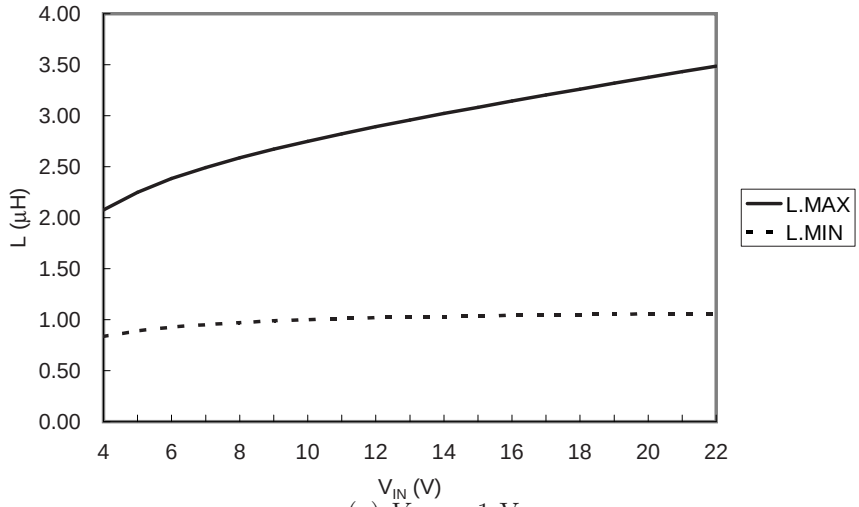


(b) $V_{out} = 1.5$ V

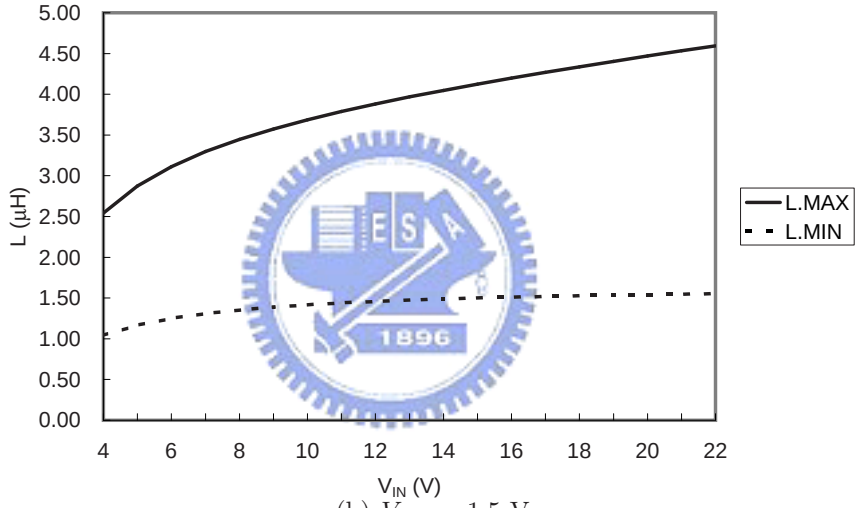


(c) $V_{out} = 2.5$ V

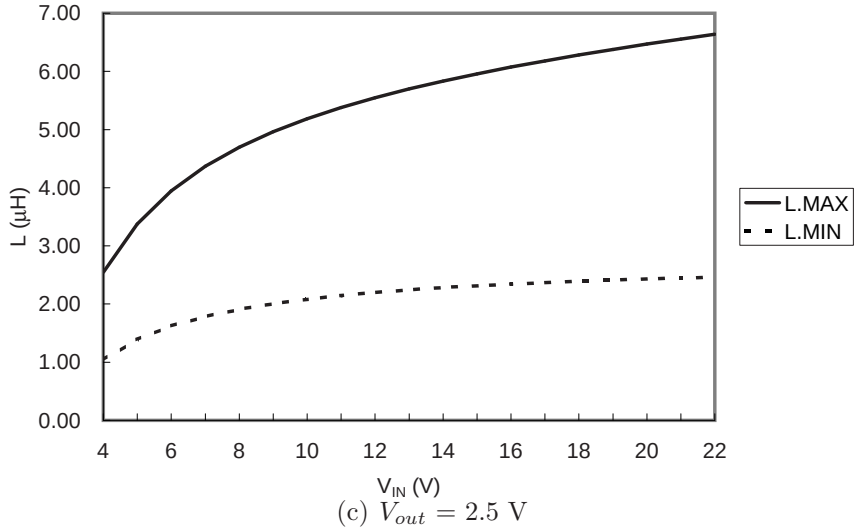
Figure 5.12: Required filter inductance at 200 kHz.



(a) $V_{out} = 1$ V

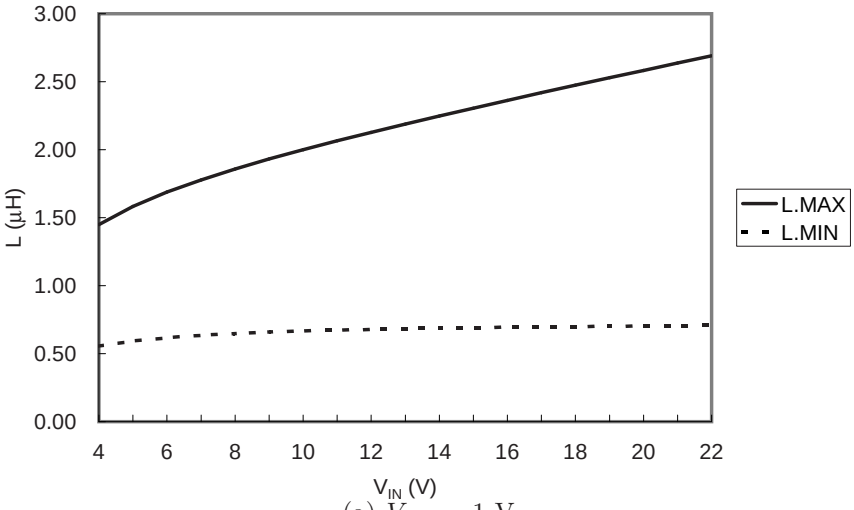


(b) $V_{out} = 1.5$ V

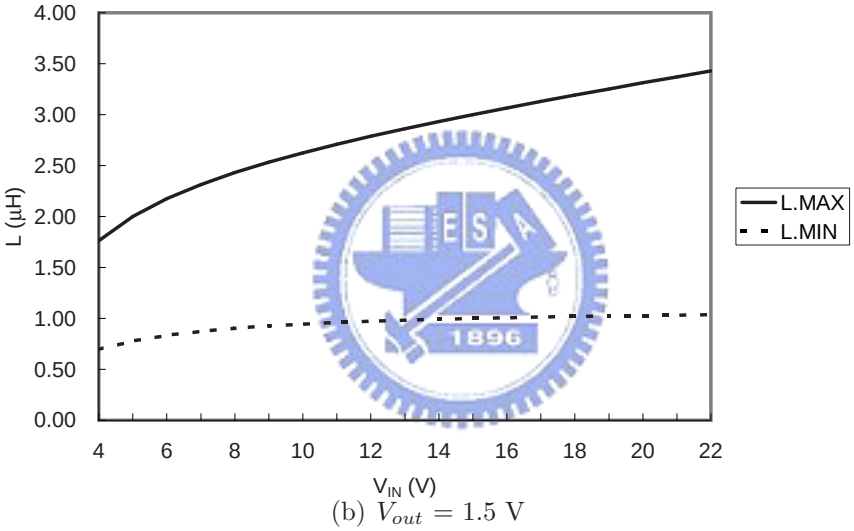


(c) $V_{out} = 2.5$ V

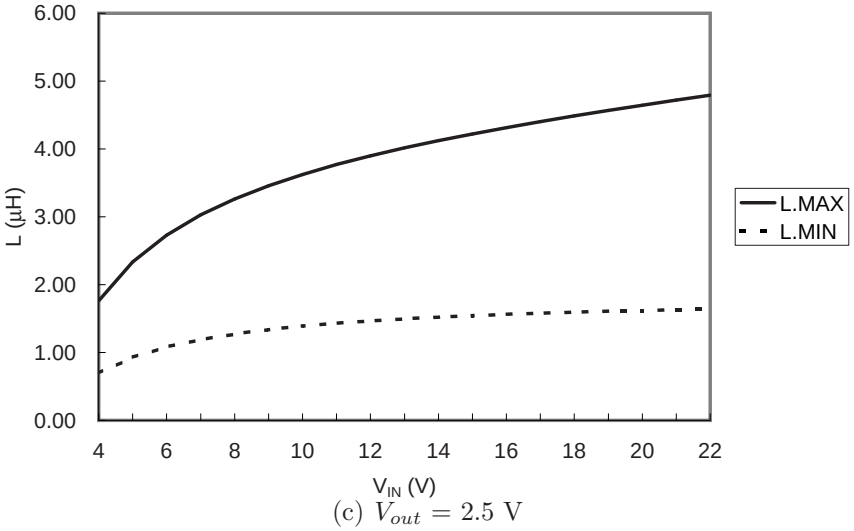
Figure 5.13: Required filter inductance at 300 kHz.



(a) $V_{out} = 1$ V

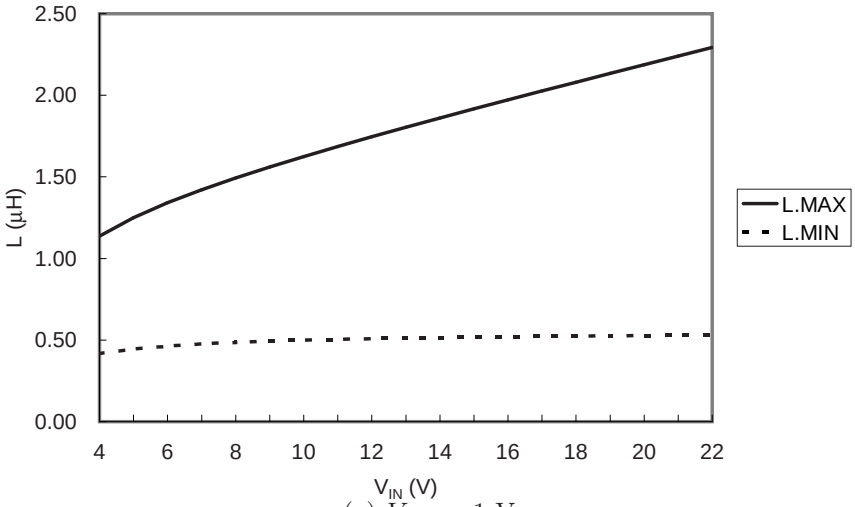


(b) $V_{out} = 1.5$ V

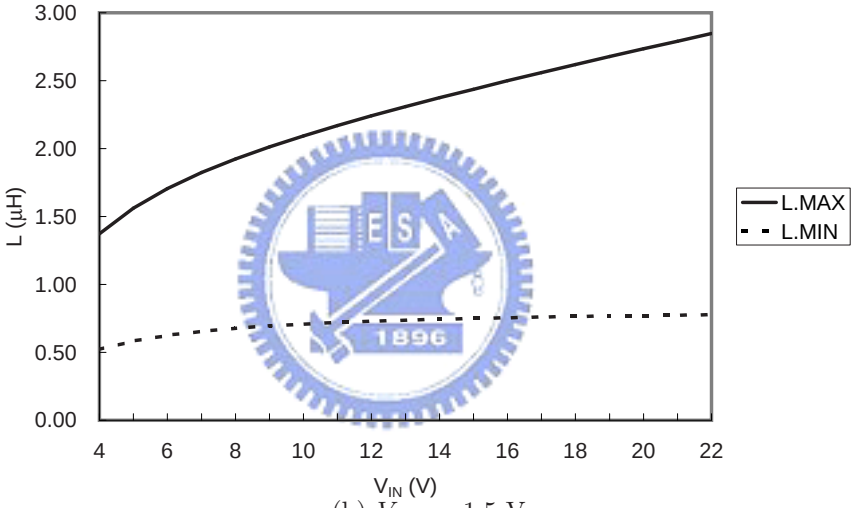


(c) $V_{out} = 2.5$ V

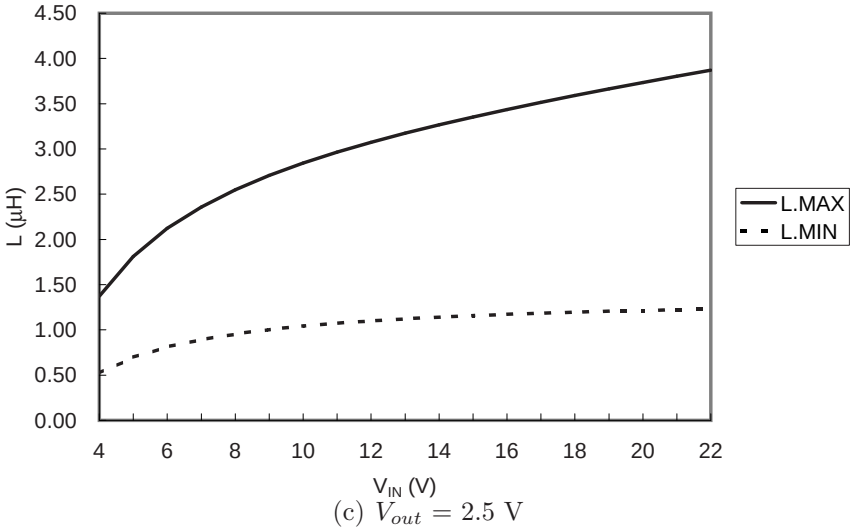
Figure 5.14: Required filter inductance at 450 kHz.



(a) $V_{out} = 1$ V



(b) $V_{out} = 1.5$ V



(c) $V_{out} = 2.5$ V

Figure 5.15: Required filter inductance at 600 kHz.

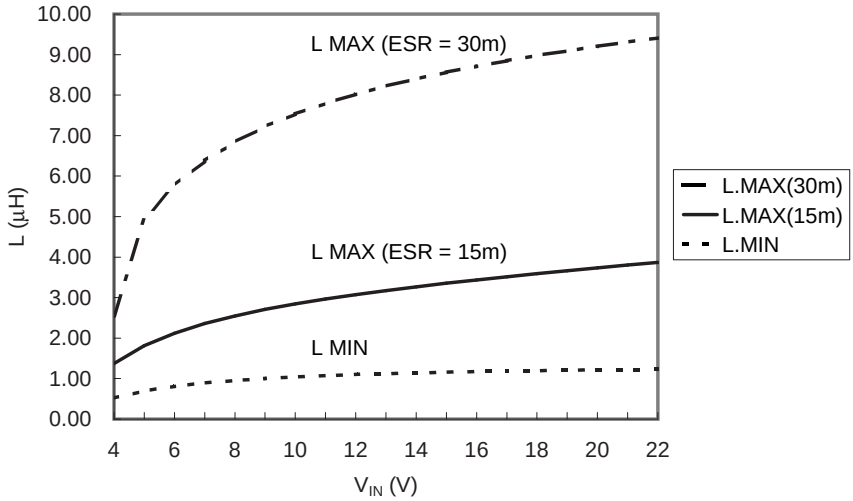


Figure 5.16: Comparison of allowable inductance range with different ESRs.

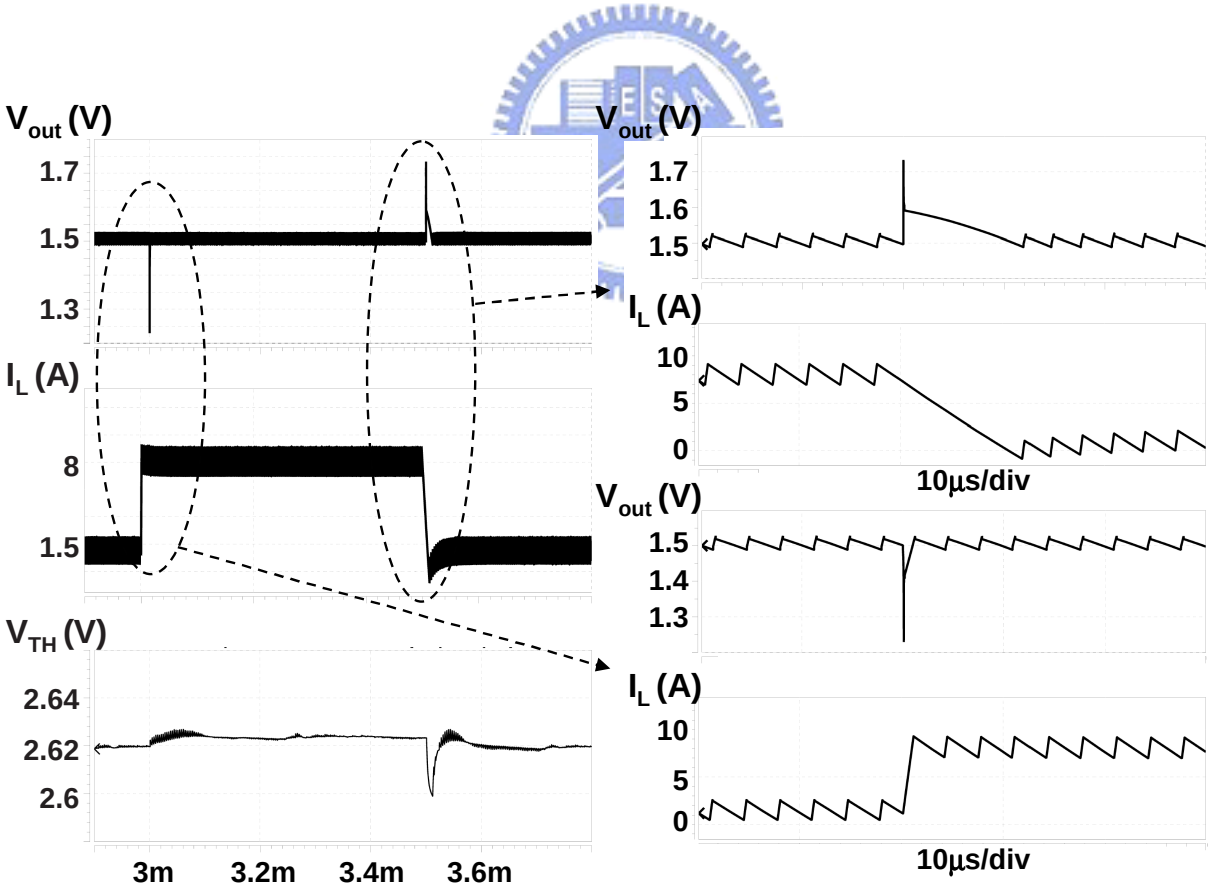


Figure 5.17: Simulated load-transient responses.

Table 5.4: Parameters used in ripple control buck regulator.

Output voltage, V_{out}	1.5 V
Input voltage, V_{IN}	20 V
Hysteresis window, V_H	20 mV
Output current, I_{out}	1.5–8 A
Filter inductor, L	2.2 μH
Filter capacitor, C	940 μF
ESR of capacitor, r_C	15 mΩ
ESL of capacitor, l_C	1 nH
Input clock frequency, f_{clk}	300 kHz

5.2.5 Simulation Results

The proposed ripple control buck regulator shown in Fig. 5.4 was simulated using the transistor level simulator SPICE. Parameter values are listed in Table. 5.4. Figure 5.17 shows the output voltage, the inductor current and the threshold voltage of the delay element waveforms during load transients. At first, the load current increased from 1.5 A to 8 A. The output voltage drops with a magnitude proportional to the product of r_C and load increment ΔI_{out}. The controller connected V_x to V_{IN} in order to increase the inductor current. The inductor current increased quickly with a slope proportional to V_{IN} - V_{out}. The controller did not connect V_x to ground until the output voltage touched the higher hysteretic threshold. When the load current decreased from 8 A to 1.5 A, operations were similar but in the opposite direction. The excess inductor current was decreased slowly with a slope proportional to V_{out}. Therefore, it took longer for V_{out} to recover. The controller did not connect V_x to V_{IN} until the output voltage touched the lower hysteretic threshold. The regulator was always stable during the load transients under this very low V_{out}/V_{IN} condition.

The switching frequency formula Eq. (5.2) does not depend on the load current. In

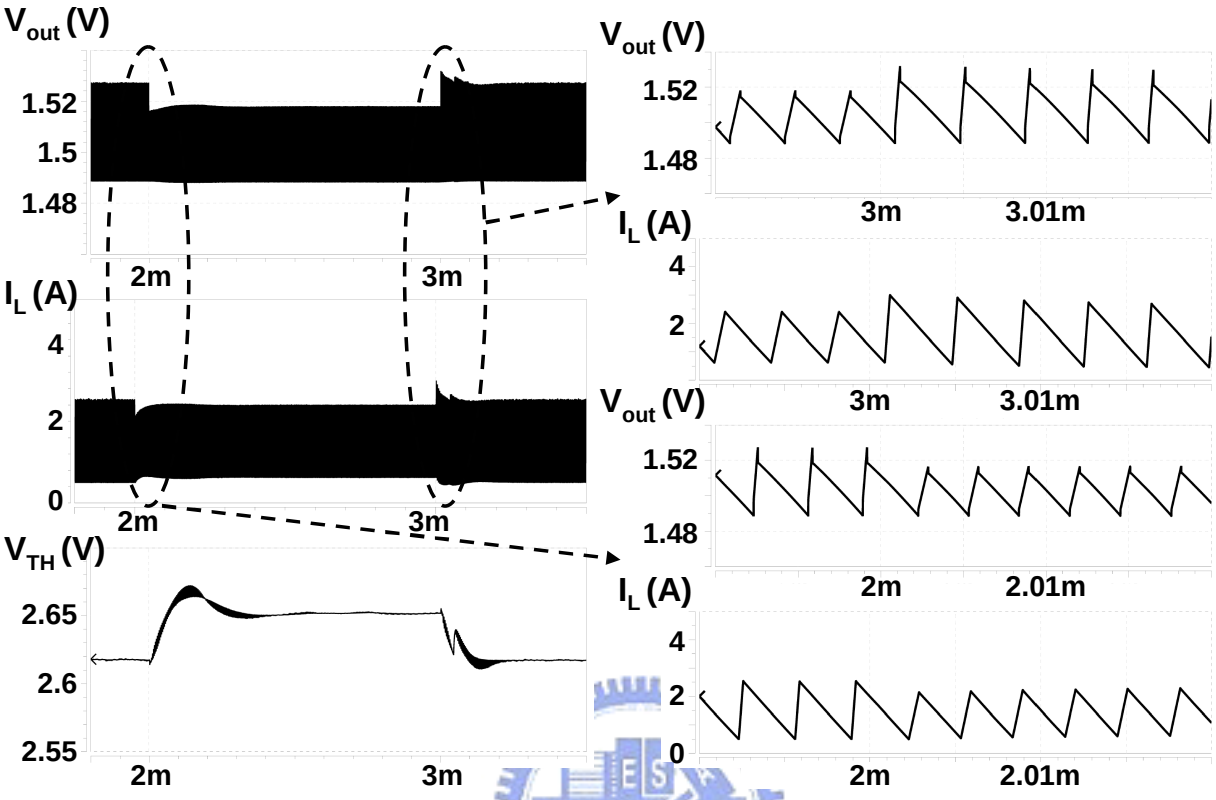
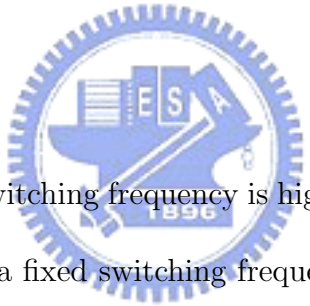


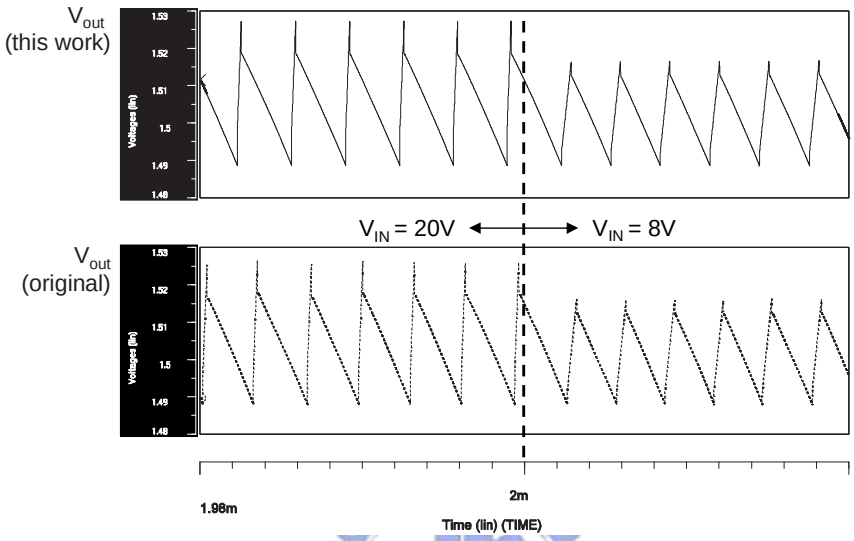
Figure 5.18: Simulated line-transient responses.

fact, the switching frequency of a conventional ripple regulator varies slightly with the load current because additional voltage drops through parasitic resistance of the filter inductor and $R_{DS(on)}$ of the power switches. Therefore, the controlled delay must be modified with the load current to maintain a fixed frequency. As shown in Fig. 5.17, V_{TH} of the delay element increased slightly after the load current increased from 1.5 A to 8 A. The frequency error was around 3.6 % at the beginning of the load transient. The error was corrected by the phase-locked loop. In the long terms, the spread in the frequency spectrum is confined within a small region. The peak-to-peak magnitude of V_{out} is determined by V_H, V_{IN}, V_{out}, and t_D. Only t_D was slightly changed under different load conditions. Load regulation is 0.046 ‰/A from simulation.

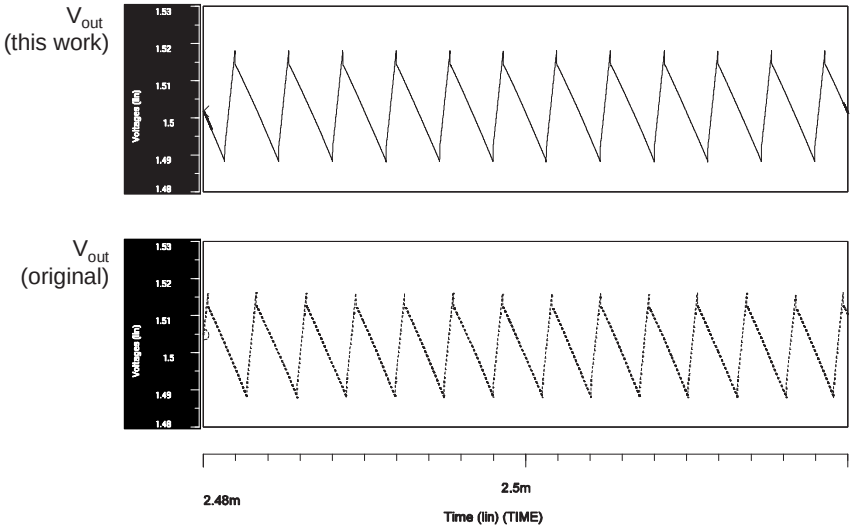
Simulated line transient responses are shown in Fig. 5.18. V_{IN} dropped from 20 V to 8 V at t = 2 ms and went back to 20 V at t = 3 ms. The ripple control regulator exhibited excellent line transient response because V_{IN} affected instantly on duty ratio. The magnitude of the ESL voltage drop was also reduced. As shown in the right of Fig. 5.18, output voltage rose less within the same time t_D when V_{IN} is low. As a result, the peak-to-peak magnitude of V_{out} changed with V_{IN}, which is interpreted as line regulation. Line regulation is 0.028 %/V from the simulation.



Referring to Fig. 5.3(a), switching frequency is higher when V_{IN} = 8 V than 20 V with the same delay. To maintain a fixed switching frequency, V_{TH} in Fig. 5.18 was increased by the phase-locked loop. To verify the effectiveness of the phase-locked loop, Figure 5.19 compares the switching frequency with an original ripple control regulator under different input voltage. The original ripple regulator refers to that shown in Fig. 5.1. The delay is not adjustable. Before the line transient in Fig. 5.19(a), the switching frequency of the proposed fixed-frequency regulator and the original one was 300 kHz. After the line transient from 20 V to 8 V, immediate switching frequencies were changed. It was 330 kHz for the proposed regulator and 328 kHz for the original regulator. At 500 μs after the transient, the control loop has entered steady state. As Fig. 5.19(b) shows, switching frequency had come back to 300 kHz and, switching frequency of the original regulator was still 328 kHz.



(a) During the line transient.



(b) 500 μs after the line transient.

Figure 5.19: Switching frequency comparison between the proposed and an original ripple control buck regulator during a line transient.

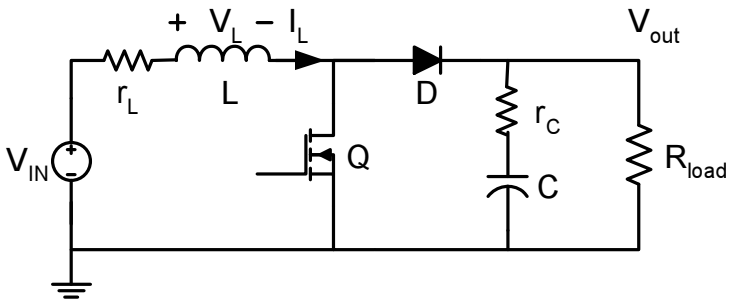


Figure 5.20: Boost converter schematic.

5.3 Current Mode Ripple Control Boost Regulator with Fixed Output Frequency

The boost converter, also called step-up converter, is a popular topology. It is chosen when the desired output voltage is always higher than the input voltage. This is a common operating condition in portable electronic systems such as digital still cameras, MP3 players, and personal digital assistants (PDA). These devices are usually powered by one to two alkaline or nickel-metal-hydride (NiMH) cells battery, or a single Li-ion cell battery. Therefore, the input voltage may vary from 0.9 V to 4.2 V. The converter has to convert the input voltage to standard chip supply voltage (e.g. 5 V, 3.3 V, or 2.5 V).

Figure 5.20 shows the schematic of the boost filter. Power switch Q is an N-channel MOSFET. The output diode D restricts the current to flow from the inductor to the output only. Inductor L and capacitor C make up the effective output filter. Resistor R_{load} represents the load seen by the power supply output. The input current for a boost converter is continuous, or non-pulsating, because the input current is the same as the inductor current. The output current for a boost converter is discontinuous, or pulsating, because the output diode conducts only during a portion of the switching cycle. The

output capacitor supplies the entire load current for the rest of the switching cycle.

During normal operation of the boost converter, Q is repeatedly switched on and off. This switching action creates a train of pulse at the junction of Q, D, and L. Although inductor L is connected to output capacitor C only when D conducts, and effective LC output filter is formed. It filters the train of pulses to produce a DC output voltage, V_{out}.

In this section, methods and circuits are proposed to achieve fixed frequency operation of the ripple control boost converter. First, steady-state relationship of the variables in the boost converter is presented. Then small-signal analysis gives the control-to-output-voltage transfer function using the PWM switch model. From the analysis, we find voltage-mode ripple control is not applicable to the boost converter. Current-mode ripple control is used to obtain proper operation in the boost converter. A feasible circuit implementation is described to synchronize the current-mode ripple control boost regulator with a reference clock. The controller includes an error amplifier and compensation network. Compensation technique is also described. A calculation example of loop parameters will be shown. Simulation results will be in the last subsection.

5.3.1 Boost Converter Steady-State Analysis

A power converter can operate in either continuous or discontinuous conduction mode. In continuous conduction mode, the current flows continuously in the inductor during the entire switching cycle in steady-state operation. In discontinuous conduction mode, inductor current is zero for a portion of the switching cycle. It starts at zero, reaches a peak value, and returns to zero during each switching cycle. It is desirable for a power converter to stay in only one mode over its expected operation conditions because the

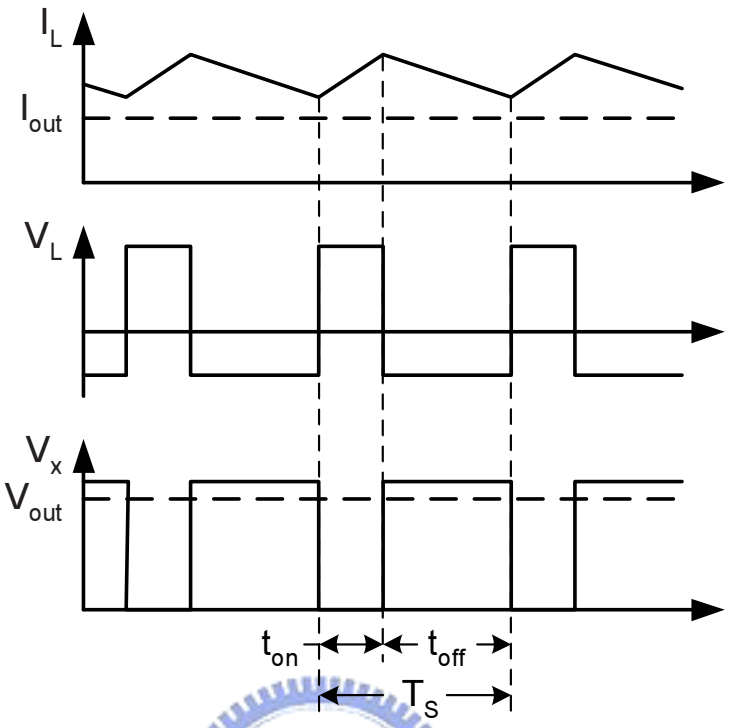


Figure 5.21: Boost converter waveforms in continuous conduction mode.

power converter frequency response changes significantly between the two modes of operation [2, 22, 75]. The main purpose of this subsection is to derive the voltage conversion relationship for the continuous conduction mode boost converter. The result is important because it shows how the output voltage depends on duty cycle and input voltage, or how the duty cycle can be calculated based on input and output voltages. Steady state implies that input voltage, output voltage, and load current are fixed and not varying.

Refer to Fig. 5.20. There are two states per switching cycle. In the on state, Q is on and D is off. In the off state, Q is off and D is on. The duration of the on state is $D \times T_s = t_{on}$, where D is the duty ratio set by the control circuit, expressed as a ratio of the switch on time to the time of one complete switching cycle, T_s. The duration of the off state is t_{off}. Since there are only two states per switching cycle for continuous

conduction mode, t_{off} is equal to $(1 - D) \times T_s$. These times are shown along with the waveforms in Fig. 5.21.

During the on state, Q, which presents a low drain-to-source resistance, $R_{DS(on)}$, has a small voltage drop of V_{DS}. There is also a small voltage drop across the DC resistance of inductor equal to $I_L \times r_L$. The current builds up in inductor L due to the inductor voltage:

$$V_{L(on)} = V_{IN} - (V_{DS} + I_L \times r_L) = L \times \frac{dI_L}{dt} \tag{5.19}$$

Since the applied voltage is essentially constant, the inductor current increase linearly with a slope:

$$\frac{dI_L}{dt} = \frac{V_{L(on)}}{L} = \frac{V_{IN} - (V_{DS} + I_L \times r_L)}{L} \tag{5.20}$$

Diode D is off during this time because it is reverse biased. The entire output load current is supplied by output capacitor C.

When Q is off, it exhibits high drain-to-source impedance. Since the current flowing in inductor L cannot change instantaneously, the current shift from Q to D. The inductor voltage reverses polarity and adds to the input voltage, making the output voltage greater than the input voltage. The voltage applied to the left side of L remains the same as before at $V_{IN} - I_L \times r_L$. The voltage applied to the right side of L is now the output voltage, V_{out}, plus the diode forward voltage, V_d. Therefore, the off state inductor voltage is given by:

$$V_{L(off)} = V_{IN} - (V_{out} + V_d + I_L \times r_L) \tag{5.21}$$

Because this applied voltage is negative, the inductor current decreases linearly with a

slope:

$$\frac{dI_L}{dt} = \frac{V_{L(off)}}{L} = \frac{V_{IN} - (V_{out} + V_d + I_L \times r_L)}{L} \tag{5.22}$$

In steady-state conditions, the average voltage across an inductor over a complete cycle is zero. Otherwise, the inductor current would have a net increase or decrease from cycle to cycle which would not be a steady state condition. This principle is called *inductor volt-second balance* [6]. Therefore:

$$V_{L(on)} \times t_{on} + V_{L(off)} \times t_{(off)} = 0 \tag{5.23}$$

Using $D \times T_S$ for t_{on}, and using $(1 - D) \times T_S$ for t_{off}, we have:

$$[V_{IN} - (V_{DS} + I_L \cdot r_L)] \cdot D \cdot T_S + [V_{IN} - (V_{out} + V_d + I_L \cdot r_L)] \cdot (1 - D) \cdot T_S = 0 \tag{5.24}$$

Therefore, the steady-state equation for V_{out} is:

$$V_{out} = \frac{V_{IN} - I_L \times r_L}{1 - D} - V_d - V_{DS} \times \frac{D}{1 - D} \tag{5.25}$$

The above equation for V_{out} illustrates that V_{out} can be adjusted by changing the duty ratio, D, and is always greater than the input because D is between 0 and 1. If V_{DS} and $I_L \times R_L$ are small enough to be ignored, Eq. 5.25 is simplified considerably to:

$$V_{out} = \frac{V_{IN}}{1 - D} - V_d \tag{5.26}$$

Above equation can be rewritten as follows:

$$D = \frac{V_{out} + V_d - V_{IN}}{V_{out} + V_d} \tag{5.27}$$

The effect of loss on the DC voltage is shown in Fig. 5.22. Below a level of duty ratio, the voltage gain is less than unity in a real boost converter.

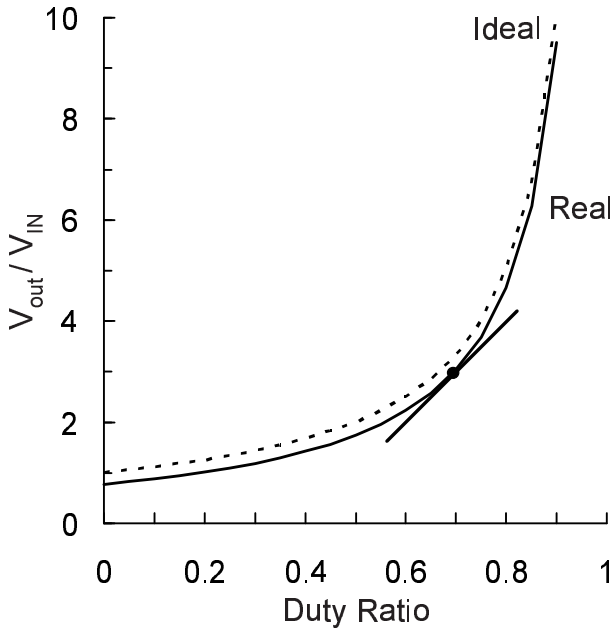


Figure 5.22: Boost converter DC voltage gain.

From Eq. 5.20, the inductor current ripple, ΔI_L is:

$$\begin{aligned} \Delta I_L &= \frac{dI_L}{dt} \times t_{on} = \frac{V_{IN} - (V_{DS} + I_L \times R_L)}{L} \times t_{on} \\ &\cong \frac{V_{IN}}{L} \times D \times T_S \end{aligned} \tag{5.28}$$

Unlike the buck filter, the average of the inductor current of the boost converter is not equal to the output current. The inductor delivers current to the output only during the off state of the converter. The relationship between the average inductor current and the output current for the continuous boost converter is given by the fact that the input power equals output power,

$$V_{IN} \times I_{L(avg)} = V_{out} \times I_{out} \tag{5.29}$$

Therefore:

$$I_{out} = I_{L(avg)} \times \frac{V_{IN}}{V_{out}} = I_{L(avg)} \times (1 - D) \tag{5.30}$$

From the above equations, we find that the average inductor current is proportional to the output current. However, the inductor ripple current, ΔI_L, is independent of the load current. Therefore, the maximum and minimum values of the inductor current track the average inductor current exactly. Critical inductor value between continuous and discontinuous conduction mode can be determined using this relationship. At the boundary of these two modes,

$$I_{L(avg)} = \frac{\Delta I_L}{2} \tag{5.31}$$

The boundary condition must occur at the minimum specified load current. Combine above equation with Eq. 5.28 and Eq. 5.30, we have:

$$I_{out(\min)} = \frac{\Delta I_L}{2} \times (1-D) = \frac{V_{IN}}{2L} \times D \times T_S \times (1-D) \tag{5.32}$$

Therefore:

$$L \geqslant \frac{V_{IN}}{2 \times I_{out(\min)}} \times T_S \times D \times (1-D) \tag{5.33}$$

To ensure continuous conduction mode, the inductor must satisfy above relationship for all likely operating conditions.

5.3.2 Boost Converter Small-Signal Analysis

The boost converter has two inputs: the input voltage and the duty ratio. The duty ratio is controlled by the controller. Referring to Fig. 5.22, unlike the buck converter, the boost converter has a nonlinear voltage conversion ratio versus duty ratio. The nonlinearity is a result of the switching components in the converter. A nonlinear circuit is difficult to analyze. However, linear characteristics can be obtained by choosing a certain operating point. As the straight line in Fig. 5.22, we can build a linear model around an operating

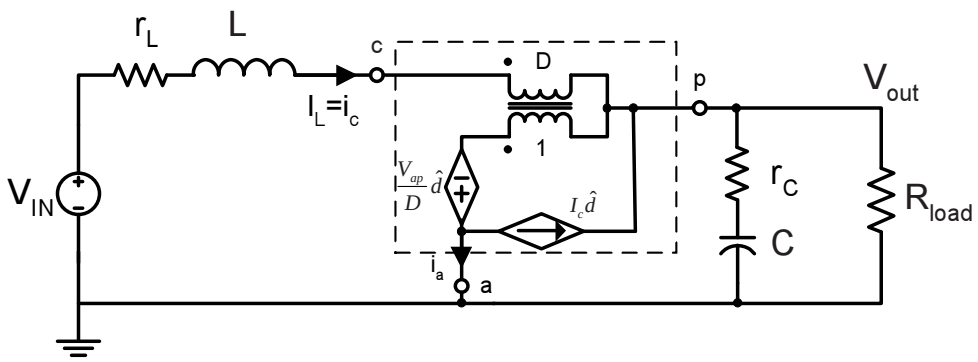


Figure 5.23: PWM switch model.

point. If the variations in duty ratio are kept small, a linear model accurately represents the nonlinear behavior of power converter being analyzed. Linearity allows the use of many analysis tools available for linear systems.

There are to ways to model the power converters. One way is to use state-space averaging (SSA) method [76]. The SSA models the *whole* converter in its entire electrical form. Its process is carried over all the elements of the converter and the process can be very long and complicated. To model the boost converter, the PWM switch model [77, 78] is used. The PWM switch model is inserted into the converter by *only* replacing the switching elements, the MOSFET switch and the diode.

The PWM switch model is drawn inside the dashed-line box in Fig. 5.23. The model is useful for determining the DC operating point and for finding AC transfer functions of a converter [5, 75, 79]. The capital letters indicate DC signals depending on the operating point of the circuit. The lowercase letters with a caret indicate the AC signals. The lowercase letters indicate signals with both DC and AC components. For example, D represents the steady-state duty ratio, $\hat{d}$ represents AC signal of the duty ratio and d represents the complete duty ratio including and DC component and AC variations.

For DC analysis, $\hat{d}$ is zero, L is a short, and C is open. By applying KVL around the loop:

$$-V_{IN} + I_L \times r_L + V_{cp} + V_{out} = 0 \tag{5.34}$$

but

$$V_{cp} = V_{ap} \times D = -V_{out} \times D \tag{5.35}$$

and

$$I_{out} = \frac{V_{out}}{R_{load}} = I_c - I_a = I_c - I_c \times D \Rightarrow I_c = \frac{V_{out}}{R_{load}} \times \frac{1}{1-D} \tag{5.36}$$

Substituting V_{cp} and I_c into the first equation, we have the ratio of the output voltage to the input voltage:

$$M = \frac{V_{out}}{V_{IN}} = \frac{1}{1-D} \times \frac{1}{1 + \frac{r_L}{R_{load} \times (1-D)^2}} \tag{5.37}$$

The same result can be obtained by setting V_d and V_{DS} to zero in Eq. 5.25 derived in the steady-state analysis subsection.

The DC analysis determines parameters V_{ap} and I_c in the PWM switch model. Therefore, we can proceed to AC analysis. Setting DC voltage V_{IN} to zero, the duty-ratio-to-output-voltage transfer function is expressed as:

$$\frac{\hat{v}_{out}}{\hat{d}}(s) = G_{do} \times \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \times \left(1 - \frac{s}{\omega_{z2}}\right)}{1 + \frac{s}{\omega_o \times Q} + \frac{s^2}{\omega_o^2}} \tag{5.38}$$

where,

$$G_{do} \cong \frac{V_{IN}}{(1-D)^2}$$
$$\omega_{z1} = \frac{1}{r_C \times C}$$
$$\omega_{z2} \cong \frac{(1-D)^2 \times R_{load} - r_L}{L}$$
$$\omega_o \cong \frac{1}{\sqrt{L \times C}} \times \sqrt{\frac{r_L + (1-D)^2 \times R_{load}}{R_{load}}}$$
$$Q = \frac{\omega_o}{\frac{r_L}{L} + \frac{1}{C \times (R_{load} + r_C)}}$$

To identify the positions of poles and zeros easily, r_L and r_C are omitted from the above equations. Therefore, there exits a double pole and a right-half-plane (RHP) zero in the transfer function and their are located at:

$$\omega_{double-pole} = \frac{(1-D)}{\sqrt{L \times C}} \tag{5.39}$$

and

$$\omega_{\text{RHP - zero}} = \frac{(1-D)^2 \times R_{load}}{L} \tag{5.40}$$

Compared with an L-C filter, this double pole shifts to lower frequencies, the phase delay also comes in at a lower frequency, making the response slower. Another troublesome feature of the boost converter is its RHP zero. The RHP zero exhibits the magnitude asymptotes of the LHP zero, and the phase asymptotes of the pole, which results in gain boost with an extra phase delay that will introduce instability into the loop gain [6].

RHP zeros are a special characteristic of active circuits. When given a changed input, there is a tendency to respond initially in the wrong direction. Eventually, the output will move in the direction commanded by the input. How fast it starts moving in the right direction is determined by the RHP zero frequency. The cause of the RHP zero is

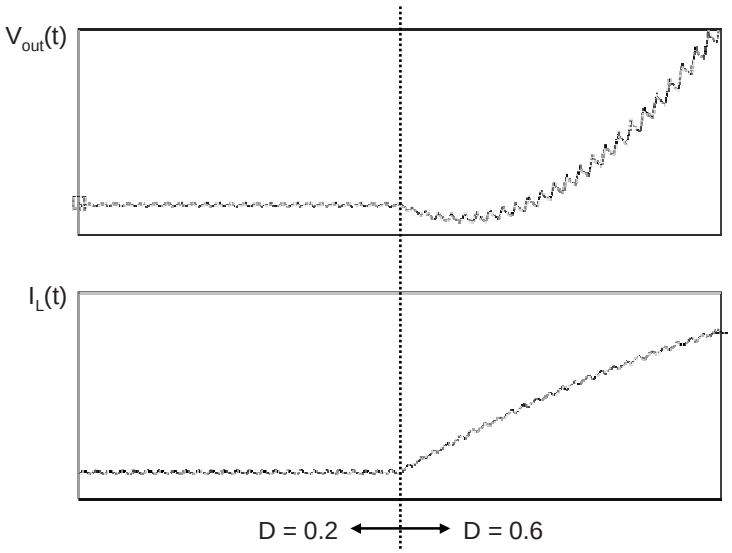
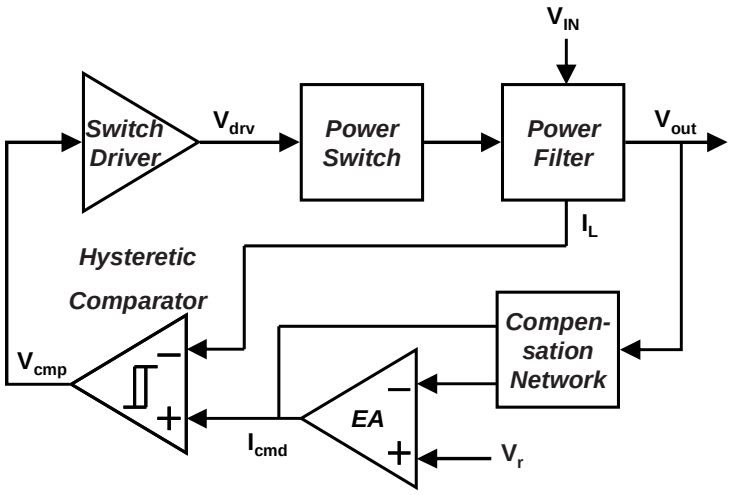


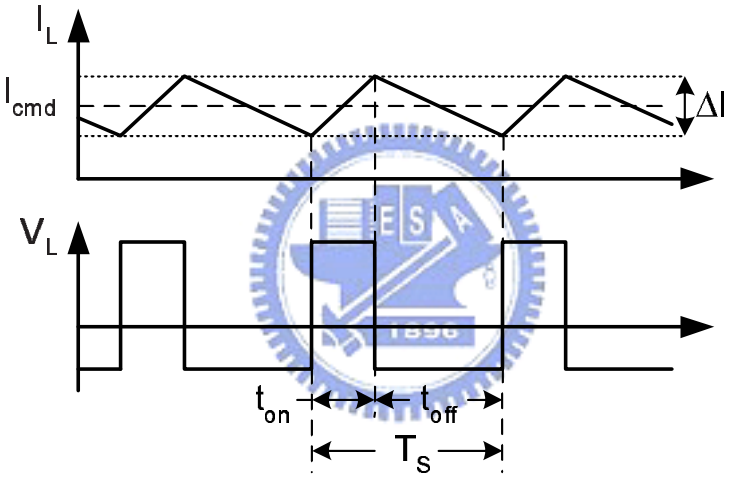
Figure 5.24: Effects of the RHP zero: a step increase in duty ratio causes a initial decrease in output voltage.

intuitive. The output capacitor of the boost converter is charged by the inductor current only when the power switch is turned off. As shown in Fig. 5.24, the immediate effect of increasing duty ratio is only to reduce the time current is flowing through the diode. Hence, an increase in command to the system results in a temporary droop in the output voltage. As the inductor current increases to its new equilibrium value, average diode current eventually increases.

This can be confusing for a controller that is monitoring the output voltage to make control decisions. There is no alternative but to wait and see where the long-term trend is before adjusting the duty cycle. Therefore, the voltage-mode ripple control regulator proposed in the previous section is not suitable for the boost power stage. Instead of monitoring the output voltage, the inductor current is sensed and controlled directly by the controller. This is called current-mode ripple control.



(a)



(b)

Figure 5.25: Block diagram and waveforms of the current-mode ripple control regulator.

5.3.3 Current-Mode Ripple Control Boost Converter

In current-mode control, the controller tries to control the inductor current directly. The duty ratio of the switch is controlled indirectly. Among various types of current-mode control, the ripple control, also called hysteretic current-programmed control [39, 80], offers the tightest control over the inductor current and the fastest attainable response of the inductor current. The block diagram of the current-mode ripple control regulator

is shown in Fig. 5.25(a). The hysteretic comparator limits the inductor current within a hysteretic window ΔI. As shown in Fig. 5.25(b), the switch is turned off when the inductor current rises to the top threshold, $I_{cmd} + \Delta I/2$. When the inductor current falls to the bottom threshold, the switch is turned on again. The current command, I_{cmd}, is generated by the error amplifier. Additional compensation network is required to improve frequency response and stability.

Much work has been done to analyze the small-signal dynamic response of the current-mode boost converter [6, 39, 46, 55, 80]. The derived small-signal transfer functions can be used to design the feedback compensation loop. The procedure of analysis is similar to that of a voltage-mode converter. However, the inductor current is now a control signal because it is tightly controlled by the current command. The duty ratio is no longer a control input and is substituted by other variables. It can be shown that the small-signal control-to-output transfer function of the current-mode ripple control boost converter is expressed as:

$$\frac{\hat{v}_{out}}{\hat{i}_{cmd}}(s) = G_{eo} \times \frac{\left(1 - \frac{s}{\omega_z}\right)}{1 + \frac{s}{\omega_p}} \tag{5.41}$$

where,

$$\omega_z = \frac{(1-D)^2 \times R_{load}}{L}$$

$$\omega_p = \frac{2}{R_{load} \times C}$$

If we introduce the control-to-inductor-current gain, k, then:

$$G_{eo} = \frac{k \times R_{load} \times (1-D)}{2}$$

An RHP zero still exists in the control-to-output transfer function. Refer to Eq. 5.40, the RHP zero expression is exactly the same as that for voltage-mode. Using current mode

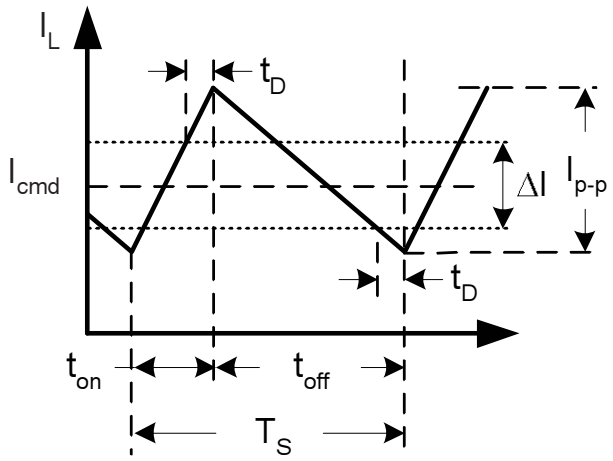


Figure 5.26: Inductor current waveform in a current-mode ripple control regulator.

does not move this at all. The reason explained in the previous subsection still exists in current-mode control. No matter what kind of control law is employed, it takes time for the switch to increase the average inductor current. Therefore, the output voltage will decrease initially and then increase.

Even though the RHP zero does exit, the number of pole is reduced from two to one. The inductor is virtually disappeared from the loop because the inductor current is directly controlled, which makes compensation easier. Compensation of the error amplifier and loop design will be discussed in the next subsection.

5.3.4 Circuit Design for Fixed Switching Frequency

Main concept of obtaining fixed switching frequency operation by inserting delay is the same as the voltage-mode ripple control buck regulator. Before going through detailed circuits design, switching frequency variation is first investigated.

Figure 5.26 shows the inductor current waveform in a current-mode ripple control regulator. During the on-time of the switch, t_{on}, the inductor current ramps up with the

slope expressed in Eq. 5.20 which is represented by A and a:

$$\frac{dI_L}{dt}(on) = \frac{V_{IN} - (V_{DS} + I_L \times R_L)}{L} = A = \frac{a}{L} \tag{5.42}$$

During the off-time, t_{off}, the inductor current ramps down with the slope expressed in Eq. 5.22 which is represented by B and b:

$$\frac{dI_L}{dt}(off) = \frac{V_{IN} - (V_{out} + V_d + I_L \times R_L)}{L} = -B = -\frac{b}{L} \tag{5.43}$$

In a ripple control regulator, the fixed hysteresis band, ΔI, controls the AC current through the inductor. But the actual inductor current ripple, I_{p-p}, is larger than the hysteresis band, because of the delay, t_D. The on-time current ripple, $\Delta I_{(on)}$, is:

$$\Delta I_{(on)} = A \times \left[t_{on} - t_D \times \left(1 + \frac{B}{A} \right) \right] \tag{5.44}$$

and the off-time current ripple, $\Delta I_{(off)}$, is:

$$\Delta I_{(off)} = B \times \left[t_{off} - t_D \times \left(1 + \frac{A}{B} \right) \right] \tag{5.45}$$

In steady state, $\Delta I_{(on)} = \Delta I_{(off)} = \Delta I$. Solving for t_{on} and t_{off} produces the following equations:

$$t_{on} = \frac{\Delta I + t_D \times (A + B)}{A} \tag{5.46}$$

$$t_{off} = \frac{\Delta I + t_D \times (A + B)}{B} \tag{5.47}$$

Because the total cycle time $T_S = t_{on} + t_{off}$ and switching frequency $f_{SW} = 1/T_S$,

$$\begin{aligned} f_{SW} &= \frac{A \times B}{\Delta I \times (A + B) + t_D \times (A + B)^2} \\ &= \frac{a \times b}{\Delta I \times L \times (a + b) + t_D \times (a + b)^2} \\ &= \frac{(V_{IN} - V_{DS} - I_L \times r_L)(V_{out} + V_d + I_L \times r_L - V_{IN})}{\Delta I \times L \times (V_{out} + V_d - V_{DS}) + t_D \times (V_{out} + V_d - V_{DS})^2} \end{aligned} \tag{5.48}$$

Neglecting losses, V_{DS} and $I_L \times r_L$, the equation is simplified as below:

$$f_{SW} = \frac{V_{IN} \times (V_{out} + V_d - V_{IN})}{\Delta I \times L \times (V_{out} + V_d) + t_D \times (V_{out} + V_d)^2} \tag{5.49}$$

In common condition, only V_{IN}, V_{out}, and t_D affect the switching frequency, because ΔI and L are seldom altered in a running system. Compared with the voltage-mode switching frequency in Eq. 5.2, the switching frequency of current mode is not a function of ESR and ESL of the output capacitor, because ESR and ESL only affect the output voltage. Therefore, the switching frequency of the current-mode ripple control regulator is less disturbed by non-ideal factors. Figure 5.27 estimates the switching frequency variations against V_{IN} with different V_{out}. Parameters used are the followings: ΔI=0.2 A, L=8.2 μH, and t_D=150 ns. The switching frequency still varies significantly with output and input voltage. To improve this drawback, circuits for synchronizing current-mode ripple control boost regulators are proposed in this thesis.

Figure 5.28 shows the proposed control loop for the boost converter. Both the output voltage and the inductor current are sampled by the controller. The output voltage is sensed through a compensation network and then amplified by an error amplifier (EA). In the ripple control regulator, the inductor current must be monitored during the whole switching cycle. Therefore, a small sensing resistor is placed in series with the inductor. Then a current sense amplifier (CSA) amplifies the signal. A comparator with hysteresis is used to avoid false crossing detections caused by the noise and is an essential part to the ripple controller. Similar to the proposed voltage-mode ripple controller, a delay element is placed after the comparator. A negative feedback loop that uses a PFD is added to determine the accurate delay value which is directly proportional to V_{TH}.

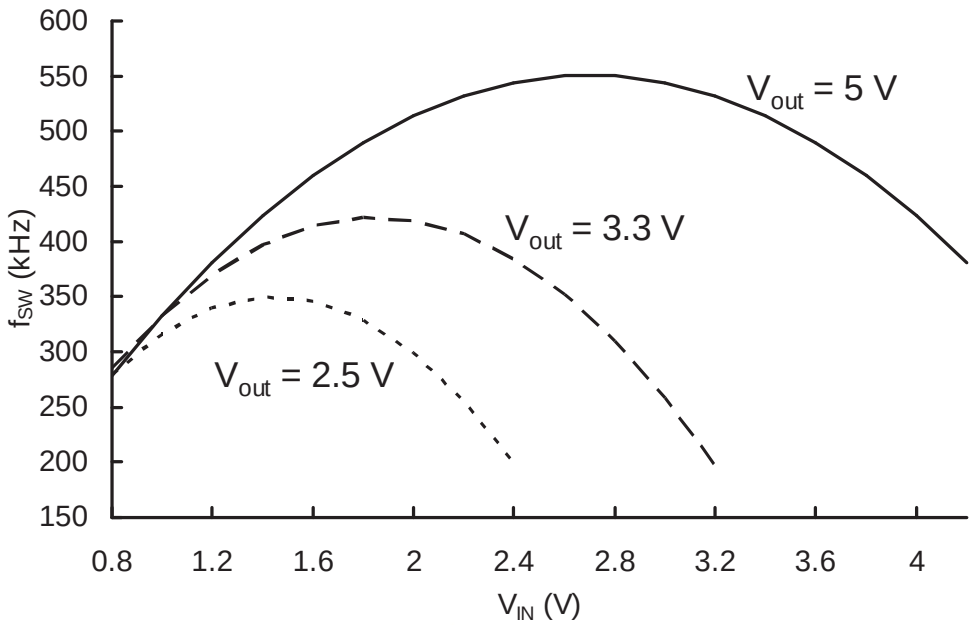


Figure 5.27: Frequency variations of the current-mode ripple control boost regulator.

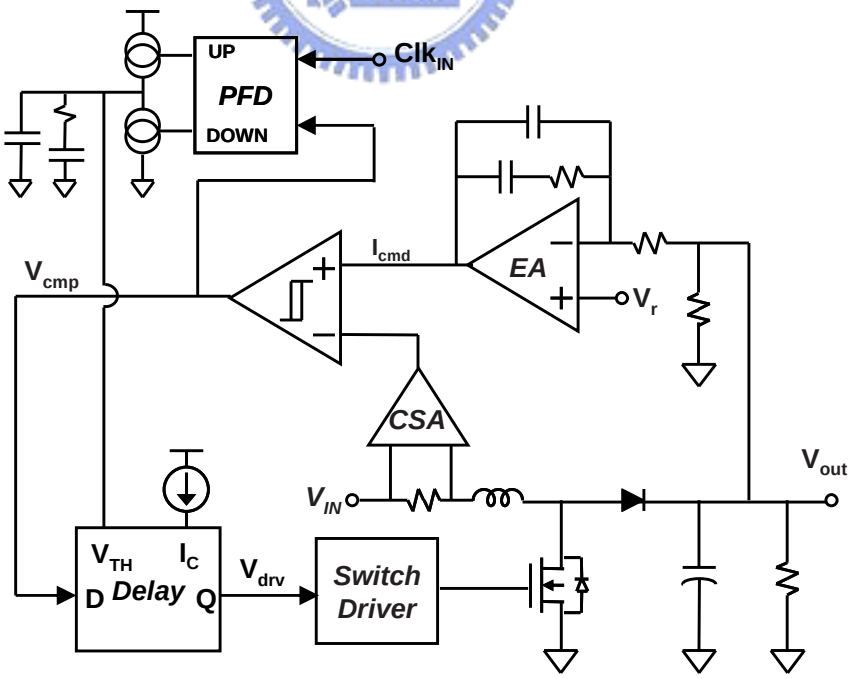
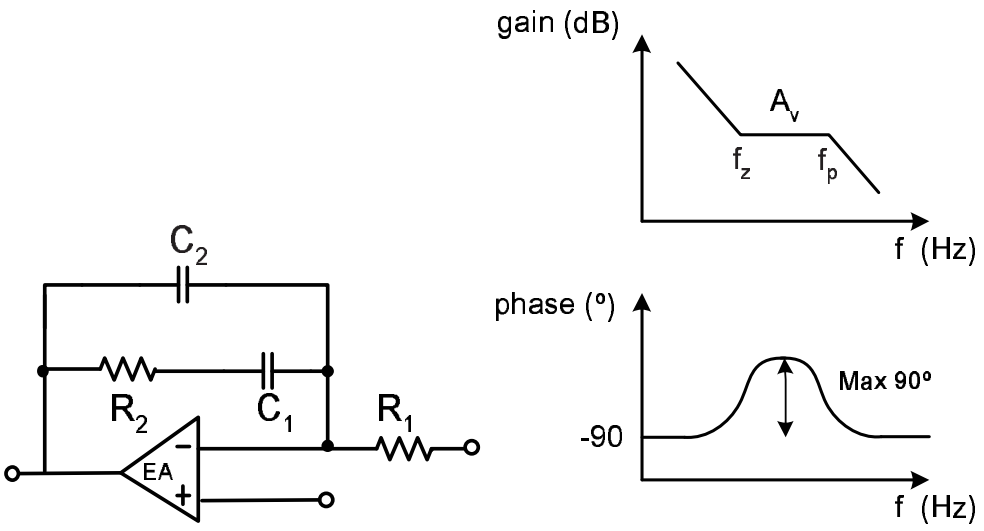


Figure 5.28: Proposed frequency synchronized boost converter.



(a) (b)

Figure 5.29: Type II error amplifier. (a)Configuration. (b)Gain and phase versus frequency characteristics

The compensation network used in the regulator is a type II error amplifier compensation [7]. Circuits and frequency responses are shown in Fig. 5.29. The locations of the zero and pole are:

$$f_z = \frac{1}{2\pi \times R_2 \times C_1} \tag{5.50}$$

$$f_p = \frac{1}{2\pi \times R_2 \times C_2} \tag{5.51}$$

and mid-frequency voltage gain, A_V, is:

$$A_V = \frac{R_2}{R_1} \tag{5.52}$$

A pole at the DC creates high gain at low frequencies. The gain is Z_{C_1}/R_1. Thus, power line 120-Hz ripple is attenuated down to a very low level at the output. In the mid-frequency range where the impedance of C_1, Z_{C_1} is small compared to R_2 and ZC_2 is large compared to R_2, the gain slope is flat and equals to R_2/R_1. At higher frequencies where Z_{C_2} is small compared to R_2, the gain is Z_{C_2}/R_1.

The type II error amplifier gains some phase boost in the frequency between the pole and zero. Therefore, the crossover frequency of total open-loop gain is usually placed here to obtain good phase margin. The farther apart f_z and f_p are, the greater the phase margin. However, if f_z is chosen too low, low-frequency gain will be lower at 120 Hz. As a result, 120 Hz attenuation will be poorer. If f_p is chosen too high, gain at high frequencies is higher. Thus, high-frequency noise spikes would come through at higher amplitude. A compromise between good phase margin, better 120Hz attenuation, and lower high-frequency noise spike must be made.

The sequence of designing a loop is first to establish the crossover frequency, f_c, where the total open-loop gain should be 0 dB. Then choose the error-amplifier gain so that the total open-loop gain is forced to be 0 dB at the frequency. Next, design the error-amplifier gain slope so that the total open-loop gain comes through f_c at a -20 db/dec slope. Finally, tailor the error-amplifier gain versus frequency so that the desired phase margin is achieved.

Sampling theory shows that f_c must be less than half the switching frequency for the loop to be stable. However, it must be considerably less than that to attenuate large-amplitude switching frequency ripple at the output. Thus, the usual practice is to fix f_c at one-tenth the switching frequency.

5.3.5 Design Considerations

Similar to the voltage-mode ripple control regulator, there are also some prerequisites for the proposed technique to work properly. Design considerations are investigated for the fixed frequency current-mode ripple control (CMRC) boost regulator.

Filter Capacitor

The filter capacitance in a switching power supply is generally selected to limit output voltage ripple within the specified level. The series impedance of the capacitor and the output current determines the output voltage ripple. As described in the previous section, the three elements of the capacitor that contribute to its impedance are ESR, ESL, and capacitance.

In a voltage-mode ripple control regulator, the output ripple is monitored to trigger switching operations. As a result, ESR and ESL are two key factors to determine the switching frequency. However, in a current-mode ripple regulator, the inductor current ripple is monitored instead of the output voltage ripple. The output voltage ripple no longer affects the switching frequency. Thus, the only consideration for choosing the filter capacitor is to meet the output voltage ripple level.

The output voltage change due to the capacitor's capacitance is usually assumed negligible. For this assumption to be true, the filter capacitance must satisfy the following equation:

$$C \gg \frac{I_{out(\max)} \times D_{\max}}{f_{SW} \times \Delta V_{out}} \tag{5.53}$$

where $I_{out(\max)}$ is the maximum output current and $D_{\max}$ is the maximum duty ratio. Because the filter capacitor supplies the entire load current during the on time, sufficient capacitance keeps output voltage within tolerance under maximum output current and maximum duty ratio. In many cases, to get sufficiently low ESR, capacitors with much more capacitance than needed are selected.

Typical output voltage and inductor current waveforms of the boost converter are

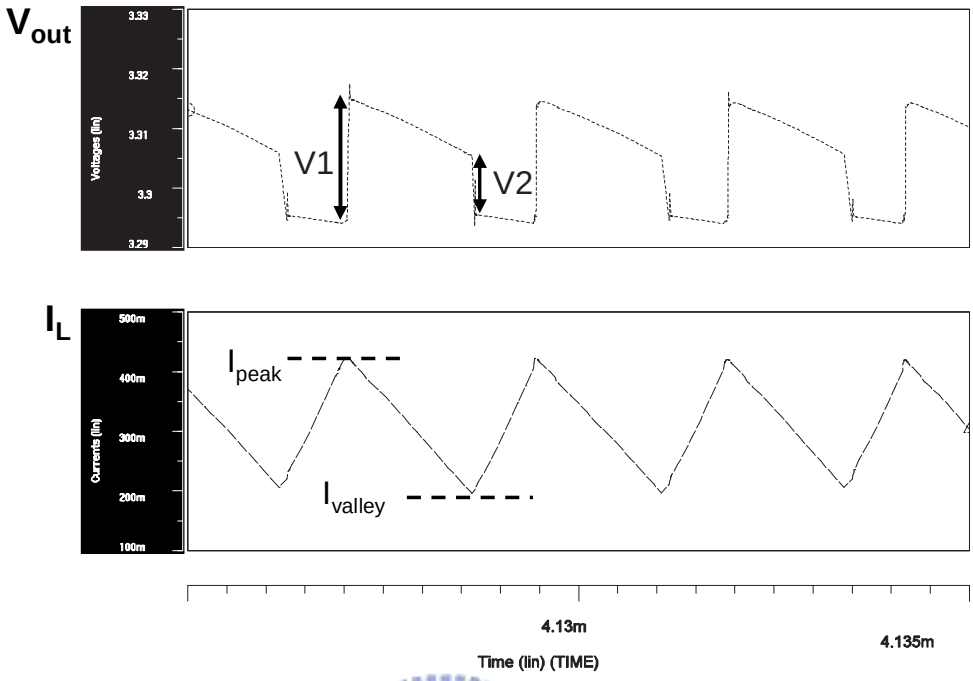


Figure 5.30: Output voltage and inductor current waveforms of the boost converter.

shown in Fig. 5.30. The ESL is removed from the circuit for simplicity. The output voltage ripple is mainly caused by the ESR. During the on time, the capacitor supplies the load current. The current flowing through the capacitor's ESR develops a voltage drop, $-I_{out} \times r_C$. During the off-time, the voltage drop is $(I_L - I_{out}) \times r_C$. Thus,

$$\begin{aligned} V1 &= r_C \times I_{peak} \\ V2 &= r_C \times I_{valley} \end{aligned} \tag{5.54}$$

From the above equations, we find that the output ripple relates to the inductor current and ESR. Thus, the maximum ESR needed to limit the ripple within ΔV_{out} is:

$$r_C \leqslant \frac{\Delta V_{out}}{\left(\frac{I_{out(\max)}}{1-D_{\max}} + \frac{\Delta I}{2}\right)} \tag{5.55}$$

ESL can cause large output ripple and must be reduced. This can be done by choosing low ESL capacitors or replacing one large device with several smaller ones in parallel.

Filter Inductor

The filter inductance must larger than the critical value that causes the circuit to operate at the edge of continuous conduction mode. At the edge of critical conduction, the average inductor current is equal to half of the inductor ripple current. In the boost power stage, the relationship of the average output current and the average inductor current is stated in Eq. 5.30. Therefore, from Eq.5.33, the minimum required inductance is obtained with a given minimum output current, $I_{out(\min)}$, and switching frequency:

$$\begin{aligned} L_{(\min)} &\simeq \frac{V_{IN}}{2 \times I_{out(\min)}} \times T_S \times D \times (1-D) \\ &\simeq \frac{(V_{out} + V_d - V_{IN})}{2 \times I_{out(\min)} \times f_{SW}} \times \left(\frac{V_{IN}}{V_{out} + V_d} \right)^2 \end{aligned} \tag{5.56}$$

In the current mode, the inductor current ripple is limited by the hysteretic window, ΔI. The maximum required inductance is determined by ΔI at a given switching frequency. With inductance larger than the maximum value, the inductor current cannot reach the hysteretic window within the required time. From Eq. 5.44, the relationship is expressed below:

$$\Delta I \geqslant A \times \left[t_{on} - t_D \times \left(1 + \frac{B}{A} \right) \right] \tag{5.57}$$

where $t_{on} = T_S \times D$, A and B are expressed in Eqs. 5.42 and 5.43. From the above equation, we obtain the maximum inductance:

$$\begin{aligned} L_{(\max)} &\simeq \frac{V_{IN}}{\Delta I} \times T_S \times D - \frac{V_{out} + V_d}{\Delta I} \times t_D \\ &\simeq \frac{V_{IN} \times (V_{out} + V_d - V_{IN})}{\Delta I \times f_{SW} \times (V_{out} + V_d)} - \frac{V_{out} + V_d}{\Delta I} \times t_D \end{aligned} \tag{5.58}$$

If t_D is much smaller than $T_S \times D$, then the above equation is simplified as below:

$$L_{(\max)} \simeq \frac{V_{IN} \times (V_{out} + V_d - V_{IN})}{\Delta I \times f_{SW} \times (V_{out} + V_d)} \tag{5.59}$$

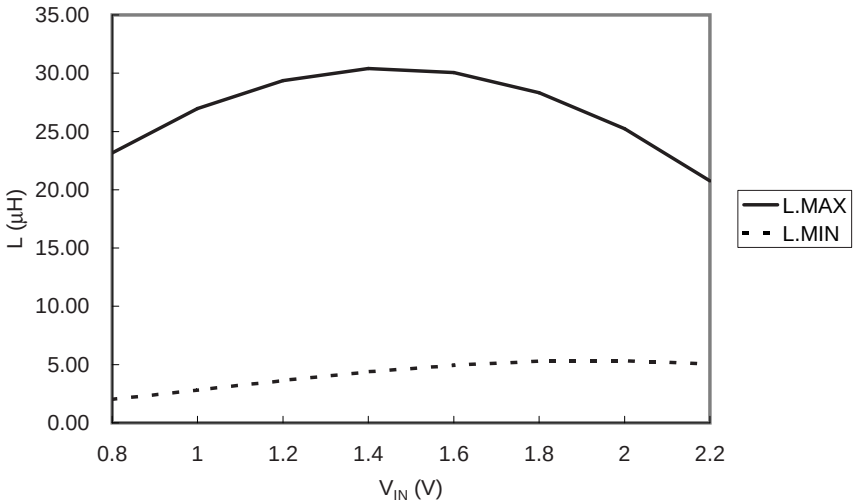
Note that the minimum and the maximum inductance values are determined by $I_{out(\min)}$ and ΔI respectively at a given frequency. Divide Eq. 5.59 by Eq. 5.56, we obtain a ratio of maximum-to-minimum allowable inductance:

$$\frac{L_{(\max)}}{L_{(\min)}} = \frac{2 \times I_{out(\min)}}{\Delta I \times (1-D)} = \frac{2 \times I_{out(\min)} \times (V_{out} + V_d)}{\Delta I \times V_{IN}} \tag{5.60}$$

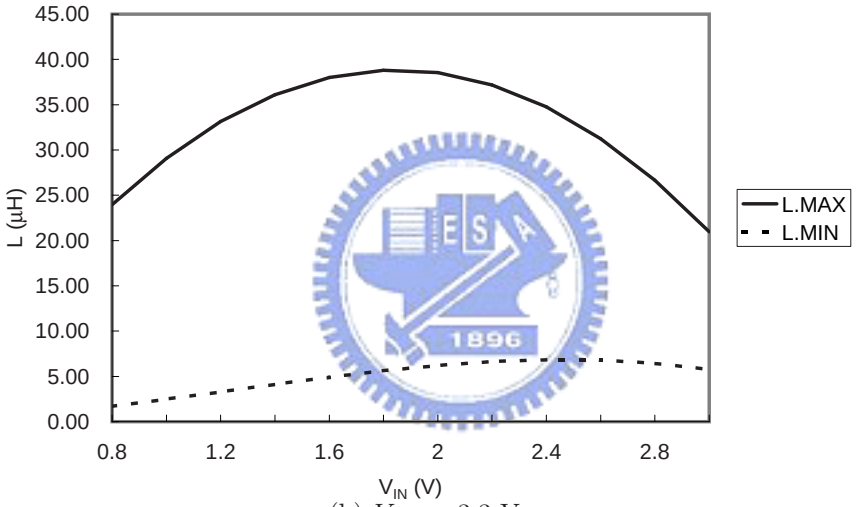
This inductance ratio is independent of the switching frequency and is adjustable by changing ΔI. A wide range of allowable inductance provides more selection of the inductor and safety against component variations. Although decreasing ΔI increases the inductance ratio, noise may interference normal operations of the hysteretic comparator with a small ΔI. Also note that the inductance ratio becomes smaller with a small V_{out}-to-V_{IN} ratio.

Assume t_D = 200 ns, ΔI = 0.1 A, V_d = 0.4 V, $I_{out(\min)}$ = 200 mA, Figures 5.31 to 5.33 plot the required maximum and minimum values of the filter inductor at different switching frequencies.

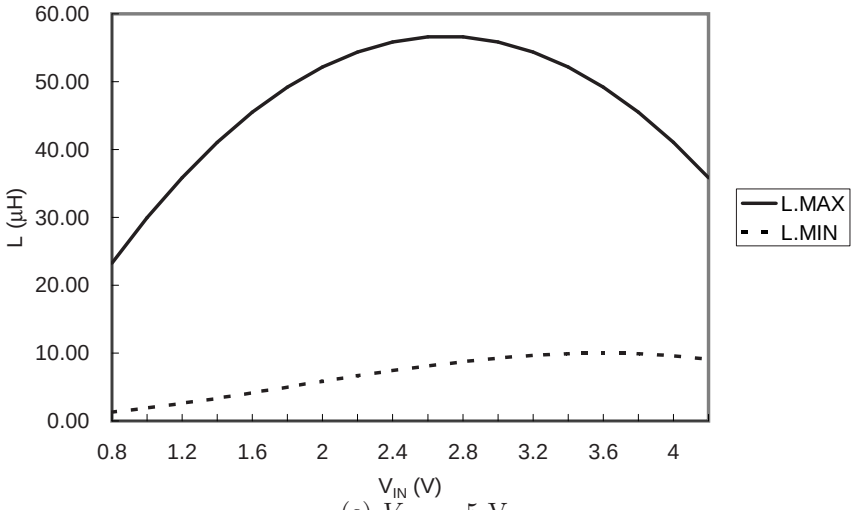
The choice of inductance must between the lowest maximum value and the highest minimum value within the possible input voltage range at the specified switching frequency. Although the inductance ratio is almost independent of the switching frequency, the differences between maximum and minimum inductance are smaller at higher frequencies. It will be difficult to choose appropriate inductors. As a result, smaller ΔI is required at high frequency. A proper choice of input voltage with respect to the specified output voltage also relaxes the inductance restrictions. Extremely high or low V_{out}-to-V_{IN} ratio usually offer few inductance choices. For example, 2.5 V output is suitable for input voltage as low as 0.8 V. On the other hand, input voltages lower than 1.2 V is not suitable to a 5 V output.



(a) $V_{out} = 2.5$ V.

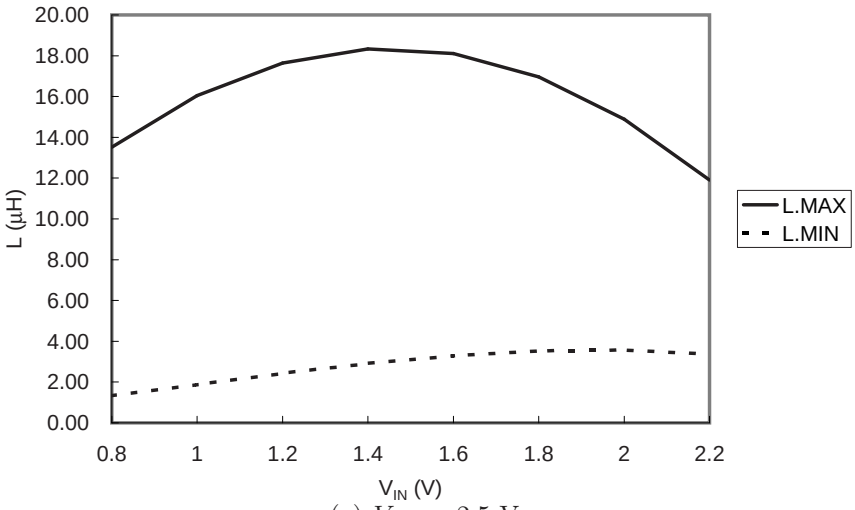


(b) $V_{out} = 3.3$ V.

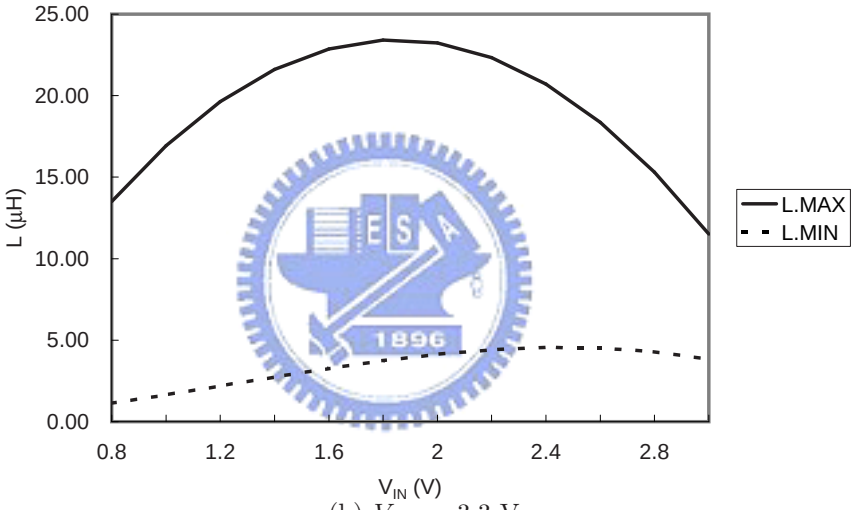


(c) $V_{out} = 5$ V.

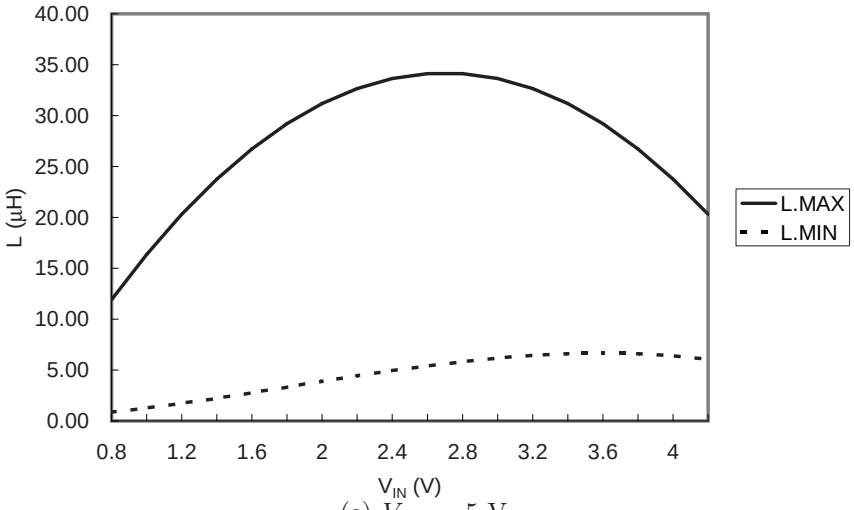
Figure 5.31: Required filter inductance at 200 kHz.



(a) $V_{out} = 2.5$ V.

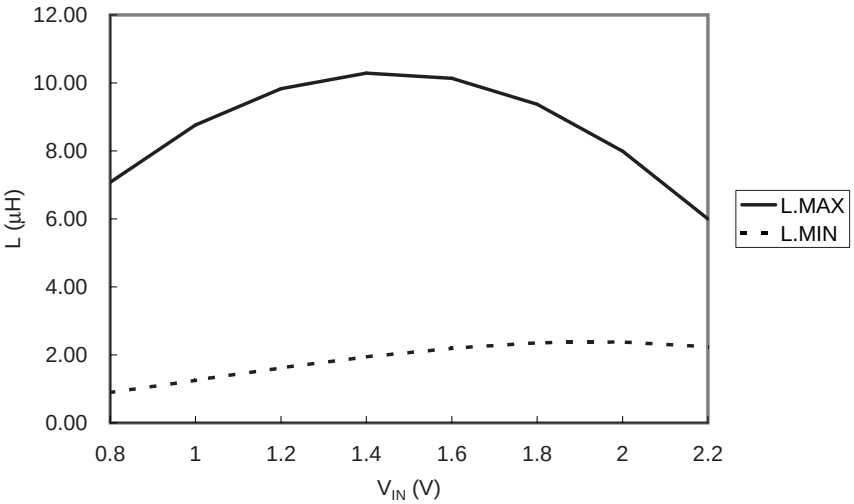


(b) $V_{out} = 3.3$ V.

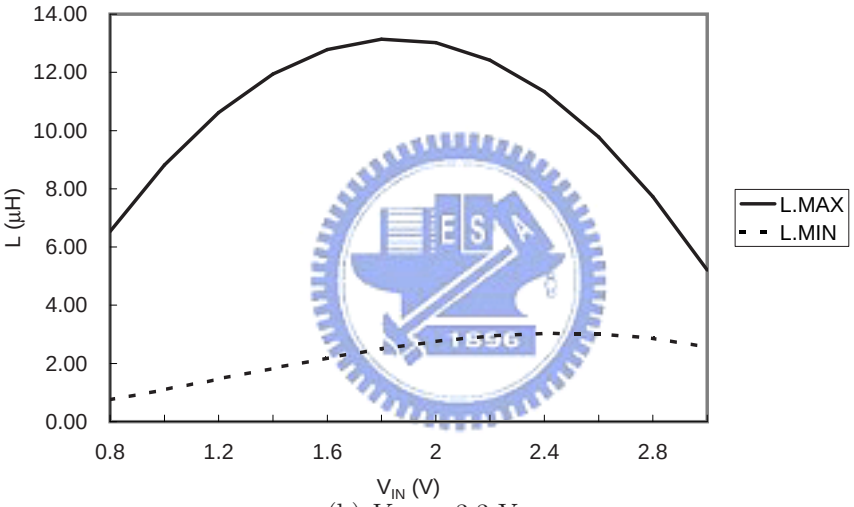


(c) $V_{out} = 5$ V.

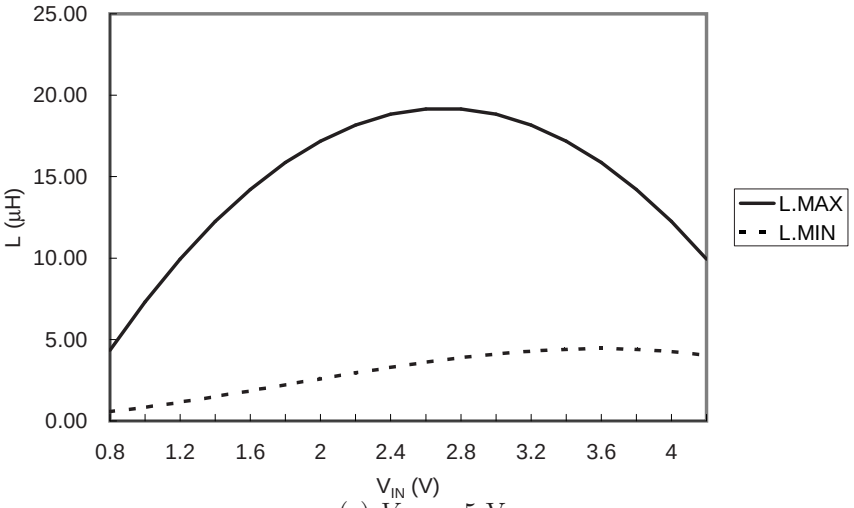
Figure 5.32: Required filter inductance at 300 kHz.



(a) $V_{out} = 2.5$ V.



(b) $V_{out} = 3.3$ V.



(c) $V_{out} = 5$ V.

Figure 5.33: Required filter inductance at 450 kHz.

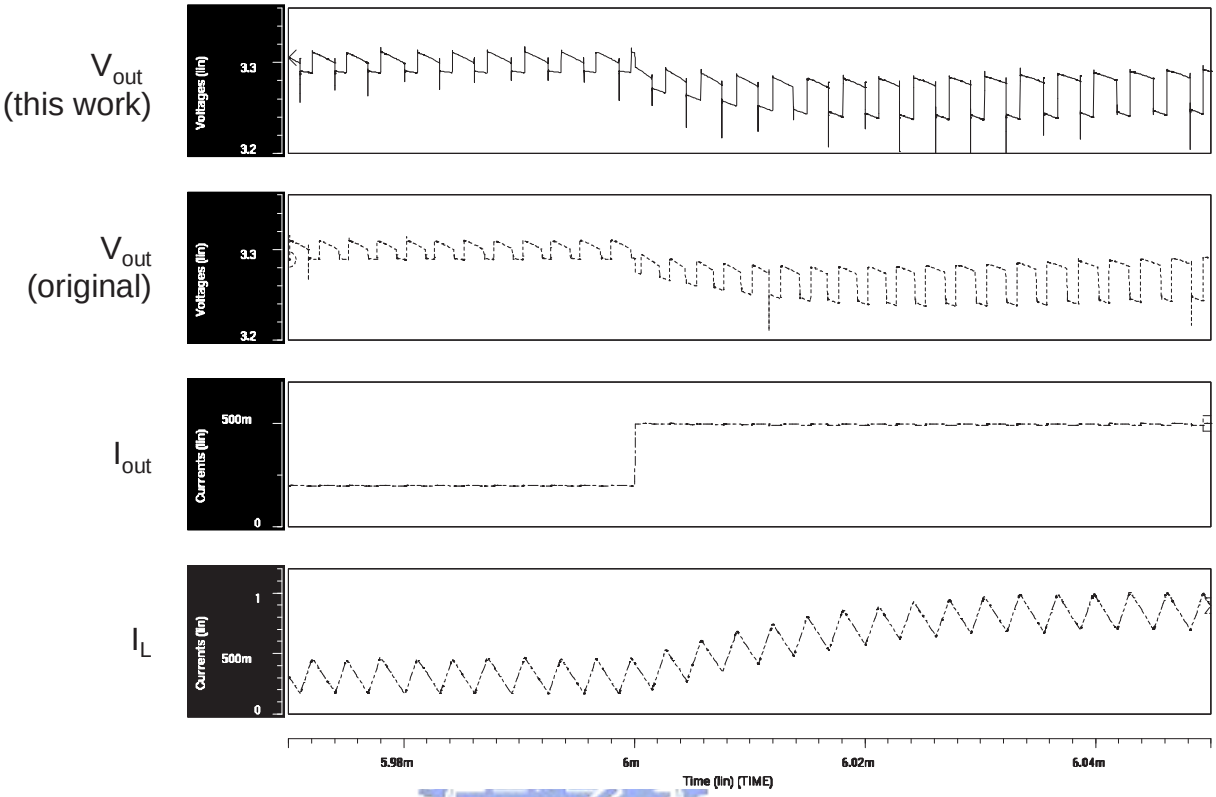


Figure 5.34: Load transient responses: Comparison of the proposed with an original CMRC boost regulator.

5.3.6 Simulation Results

Proposed current-mode ripple control boost regulator shown in Fig. 5.28 was simulated using SPICE. Parameter values are listed in Table 5.5. Output voltage is 3.3 V and input voltage is 2.4 V which is nominal voltage of a two-cell NiMH battery. Figure 5.34 shows the output voltage and the inductor current waveforms during a load transient. The output current stepped from 200 mA to 500 mA. For comparison, output voltage of an original varying-frequency CMRC boost regulator is also presented. The original CMRC boost regulator refers to that shown in Fig. 5.25. In steady state, the switching frequency was locked at 300 kHz. During the load transient, both regulators exhibited fast transient

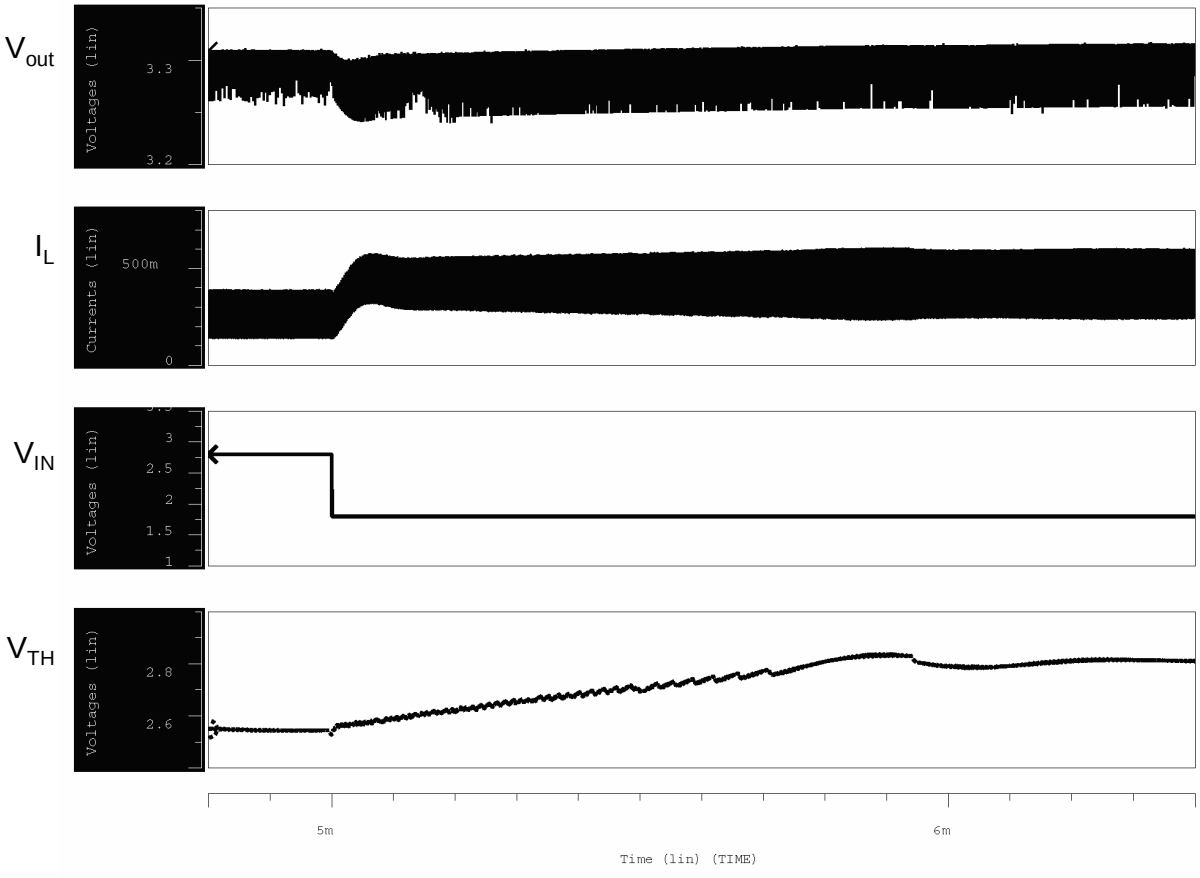


Figure 5.35: Line transient response of proposed CMRC boost regulator.

response. The output voltage swing increased after the load transient because it is the product of capacitor ESR and output current, $r_C \times I_{out}$. A decrease in average output voltage occurs with the increase in load current because of the finite gain of the error amplifier. Thus, load regulation is 0.96 %/A from simulation. Refer to Eq. 5.48 and 5.49, load current affects little on switching frequency. Therefore, even the original CMRC regulator varied slightly in switching frequency.

Battery voltage range of a two-cell NiMH battery is from 2.8 V (fully charged) to 1.8 V (depleted). Thus, the input voltage is gradually decreasing while the system is operating. The original ripple regulator may encounter varying switching-frequency problem in

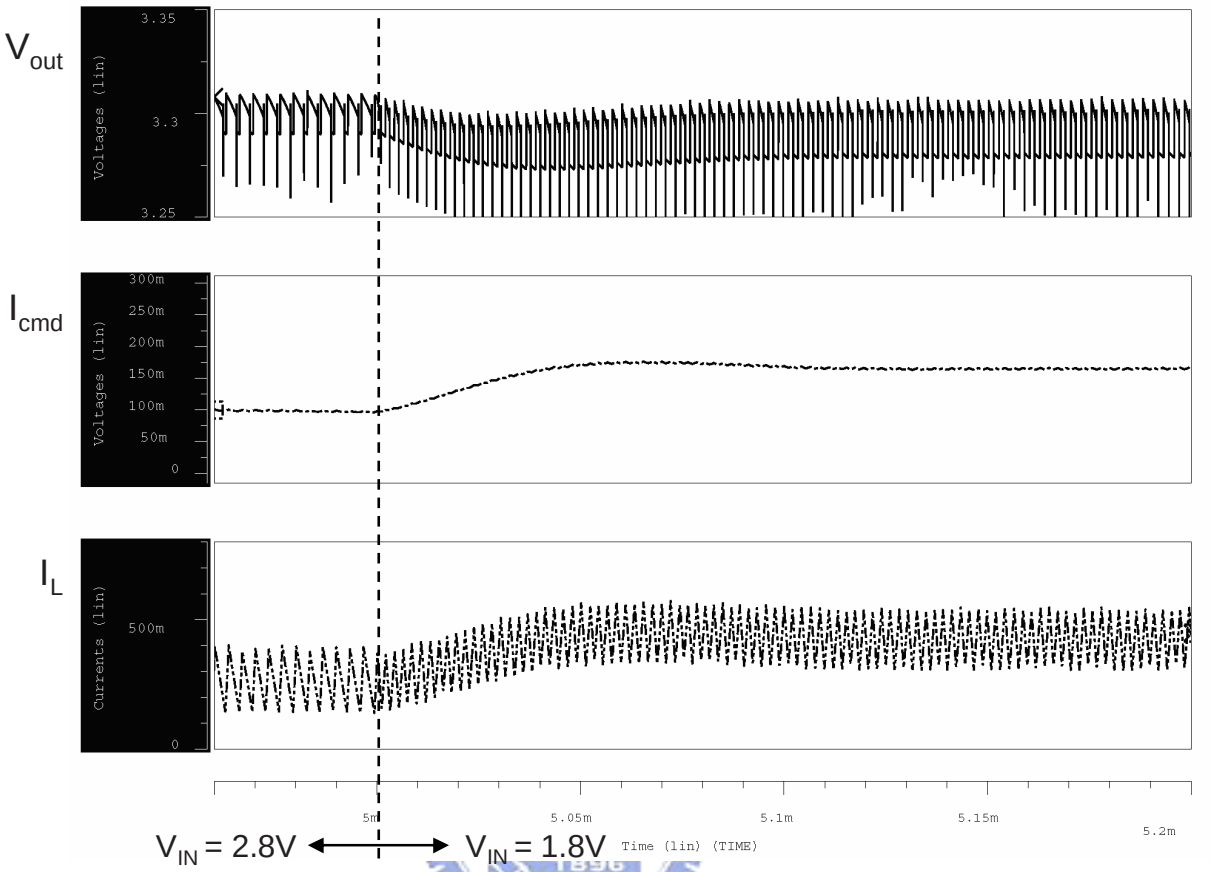


Figure 5.36: Output Voltage, current command, and inductor current waveforms during line transient.

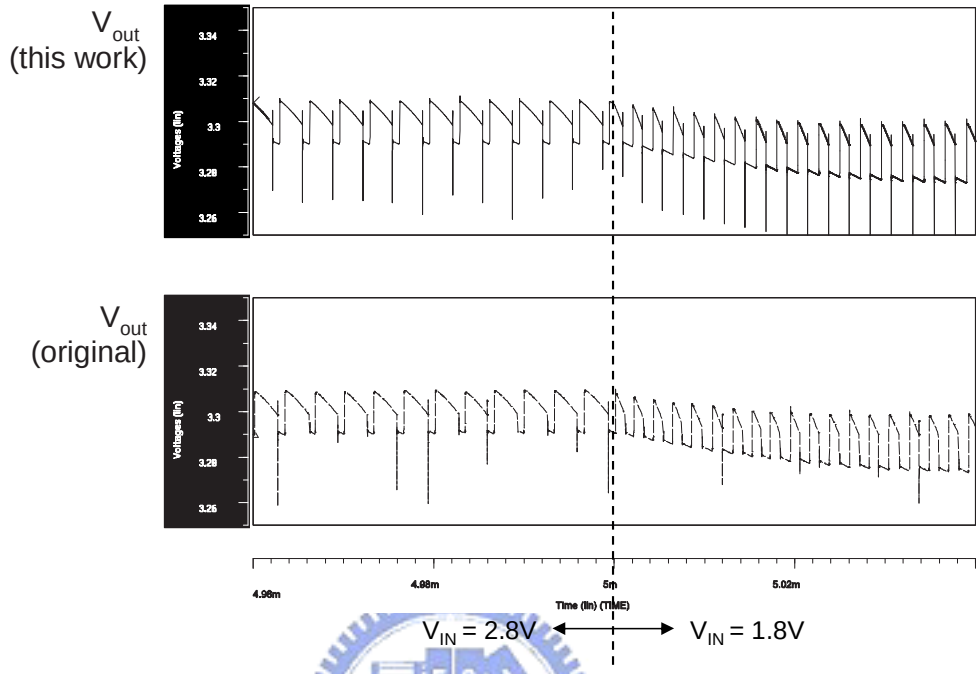
battery-powered systems. Simulated line transient waveforms of the proposed regulator are shown in Fig. 5.35. Waveforms of V_{out}, I_L, V_{IN}, and threshold voltage of the delay element, V_{TH}, are shown from top to bottom. Larger V_{TH} represents more delay is add to the loop. V_{IN} dropped from 2.8 V to 1.8 V at t = 5 ms. Zoomed waveforms are also shown in Fig. 5.37. The ripple control regulator exhibited excellent line transient response because the decrease in V_{IN} instantly affects the up and down slopes of the inductor current. Therefore, the duty ratio immediately responses the change in V_{IN}. Refer to Eq.5.30, the inductor current, I_L is inversely proportional to $(1 - D)$ if I_{out} is

unchanged. Thus, I_L was increased after the line transient because duty ratio, D, was increased. Since I_L is controlled by the current command, I_{cmd}, generated by the error amplifier, average of V_{out} also dropped because the I_{cmd} was increased. Their waveforms are shown in Fig. 5.36. As a result, the average value of V_{out} changed with V_{IN}, which is interpreted as line regulation. Line regulation is 0.75 %/V according to the definition in Eq. 2.4.

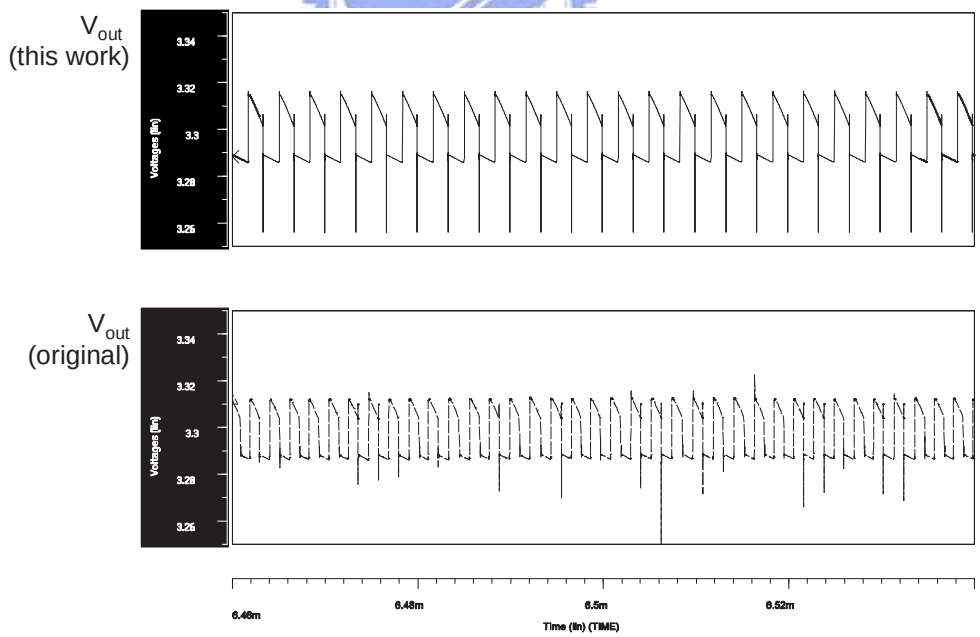
Referring to Fig. 5.27, switching frequency is higher when $V_{IN} = 1.8$ V than 2.4 V with the same delay. To maintain a fixed switching frequency, V_{TH} in Fig. 5.35 was increased by the phase-locked loop. To verify the effectiveness of the phase-locked loop, Figure 5.37 compares the switching frequency with an original CMRC regulator under different input conditions. No extra delay is inserted besides internal system delay. Before the line transient shown in Fig. 5.37(a), the switching frequencies of the proposed fixed-frequency regulator and the original regulator were equally 300 kHz. After the line transient from 2.8 V to 1.8 V, both immediate switching frequencies were increased to 455 kHz. After 1.5 ms, the control loop had already entered steady state. As Fig. 5.37(b) shows, switching frequency of proposed regulator had come back to 300 kHz, but it was still 455 kHz for the original regulator.

5.4 Summary

Methods and circuits for achieving fixed output frequency operations of ripple control buck and boost regulator have been presented. Switching frequency of conventional ripple control regulators is a function of circuit delay, ESR of the output capacitors, and many other parameters. The proposed control loop adjusts delay of the controller and



(a) During the line transient.



(b) 1.5 ms after the line transient.

Figure 5.37: Switching frequency comparison between proposed and an original CMRC boost regulator during line transient.

Table 5.5: Parameters used in CMRC boost regulator.

Output voltage, V_{out}	3.3 V
Input voltage, V_{IN}	2.4 V
Reference voltage, V_r	1.2 V
Output current, I_{out}	200–500 mA
Filter inductor, L	8.2 μH
Filter capacitor, C	100 μF
DCR of inductor, r_L	0.1 Ω
ESR of capacitor, r_C	50 mΩ
On-state resistance of MOSFET, R_{ON}	20 mΩ
Input clock frequency, f_{clk}	300 kHz
Diode forward voltage, V_d	0.4 V
CSA gain	5
Inductor current hysteresis, ΔI	0.2A
Current-sense resistor, R_S	80 mΩ
Compensation resistor, R_1	2.1 kΩ
Compensation resistor, R_2	11 kΩ
Compensation capacitor, C_1	80 nF
Compensation capacitor, C_2	2 nF

thus controls the output frequency. This is done by using a PLL to lock the frequency of the switching signal with the input clock. A linear model of the PLL has been derived for stability analysis. Simulation results showed the proposed method provides the ripple regulator a fixed frequency operation. Good load/line transient response and tight regulation were also observed from simulation.

Chapter 6

Conclusions and Future Works

6.1 Conclusions

In this dissertation, several high performance control topologies for switching DC–DC converters are addressed. Besides the high efficiency and high power packing density nature of switching regulators, proposed regulators have achieved the goals of fast response, tight regulation, high stability, fixed frequency, and compact system structure. Applications of these voltage regulators cover from voltage regulating module for desktop CPUs or battery powered notebook CPUs to portable devices. Voltage conversions of these regulators include step-down conversion, low output-to-input ratio step-down conversion, and step-up conversion.

A digital control topology of PWM DC–DC converter using proportional current feedback is presented. Proposed control loop retains the advantages of voltage-mode control, but has the fast load transient response like the current-mode control. Novel A/D converter structure and control law realization greatly reduce system complexity. The control circuit is implemented in a digital process for verification. Simulation and experimental results show that the output voltage dropped 150 mV and recovered to static tolerance in

100 μs as the output current rose from 2 A to 20 A. The experimental results agree with that from the behavioral model. Its dynamic response has been shown to meet the power requirements of current applications with minimum hardware. This compact controller is a competitive choice to current mode control and a better solution in system integration.

Two common free-running control topologies, ripple control and constant on-time control, are investigated. Circuits architectures are proposed to improve these controllers. Switching frequency of the constant on-time regulator is stabilized by adjusting the on time according to input and output voltage. Noise on the feedback signal interferes with normal operations of the comparator. Unstable operation is observed at the output. Instability can be also predicted from loop gain of the free-running control. A novel compensation circuit was proposed to improve the frequency response and noise immunity of constant on-time control. This compensation circuit uses a built-in integrator to generate a ramp signal to trigger the comparator. Therefore, it is less susceptible to noise. Stable operation and fast response are obtained. Experiment and simulation results showed fast response during load and line transients. Efficiency from 87 % to 93 % is obtained over a load range from 10 mA to 3 A with 5 V input and 2.476 V output. The load and line regulations are 0.032 %/A and 0.034 %/V, those are superior to conventional current-mode and voltage-mode PWM control. Low switching noise and low output ripple make proposed regulator suitable for low voltage applications.

Methods and circuits for achieving fixed output frequency operations of ripple control buck regulator have been presented. Ripple control is well known for wide conversion range and fast response. However, switching frequency of conventional ripple control regulators

is a function of circuit delay, ESR of the output capacitors, and many other parameters. Varying switching frequency can cause EMI problem in a system. The proposed control loop locks the frequency of switching signal with the input clock by using a phase-locked loop. Circuit design and PLL analysis were presented. Simulation results showed the proposed method provides the ripple regulator a fixed frequency operation without any instability problem under a very low V_{out}/V_{IN} condition that is difficult for conventional PWM controllers. Load regulation is 0.046 ‰/A and line regulation is 0.028 %/V.

For portable devices, input voltage provided by the batteries may vary significantly from 0.9 V to 4.2 V for different cells from fully charged to depleted. Chip supply voltage in a portable device is often optimized for efficiency. Therefore, the battery voltage needs be converted to chip supply voltage. The boost converter is used to perform this step-up conversion. From the small-signal analysis of the boost converter, RHP zero exists in the control-to-output transfer function. Therefore, current-mode ripple control is more suitable for the boost converter. The current-mode ripple control monitors and controls the inductor current. The tightly-controlled inductor current effectively eliminates the inductor in the transfer function. However, proper error-amplifier compensation is still required. This dissertation provides a procedure to design the control loop of the current-mode ripple control boost controller. Simulation results showed fixed frequency operation and fast load/line transient responses. Load regulation is 0.96 %/A and line regulation is 0.75 %/V.

6.2 Future Works

In this dissertation, several prototypes have been developed to realize proposed control techniques. However, there are some efforts to do for better system performance: (1) Interleave topology may increase current capability and transient response; (2) An offset reduced comparator and error correction technique can improve the accuracy of the A/D converter; (3) Integration of digital and driver circuits into the control chip will improve efficiency. Tapped delay line scheme for digital PWM generation is also a possible solution to increase efficiency but at the cost of more chip area [32]; (4) Feasible circuit implementation techniques are proposed in this dissertation to build fixed frequency ripple regulators. Further verification can be made on the silicon; (5) Because the current-mode ripple controller must sense the inductor current during the whole switching cycle. A resistor is placed in series with the inductor, which reduces efficiency. Current sense technique without this sensing resistor is a possible way to improve the efficiency; (6) High switching frequency can further reduce component size and accelerate transient response. Improvements on power MOSFET technology is the key to increase switching frequency.

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論文題目：應用於切換式直流至直流轉換器之高性能互補金氧半控制器

HIGH PERFORMANCE CMOS CONTROLLERS FOR SWITCHING-MODE DC–DC CONVERTERS

著　作　：(如後附頁)


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Publication List

(A) Regular Journal Paper

Chung-Hsien Tso and Jiin-Chuan Wu, "Analysis and Implementation of Proportional Current Feedback Technique for Digital PWM DC–DC Converters," *IEICE Transactions*, vol.E86-C, no.11, pp.2300–2308, Nov. 2003.

(B) Brief Journal Paper

Chung-Hsien Tso and Jiin-Chuan Wu, "A Ripple Control Buck Regulator with Fixed Output Frequency," *IEEE Power Electronics Letters*, vol.1, no.3, pp.61–63, Sept. 2003.

(C) International Conference Paper

1. **Chung-Hsien Tso** and Jiin-Chuan Wu, "An Integrated Digital PWM DC/DC Converter," *IEEE ICECS 2000*, vol. 1, 2000, pp.104–107.
2. **Chung-Hsien Tso** and Jiin-Chuan Wu, "An Integrated Digital PWM DC/DC Converter Using Proportional Current Feedback," *IEEE ISCAS 2001*, vol. 3, 2001, pp.65–68.