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碩士論文

低溫複晶矽薄膜電晶體
其遷移率與可靠度之研究

Study on the Mobility and Reliability of Low Temperature Poly-Si Thin-Film Transistors

研 究 生：徐源竣

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摘　要

在本論文中，首先，我們研究利用氮化矽層去覆蓋複晶矽薄膜電晶體的新式結構。我們發現與傳統複晶矽薄膜電晶體相較之下，有著氮化矽覆蓋層的複晶矽薄膜電晶體有較好的電特性。我們提高了導通電流及場效遷移率，這是因為氮化矽覆蓋層在通道中造成張力還有降低源極/汲極的串聯電阻。再者，氮化矽覆蓋層的複晶矽薄膜電晶體也抑制了扭曲效應 (Kink effect)，閘極引發汲極漏電(GIDL)，還有改善了可靠度，這是因為此種新式結構薄膜電晶體可以降低橫向電場。

接著，我們進行有關 P 型通道之多重通道(multi-channel)複晶矽薄膜電晶體的研究。此種元件的電特性如導通電流，臨界電壓(threshold voltage)及次臨限擺幅(subthreshold swing) 會隨著通道條數變多而被改善，這是因為我們提高了有效的通道寬度和加強了閘極的控制能力。而元件的可靠度也會隨著通道條數增加而被改善，這是因為在多重通道結構下加強了閘極的控制能力。

最後，我們探討有關複晶矽薄膜電晶體生命週期(lifetime)的問題。發現到最

糟的熱載子應力測試條件跟元件的通道長度有相關性。在短通道元件中，最糟的熱載子應力測試條件是閘極電壓等於臨界電壓而非傳統上閘極電壓等於二分之一汲極電壓。此外，導通電流退化的情形在高和位的汲極應力測試下的不同的現象。這是因為在薄膜電晶體中不僅碰撞游離(impact ionization)還有寄生雙極性接面電晶體效應(parasitic bipolar junction transistor effect)去造成元件的退化。我們亦發現當在粹取複晶矽薄膜電晶體之生命週期時與金屬氧化層場效電晶體有著不同的現象，在一大範圍的汲極電壓應力測試下有著兩種斜率的生命週期投射現象。

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ABSTRACT

In this thesis, first, we studied the new structure of poly-Si TFTs with capping silicon nitride passivation layer. It was found that this device have better electrical characteristic than convention poly-Si TFTs. We enhanced electron mobility and on current due to local tensile strain in the channel and low source/drain series resistance. Moreover, the proposed poly-Si TFTs also suppressed kink effect, effect of gate induced drain leakage (GIDL) and improved reliability due to low horizontal electric field in this new structure of poly-Si TFTs.

Then, p-channel poly-Si TFTs with multi-channel structure were studied. The device's electrical characteristic such as on-current, threshold voltage, and subthreshold swing were improved with increasing the channel stripes due to the increasing effective channel width and enhancement of gate control capability. The reliability of proposed poly-Si TFTs were improved with increasing the stripes of channel. This is due to better gate control capability in multiple channel structure.

Finally, we studied the lifetime issue of poly-Si TFTs. It was found that the

worst-case of stress condition depend on device channel length. In short channel device, the worst-case of stress condition is under $V_G \approx V_{th}$, not $V_G=1/2\ V_D$. Moreover, I_{on} degradation under both high and low V_D of stress conditions has different phenomena. This is due to not only impact ionization but also parasitic bipolar junction transistor effect to degradation poly-Si TFTs. Then, it is found that lifetime extraction of poly-Si TFTs is not the same with that of MOSFETs. There are dual slop lifetime projections in wide drain voltage.

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Chapter 1

Introduction

1.1 Overview of Low Temperature Poly-Si Thin-Film Transistors

The study of polycrystalline silicon (poly-Si) thin film transistors (TFTs) fabricated using a maximum temperature below 600C commenced in 1980s. We defined this kind of poly-Si TFTs as Low temperature polysilicon thin film transistors (LTPS-TFTs) . It have received much attention in recent years because of their applications , such as active matrix liquid crystal displays (AMLCDs) [1-3] , active matrix organic light emitting displays (AMOLEDs) [4-6] , high density static random access memories (SRAMs) [7], electrical erasable programming read only memories (EEPROM) [8][9] and candidate for 3-dimenstion ICs' applications [10] . Within those applications, the application of active matrix liquid crystal displays (AMLCDs) is the major driving force to promote the developments of poly-Si TFT technology .

The first generation of active matrix liquid crystal displays (AMLCDs) used a-Si:H TFTs for the pixel switching device. The advantages of a-Si:H TFTs are their compatibility with low processing temperature on large-area glass substrates and low leakage current due to the high off-stated impedance. However , the low electron field-effect mobility(<1 cm2/Vs) has limited the development of AMLCDs technology. So , the poly-Si TFTs acted important role for AMLCDs development , because the high field effect mobility and the high driving current of poly-Si TFTs makes the integration of switching pixels and driver circuits possible [11]. Moreover, the aperture ratio and the panel brightness can be also greatly promoted due to small

device size needed using poly-Si TFTs [12]. Therefore, the performance of display can be significantly improved. As a result, ploy-Si TFTs have a great potential to realized high-performance large-area AMLCDs applications, and further to accomplish System-on-Panel (SOP).

As compared with single crystalline silicon, the polycrystalline Silicon may consist of many grains, whose boundaries are composed of unsatisfied dangling silicon bonds that may trap charge carriers and become charged. This results in the formation of potential barriers between grains and also between the grain interior and its boundary [13]. The major effect of grain boundaries and intra-grain defects on the electrical performance of a TFT results from lowering the carrier mobility. This results in a degradation of drive current and subthreshold swing , and increases the threshold voltage, leakage current, and the temperature dependence of the device[13][14]. In order to obtain desirable electrical characteristics of poly-Si TFTs , several methods have been proposed to improve the device performance by enlarging the grain size of poly-Si films[15][16] and reducing the trap states in grain boundaries . Many crystallization techniques have been proposed to achieve low temperature polycrystalline silicon (LTPS) TFTs , such as SPC (solid phase crystallization)[17] , ELA (excimer laser annealing)[18][19] and MILC (metal induced lateral crystallization)[20]. Plasma treatments is also a method for reducing trap states in grain boundaries, various plasmas such as H_2 [21], NH_3 [22], N_2O[23] and O_2 plasmas [24] have been intensely investigated in recent years.

Moreover, the device performance could also be improved by adopting novel device structures. Offset drain/source [25], Lightly doped drain (LDD) [26], gate overlapped LDD [27] , multiple channel structure [28] , Double or multiple gate structures [29], vertical channel [30] have been proposed and investigated intensively.

1.2 Motivation

In this thesis, we focus on the enhancement of mobility of poly-Si TFTs. This is because we want to gain higher on-current for AMLCD applications. Thus, the aperture ratio will be increased and then brightness will certainly increase. In recent years, the poly-Si TFTs have many applications which not only AMLCD but also 3-d circuit applications are very popular. We enhanced mobility of poly-Si TFTs can help system and circuit designer having wide window to design.

First, we have proposed that using nitride capping layer enhances mobility. It have been demonstrated that tensile strain in the channel will enhance electron mobility. Previous reports indicated that they applied mechanical stress on the wafer to test device and then observed electrical characteristics of tested device. It was found that tensile strain improves the electron mobility and the drain current of n-channel device including MOSFETs and TFTs [31][32]. On the contrary, Compressive strain reduced the electron mobility. It is well know that nitride layer has tensile stress. So, we want to utilize tensile strain of silicon nitride layer to forming compressively strained polysilicon gate electrode and then give a tensile stress on the channel [33]. Moreover, in mainstream CMOS technology, nitride spacer was used for reducing off-state leakage and improving the on-state drivability [34]. Because nitride spacer can induce electron to reduce resistance in offset region for improving the on-state drivability. Furthermore, the capping silicon nitride layer can reduce moisture incorporation. So, we proposed poly-Si TFTs with capping nitride layer to improve device performance.

Then, we proposed the p-channel poly-Si TFTs with multichannel structure. P-channel poly-Si TFTs have been used for many applications, such as low-power SRAMs [35], High-Resolution Active Matrix [36] and EEPROM's [37]. In circuit

design, CMOS technique is a very important technique. Because it have many advantage such as low power consumption, fully restored logic and better reliability. We would like realized CMOS technique by using TFTs device. So P-Channel and N-Channel TFTs are needed for integrated CMOS circuit. Moreover, the stability of p-channel polysilicon TFTs has not been investigated as much as n-channel polysilicon TFTs. So, we will discuss characteristic and reliability of P-Channel poly-Si TFTs in this thesis. It is well know that the characteristics of poly-Si TFTs are dominated by the large trap density in poly-Si film. When channel width scaled down, devices are reported to exhibit better performance such as lower threshold voltage and smaller trap density [38]-[40]. As a result, Poly-Si TFTs with narrow and multiple channels have been proposed to improve device performance [41][42]. Previous reports indicated that the existence regions near the poly-Si pattern edge where the grain boundary trap density is much smaller than elsewhere in the poly-Si film [38]. When channel width decreasing the effect of poly-Si pattern edge dominates and causes an effective trap density decreasing. Moreover, Due to the formation of active region island the gate electrode layer that climbs across the channel may induce side channels in both sides of the channel region. When channel width scaled down these side-channels become comparable to the main channel, accordingly increasing the effective channel width. Additionally, in CMOS technology, tri-gate [43] structure has been reported to exhibit superior gate control over the channel than a conventional single-gate MOSFET. Thus, we incorporate multi-channel with different channel widths, and tri-gate structure to achieve the high-performance and high reliability poly-Si TFTs. So, we proposed p-channel multichannel poly-Si TFTs and discussed characteristics and reliability of proposed poly-Si TFTs.

Finally, we focus on the reliability of poly-Si TFTs. It has been reported that the worst-case hot carrier degradation for conventional MOSFETs is under V_G=1/2 V_D

[44], and the device's degradation depends on the trap states generation, which are proportional to the I_{sub} [45]. This means that drain-avalanche-hot-carrier (DAHC) injection causes the severest damage on the device's characteristics. Therefore, DAHC-induced substrate current I_{sub} was used to monitor the device degradation and predict the device lifetime. However, it is known that the worst-case hot carrier degradation for SOI MOSFETs is under $V_G \approx V_{th}$ [46]. After hot-carrier stress, the degradation mechanism of the device was significantly different at both low and high drain bias [47][48]. They concluded that the parasitic bipolar transistors (PBT) might be the dominate factor to enhance the stressed current and also the device degradation rate. So, the lifetime of MOSFETs is unsuitable for SOI MOSFETs.

Poly-Si TFTs have received much attention in recent years because of their applications. Although, it have many studies to improve performance of poly-Si TFTs. However, the lifetime issues of poly-Si TFTs are not well studied. Because body contact is a lack of poly-Si TFTs, the floating body effect will influence the reliability of device. To date, there still does not exit a clear consensus on the hot-carrier effect of these devices compared to bulk. Therefore, in this thesis, we want to investigate the lifetime prediction of poly-Si TFTs, and the degradation mechanism at different drain bias under hot carrier stress.

1.3 Organization of the Thesis

In the following sections, we will show our research efforts.

In Chapter 2, the electrical characteristics and fabrication processes of low temperature poly-Si TFTs with silicon nitride capping layer will be proposed. Experimental results reveal that the performance and reliability of our devices have remarkable improvements in comparison with conventional TFTs. Additionally, we

make a detail discussion to explain the results of experimental.

In Chapter 3, the fabrication processes and electrical characteristics of p-channel ploy-Si TFTs with different stripes of channel will be proposed. Experimental results reveal that poly-Si TFTs with multiple channels have better performance and reliability than the conventional TFTs. Then, we will make a complete discussion about the electrical characteristics and reliability issue of poly-Si TFTs with multiple channels.

In Chapter 4, the reliability issue of poly-Si TFTs with different channel geometry will be investigated by applying different drain bias. It is found that I_{on} degradation under both high and low drain bias of stress conditions has different phenomenon. Then, we will analyze the degradation mechanism under hot carrier stress with wide drain voltage bias for the devices with different channel geometry.

At the end of this thesis, we will make a conclusion in Chapter 5.

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Chapter 2

Performance Enhancement of Low Temperature Polysilicon Thin Film Transistor with Silicon Nitride Capping layer

2.1 Introduction

In recent years, flexible electronics have been investigated and were paid attention, such as electronic paper, flexible display, sensor skin and electrotextiles. It required building electron device on flexible and deformable substrate [1]-[4]. Therefore, device will be stressed when operating flexible electronics. In this condition, mechanical strain is a major force to stress device.

There are many researches to comprehend effect of mechanical strain in device. In previous reported, they measured device characteristic when device under mechanical strain. it was found that tensile strain improves the electron mobility and the drain current of n-channel device including MOSFETs and TFTs [5][6]. On the contrary, Compressive strain reduced the electron mobility.

Recently, the strain-Si MOSFETs have become attractive for high speed complementary-metal-oxide-semiconductor (CMOS) device applications [7][8].the improvement of carrier mobility has been intensely studied by introducing strain in the channel region, such as strained-Si on SiGe substrate. However, the fabrication of the strained-Si devices is more complicated, such as forming a relaxed SiGe buffer layer. Previously studied indicated that uniaxial strained channel from contact etch stop silicon nitride (SiN) layer increase current drivability[9][10]. Because silicon

nitride layer has tensile strain and further forming compressively strained polysilicon gate electrode and then give a tensile stress on the channel.

In this chapter, we fabricated poly-Si TFTs with capping silicon nitride layer to created a tensile stress on the channel. It was found that this device have better electrical characteristic than convention poly-Si TFTs. We enhanced electron mobility and on current due to local tensile strain and low source/drain series resistance and then suppressed kink effect, gate induced drain leakage(GIDL) effect and improved reliability due to low horizontal electric field in Capping Nitride poly-Si TFTs. We will make a detail discussion in later section.

2.2 Device Fabrication

Figure 2-1 show the process flow and cross-sectional view of the investigated poly-Si TFT. First, 500-nm-thick thermal oxide was grown on the Si wafer by using a furnace system. All the experimental devices in this study were fabricated on thermally oxidized Si wafers. Then, 50-nm-thick amorphous silicon layers were deposited on the thermal oxide layer using a low-pressure chemical vapor deposition (LPCVD) system at 550°C. Then, amorphous silicon films were recrystallized by solid phase crystallization (SPC) method at 600°C for 24 hours in an N_2 ambient to form poly-Si films. Poly-Si films were patterned into active regions by transformer couple plasma (TCP) etching system using mixture gases of Cl_2 and HBr.

After RCA cleaning procedure, a 50-nm-thick TEOS oxide was deposited by LPCVD with TEOS and O_2 gases at 695°C to form the gate insulator. A 150-nm-thick poly-Si was deposited to serve as the gate electrode by LPCVD at 595°C. Then, the poly-Si film was patterned and etched by TCP etching system to form the gate electrode and the gate oxide on source/drain was removed using dilute HF solution. The regions of source, drain, and gate were doped by a self-aligned phosphorous ion

implantation at the dosage and energy of 5×10^{15}ions/cm^{-2} and 20keV, respectively. The dopant activation was performed by furnace system at 600°C for 12 hours, followed by a deposition of 250nm-thick silicon nitride layer and 300nm-thick passivation oxide using PECVD system at 350°C and the definition of contact holes. Then, we etched passivation oxide by BOE solution. After removed passivation oxide, 90% silicon nitride layer was etched by dry etching system and utilized oxide layer as a hard mask for etching 10% silicon nitride layer by wet etch in H_3PO_4 solution. Finally, a 800-nm-thick Al was deposited by sputter and patterned for metal pads, and devices were passivated by NH_3 plasma treatment for 30 minute at 300°C. For comparison, the control samples have no capping nitride layer. It only deposited passivaton oxide using PECVD system at 350°C.

2.3 Method of Device Parameter Extraction

In this thesis, we use Ellipsometer to measure the thickness of poly-Si, amorphous-Si and TEOS oxide films in the fabrication procedure. All the electrical characteristics of proposed poly-Si TFTs were measured by HP 4156B-Precision Semiconductor Parameter Analyzer.

Many methods have been proposed to extract the characteristic parameters of poly-Si TFTs. In this section, those methods are described.

2.3.1 Determination of Threshold Voltage

Threshold voltage (V_{th}) is an important parameter required for the channel length-width and series resistance measurements. However, V_{th} is not uniquely defined. Various definitions have been proposed and the reason can be found in I_D-V_{GS} curves. One of the most common techniques is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of

50~100mV to ensure operation in the linear region [17]. The drain current is not zero when V_{GS} below threshold voltage and approaches zero asymptotically. Hence the I_{DS} versus V_{GS} curve can be extrapolated to I_D=0, and the V_{th} is determined from the extrapolated intercept of gate voltage (V_{GS}) by

$$V_{th} = V_{GS} - \frac{V_{DS}}{2} \quad \text{---------- (Eq. 2.1)}$$

Equation (2.1) is strictly only valid for negligible series resistance. Fortunately series resistance is usually negligible at the low drain current when threshold voltage measurements are made. The I_{DS}-V_{GS} curve deviates from a straight line at gate voltage below V_{th} due to subthreshold current and above V_{th} due to series resistance and mobility degradation effects. It is common practice to find the point of maximum slope of the I_{DS}-V_{GS} curve and fit a straight line to extrapolate to I_D=0 by means of finding the point of maximum of transconductance (Gm).

In this thesis, we use a simpler method to determinate the V_{th} called constant drain current method. The voltage at a specified threshold drain current is taken as the V_{th}. This method is adopted in the most studied papers of poly-Si TFTs. It can be given a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current is specified at (W/L)×10nA for V_{DS}=0.1V and (W/L)×100nA for V_{DS}=5V, where W and L are channel width and channel length, respectively.

2.3.2 Determination of Subthreshold-Swing

Subthreshold swing (S.S.) is a typical parameter to describe the control ability of gate toward channel, which reflects the turn on/off speed of a device. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude.

The S.S. should be independent of drain voltage and gate voltage. However, in reality, the S.S. increases with drain voltage due to channel shortening effect such as charge sharing, avalanche multiplication and punchthrough effect. The subthreshold swing is also related to gate voltage due to undesirable and inevitable factors such as the serial resistance and interface states.

In this thesis, the S.S. is defined as one-third of the gate voltage required to decrease the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

2.3.3 Determination of Field Effect Mobility

Usually, field effect mobility (μ_{eff}) is determined from the maximum value of transconductance (Gm) at low drain bias. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so that the first order of I-V relation in the bulk Si MOSFETs can be applied to poly-Si TFTs. The drain current in linear region ($V_{DS} < V_{GS} - V_{th}$) can be approximated as the following equation:

$$I_{DS} = \mu_{eff} C_{ox} \left(\frac{W}{L} \right) \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right] \quad \text{---------- (Eq. 2.2)}$$

where W and L are channel width and channel length, respectively. C_{ox} is the gate oxide capacitance per unit area and V_{th} is the threshold voltage. Thus, the transconductance is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{eff} C_{ox} \left(\frac{W}{L} \right) V_{DS} \quad \text{---------- (Eq. 2.3)}$$

Therefore, the field-effect mobility is

$$\mu_{eff} = \frac{L}{C_{ox} W V_{DS}} g_{m(\max)} \Big|_{V_{DS} \to 0} \quad \text{---------- (Eq.2.4)}$$

2.3.4 Determination of ON/OFF Current Ratio

On/off current ratio is one of the most important parameters of poly-Si TFTs since a high-performance device exhibits not only a large on-current but also a small off-current (leakage current). The leakage current mechanism in poly-Si TFTs is not like that in MOSFET. In MOSFET, the channel is composed of single crystalline Si and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in poly-Si TFTs, the channel is composed of poly-Si. A large amount of trap state densities in grain structure attribute a lot of defect states in energy band gap to enhance the tunneling effect. Therefore, the leakage current is much larger in poly-Si TFTs than in MOSFET. When the voltage drops between gate voltage and drain voltage increases, the band gap width decreases and the tunneling effect becomes much more severe. Normally we can find this effect in typical poly-Si TFTs' I_{DS}-V_{GS} characteristics where the magnitude of leakage current will reach a minimum and then increase as the gate voltage decreases/increases for n/p-channel TFTs.

There are a lot of ways to specify the on and off-current. In this chapter, take n-channel poly-Si TFTs for examples, the on-current is defined as the drain current when gate voltage at the maximum value and drain voltage is 5V. The off-current is specified as the minimum current when drain voltage equals to 5V.

$$\frac{I_{ON}}{I_{OFF}} = \frac{Maximum \quad Current \quad of \quad I_{DS}-V_{GS} \quad Plot \quad at \quad V_{DS}=5V}{Minimum \quad Current \quad of \quad I_{DS}-V_{GS} \quad Plot \quad at \quad V_{DS}=5V} \quad \text{-------- (Eq. 2.5)}$$

2.3.5 Extraction of Grain Boundary Trap State Density

The Trap State Density (N_t), which can be determined by the theory established by Levinson *et al.* [18], which is based on Seto's theory [19].

For poly-Si TFTs, the drain current I_{DS} can be given as following:

$$I_{DS} = \mu_{FE} C_{ox} \left(\frac{W}{L} \right) V_{DS} V_{GS} \exp\left(\frac{-q^3 N_t^{\,2} L_c}{8\varepsilon_{Si} kTC_{ox} V_{GS}} \right)$$ ---------- (Eq. 2.6)

Where,

μ_{eff}	field-effect mobility of carriers
q	electron charge
k	Boltzmann's constant
ε_{Si}	dielectric constant of silicon
T	temperature
N_t	trap-state density per unit area
L_c	channel thickness

This expression, first developed by Levinson *et al.*, is a standard MOSFET's equation with an activated mobility, which depends on the grain-boundary barrier height. Levinson *et al.* assumed that the channel thickness was constant and equal to the thickness of the poly-Si film (t). This simplifying assumption is permissible only for very thin film (t<10nm). The trap-state density can be obtained by extracting a straight line on the plot of $ln(I_{DS}/V_{GS})$ versus $1/V_{GS}$ at low drain voltage and high gate voltage.

Proano *et al.* [20] thought that a barrier approximation is to calculate the gate induced carrier channel thickness by solving Poisson's equation for an undoped material and to define the channel thickness (L_c) as a thickness in which 80% of the total charges were induced by the gate. Doing so, one obtains

$$L_c = \frac{8kTt_{ox}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}}}}{q\left(V_{GS} - V_{fb}\right)}$$ ---------- (Eq. 2.7)

which varies inversely with $(V_{GS}-V_{fb})$. This predicts, by substituting Eq.2.7 into Eq.2.6, that $ln[I_{DS}/(V_{GS}-V_{fb})]$ versus $1/(V_{GS}-V_{fb})^2$. We use the gate voltage at which minimum leakage current occurs as flat-band voltage (V_{fb}). Effective trap-state density (N_t) can be determined from the square root of the slope.

2.4 Results and Discussion

2.4.1 Characteristics of poly-Si TFTs with capping silicon nitride layer

We measured device characteristics while we have done the device fabrication. Fig. 2-2 shows the transfer characteristics (I_{DS}-V_{GS}) for the control and Capping Nitride poly-Si TFTs. The measurements was performed at drain voltage of V_{DS}=5V. The measured and extracted parameters from the devices are listed in table 2-1. the threshold voltage, subthreshold swing, on-current (V_{GS}=20V), and off-current (V_{GS}=-10V) were measured at V_{DS}=5V.

In the Fig.2-2, we can see that the Capping Nitride poly-Si TFTs exhibit better on-state characteristics than the control sample. In off-state, under a large negative gate bias, the leakage currents of the Capping Nitride poly-Si TFTs ($1.71*10^{-10}$) are significant lower than the control poly-Si TFTs ($1.61*10^{-9}$). It was quite obvious that gate induce drain leakage (GIDL) was suppressed in Capping Nitride poly-Si TFTs. Moreover, the threshold voltage and subthreshold swing of the Capping Nitride poly-Si TFTs (0.16V & 0.98V/dec.) was found to be superior to the control sample (0.67V & 1.25V/dec.). Fig. 2-3, we compared the field effect mobility between those two samples, the proposed TFTs shows large enhancement of mobility compared with conventional TFTs. They were found to be 23(cm^2/V.s) and 32.5(cm^2/V.s) for the control and Capping Nitride poly-Si TFTs, respectively. The mobility of Capping Nitride poly-Si TFTs has greatly enhancement by 41.3%. This is due to capping nitride layer has tensile strain and further forming compressively strained polysilicon gate electrode and then give a tensile stress on the channel to result in electron mobility enhancement [11] .

Fig. 2-4 shows the plot of $ln[I_{DS}/(V_{GS}-V_{fb})]$ versus $1/(V_{GS}-V_{fb})^2$ at low drain voltage and high gate voltage for the control and the Capping Nitride samples. The

effective trap state density calculated from the slopes for the control and Capping Nitride samples were $8.32*10^{12}cm^{-2}$ and $3.89*10^{12}cm^{-2}$, respectively. The proposed poly-Si TFTs have less trap state density then the control samples, we deduced that proposed poly-Si TFTs have NH_3 plasma treatment when deposited silicon nitride layer. Fig. 2-5 shows Source/drain series resistance extraction of (a) the Control and (b) the Capping Nitride poly-Si TFTs. We found that Capping Nitride poly-Si TFTs' series resistance is small than the control poly-Si TFTs. They were found to be 5.83kΩ and 1.92kΩ for the control and Capping Nitride poly-Si TFTs, respectively. This result attributed nitride layer induced electron in source/drain region when device operated. So, source/drain series resistance are decreased. The schematic diagram of the mechanical of source/drain series resistance reduction is shown in Fig. 2-6.

Fig.2-7 shows the output characteristics of the control and proposed poly-Si TFTs. It can be seen that the kink effect was suppressed in Capping Nitride poly-Si TFTs and saturation current greatly enhanced. This is attributed to the facts that nitride layer reduce horizontal electrical field [12] and further reduce impact ionization rate, the carrier that pile up in the channel is decreasing. So, kink effect was suppressed in Capping Nitride poly-Si TFTs. However, the enhancement of saturation current is due to high field effect mobility.

2.4.2 Reliability of poly-Si TFTs with capping silicon nitride layer

Furthermore, we discussed the reliability of proposed TFTs and convention TFTs. We apply DC stress to the device, the hot carrier stress test was performed at V_D=20V, V_G=10V, and source electrode grounded for 1000 sec to investigate the device reliability. Fig. 2-8 shows the variation of the on-state current (I_{on}) and threshold

voltage (V_{th}) over hot carrier stress time. The variations of Ion and V_{th} were defined as $(I_{on,stressed}-I_{on,initial})/I_{on,initial}*100\%$ and $(V_{th,stressed}-V_{th,initial})/V_{th,initial}*100\%$, respectively, where $I_{on,stressed}$, $V_{th,stressed}$, $I_{on,initial}$, and $V_{th,initial}$ represent the measured values before and after electrical stress.

Notably, the control shows relatively large variations in I_{on}, and V_{th} after 1000sec stress. These results imply that Capping Nitride poly-Si TFTs greatly reduced the device degradation under hot carrier stress, this is attributed to the fact that similarly high-k spacer structure can reduce horizontal electrical field [12] and then decrease the impact ionization rate. So, the Capping Nitride poly-Si TFTs have better reliability then the control samples.

2.5 Summary

We fabricated high performance TFTs with capping silicon nitride layer. The characteristic of proposed TFTs have great improvement, such as higher on-current, higher mobility, lower subthreshold swing, suppressing kink effect and GIDL effect and good reliability. The process of proposed TFTs is uncomplicated and no need of extra mask step. We believe that the proposed TFTs will be candidate in high performance TFTs application.

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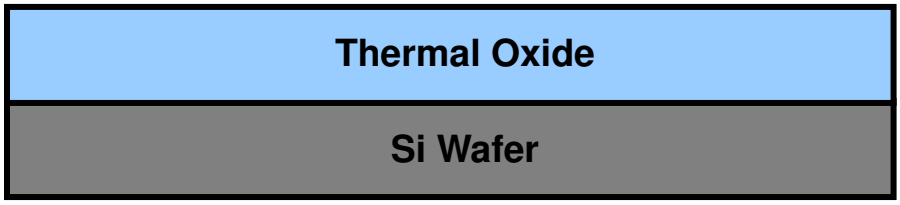
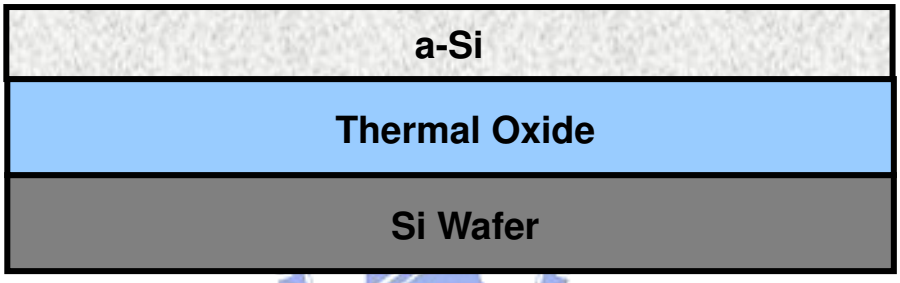
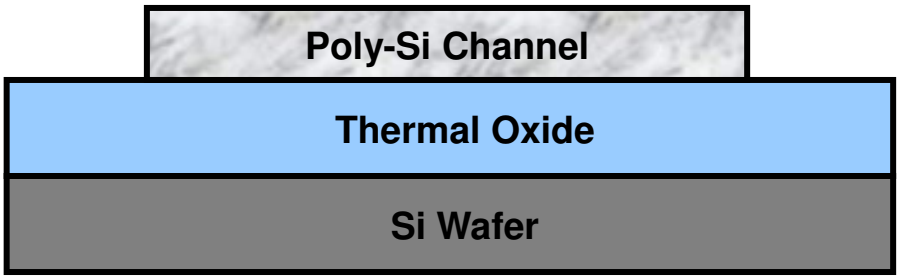


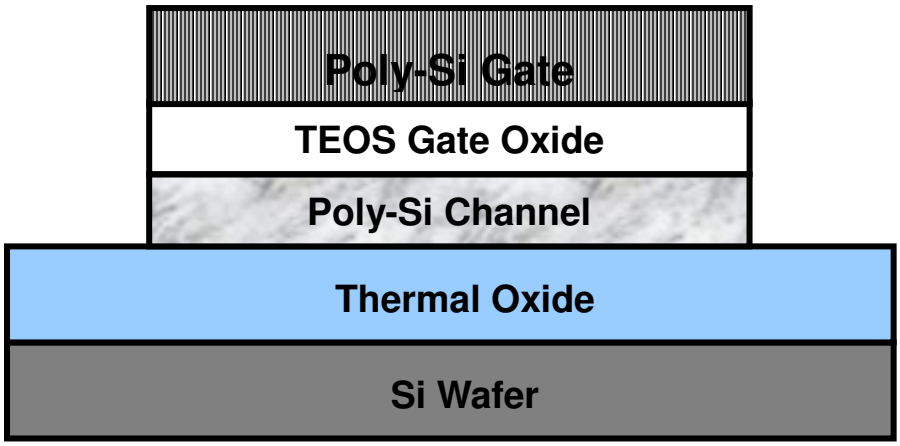
(a) Thermal oxidation grown by furnace



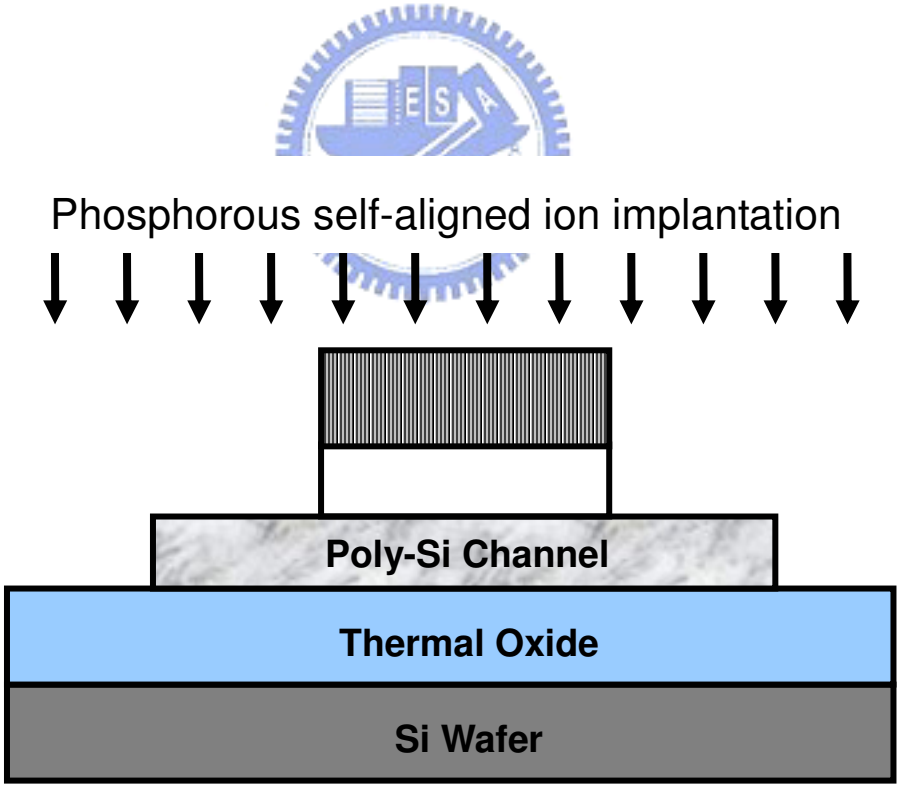
(b) Amorphous Si (a-Si) deposited by LPCVD



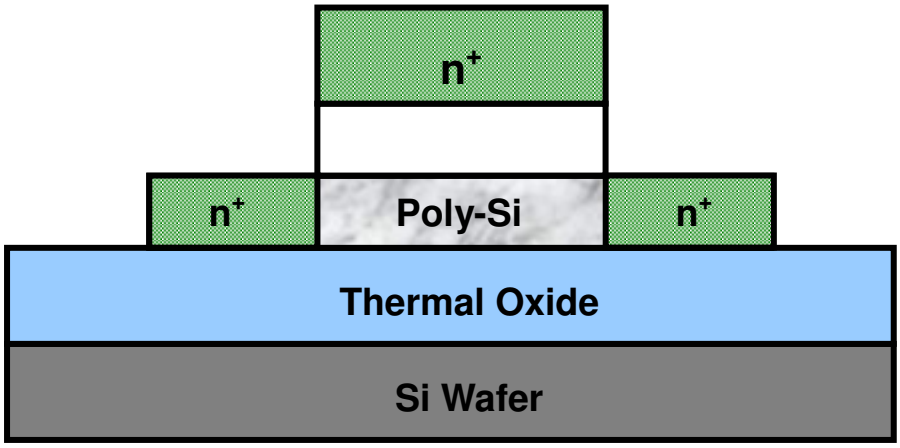
(c) Recrystallization of a-Si film into poly-Si channel by SPC, active region defined



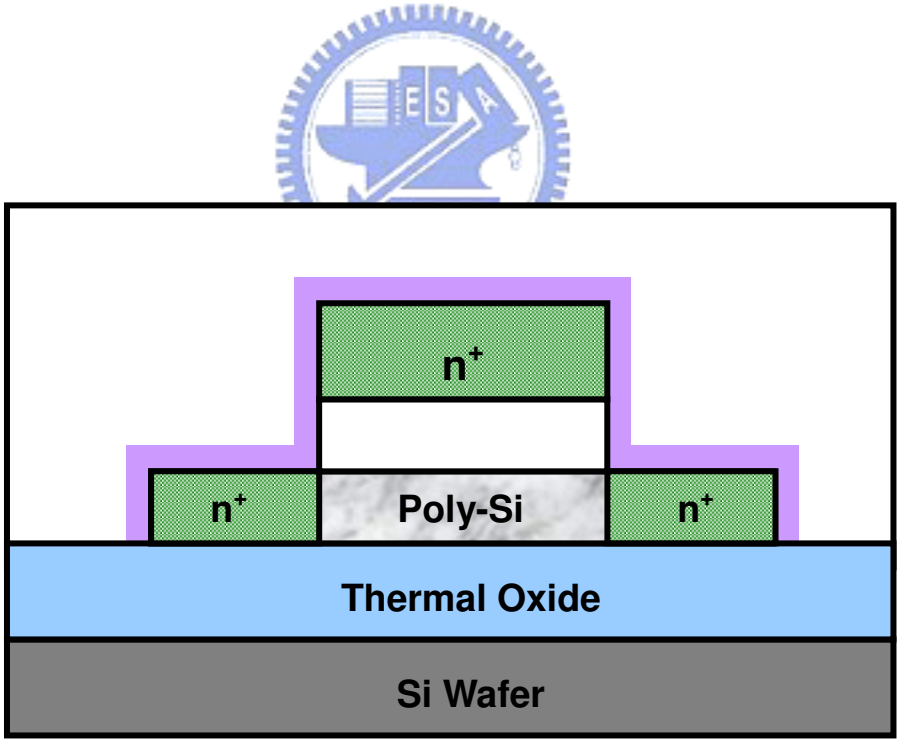
(d) Deposition of TEOS gate oxide by LPCVD and poly-Si gate by LPCVD



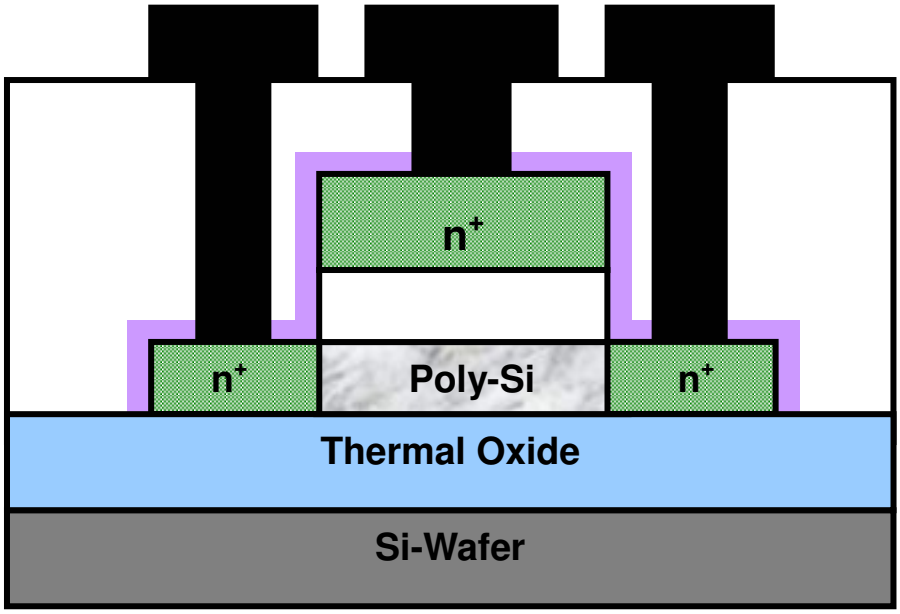
(e) The gate electrode defined and self-align phosphorous ion implantation



(f) Dopant activation by excimer laser annealing



(g) Deposition of silicon nitride layer and passivation oxide by PECVD



(h) Contact holes opened and metal pads formation

Fig 2-1 Schematic diagram of fabrication process for Capping Nitride poly-Si TFTs

Table 2.1 Comparison of device characteristics of the Control and Capping Nitride poly-Si TFTs.

Poly-Si TFTs	Control	Capping Nitride
V_{th} (V)	0.67	0.16
S.S (V/dec.)	1.25	0.98
μ_{Eff} (cm^2/V.s)	23	32.5
I_{on} @ VG=20V	$1.08*10^{-4}$	$1.60*10^{-4}$
I_{off} @ VG=-10V	$1.61*10^{-9}$	$1.71*10^{-10}$
Rs (Ω)	$5.83*10^{3}$	$1.92*10^{3}$
N_t (cm^{-2})	$8.32*10^{12}$	$3.89*10^{12}$

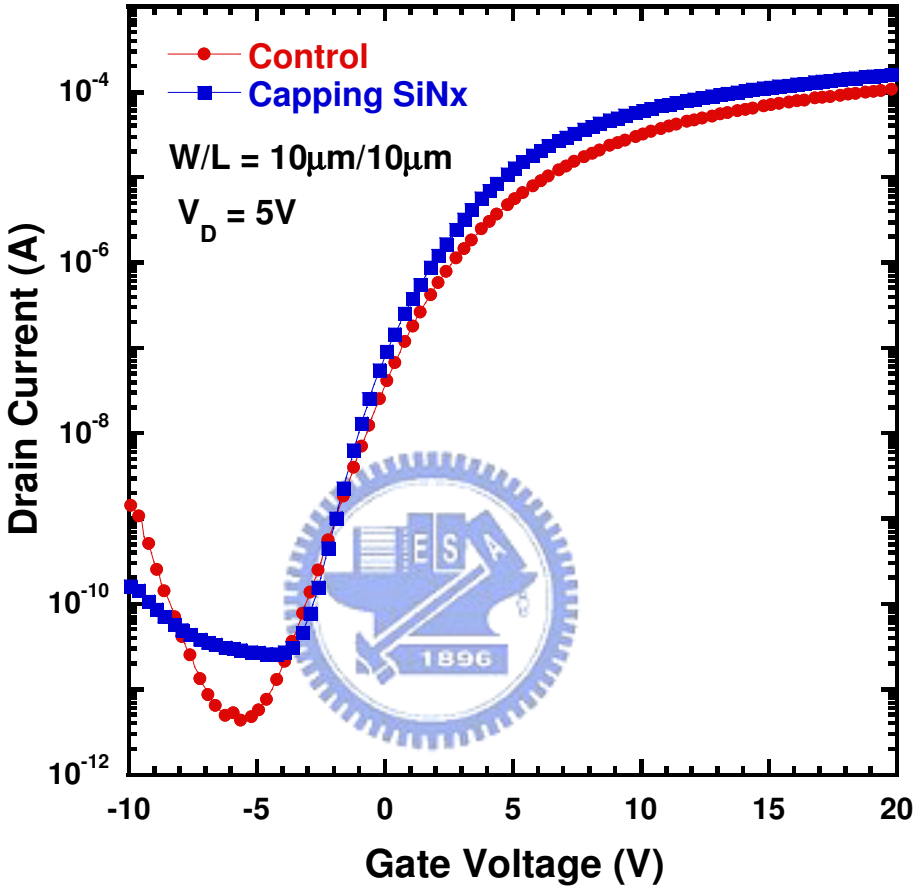


Fig. 2-2 Transfer characteristics of the Control and Capping Nitride poly-Si TFTs with V_{DS}=5V

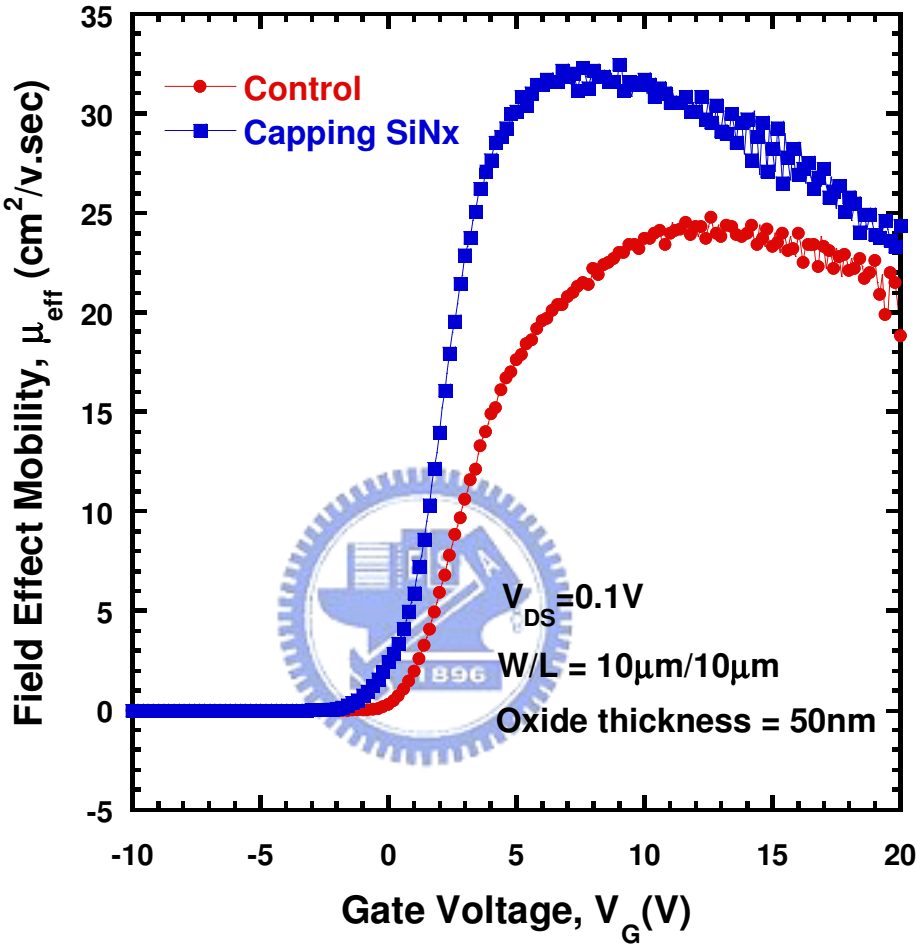


Fig. 2-3 Field-effect mobility of the Control and Capping Nitride poly-Si TFTs with V_{DS}=0.1V

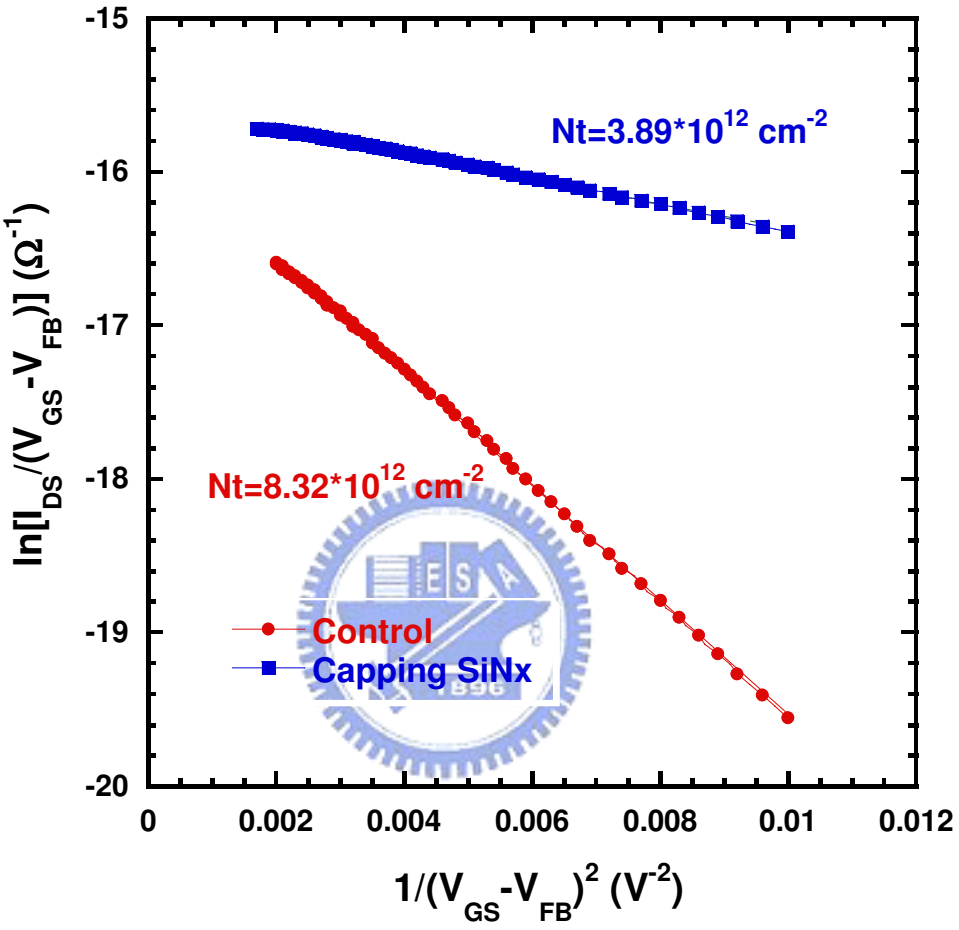
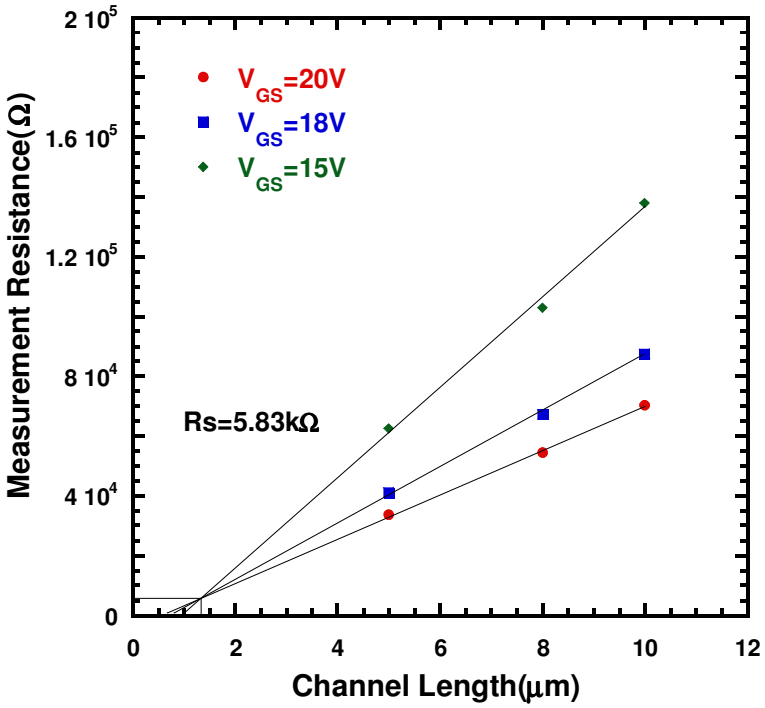
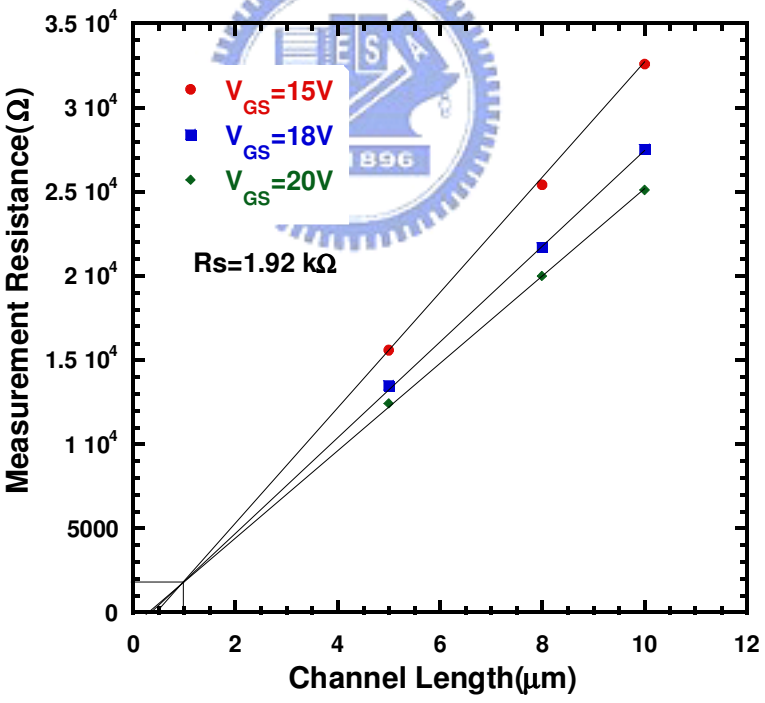


Fig. 2-4 Trap state density extraction of the Control and the Capping Nitride poly-Si TFTs



(a) Control poly-Si TFTs



(b) Capping Nitride poly-Si TFTs

Fig. 2-5 Source/drain series resistance extraction of (a) the Control and (b) the Capping Nitride poly-Si TFTs

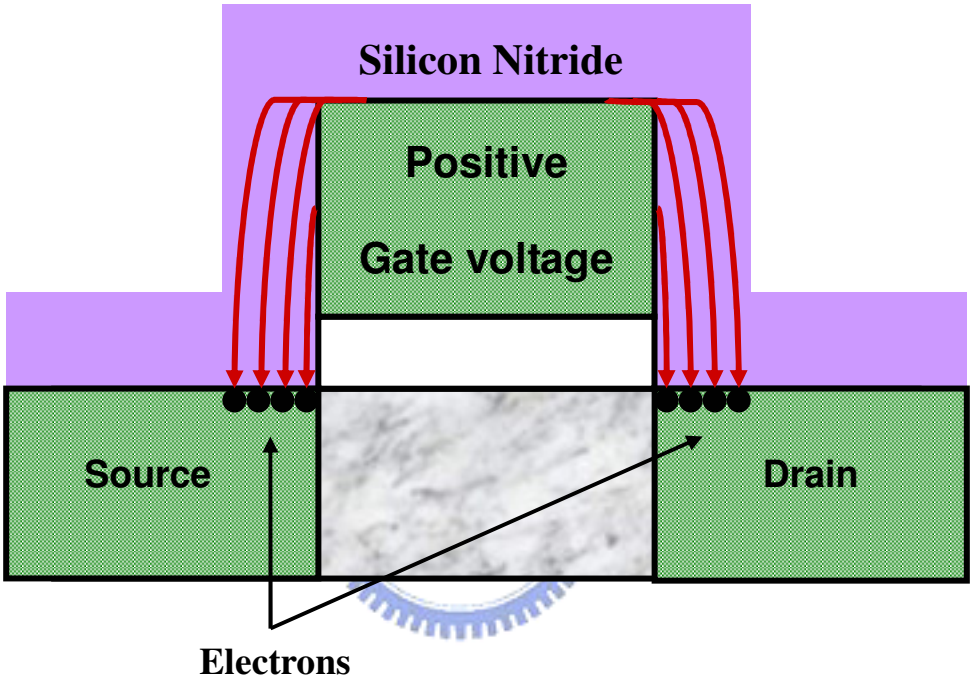


Fig. 2-6 Mechanism of reduction of source/drain series resistance

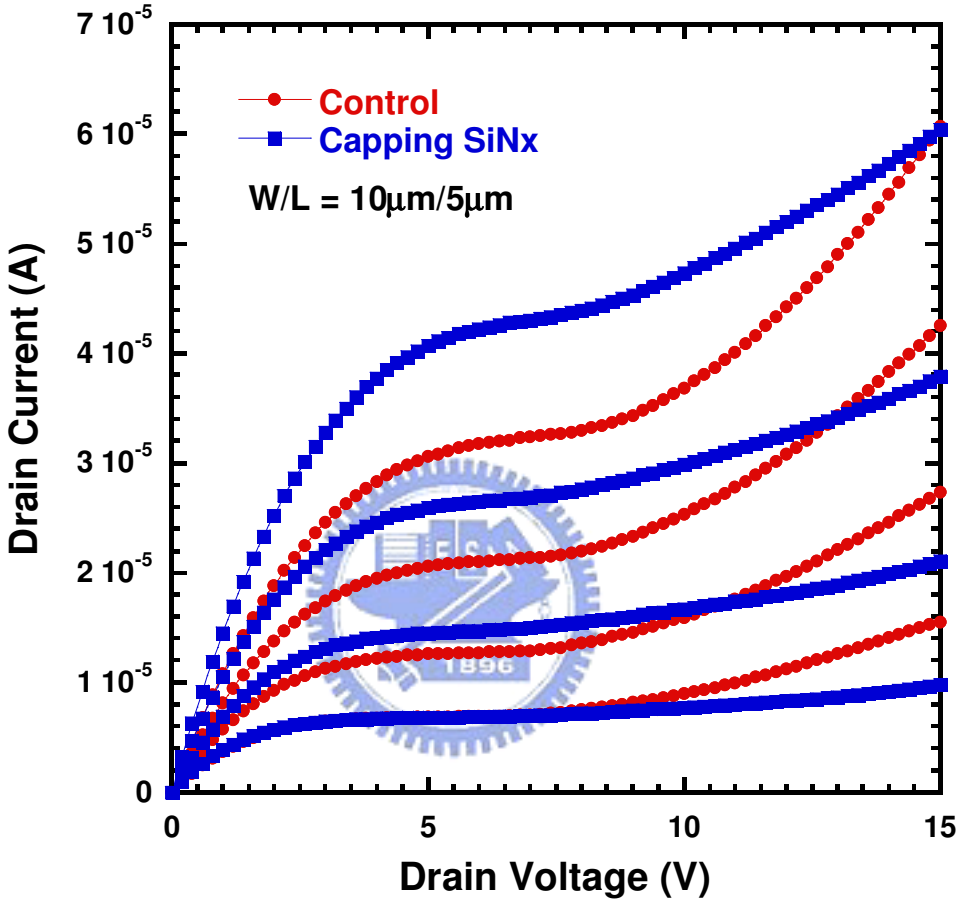
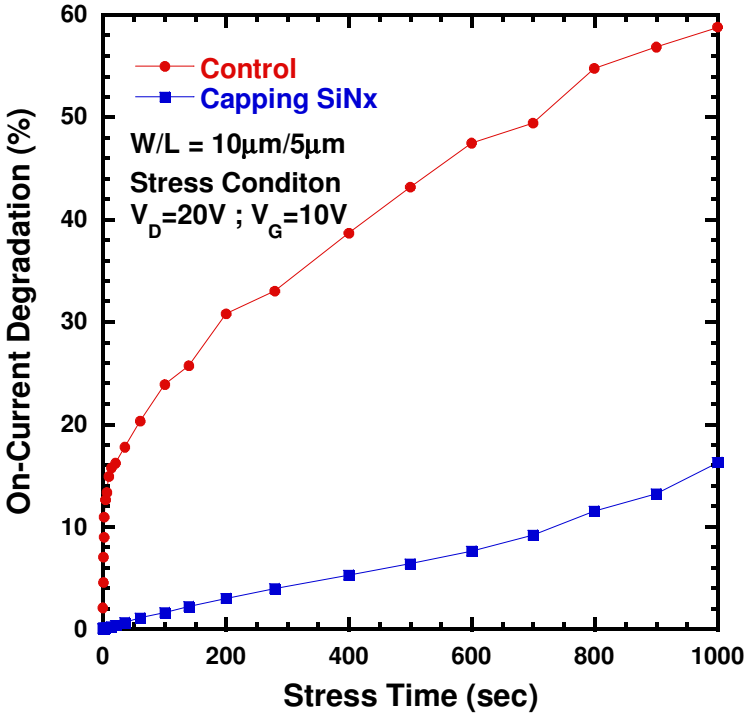
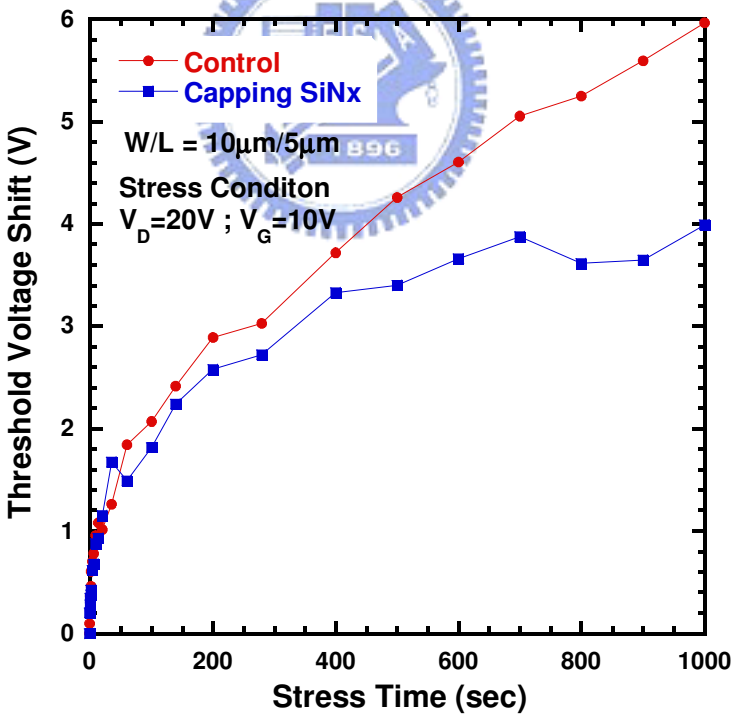


Fig. 2-7 Output characteristic of the Control and the Capping Nitride poly-Si TFTs



(a) On-current degradation with stress time



(b) Threshold voltage degradation with stress time

Fig. 2-8 (a) on-current and (b) threshold voltage degradation as a function of stress time under hot-carrier stress

Chapter 3

Characteristic and Reliability of P-Channel Poly-Si TFTs with Multi-Channel Structure

3.1 Introduction

P-channel poly-Si TFTs have been used for many applications, such as low-power SRAMs [1], High-Resolution Active Matrix [2] and EEPROM's [3]. In circuit design, CMOS technique is a very important technique. Because it have many advantage such as low power consumption, fully restored logic and better reliability. We would like realized CMOS technique by using TFTs device. So P-Channel and N-Channel TFTs are needed for integrated CMOS circuit. We believed that Poly-Si TFTs technology is the most promising candidate for the ultimate goal of building fully integrated flat panel display system-on-glass. Moreover, the stability of p-channel polysilicon TFTs has not been investigated as much as n-channel polysilicon TFTs. So, we discussed characteristic and reliability of P-Channel poly-Si TFTs in this chapter.

It is well know that the characteristics of poly-Si TFTs are dominated by the large trap density in poly-Si film. When channel width scaled down, devices are reported to exhibit better performance such as lower threshold voltage and smaller trap density [4]-[6]. As a result, Poly-Si TFTs with narrow and multiple channels have been proposed to improve device performance [7][8]. Previous reports indicated that the existence regions near the poly-Si pattern edge where the grain boundary trap density is much smaller than elsewhere in the poly-Si film [4]. When channel width

decreasing the effect of poly-Si pattern edge dominates and causes an effective trap density decreasing. Moreover, Due to the formation of active region island the gate electrode layer that climbs across the channel may induce side channels in both sides of the channel region. When channel width scaled down these side-channels become comparable to the main channel, accordingly increasing the effective channel width. Additionally, in CMOS technology, tri-gate [9] structure has been reported to exhibit superior gate control over the channel than a conventional single-gate MOSFET. Thus, we incorporate multi-channel with different channel widths, and tri-gate structure to achieve the high-performance and high reliability poly-Si TFTs.

Previous reports have demonstrated that n-channel poly-Si TFTs with multi-channel structure can improve device performance [10] and also discussed reliability of n-channel poly-Si TFTs with multi-channel structure. In this chapter, we fabricated p-channel poly-Si TFTs with multi-channel structure. We will analyze and discuss both characteristic and reliability of the proposed poly-Si TFTs in this chapter.

3.2 Experiment

Figure 3-1 shows the process flow of the proposed poly-Si TFTs. First, 500-nm-thick thermal oxide was grown on the Si wafer by using a furnace system. All the experimental devices in this study were fabricated on thermally oxidized Si wafers. Then, 100-nm-thick amorphous silicon layers were deposited on the thermal oxide layer using a low-pressure chemical vapor deposition (LPCVD) system at 550°C. Then, amorphous silicon films were recrystallized by solid phase crystallization (SPC) method at 600°C for 24 hours in an N_2 ambient to form poly-Si films. Poly-Si films were patterned into active regions by transformer couple plasma (TCP) etching system using mixture gases of Cl_2 and HBr.

After RCA cleaning procedure, a 50-nm-thick TEOS oxide was deposited by

LPCVD with TEOS and O_2 gases at 695°C to form the gate insulator. A 150-nm-thick poly-Si was deposited to serve as the gate electrode by LPCVD at 595°C. Then, the poly-Si film was patterned and etched by TCP etching system to form the gate electrode and the gate oxide on source/drain was removed using dilute HF solution. The regions of source, drain, and gate were doped by a self-aligned BF_2 ion implantation at the dosage and energy of 5×10^{15}ions/cm^{-2} and 40keV, respectively. The dopant activation was performed by furnace system at 600°C for 8 hours, followed by a deposition of 400nm-thick passivation oxide using PECVD system at 350°C and the definition of contact holes. Finally, a 500-nm-thick Al was deposited by sputter and patterned for metal pads, and devices were passivated by NH_3 plasma treatment for 30 minutes at 300°C.

Figure 3-2 presents the cross-section of the conventional and multi-channel poly-Si TFTs, which is parallel to the direction of the source and drain electrode. Figure 3-3 depicts the cross-section perpendicular to the direction of the source and drain electrode. In next section, we will discuss the transfer characteristics of the conventional and proposed TFTs with single,4, 8, 20, and 40 stripes of the same total channel width. The top view of proposed TFTs with different channel strips as shown in Fig. 3-4. The detailed data of these structures were summarized in Table 3-1.

3.3 Results and Discussion

3.3.1 Characteristics of P-Channel Poly-Si TFTs with Multiple Channels

Figure 3-5 shows the transfer characteristics (I_{DS}-V_{GS}) for the conventional and proposed TFTs with different stripes of channel. Table 3-2 summarizes the measured and extracted parameters from the devices. The threshold voltage, subthreshold swing, on-state current (V_{GS}=-25V) and the off-state current (V_{GS}=0V) were measured at

V_{DS}=-5V. It is obvious that the electrical characteristics of the poly-Si TFTs with multiple channels are significantly improved. In this figure, we can see that on-state current increases with channel stripes increasing. This is due to side wall effect and the better gate control capability in the multi-channel structure TFTs. The side wall effect means that we gain extra channel width in multi-channel structure TFTs as shown in Fig. 3-3 and then the better gate control capability is due to the poly-gate climb across channel region to form the tri-gate structure in multi-channel TFTs. Threshold voltage and subthreshold swing decreased with the stripes of channel increased is also due to the better gate capability in multi-channel TFTs.

Fig. 3-6 shows the field effect mobility of P-type multi-channel poly-Si TFTs with different stripes of channel. It can be seen that the field effect mobility increases when stripes of channel increases. Because we extracted filed effect mobility from transfer characteristics at V_{DS}=-0.1, the enhancement of mobility can be also explained to the side wall effect and the better gate control capability in the multi-channel structure TFTs. Fig. 3-7 shows the distribution of threshold voltage and field effect mobility of the proposed multi-channel poly-Si TFTs with different stripes of channel. The vertical bars indicate the minimum and maximum value of the devices characteristics and the squares are the average values. In this figure, we can clear see the threshold voltage decreased when stripes of channel increased and the mobility increased as stripes of channel increased. In this figure, we also found that we gained better uniformity in proposed poly-Si TFTs due to better gate control capability.

It has been reported that the grain boundary trap state density in the channel regions near the pattern edge is much lower than elsewhere in the poly-Si channel [6]. In order to verify if the trap state density reduced or not, the effective trap state density (N_t) was calculated. Figure 3-8 shows the effective trap state density

extraction of the poly-Si TFTs with various stripes of channel. This figure shows the plot of $ln[I_{DS}/(V_{GS}-V_{fb})]$ versus $1/(V_{GS}-V_{fb})^2$ and we fitted line for each different stripes. We can see that the slop decreased with the stripes of channel increased and then we utilized this slop to calculated effective trap state density. The effective trap state density for S1, M4, M8, M20, and M40 are $6.42\times10^{12}cm^{-2}$, $6.28\times10^{12}cm^{-2}$, $6.18\times10^{12}cm^{-2}$, $5.46\times10^{12}cm^{-2}$,and 4.87×10^{12} ,respectively. This is because the better gate control capability causes the lower potential barrier locating at the grain boundary and easy to passivate trap state in the grain boundary when we done plasma treatment. Fig. 3-9 shows the plot of trap state density versus different strips of channel. We can see that trap state density decreases with channel stripes increasing obviously. However, from Fig. 3-10, we can see that the increase ratios of the on-state current for M4, M8, M20, and M40 are 2.17%, 4.62%, 17.1% and 35.3%, respectively, and they are much larger than the increase ratio of the effective channel width. Therefore, we demonstrated the channel sidewall effect was not the only factor to improve the electrical characteristics of multiple channel poly-Si TFTs. The better gate control capability is another factor to improve the on-current and field effect mobility because there are many corner in the multiple channel structure, the corner's electrostatic focusing is very strong and caused high carrier concentration in the channel region.

Figure 3-11 shows the output characteristics of the conventional and proposed poly-Si TFTs with different stripes of channel under V_G-V_{th}=-1; -2; -3V. It can be seen that the floating body effect was suppressed with the increase of the stripes of poly-Si channels. The better gate control ability, the larger depletion region existed in the channel, and therefore the fewer electrons accumulated within the channel region. So, it can be concluded that the floating body effect suppression was attributed to the improvement of gate control capability.

3.3.2 Reliability of P-Channel poly-Si TFTs with multiple channels

Finally, the reliability issue of the conventional and the proposed poly-Si TFTs with single, 2, 4, 10, and 20 stripes of the same total channel width were discussed. The hot-carrier stress test was performed at $V_{D,stress}$=-15V, $V_{G,stress}$=-15V, and source electrode grounded for 500sec to investigate the device reliability. Figure 3-12 shows the variations of the on-state current (I_{on}) and threshold voltage (V_{th}) over hot carrier stress time. The variations of I_{on} and V_{th}, were defined as $(I_{on,stressed} - I_{on,initial})/I_{on,initial} \times 100\%$ and $(V_{th,stressed} - V_{th,initial})/V_{th,initial} \times 100\%$, respectively, where $I_{on,stressed}$, $V_{th,stressed}$, $I_{on,initial}$, and $V_{th,initial}$, represent the measured values before and after electrical stress. In this figure, we can see that the degradation rate of the on-state current and threshold voltage improved with the increase of the stripes of poly-Si channel. This is due to better gate control capability in multiple channel structure. The depletion region in channel region becomes large so that fewer electron accumulation in the channel region. The floating body effect and effect of parasitic bipolar junction transistor will be suppressed. So, the reliability of multiple channel poly-Si TFTs were improved.

3.4 Summary

The effects of the numbers of the channel strips in P-type multi-channel TFTs on the performance and reliability have been investigated. As the stripes increased, the electrical characteristics and reliability of devices were improved significantly due to the enhancement of gate control capability. The n-type multi-channel TFTs have been investigated in previous reports. So, we might integrate n-type and p-type multi-channel TFTs to CMOS application. Furthermore, using CMOS technique applies to 3-D circuit applications.

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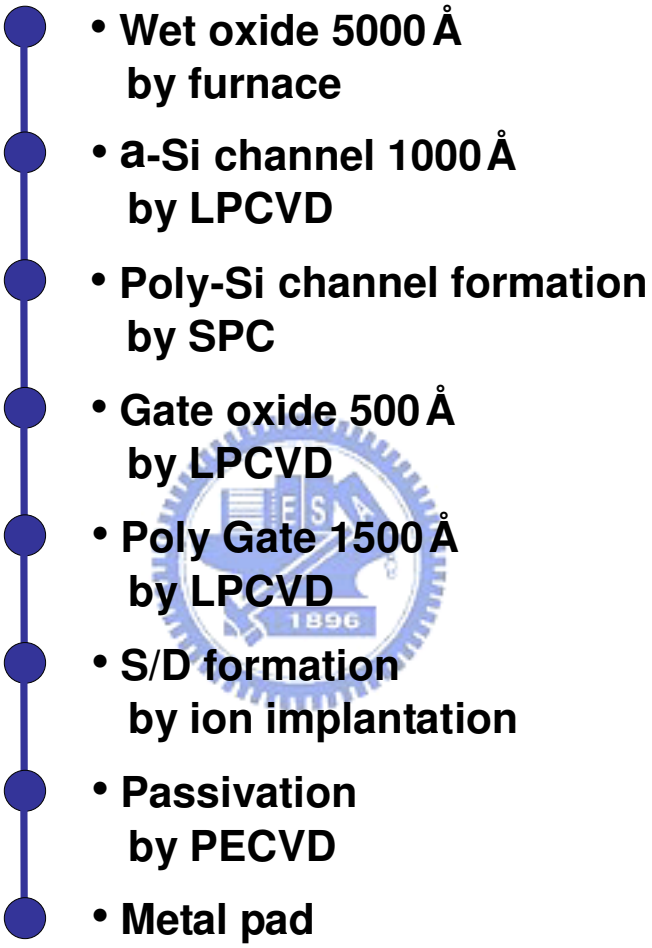


Fig. 3-1 Process flow of the conventional and multi-channel poly-Si TFTs.

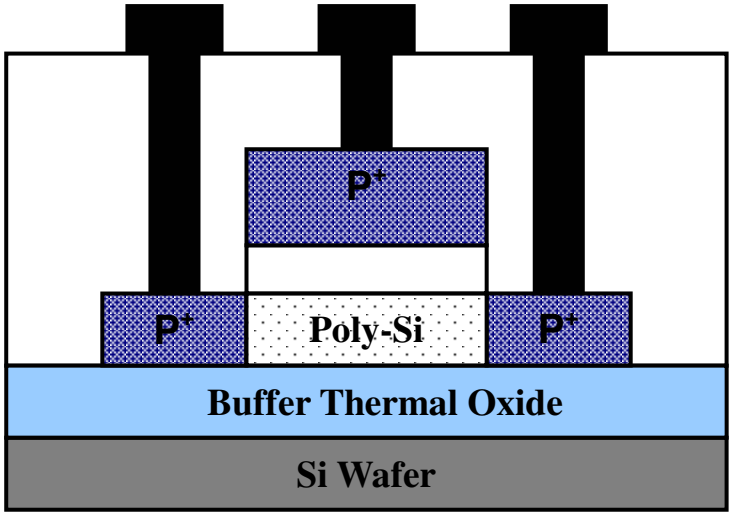


Fig. 3-2 Cross-section of the conventional and multi-channel poly-Si TFTs is parallel to the direction of the source and drain electrode.

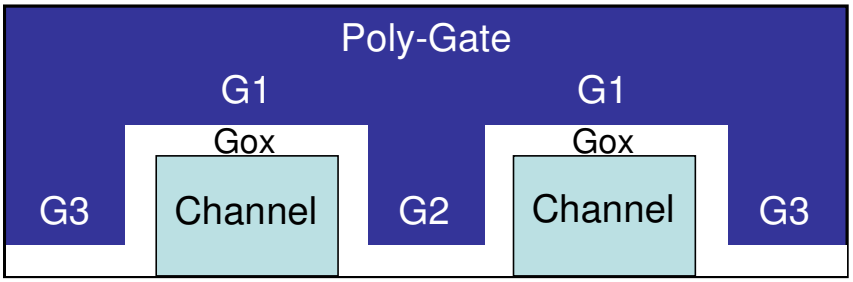
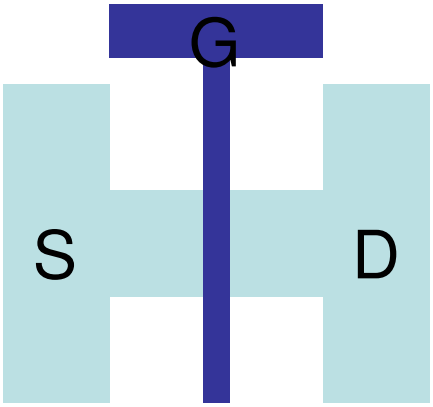
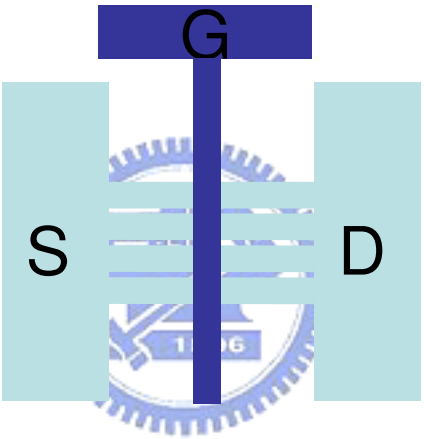


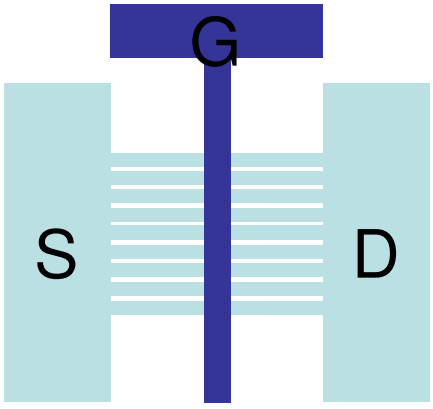
Fig. 3-3 Cross-section of the conventional and multi-channel poly-Si TFTs is perpendicular to the direction of the source and drain electrode.



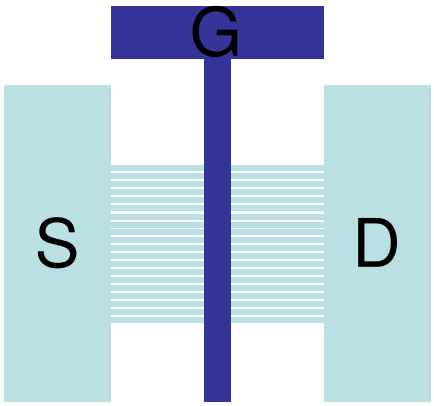
(a) Conventional TFT with single channel (S1)



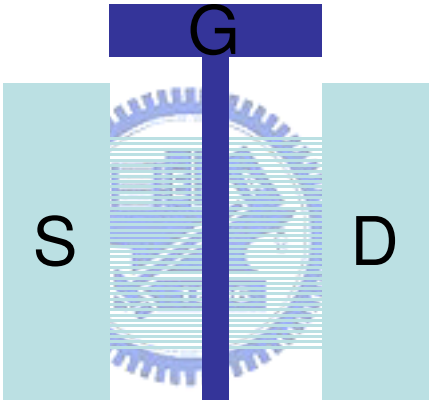
(b) Multi-channel TFT with 4 stripes (M4)



(c) Multi-channel TFT with 8 stripes (M8)



(d) Multi-channel with 20 stripes (M20)



(e) Multi-channel with 40 stripes (M40)

Fig. 3-4 Top view of the conventional and multi-channel poly-Si TFTs in (a), (b), (c), and (d). (The effective channel width W_{eff} = 40 μ m ; channel length L = 2 μ m.)

Table 3-1 Summary of the dimensions of S1, M4, M8, M20 and M40 TFTs. All devices have the same active channel thickness 100nm, gate TEOS-oxide thickness 50nm, and total channel width 40μm

	S1	M4	M8	M20	M40
Gate length (μm)	2	2	2	2	2
Channel number	1	4	8	20	40
Each channel width (μm)	40	10	5	2	1

Table 3-2 Summary of device parameters of the conventional and the proposed p-channel multi-channel poly-Si TFTs (W/L = 40μm/2μm) with different stripes of channel.

	S1	M4	M8	M20	M40
V_{th}(V)	-11.5	-11.0	-10.5	-9.7	-8.9
S.S(V/dec.)	1.287	1.276	1.204	1.123	1.143
μ_{eff}(cm2/V.s)	14.1	14.5	15.0	16.3	18.6
I_{on}@ V_G=25V(A)	$8.95*10^{-4}$	$9.14*10^{-4}$	$9.36*10^{-4}$	$1.05*10^{-3}$	$1.21*10^{-3}$
I_{off} @ V_G=0V(A)	$6.67*10^{-9}$	$7.65*10^{-9}$	$1.04*10^{-8}$	$1.10*10^{-8}$	$1.37*10^{-8}$
ON/OFF Ratio	$1.34*10^{5}$	$1.20*10^{5}$	$0.9*10^{5}$	$0.96*10^{5}$	$0.88*10^{5}$
Nt (cm^{-2})	$6.42*10^{12}$	$6.28*10^{12}$	$6.18*10^{12}$	$5.46*10^{12}$	$4.87*10^{12}$

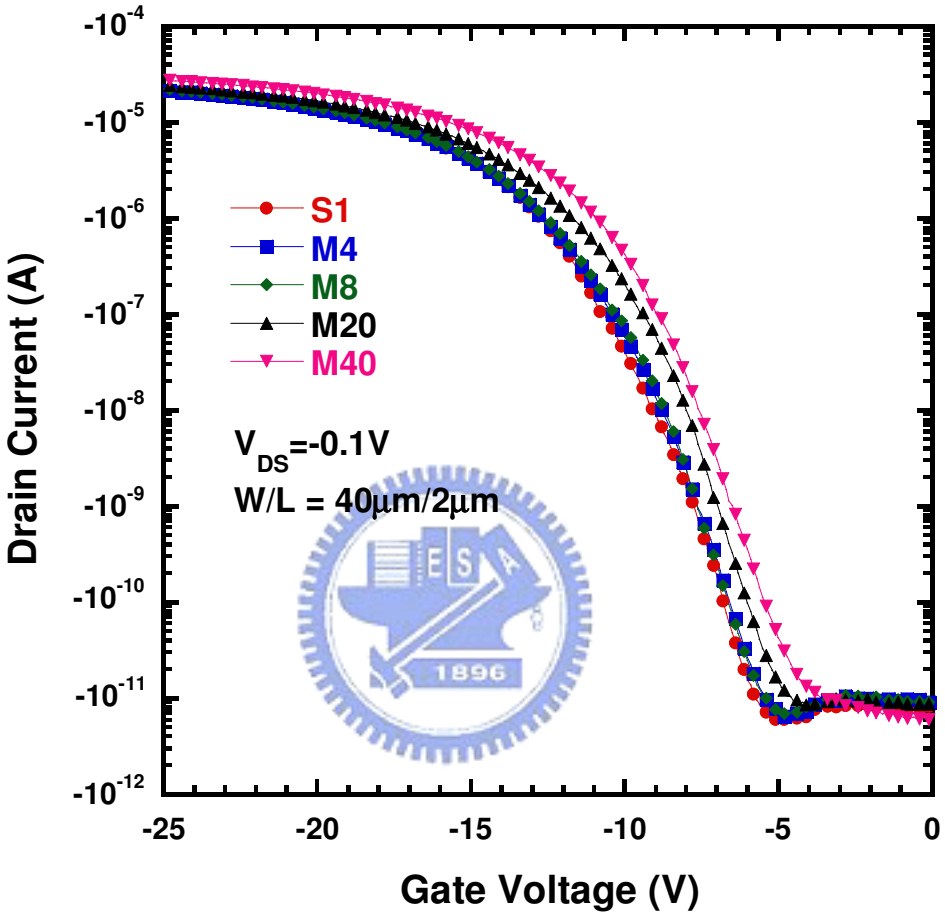


Fig. 3-5 Transfer characteristics of the conventional and the proposed p-channel multi-channel poly-Si TFTs with different stripes of channel.

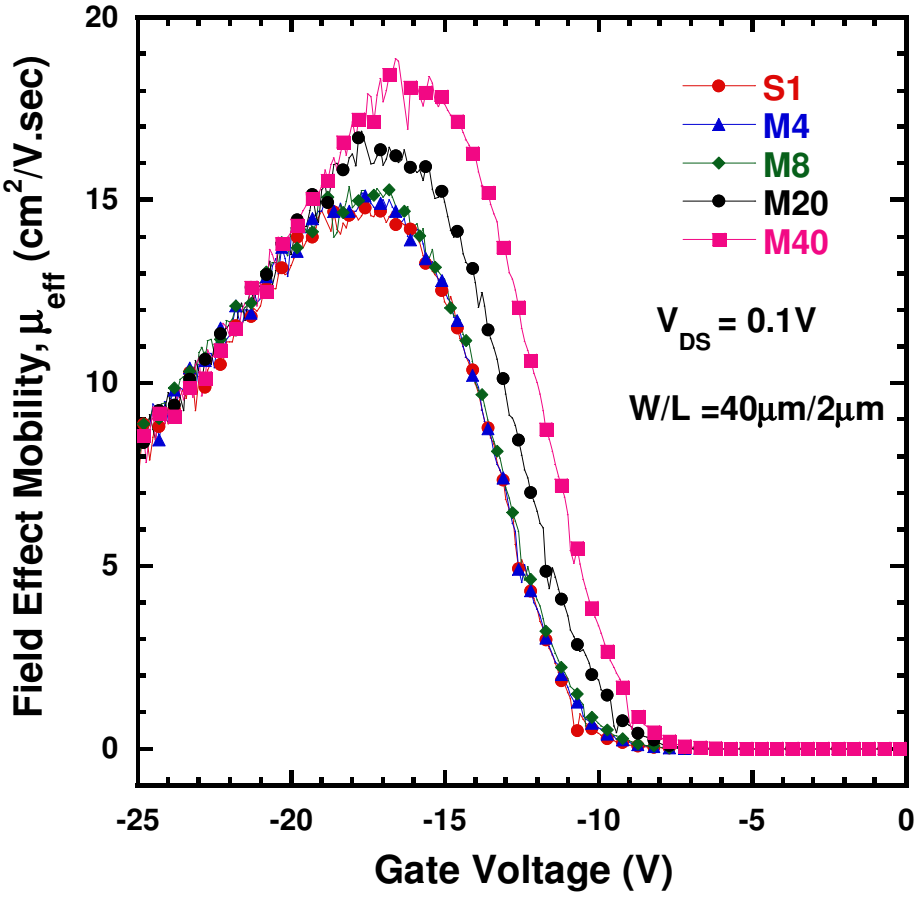
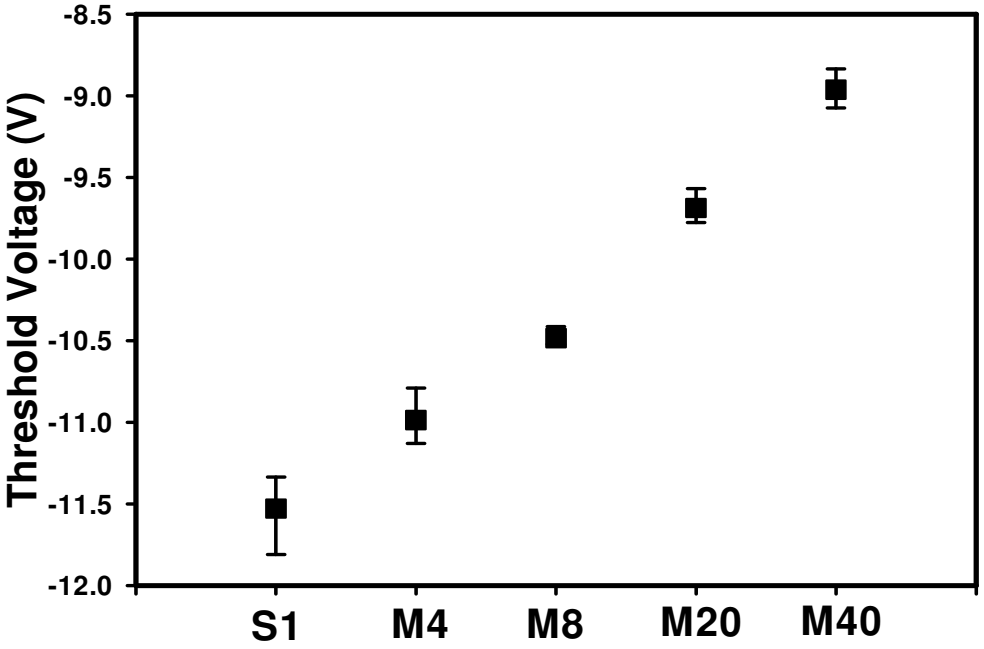
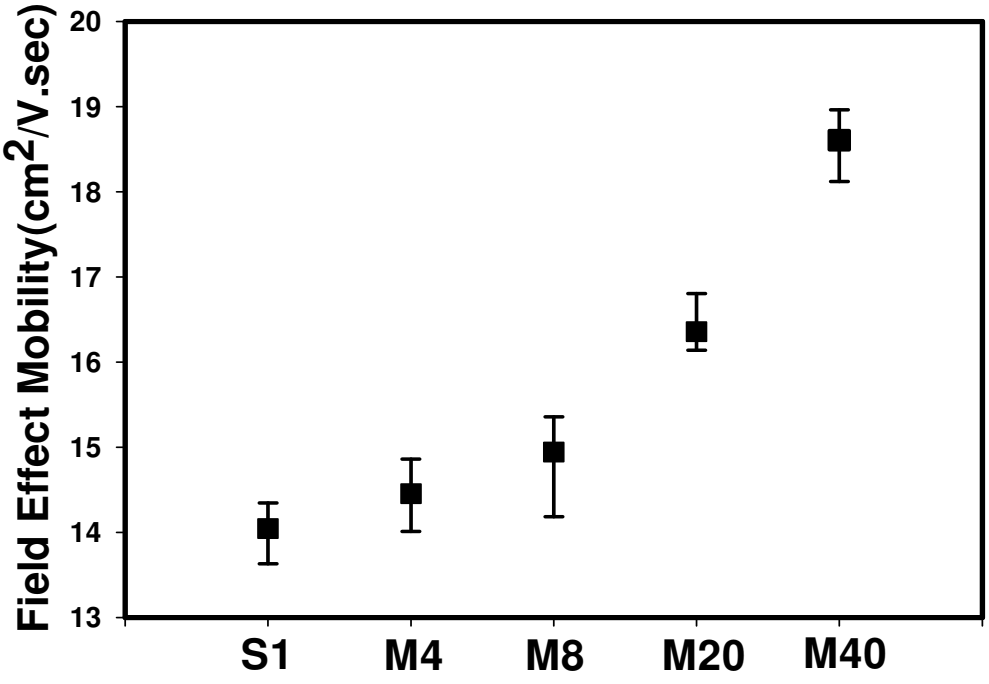


Fig. 3-6 Field effect mobility of the conventional and the proposed p-channel multi-channel poly-Si TFTs with different stripes of channel.



(a) Threshold voltage distribution



(b) Field effect mobility distribution

Fig. 3-7 Distribution of (a) Threshold voltage and (b) Field effect mobility of the proposed p-channel multi-channel poly-Si TFTs with different stripes of channel. The vertical bars indicate the minimum and maximum value of the devices characteristics and the squares are the average values

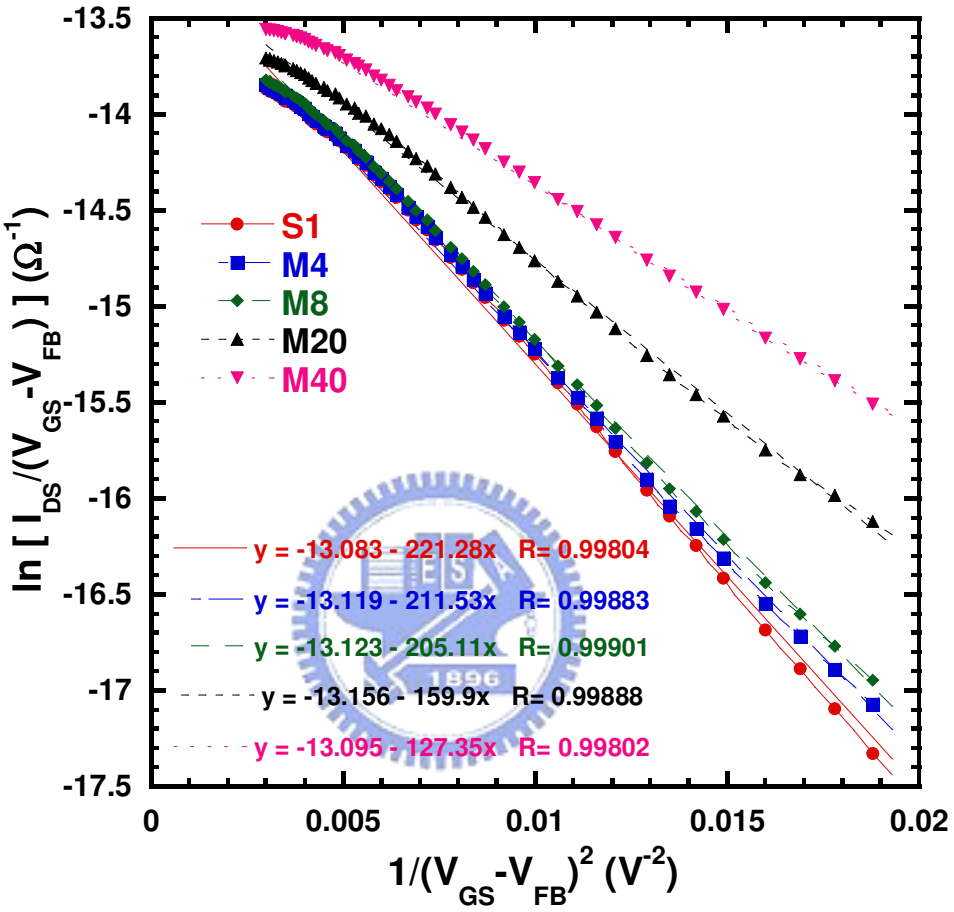


Fig. 3-8 Trap state density extraction of the conventional and the proposed p-channel multi-channel poly-Si TFTs with different stripes of channel.

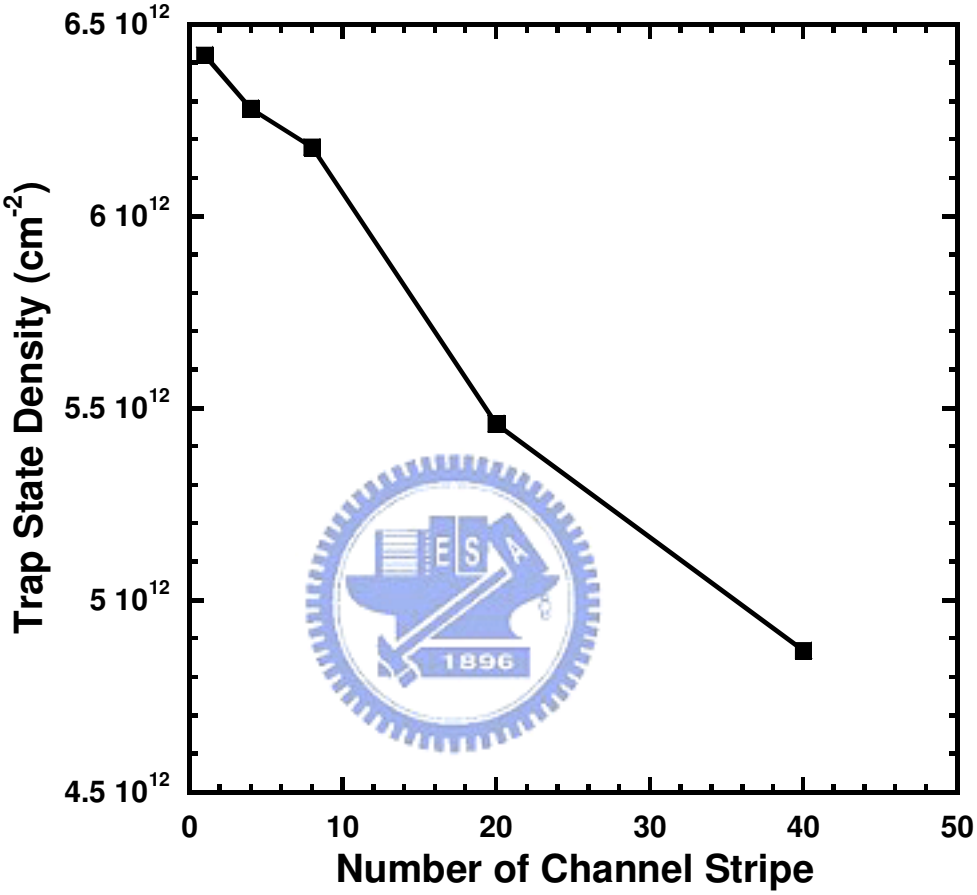


Fig. 3-9 Trap state density of the proposed p-channel multi-channel poly-Si TFTs with different stripes of channel.

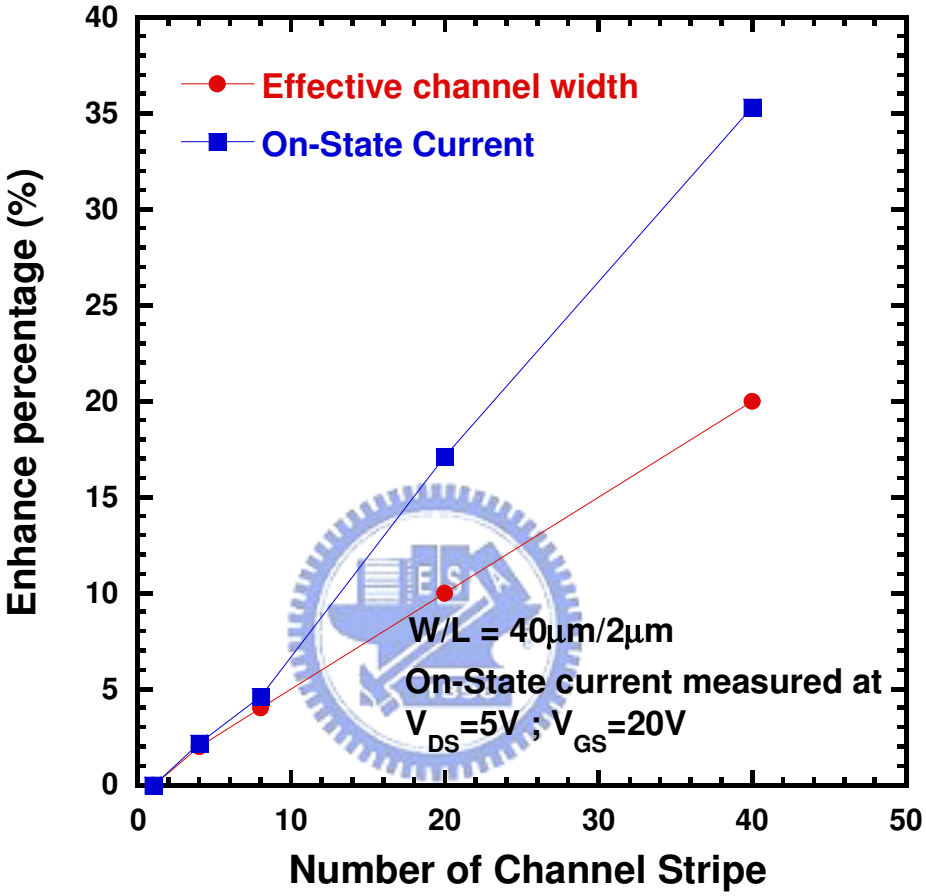


Fig. 3-10 Increasing ratio of the effective channel width and the on-state current as a function of number of channel stripes.

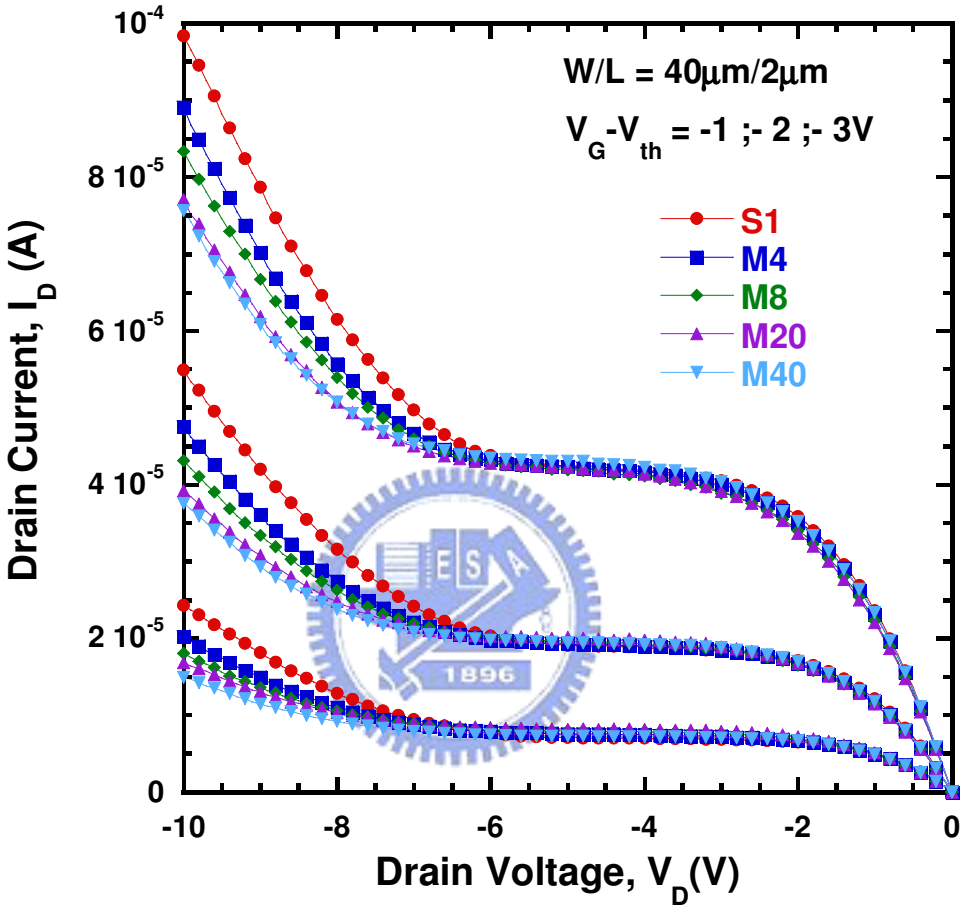
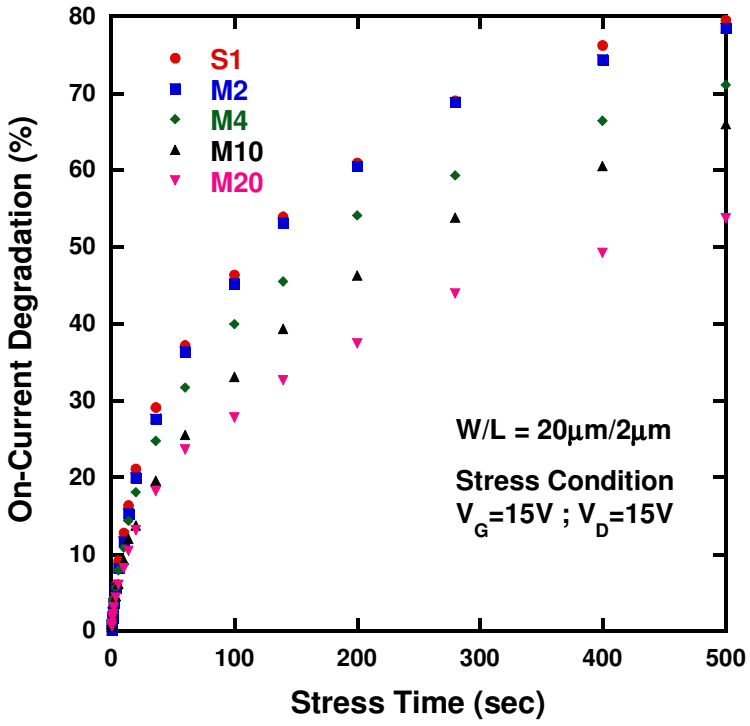
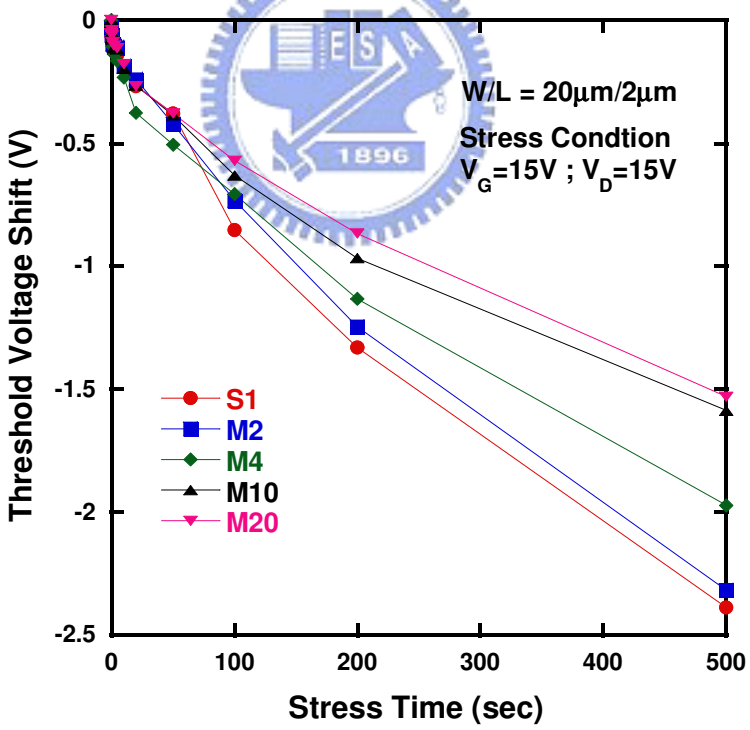


Fig. 3-11 Output characteristics of the conventional and the proposed p-channel poly-Si TFTs with different stripes of channel. ($V_G - V_{th}$ = 1; 2; 3V)



(a) On-state current degradation with stress time



(b) Threshold voltage degradation with stress time

Fig. 3-12 (a) on-current, and (b) threshold voltage degradation as a function of stress time under hot-carrier stress.

Chapter 4

Investigated the lifetime of low temperature poly-Si TFTs with different dimension of channel

4.1 Introduction

Poly-Si TFTs have received much attention in recent years because of their applications. , such as active matrix liquid crystal displays (AMLCDs) [1] , active matrix organic light emitting displays (AMOLEDs) [2] , high density static random access memories (SRAMs) [3], electrical erasable programming read only memories (EEPROM) [4] and candidate for 3-dimenstion ICs' applications [5] . Although, it have many studies to improve performance of poly-Si TFTs. However, the lifetime issues of poly-Si TFTs are not well studied. Because body contact is a lack of poly-Si TFTs, the floating body effect will influence the reliability of device. To date, there still does not exit a clear consensus on the hot-carrier effect of these devices compared to bulk. For this reason, we interest in studying of lifetime of poly-Si TFTs.

The investigated of lifetime issue in MOSFET have been well-studied. For MOSFET, drain-avalanche-hot-carrier (DAHC) injection, based on impact ionization near the drain, causes the severest damage on the device's characteristics. The device's degradation depends on the trap states generation, which is also proportional to the substrate current (I_{sub}) [6]. Therefore, DAHC-induced I_{sub} is used to monitor the device degradation and to predict the device lifetime. Under the severest DAHC stress, the empirical model for the lifetime prediction has been reported. It showed a single slope lifetime projection.

Due to the lack of body terminal in poly-Si TFT, holes generated during impact ionization will be recombined with electron as they flow to the channel, or they will accumulate in the substrate near the source. The injection of holes into the body will lowers the potential barriers between the source and the channel. When the voltage drop across the body-source junction is large enough, the parasitic bipolar transistors (PBT) will be turned on. The action of PBT will enhance the on-current and then increase the device degradation rate [7]. Therefore, PBT should be considered as predicting the lifetime of poly-Si TFTs. In this chapter, we used the conventional empirical extrapolating method of MOSFETs to predict the lifetime of poly-Si TFTs. However, there was apparent dual slop lifetime versus the reciprocal drain voltage behavior in wide range drain stress voltages (V_{DS}). Typically, extrapolation of the lifetime to low drain voltages can be made from results obtained by stressing at large drain voltages. So, it will make wrong lifetime extraction in poly-Si TFTs. We also investigated influence of channel dimension about lifetime in poly-Si TFTs. It showed different phenomena in short and long channel device due to PBT effect. We will discuss this in detail in a later section.

4.2 Experiment

Figure 4-1 and 4-2 show the process flow and cross-sectional view of the investigated poly-Si TFT. First, 500-nm-thick thermal oxide was grown on the Si wafer by using a furnace system. All the experimental devices in this study were fabricated on thermally oxidized Si wafers. Then, 100-nm-thick amorphous silicon layers were deposited on the thermal oxide layer using a low-pressure chemical vapor deposition (LPCVD) system at 550°C. Then, amorphous silicon films were recrystallized by solid phase crystallization (SPC) method at 600°C for 24 hours in an N_2 ambient to form poly-Si films. Poly-Si films were patterned into active regions by

transformer couple plasma (TCP) etching system using mixture gases of Cl_2 and HBr.

After RCA cleaning procedure, a 50-nm-thick TEOS oxide was deposited by LPCVD with TEOS and O_2 gases at 695°C to form the gate insulator. A 150-nm-thick poly-Si was deposited to serve as the gate electrode by LPCVD at 595°C. Then, the poly-Si film was patterned and etched by TCP etching system to form the gate electrode and the gate oxide on source/drain was removed using dilute HF solution. The regions of source, drain, and gate were doped by a self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15}ions/cm^{-2} and 30keV, respectively. The dopant activation was performed by rapid thermal annealing (RTA) system at 700°C for 30sec, followed by a deposition of 400nm-thick passivation oxide using PECVD system at 350°C and the definition of contact holes. Finally, a 500-nm-thick Al was deposited by sputter and patterned for metal pads, and devices were passivated by NH_3 plasma treatment for 1 hour at 300°C. The transfer characteristics of the poly-Si TFT is shown in Fig. 4-3.

4.3 Result and Discussion

Impact ionization near the drain is a main mechanism to cause substantial trap states at the interface for MOSFETs under a hot carrier stress. From the empirical model, the I_{on} degradation can be expressed as

$$\Delta I_{on} / I_{on0} = A \times t^{n} \quad \text{---------- (Eq. 4.1)}$$

The magnitude of degradation, A, which has physical meaning as the number of excess carrier generated by impact ionization, has been known to have the V_{DS} dependency:

$$A \propto \exp(-a / V_{DS}) \quad \text{---------- (Eq. 4.2)}$$

where a is a constant. On the other hand, the peak substrate current (I_{sub}) and the

increase of trap states, which are also proportional to the number of electron-hole pairs generated by impact ionization, can be also expressed in the same dependency [8][9].

$$N_{it} \propto I_{sub} \propto \alpha \propto \exp(-c/E) \propto \exp(-c/V_{DS}) \propto A^{c/a} \quad \text{---------- (Eq. 4.3)}$$

where α is the impact ionization factor, c is a constant, and E is the local electric field near the drain. Using (Eq. 4.2), (Eq. 4.3), and (Eq. 4.4), the lifetime (τ) of the MOSFET under a certain criterion can be expressed as:

$$\tau \propto \exp(b/V_{DS}) \quad \text{---------- (Eq. 4.4)}$$

where b is also a constant. In equation 4-4, we can see that the lifetime proportional to the reciprocal drain voltage at log-scale and only single lifetime projection in this conventional empirical model. In this chapter, we will use this conventional empirical model to investigate the lifetime of poly-Si TFTs.

First, we define the worst case of hot carrier stress of poly-Si TFTs. It has been demonstrated that the worst-case hot carrier degradation for MOSFET is known to be under V_G=1/2 V_D [10]. However, due to the PBT action, the worst-case degradation for SOI-MOSFETs is $V_G \approx V_{th}$ [11]. However, the worst-case hot carrier degradation for poly-Si TFTs have not been investigated well and few reports emphasized the relationship between the worst-case hot carrier degradation and the channel dimension. Fig. 4-4 shows the on-current degradation under stress conditions of V_G=1/2V_D and V_G=V_{th} at V_{DS}=16V for different channel geometry. Fig. 4-4(a) shows the on-current degradation rate of the channel length L=10μm and the channel width W=10μm. In this channel geometry, we found that the V_G=1/2V_D cause severest damage of poly-Si TFTs. Fig.4-4(b) shows the on-current degradation rate of the channel length L=2μm and the channel width W=10μm. In this channel geometry, we found that the V_G= V_{th} cause severest damage of poly-Si TFTs. Fig.4-4(c) shows the on-current degradation

rate of the channel length L=2μm and the channel width W=2μm. In this channel geometry, we found that the $V_G = V_{th}$ also cause severest damage of poly-Si TFTs. We make a conclusion that the worst-case hot carrier degradation for poly-Si TFTs relate to the channel length significantly. In short channel device, the worst-case condition is $V_G = V_{th}$. However, the worst-case condition is $V_G = 1/2\ V_D$ in long channel device.

Following, the DC stress $V_G = V_{th}$, wide drain voltage and source grounded was performed for 1000sec with different channel geometry. Fig. 4-5 shows the lifetime extraction of poly-Si TFTs with channel length of 10μm and channel width of 10μm. The on-current variation is a function of stress time with various V_{DS} as shown in Fig. 4-5(a). As can be seen, the slope *n*, in log-log plot depends on the V_{DS} strongly. Obviously, two sets of slopes can be observed. The slopes for high V_{DS} stress conditions are higher than the low V_{DS} stress conditions'. Fig. 4-5(b) presents the lifetime (τ) as function of the reciprocal V_{DS}. The lifetime is defined as the time taken for 10% I_{on} degradation. We found the dual slopes lifetime projection in wide drain voltage. The slopes for high drain voltage region are lower than the low drain voltage region's. This indicated that high drain voltage region cause severest damage of poly-Si TFTs. This phenomenon will be discussed later. Fig. 4-6 shows the lifetime extraction of poly-Si TFTs with channel length of 2μm and channel width of 10μm. The on-current variation is a function of stress time with various V_{DS} as shown in Fig. 4-6(a). It also can be found that the slope *n* depends on the V_{DS} and two sets of slopes appeared in this figure. The slopes for low V_{DS} stress conditions are higher than the high V_{DS} stress conditions'. A similar tendency has been investigated in SOI MOSFETs [12][13] . Fig. 4-6(b) presents the lifetime (τ) as function of the reciprocal V_{DS}. We can see the dual slopes lifetime projection in wide drain voltage. The slopes for low drain voltage region are lower than the high drain voltage region's. This illustrated that low drain voltage region cause severest damage of poly-Si TFTs. We

are also interested in the lifetime issues of different channel width. Fig. 4-7 shows the lifetime extraction of poly-Si TFTs with channel length of 2μm and channel width of 2μm. Fig 4-7(a) shows the on-current variation as a function of stress time with various V_{DS}. Fig. 4-7(b) presents the lifetime (τ) as function of the reciprocal V_{DS}. It is obviously that Fig. 4-6 and Fig. 4-7 have the same tendency. We deduced that the lifetime issue greatly depends on channel length. We explained these phenomenons of above as following.

So, when predicting the lifetime of poly-Si TFTs, the PBT phenomenon must be considered. Figure 4-8 shows the current generation in the poly-Si TFTs with a floating body. In this figure, the intrinsic drain current (I_D) induces a hole current (I_{sub}) due to impact ionization near the drain side, and the I_{sub}, which flows to the source induces a bipolar electron current (I_e), can be expressed as:

$$I_{sub} = (M-1)I_D \quad \text{---------- (Eq. 4.5)}$$

The bipolar electron current (I_e) can be expressed as:

$$I_e = (\beta+1)I_{sub} = (\beta+1)(M-1)I_D \quad \text{---------- (Eq. 4.6)}$$

where β is the bipolar current gain, and M is the impact-ionization multiplication factor, which can be expressed as:

$$(M-1) = \int \alpha dy \quad \text{---------- (Eq. 4.7)}$$

Then, I_e which injects into the channel will enlarge I_D, and enhance impact ionization near the drain to generate higher I_{sub}.

$$I'_D = I_D + I_e = [1+(\beta+1)(M-1)]I_D \quad \text{---------- (Eq. 4.8)}$$

$$I'_{sub} = [(M-1)+(\beta+1)(M-1)^2]I_D \quad \text{---------- (Eq. 4.9)}$$

Therefore, using (Eq. 4.6), (Eq. 4.7), (Eq. 4.9), and (Eq. 4.10), a general form of I_{sub} is derived and expressed as

$$I_{sub} = (M-1)\left\{\frac{\left[(\beta+1)^n (M-1)^n - 1\right]}{\left[(\beta+1)\ (M-1)\ - 1\right]}\right\}\ I_D \approx (\beta+1)^{n-1}(M-1)^n I_D \quad \text{-------- (Eq. 4.10)}$$

Where *n* is a positive integer. From (Eq. 4.4) and (Eq. 4.5), it is demonstrated that τ is proportional to the reciprocal I_{sub}. So, it can be expresses as:

$$\tau \propto 1/(\beta+1)^{A_0}(M-1)^{B_0} \quad \text{---------- (Eq. 4.11)}$$

where A_0 and B_0 are constant. As can be seen, this form shows the lifetime prediction including both impact ionization and PBT effects.

Moreover, it has been investigated by using simulation method that β varies with V_{DS} [14]. The β decreases dramatically with increasing V_{DS} [14]. This can be explained by the high current injection [14][15]. Therefore, under high V_D stress condition, (*M*-1) is large and β is small, which can be neglected. Then, $\tau \propto 1/(M-1)^{B_0}$, which means that the impact ionization is almost the only factor to degradation device. However, under low V_D stress condition, β is large. In this condition, the PBT action must be considered. So, we can see that low drain voltage region cause severest damage of poly-Si TFTs for short channel device as shown in Fig. 4-6 and Fig. 4-7. However, it has opposite tendency in long channel device as shown in Fig. 4-5. We illustrated that as following. Impact ionization occurs near the drain side and electron flows into drain electrode. However, hole flows to bottom of channel and source side due to vertical electric field and lateral electric field, respectively. Recombination mechanism will occurs when hole flows in the channel. Then, the hole that flows to the source side decreases due to moving in the long channel. However, a small number of the hole near the source side can't raise potential enough to turn on the parasitic BJT. As this condition, the increasing of lateral electric field will make the number of the hole that flows to the source side increasing. The parasitic BJT will be turned on as drain voltage increasing. So, Fig.

4-5 shows that high drain voltage region cause severest damage of poly-Si TFTs. This is also due to parasitic BJT effect.

4.4 Summary

The Lifetime issue of poly-Si TFTs with different channel geometry has been investigated. The worst-case of stress conditions is under $V_G \approx V_{th}$ not $V_G = 1/2\ V_D$ in short channel poly-Si TFTs. Moreover, I_{on} degradation under both high and low V_D of stress conditions has different phenomena. This is due to not only impact ionization but also parasitic bipolar junction transistor effect to degradation poly-Si TFTs. Then, it is found that lifetime extraction of poly-Si TFTs is not the same with that of MOSFETs. There are dual slopes lifetime projections in wide drain voltage. We can't use the high drain voltage to accelerate degradation of poly-Si TFTs as before because this method will extract wrong lifetime.

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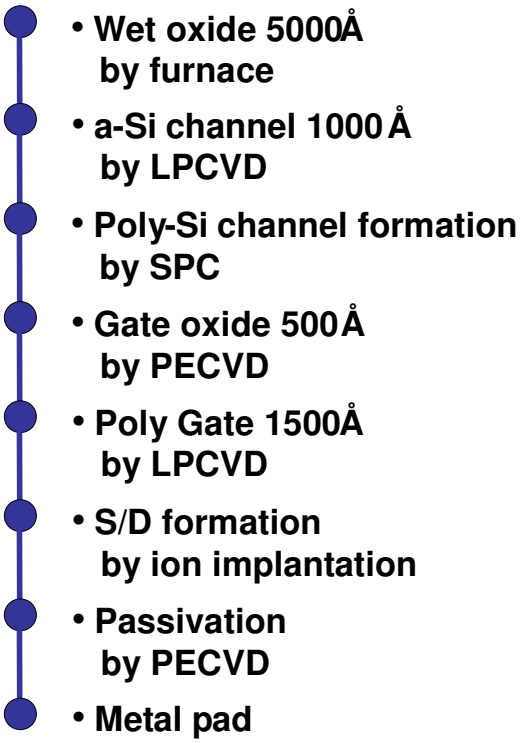


Fig. 4-1 Process flow of the conventional poly-Si TFTs.

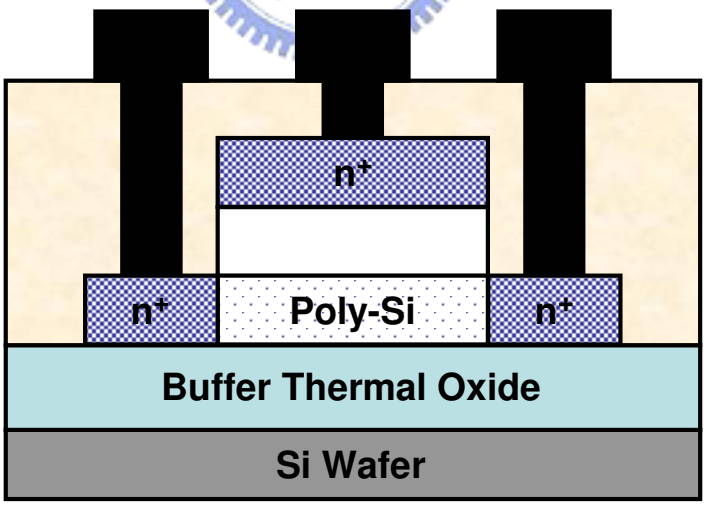


Fig. 4-2 Cross-section of the conventional poly-Si TFTs.

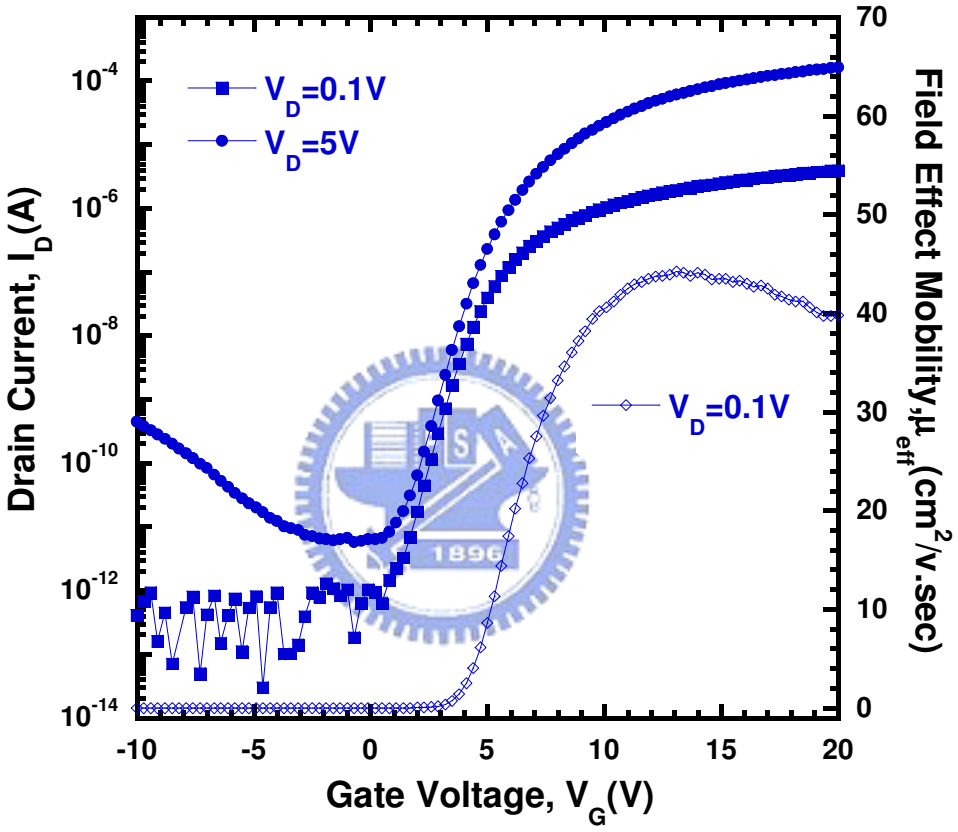
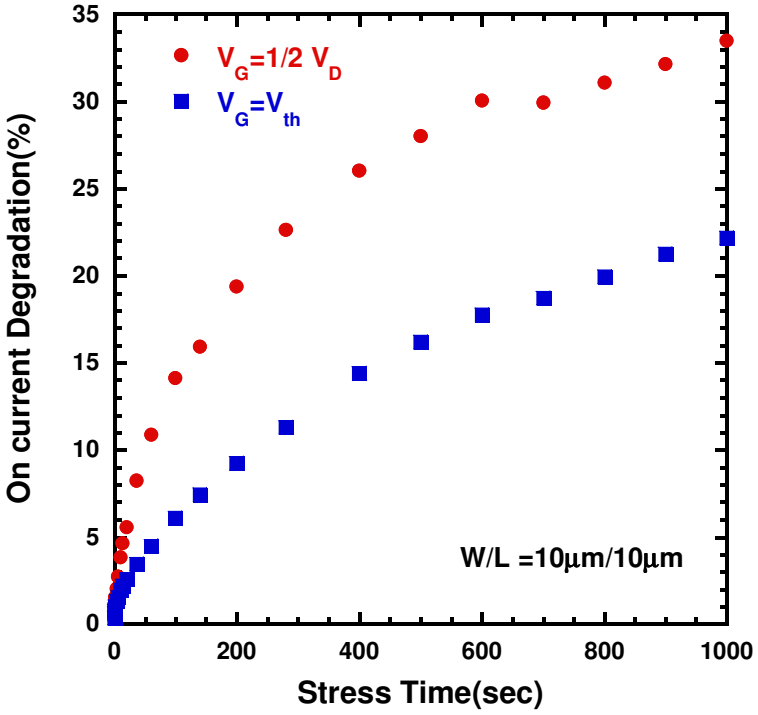
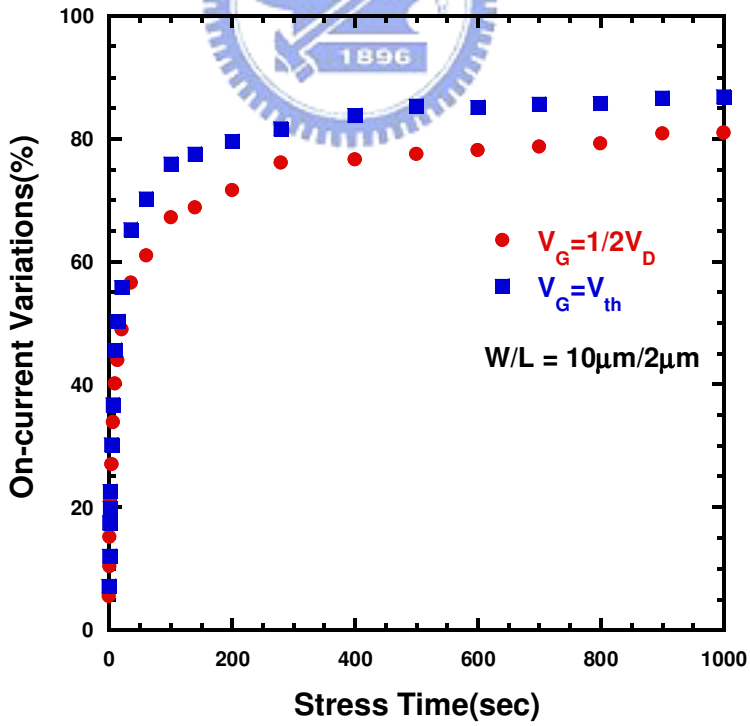


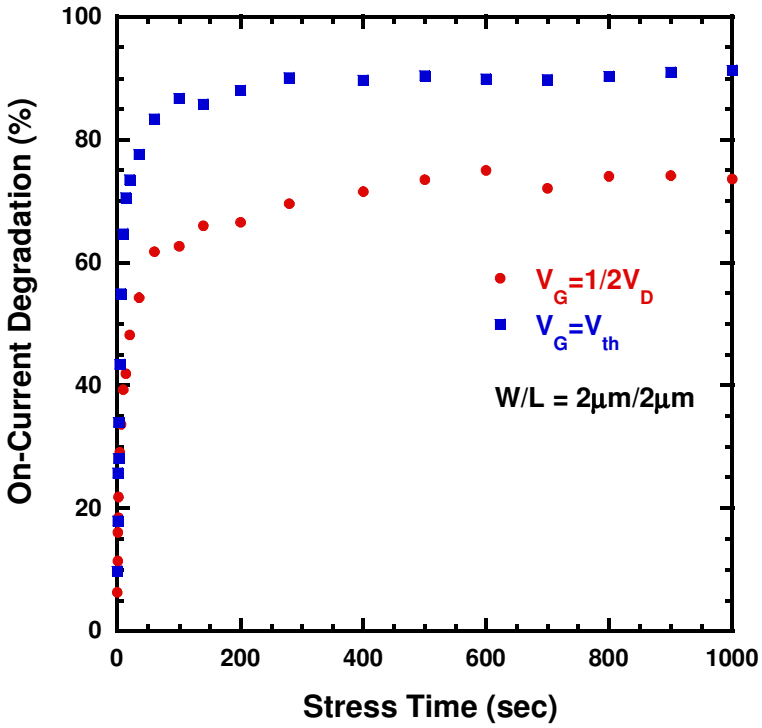
Fig. 4-3 Transfer characteristics of the conventional poly-Si TFTs



(a) channel length L=10μm ; channel width W=10μm

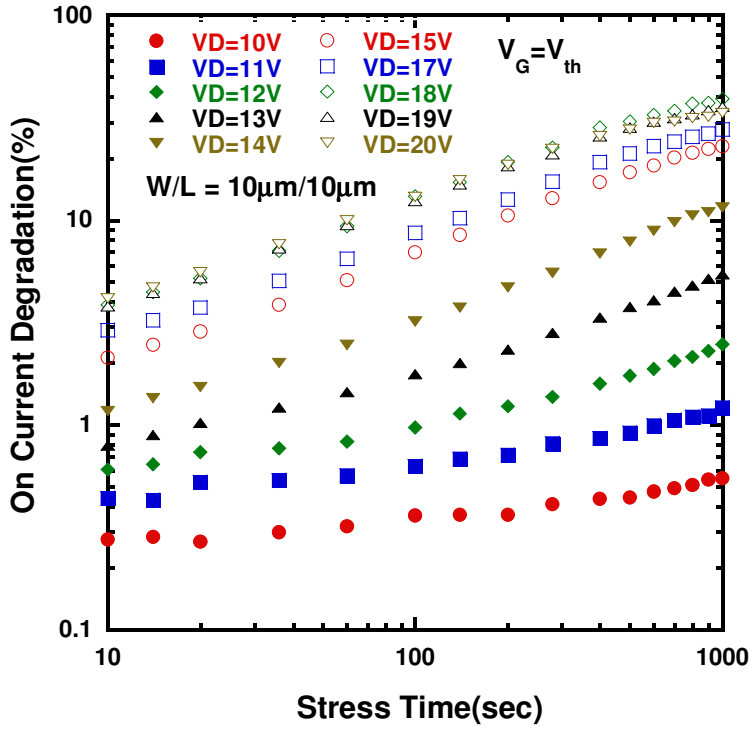


(b) channel length L=2μm ; channel width W=10μm

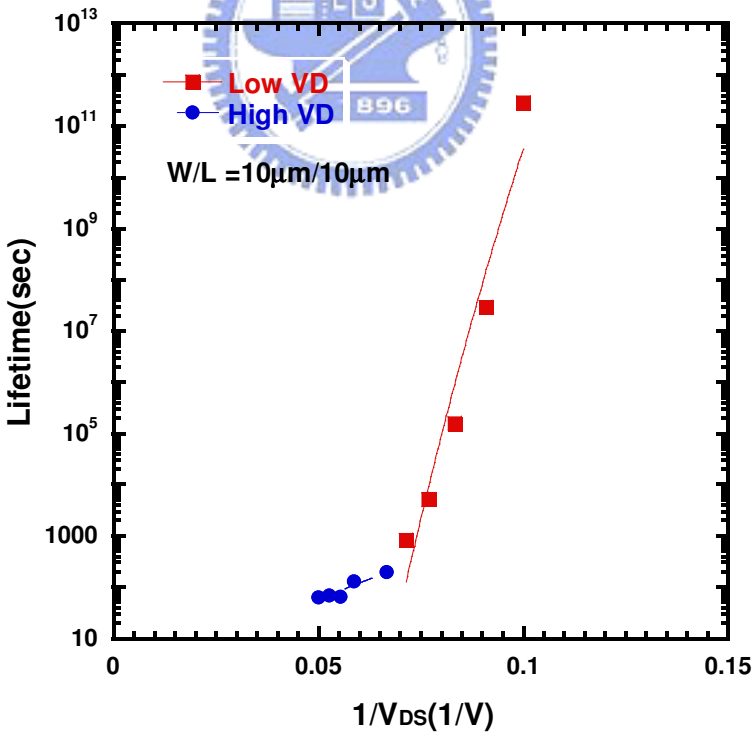


(c) channel length L=2μm ; channel width W=2μm

Fig. 4-4 On-current degradation under stress conditions of V_G=1/2V_D and VG=V_{th} at V_{DS}=16V for different channel geometry

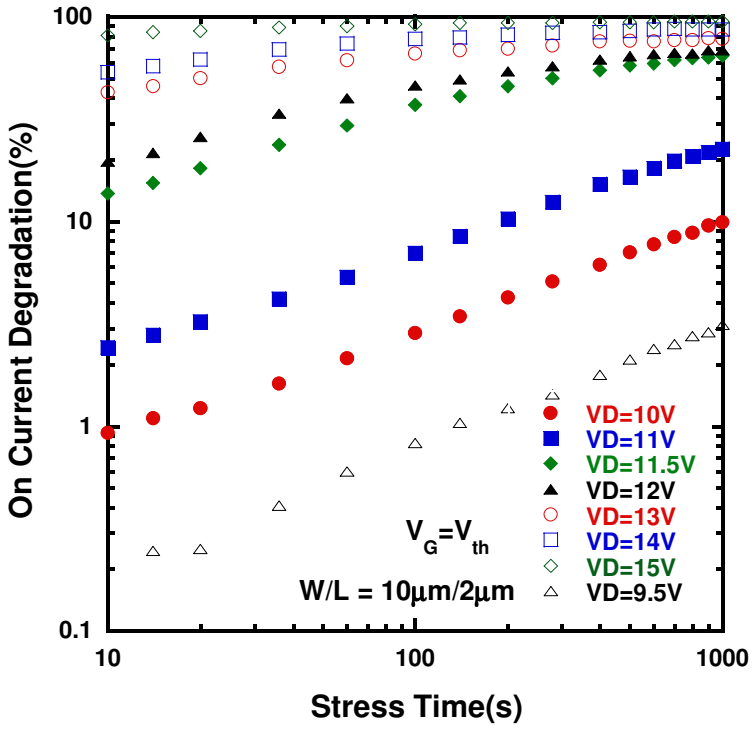


(a) On-current degradation as a function of stress time with stress drain voltage (V_{DS}) as a parameter

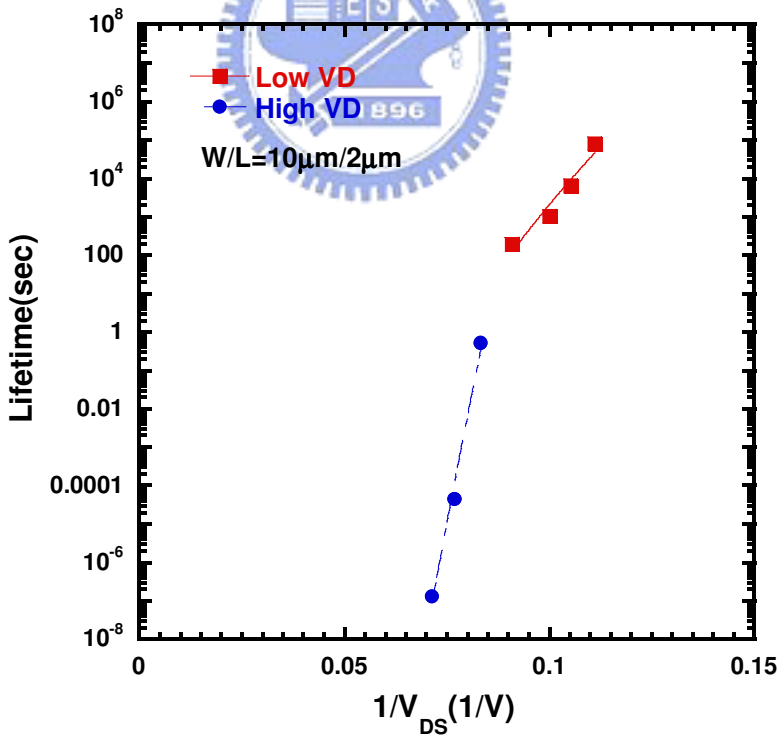


(b) Lifetime as function of the reciprocal drain voltage stress for poly-Si TFTs stressed as $V_{GS}=V_{th}$ with V_{DS} of wide range

Fig. 4-5 Lifetime extraction of poly-Si TFTs with channel length of 10µm and channel width of 10µm

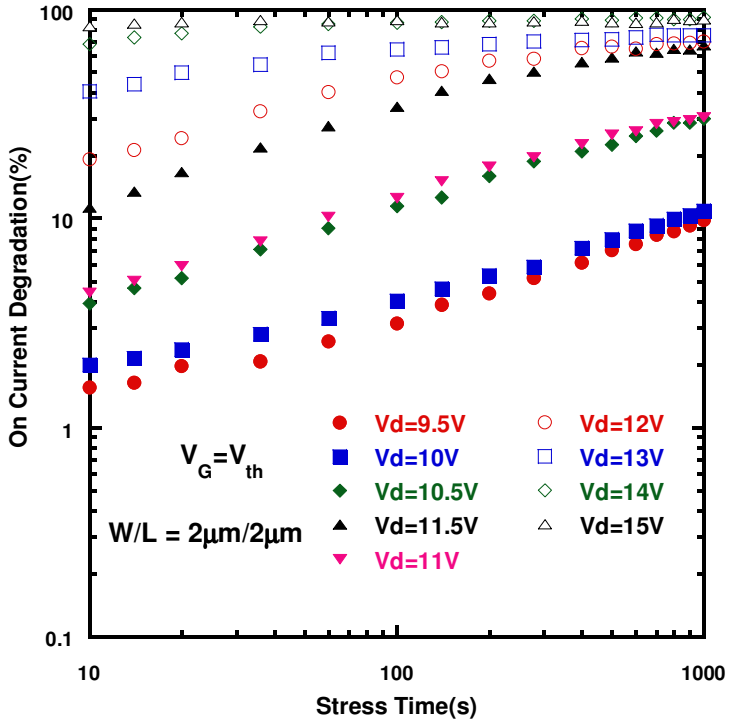


(a) On-current degradation as a function of stress time with stress drain voltage (V_{DS}) as a parameter

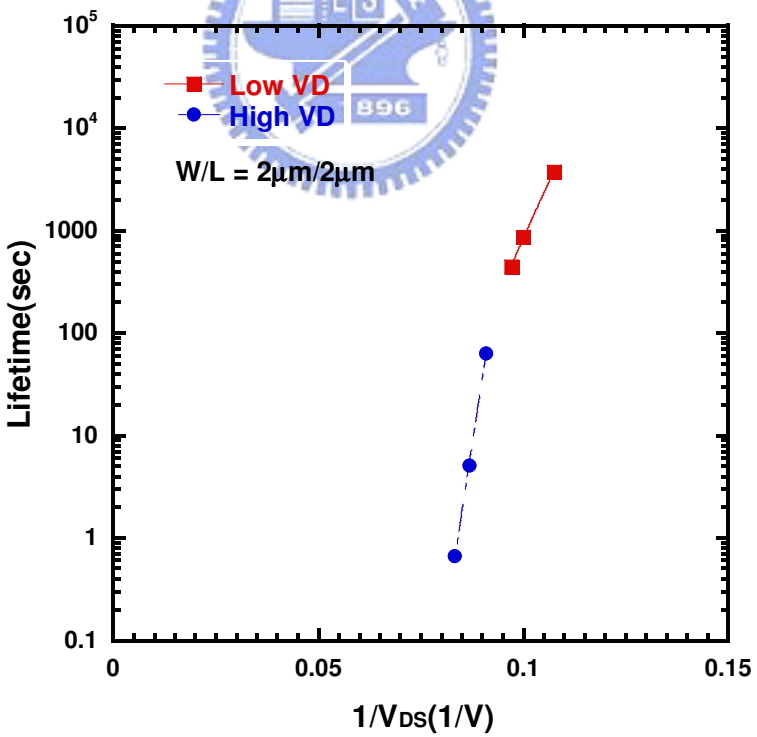


(b) Lifetime as function of the reciprocal drain voltage stress for poly-Si TFTs stressed as $V_{GS}=V_{th}$ with V_{DS} of wide range

Fig. 4-6 Lifetime extraction of poly-Si TFTs with channel length of 2µm and channel width of 10µm



(a) On-current degradation as a function of stress time with stress drain voltage (V_{DS}) as a parameter



(b) Lifetime as function of the reciprocal drain voltage stress for poly-Si TFTs stressed as $V_{GS}=V_{th}$ with V_{DS} of wide range

Fig. 4-7 Lifetime extraction of poly-Si TFTs with channel length of 2μm and channel width of 2μm

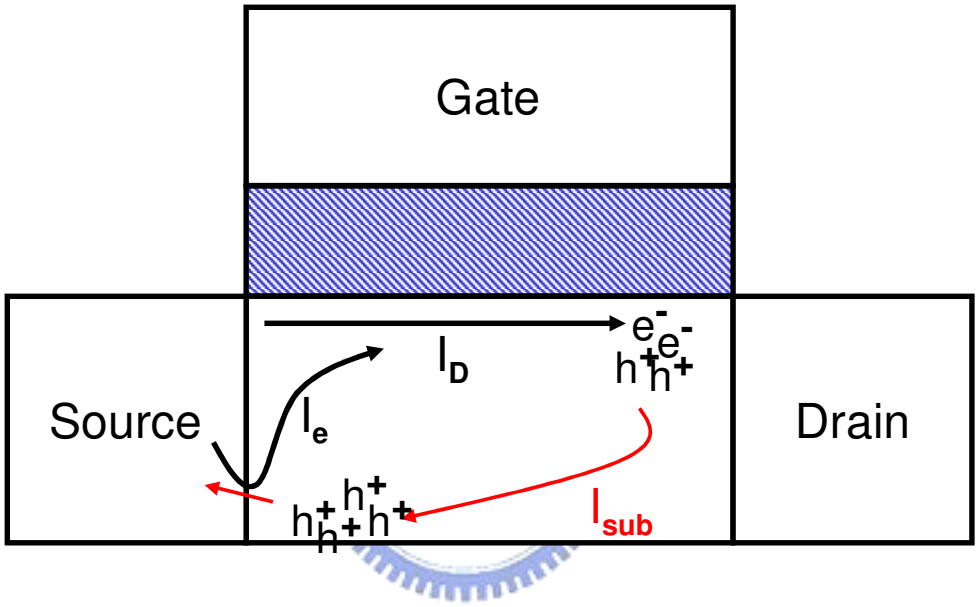


Fig. 4-8 Schematical plot of the occurrence of impact ionization and bipolar multiplication in the poly-Si TFTs.

Chapter 5

Conclusions

This thesis includes three topics. First, we fabricated high performance TFTs with capping silicon nitride layer. The characteristic of proposed TFTs have great improvement, such as higher on-current, higher mobility, lower subthrehold swing, suppressing kink effect and GIDL effect and good reliability. The improvement of performance is due to two reasons. First, nitride capping layer has tensile strain and further forming compressively strained polysilicon gate electrode and then give a tensile stress on the channel. Second, similar high-k spacer induced source/drain electron easy when device operated. It causes reducing of source/drain series resistance. The improvement of reliability is due to the fact that similar high-k spacer reduced lateral electric field. So, the kink effect and the reliability were improved. The process of proposed TFTs is uncomplicated and no need of extra mask step. We believe that the proposed TFTs will be candidate in high performance TFTs application.

Then, the effects of the numbers of the channel strips in P-type multi-channel TFTs on the performance and reliability have been investigated. As the stripes increased, the electrical characteristics of devices were improved significantly due to the effective width increasing and the enhancement of gate control capability. Then, the reliability was improved with stripes of channel due to tri-gate structure induced large depletion region in the channel so that fewer electron accumulation in the channel region. The floating body effect and effect of parasitic bipolar junction

transistor will be suppressed. So, the reliability of multiple channel poly-Si TFTs were improved. The n-type multi-channel TFTs have been investigated in previous reports. So, we might integrate n-type and p-type multi-channel TFTs to CMOS application. Furthermore, using CMOS technique applies to 3-D circuit applications.

Finally, The Lifetime issue of poly-Si TFTs with different channel geometry has been investigated. The worst-case of stress conditions is under $V_G \approx V_{th}$ not $V_G=1/2\ V_D$ in short channel poly-Si TFTs. Moreover, I_{on} degradation under both high and low V_D of stress conditions has different phenomena. This is due to not only impact ionization but also parasitic bipolar junction transistor effect to degradation poly-Si TFTs. Then, it is found that lifetime extraction of poly-Si TFTs is not the same with that of MOSFETs. There are dual slop lifetime projections in wide drain voltage. We also found that the lifetime extraction of the short channel and long channel device shows the opposite tendency. We can't use the high drain voltage to accelerate degradation of poly-Si TFTs as before because this method will extract wrong lifetime.

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The Investigation of Mobility and Reliability of Low Temperature Poly-Si Thin-Film Transistors

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