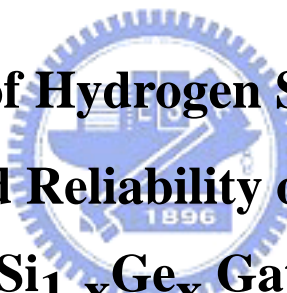


國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

氫含量對於矽鍺閘極元件之特性與可靠度分析



**The Effect of Hydrogen Species on the
Performance and Reliability of Transistors with
 $\text{Si}_{1-x}\text{Ge}_x$ Gate**

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中華民國九十五年六月

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摘要

在本研究中，我們探討了不同氫含量對於具有矽鍺閘極的深次微米電晶體的性能影響和可靠度分析。使用矽鍺當P型金氧半場效電晶體 (PMOSFETs) 之閘極有許多優點，包括有效降低閘極空乏效應並且改善閘極片電阻。為了改變在電晶體中的氫含量，元件分成三種不同的製程條件。對照的樣本是使用氮氫混合氣體退火(forming gas anneal)，另一種條件則是採用氮氣退火，第三種條件則是在的TEOS覆蓋層之前先使用電漿增強式化學氣相沈積一層氮化矽。我們研究不同條件的P型金氧半場效電晶體的負偏壓溫度不穩定特性(NBTI)。氮氫混合氣體退火和具有氮化矽覆蓋層的元件都可以有效地修補界面的缺陷，但是二者具有不同的臨界電壓。雖然氮化矽覆蓋層可以大量地降低界面狀態密度，並且增加反轉層的電容，但從結果可看出覆蓋的氮化矽層會使得NBTI特性變得更

差。使用電漿增強式化學氣相沈積的氮化矽含有大量的氫，也就是使可靠度惡化的主要原因。然而，使用氮氫混合氣體退火展現出不同的行為。值得注意的是，使用氮氫混合氣體退火或氮氣退火在基本電性以及負偏壓溫度不穩定特性上具有幾乎相同的趨勢，唯獨在一開始的界面狀態密度界不同。而具有氮化矽覆蓋的元件，不論使用氮氫混合氣體退火或氮氣退火皆具有相同的特性。電性回復效應可以有效降低界面狀態的產生，因此動態負偏壓溫度不穩定性與交流應力也被用來模擬電路中元件的操作特性。我們觀察到，交流應力頻率強烈影響具有氮化矽覆蓋層元件之臨界電壓改變、與界面態位之產生。



The Effect of Hydrogen Species on the Performance and Reliability of Transistors with $\text{Si}_{1-x}\text{Ge}_x$ Gate

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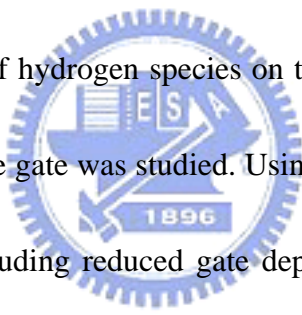
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Abstract



In this work, the effect of hydrogen species on the performance and reliability of deep submicron transistors with SiGe gate was studied. Using SiGe as gate material of PMOSFETs has numerous advantages, including reduced gate depletion effect and improved gate sheet resistance. To set various hydrogen contents in the test transistors, wafers were split three ways. Specifically, the control split was annealed in forming gas, while the N_2 -split was annealed in nitrogen ambient and the SiN-split received an extra PE-SiN layer in addition to the normal TEOS passivation. Negative bias temperature instability (NBTI) characteristics of PMOSFETs of all splits were investigated. Both forming gas and SiN capping can effectively passivate interface states, and result in threshold voltage difference. Although SiN capping would greatly reduce interface state density and increase inversion capacitance, our results indicate that the SiN capping may simultaneously aggravate the NBTI characteristics. An

abundant hydrogen species contained in the PE-SiN layer may be the culprit for the worsened reliability. However, forming gas anneal shows a different behavior. In particular, forming gas and N₂ anneals result in almost identical electrical characteristics and NBTI behaviors, albeit their fresh D_{it} is quite different. Unlike SiN capping, the NBTI characteristics of PMOSFETs receiving either forming gas or N₂ gas anneal are nearly identical. Dynamic NBTI and AC stress characteristics were used to simulate the switching operation of PMOSFETs in circuits, the electric passivation effect effectively reduces the interface states generation. Both threshold voltage shift and interface states generation are strongly dependent on frequency for devices with SiN capping layer.



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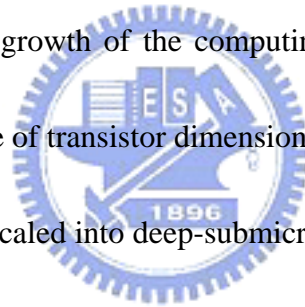


Chapter 1

Introduction

1.1 General Background

The famous “Moore’s Law”, proposed by Gordon Moore in 1965 [1], states that the number of transistors on integrated circuits doubles every 24 months. For the past four decades, the advancement in IC industry more or less followed this intelligent foresight in its pursuing better performance with lower cost. It can be said that “Moore’s Law” is the basis for the overwhelmingly rapid growth of the computing power. In order to keep close pace with “Moore’s Law”, shrinkage of transistor dimensions is needed.



As CMOS technology is scaled into deep-submicron regime for higher density and speed, thinner gate oxide is required to provide sufficient current drive while the supply voltage is scaled down. Ultra-thin gate oxide (<2nm) has been reported in CMOS devices [2,3]. With such thin oxides, the poly-depletion effect (PDE) and boron penetration have become critical issues. These technical issues impose strict limitations on the process window and may degrade device performance [4,5]. To alleviate these problems [6,7], the Poly-SiGe has been proposed as a promising alternative gate material by taking advantage of its lower PDE and boron penetration. Process compatibility with existing Si technology has been demonstrated and significant improvements of deep-submicron PMOS transistor performance have been

observed [8].


Since the melting point of SiGe is lower than that of Si, physical phenomena controlling fabrication processes, such as deposition, crystallization, grain growth, and dopant activation, occur at a lower temperature for SiGe than for Si. Thus, lower process temperature can be used for fabricating devices with poly-SiGe gate. It is thus preferable to poly-Si for various applications in technologies that have limited thermal budget tolerance.

With the continuous shrinking of the MOS transistor dimensions, additional reliability issues emerge. A number of characterization schemes, such as time- or charge-to-breakdown (T_{BD} or Q_{BD}), hot carrier stress, and negative-bias-temperature-instability (NBTI) test, have been developed to evaluate the reliability of dielectrics as well as to predict the lifetime of the MOS device. As the oxide thickness is thinned down to the regime of 3nm or less, hot carrier effects become less important due to the reduced operation voltage [9,10]. On the other hand, negative-bias-temperature instability (NBTI) of pMOSFETs with ultra-thin gate dielectrics has been reported as one of the most serious reliability issues for modern scaled CMOS devices due to the large threshold voltage shift and drive current degradation [11-13]. The NBTI degradation may even become the major factor in limiting the device lifetime when the gate oxide thickness is scaled down to 3.5 nm and less. Despite many research efforts, detailed NBTI degradation mechanism is not yet fully understood. This is further complicated by the fact that the NBTI is affected by several other factors, such as hydrogen incorporation

and boron penetration.

Conventional NBTI testing is based on static experimental data. The measurements disregard the electric passivation effect [14,15] of the interface traps during the operation of PMOSFETs in digital circuits, and therefore overestimate the degradations of PMOS devices. In this aspect, results of dynamic NBTI (DNBTI) stress measurements are much closer to the situation of practical circuit operation. Therefore, it is important to investigate NBTI under such dynamic stress conditions.

1.2 Brief Review of SiGe Gate Technology



Technical challenges emerge as the critical dimensions of semiconductor devices are scaled down to the deep-submicron regime in a pursuit of higher levels of integration and performance. The dual-gate process has replaced the conventional single-gate process for advanced CMOS fabrication. For dual-gate process, boron penetration through the gate oxide from the p⁺-doped gate of pMOSFETs becomes a major concern. In addition, gate-depletion effect due to insufficient dopant activation at the gate/dielectric interface becomes more significant as gate oxide thickness is scaled down, and leads to the degradation of the drive current.

To alleviate the above-mentioned problems, poly-SiGe has been proposed as a promising alternate gate material to replace the conventional poly-Si gate. First, the dopant activation in

poly-SiGe is better than in poly-Si for p-type gate material [16,17]. Besides, the p-type poly-SiGe film has lower resistivity, reduced gate-depletion effect, and suppressed boron penetration, thanks to the higher dopant activation ratio comparing with poly-Si film. The mechanism of the improved boron activation is presumably caused by the local strain compensation due to the difference in atomic radii between Si and B atoms [18].

When p^+ poly-Si is substituted by p^+ poly-SiGe as the gate material for the PMOS device, the change in the gate to semiconductor work-function difference, Φ_{ms} , can be approximately calculated as the difference in the energy bandgaps between the two heavily-doped materials, i.e., $\Delta\Phi_{ms} = E_G^{poly-Si} - E_G^{poly-SiGe}$. This is due to the fact that the position of the conduction band edge of the materials remains essentially unchanged regardless of the Ge incorporation. For high Ge concentration, a significant amount of stress contained in the poly-SiGe grains results in an extra reduction of the gate work-function [19].

In order to retain the threshold voltage at a specific value, one can change Φ_{ms} by reducing the channel doping. As a result, hole mobility is enhanced due to the reduction of Coulomb scattering centers in the channel region. The drive current is thus increased. The subthreshold swing could also be reduced due to decrease in the depletion layer capacitance, leading to an improved I_{on}/I_{off} ratio. The reduction of the body factor results in weaker threshold voltage dependence on variations of the substrate potential.

The dopant activation temperature could be reduced owing to the lower melting point of

poly-SiGe films [20], and this is conducive to reducing the process thermal budget. The poly-SiGe alloy films also have good compatibility with standard CMOS processing.

1.3 Organization of This Thesis

In this thesis we investigate the effect of hydrogen species on the performance and reliability of PMOSFETs devices with SiGe gate. This thesis is divided into four chapters.

In Chapter 2, we briefly describe the key process flow for fabricating the PMOS devices with the SiGe gate. In order to verify the effect of hydrogen species under NBTI stress, splits with different hydrogen incorporations are fabricated and characterized. In addition, we present the characterization method and the stress conditions.

In Chapter 3, the results of basic electrical characteristics and the static and dynamic NBTI characteristics of the devices are presented. Effects of PE-SiN capping on the NBTI are also discussed.

Finally important conclusions derived from our experimental results are summarized in Chapter 4. Some recommendations and suggestions for future work are also given.

Chapter 2

Device Fabrication and Measurement Setup

2.1 Process Flow

The PMOSFETs were fabricated on 6-inch n-type (100) Si wafers with resistivity of 2~7 Ω -cm. Standard local oxidation of silicon (LOCOS) process was used for devices isolation. Threshold voltage adjustment and anti-punch through implantation were done by implanting 80 KeV As⁺ and 120 KeV P⁺, respectively. After the growth of 3 nm-thick thermal gate oxide, a 150 nm undoped amorphous-SiGe layer was deposited by low-pressure chemical vapor deposition (LPCVD), using SiH₄ and GeH₄ as precursors at 450°C to serve as the gate, followed by gate etch process to pattern the film. Next, shallow source/drain (S/D) extensions were formed by implanting BF₂⁺ at 10 keV with a dose of 1 \times 10¹⁵cm⁻². After the formation of a TEOS sidewall spacer (50-nm), deep S/D junctions were formed by implanting B⁺ at 15 keV and a dose of 5 \times 10¹⁵cm⁻². Wafers were then annealed by rapid thermal anneal (RTA) in a nitrogen ambient at 900°C for 30 sec to activate dopants in the gate, S/D, and substrate regions. Afterwards, two types of samples were fabricated with TEOS layer or SiN/TEOS passivation layer deposited on top of the transistors by plasma-enhanced CVD (PECVD). After contact hole etching, normal metallization scheme was carried out. The final step was a post metal anneal performed at 400°C for 30 min to passivate the dangling bonds and to

reduce interface state density in the gate oxide/Si interface. Cross-sectional view of the fabricated device was shown in Fig. 2.1. To investigate the effect of hydrogen species, two splits of samples annealed in either forming gas or N₂ ambient were fabricated. Major conditions of the PMOSFETs splits are shown in Table 2.1.

2.2 Measurement Setup

2.2.1 Electrical Characterization

Electrical characterizations were performed using an HP 4156 system. A precision impedance meter, HP4284, was used for C-V measurements. Temperature-regulated hot chucks were controlled at temperatures ranging from 25°C to 130°C.

Split C-V method was employed to determinate the hole mobility. The electric field and charge densities produced by the gate voltage is express as:

$$E_{eff} = \frac{Q_b + \eta Q_n}{K_s \epsilon_0} \quad (2-1)$$

$$Q_b = \int_{V_{fb}}^{V_g} C_{gb} dV'_g \quad (2-2)$$

$$Q_n = \int_{-\infty}^{V_g} C_{gc} dV'_g \quad (2-3)$$

where Q_b and Q_n are charge densities in depletion layer and inversion layer, respectively. The parameter $\eta = 1/3$ for hole mobility. The gate-to-substrate capacitance (C_{gb}) and gate-to-channel capacitance (C_{gc}) were measured using the configurations illustrated in Fig.

2.2.

The existence of a gate leakage current may affect the accuracy in measuring the drain conductance. To solve this problem, we propose some new approaches as followed. The channel current is simply given by the average of the source and the drain currents. For surface carrier concentration evaluation, we have adopted a simple approach that takes drain voltage effect into account [21].

$$\mu(V_g) = \frac{L}{W} \cdot \frac{I_s(V_g) + I_d(V_g)}{2V_d} \cdot \frac{1}{qN_s(V_g)} \quad (2-4)$$

$$N_s(V_g) = \frac{(N_s^{source}(V_g) + N_s^{drain}(V_g))}{2} = \frac{1}{2q} \left(\int_{-\infty}^{V_g} C_{gc}(V'_g) dV'_g + \int_{-\infty}^{V_g - V_d} C_{gc}(V'_g) dV'_g \right) \quad (2-5)$$

2.2.2 Charge Pumping Measurement

It is well known that the charge pumping measurement is used to quantify the interface state density by monitoring the substrate current. The basic charge pumping measurement involves the measurement of the substrate current while a series of voltage pulses with fixed amplitude, rise time, fall time, frequency, and duty cycle is being applied to the gate of the transistor, with source and drain connected to a reverse bias.

In the characterization, square-wave ($f = 1\text{MHz}$) voltage signals were applied to the gate with a constant pulse amplitude of 1.5 V, and a varying base voltage to tune the surface condition from inversion to accumulation. Fig. 2.3 shows the configuration of measurement setup used in the charge pumping experiment. A MOSFET with a gate area of A_G gives the

charge pumping current as:

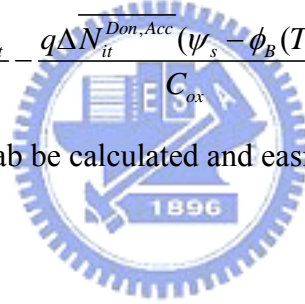
$$I_{cp} = qA_G f N_{it} \quad (2-5)$$

Interface trap density could be evaluated using the above equation.

Oxide traps cannot respond to the I_{cp} signal at high frequency and are categorized as slow traps. The mean interface trapped charge contributes only by ϕ_B as surface potential is roughly equal to $2\phi_B$. A simple and direct way to deduce oxide trap density (N_{ot}) is to calculate the difference between the measured V_{th} and the term contributed by N_{it} from charge pumping results, using the following formula:

$$\Delta V_{th}(T) = -\frac{q\Delta N_{ot}}{C_{ox}} - \frac{q\Delta N_{it}^{Don,Acc}(\psi_s - \phi_B(T))}{C_{ox}} \quad (2-6)$$

Therefore, ΔN_{ot} during stress can be calculated and easily determined.



2.3 Stress Measurement

2.3.1 Brief Review of NBTI

Negative-bias-temperature instability (NBTI) has been known to be a reliability concern since 1970s for p-channel metal-oxide silicon (MOS) field-effect transistors and complementary MOS (CMOS) inverter circuits [13,22]. This instability is seen as an increase with time of both interface-trap density and positive oxide-fixed-charge density during the operation of these devices. Recently, negative-bias-temperature instability has been identified as one of the major reliability concerns for deep sub-micron PMOSFETs [23,24].

For the aggressive scaling of CMOS technologies, an ultra thin gate oxide is essential to achieve high drive current under low power operation. The integrity and reliability of such a thin gate oxide are therefore crucial for ULSI manufacturing. NBTI manifests itself as absolute drain current I_{Dsat} , and transconductance (g_m), decrease as well as increase in the absolute “off” current I_{off} and absolute threshold voltage V_{th} .

It was observed that a large number of interface states and positive fixed charges were generated during negative-bias-temperature stressing (NBTS), resulting in a negative shift in threshold voltage showing a power-law dependence on stress time:

$$\Delta V_{th} = At^b \quad (2-7)$$

This phenomenon becomes more significant as gate oxide is scaled down, and may even become the limiting factor for deep sub-micron p-channel devices. The shift in threshold voltage and degradation in transconductance have been suggested to be due to the interfacial electrochemical reactions related to the holes from the channel inversion layer. The exponential value of the power law equation is around 0.25, which could be explained by the diffusion-controlled electrochemical reactions [12,25]. Based on the $t^{0.25}$ -like time evolution, a generalized reaction-diffusion model for interfacial charge formation based on the trivalent silicon and its hydrogen compounds has been proposed [11].

2.3.2 Diffusion-Limited Reaction Model

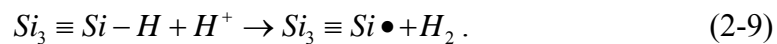
Diffusion-Limited reaction model was originally proposed by Svensson et al. [26]. In the

model, an interface trap is a trivalent silicon atom with an unsaturated valence electron (i.e., dangling bond) at the Si-SiO₂ interface. It is denoted by $Si \equiv Si \cdot$ and acts as an active interface trap. A post-metal-anneal in a forming gas (typically 5% H₂ in N₂ ambient) is widely used to passivate the interface dangling bonds, and introduces a lot of hydrogen-terminated trivalent Si bonds that are electrically inactive at the actual interface. If the terminated hydrogen is released from the $Si \equiv Si-H$ bond by some dissociation mechanism, the remaining interface trivalent silicon (i.e., dangling bond) is restored as an active interface trap. Various mechanisms have been proposed for the dissociation process.

High electric fields can dissociate the silicon-hydrogen bond, according to the model [13]



where H⁰ is a neutral interstitial hydrogen atom or atomic hydrogen. Recent first-principle calculations show that the positively charged hydrogen or proton H⁺ is the only stable charge state of hydrogen at the interface [27], and that H⁺ reacts directly with the SiH to form an interface trap, according to the reaction [26]:



The SiH is polarized in this model such that the mobile positive H⁺ migrates towards the negatively charged dipole region in the SiH molecule. The H⁺ atom then reacts with the H⁻ to form H₂, leaving behind a positively charged Si dangling bond.

A different model considers the interaction of SiH with “hot holes” or holes near or at the Si/SiO₂ interface [11]. Dissociation involving holes is given by

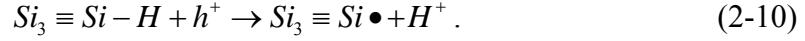
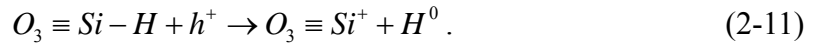


Fig. 2.4 is a schematic illustration of reaction-diffusion model for N_{it} generation.

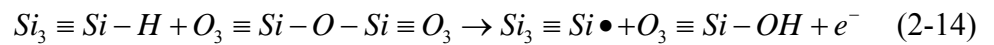
The fixed charge (Q_f) also contributes to threshold voltage shift near the SiO₂/Si interface. Q_f is a by-product of trivalent Si defect in the oxide, generated with the reaction



And the general electrochemical reaction can be express as follow:



In the reaction in (2-12), byproduct “X” is a “neutral species”, and in (2-12) and (2-13), Y and Z are unknown species depending on the nature of diffusing species X. As a result, the Svensson’s model is expressed as:



As discussed in Ref. 11, the interface trap density (N_{it}) and fixed oxide charge density (N_f) are shown to increase as:

$$\Delta N_{it} = CE_{ox}^{1.5} t^{0.25} \exp(-E_a / kT) / T_{ox} ; \quad (2-15)$$

$$\Delta N_f = C' E_{ox}^{1.5} t^{0.14} \exp(-E_a' / kT) , \quad (2-16)$$

where C and C’ are appropriate constant values, E_{ox} is the electric field in the oxide, T_{ox} is the

oxide thickness and t is the aging time. Ogawa et al. [11] found that the generation of fixed oxide charges is independent of oxide thickness, but is inversely proportional to oxide thickness for interface trap generation. This suggests that NBTI is worse for thinner oxide, but this phenomenon is not always observed and highly dependent on the process conditions.

The stable interface traps are only formed if by-product species, X , diffuses away from the interface into the oxide bulk.



where “ X ” could be H-related species.

As proved by Jeppson and Svensson [12], the observed $t^{0.25}$ behavior of the interface trap generation suggests the generation process is diffusion-controlled. N_{it} buildup equals the total number of released H species. Hole-assisted reaction breaks interfacial SiH bonds, resulting in Nit generation:

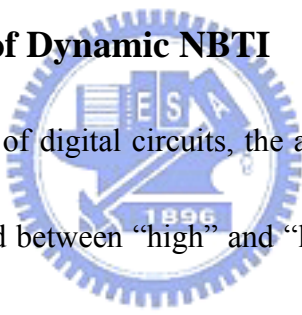
$$\Delta N_{it} = S_N (D_X t)^n, \quad (2-18)$$

where D_X is the diffusion coefficient of X in the oxide, time exponent n depends on the type of H species trapped and released in the oxide bulk [28].

The model that has often been invoked to explain the $t^{0.25}$ dependence of the trap generation rates is only partially correct [11]. In fact, there may exist six regimes of the reaction-diffusion model for Nit generation [29] as shown in Fig. 2.5. During the early stress stage, the generation of interface states and hydrogen species is limited by the dissociation

rate (Regime 1, $N_{it} \sim t^1$). Then, the process enters the quasi-equilibrium regime (Regime 2, $N_{it} \sim t^0$) immediately. After some stress time, the transport of hydrogen species limits the dissociation process (Regime 3, $N_{it} \sim t^{0.25}$). However, the reaction-controlled regime could directly merge into the diffusion-controlled regime. The rate of N_{it} changes after H diffusion front reaches the SiO_2/poly interface. Either H absorption into poly ensures faster H removal and higher rate of N_{it} (Regime 4) or H reflection from poly would result in N_{it} saturation (Regime 5). Finally, N_{it} should eventually saturate when all SiH bonds are broken (Regime 6).

2.3.3 Brief Review of Dynamic NBTI



During normal operations of digital circuits, the applied bias to the gate of PMOSFETs in a CMOS inverter is switched between “high” and “low” voltages. During the “low” phase of PMOSFET bias, the “electric passivation” effect may effectively reduce the interface traps generated during the “high” phase. The dynamic NBTI (DNBTI) effect greatly prolongs the lifetime of PMOSFETs operating in a digital circuit, while the conventional static NBTI measurement underestimates the PMOSFETs lifetime [30,31]. Furthermore, the DNBTI effect is dependent on temperature and gate oxide thickness [32]. A physical model is proposed for DNBTI that involves the interaction between hydrogen and silicon dangling bonds [33]. According to this reaction-diffusion theory, the ΔV_{th} is attributed to the creation of interface traps as a consequence of dissociation of Si-H bonds, and subsequent diffusion of the released

hydrogen species towards the gate electrode. In the recovery process, released hydrogen re-passivates Si dangling bonds [33]. The ΔV_{th} recovery progresses in accordance with the power law dependency as follows:

$$\Delta V_{th} = A - B \cdot t^n, \quad (4-10)$$

where B/A ratio indicates the ratio of a recovery reaction coefficient to ΔV_{th} just after NBT stress. This finding has significant impact on the determination of maximum operation voltage as well as lifetime for future scaling of CMOS devices. Therefore, it is critically important to investigate NBTI under such dynamic stress conditions.

2.3.4 Stress Measurement Setup

Static NBTI stressing and AC stressing were performed using an HP 4156 system. DNBTI stressing tests were performed using a Keithley 4200 system. The fabricated devices were subjected to bias-temperature-stress (BTS) varying from 70°C to 130°C. During the BTS, a negative gate bias (-3.2 V~ -3.8 V) was applied, while drain/source

Chapter 3

Experimental Results and Discussion

3.1 Basic Electrical Properties of Poly-SiGe-Gated Devices

Figure 3.1 shows the cumulative probability distribution of sheet resistance for poly-Si and poly-SiGe (Ge: 20%) gates with nominally identical implant and annealing conditions. As can be seen in the figure, the sheet resistance becomes lower with the incorporation of Ge, owing to the higher dopant activation [16]. Figure 3.2 compares the C-V characteristics of the devices. This further confirms the fact that poly-SiGe gate could effectively suppress the poly-depletion effect. Figure 3.3 shows the mobility as a function of effective vertical electric field. PMOSFETs with poly-SiGe gate show comparable hole mobility over their conventional poly-gated counterparts with nominally identical channel doping profile. However, lowering in channel doping to compensate for V_{th} shift due to work-function difference in poly-SiGe-gated devices may result in improved low-field mobility. Figure 3.4 (a) shows the I_d - V_g characteristics and transconductance (G_m), respectively. The G_m of poly-SiGe-gated devices is higher than that of their poly-Si-gated counterparts. This results in improved output characteristics for devices with poly-SiGe gate, as shown in Fig. 3.4 (b). As can be seen in Fig. 3.5, the poly-Si-gated devices depict higher $|V_{th}|$ than poly-SiGe-gated devices. This seems to be inconsistent with the results reported in the literature [34,35]. To

clarify the issue, we have double-checked the experimental procedure, and used the CVC (CVC is a fitting software which can used to fit capacitance versus voltage curve. By using the fitting of CV curve, the software would show us the flat band voltage, substrate dopant concentration, and we can calculate the threshold voltage.) fitting to find the substrate doping. Figures 3.6 (a) and (b) show the measured C-V characteristics together with the CVC fitting curve. As can be seen in these figures, the fitting curves match perfectly with the measured data except for the inversion region. The p-channel MOSFET threshold voltage is given by

$$V_{th} = V_{fb} - 2\phi_f - |Q_B| / C_{ox}, \quad (3-1)$$

where $\phi_f = (kT/q) \ln(N_D/n_i)$, $|Q_B| = (4qK_s \epsilon_o \phi_f N_D)^{1/2}$ and C_{ox} is the oxide capacitance per unit area. In Table 3.1, the $|V_{th}|$ calculated using the fitting approach and the measured data are both larger for poly-Si-gated devices. From the fitting results we found that the substrate doping concentration of two splits is different. This is one of the factors that account for the threshold voltage difference. In Table 3.2, we calculate and compare the threshold voltage values, both with a substrate doping concentration of $2.538 \times 10^{18} \text{ cm}^{-3}$. The results indicate that the poly-SiGe gated device now has a larger V_{th} . Clearly, the higher substrate doping concentration in the poly-Si-gated devices is the root cause of the higher $|V_{th}|$ over poly-SiGe-gated devices.

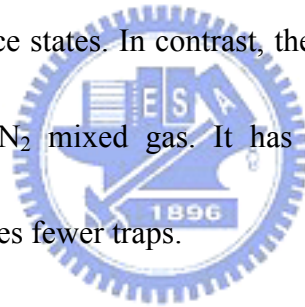
3.2 Basic Electrical Properties of Devices

In order to investigate the effect of hydrogen species, we studied 4 splits of devices with different hydrogen contents listed in Table 2.1 (denoted as Sample #A ~ Sample #E). Figures 3.7 (a) and (b) show the I_d - V_g characteristics of different splits of devices. It can be seen that all splits depict indistinguishable subthreshold characteristics. However, in Fig. 3.8 (a), the transconductance (G_m) of Sample #B is slightly larger than that of Sample #C. Interestingly, the G_m of Sample #D is almost the identical to that of Sample #B. Apparently the extra hydrogen species from SiN deposition does not significantly enhance device performance.

Although it was found that the stress of the nitride film deposited by PECVD is compressive in nature [36], the SiN thickness in the fabricated devices is too thin to provide sufficient stress to induce channel strain. Hence, no drive current enhancement is observed in this work.

In Fig. 3.8 (b), the G_m of two samples exhibits similar trends due to the use the forming gas anneal that would passivate the interface traps. Figures 3.9 (a) and (b) show output characteristics of devices with $0.5\mu\text{m}$ channel length. The saturation current measured at $V_D = -2\text{V}$ and $V_G - V_t = -2\text{V}$ is almost indistinguishable between Sample #B and Sample #D, while the saturation current of Sample #C is lower. The saturation current of Sample #E is also lower than that of Sample #D. We believe the forming gas anneal would effectively passivate interface traps which explains the larger saturation current detected in Sample #B over Sample #C and in Sample #D over Sample #E. Figures 3.10 (a) and (b) show the

capacitance-voltage (C-V) curves for all splits of samples. Again the capacitance is almost identical at $V_G = -2.5V$ for Samples #B and #C. Besides, Samples #D and #E also have indistinguishable capacitance measured at $V_G = -2.5V$. It can be seen that the annealing processes do not affect the capacitance. It is worth noting that a slight increase in inversion capacitance is observed in Sample #D, which can be explained by extra hydrogen species that could passivate interface traps at the oxide/Si interface. The above results suggest that SiN-capping can passivate interface states more effectively than forming gas anneal. Because the SiN capping was deposited by PECVD that produced hydrogen radicals, it is more effective in passivating interface states. In contrast, the forming gas anneal was performed in a furnace at $400^\circ C$ with H_2/N_2 mixed gas. It has insufficient energy for interface trap passivation, and it just passivates fewer traps.



Figures 3.11 (a) and (b) show V_{th} versus channel length for all splits of samples. Similar trends in V_{th} roll-off are observed. However, the V_{th} value is different among these four splits. The observed V_{th} difference could probably be ascribed to different amounts of incorporated hydrogen species among the splits. Sample #C has less hydrogen content, as compared with the control and SiN-capped splits. As shown in Fig. 3.11, the absolute value of V_{th} is indeed proportional to the hydrogen contents of the devices.

Figure 3.12 (a) shows charge pumping current (I_{cp}) of the fresh devices for all splits of samples at $25^\circ C$. It can be seen that I_{cp} is the smallest for Sample #D. In this work, the SiN

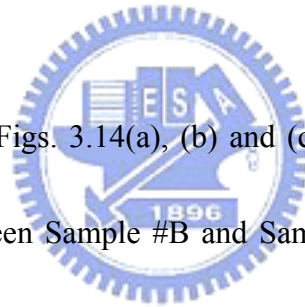
capping layer was deposited by PECVD, and a large amount of hydrogen species could be introduced during PECVD deposition with the use of SiH₄ and NH₃ as the precursors. As a result, a significant portion of interface states would be passivated [37]. By contrast, the N₂-anneal depicts a larger I_{cp} due to its smaller hydrogen contents for Sample #C over #B. In fact, Sample #D indeed contains the largest amount of hydrogen species among all splits. In Fig. 3.12 (b), samples #D and #E have similar charge pumping current. Because the hydrogen species which produced by nitride deposition are too much, the two different anneal will not influence the numbers of interface traps.

3.3 Static NBTI Characterization



Figures 3.13, 3.14 and 3.15 show the results of NBTI stress performed at 70°C with gate overdrive bias of -3.5V ($V_{GO} = V_G - V_{th}$). As can be seen in Fig. 3.14, Sample #A and Sample #B show similar ΔV_{th} and ΔN_{it} , but Sample #A shows worse $G_{m_{max}}$ degradation. It is worth noting that the curves depict a fractional power-law dependence on time ($\Delta V_{th} \propto t^n$). The exponent values of Sample #A in both ΔV_{th} and ΔN_{it} are larger than those of Sample #B. It is obvious that if the stress time is much longer than 5000 seconds Sample #A will depict larger ΔV_{th} and ΔN_{it} than Sample #B. Because the SiGe gate suppresses boron penetration [16,17], and there are less defects at SiO₂/Si interface, the SiGe shows better NBTI reliability. Figure 3.14 shows the NBTI characterization results for Samples #B, #D, and #E. It can be seen that

the threshold voltage shift, ΔV_{th} , is the largest for the devices with SiN capping (Sample #D), while the other two splits show similar but smaller ΔV_{th} . Similarly, ΔN_{it} and Gm degradation are also the worst for Sample #D. The smallest pre-stress I_{cp} (Fig. 3.12 (a)) can be explained by the fact that Si-H bonds are passivated by extra hydrogen species during SiN deposition, while the largest ΔN_{it} suggests that these bonds are being broken during the NBTI stress process. In addition, the passivation of interface states by extra hydrogen species from SiN layer is what is termed “virtual passivation”, i.e., it can be easily broken during later NBTI stress. The excess hydrogen species thus becomes the culprit for aggravated NBTI during NBTI stressing.



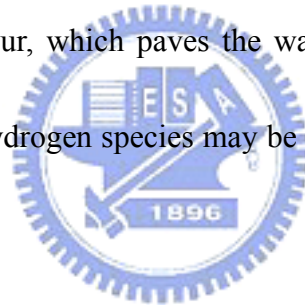
In contrast, as shown in Figs. 3.14(a), (b) and (c), ΔV_{th} , ΔN_{it} and Gm degradation are almost indistinguishable between Sample #B and Sample #C. Although forming gas anneal can supply hydrogen species for interface state passivation, the NBTI is apparently not degraded by forming gas anneal. Fig. 3.15 shows that Samples #D and #E have similar ΔV_{th} , ΔN_{it} and Gm degradation. We believe the effect of SiN capping would dominant the NBTI degradation over that of post metal anneal.

Figures 3.16, 3.17 and 3.18 show the results of NBTI stress performed at 130°C with gate overdrive bias of -3.8V. The trends are similar to those occurring at 70°C. The devices with SiN capping have aggravated NBTI behaviors.

The above results clearly indicate that the use of PECVD SiN capping may result in

degraded NBTI. One plausible origin is postulated to explain the worsen NBTI: higher density of Si-H bonds at the oxide/Si interface, since the SiN layer contains a large amount of hydrogen species because of the use of SiH₄ and NH₃ precursor gases. This is evidenced by the higher exponent value of the power-time dependence for devices with SiN capping.

The exponent value is different in ΔV_{th} and in ΔN_{it} for all splits of samples. This is consistent with the observation that the threshold voltage would be degraded by not only the increase of interface traps but also oxide charges. The second component to cause ΔV_{th} is related to trapped charges in the oxide [38,39]. Under NBTI stress conditions, an increase in oxide defects is known to occur, which paves the way for eventual oxide breakdown once critical limit is reached. The hydrogen species may be proton type (H⁺) that would be trapped in oxide during NBTI stress.



Figures 3.19 to 3.23 show ΔV_{th} and ΔN_{it} characteristics as a function of time under different V_{GO} at 130°C for all splits of samples. ΔV_{th} and ΔN_{it} in all cases increase with increasing voltage. Because $\Delta N_{it} \propto E_{ox}^{1.5}$, higher V_{GO} can induce larger amount of N_{it} and degradation.

3.4 DNBTI and AC stress

To simulate the switching operation of the device in the CMOS circuits, the gate voltage during NBTI stress is switched between negative and zero biases for all splits of samples, as

shown in Figures 3.24 and 3.25. The conditions during stress periods were $V_{GO}=-3.5V$ for 1000 seconds, and performed at $130^{\circ}C$, while in the passivation periods V_G was set at $0V$ for 1000 seconds. Other terminals were grounded during the measurements. Figure 3.24 shows the results for Samples #A, #B, and #C. It is seen that ΔV_{th} and ΔN_{it} have similar values and trends. Figure 3.25 shows that for Samples #D and #E, ΔV_{th} and ΔN_{it} are larger than other splits. The recovery is influenced by the passivation voltage V_G [40]. It may be due to the electron trapping related to the positive hydrogen charges in the gate dielectric according to reaction (2-17).

Furthermore, the frequency dependence of NBT degradation was measured and shown in Figs. 4.26 to 4.29 with 50% duty cycle. V_{th} and N_{it} are plotted as a function of frequency, as shown in Fig.3.30. Both V_{th} and N_{it} are strongly dependent on frequency for devices with SiN capping layer. The higher the AC frequency, the less V_{th} and N_{it} degradations. This is ascribed to the shortened stress time with increased frequency. It results in parts of broken SiH bonds being recovered before being driven into the next stress state. Interface trap generation would be reduced by increasing AC stress frequency and V_{th} is suppressed indirectly. Reduction in NBT degradation for Samples #D and #E under AC stress is more significant than that for Samples #B and #C, mainly because the amount of broken SiH bonds with SiN capping layer is larger for Samples #D & #E.

Chapter 4

Conclusions

4.1 Conclusions

Using SiGe as gate material of PMOSFETs has numerous advantages, including reduced gate depletion effect and improved gate sheet resistance. Both forming gas and SiN capping can effectively passivate interface states, and result in threshold voltage difference. Although SiN capping would greatly reduce interface state density and increase inversion capacitance, our results indicate that the SiN capping may simultaneously aggravate the NBTI characteristics. An abundant hydrogen species contained in the PE-SiN layer may be the culprit for the worsened reliability. However, forming gas anneal shows a different behavior. In particular, forming gas and N₂ anneals result in almost identical electrical characteristics and NBTI behaviors, albeit their fresh D_{it} is quite different. Unlike SiN capping, the NBTI characteristics of PMOSFETs receiving either forming gas or N₂ gas anneal are nearly identical.

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	Passivation layer	Post metal anneal	index
Poly-Si gate	TEOS 300nm	Forming gas anneal	A
SiGe gate	TEOS 300nm	Forming gas anneal	B
		N ₂ anneal	C
SiGe gate	SiN 40nm + TEOS 300nm	Forming gas anneal	D
		N ₂ anneal	E

Table 2.1 Split conditions.

	Poly-Si	SiGe
V_{fb} (CVC fit)	1.253 V	1.117 V
Substrate Dopant (CVC fit)	3.609e18 cm ⁻³	2.538e18 cm ⁻³
 Q_B /C_{ox}	1.082 V	0.902 V
V_{th} (Calculated)	-0.829 V	-0.766 V
V_{th} (Measurement)	-0.821 V	-0.774 V

Table 3.1 CVC fitting.

	Poly-Si	SiGe
V_{fb} (CVC fit)	1.253 V	1.117 V
Substrate Dopant (CVC fit)	2.538e18 cm ⁻³	2.538e18 cm ⁻³
 Q_B /C_{ox}	0.902 V	0.902 V
V_{th} (Calculated)	-0.630V	-0.766 V

Table 3.2 CVC fitting with the same substrate dopant concentration.

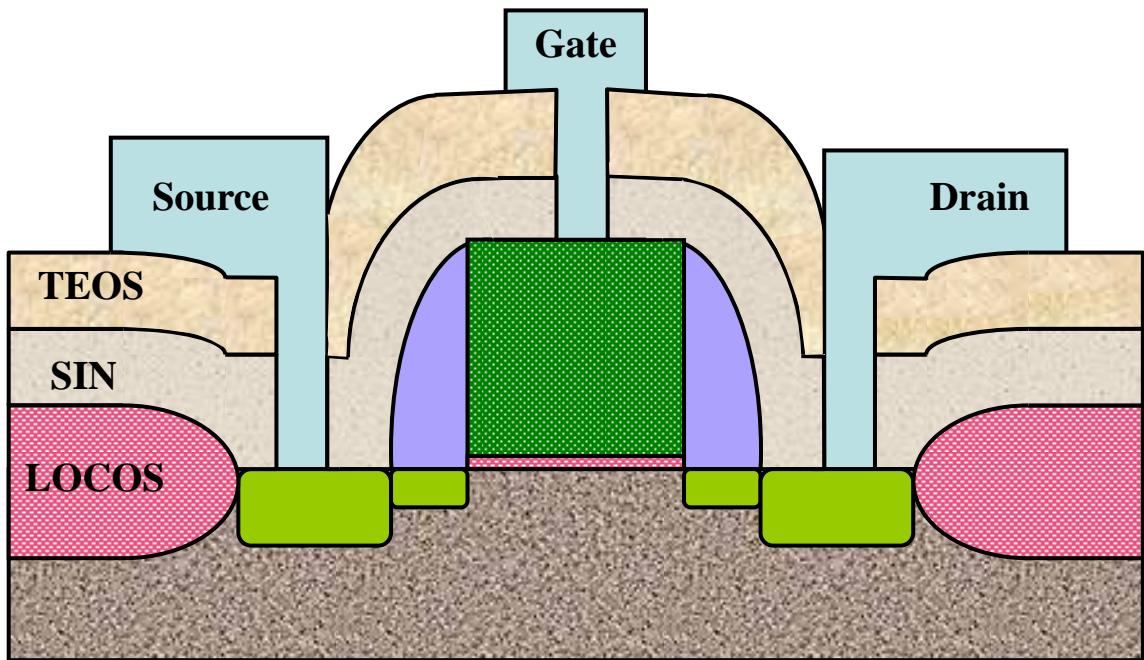


Fig. 2.1 Schematic cross section of the local strained channel PMOSFET.

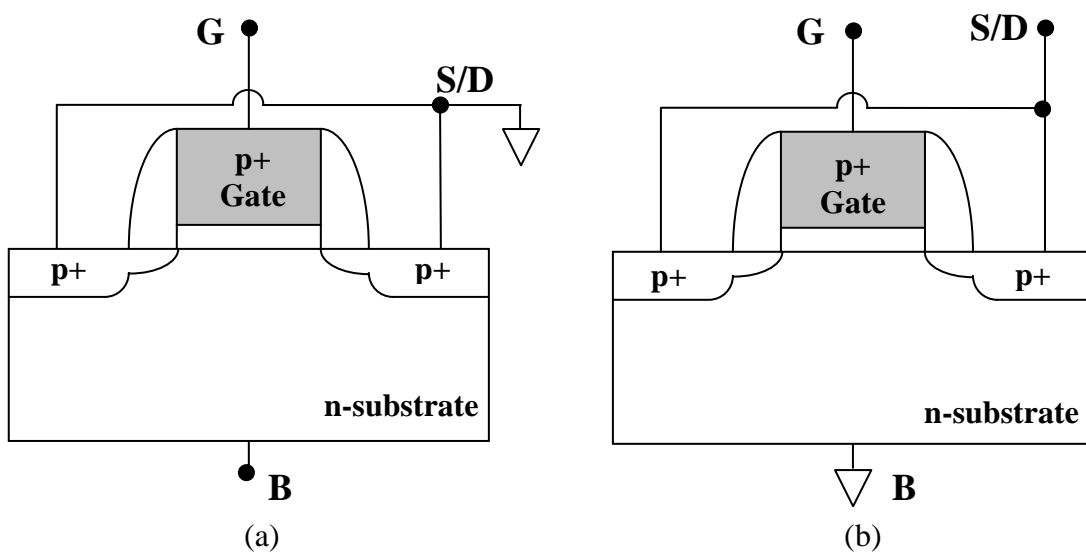


Fig. 2.2 Configuration for (a) gate-to-substrate, (b) gate-to-channel capacitance measurements.

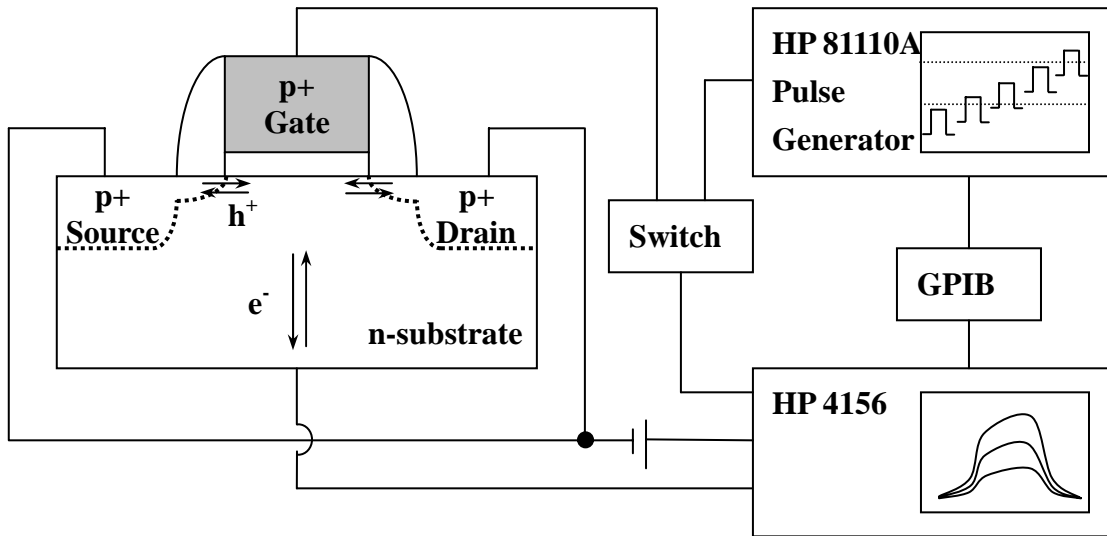


Fig. 2.3 Measurement setup in our charge pumping experiment.

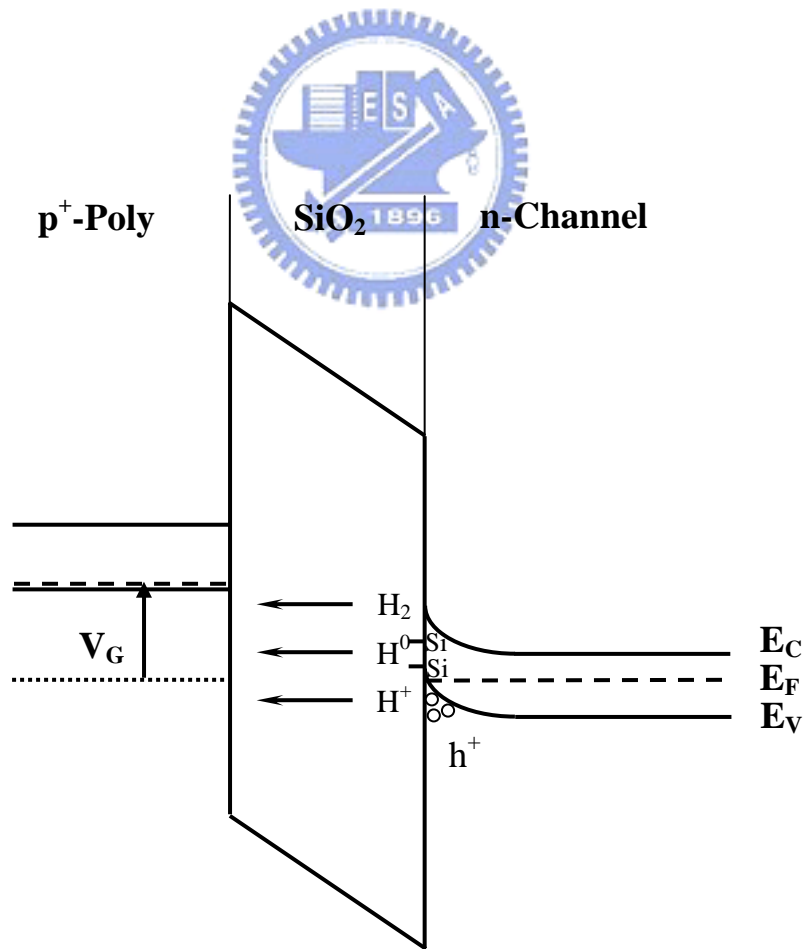


Fig. 2.4 Schematic view of the field-induced hydrogen species current through the gate oxide during negative bias aging.

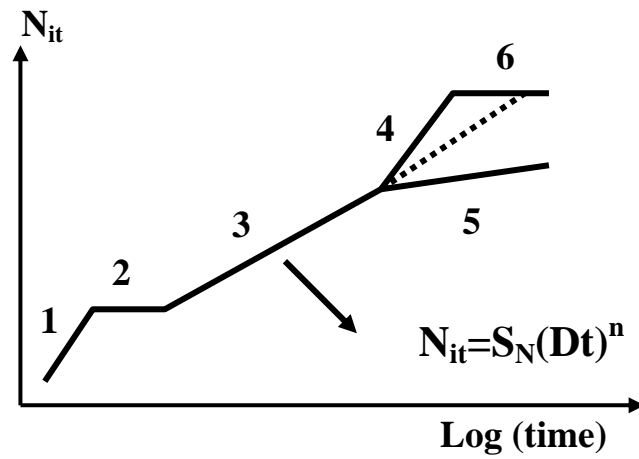


Fig.2.5 Various phases of N_{it} buildup. 1: reaction-limited, 2: quasi-equilibrium, 3: diffusion-limited, 4: enhancement due to poly absorption, 5: saturation due to poly reflection, 6: final saturation [29].

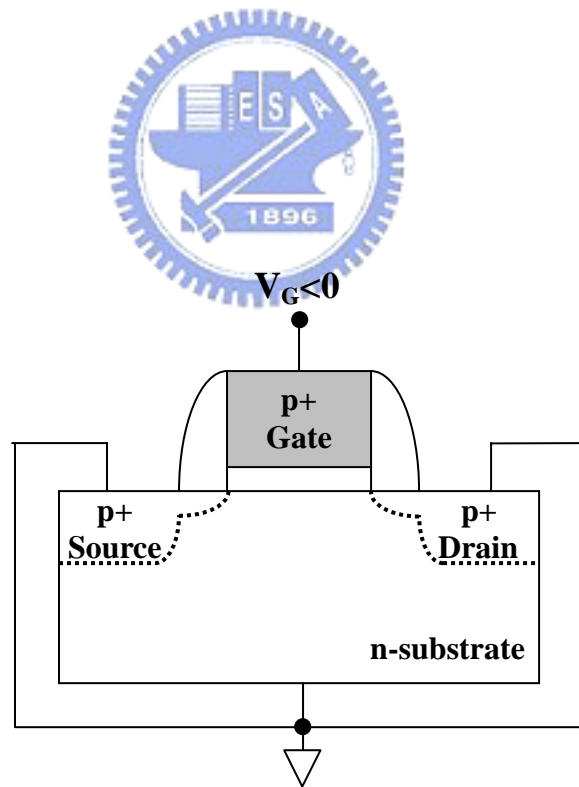


Fig. 2.6 Bias configuration of NBTI stressing.

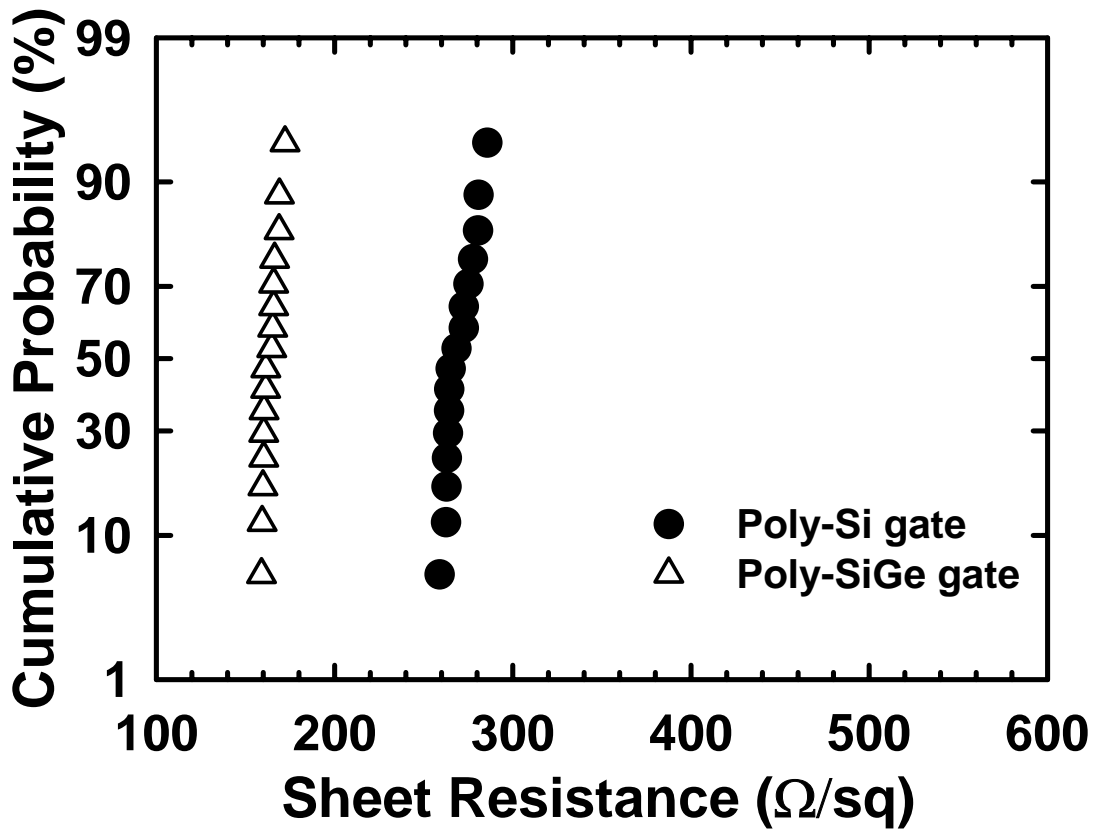


Fig. 3.1 Cumulative probability distribution of sheet resistance of poly-Si and α -SiGe films. Both with thickness of 150nm, implanted with B implant (dose $3e15cm^{-2}$, 8KeV) and annealed at 900°C 30sec.

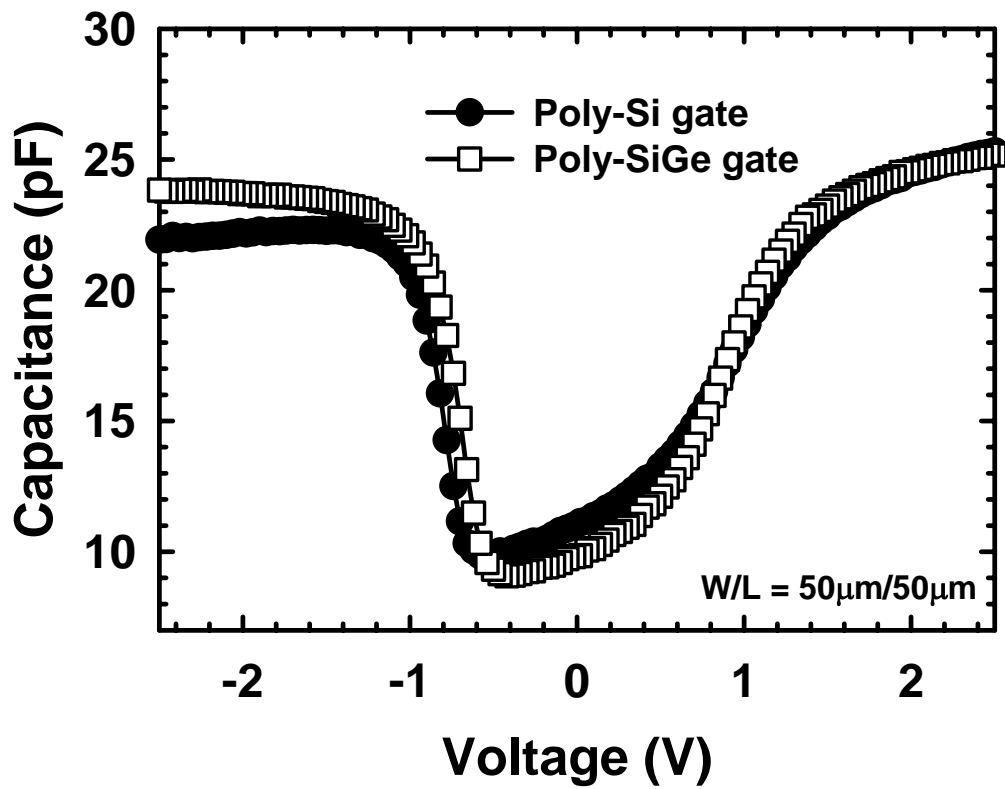


Fig. 3.2 Capacitance of devices with poly-Si and α -SiGe gates.

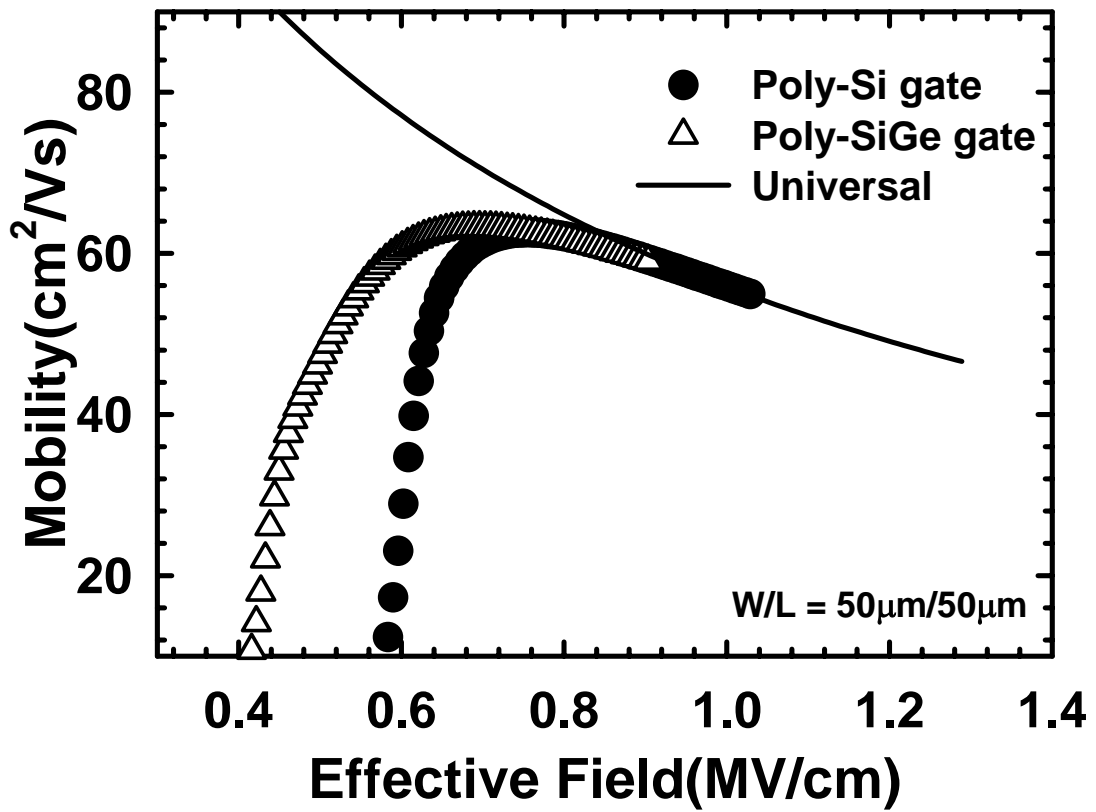
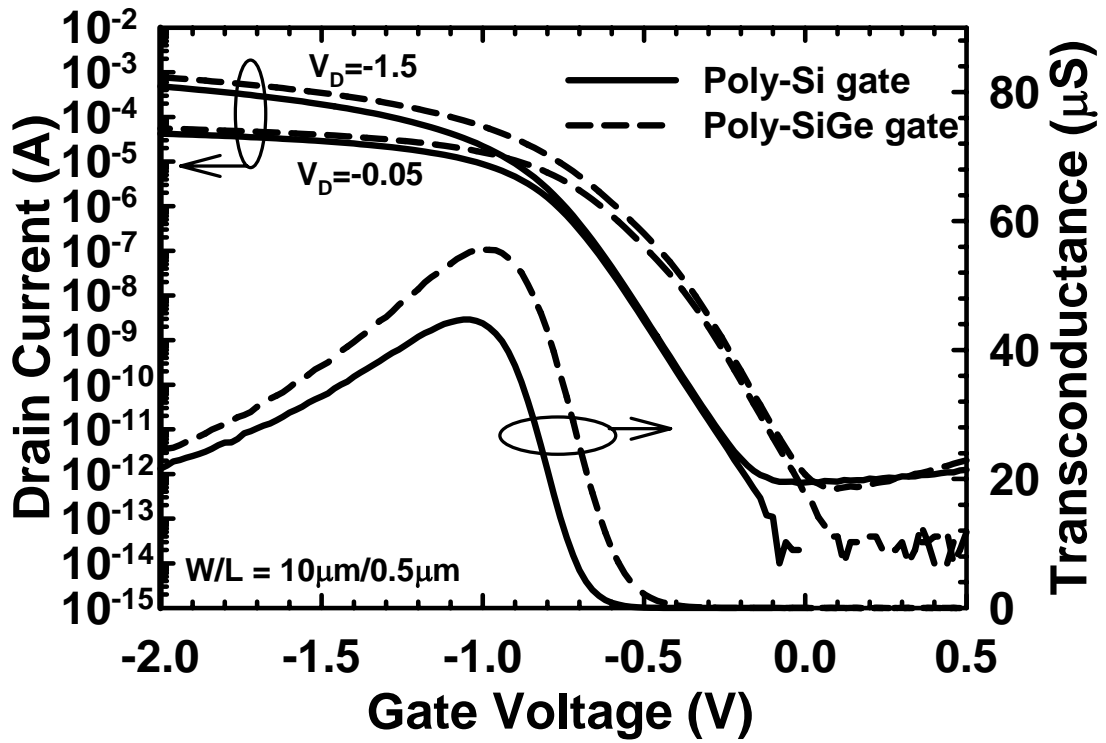
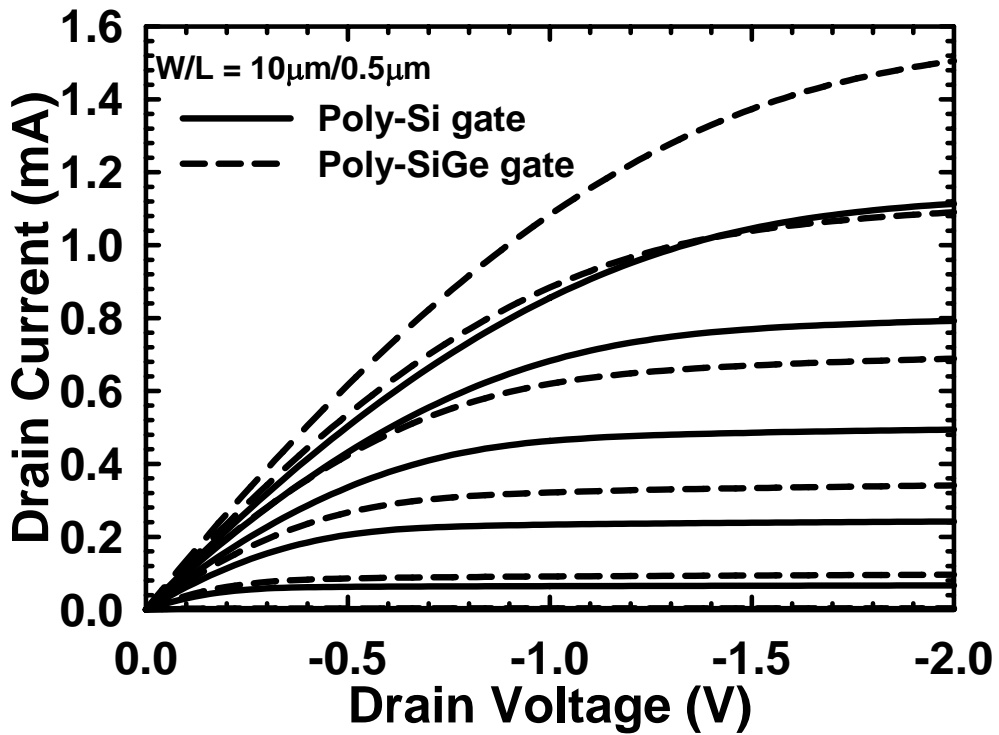


Fig. 3.3 Comparison of hole mobility among different gate materials measured by split-CV method.



(a)



(b)

Fig. 3.4 (a) I_D - V_G characteristics, and (b) output characteristics, $V_G - V_{th} = 0 \sim -2$ V, step = -0.4 V for poly-Si and α -SiGe gates.

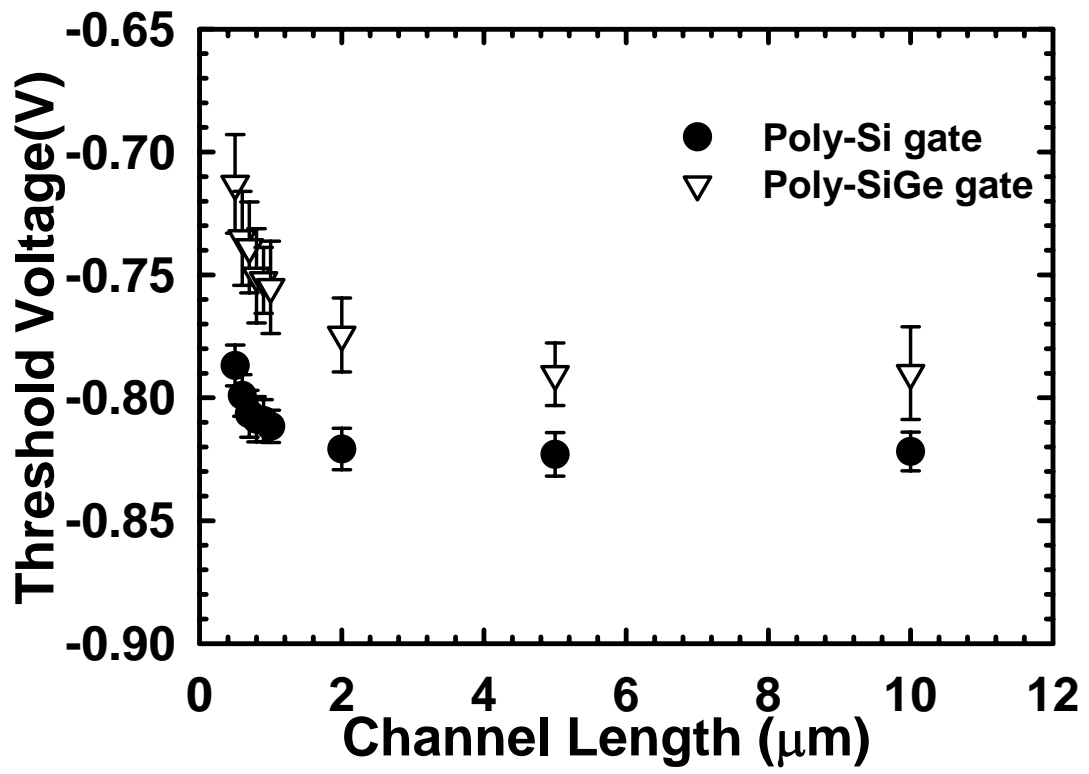
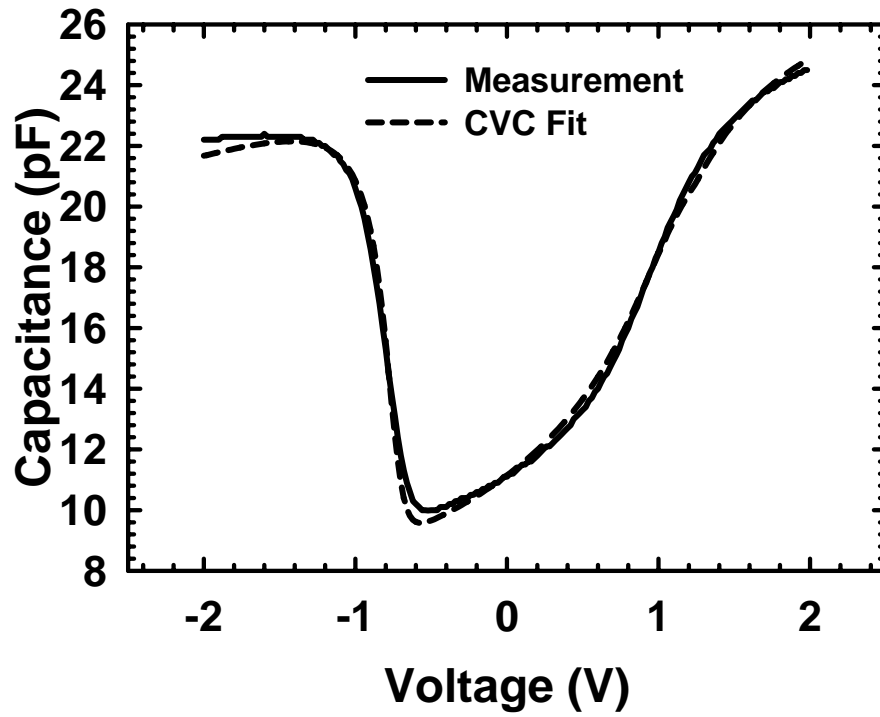
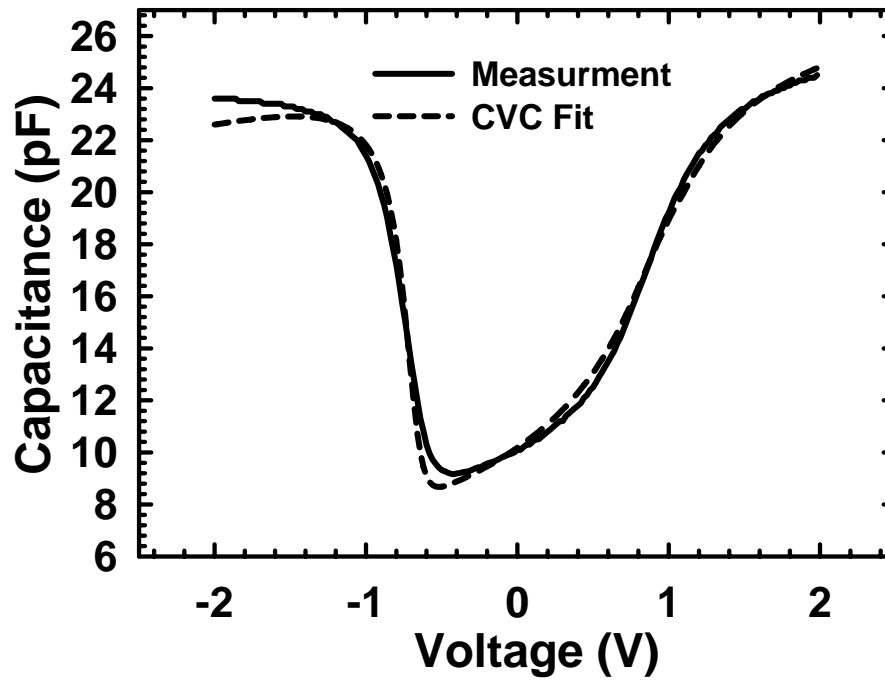


Fig. 3.5 Threshold voltage of devices with different gates as a function of channel length.

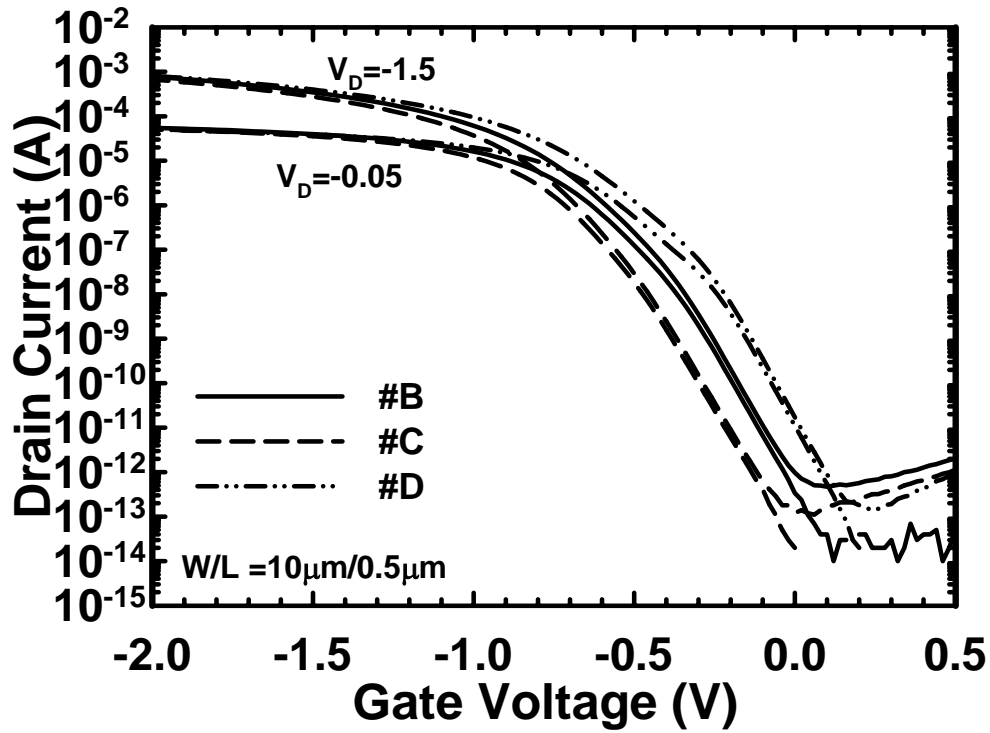


(a)

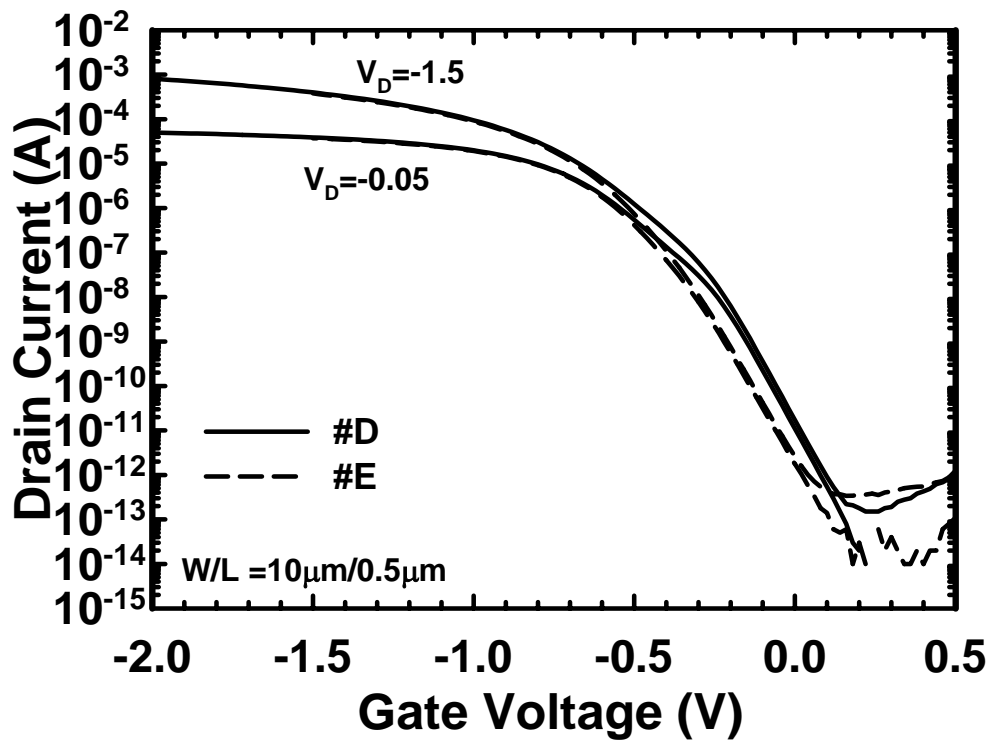


(b)

Fig. 3.6 Capacitance of devices with CVC fitted and measured with (a) poly-Si, and (b) α -SiGe gates. $L/W = 50\mu\text{m}/50\mu\text{m}$.

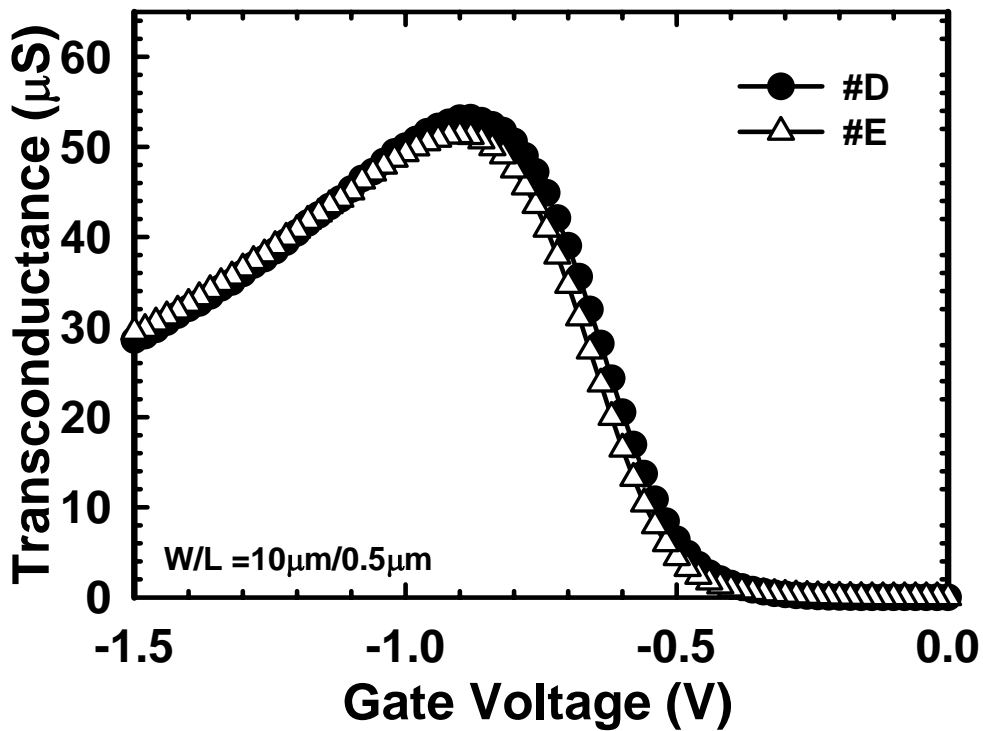
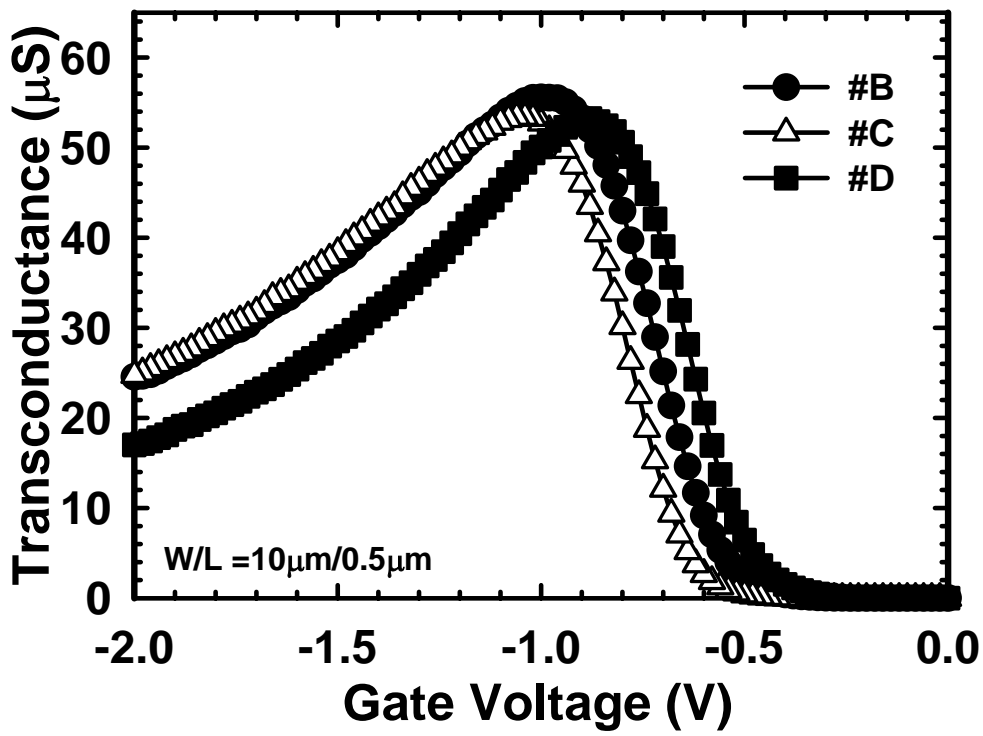


(a)



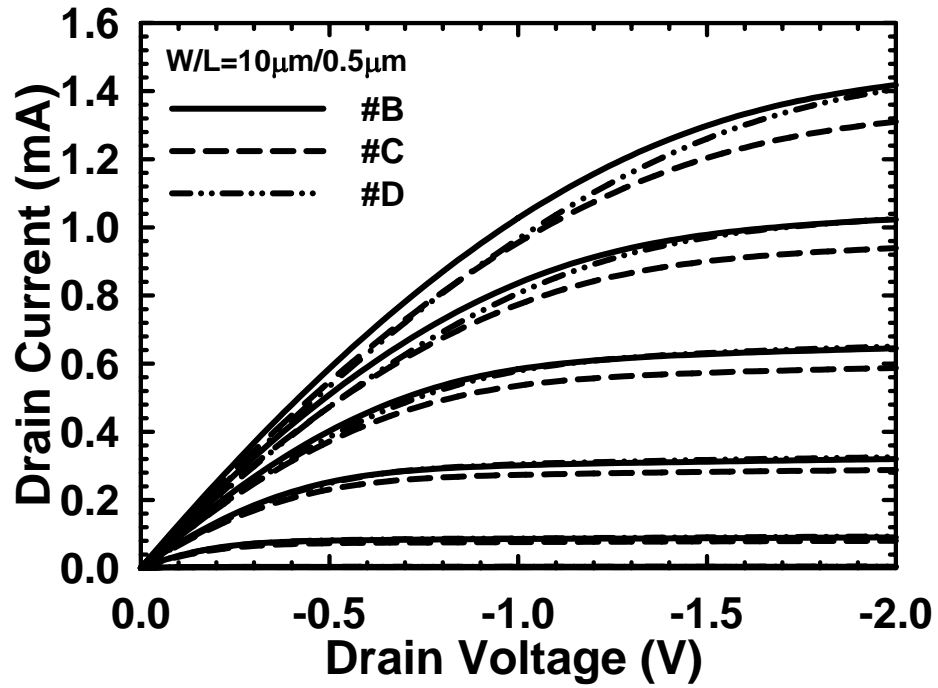
(b)

Fig. 3.7 I_D - V_G characteristics of devices with different split conditions for (a) #B, #C, and #D; (b) #D and #E.

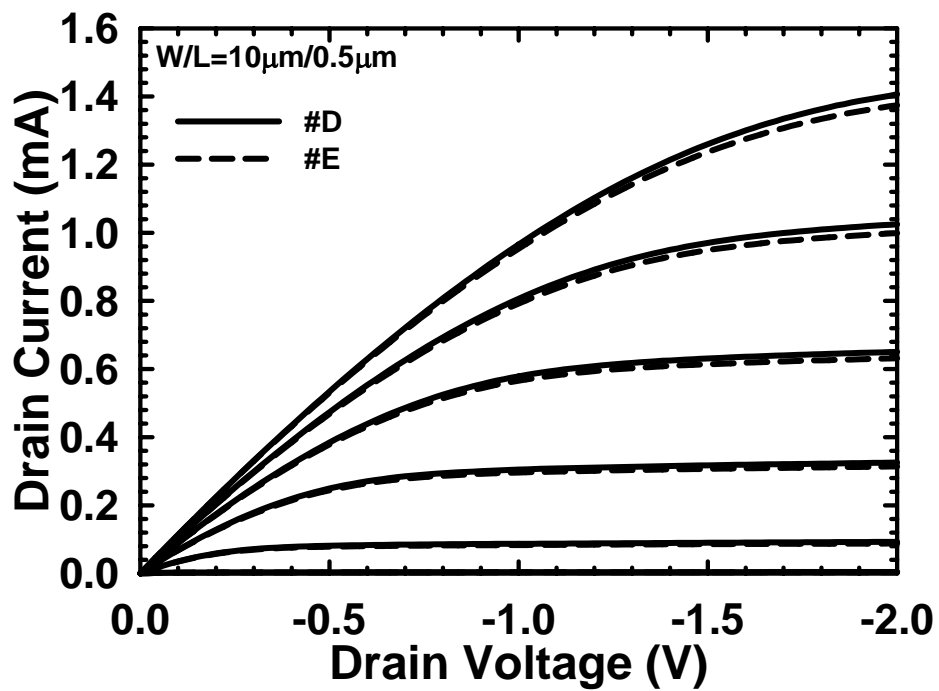


(b)

Fig. 3.8 Transconductance for devices with different split conditions for (a) #B, #C, and #D; (b) #D and #E.

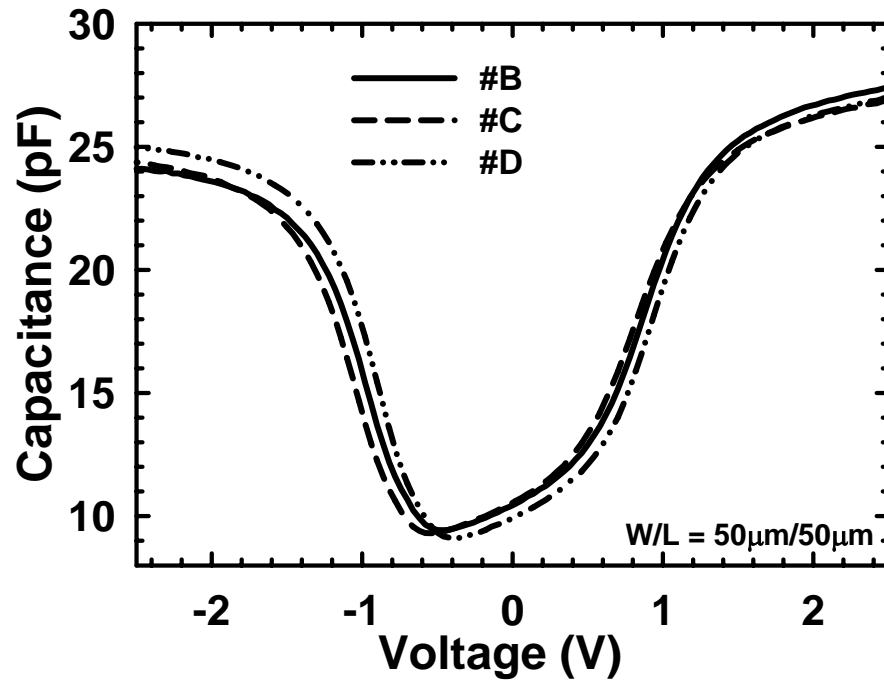


(a)

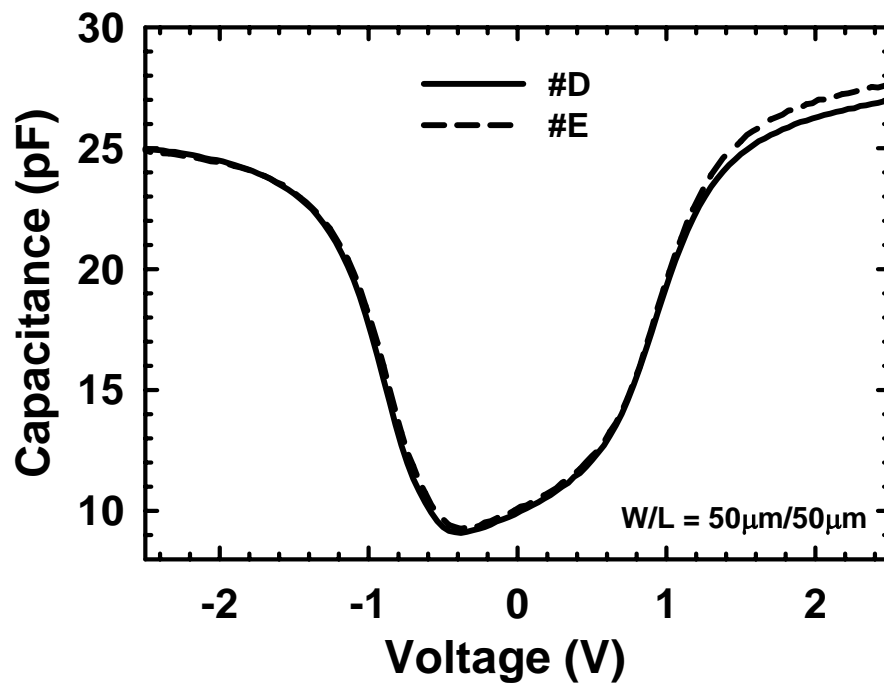


(b)

Fig. 3.9 Output characteristics for devices with different split conditions for (a) #B, #C, and #D; (b) #D and #E.

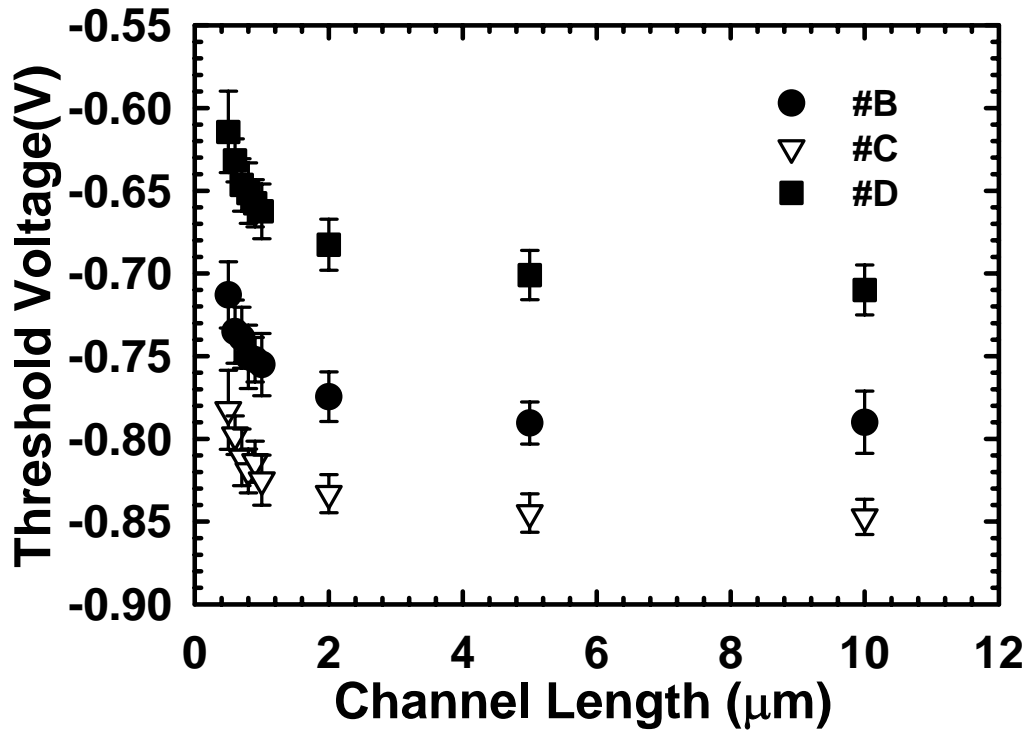


(a)

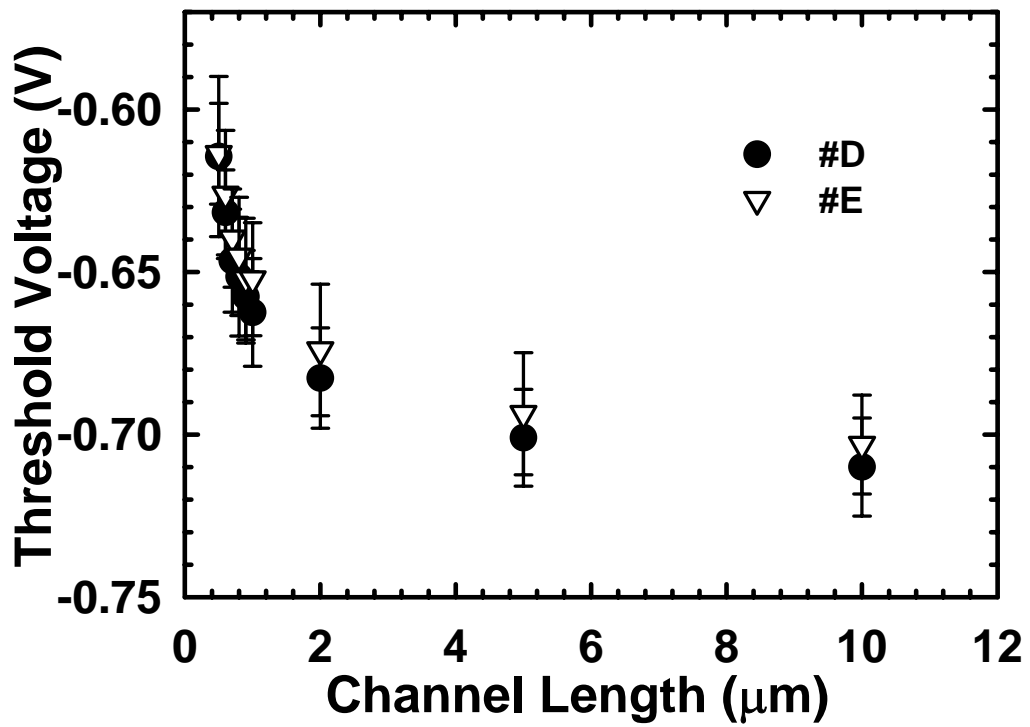


(b)

Fig. 3.10 Capacitance for devices with different split conditions for (a) #B, #C, and #D; (b) #D and #E.

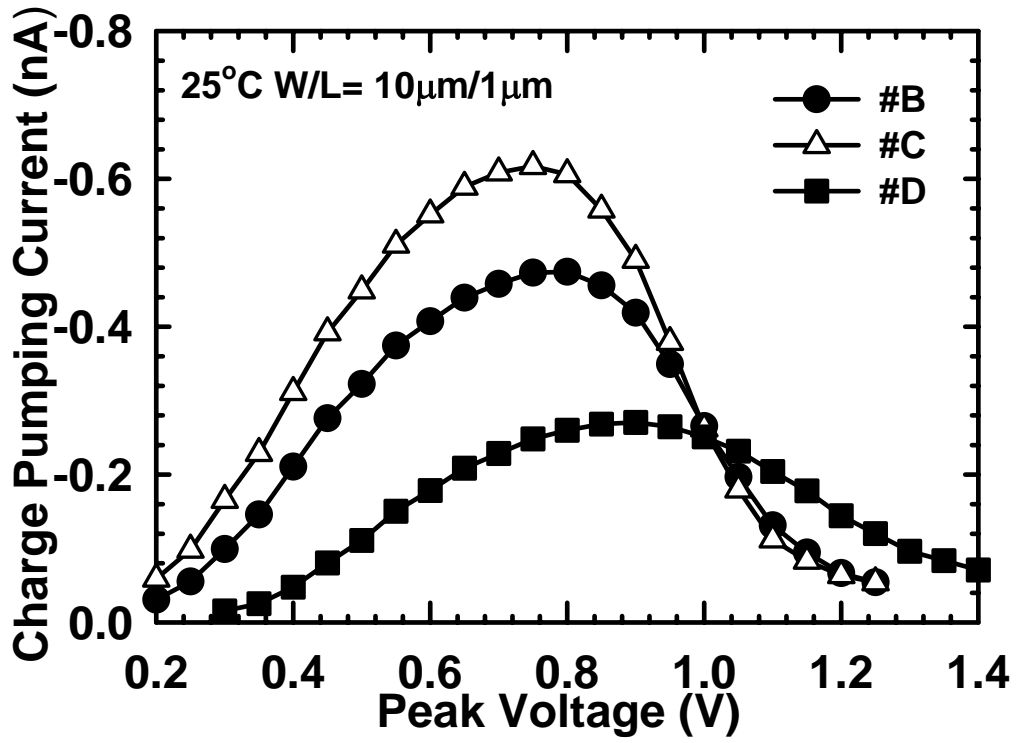


(a)

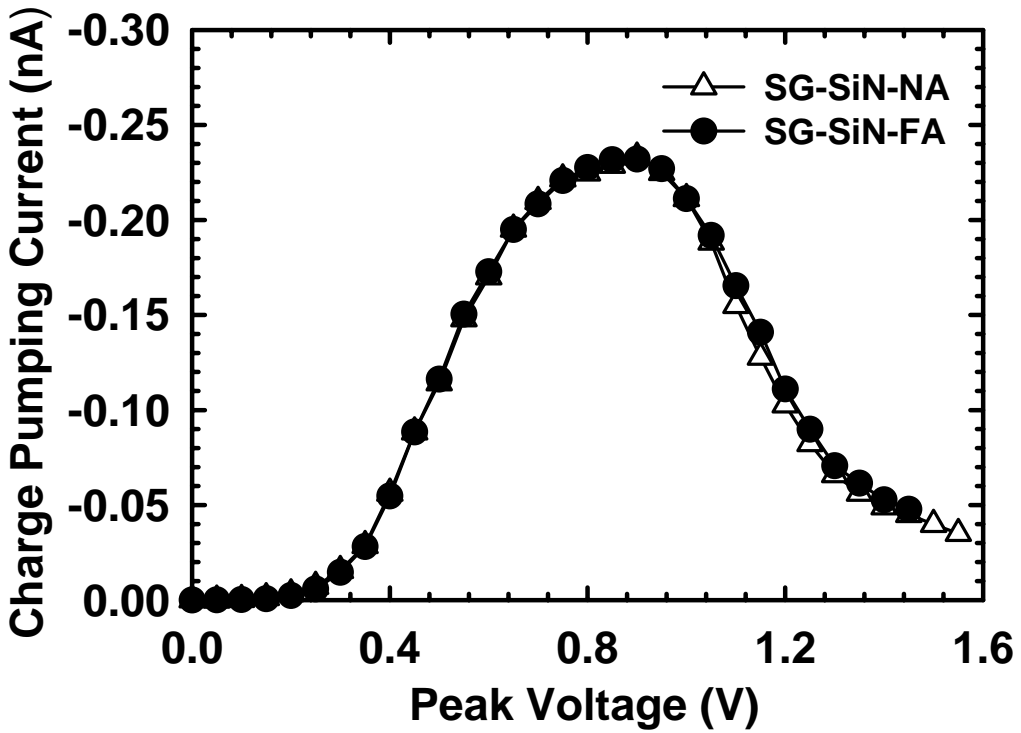


(b)

Fig. 3.11 Threshold voltage of devices with different splits as a function of channel length for (a) #B, #C, and #D; (b) #D and #E.

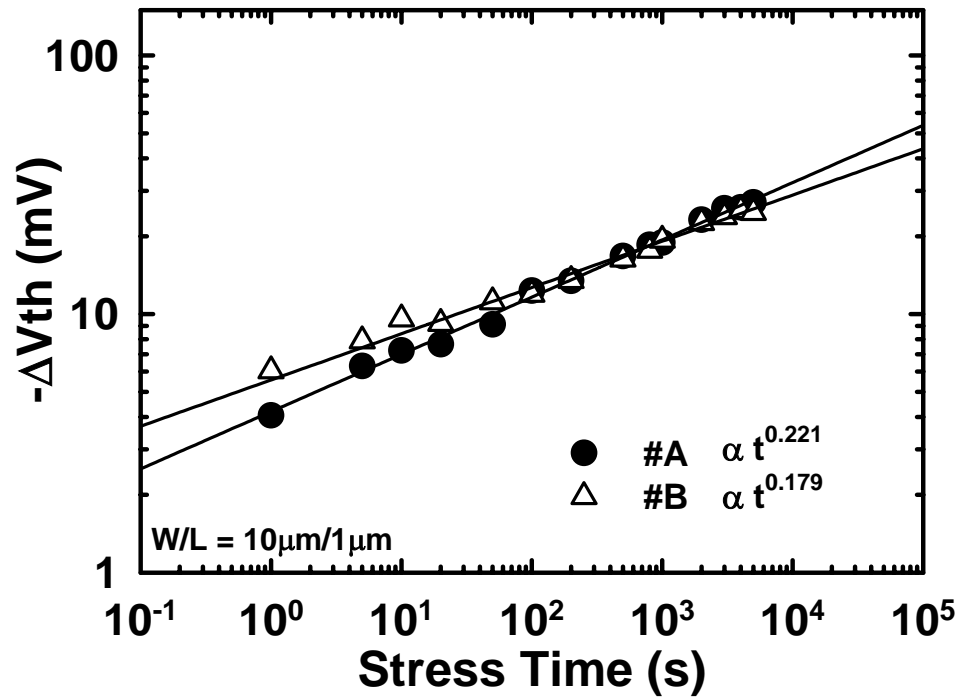


(a)

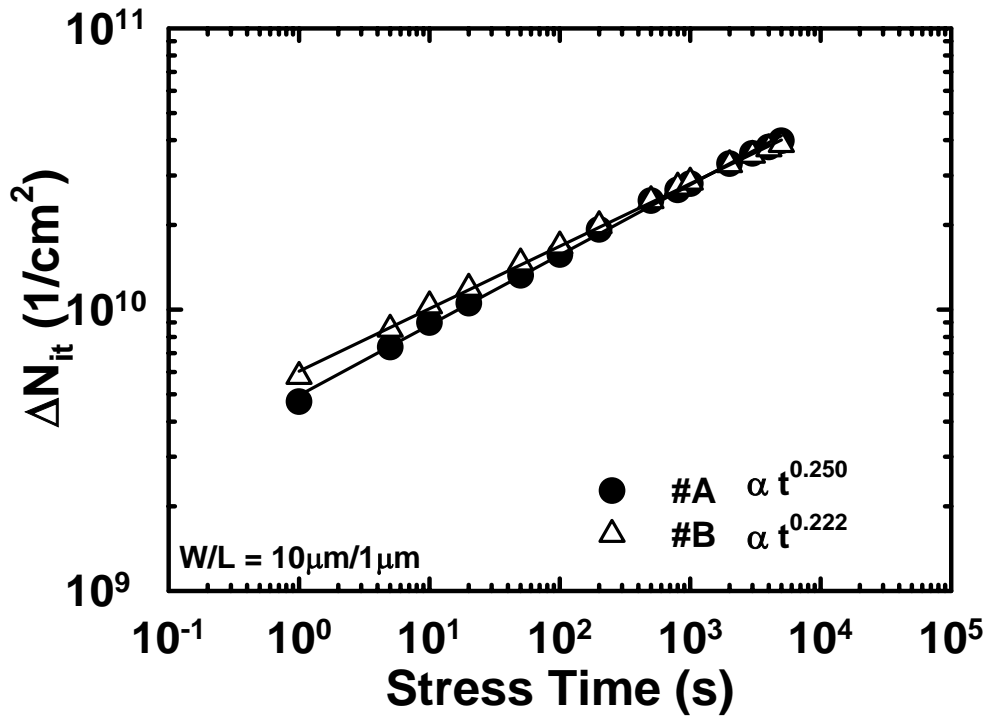


(b)

Fig. 3.12 Charge pumping currents for devices with different conditions, for (a) #B, #C, and #D; (b) #D and #E, pulse amplitude=1.5V, frequency=1MHz.

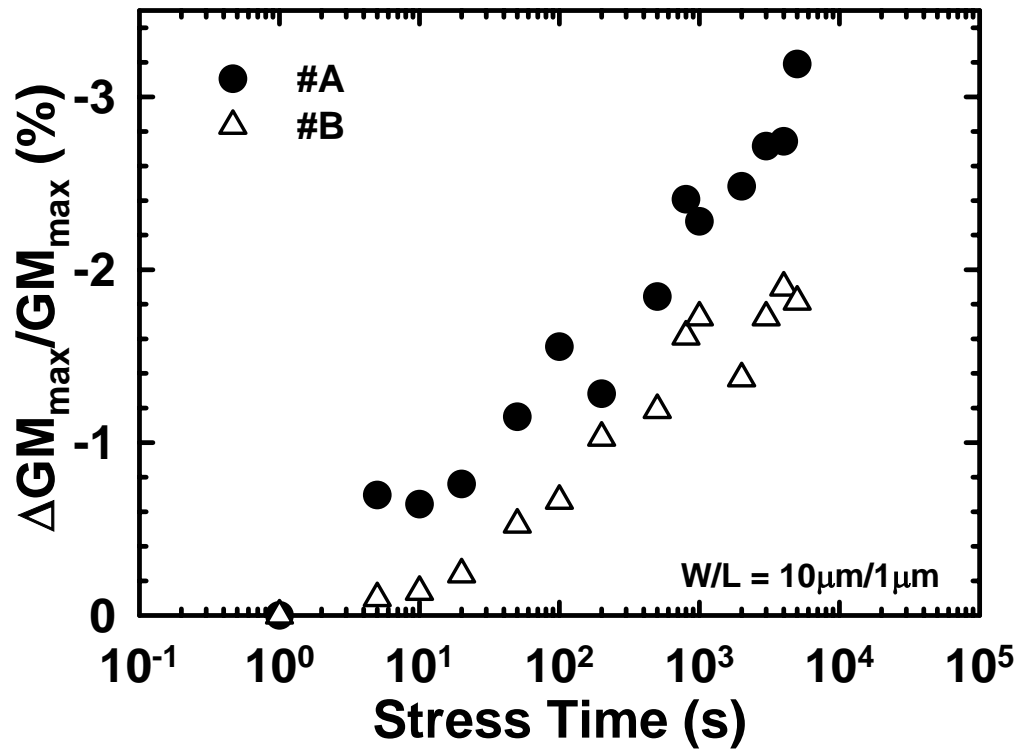


(a)



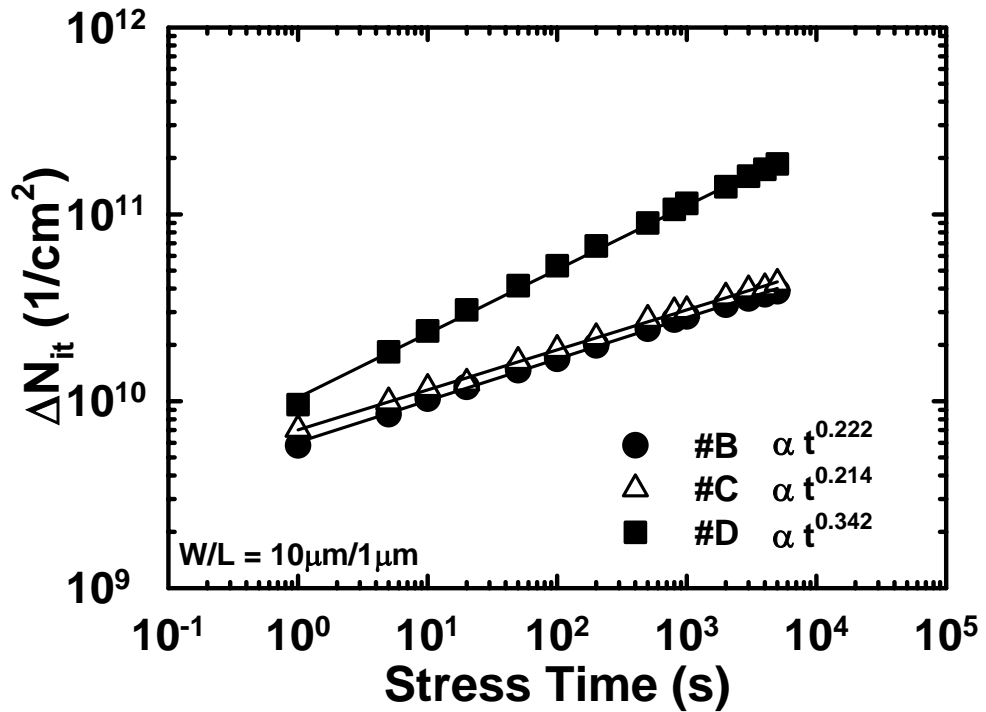
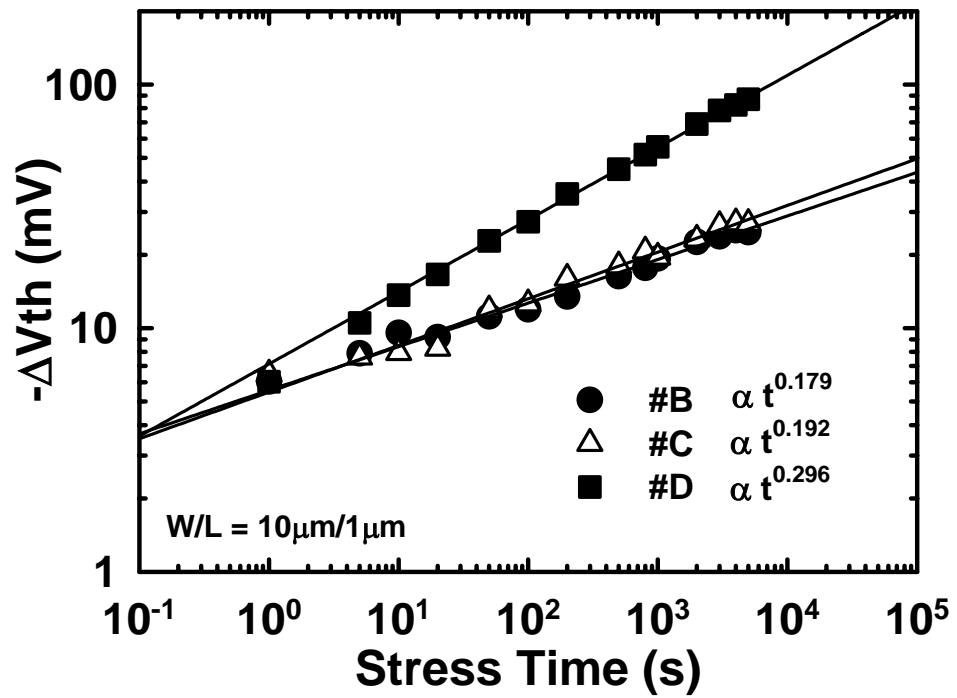
(b)

Fig. 3.13 (a) Threshold voltage shift, and (b) interface trap density increasing at 70°C during $V_{GO} = -3.5$ V stress aging for #A and #B.



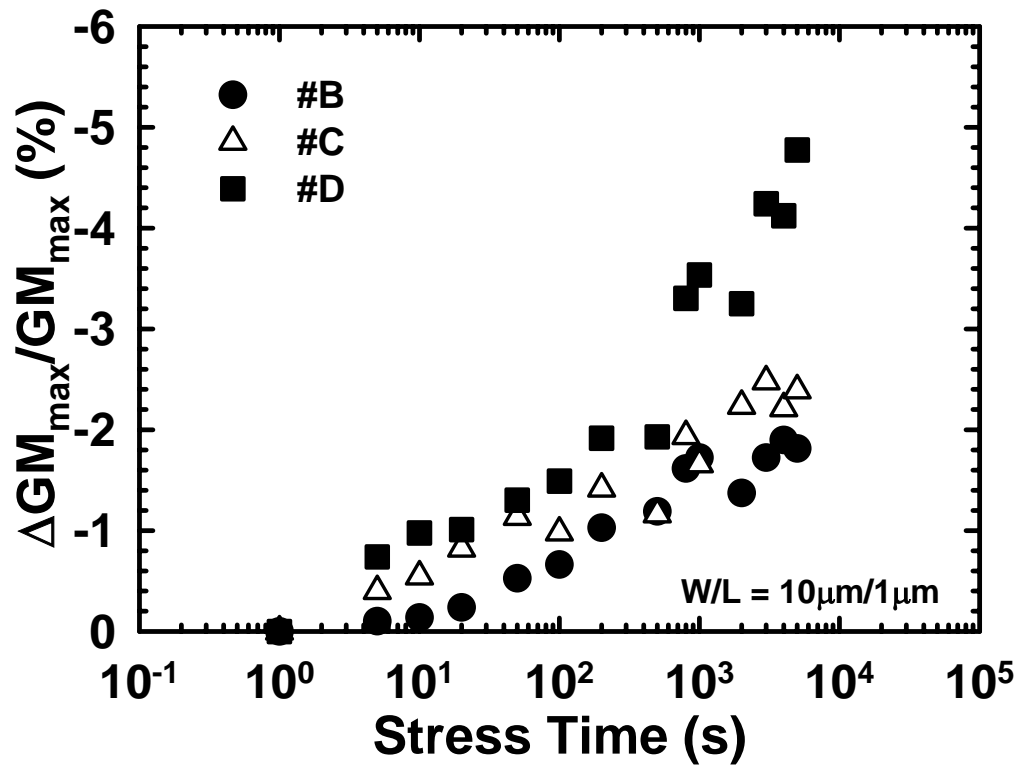
(C)

Fig. 3.13 (c) Transconductance degradation at 70°C during $V_{GO} = -3.5$ V stress aging for #A and #B.



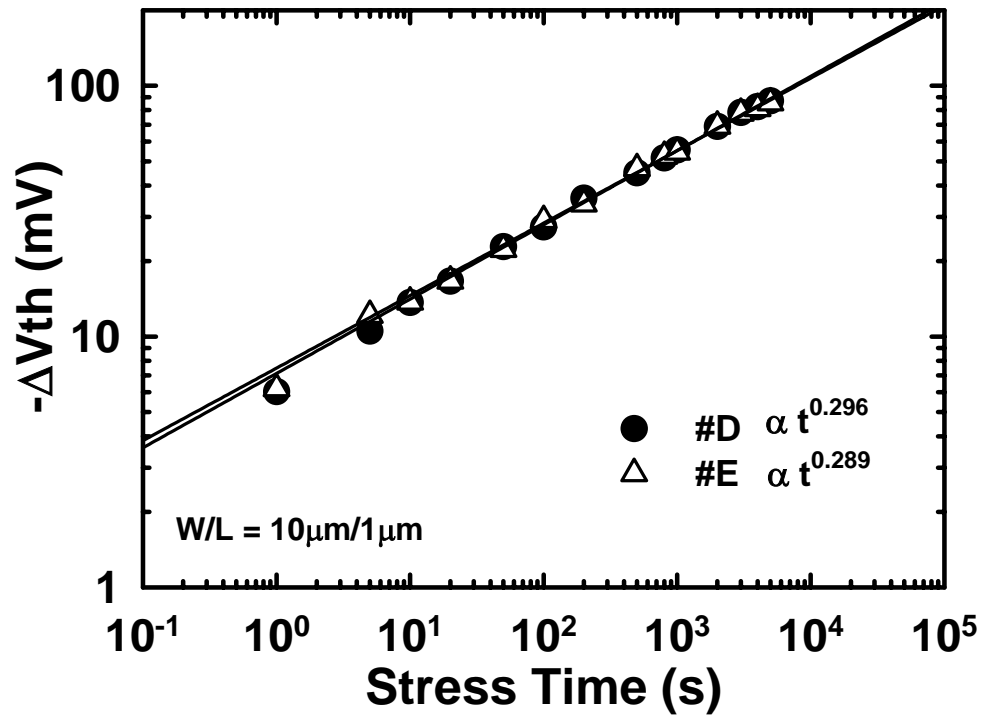
(b)

Fig. 3.14 (a) Threshold voltage shift, and (b) interface trap density increasing at 70°C during $V_{GO} = -3.5$ V stress aging for #B, #C, and #D.

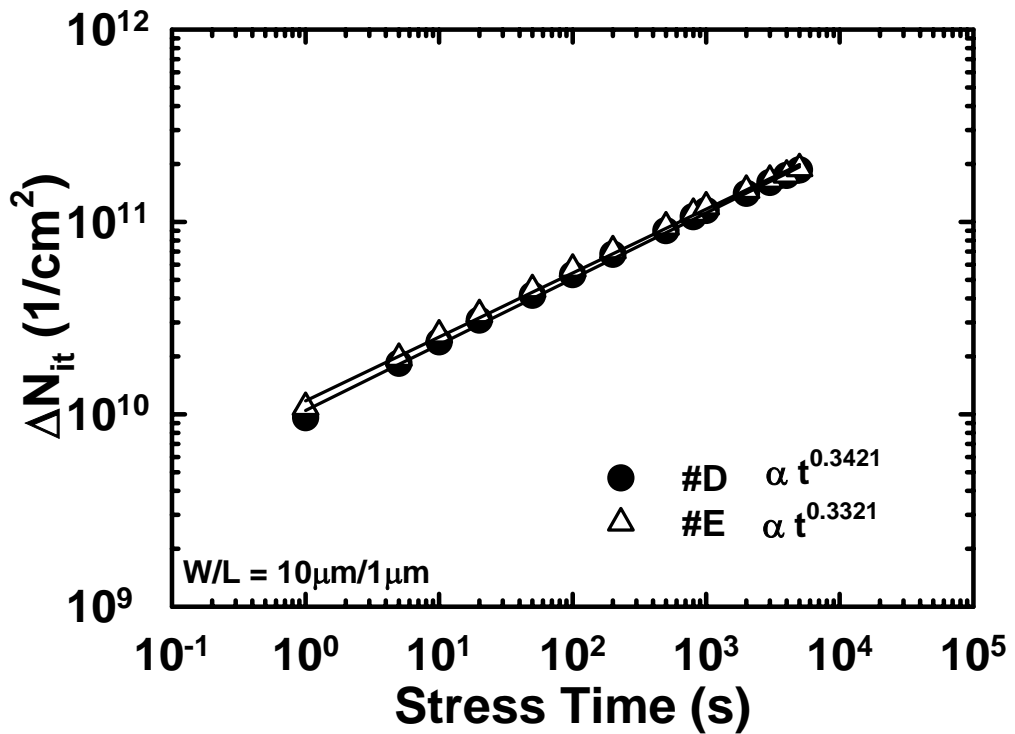


(c)

Fig. 3.14 (c) Transconductance degradation at 70°C during $V_{GO} = -3.5$ V stress aging for #B, #C, and #D.

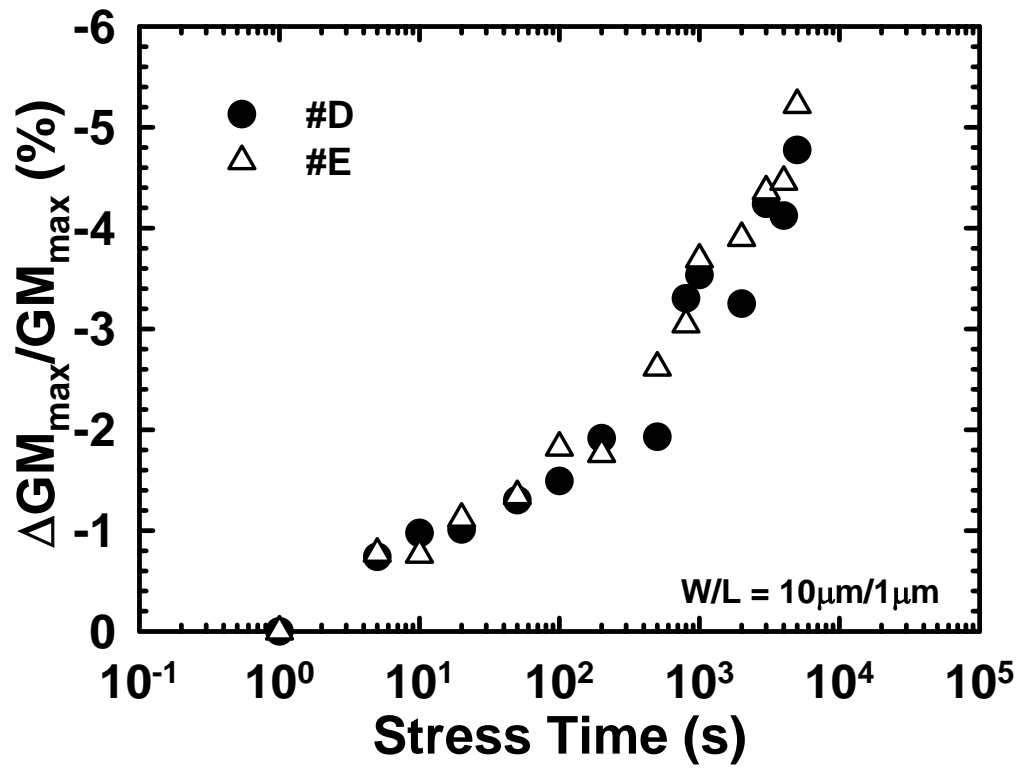


(a)



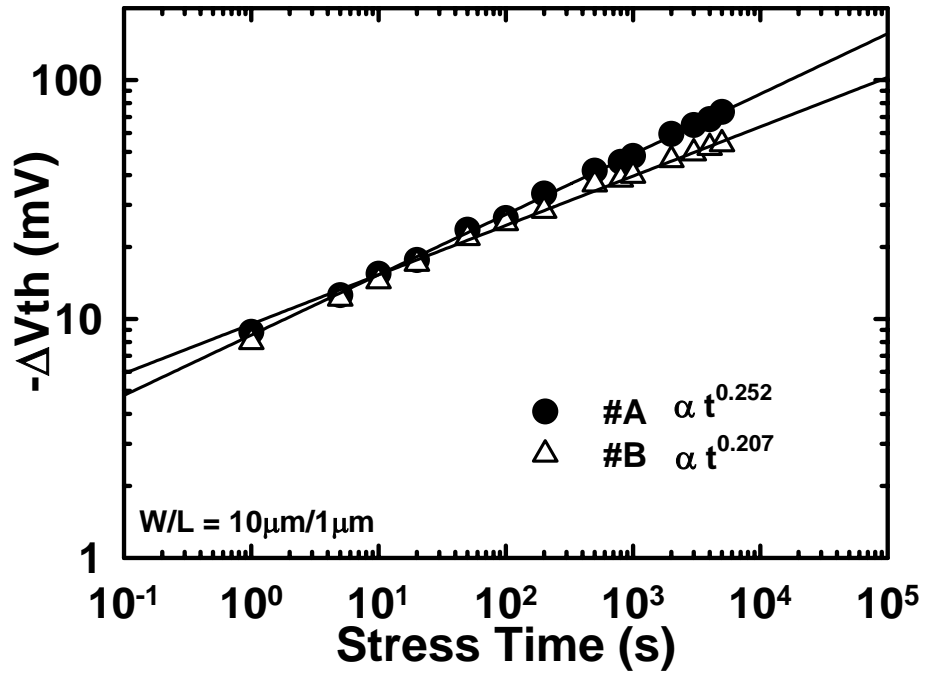
(b)

Fig. 3.15 (a) Threshold voltage shift, and (b) interface trap density increasing at 70°C during $V_{GO} = -3.5$ V stress aging for #D and #E.

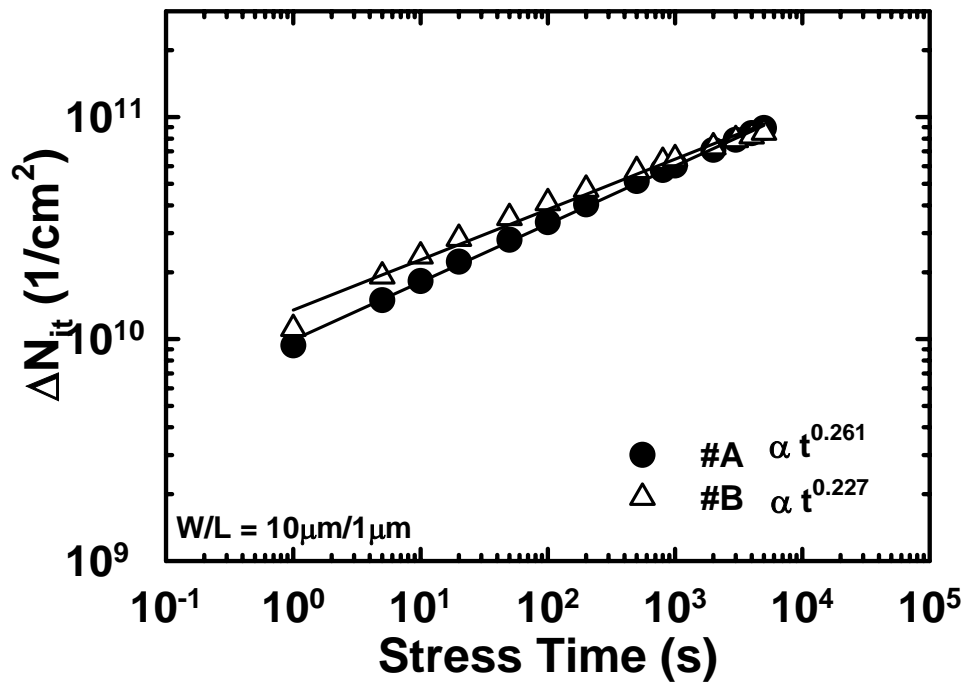


(c)

Fig. 3.15 (c) Transconductance degradation at 70°C during $V_{GO} = -3.5$ V stress aging for #D and #E.

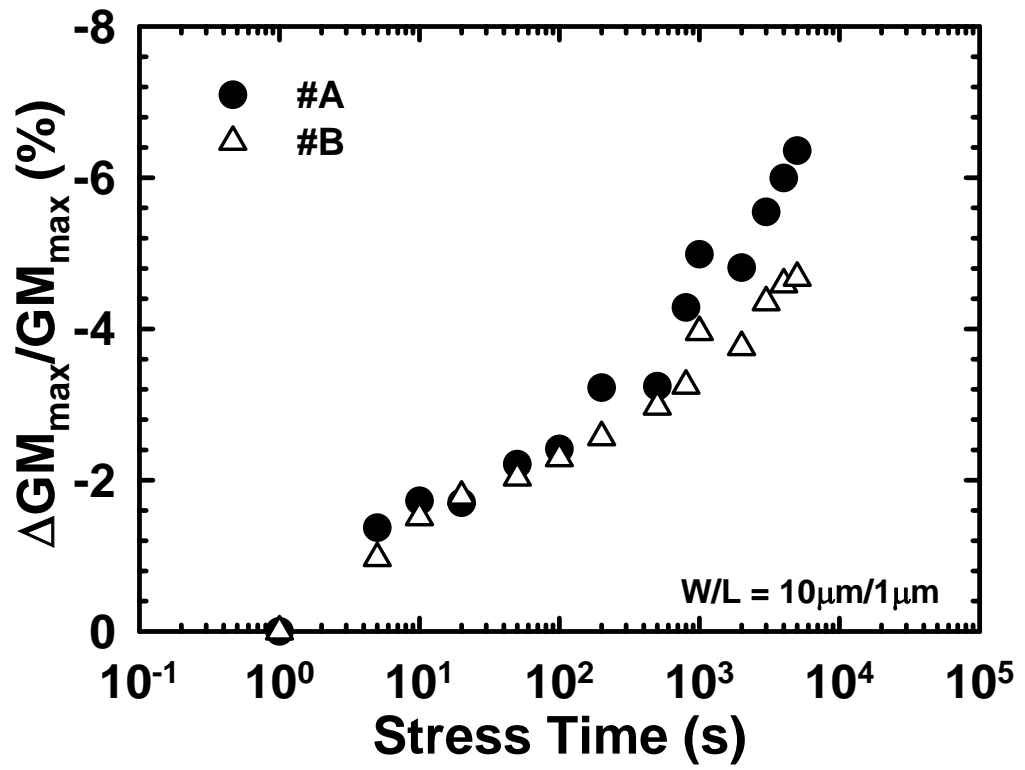


(a)



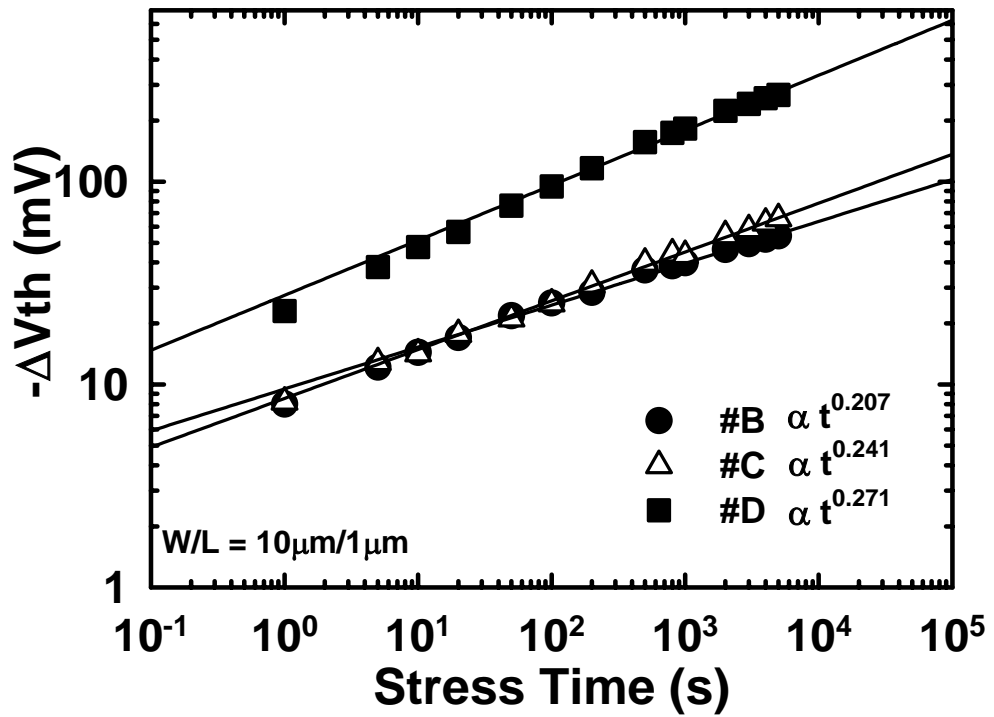
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Fig. 3.16 (a) Threshold voltage shift, and (b) interface trap density increasing at 130°C during $V_{GO} = -3.8$ V stress aging for #A and #B.

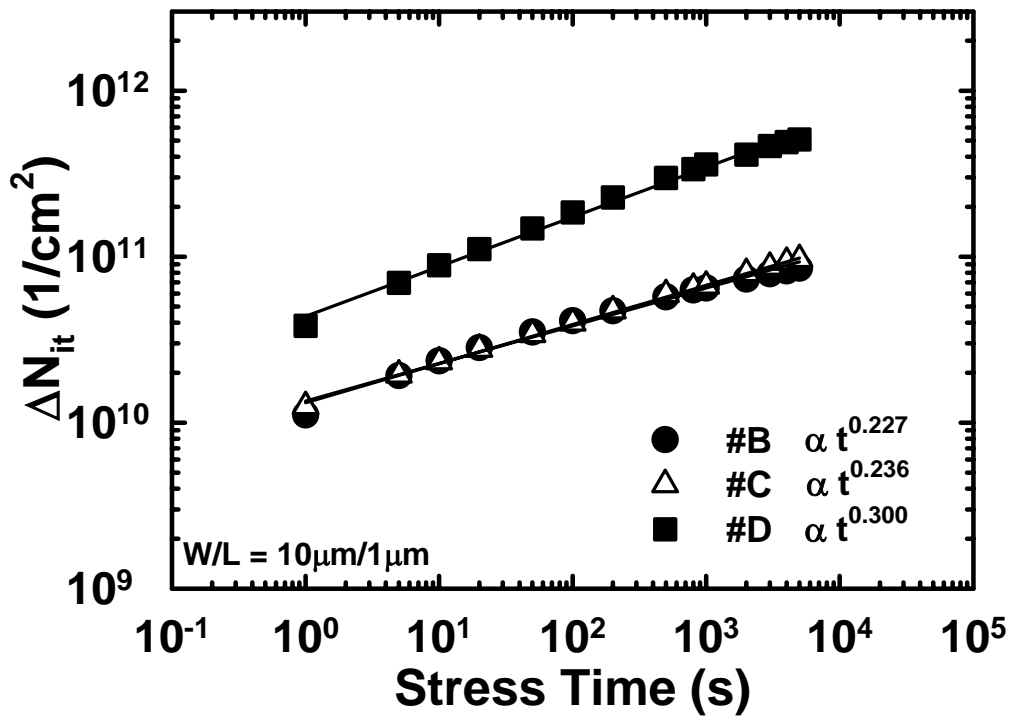


(c)

Fig. 3.16 (c) Transconductance degradation at 130°C during $V_{GO} = -3.8$ V stress aging for #A and #B.

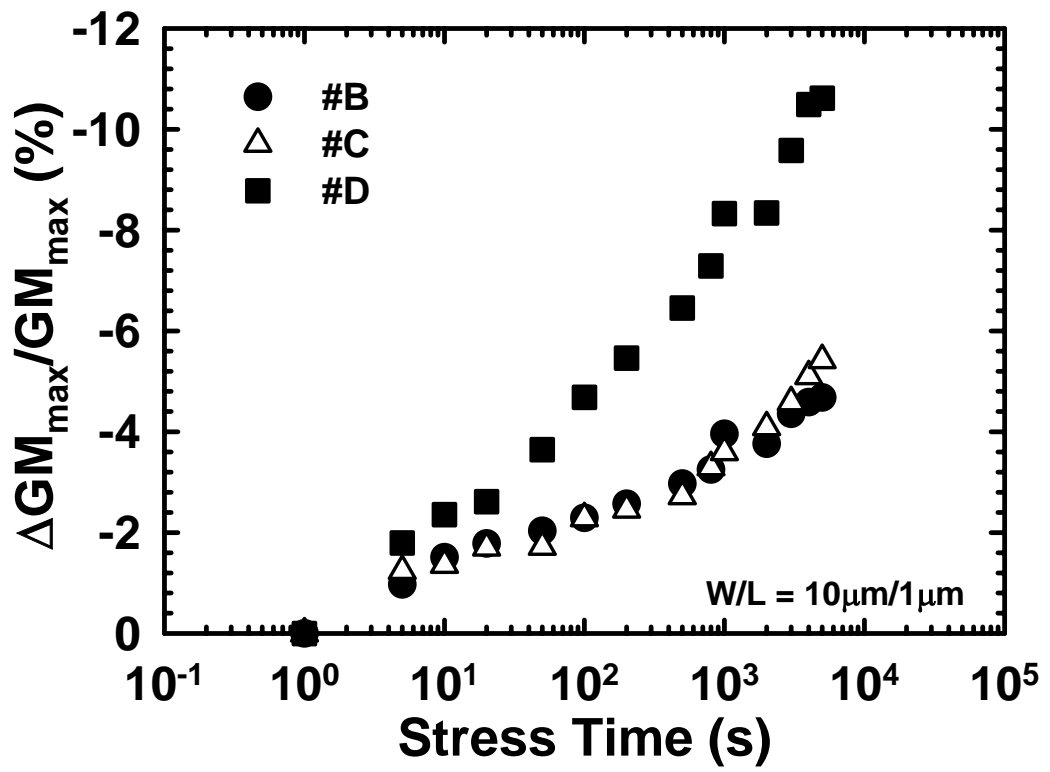


(a)



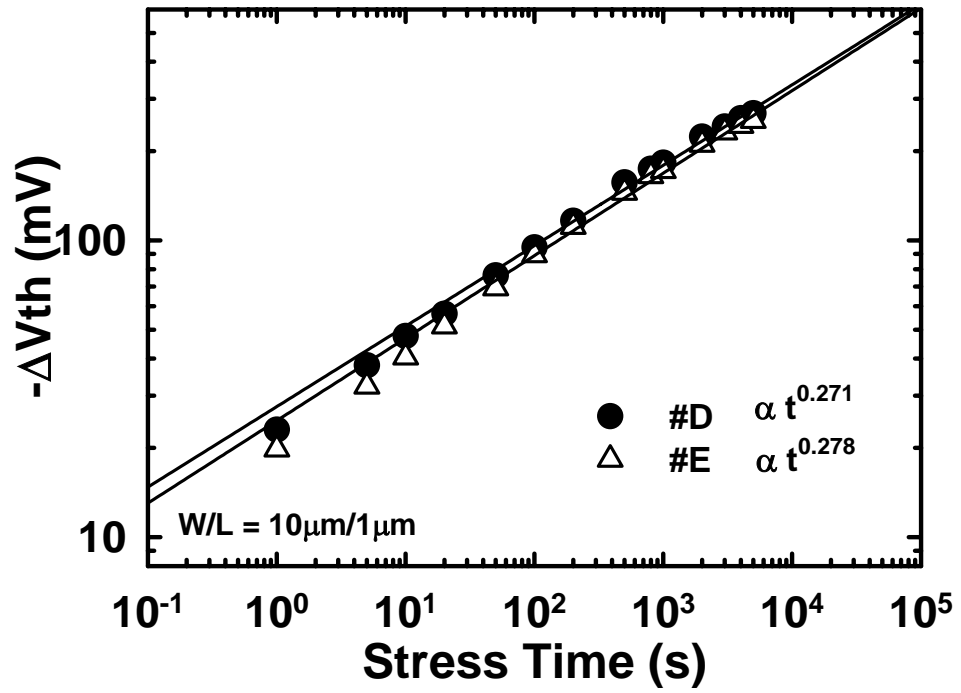
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Fig. 3.17 (a) Threshold voltage shift, and (b) interface trap density increasing at 130°C during $V_{GO} = -3.8$ V stress aging for #B, #C, and #D.

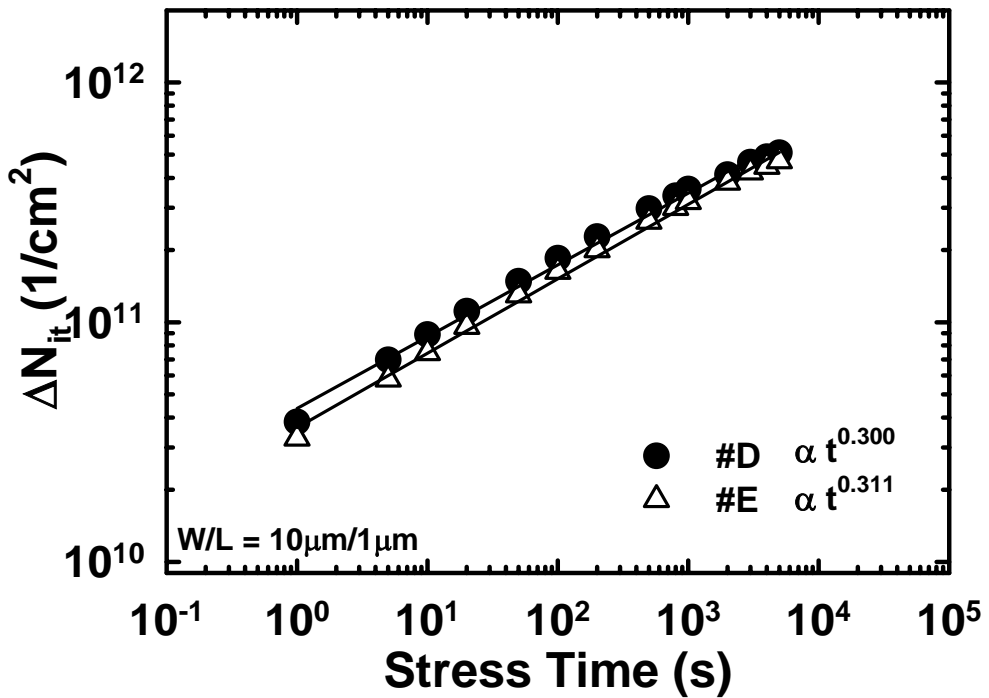


(c)

Fig. 3.17 (c) Transconductance degradation at 130°C during $V_{GO} = -3.8$ V stress aging for #B, #C, and #D.

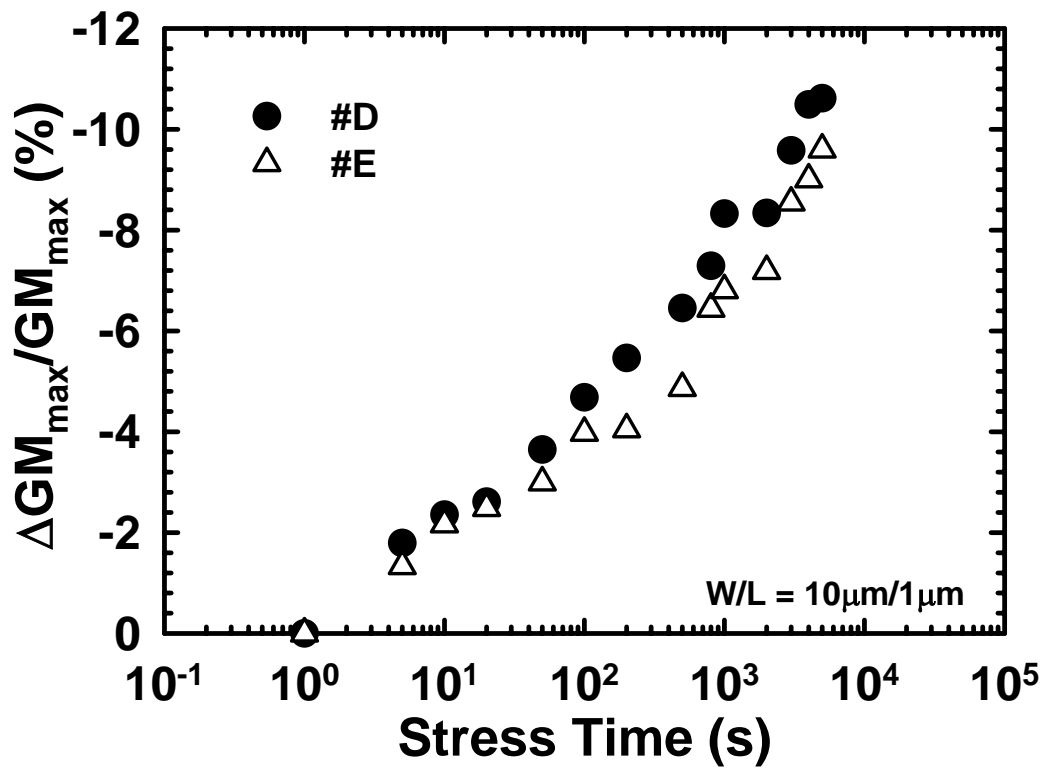


(a)



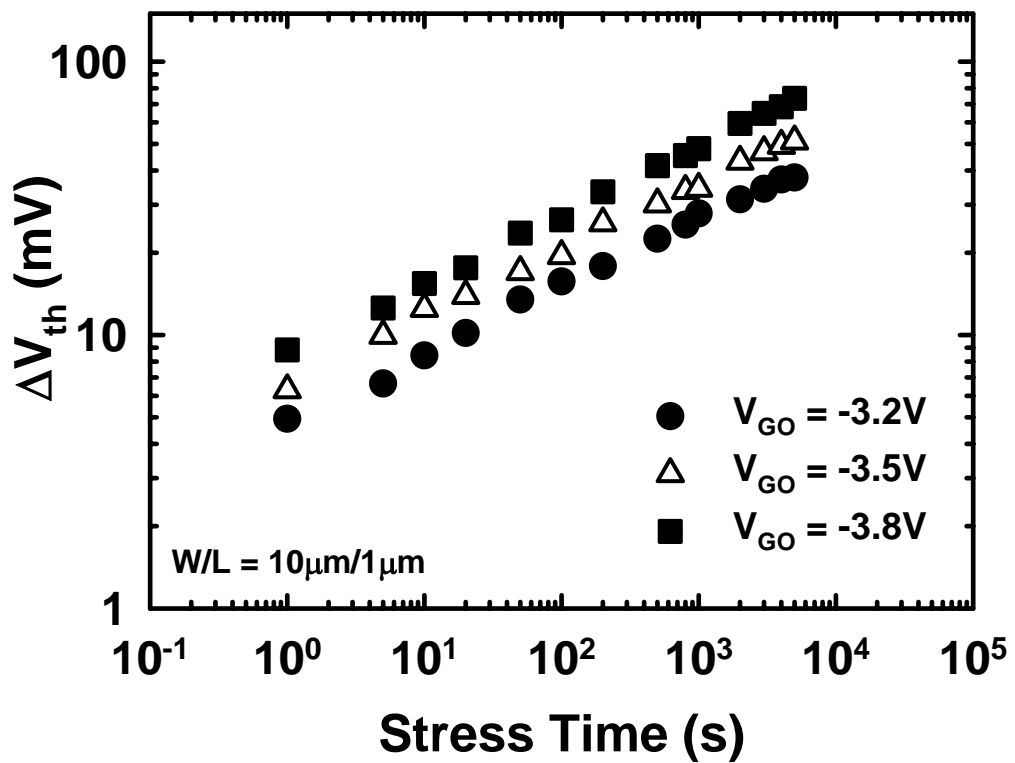
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Fig. 3.18 (a) Threshold voltage shift, and (b) interface trap density increasing at 130°C during $V_{GO} = -3.8$ V stress aging for #D and #E.

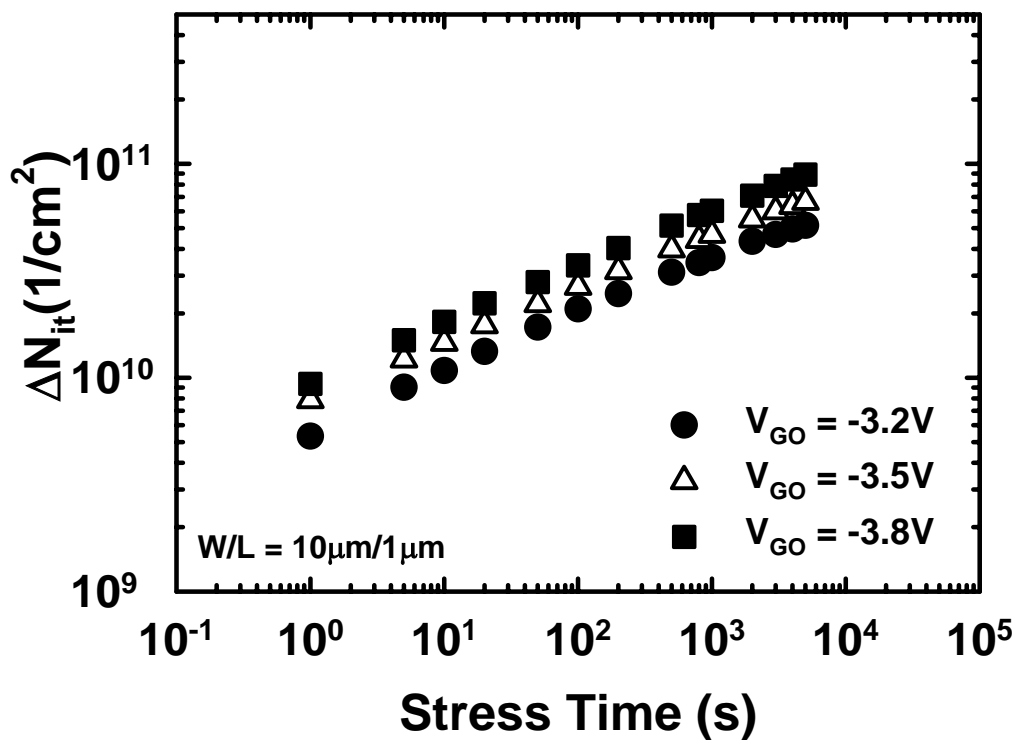


(c)

Fig. 3.18 (c) Transconductance degradation at 130°C during $V_{GO} = -3.8$ V stress aging for #D and #E.

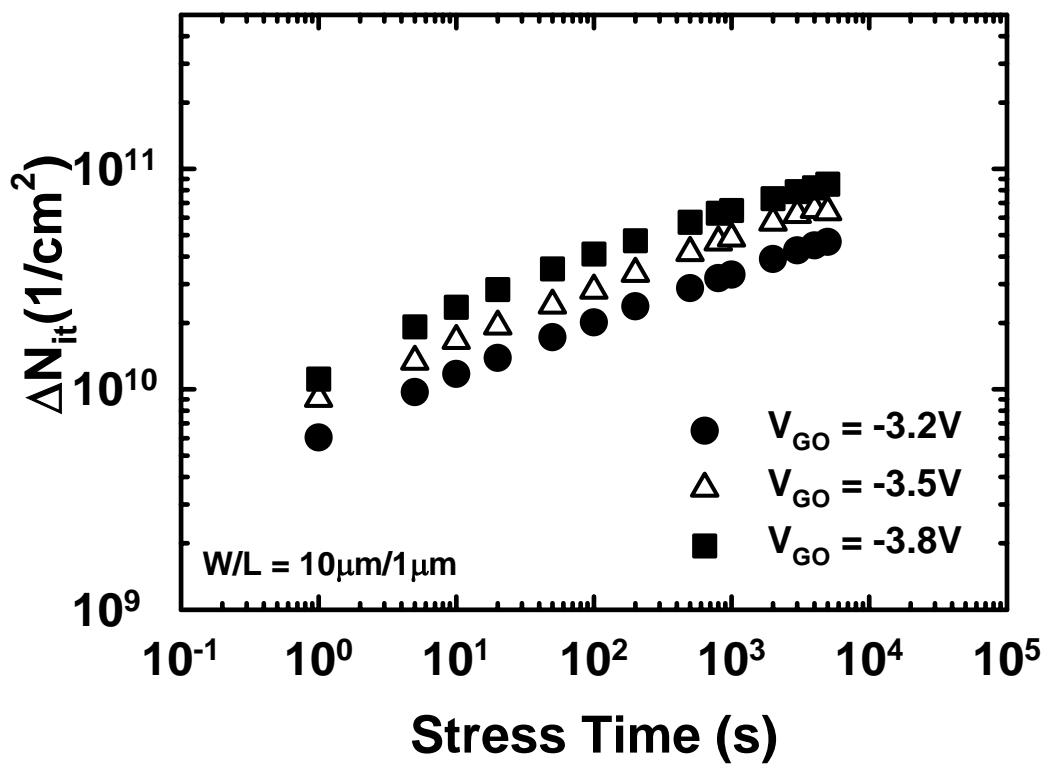
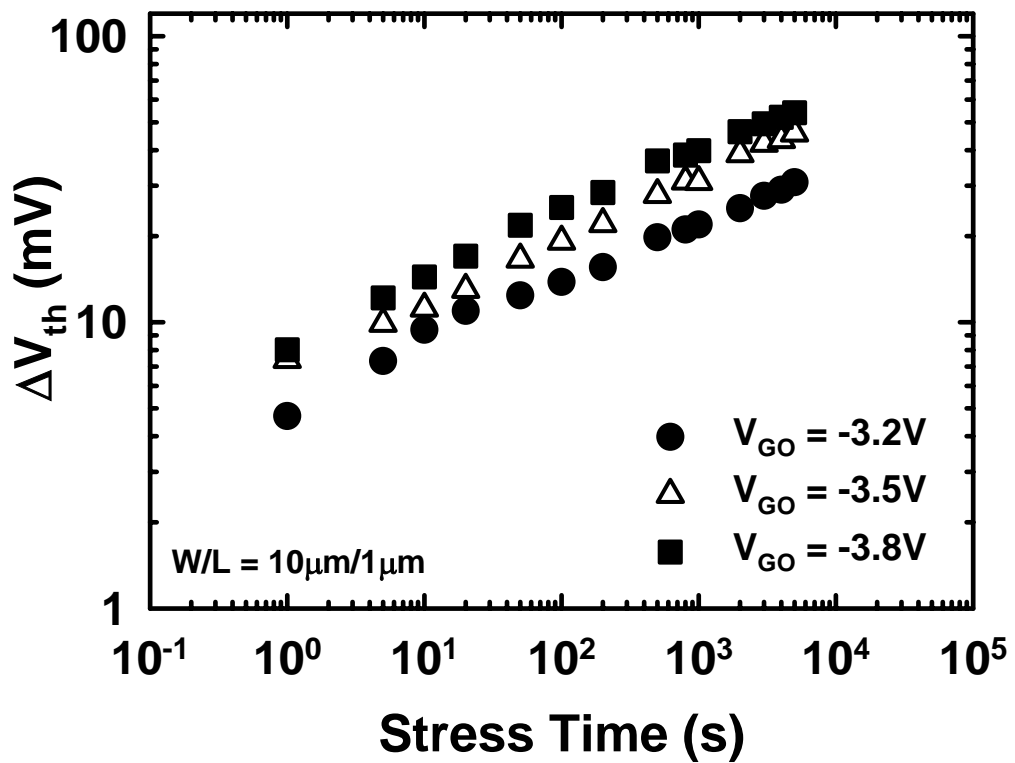


(a)



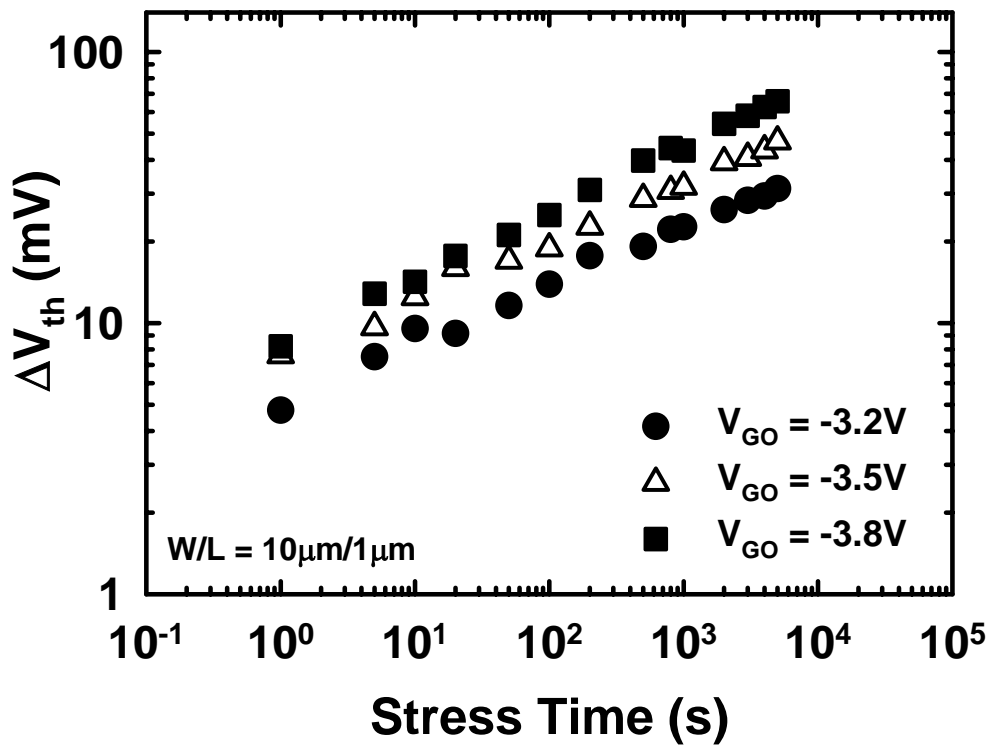
(b)

Fig. 3.19 (a) Threshold voltage shift, and (b) interface trap density increasing of #A at 130°C with different V_{GO} stresses.

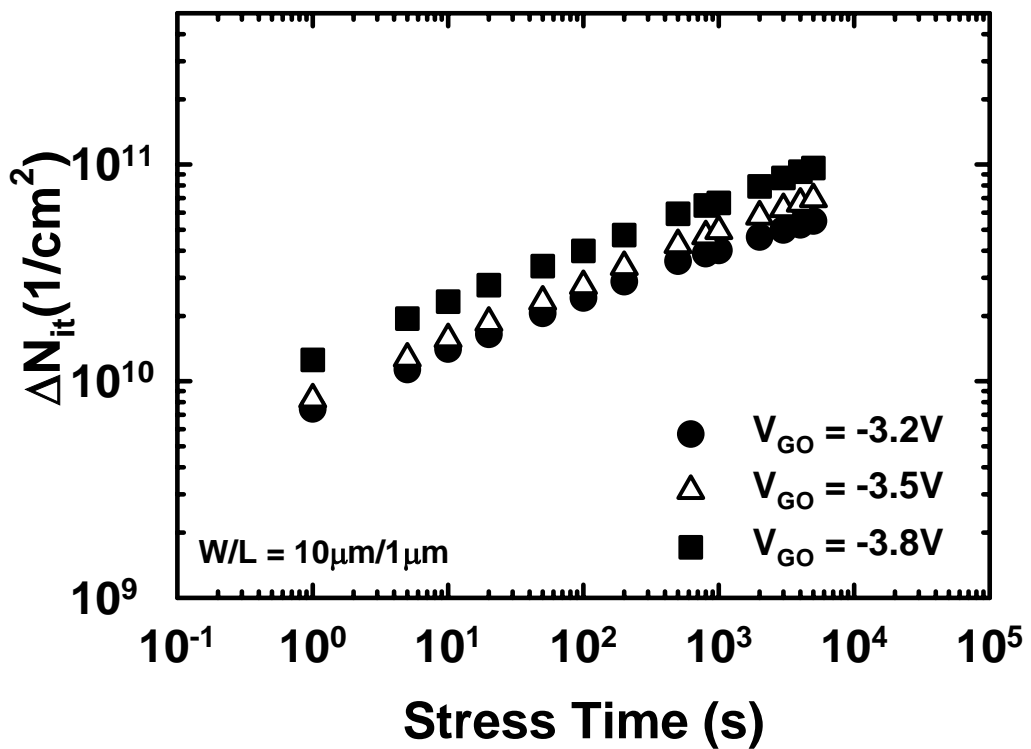


(b)

Fig. 3.20 (a) Threshold voltage shift, and (b) interface trap density increasing of #B at $130^\circ C$ with different V_{GO} stresses.

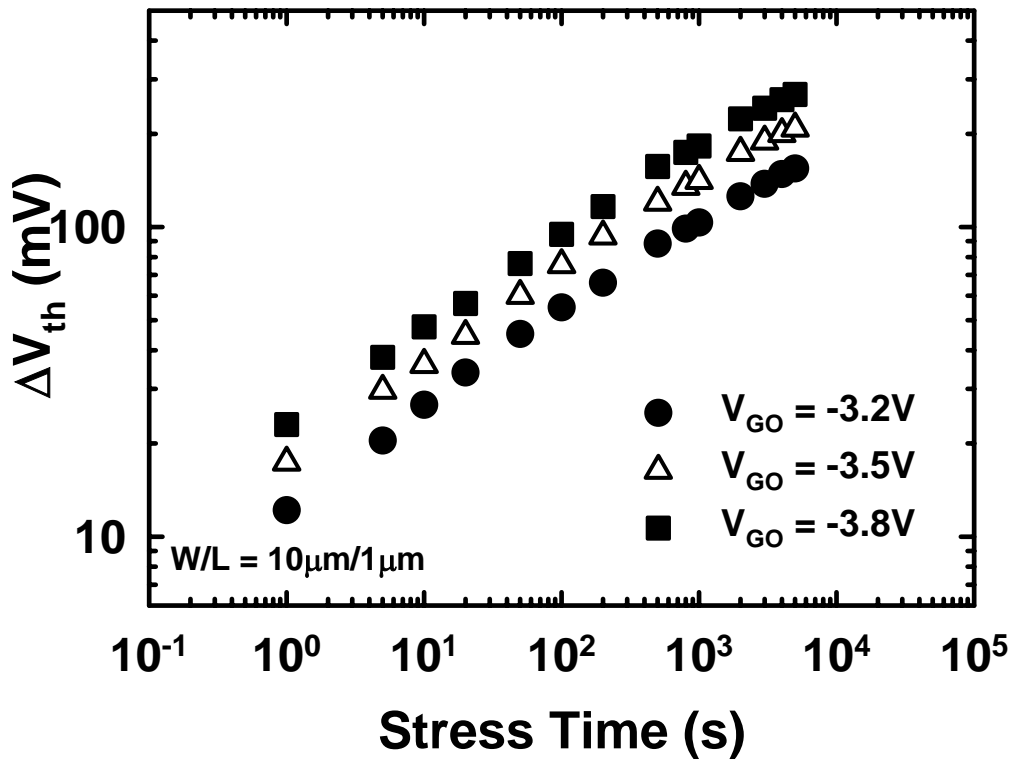


(a)

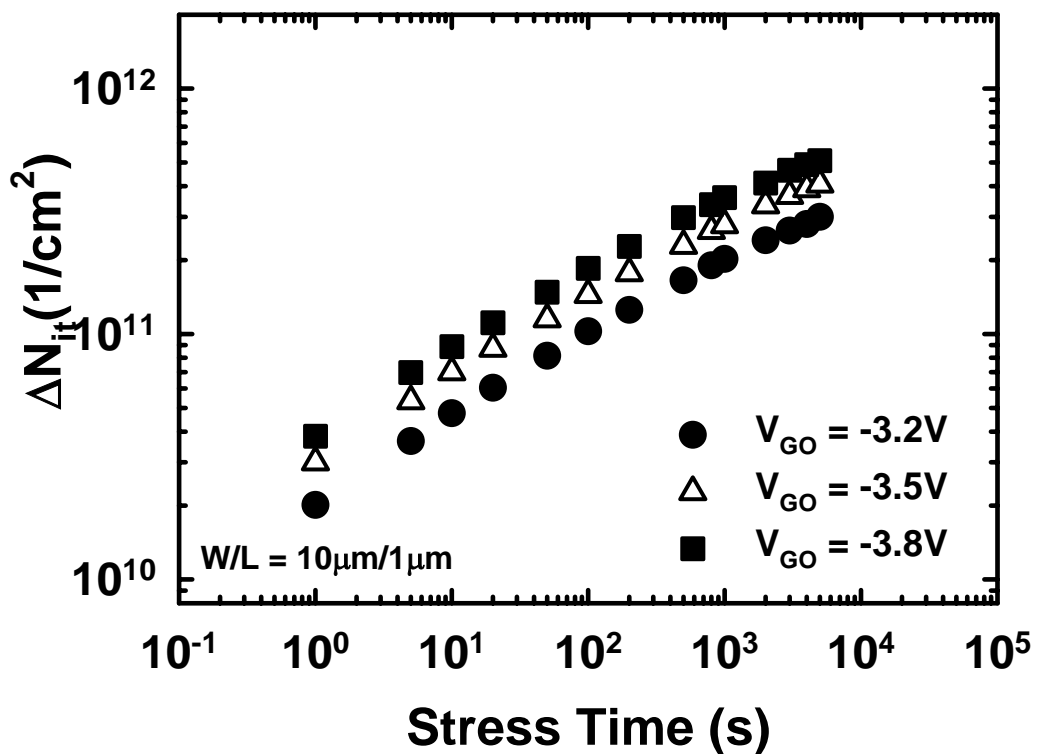


(b)

Fig. 3.21 (a) Threshold voltage shift, and (b) interface trap density increasing of #C at $130^\circ C$ with different V_{GO} stresses.

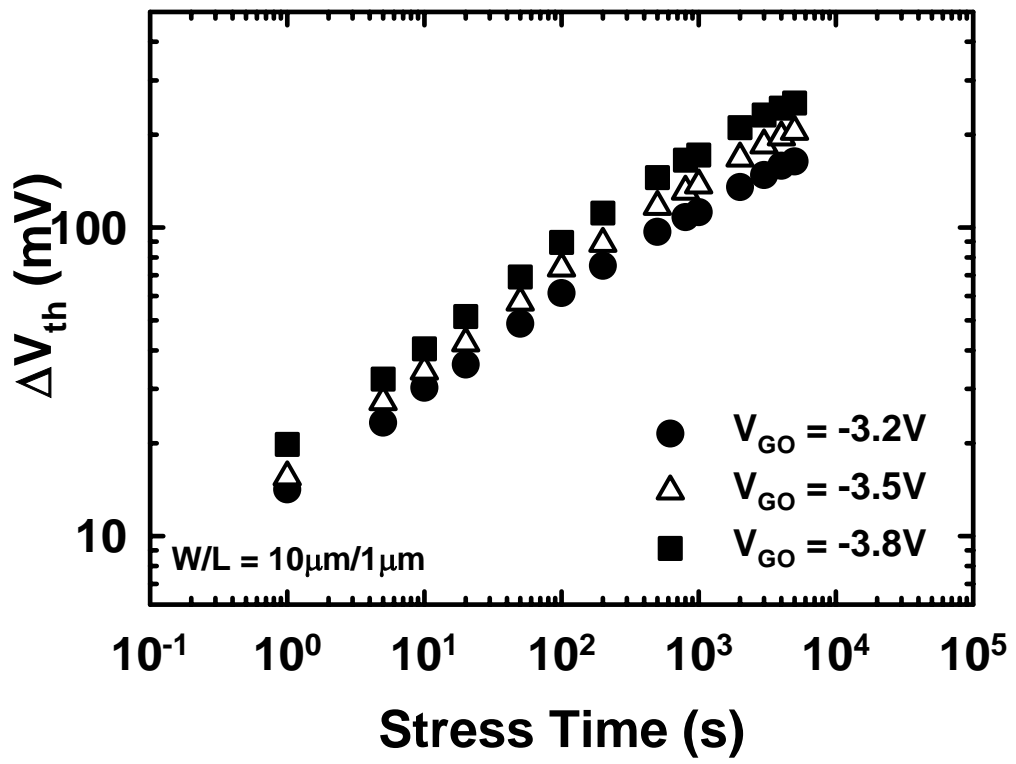


(a)

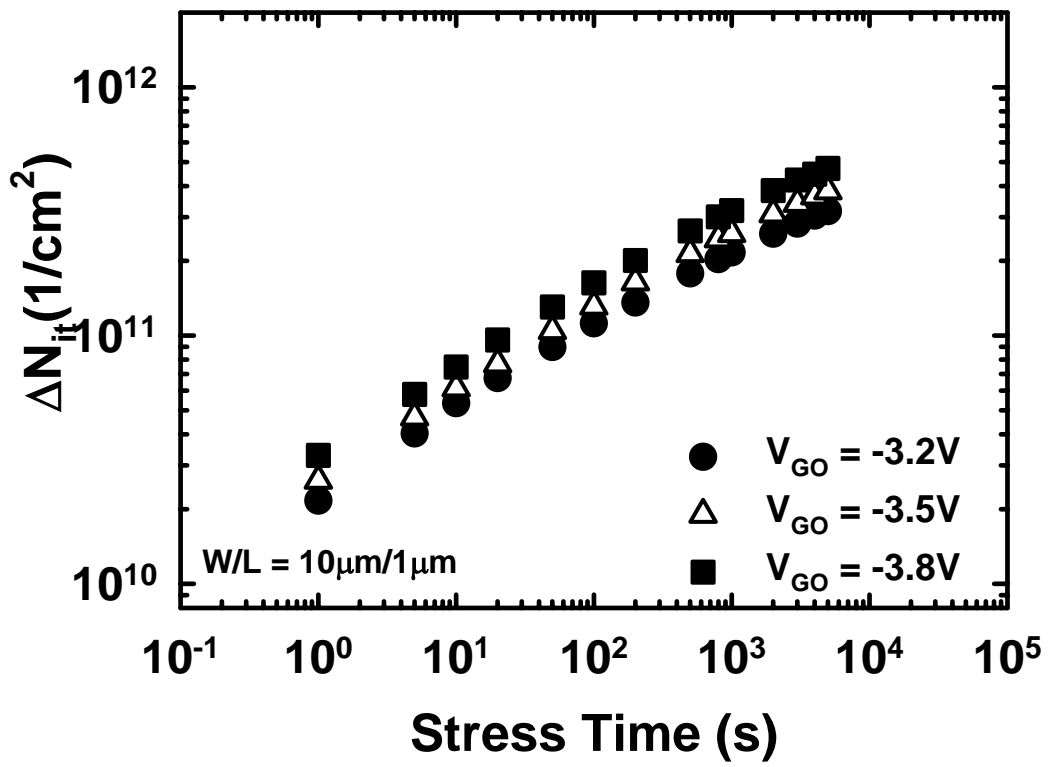


(b)

Fig. 3.22 (a) Threshold voltage shift, and (b) interface trap density increasing of #D at 130°C with different V_{GO} stresses.

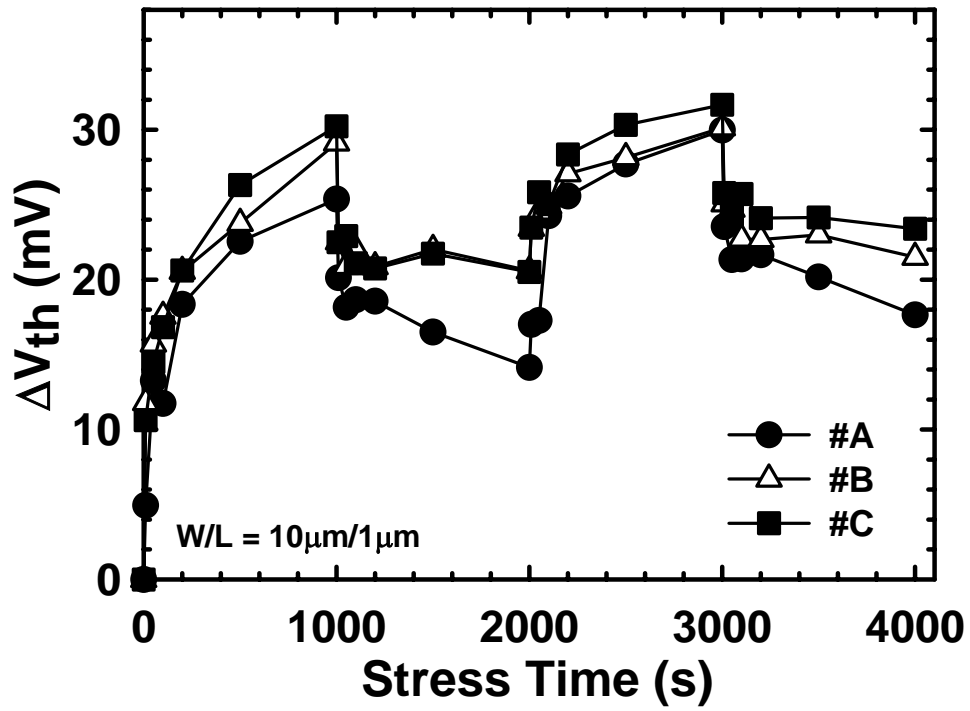


(a)

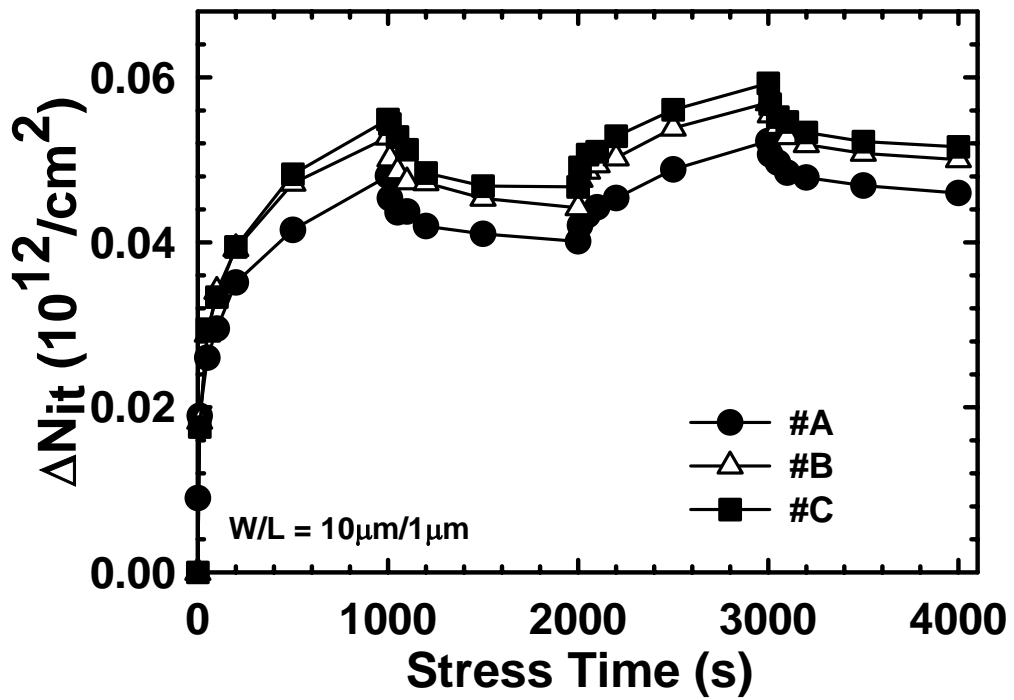


(b)

Fig. 3.23 (a) Threshold voltage shift, and (b) interface trap density increasing of #E at $130^\circ C$ with different V_{GO} stresses.

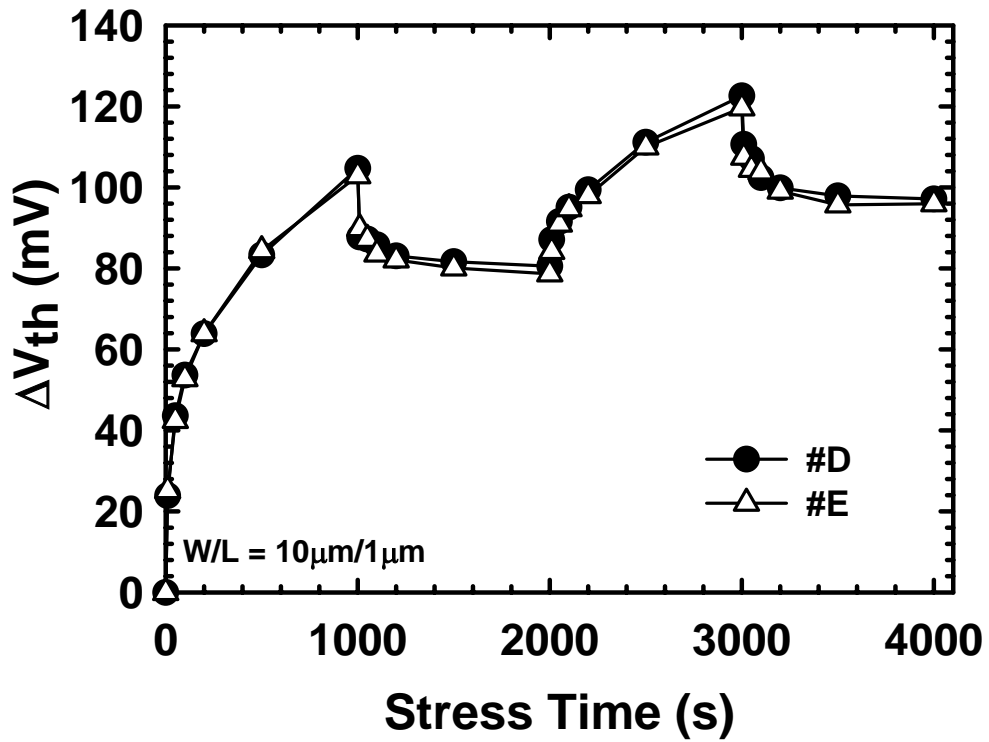


(a)

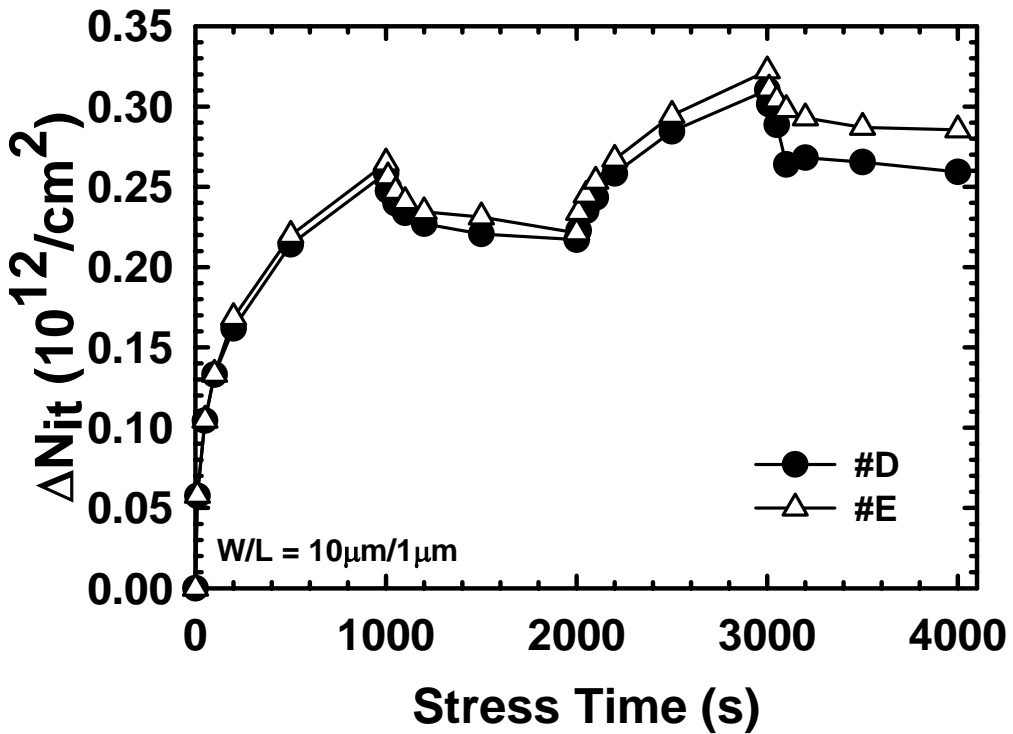


(b)

Fig. 3.24 (a) Threshold voltage shift, and (b) interface trap density change for #A, #B, and #C during $V_{GO} = -3.2V$ and passivation voltage = $0V$ at $130^{\circ}C$.

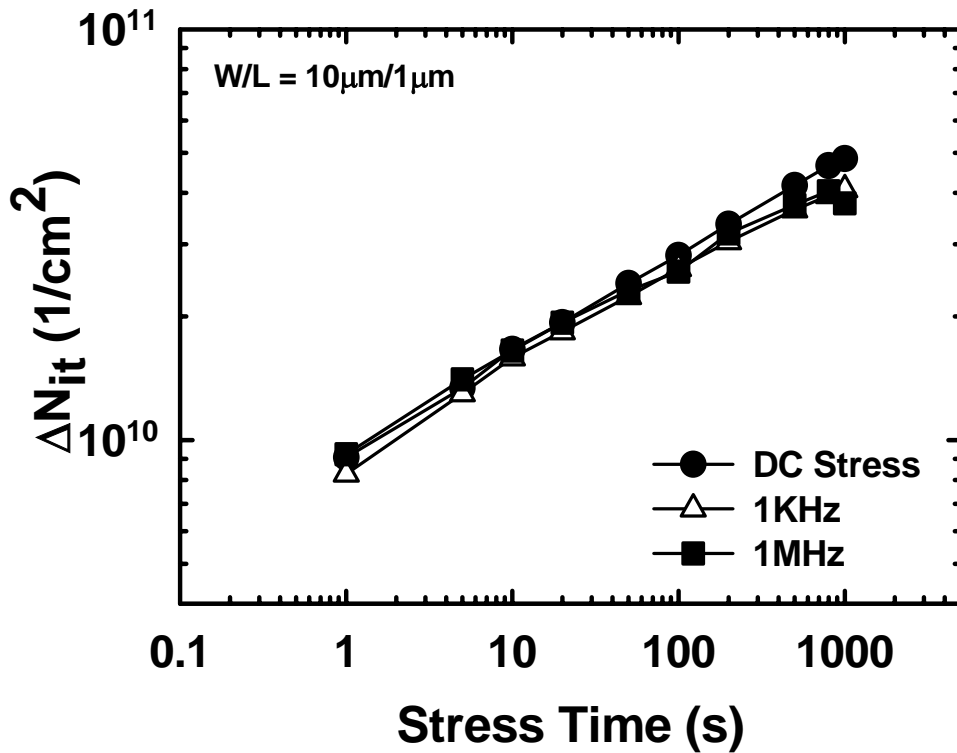
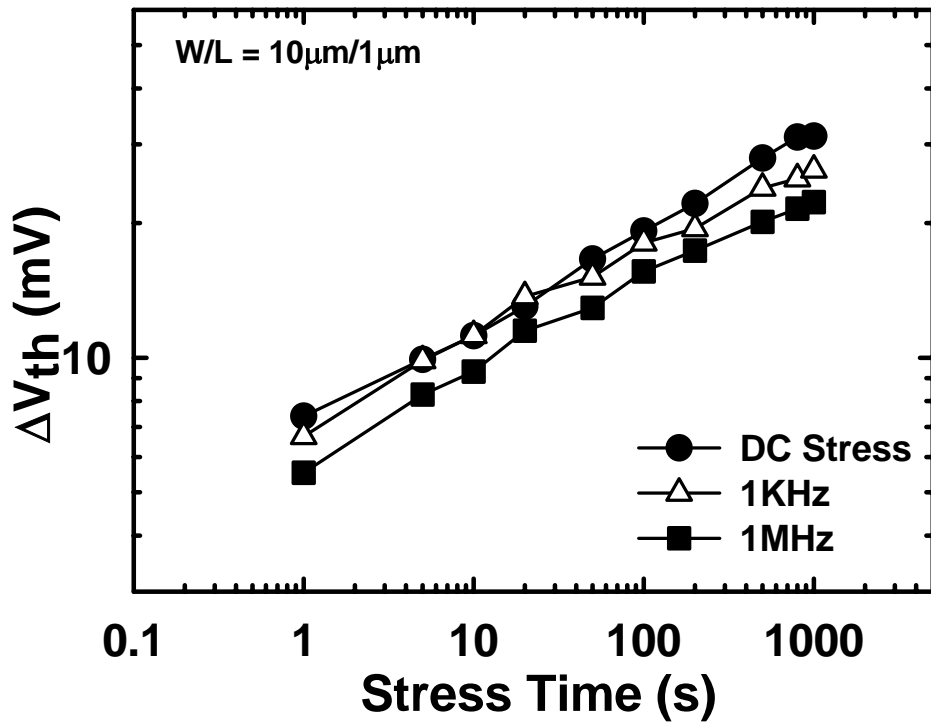


(a)



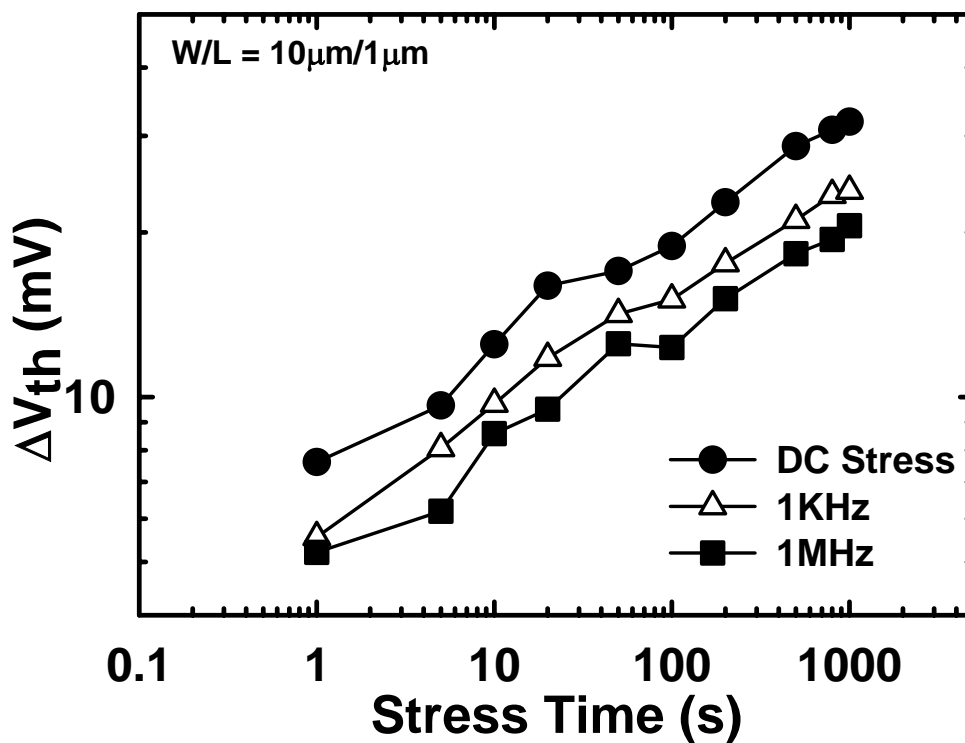
(b)

Fig. 3.25 (a) Threshold voltage shift, and (b) interface trap density change for #D and #E during $V_{GO} = -3.2V$ and passivation voltage = 0V at 130°C.

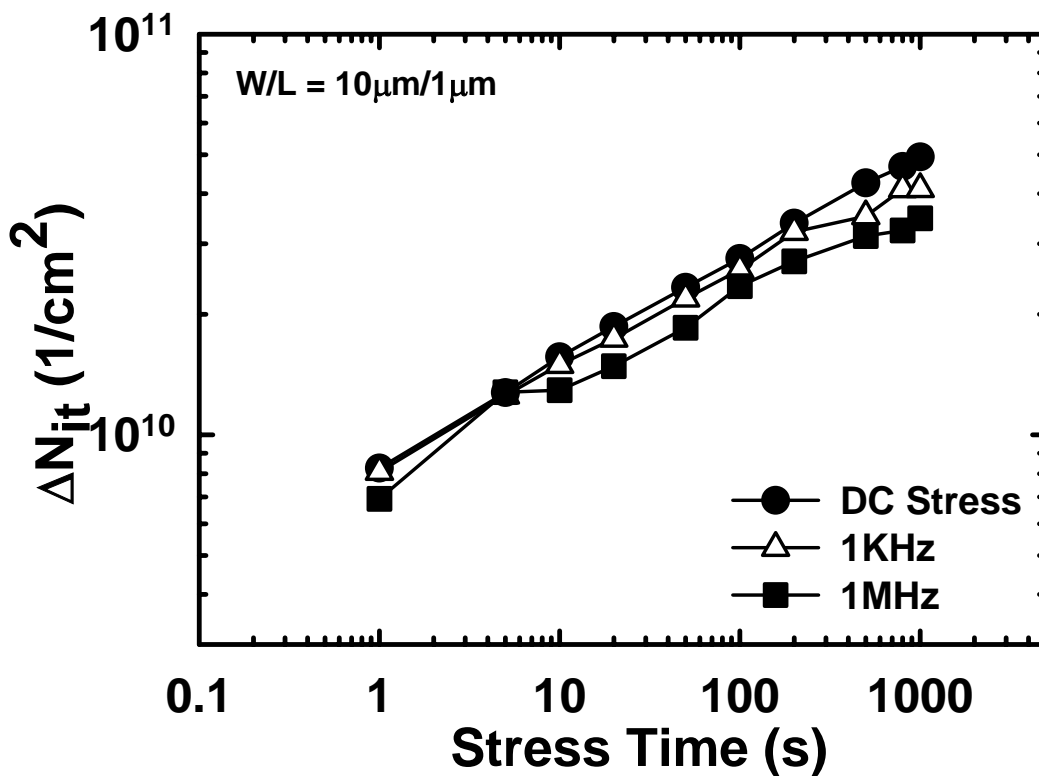


(b)

Fig. 3.26 (a) Threshold voltage shift, and (b) interface trap density change of #B during different frequency AC stresses ($V_{Go} = -3.5V$) at 130°C.

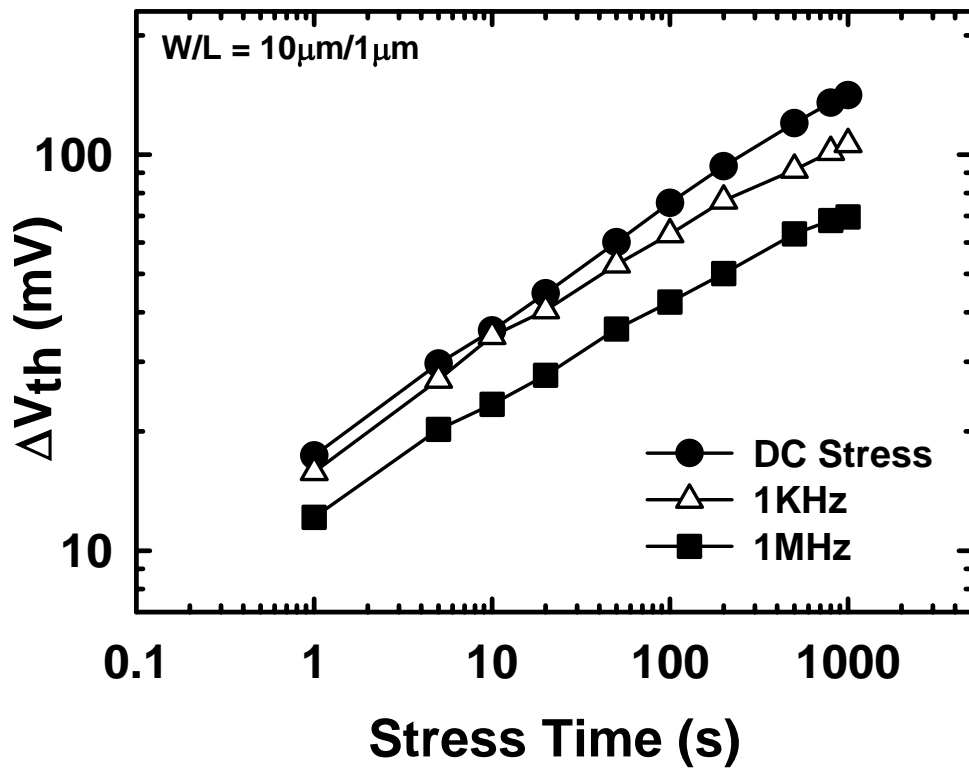


(a)

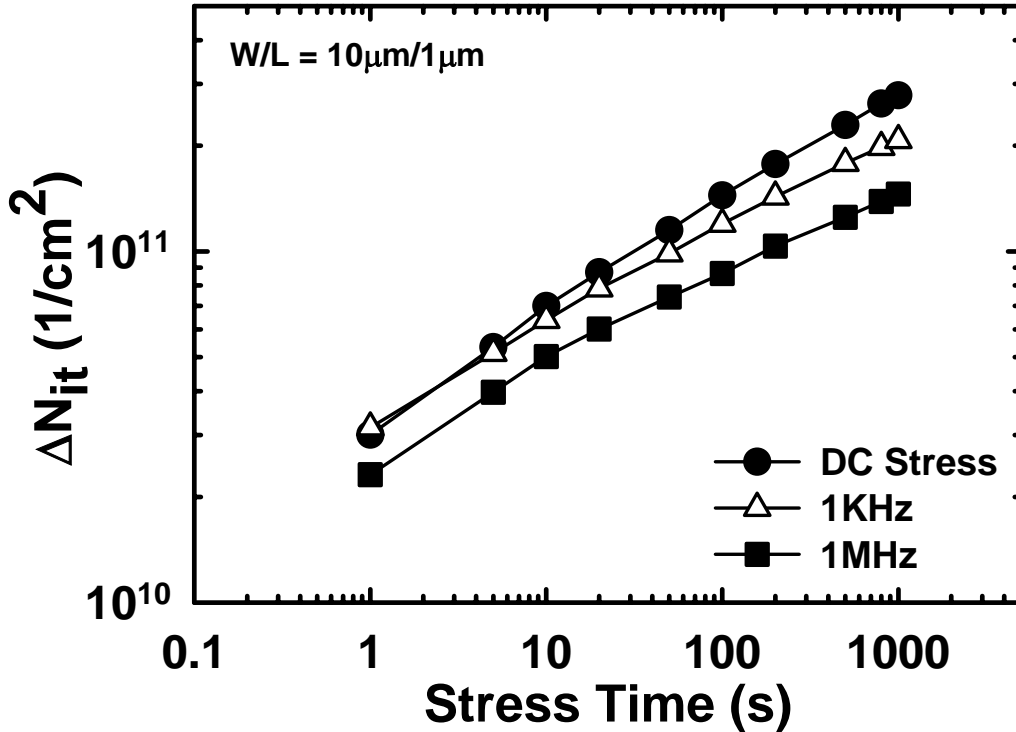


(b)

Fig. 3.27 (a) Threshold voltage shift, and (b) interface trap density change of #C during different frequency AC stresses ($V_{Go} = -3.5V$) at 130 $^{\circ}C$.

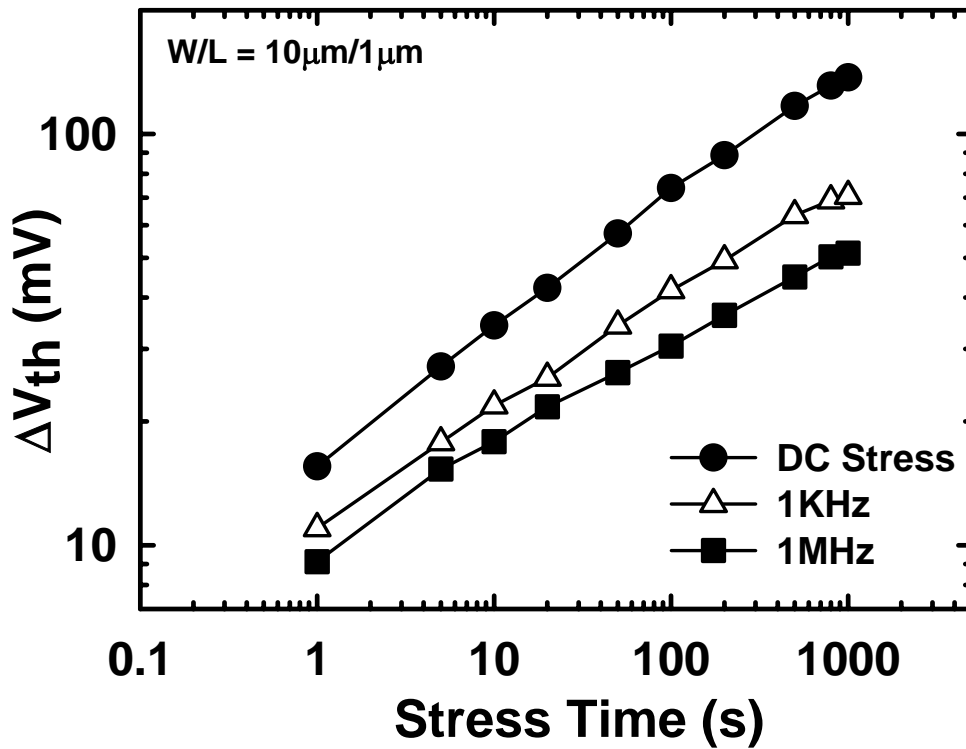


(a)

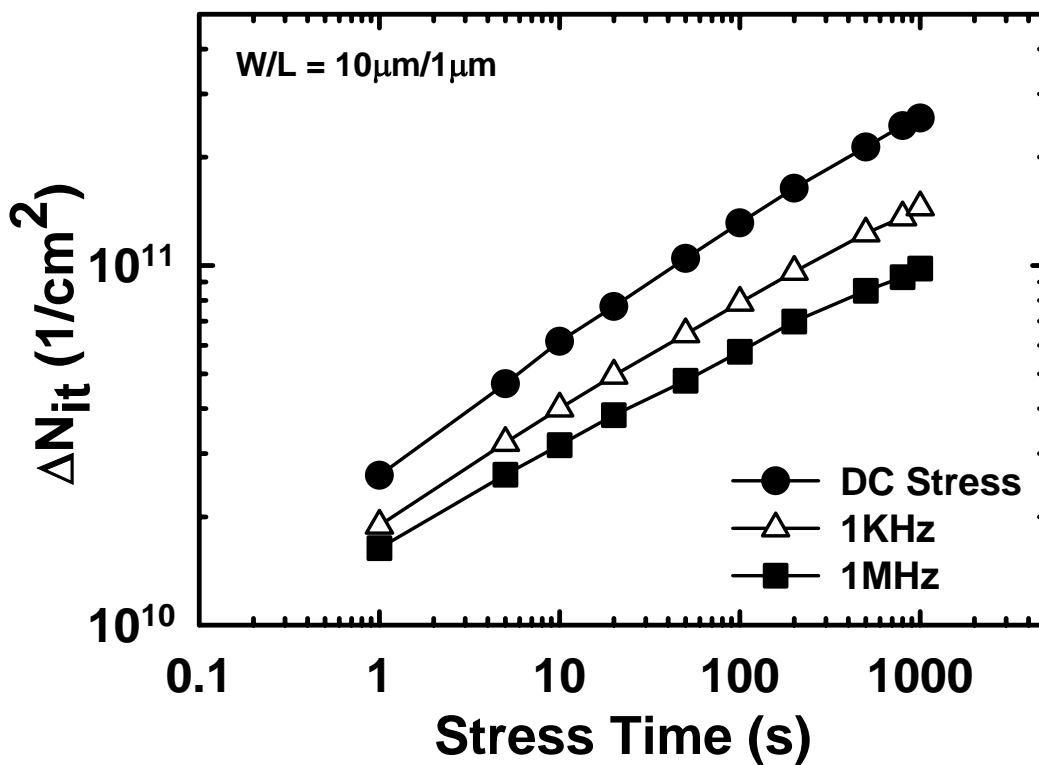


(b)

Fig. 3.28 (a) Threshold voltage shift, and (b) interface trap density change of #D during different frequency AC stresses ($V_{Go} = -3.5V$) at 130°C.

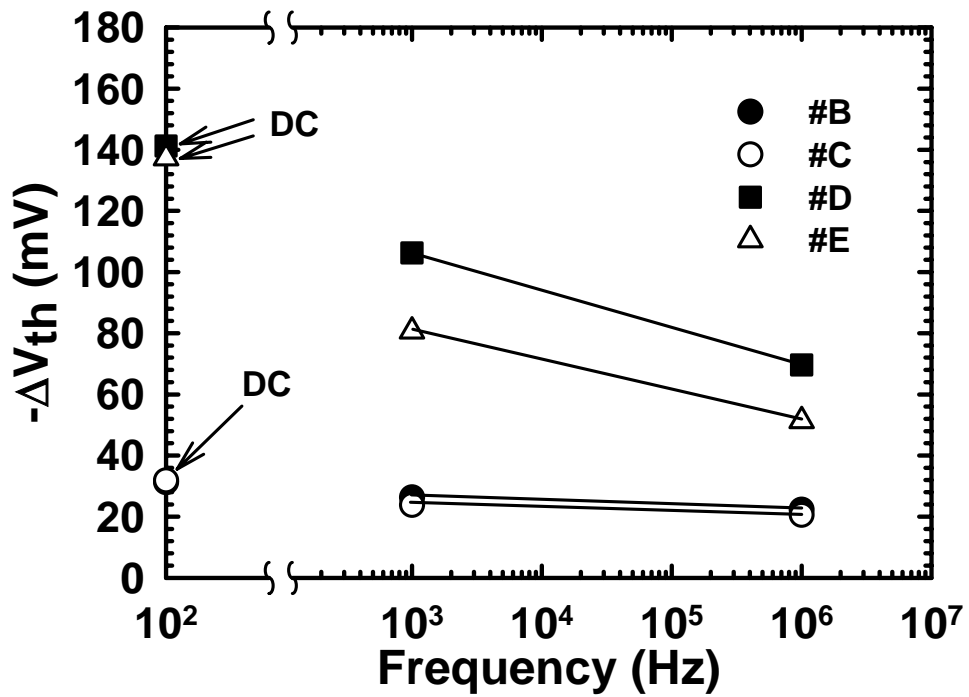


(a)

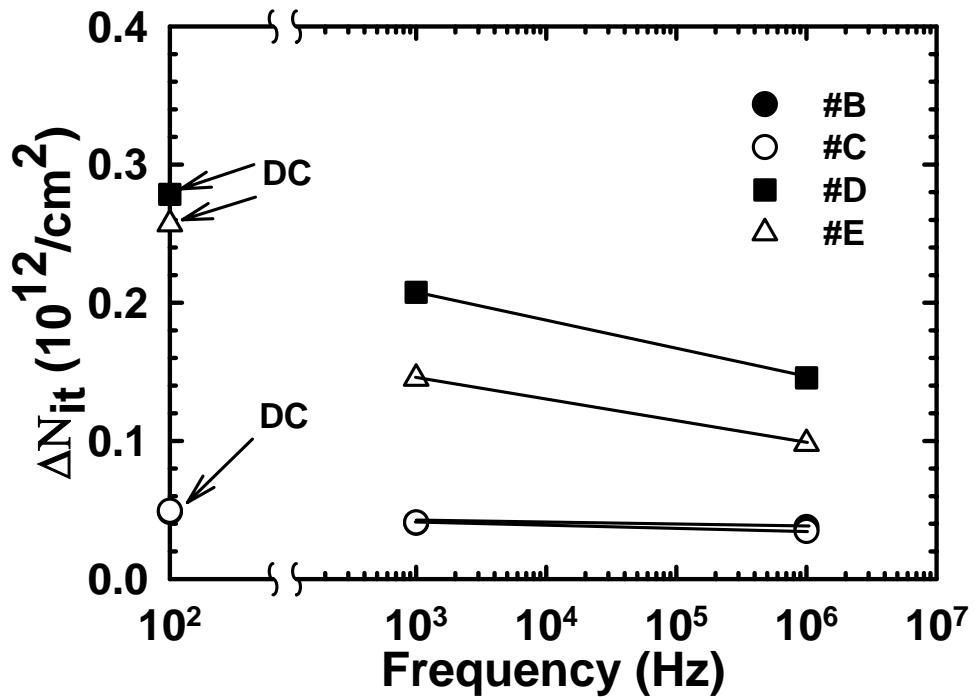


(b)

Fig. 3.29 (a) Threshold voltage shift, and (b) interface trap density change of #E during different frequency AC stresses ($V_{Go} = -3.5V$) at 130°C.



(a)



(b)

Fig. 3.30 (a) Threshold voltage shift, and (b) interface trap density change as a function of frequency for devices with different split conditions, after $V_{GO} = -3.5\text{V}$ 1000sec stress at 130°C .

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論文題目：氫含量對於矽鍺閘極元件之特性與可靠度分析

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