國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

矽鍺奈米線在不同製程條件下之電特性研究

A Study of Electrical Properties under Various Process Conditions for SiGe Nanowire

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摘要

本論文中我們成功地利用間隙壁（spacer）製做出奈米等級的矽鍺奈米線，在不同的溫度、時間，將矽鍺氧化，探討在不同條件下所造成的鍺含量和所對應的電性分析，再和傳統的複晶矽奈米線去作比較。所有的矽鍺薄膜都是利用冷壁式超高真空化學氣相沉積法（UHVCVD）在二氧化矽(SiO_2)上沉積而成。我們利用掃瞄式電子顯微鏡 Scanning Electron Microscopy (SEM)去觀察氧化前後的矽鍺奈米線的大小，發現在相同的製程條件下矽鍺奈米線和矽鍺薄膜有相同的氧化趨勢。此外，我們還可以利用鍺緻密化(Ge condensation)的技術做出更小的奈米線，增加其傳導率(conductivity)。

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Abstract

In the thesis, we successfully utilize the spacer to fabricate a SiGe nanowire, which oxidized at different temperatures, times, discussion the germanium content relative electrical analysis under the variant condition, and make the comparison with the conventional Poly-Si nanowire. All the SiGe films are deposition on SiO_2 by cold-wall ultrahigh vacuum chemical vapor deposition (UHVCVD). We utilize Scanning Electron Microscopy (SEM) to observe the silicon germanium nanowire size before oxidation and after oxidation, discovery silicon germanium nanowire and silicon germanium thin film has the same oxidized tendency under the same oxidation condition. Additionally we also can utilized the technology of Ge condensation to makes a smaller nanowire, increases its conductivity.

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Chapter 1

Introduction

1.1 Background

For improving device performance, the strain-or band-structure-induced mobility enhancement to increase the drive current may also be employed. One of the most notable effects is the enhanced hole mobility in silicon–germanium (SiGe) under biaxial compressive strain. Recently, there have been demonstrations of enhanced performance for p-type SiGe-channel MOSFET on bulk Si substrate down to a channel length of 100 nm. The introduction of SiGe offers the possibility of bandgap engineering in the Si system and thus the realization of n- and p-type heterostructure MOSFETs.

The recent research on silicon heterostructure MOSFETs (HMOSFETs) is strongly motivated by the anticipated compatibility with the existing Si-CMOS fabrication technology. Presently, SiGe HMOSFETs are manufactured by modifying some of the fabrication steps of a commercially available Si-CMOS technology. The most important requirement to avoid the strain relaxation being the low thermal budget essential for processing strained SiGe layers.

1.2 The characteristics of SiGe

As channel length of metal-oxide-semiconductor field-effect transistors (MOSFETs) is deeply scaled down to sub-100nm, enhancing the carrier mobility in the channel is desired for improving the

performance of complementary MOS (CMOS) circuits. For this purpose Ge is a promising channel material for MOSFETs because of high mobility of both the electrons and holes. In addition, the hole mobility in Ge is about a factor of 5 higher than in Si (2000 cm^2/V s in bulk undoped Ge at room temperature) [1]. Theoretical calculations have predicted a very high hole mobility in compressively strained SiGe alloys [2-3]. This is attributed to the strain-induced heavy-hole (hh)/light-hole (lh) splitting. The holes have a light n-plane effective mass (dependent upon alloy composition), and thus the room temperature hole mobility is predicted to be 3-10 times higher than in Si (the highest value for bulk undoped Si is about 400 cm^2/V s) [1], Additionally, some of the key features of the oxidation of SiGe from the above studies can be summarized as follows [4-6]: (1) During oxidation, Ge is completely rejected from the oxide and piles up at the oxide/substrate interface, forming a Ge-rich layer. (2) There is no loss of Ge on oxidation. (3) The oxidation rate of SiGe in a dry oxygen environment is essentially the same as that of pure Si. For wet oxidation, the rate for SiGe in the linear regime is 2 to 3 times higher than the rate of pure Si: but it is almost the same in the parabolic regime.

1.2.1 Oxidation mechanism of SiGe

The catalytic effect of Ge on the oxidation of Si had been observed before by Fathy, Holland, and White in Ge implanted Si [7]. In this case, enough Ge on the oxidation of Si had to be snow-plowed in order for oxidation enhancement to be observed. They proposed that breaking of the weaker Si-Ge bound as compared with Si-Si explain the rate enhancement. This may only be the last event, not necessarily controlling.

For example, represents a steady-state situation in which Si-Si bonds must still be broken below the Ge-enriched layer to supply the needed Si flux to the interface to maintain the high oxidation rates. Attention should be focused on the growth interface and interactions there since the Ge effect is found only in the initial and linear regime of oxidation.

There are several indications that generation of interstitials at the reaction interface and subsequent diffusion is not occurring during the SiGe oxidation. The high enrichment content at the interface would imply that Ge interstitials should be generated as a stress relief mechanism in preference to Si interstitials which are being rapidly depleted through oxidation; interstitials would tend to cause intermixing, diffusion of Ge into the bulk, and formation of extrinsic dislocation loops. That removal of Si from the substrate by oxidation creates a vacancy excess which not only helps compensate the stress but on diffusion onward can also account for the rapid diffusion of Si to the interface through the Ge-rich region. The excess vacancies may help to enhance the oxidation but in the process would lead to a less dense interfacial oxide and high levels of interface state. The vacancy flux would also explain the formation of voids at the original Si/SiGe interface where diffusivity is reduced discontinuously and accumulation occurs leading to condensation.

1.2.2 Oxidation behavior of SiGe

Study the oxidation of SiGe alloys compositions (25, 50 and 75 at % Ge) (Figure 1-1). All of the oxidations were performed at 900℃ in wet atmosphere on 7500Å films grown by molecular beam epitaxy (MBE). At

low Ge concentrations [8-10], the rate of oxidation is enhanced by the presence of Ge and enough Si can be provided to the interface, resulting in fast initial oxidation and the formation of pure SiO_2. In alloys containing 50 and 75 at.% Ge, the rate of diffusion of Si to the oxide/alloy interface is sufficiently slow with respect to the rate of oxidation that it rapidly becomes impossible to grow pure SiO_2. Thus, the initial oxide formed is a mixed (Si, Ge)O_2 oxide. Eventually, the activity of oxygen at the interface decreases because of the thickness of the oxide, resulting in a slow down of the oxidation rate. This makes it possible for Si to diffuse to the interface as fast as is required to form pure SiO_2.

For SiGe with Ge concentration below 50%, Si was preferentially oxidized and only one Ge-rich layer was formed at the oxide/substrate interface. On the other hand, for SiGe with Ge concentration above 50%, two Ge-rich layers were formed after oxidation with one at the oxide/ substrate interface and the other at the oxide surface.

1.2.3 Conservation of total amount of Ge in SiGe layer during oxidation

There are two groups, A and B, by their initial SGOI thickness Ti. The samples were oxidized in dry oxygen gas at 1050℃. The thickness of each layer was measured by sp1`ectroscopic ellipsometry and transmission electron microscopy (TEM). The thickness values obtained using these two methods were consistent within the accuracy of a few %. The Ge fraction in the SGOI layer was analyzed by Rutherford backscattering spectroscopy (RBS), sputtering Auger electron

spectroscopy (AES) and energy dispersive X-ray spectroscopy (EDS). Secondary ion mass spectroscopy (SIMS) was used to evaluate the Ge concentration in the oxide layers.

In Figure 1-2 the total amount of Ge atoms in the SGOI normalized by the value before oxidation is plotted as a function of oxidation time. It is found that the amount is kept constant during oxidation. This result enables an estimation of the final Ge fraction x_f based on the simple relationship $x_f = x_i\ (T_i/T_f\ )$. Here, x_i, T_i and T_f are the initial Ge fraction, and the initial and final SGOI thicknesses, respectively. The conservation of Ge atoms in the SGOI layers and the low Ge concentration in the oxide layer indicate that the SiGe oxide layer rejected the Ge atoms which remained in the SGOI layer. This result suggests that the oxidation temperature of 1050℃ is considerably higher than the crossover temperature proposed by Kilpatrick and Jaccodine [11].

1.2.4 Process ambient of SiGe

The rates of oxidation of SiGe compared with rates of oxidation for pure Si, both in the wet and dry ambient. It is shown that the presence of Ge at the SiO_2/Si interface increases the rate of wet oxidation by a factor of about 2.5, while it does not affect the rate of dry oxidation (Figure 1-3). By decreasing the partial pressure of H_2O sufficiently, the rate of wet oxidation can be decreased to match that of dry oxidation. In this case again, Ge has no effect on the rate, contrary to what has been proposed before, Ge is being piled up at the interface both for fast and slow oxidation. The role of Ge is to suppress the formation of Si interstitials

and that this is the rate limiting step in cases of rapid oxidation. For slower oxidation, interstitials have considerably more time to diffuse away and thus their formation and diffusion is not rate limiting.

1.3 Fabrication of nanowire

Semiconductor nanowire have been explored for use as building blocks to construct various electronic and optical devices, including logic gates [12], address decoders [13], memory components [14], light emitting diodes [15], photodetectors [16], lasers [17], and chemical sensors [18]. There are various methods for fabricating patterned nanowires. The methods to fabricate nanowire are (1) lithography with photons in UV, DUV, EUV and X-ray spectrum; (2) machining using AFM, STM, NSOM; (3) replication against masters (or molds) via physical contact printing, molding and embossing; (4) self- assembly by using surfactant systems, block copolymers, crystallization of proteins and colloids; (5) spacer formation.

1.3.1 Photo lithography

In photon and particle-based lithography, by using nonlinear resists, near-field phase shifting or topographically directed technology, it has been possible to achieve sub-50nm feature. For example, EBL has demonstrated the ability to achieve 20nm width nanowires with 60nm height. Height is often limited by the lift-off process. Extreme ultraviolet light (EUV) lithography has generated 38nm patterns [19].

1.3.2 Fabrication by AFM, STM, NSOM

In 1990, J. A . Dagata *et al*. proposed the tip-induced anodic surface

oxidation by using scanning probe lithography (SPL) (Figure 1-3) to define nano- patterns on the semiconductor surface. AFM, STM and NSOM and the like are called SPM. Its operation mechanism is in an environment humidity control when approximately 50%, the sample surface attaches a water thin film, when the probe contacts this water thin film, take the probe as negative electrode, the sample surface is the positive electrode, gives a negative bias to probe, the water molecule can start to ionization, and produces the partial region oxide compound with the probe under- neath sample surface. The probe produces the electric field can along with the distance of sample surface to attenuation, the oxidation stops immediately when the electric-field intensity is smaller than 10^9 V/m [20]. The oxide compound growth speed with executes gives the probe bias to have the enormous relations. In process by way of program configure, but fine holds controls scans the probe the displacement, carries on oxide compound of the specific line to grow, then achieves the micro region design forming the goal, this is scanning probe lithography technique to apply to the lithography at the beginning of shape.

1.3.3 Micro imprinting

In microcontact printing, micromolding [21], embossing and nano-imprinting techniques (Figure 1-4) [22], issues limited by van der Waals forces , speed of capillary filling and adhesion of mold and replica are overcome by using low-viscosity solutions and surface modification. Step and flash technology has demonstrated the ability to imprint sub-20nm features [23]. Although such methods may translate the serial

method of EBL/EUV into a parallel patterning process, the mold formation still depends on EBL/EUV and its use restricted by the high cost of molds.

1.3.4 Self- assembly nanowire

Germanium is an important semiconducting electronic material with high carrier mobility and a band gap of approximately 0.6 eV. Nanowires of germanium were first reported by the group of Heath about ten years ago, synthesized by using a solvothermal approach [24]. Recently, laser ablation (820℃) [25], vapor transport (900-1100℃) [26], and solvothermal methods (300-400℃, 100 atm) were used for growth. Those high quality Ge nanowires are synthesized by a simple CVD process at 275℃ under atmospheric pressure. This represents the mildest growth conditions for single-crystal nanowire synthesis. An efficient Ge feedstock from GeH_4 and the low eutectic temperature of Ge-Au nanoclusters are the key factors that afford vapor-liquid-solid (VLS) growth of Ge nanowires at low temperatures. (Figure 1-5) Dunwei Wang *et al.* carried out CVD growth at 275℃ under a 10 sccm (standard cubic centimeter) flow of GeH_4 (10% in He) in tandem with a 100 sccm flow of H_2 in a 2.5 cm furnace reactor (total gas pressure 1 atm) for 15 min. The SiO_2 substrate used in this work contained preformed Au nano-crystals (approximately 20 nm in diameter) deposited uniformly on the surface from a colloidal solution.

1.3.5 Spacer formation

Controlled deposition and size reduction, which involves deposition

on cleaved edges, or oxidation, followed by anisotropic etching forming spacers. (Figure 1-6) This process provides a density increase as well as size reduction. It can be used to pattern silicon fins for double-gate MOSFETs [27].

Chapter 2

Device Fabrication

First, the test samples were oxidized at various oxidation conditions before the nanowire structure got oxidized. And spacer was utilized to fabricate the SiGe nanowires. Our process involves defining the active area (AA) by etching an island by conventional G-line lithography, followed by deposition of SiGe layer. Later, the conformal SiGe layer was etching back to the edge of the island by dry etching. The thickness of the island determines the height and the width of the nanowires.

General Fabrication Process

2.1 Wafer preparation

All experiments were performed with p-type 6-inch (100)-oriented silicon wafer. The resistivity of the silicon substrate is around 1~10 ohm-cm. Samples were prepared by the following process:

2.2 Define Active Area Regions

2.2.1 Standard RCA Clean and 1100℃ wet oxidation was performed. The thickness of the oxide is about 3000Å

2.2.2 Define AA region with Mask 1. (Figure 2-1)

G-line lithography was used and then dry etching by TE5000 R.I.E system was employed. A height step was created to form a SiGe spacer at the next process.

2.3 **Define desired spacer**

2.3.1 Deposition 150Å α-Si layer on oxide before SiGe layer deposition.

Adhesion between SiGe film and SiO_2 layer was then improved.

2.3.2 Deposition SiGe layer by UHVCVD 550℃ 600s.

The thickness of the SiGe layer is about 500Å. (Figure 2-2)

2.3.3 Define S/D region with Mask 2. (Figure 2-3)

The S/D and channel region were patterned.

2.3.4 Dry etching process.

SiGe was etched by TCP 9400SE Poly-silicon Etcher and 10% over etch was performed.

2.3.5 Etching over two side spacer with Mask 3. (Figure 2-4)

Isolation of the loop structure.

2.4 Oxidation in various process conditions

Different oxidation temperature and time

2.5 Ion implantation for S/D with Mask 4

10 K ev of acceleration voltage, B^+ 5 x 10^{15} ions/cm^2

2.6 Define bottom gate via with Mask 5 (Figure 2-5)

Etching via by BOE

2.7 Contact formation (Figure 2-6)

2.7.1 Coating Aluminum with Thermal Coater

2.7.2 Define Contact Pad with Mask 6

2.7.3 Al sintering at 450℃ in N_2 ambient for 30 minutes

Nanowires with two different sizes were fabricated. Wires in group 1 was formed by spacer, and wires in group 2 (test sample) was made through lithography.

The detailed fabrication process flow of group 2 are listed as follows (Figure 2-7).

1. (100) orientation Si wafer
2. Initial cleaning
3. Thermal wet oxidation at 1100℃ to grow 300nm thermal SiO_2 in horizontal furnace.
4. 150 Å α-Si was deposited by LPCVD with SiH_4 gas
5. 500 Å SiGe was deposited by UHVCVD at 550℃ with SiH_4 and GeH_4 gas
6. Oxidation in various temperature and time
7. Mask#1：Define S/D and channel
8. 500 Å SiGe + 150 Å α-Si wet etching by poly etching solution
9. RCA cleaning
10. 100nm gate dielectric deposition by PECVD at 300℃
11. 200nm poly-Si was deposited by LPCVD at 620℃ with SiH_4 gas
12. Mask#2：Define gate regions
13. Poly-Si wet etching by poly etching solution, gate oxide wet etching by BOE
14. Ion implantation：B, 10 K ev, 5 x 10^{15} ions/cm^2

15. Dopant activation in N2 ambient at 950℃ for 30 min in furnace
16. 300nm oxide was deposited by PECVD as passivation layer
17. Mask#3：contact holes formed
18. 500nm Al thermal evaporation
19. Mask#4：Al pattern defined
20. Etching Al and removing photoresist
21. Al sintering at 450℃ in N_2 ambient for 30 minutes

The electrical properties of SiGe nanowire were measured with the contact pad served as source and drain, and substrate served as gate.

Chapter 3

Results and Discussions

We have successfully fabricated SiGe nanowire on silicon wafer, and the electrical characteristics of the nanowire were measured. In this chapter, SiGe test structure was fabricated and measured first and then SiGe nanowire structure followed. We make discussion on some key points in nanowire device fabrication and also on the measured electrical properties. We used *HITACHI S-4000–FESEM* to observe the nanowires and measure the size of them, and the I-V characteristics were measured by *HP4156 semiconductor parameter analyzer.*

3.1 Electrical property of SiGe films

3.1.1 Influence of Oxidation Time on Electrical Properties

Figure 3-1 shows I_D-V_G characteristics of four different devices: un-oxidized, oxidation for 4 minutes, oxidation for 16 minutes, and oxidation for 36 minutes, respectively. $Si_{0.93}Ge_{0.07}$ film was used in this experiment. All of the oxidized devices were oxidized at 1000℃ minutes in dry ambient. The trend of the curves indicates that longer oxidation time would result in higher on current. Besides, after calculation, the On/Off ratios are 3.3, 1.6, 1.5 times higher than un-oxidized device for 36 min 16 min 4 min, respectively. In the longer oxidation time devices, more amount of Si was oxidized and achieves higher Ge concentration. Same trend would be found in the I-V characteristics diagram.

Figure 3-2 represents I_D-V_D characteristics from different oxidation time devices. As predicted, 36 min-oxidized device has best on current, which is 5.08μA at V_D = -8V. For the other devices, they are 1.52μA, 0.75μA, and 0.61μA for 16 min-oxidized, 4 min-oxidized, and un-oxidized device, respectively.

It is supposed that if Si in SiGe layer is fully oxidized, the performance of the SiGe-based p-MOSFET would always be improved since the positive correlation between the amount of oxidized Si and the mobility of SiGe channel.

3.1.2 Influence of Oxidation time for SiGe films

Figure 3-3 shows I_D-V_G characteristics of three different devices: un-oxidized, oxidation at 950℃, and oxidation at 1000℃ at V_D = -5 V. $Si_{0.89}Ge_{0.11}$ film was used. Both of the oxidized devices were oxidized for 16 minutes in dry ambient. It can be seen that oxidized devices shows better electrical performance than the un-oxidized one, and the device of 1000℃ shows even higher on current than the one of 950℃ while the both devices have roughly the same off current.

Figure 3-4 shows I_D-V_D characteristics which are consistent with the prediction：The device oxidized at 1000℃ has highest I_D of the three devices. For the other devices, they are 2.58μA, 1.83μA, and 0.40μA at V_D = -6V for 1000℃ oxidized, 950℃ oxidized and the un-oxidized, respectively.

According to above three diagrams, it is known that since SiGe got oxidized, Ge concentration got enhanced, and then mobility also increases which resulted in higher transconductance and on current. As the improvement of on current is higher than the increasing of off current, On/Off ratio then gets improved. With higher oxidation temperature, the oxidation rate would be higher, which makes more Si in SiGe layer got oxidized. Then the mobility would be even higher, and better performance is achieved.

3.2 $Si_{0.89}Ge_{0.11}$ Nanowire shows the same behavior as test SiGe films

Figure 3-5 and Figure 3-6 show the I_D-V_D characteristics of $Si_{0.89}Ge_{0.11}$ nanowire. In Figure 3-5, the nanowire was not oxidized, and the gate length L = 6μm. In Figure 3-6, the nanowire was oxidized at 1000℃ 4min, the gate length L = 13μm. Clearly, higher current was obtained at negative gate voltages, demonstrating that the SiGe nanowire is a p-type semiconductor. The figure of I_D-V_D characteristics is somewhat nonlinear, which indicates non-ideal contact between the electrodes and nanowire. But as we know, there are still some reasons which affect the drive current including the diameter of the nanowire, wire length, the dopant condition, heat treatment, and the electrode contact, etc. So, if we want to compare the two structures, we should normalize them.

The equation about current I is

$$V = I \cdot R = I \cdot \rho \cdot \frac{L}{A}$$, ρ is the resistivity.

We fix the voltage at V_D = 5V and V_G = -10V to be constant. Rewrite the equation, the σ is

$$\rho = A \big/ (I \cdot L) \quad \longrightarrow \quad \sigma = (I \cdot L) \big/ A$$

σ is the conductivity (Ampere per unit length) term and this is proportional to the current I and device length L. The area of the nanowire we could observe from the TFSEM. Figure 3-7(a) show the top view SEM picture and Figure 3-7(b) show the cross-section view SEM picture. There was fluctuation in each width and height which was controlled by the TCP dry etcher. The fluctuation must be decreased because the diameter of the nanowire is directly related to the current. So we make the average size of the $Si_{0.89}Ge_{0.11}$ nanowire. Additionally, we define the width of nanowire equal the width at half of height of the nanowire. We can obtain the average of the $Si_{0.89}Ge_{0.11}$ nanowire height is 85 nm and the width is 43 nm, we thought that the nanowire was a triangle column shape, so the average area is about 3655 nm^2. The $Si_{0.89}Ge_{0.11}$ nanowire at V_D=3V and V_G=-10V, by calculation, the $Si_{0.89}Ge_{0.11}$ nanowire current per unit length (conductivity) is σ = 10.65 A/cm for L = 6μm. For the oxidized the nanowire in figure 3-8, show the cross-section view. It is during 1000℃ oxidation and etching oxide by buffer oxide solution (BOE). It is found that the size of SiGe nanowire after oxidation is smaller than which is un-oxidized, due to what was already described above: Si atoms in the SiGe film was oxidized to form SiO_2, and was then removed by BOE solution. The height and the width of the nanowire cannot be measured precisely because of the resolution of

SEM, but the cross-section area of the oxidized nanowire is undoubtedly smaller than un-oxidized nanowire 3655 nm^2. Besides, as described in the previous section, Ge content in SiGe film would get increased after oxidation, it can be known that the Ge content in SiGe nanowire would also be higher than un-oxidized nanowire. From the above statements, it can be concluded that the conductivity of oxidized nanowire would be higher than un-oxidized nanowire.

3.3 $Si_{0.89}Ge_{0.11}$ nanowire compare with Poly-Si nanowire

The SEM picture of Poly-Si nanowire fabricated by spacer process is shown in figure 3-9, and the I-V characteristics were compared with $Si_{0.89}Ge_{0.11}$ nanowire. Figure 3-10 shows I_D-V_D characteristics at different gate bias for Poly-Si nanowire with L = 8μm. As described in the previous section, the size of nanowire makes influence on electrical properties, so normalization of wire cross-sectional area, wire length, and bias voltage were made to achieve more accurate results. Data of SiGe nanowire before oxidation, SiGe nanowire after oxidation, and Poly-Si nanowire were listed in table 3-1. From this table, it is found that the conductivity of un-oxidized SiGe nanowire is higher than that of poly-Si nanowire, while the oxidized SiGe nanowire shows even higher conductivity.

Chapter 4

Conclusions

In our thesis, SiGe nanowire was successfully fabricated on silicon wafer with conventional lithography process. The electrical properties were measured by HP4156A and the structures of the SiGe nanowire on the sidewall spacer were observed by SEM. By our experiment of SiGe-based p-MOSFETs test structure, it is found that the devices of higher oxidation temperature and longer oxidation have more improvement in electrical properties. From the ID-VD characteristics, the same oxidation conditions were also performed for the SiGe nanowire and the same trench were achieved

Chapter 5

Future work

According to the literature nowadays, less research was done of the mechanism of SiGe. Oxidation temperature, oxidation time, interface reaction, and the content variation of Ge must be considered during the oxidation process. The influence of the thickness of SiGe film on the electrical characteristics is another way of researching. Whether the diffusion of Ge atoms makes higher concentration of GeO_2 is also worth studying in the future.

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	Length	Current (A)	Area	Conductivity
Poly nanowire	8 μ m	5.68 x 10-^{7}	13839 nm^{2}	1.095 A/V·cm
SiGe nanowire	6 μ m	3.99 x 10^{-7}	3655 nm^{2}	10.65 A/V·cm
S/D/Channel implant	10 μ m	9.72 x 10^{-6}	3655 nm^{2}	88.65 A/V·cm
After oxidation	13 μ m	8.99 x 10^{-7}	< 3655 nm^{2}	---

Table 3-1 Conductivity σ = I · L /(V · A) ; Unit : **A/(V·cm)**

at VD = 3V and VG = -10

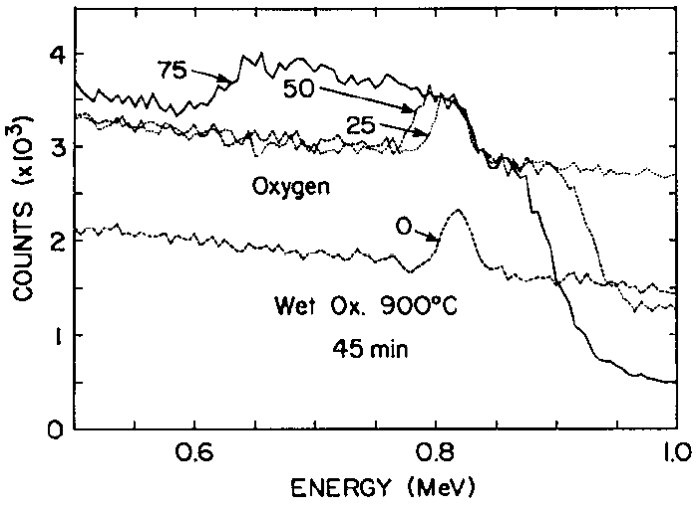


Figure 1-1. Oxygen peaks of backscattering spectra for pure Si and samples containing, respectively, 25, 50, and 75 at.% Ge, after 45 min oxidation at 900 “C.

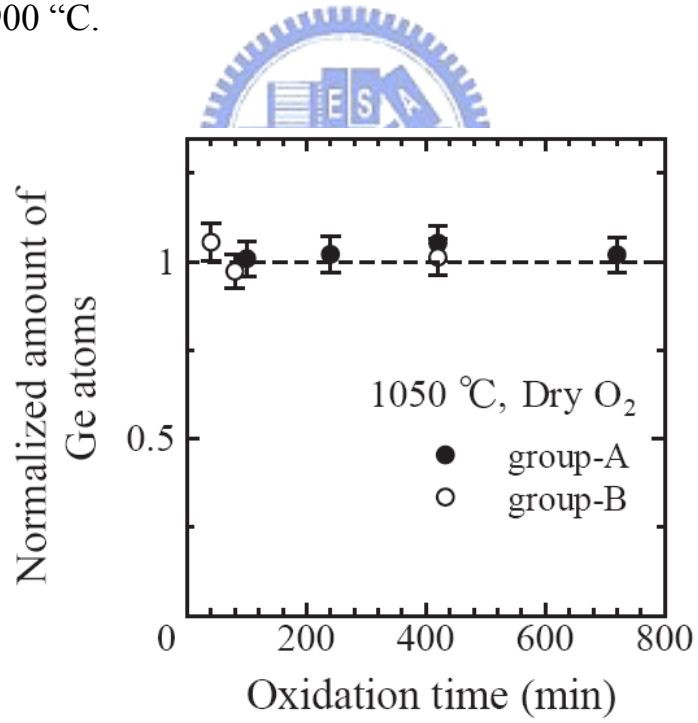


Figure 1-2. The total amounts of Ge atoms after oxidation normalized by those before the oxidation as a function of oxidation time for the SGOI layers with initial thicknesses of 70 ± 10 nm (○) and 320 nm (●)

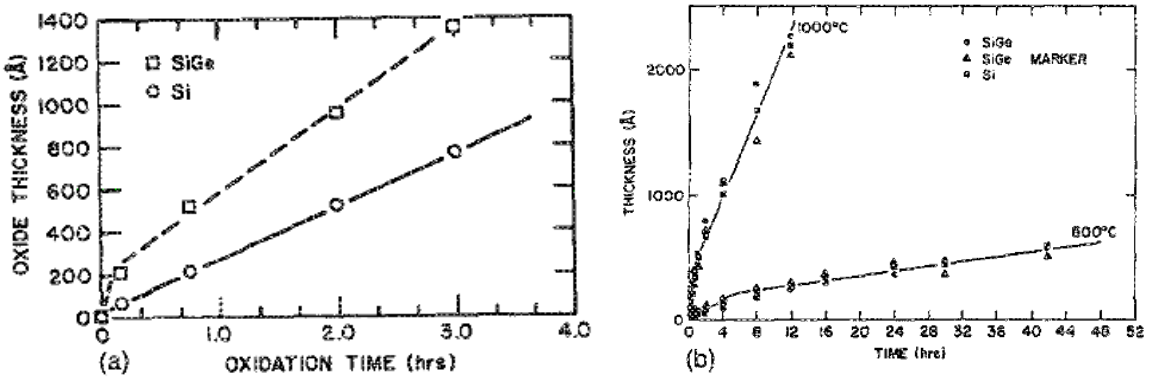


Figure 1-3. Rate of oxidation of Si and SiGe; (a) wet oxidation, 800℃; (b) dry oxidation, 800 and 1000℃.

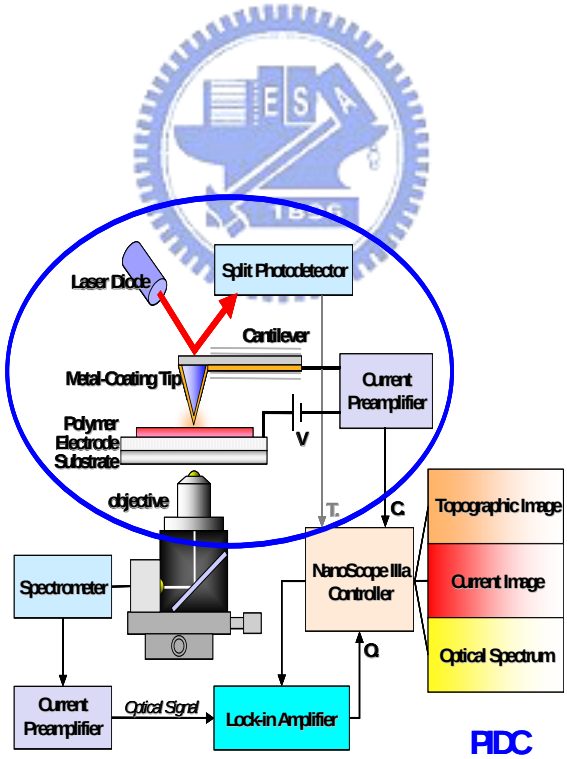


Figure 1-4. Schema of Scanning Probe Lithography (SPL).

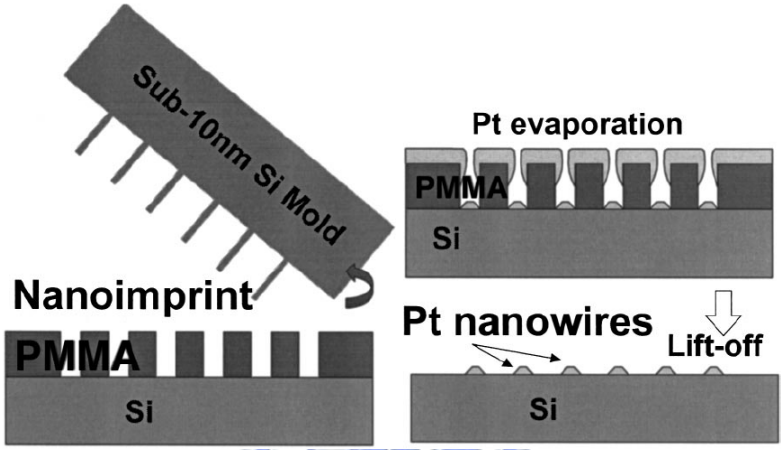
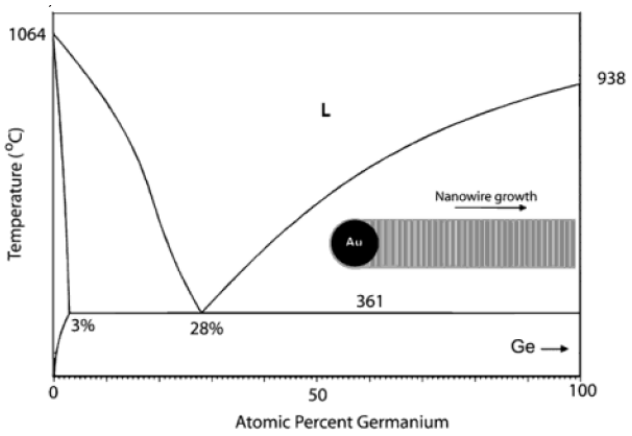


Figure 1-5. Schematic process flow of nanoimprint (a) After nanoimprint and removal of residual PMMA by O_2 plasma (b) Pt evaporation and lift-off.

(a)



(b)

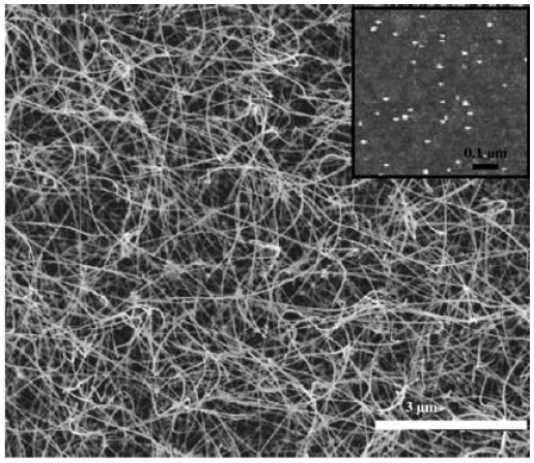


Figure 1-6. (a) Binary Phase Diagram for the Au:Ge. (b) An SEM image of Ge nanowires synthesized by CVD at 275℃ on a SiO_2/Si substrate. The inset shows an AFM image of Au nanoclusters on the substrate recorded prior to CVD.

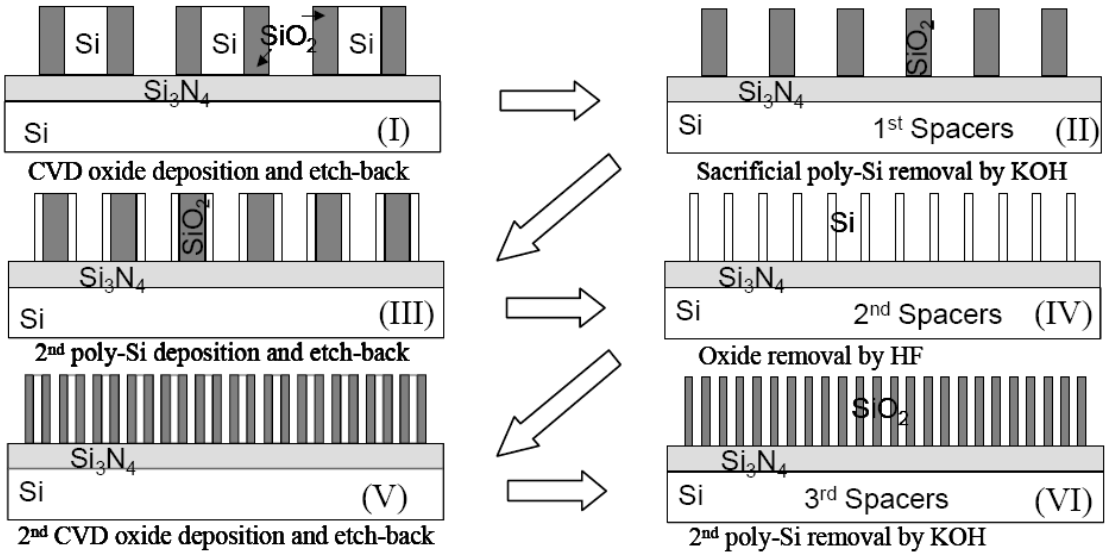


Figure 1-7 Schematic view of iterative spacer lithography (ISL).

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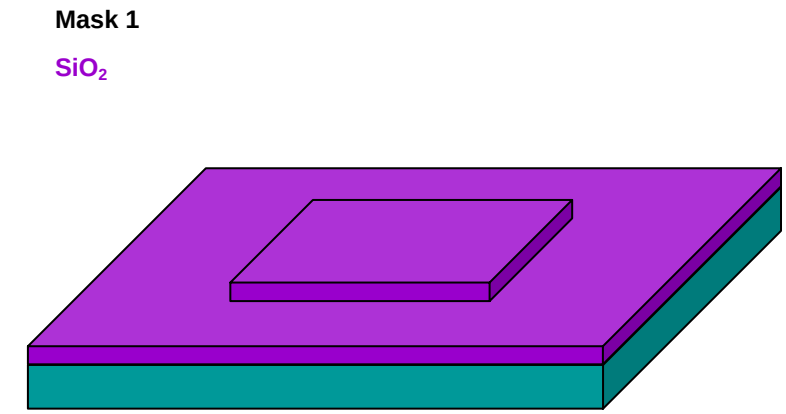


Figure 2-1. Define AA region.

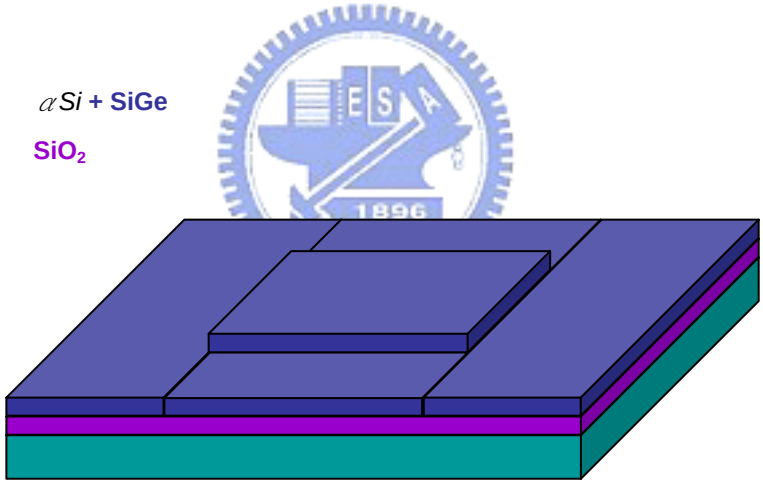


Figure 2-2. Deposition α-Si + SiGe.

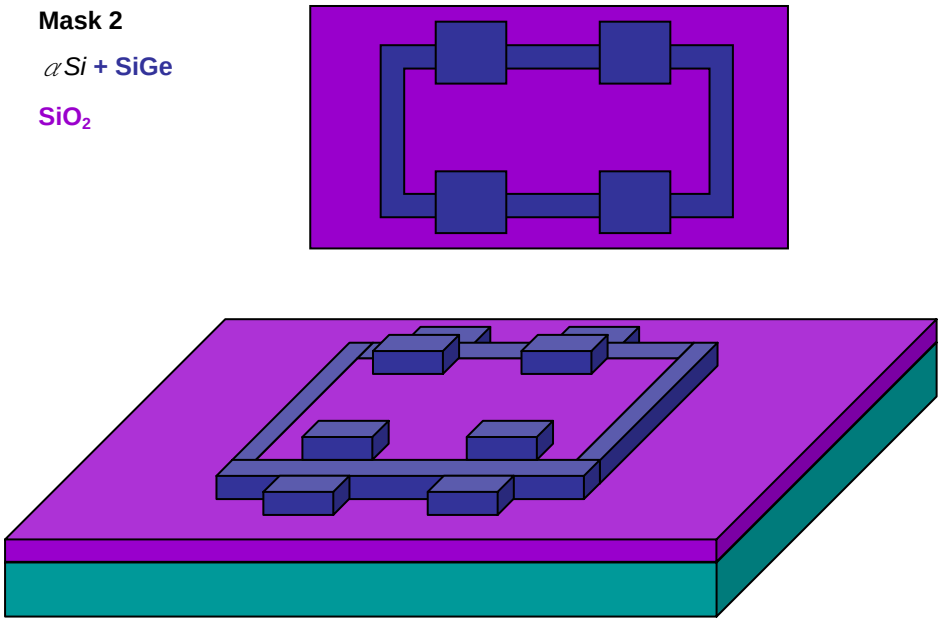


Figure 2-3. Define S/D region.

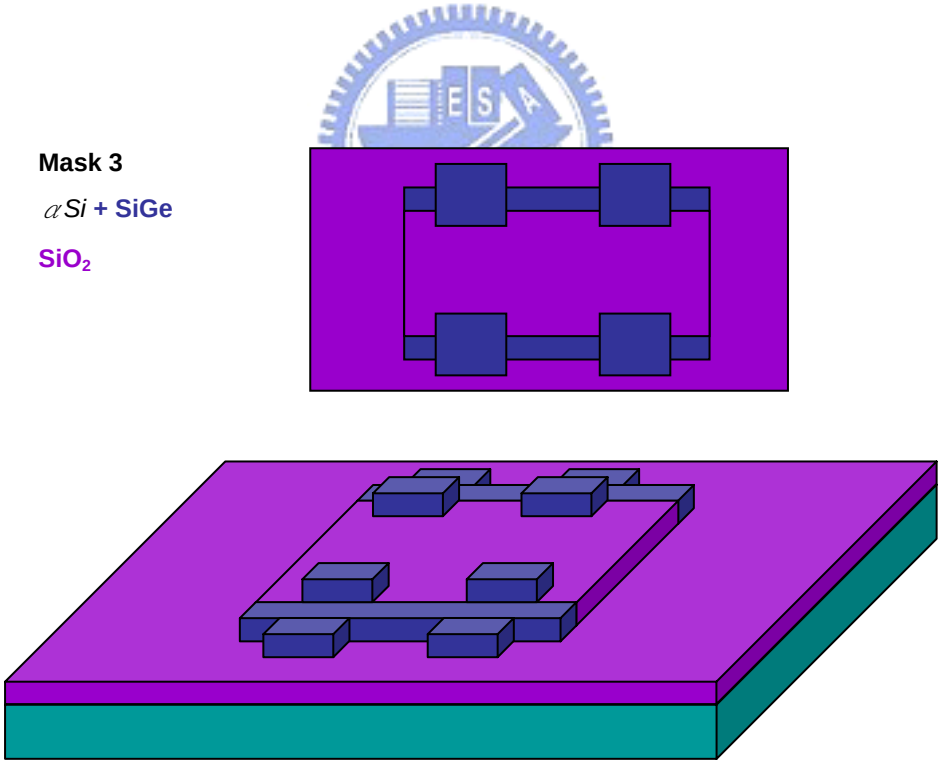


Figure 2-4. Etching over two side spacer.

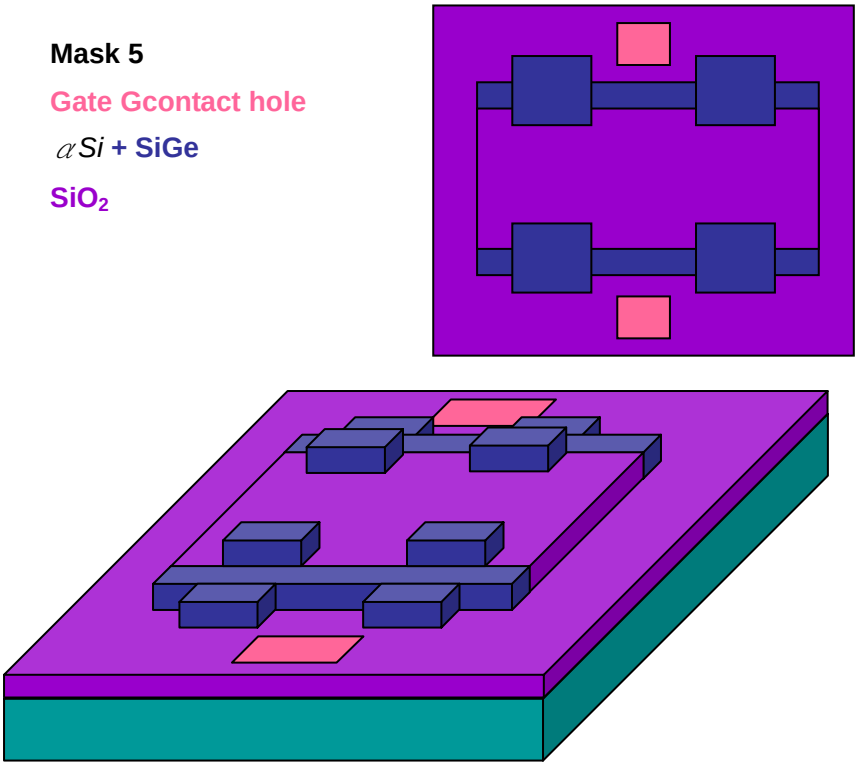


Figure 2-5. Define Bottom gate via.

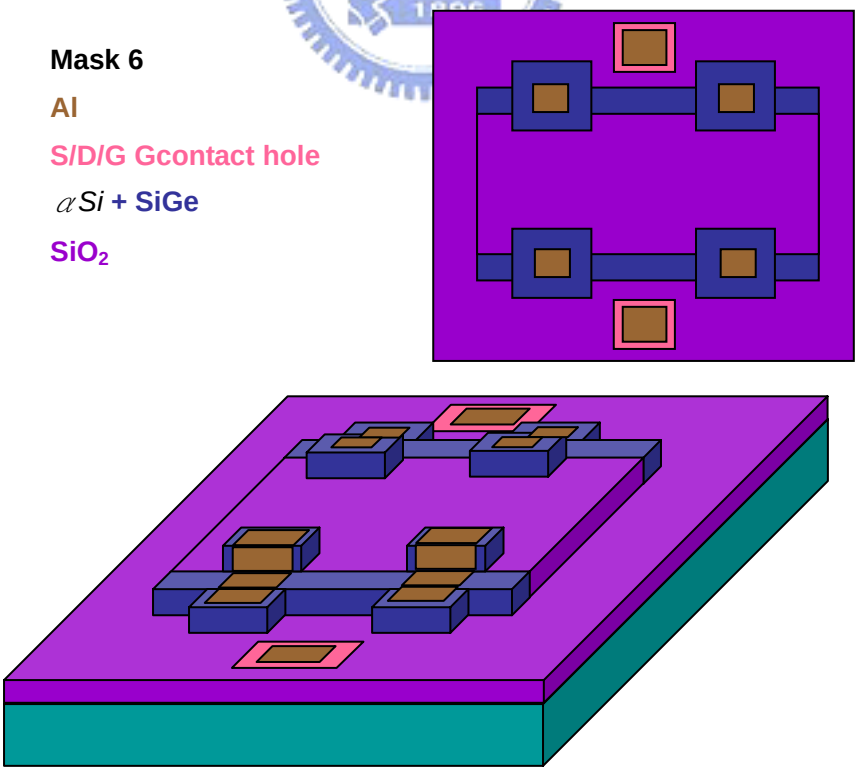


Figure 2-6. Al contact.

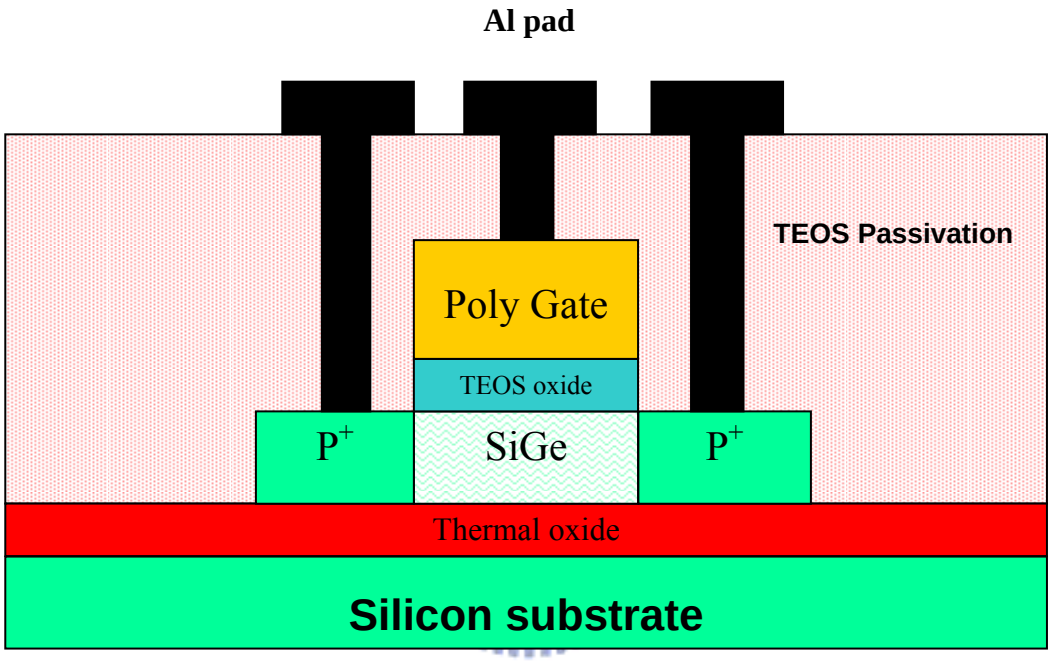


Figure 2-7. The completed test SiGe MOS structure.

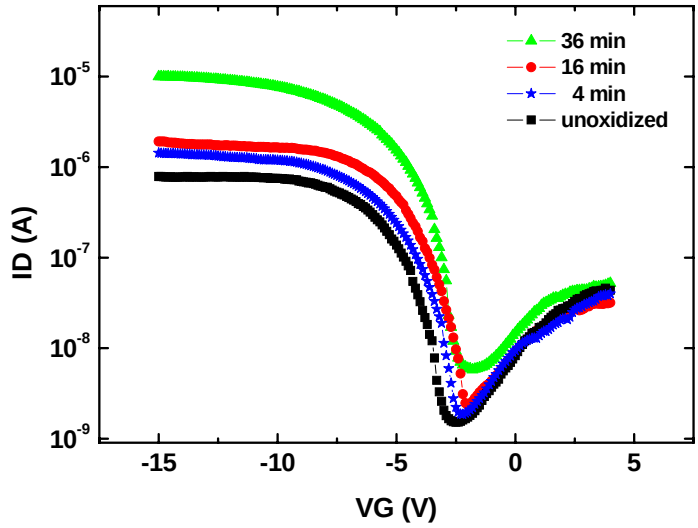


Figure 3-1. I_D-V_G transfer characteristics of different oxidation times of the test structure； W/L = 1 μm/μm at V_D = -5 V.

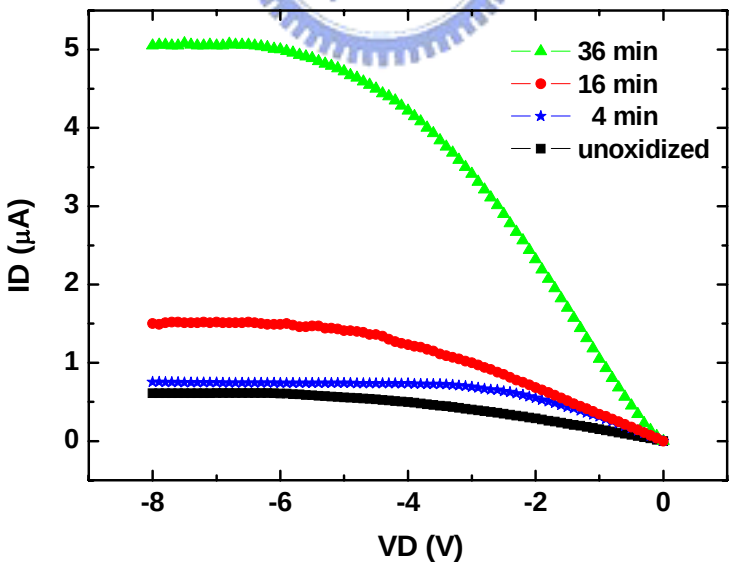


Figure 3-2. I_D-V_D transfer characteristics of different oxidation times of the test structure； W/L = 1 μm/μm at V_G - V_t = 3V.

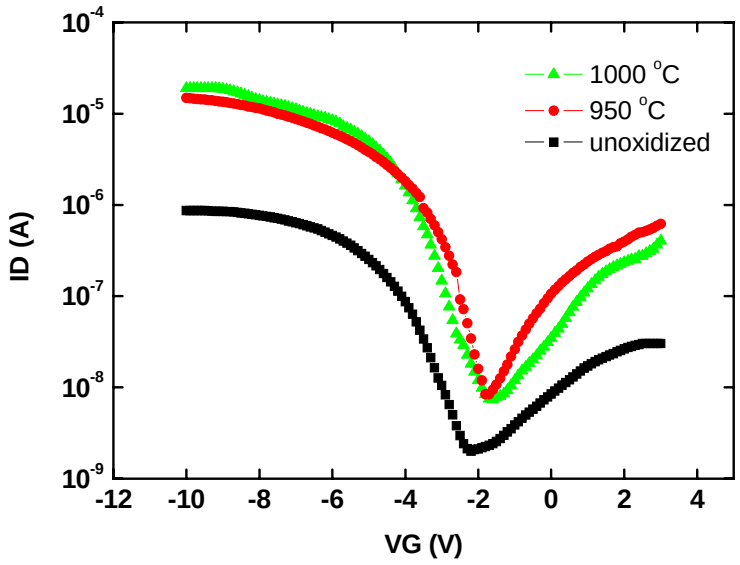


Figure 3-3. I_D-V_G transfer characteristics of different oxidation temperatures of the test structure； W/L = 1 μm/μm at V_D = -5 V.

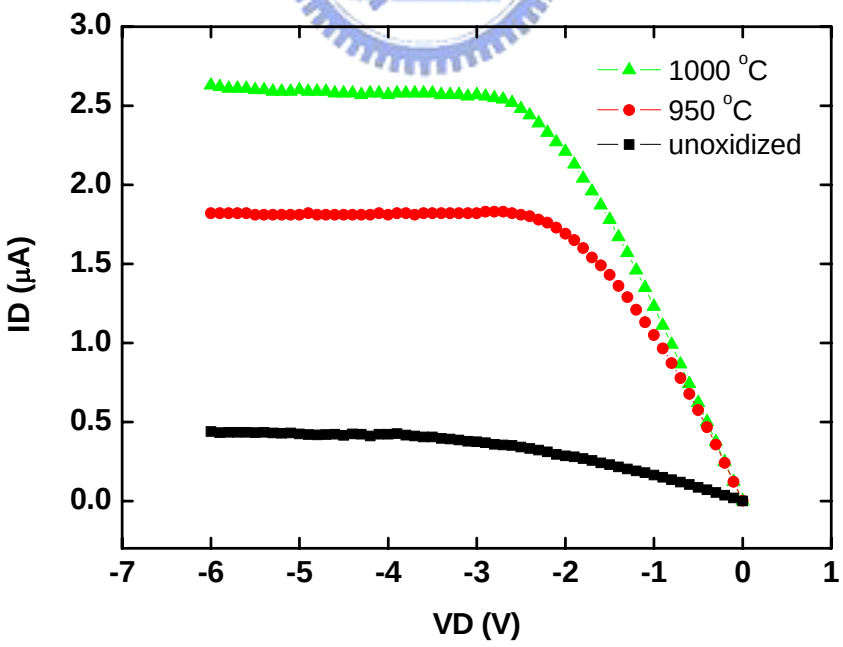


Figure 3-4. I_D-V_D transfer characteristics of different oxidation temperatures of the test structure； W/L = 1 μm/μm at V_G - V_t = 3V.

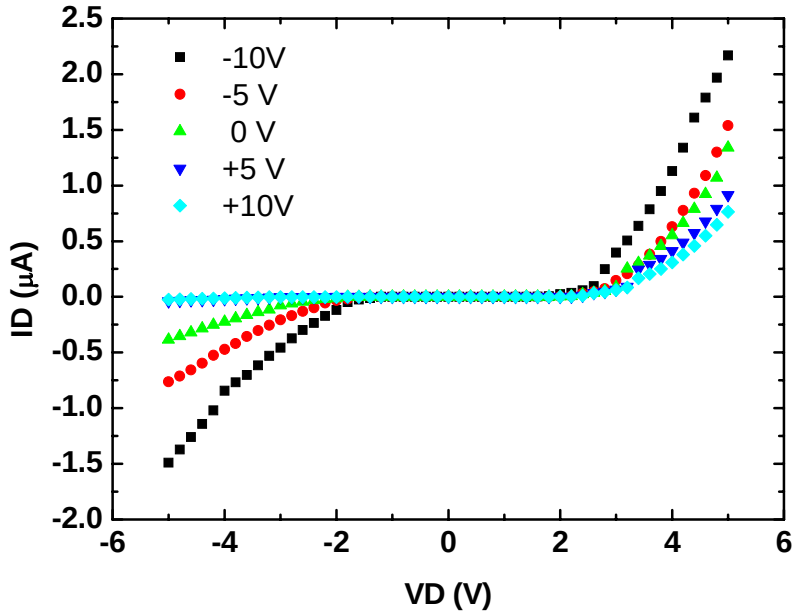


Figure 3-5. SiGe nanowire I_D - V_D characteristics before oxidation.

(L = 6 μm , V_G = -10 ~ 10 V)

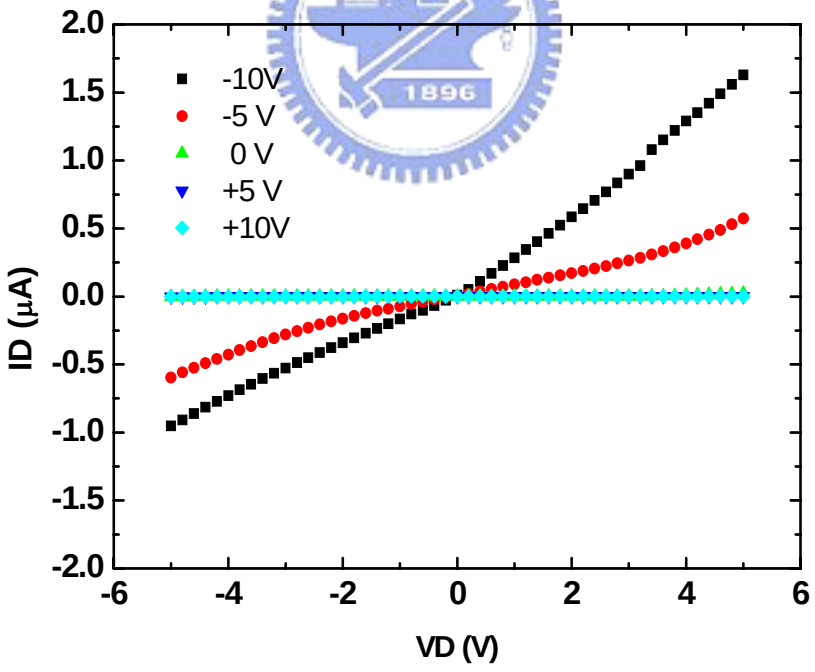
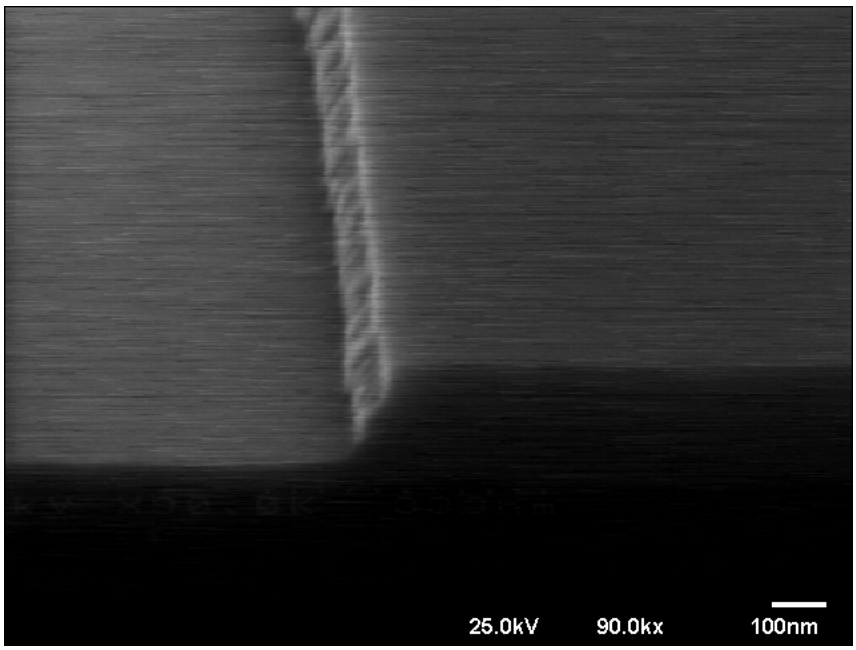
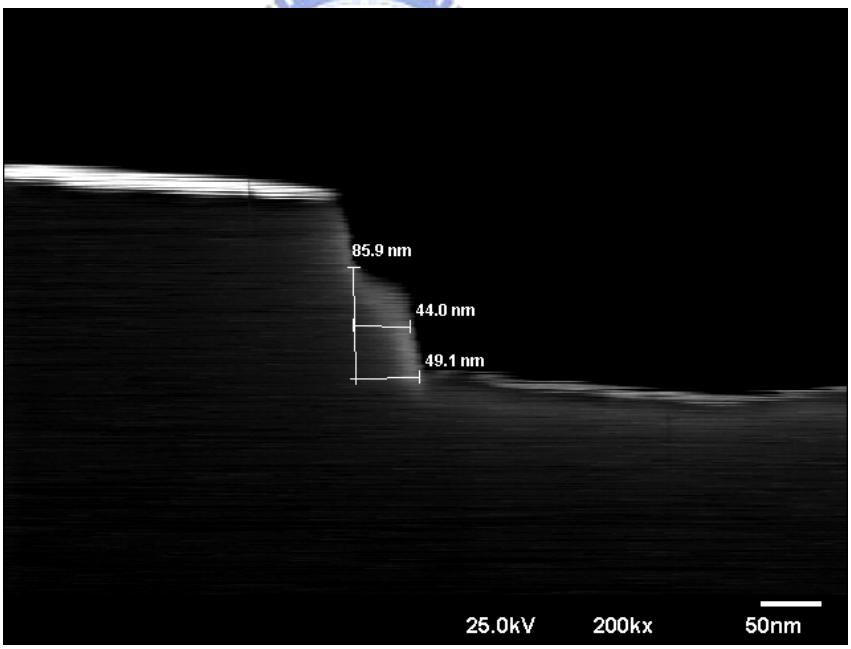


Figure 3-6. SiGe nanowire I_D - V_D characteristics after 1000℃ oxidation.

(L = 13 μm , V_G = -10 ~ 10 V)



(a)



(b)

Figure 3-7. (a), (b) The cross-section view of $Si_{0.89}Ge_{0.11}$ nanowire observed by SEM.

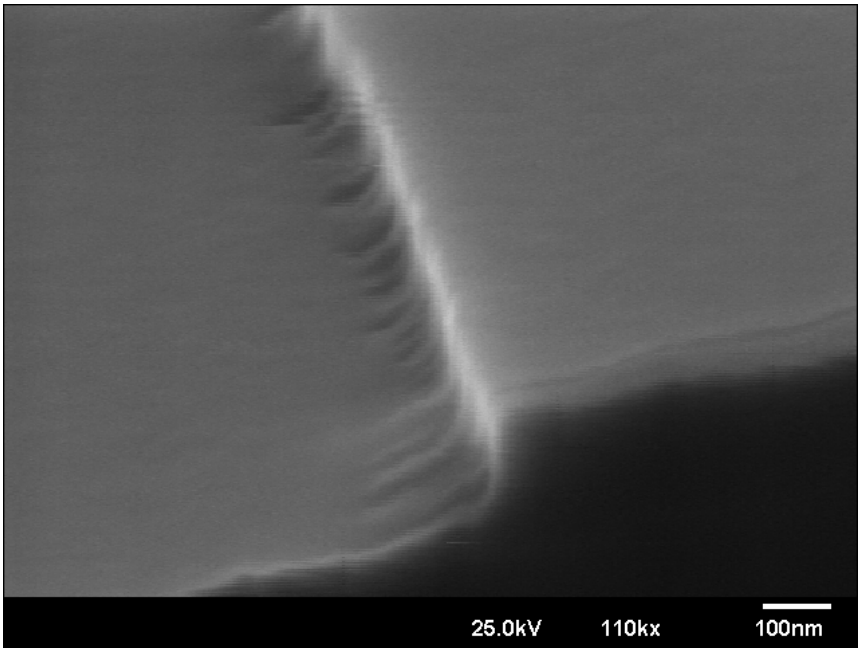


Figure 3-8. The cross-section view of $Si_{0.89}Ge_{0.11}$ nanowire after oxidation observed by SEM.

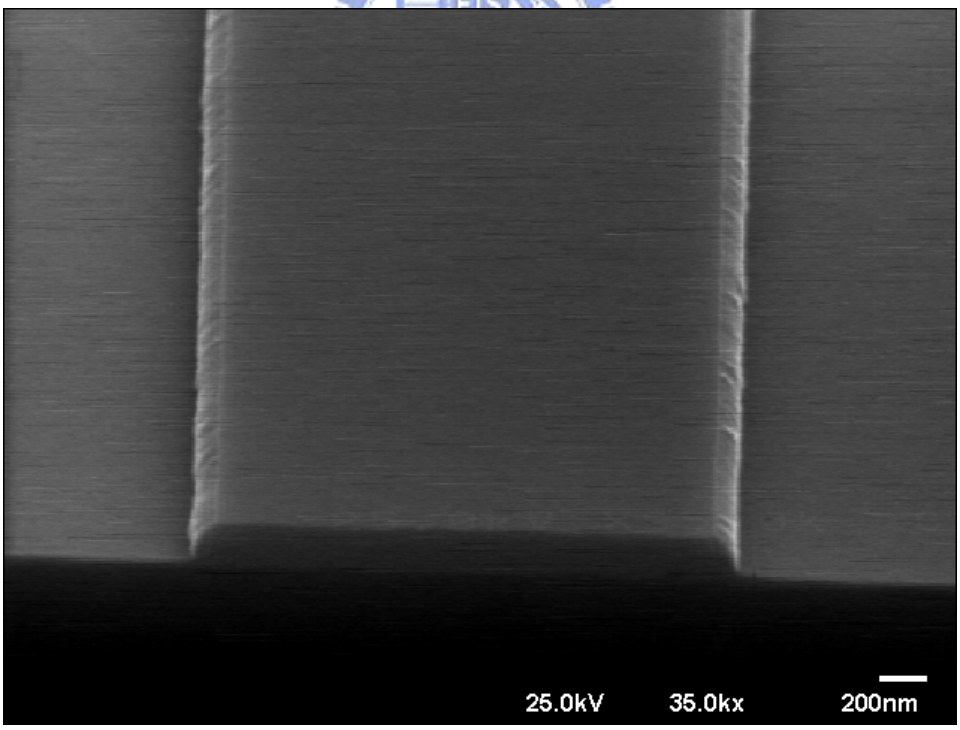


Figure 3-9. The cross-section view SEM picture of Poly-Si nanowire

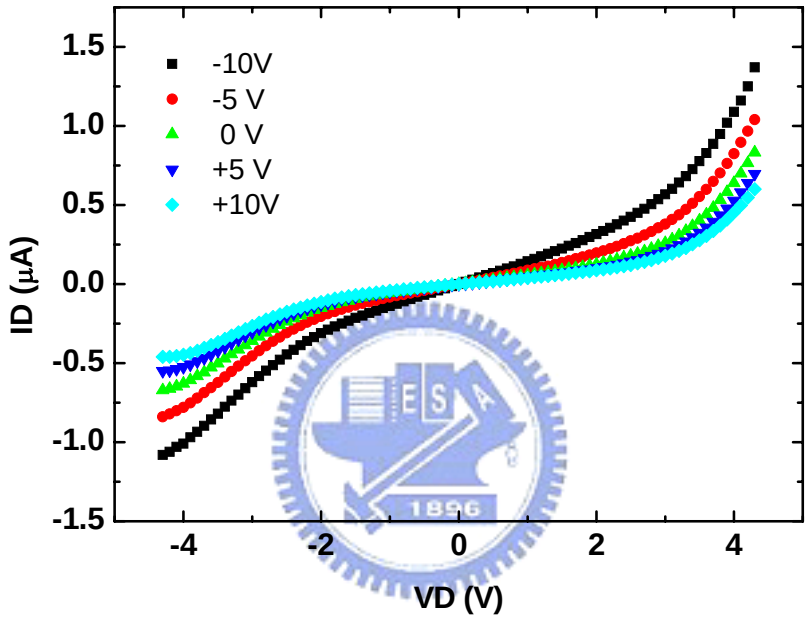


Figure 3-10 Poly-Si nanowire I_D - V_D characteristic

(L = 8 μm , V_G = -10 ~ 10 V)

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碩士論文：矽鍺奈米線在不同製程條件下之電特性研究

A Study of Electrical Properties under Various Process Conditions for SiGe Nanowire