國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

具有氮化矽覆蓋層之形變 N 型金氧半場效電晶體之元件特性與熱載子退化效應

Device Characteristics and Hot Carrier Degradation of Strained NMOSFETs with SiN Capping Layer

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摘要

當互補式金氧半場效電晶體的結構因微縮而達到其極限時，形變通道（strained channel）可用來增進載子的遷移率。已有研究證明，可利用矽與矽鍺之間晶格的不協調，而在矽鍺基板上製造出形變矽元件。雖然雙軸伸張形變矽在近年來被應用為增進載子遷移率的技術，而受到廣泛重視，但此技術被證明有如下缺點，如因在界面上有大量的貫穿差排而使得元件難以製作，以及鍺原子會向外擴散、源極與汲極延伸區的摻雜易快速擴散和其基板的高成本…等等。相形之下，單軸形變卻可用簡單結構上的改變而製作出來，從而避免雙軸形變中複雜的晶圓製作、高成本以及大量缺陷等問題。

近期局部形變元件逐漸成為用來增進載子遷移率的主要技術（如氮化矽覆蓋之元件）。在這篇論文，我們證明在N型金氧半場效電晶體中，氮化矽覆蓋層及其相關沉積製程對元件特性與熱載子退化效應的影響。我們利用低壓化學氣相沉積系統沉積氮化矽覆蓋層 ，來造成元件通道的形變 ，進而增進其載子遷移率。而沉積氮化矽的過程中，多餘的熱預算（thermal budget）與形變效應會使臨界電壓下滑（threshold voltage roll-off）更加惡化。除此之外，氮化矽的覆蓋也會使熱載子退化效應更嚴重。

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Abstract

As the scaling of CMOS structure reaches its fundamental limits, the carrier mobility enhancement has been intensively pursued by introducing strain in the channel region. This has been demonstrated in strained Si devices on SiGe substrates by taking advantage of the lattice mismatch between Si and SiGe. Although biaxial tensile strained silicon has received considerable attention in the last decade as a technique for mobility enhancement, it has been proven to be difficult to implement because of misfit and threading dislocations, Ge up-diffusion, fast diffusion of S/D extensions, and high cost. In contrast, uniaxial strain can be more easily implemented by simple structure modification, thus avoiding the complex wafer fabrication, high cost, and defects of biaxial strain.

Recently locally strained devices have emerged as the main technique for carrier mobility enhancement (e.g., SiN-capped devices). In this thesis, we investigated the impact of silicon nitride (SiN) capping layer and the associated deposition process on

the device characteristics and hot-electron degradation of NMOSFETs. The SiN layer used to induce channel strain for mobility enhancement was deposited by low-pressure chemical vapor deposition (LPCVD). The deposition of the SiN would aggravate threshold voltage roll-off due to additional thermal budget and the strain effect. Besides, the device hot-electron degradation is aggravated by the SiN-capping.

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謝 雨 霖

誌于風城交大 2006

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Chapter 1
Introduction

1-1 General Background and Motivation

1-1.1 Introduction

With progress made in science and technology, semiconductor industry has made great strides into the nanometer era. It is an inevitable trend to scale the device channel length for increasing the operation speed and density of devices, and for decreasing the operation voltage. Moreover, thinner gate oxide is required to provide sufficient current drive while the supply voltage is scaled down [1, 2].

But there are many pending issues that need to be solved, like short channel effect for scaled devices and higher gate leakage current associated with the use of ultra thin gate oxide. Higher leakage current will result in higher power consumption of devices and degrade the subthreshold swing therefore worsen the switching performance of the devices. When the size of the devices approaches the limit set by fundamental physics, how to further increase the devices' operating speed is also worth studying, in addition to the conventional scaling rules.

1-1.2 Strained-Si device physics

With the scaling of the device size, performance improvement of CMOS devices faces a number of obstacles. It is becoming more and more difficult to maintain high transistor performance because of mobility degradation caused by heavier substrate doping. Mobility enhancement technology is one way to offer dramatic improvements in CMOS devices. In order to realize high-speed performance, it is necessary to increase the carrier mobility for scaled devices with the gate length down to the sub-100-nm and below. Recently, a number of groups have shown that short-channel NMOS devices

incorporating thin strained-Si surface channels can achieve significant drive current enhancement. For examples, MOSFETs with high bi-axial tensile channel stress by growing a Si channel layer on a relaxed SiGe substrate has been demonstrated [3]. Figure 1.1 shows the logic potential solution in International Technology Roadmap for Semiconductors (ITRS)[4, 5]. It indicates that strain-Si technology would be more mature in recent year.

Bi-axial tensile strain can improve both NMOSFET and PMOSFET drive current by altering the band structure of the channel and appears to be promising for CMOS manufacturing. Peak electron mobility enhancements measured in uniformly doped devices saturate near r ~ 1.8 for strained Si with substrate Ge content above 20% (r = μ_{eff}<strained Si> / μ_{eff}<unstrained Si> = mobility enhancement ratio.) [6, 7].

The carrier distribution in energy valley, scattering rate, and effective mass are the most important factors of mobility enhancement for strained-Si devices ($\mu = \frac{q\tau}{m^*}$, where$1/\tau$ is the scattering rate and m^* is the conductivity effective mass). From the viewpoint of electrons, bulk Si has six degenerate conduction band valleys of the same energy, as illustrated in Figure 1.2 [8]. In bi-axially tensile devices, because of the lattice mismatch, the in-plane (x-y plane) and out-of-plane energy valley (z-axis) will be altered by the strain. The strain splits the six-fold degenerate conduction band into a two-fold (Δ2, out-of-plane) and a four-fold (Δ4, in-plane) degenerate band in the energy band diagram (Figure 1.3).

One contributor to the electron mobility enhancement in strained Si is the energy splitting ΔEs between the Δ2 and Δ4 bands, which is proportional to the Ge content x of the relaxed buffer as ΔEs = 0.67x (eV). Because the Δ2 band energy is lower than the Δ4 band energy, the electron will preferentially occupy the Δ2 band. The energy difference (ΔE) between Δ2 and Δ4 sub-bands determines the total population of the

bands. Owing to the smaller effective mass, the Δ2 band can be considered as a high-mobility band as compared with the Δ4 band. As a consequence the electron mobility could be increased. Thus the mobility enhancement will be proportional to the relative electron population of the Δ2 and Δ4 bands in the strained-Si as compared with the bulk Si devices. Another contributor to the electron mobility enhancement in strained Si is that the splitting of conduction band can suppress inter-valley phonon scattering, which can reduce the electron scattering rate ($1/\tau$) [9, 10].

From the viewpoint of hole, the valence band structure of Si is more complex than the conduction band. For unstrained bulk-Si devices, holes occupy the top two bands: the heavy and light hole bands, which degenerate at gamma-point (k=0). With the bi-axial strain, the valance bands will split at gamma-point (k=0), as shown in Figure 1.4. We can see that light hole (smaller effective mass) band lies upper than heavy hole band in out-of-plane band diagram, so that holes prefer to assemble in light hole band (i.e., upper band represents lower energy for holes) [9, 10]. Strain reduces the acoustic scattering rate by altering the light and heavy hole band density of states and/or by reducing inter band optical phonon scattering through light to heavy hole band splitting, thus increasing the mobility. For biaxial stress since there is no mass improvement, the mobility enhancement only results from reduced scattering and thus requires ~25-30% Ge (>1GPa stress). This is because a splitting energy greater than 60 meV (i.e., must be higher than optical phonon energy in Si) or stress greater than 1 GPa is necessary to appreciably suppress intervalley phonon scattering [11].

Although the merit of mobility enhancement has been demonstrated, it should be noted that the thickness of the top strained-Si layer must be thinner than the critical thickness that depends on the Ge content of the underlying relaxed SiGe layer to avoid the generation of high amount of dislocations [12]. Besides, there are other issues that significantly compromise the advantages of strained-Si (on relaxed SiGe layer) devices.

These issues include surface roughness, fast diffusion of n-type dopants, thermal stability of silicide, strained-Si thickness control, Ge out diffusion [6], self heating, and expensive wafer cost.

Recently, uni-axial channel strain technology was proposed to suppress the aforementioned concerns. Uni-axial strain can be engineered by modifying contact-etch-stop-layer (CESL) deposition [13, 14], shallow trench isolation (STI) [15, 16], source/drain (S/D) material [17], silicidation [18], packing process [19], and so on. Furthermore, the behaviors of carrier mobility under uni-axial strain depend on the strength of the strain and the orientation [20] (see Figure 1.5). Uni-axial strain can be applied arbitrarily in any direction relative to the carrier transport direction. The channel tensile and compressive stress can be applied separately to NMOS and PMOS devices to enhance performance, respectively (see figure 1.5). Enhancements of carrier mobility under bi-axial and uni-axial strain were actually induced by different factors and mechanisms.

To compare the bi-axial and uni-axial strain, the changes in the scattering and effective mass are taken into account to quantify the mobility enhancement of holes, both of which depend on the strain-altered valance band. Unlike the case in unstressed case, the effective mass of bi-axial tensile and longitudinal uni-axial compressive stresses is nearly constant over the surface energy range of a few kT below the valence band. The strain removes the degeneracy and reduces the band-to-band coupling, resulting in roughly constant effective mass. From the work of C. W. Leitz et al. [11], we can observe that uni-axial compressive strained MOSFETs may have lighter in-plane effective mass by full-band Monte Carlo simulation, which will improve hole mobility. But for bi-axial tensile stress, the effective mass is heavier than that in un-strained case (Figure 1.4), so the hole mobility enhancement is only possible through the reduction of inter-valley scattering. This effect becomes significant only when the strain level is high

enough (e.g., Ge > 20 %) as mentioned above. But the reduction of the intra-band acoustic scattering by altering the light- and heavy-hole band density-of-states is negligible for uni-axial strain in Si, even at several hundreds of mega-pascal. Because the energy difference $\triangle Es$ between light-hole band and heavy-hole band is split by uni-axial stress at gamma-point (k=0) and reduces the optical phonon scattering.

The mobility enhancement of uni-axial strain at high vertical electric field is higher than the bi-axial case. This represents another advantage of uni-axial strain over the bi-axial strain. Hole mobility at high vertical field would have different behaviors between uni-axial compressive and biaxial tensile stresses. Splitting of light- to heavy-hole band caused by uni-axial and biaxial stresses has no significant difference without considering surface quantization confinement. However, the splitting of light- and heavy-hole bands caused by bi-axial tensile stress would be annulled at high electric field due to surface confinement [10]. In contrast, hole mobility enhancement under uni-axial compressive strain is not annulled by surface confinement, which represents a major advantage for MOSFETs operating at high electric fields. The splitting magnitude of the surface confinement depends on the relative magnitude of the stress altering light and heavy hole out-of-plane effective masses. Recent reports [10] showed an interesting finding that the out-of-plane effective mass of light hole is heavier than heavy hole for uni-axial stress and causes the increase of the light- to heavy-hole band splitting. On the contrary, for bi-axial stress the previously-reported out-of-plane effective mass of light hole is lighter than heavy hole and causes reduced band splitting. This is the reason why the bi-axial stress degrades hole mobility enhancement at high vertical electric fields.

In strained-Si NMOSFETs, the strain will induce valence band offset [21]. The negative valence band offset causes the Fermi level to move closer to the conduction band, thus the band offset lowers the threshold, resulting in shallower channel depletion. The fact that the threshold voltage shift caused by bi-axial tensile stress is larger than

that by uni-axial tensile strain and has been reported for NMOSFETs [21]. This is because the bi-axial tensile stress induces more band gap narrowing than uni-axial tensile strain. For PMOSFETs, larger shift of light-hole band edge under bi-axial tensile strain leads to a larger shift in Vth than the case with uni-axial compressive strain [10].

1-1.3 Motivation

The SiN CESL (contact-etch-stop-layer) has been implemented by the industry to induce channel strain for mobility enhancement of NMOS [13, 14]. In this study we discuss the impact of SiN-capping layer on locally strained device characteristics.

Device degradation induced by hot electrons represents one of the most critical reliability issues in deep sub-micron NMOSFETs [22, 23]. The physical mechanisms and characteristics of hot electron degradation have been extensively examined [24, 25]. The degradations in terms of threshold voltage shift (ΔV_{th}), drain current degradation (ΔI_{DS}), and transconductance degradation (ΔG_m), have been studied by using the accelerated stress test. However, there seem to be very few works devoted to investigating the impact of SiN capping layer and the associated deposition process on the hot carrier reliability of the strained devices. This motivates us to carry out this study on the hot carrier degradation of NMOSFETs devices having local channel strain induced by the SiN-capping layer.

1-2 Organization of This Thesis

In addition to this chapter, this thesis is divided into the following chapters.

In Chapter 2, we briefly describe the process flow for fabricating the NMOS devices with the SiN capping layer. We also present the characterization method, measurement setup, and the stress conditions.

In Chapter 3, we show and discuss the improvement on device performance with SiN capping layer. The results on evaluating the hot carrier characteristics of the locally strained devices are also presented. Effects of strain on the hot carrier are also discussed.

Finally, important conclusions generated from our experimental results are summarized.

Chapter 2
Device Fabrication and Measurement Setup

2-1 Device Fabrication and Process Flow

The NMOSFETs were fabricated on 6-inch p-type (100) Si wafers with resistivity of 15~25Ω-cm and the wafer thickness is 655 ~ 695 μm. The p-type well was formed first by BF_2^+ implantation at 100 keV and 1×10^{13} cm^{-2}. Next, a standard local oxidation of silicon (LOCOS) process with channel stop implant (by BF_2^+ implantation at 120 keV and 4×10^{13} cm^{-2}) was used for device isolation. Threshold voltage adjustment and anti-punch through implantation were done by implanting 40 KeV BF_2^+ and 35 KeV B^+, respectively. After splitting the wafers to receive the growth of 3 nm-thick thermal gate oxide, a 150nm undoped poly-Si layer was deposited by low-pressure chemical vapor deposition (LPCVD), followed by gate etch process to pattern the film. The Source/Drain (S/D) extension regions were then formed by As^+ implantation at 10 keV and 5×10^{14} cm^{-2}. After a 80nm TEOS spacer formation, S/D regions were formed by P^+ implantation at 15 keV and 5×10^{15} cm^{-2}. Then the substrate electrode patterning was performed through lithography and etching processes, followed by the formation of the substrate junction by BF_2^+ implantation at 40 keV and 5×10^{15} cm^{-2}. Rapid thermal anneal (RTA) was then carried out in a nitrogen ambient at 900°C for 30 sec to activate dopants in the gate, S/D, and substrate regions.

Afterwards, most samples were capped with a SiN capping layer (contact-etch-stop-layer, CESL) with different thickness (100nm, 200nm and 300nm), using low-pressure chemical vapor deposition (LPCVD) system, while some wafers were deliberately skipped of the SiN capping layer to serve as the controls. The SiN

deposition was performed at 780 ℃ with SiH_2Cl_2 and NH_3 as the reaction precursors. For some samples having the SiN capping, the SiN layer was removed later in order to evaluate the impact of SiN deposition process itself on the device performance (denoted as the SiN-removal split). Then wafers were combined to receive a 300nm TEOS passivation by LPCVD system. After contact hole etching, normal metallization scheme was carried out. The final step was a forming gas anneal performed at 400°C for 30 min to passivate the dangling bonds and to reduce interface state density in the gate oxide/Si interface. Cross-sectional view of the fabricated device was shown in Fig. 2.1. NMOSFETs with different split conditions are summarized in Table 2.1.

2-2 Measurement Setup

2-2.1 Electrical Measurement Setup

Current-voltage (I-V) and capacitance-voltage (C-V) characteristics were evaluated by an HP4156A precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. Temperature-regulated hot chuck was used to control the device under test at a fixed temperature of 25°C.

Charge pumping measurement is widely used to characterize interface state densities in MOSFET devices [26]. This type of measurement is very effective because it allows the exclusion of gate leakage contribution to the calculated interface state densities presented in thin gate oxides and at lower frequencies [27, 28]. Therefore, to accurately analyze interface state densities or bulk traps in the dielectrics from charge pumping measurement results, we need to pay a close attention to the leakage current issue. The basic charge pumping measurement includes the measurement of the substrate current while a series of voltage pulses with fixed amplitude, rise time, fall time, frequency, and duty cycle is being applied to the gate of the transistor (Figure 2.2),

with source and drain connected to a small reverse bias, and substrate connected to ground. Three conventional types of voltage pulse train, namely, (a) fixed amplitude sweep, (b) fixed base sweep, and (c) fixed peak sweep, as depicted in Figure 2.3 could be applied to the gate electrode. In this thesis, we used the "fixed amplitude sweep" mode to calculate interface trap density, and the "fixed base sweep" mode to analyze the lateral distribution of interface trap, respectively. Square-wave waveforms (f = 1MHz) were applied to the gate, and the base voltage was varied to change the surface condition from inversion to accumulation, while keeping the pulse amplitude at 1.5V. A MOSFET with a gate area of A_G gives the charge pumping current as [29]:

$$I_{cp} = qA_G fN_{it} \tag{2-1}$$

, from which the interface trap density (N_{it}) could be calculated.

2-2.2 Hot Carrier Reliability Measurement Setup

In our reliability measurements, devices were stressed with the drain voltage set at a highly positive voltage, and the gate terminal biased at the voltage where maximum I_{sub} occurred to accelerate the degradation. So the Isub-V_G curve with the drain terminal biased at a given voltage was measured first to find V_G@$Isub_{max}$ before stressing the device. To monitor the degradation caused by the hot electrons, the I_D-V_G characteristics at V_{DS} = 0.05 V (linear region) and charge pumping current were measured before and after the stress. The degradations in terms of threshold voltage shift (ΔV_{th}), generation of interface trap density (ΔN_{it}), and transconductance degradation (ΔG_m), were detected and recorded in the accelerated stress test.

2-2.3 Extraction Procedure of Lateral Distribution of Nit

The lateral distribution of interface state post hot carrier stress of all splits was also

discussed in this work. This method builds on [30] and the measurement setup is shown in Figure 2.4. The experimental procedures of this method are described below.

(1) Measure the Icp-V_h curve on a virgin MOSFET from the drain junction (with the source junction floating), and from it establish the V_h versus $V_{th}(x)$ relationship [31] near the junction of interest.

(2) Record the Icp-V_h curve after hot-carrier injection.

(3) The hot-carrier-induced interface state distribution, $N_{it}(x)$, is obtained from the difference of the Icp-V_h curve before and after hot carrier stress.

Chapter 3
Results and Discussion

3-1 Electrical Characteristics of Locally Strained NMOSFETs

3-1.1 Basic Electrical Characteristics

Measurements of stress induced by the SiN film were performed on Si wafers capped with a blanket SiN layer with different thickness. The results are shown in figure 3.1. It can be seen that the tensile stress becomes larger when the SiN capping layer becomes thicker. Figure 3.2 shows the I_D-V_D characteristics of NMOSFETs for all splits (i.e., control, SiN-capped splits with three different thickness and SiN-removal splits). It can be seen that the SiN-capped splits all show apparent drain current enhancement, with the improvement increases with increasing SiN-capping thickness. In contrast, almost no current enhancement is observed for the SiN-removal samples. Obviously the current enhancement is straightly due to the induced strain from the SiN capping layer. When the SiN-capping layer is removed, there is no residual strain remaining in the channel. The Id-Vg characteristics of the same devices are shown in figure 3.3. We can see that the impact of SiN-capping layer mentioned above also reflects on the result of transconductance (Gm). It is also seen that the subthreshold slope of all devices almost does not appear to be influenced by the SiN-capping or SiN-removal. Figure 3.4 shows the subthreshold swing for all splits. It indicates that there was only a slight change in subthreshold swing with SiN-capping or SiN-removal.

Nevertheless, a slightly higher transconductance in SiN-removal splits over the controls was observed, as shown in figure 3.3(b). It can be ascribed to the decrease of interface state density with the deposition of the SiN capping layer. It is well known that hydrogen species can effectively passivate the dangling bonds at the Si/SiO_2 interface. In the LPCVD system used for SiN deposition, SiH_2Cl_2 and NH_3 were employed as the

reaction precursors, so the reaction chamber would be filled with hydrogen species during the deposition process. The hydrogen species would in turn passivate the dangling bonds at the Si/SiO_2 interface. Figure 3.5 shows the results of charge pumping measurements for all splits. It agrees with the aforementioned inference that Icp of the SiN-removal splits is less than that of the controls, as shown in figure 3.5(b). This also explains why Gm in the SiN-removal splits is slightly larger than that in the control ones, as shown previously in figure 3.3(b). From figure 3.5(a), we can see that the channel strain indeed causes the increase of interface states at the Si/SiO_2 interface. Nevertheless, an interesting result is also observed that the charge pumping current decreases with increasing SiN-capping thickness (figure 3.5(a)). It is because when the SiN deposition time is prolonged, more and more hydrogen species participate in interface state passivation. In other words, there are two factors that change the interface state density. One is the hydrogen species from the reaction precursors and the other is the stress induced by the SiN capping layer.

Figure 3.6 shows the percentage increase of the drive current of the SiN-capped and SiN-removal samples compared with the controls, as a function of channel length. We can see that the drive current enhancement reaches about 12%, 17%, and 20% at a channel length of 0.4 μm for devices with SiN thickness of 100 nm, 200 nm, and 300 nm, respectively, while SiN-removal devices show essentially no enhancement. It can also be seen that when the channel length decreases, the strain effect enhances. In other words, the strain is distributed locally near the source and drain. So the drain current enhancement becomes more prominent with decreasing channel length. The capacitance-voltage characteristics of the samples are shown in figure 3.7. It can be seen that the oxide thickness difference among the splits is negligible, albeit slightly larger poly depletion effect is observed in the SiN-capped and SiN-removal devices. We believe this is caused by the SiN deposition. Since the temperature of the LPCVD

system was brought up to 780˚C for SiN deposition, out-diffusion of poly gate dopant at such a high temperature may be one of the factors that lower the inversion gate capacitance. However, the origin of this phenomenon remains unclear and more efforts are needed for a full understanding at this stage.

3-1.2 Short Channel Effect

Threshold voltage (V_{th}) roll-off characteristics of the devices are shown in figure 3.8. The results are obtained at V_{DS} = 0.05 V. It is worth noting that the control sample depicts a reverse-short-channel-effect (RSCE). This can probably be explained by boron segregation at the implant-damaged regions located near the edge of the channel [32]. However, this phenomenon is not observed on the SiN-capped and SiN-removal splits. Additional thermal budget associated with the SiN deposition step would reduce the boron segregation effect, explaining the suppression of the RSCE as shown in figure 3.8(b). Another interesting trend is shown in figure 3.8(a). It can be seen that a grave Vth roll-off behavior is observed for the SiN-capped devices, however, the phenomenon is puny for the SiN-removal devices, as shown in figure 3.8(b). It indicates that the channel strain induced by the SiN capping layer is relaxed by removing the SiN capping layer. Since the bandgap narrowing effect caused by channel stress [17] is negligible when the SiN is removed, so the SiN-removal splits show better Vth roll-off behavior than the SiN-capped counterparts.

Drain induced barrier lowing (DIBL) is another guide for evaluating the short channel effects. We use the interpolation method to calculate DIBL effect for all splits. The results are shown in figure 3.9. It is clearly seen that there is no distinguishable difference among all splits. It appears that the SiN capping layer will not complicate the DIBL effect of the samples.

3-2 Hot Carrier Degradation of Locally Strained NMOSFETs

3-2.1 Substrate current and impact ionization rate

A hot carrier with sufficient energy can creation more charge carriers through impact ionization. For NMOSFET devices, holes generated by impact ionization are collected by the substrate. Figure 3.10 shows the substrate current (I_{sub}) versus gate voltage for all splits of devices. It can be seen that the substrate current of the SiN-capped devices is larger than that of the SiN-removal counterparts. This result shows clearly that the channel strain plays an important part in affecting the generation of channel hot electrons and the associated impact ionization process. Bandgap narrowing and mobility enhancement, both due to channel strain, may mainly be the whys and wherefores to enhance the ionization rate [33]. Also it is noted that a larger substrate current is observed as the SiN thickness increases, which is attributed to the increased mobility with increasing SiN thickness. It is also interesting to note that, as in figure 3.10(b), substrate current in the SiN-removal splits is a slightly larger than the control counterparts. This can be explained by the additional thermal budget associated with the fabrication that serves to reduce the implant damage near the drain region, and the extra hydrogen species incorporated that can passivate the dangling bonds at the Si/SiO_2 interface, as mention above. The extra weak Si-H bonds would enhance the ionization rate and produce more hot electrons and holes [34, 35], so the substrate current of SiN-removal samples is larger than that of the controls.

Figure 3.11 shows the impact ionization rate (I_{sub}/I_D) in all splits. Strangely, the impact ionization rate (I_{sub} /I_D) is nearly the same irrespective of the thickness of SiN capping layer. This result is different from the aforementioned results of substrate current, shown previously in figure 3.10(a). Bandgap narrowing due to strained channel will increase the barrier for electrons going from the silicon conduction band to the

conduction band of the gate electrode, so that SiN-capped samples do not show larger I_{sub}/I_D. Enhanced drain current (I_D) due to strained channel will be another reason.

3-2.2 Hot carrier stress

As discussed above, it is expected that devices with SiN capping would show aggravated hot carrier degradation. Figure 3.12 and figure 3.13 show threshold voltage shift and increased interface state density, respectively, for all splits of devices that received hot-electron stressing at V_{DS} = 4.5 V and V_{GS} at maximum substrate current. All devices are with channel length/width = 0.5μm/10μm. Note that, although the SiN capping may significantly worsen the degradation, the difference among samples with different SiN thickness is very small.

To carry out the painstaking task of investigating the impact of SiN capping layer on the device, we concentrate on comparing the control, 300nm-SiN-capped and 300nm-SiN-removal splits. Typical results of hot-electron stressing for the three splits of samples are shown in figure 3.14. Channel length and width of the test devices are 0.5 μm and 10 μm, respectively. The devices were stressed at V_{DS} = 4.5 V and V_{GS} at maximum substrate current. The I_D-V_G characteristics at V_{DS} = 0.05 V were measured before and after the stress to evaluate the degradation caused by the hot electrons. As shown in figure 3.14, the degradation is the worst in the SiN-capped sample among the three splits. The aggravation is alleviated in the SiN-removal sample, though the resultant degradation is still worse than the control counterpart.

Figure 3.15 shows the shift of threshold voltage (ΔV_{th}), degraded peak transconductance (ΔG_m), and increased interface state density (ΔN_{it}) as a function of the stress time. As mentioned above, the device with channel strain depicts aggravated degradation in terms of larger shifts in these parameters. We assume that the bandgap narrowing effect and the increased carrier mobility in the strained channel devices [33,

36] are the two primary culprits for the aggravated hot carrier degradation in the SiN-capped samples. These two factors may increase the impact ionization rate in the device, which is evidenced in figure 3.10, and lead to higher degradation.

Despite the relieving of the channel strain by SiN removal, the SiN-removal sample also shows much severe degradation than the control sample, as shown in figure 3.14 and figure 3.15. This phenomenon distinctly indicates that the SiN deposition process itself may result in the enhanced damage effect in the short channel devices. According to previous reports [33, 37], interface states could be generated due to the breaking of Si-H bonds by hot electrons, and the generated interface states would greatly degrade the device performance. Figure 3.16 shows charge pumping current for the three splits of fresh devices. As mentioned above, the SiN-removal sample shows the smallest charge pumping current (Icp) among all three splits which is due to the use of H-containing precursors (e.g., SiH_2Cl_2 and NH_3) in the SiN deposition step. However, hot carrier degradation would not follow this trend even if the SiN-removal sample has lower interface trap density. Figure 3.17 shows the increase in charge pumping current after 5000 s hot carrier stress (V_G@$Isub_{max}$ and V_{DS} = 4.5 V) for the three splits of devices. It is seen that more interface states than those in the control sample are actually generated in the SiN-removal device, implying that the extra hydrogen species from SiN layer are an important contributor for the aggravated degradation.

3-3 Analysis of the Distribution of Interface Trap Density

The measurement presented in section 2-2.3 was used to extract lateral distribution of interface trap state. It should be noted that the local V_{th} and V_{fb}, across the MOSFET, are not uniform due to the lateral doping variation as shown in figure 3.18. In order to detect the interface states, the voltage pulses applied during measurements must

undergo alternate accumulation and inversion cycles. Therefore, there should be no Icp as the high-level voltage (V_h) is lower than the minimum V_{th} under the gate. Only after V_h starts to exceed the local V_{th} in the channel will Icp begin to grow. Before V_h reaches the maximum local V_{th} in the channel, only interface states residing near the drain side will contribute to Icp, as the needed electrons cannot yet flow to the drain side from the source.

We choose the control sample for an example. If we assume that the interface state density is spatially uniform along the channel, which can be written as

$$I_{cp,\max} = q\, f\, N_{it}\, W\, L \tag{3-1}$$

where f is the gate pulse frequency, W is the channel width, and L is the channel length. Because V_{th} is not uniformly distributed, when V_h reaches the maximum local V_{th} in the channel, only interface states residing near the drain side (i.e., the shadow region in figure 3.18) will contribute to Icp. In figure 3.19, the corresponding Icp (V_h) comes from the interface state distributed in the region between the gate edge and the position where its local V_{th} equals V_h, i.e.,

$$I_{cp}(V_h) = q\, f\, N_{it}\, W\, x \tag{3-2}$$

where x represents the distance from the gate edge to the position where $V_{th}(x) = V_h$. Comparing (3-1) and (3-2), we can derive

$$x = \frac{L I_{cp}(V_h)}{I_{cp,\max}} \tag{3-3}$$

Figure 3.20 shows the local V_{th} versus distance x of the control sample. The local V_{th} decreases sharply as x is smaller than 0.07 μm. We can presume that the drain junction is near x = 0.07 μm.

After subjecting to 10 second of hot carrier stress (V_G@$Isub_{max}$ and V_{DS} = 4.5 V), the incremental charge pumping current (ΔIcp), as shown in Fig. 3.21, at a given V_h, is

proportional to the number of generated interface traps from the gate edge to the point x. ΔIcp can be written as

$$\Delta I_{cp} = q\, f\, W \int_0^x N_{it}(x)\, dx \tag{3-4}$$

Therefore, the Nit(x) generated by the hot carrier stress can be expressed as follows:

$$N_{it}(x) = \frac{d\Delta I_{cp}}{dx}\frac{1}{q\, f\, W} = \frac{d\Delta I_{cp}}{dV_h}\frac{dV_h}{dx}\frac{1}{q\, f\, W} \tag{3-5}$$

The relationship of $\frac{dV_h}{dx}$ versus x can be derived from V_h versus x, so the lateral distribution, Nit (x), could be obtained from the procedure mentioned above.

By the same procedure, the derived lateral profiles of the interface states for all splits of devices could be extracted by Eq. (3-5), and the results are shown in figure 3.22. From this figure we can directly calculate the damage region and the amount of interface states generated by the hot-carrier stress. We can see that the damage region is confined within the drain edge in all splits. This is reasonable since the hot-carrier effect is localized. It is obviously seen that interface state generation sharply increases in SiN-capped samples near the drain region, and the SiN-removal samples also show larger degradation than the control counterparts, even though the channel strain has been eliminated in these devices. These results are consistent with those mentioned above in section 3-2. In short, channel strain is responsible for the gravest hot carrier degradation observed in SiN-capped samples, while hydrogen species piled up at the source/drain edge during the SiN deposition is responsible for the slightly larger interface state generation in the SiN-removal devices over the control devices.

Chapter 4
Summary and Conclusion

In this thesis, the effects of LPCVD SiN process and the channel strain induced by the SiN-capping layer on the device characteristics and hot-electron degradation were investigated. Several important phenomena were observed and summarized as follows.

First, the channel strain induced by the SiN capping layer over the gate greatly boosts the drive current of short-channel devices. For example, enhancement ratio up to 20 % is achieved for the device with 300nm SiN-capping layer at a channel length of 0.4 μm. The SiN-removal devices show slightly higher Gm than the control sample owing to the passivation of the hydrogen species during the deposition process. Thermal budget associated with the deposition of the SiN capping layer could alleviate the reverse short-channel effect of the uncapped devices. Moreover, the bandgap narrowing effect due to the channel strain may result in further lowering in V_{th} as the channel length is shortened.

Secondly, hot-electron degradation is adversely affected when the SiN is deposited over the gate, even if the channel strain is relieved by subsequent SiN removal. The accompanying bandgap narrowing and the increased carrier mobility tend to worsen the hot-electron reliability in the SiN-capped devices. However, the hot carrier degradation of devices with SiN capping is independent of SiN thickness due to bandgap narrowing. Finally, enhanced edge effect caused by the hot carrier stress is also observed in SiN-removal devices.

In this work, additional thermal budget and hydrogen species are the two prime culprits for aggravated reliabilities in strained devices. Optimization of both SiN deposition process and the film properties are thus essential for the implementation of the uniaxial strain in NMOS devices.

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Figures

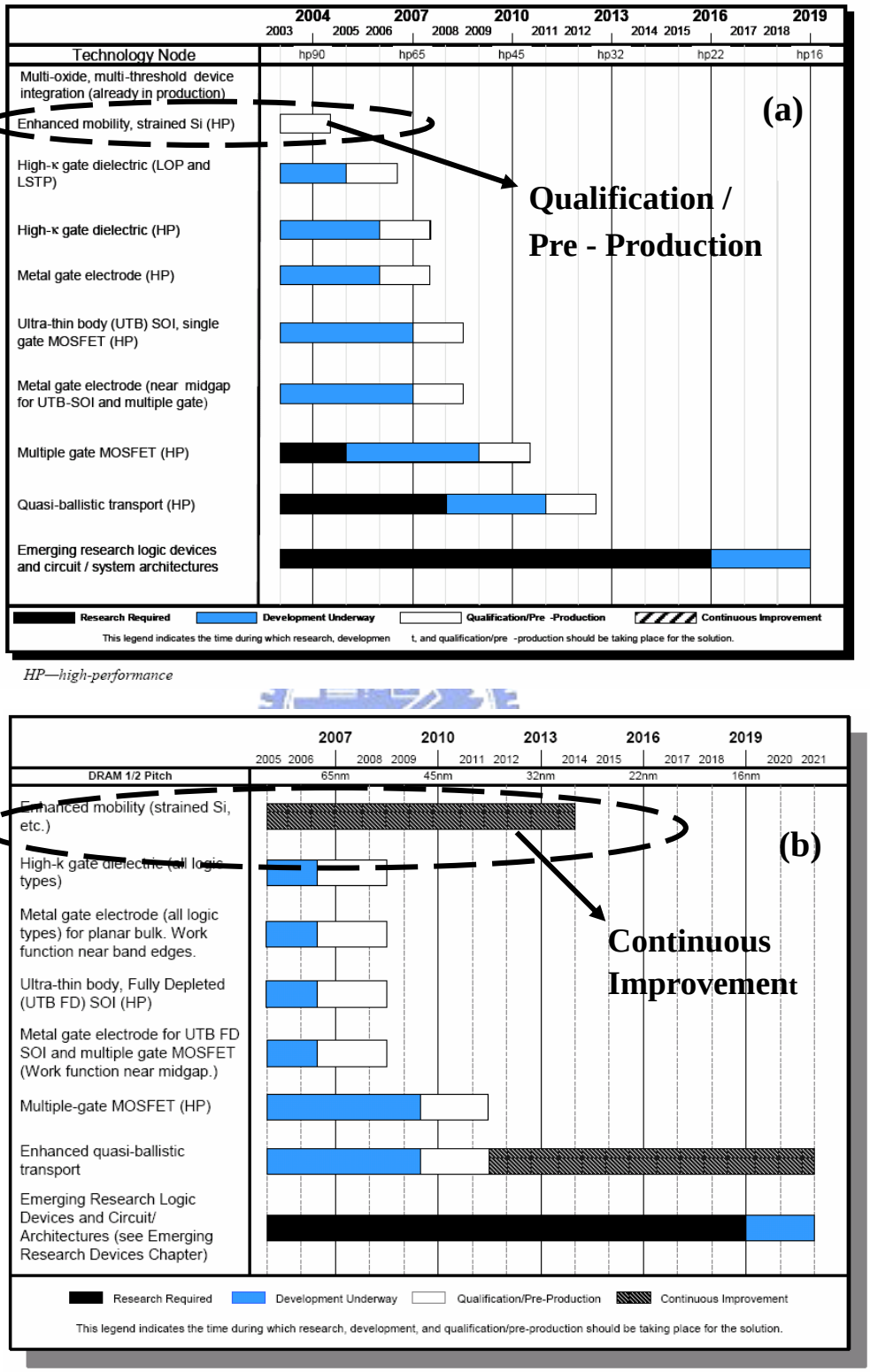


Fig.1.1 Logical potential solution on International Technology Roadmap for Semiconductors. (a) From Process Integration, Devices, and Structure in 2003 [4]. (b) From Process Integration, Devices, and Structure in 2005 [5].

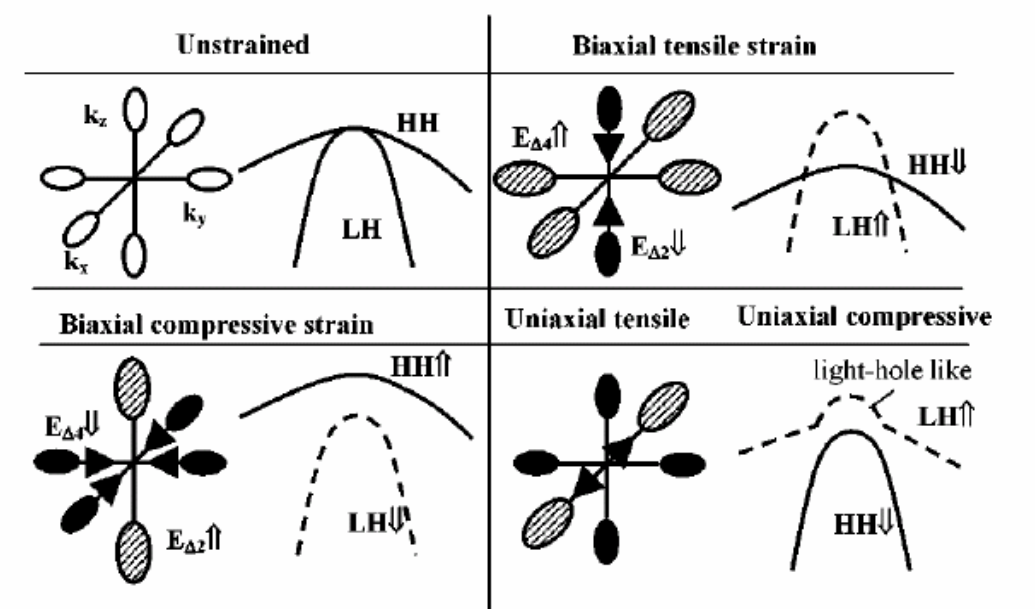


Fig.1.2 Fig. 1.2 Simple schematic of conduction and valence band bending with strain [8].

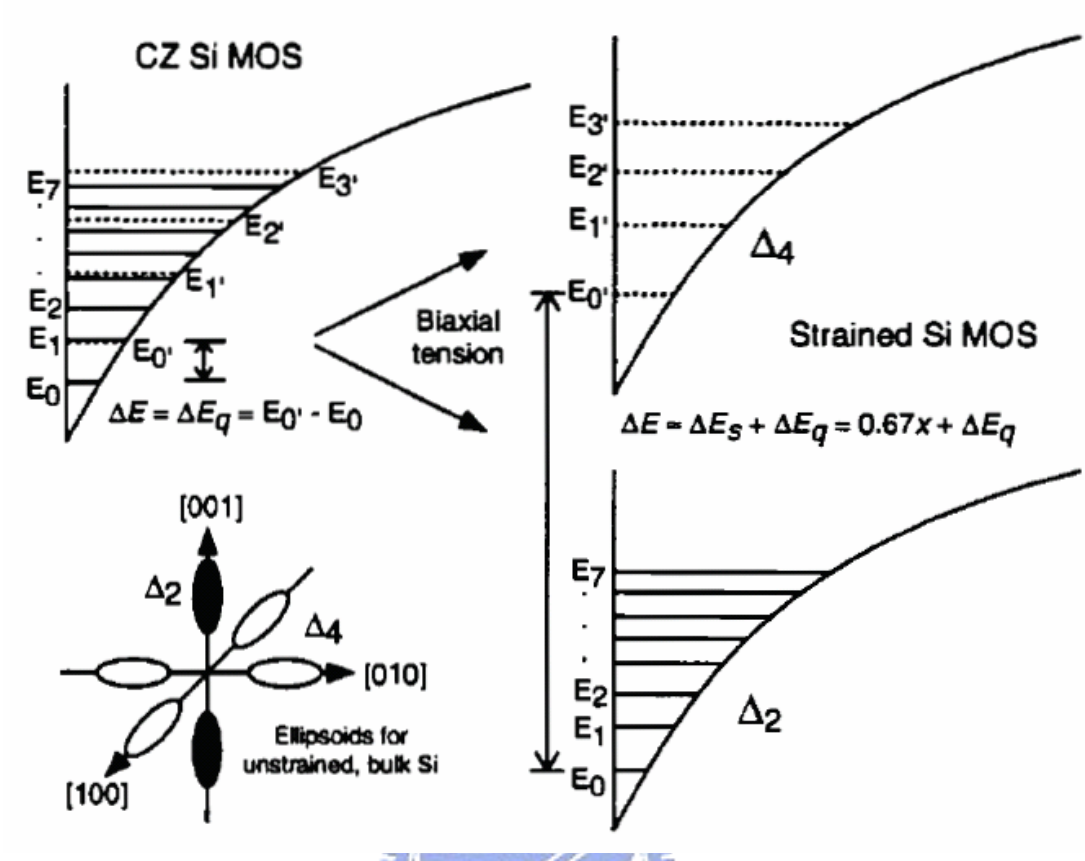


Fig.1.3 Schematic diagram of the energy sub-bands with unstrained and bi-axial strain in an MOS inversion layer [9].

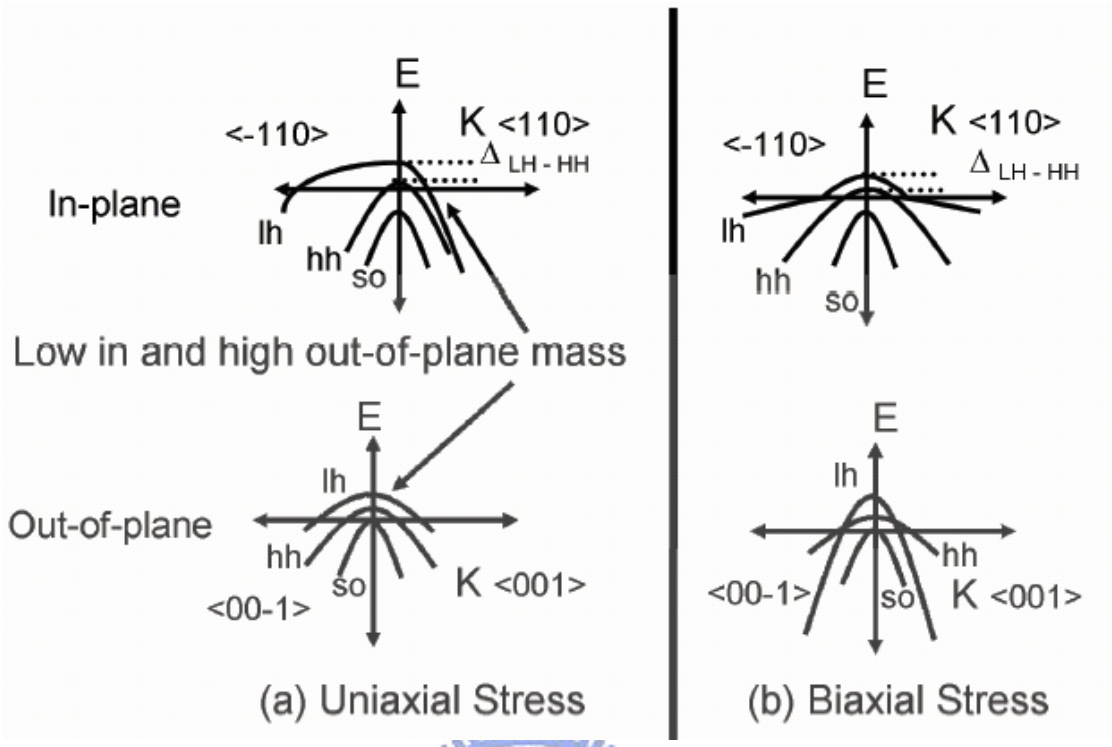
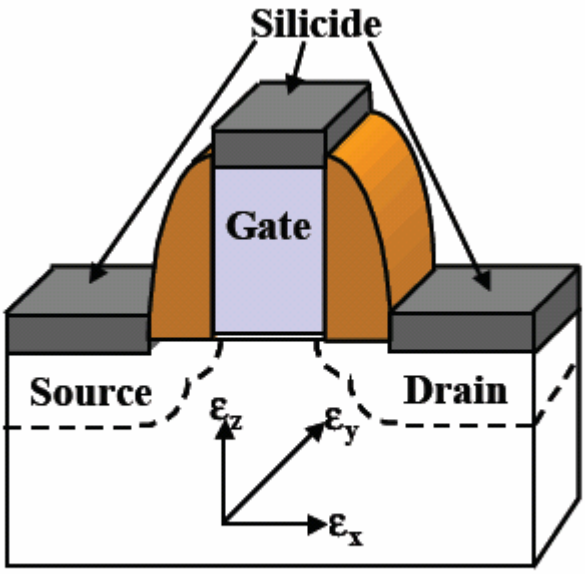


Fig.1.4 Schematic diagram of the valence bands E vs. k in uni-axial strained and bi-axial strain Si layers [10].



*Strain change = Increased tensile or decreased compressive strain

Direction of Strain Change*	CMOS Performance Impact	
	NMOS	PMOS
X	Improve	Degrade
Y	Improve	Improve
Z	Degrade	Improve

3D Strain Sensitivity of CMOS Current Drive

Fig.1.5 Schematic illustration for 3D process-induced strain component [20].

Gate		SiN Layer	Passivation Layer
Oxide 30Å	Undoped Poly-Si 1500Å	W/O (control)	TEOS 3000 Å
		SIN 300nm	
		Remove SIN 300nm	
		SIN 200nm	
		Remove SIN 200nm	
		SIN 100nm	
		Remove SIN 100nm	

Table 2.1 Split table of capping layer and oxide thickness.

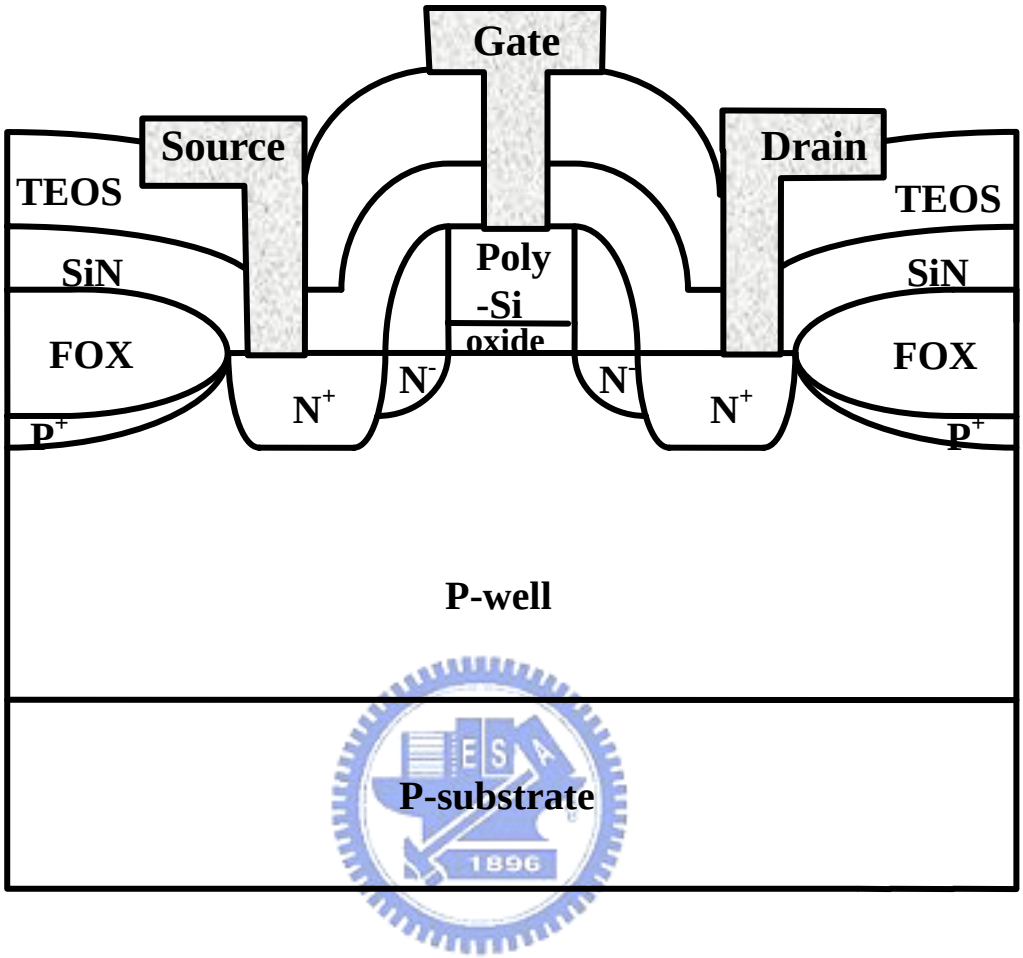


Fig.2.1 Schematic cross section of the locally-strained-channel NMOSFET.

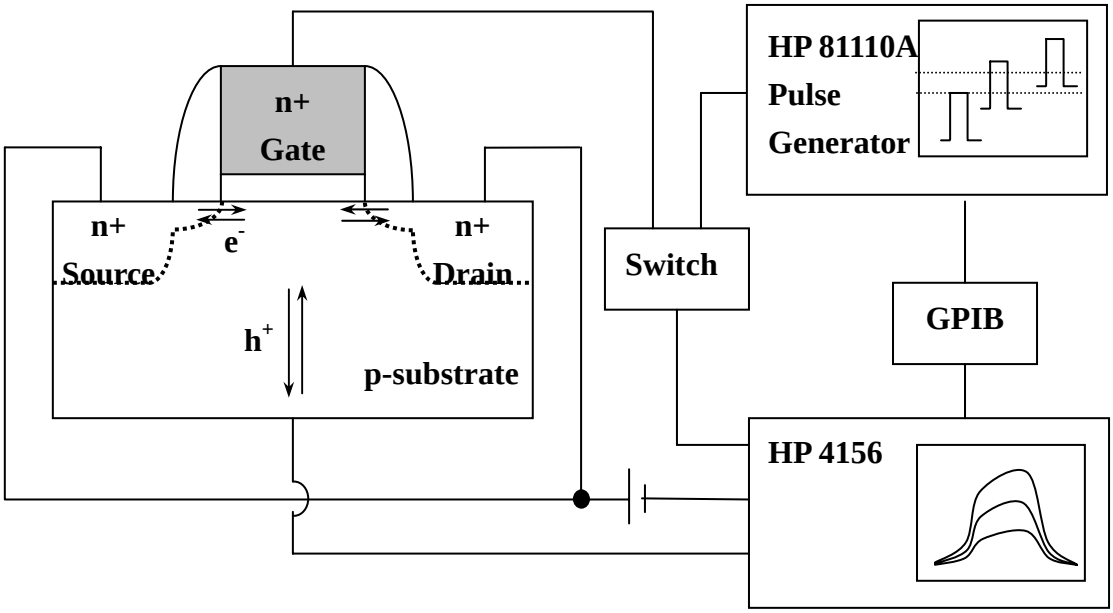


Fig.2.2 Setup structure for charge pumping.

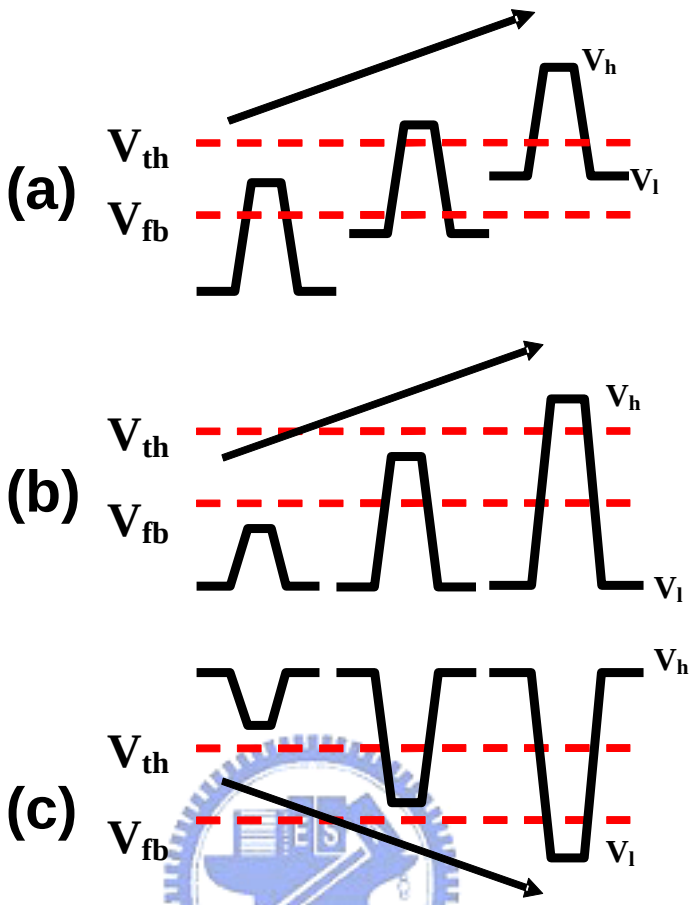


Fig.2.3 Schematic illustrations for the charge pumping measurement with (a) fixed amplitude, (b) fixed base sweep, and (c) fixed peak sweep. The arrows indicate the sweep directions.

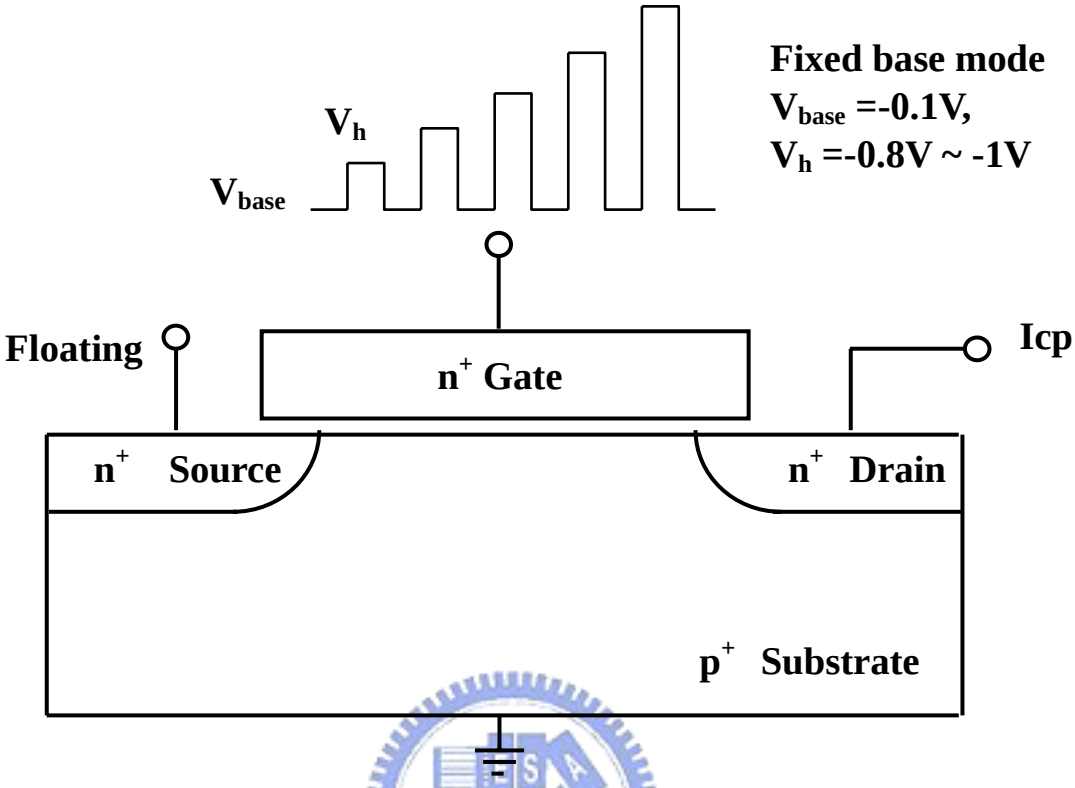


Fig.2.4 Measurement setup of single-junction charge pumping measurement.

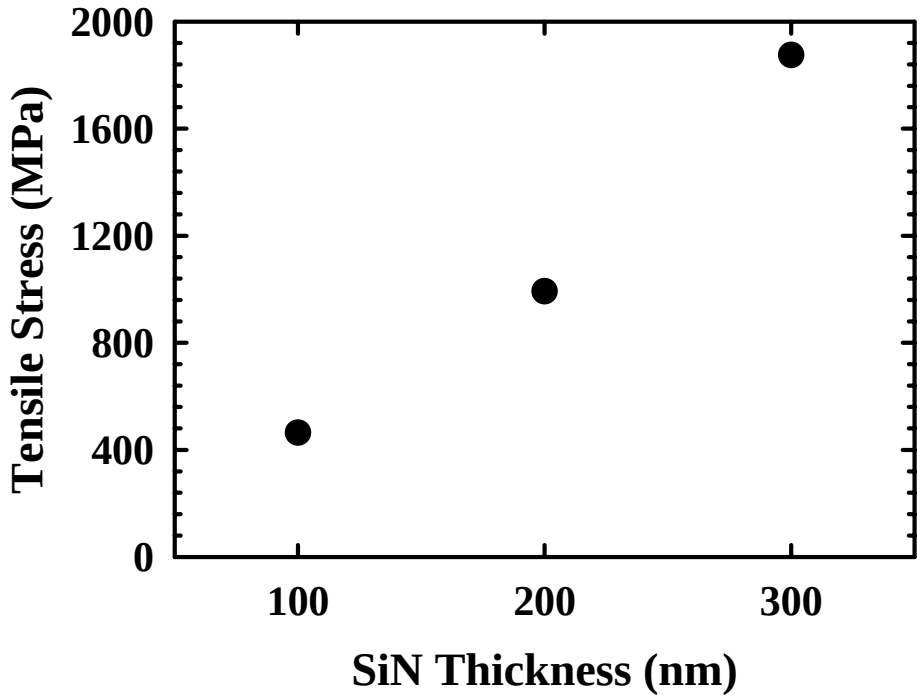


Fig.3.1 Measured tensile strain as a function of SiN thickness.

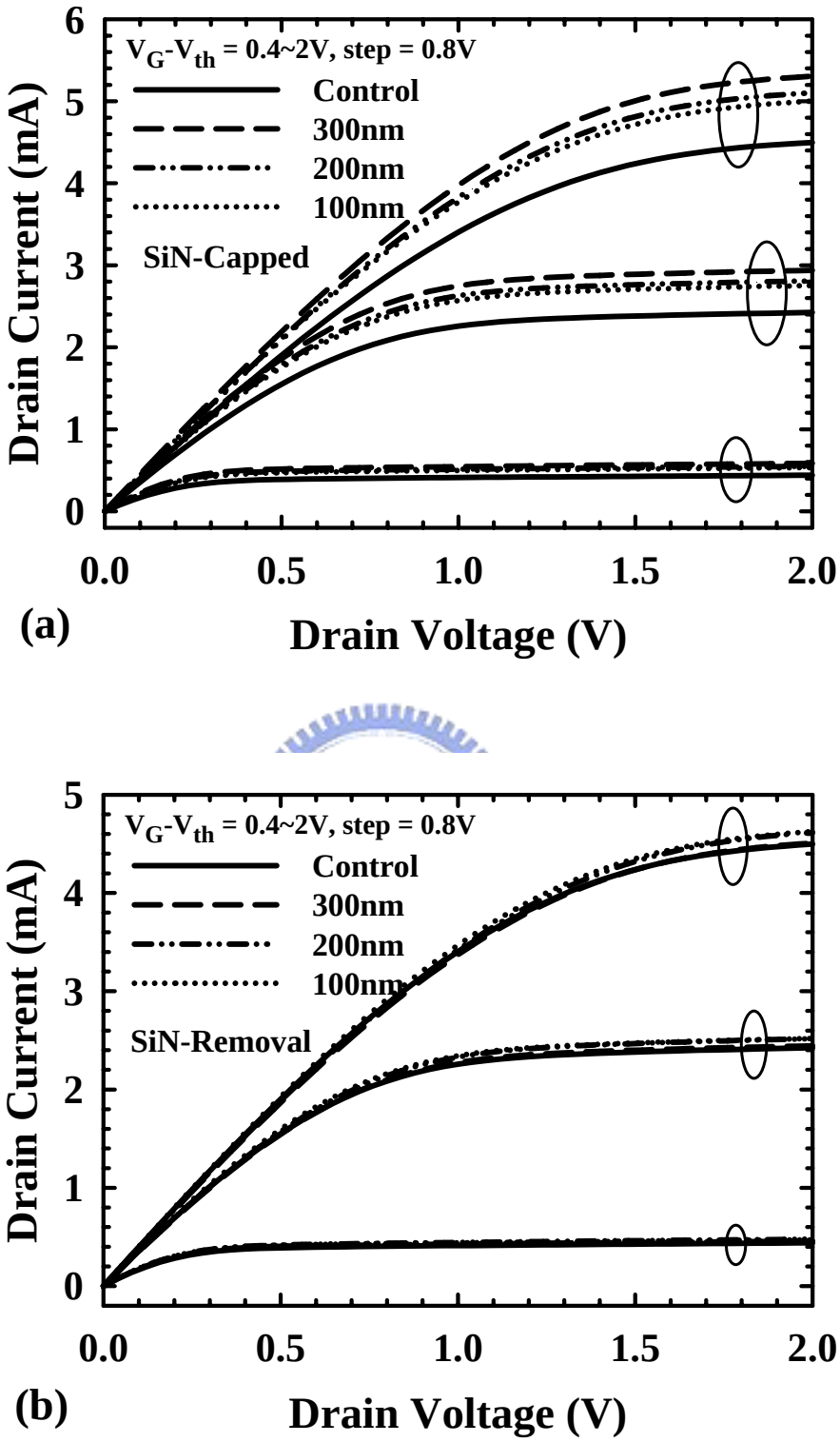


Fig.3.2 I_D-V_D Characteristics of different splits of NMOSFETs. Channel length/width = 0.5μm /10μm. (a) Control and SiN-capped devices with three different thicknesses. (b) Control and SiN-removal devices.

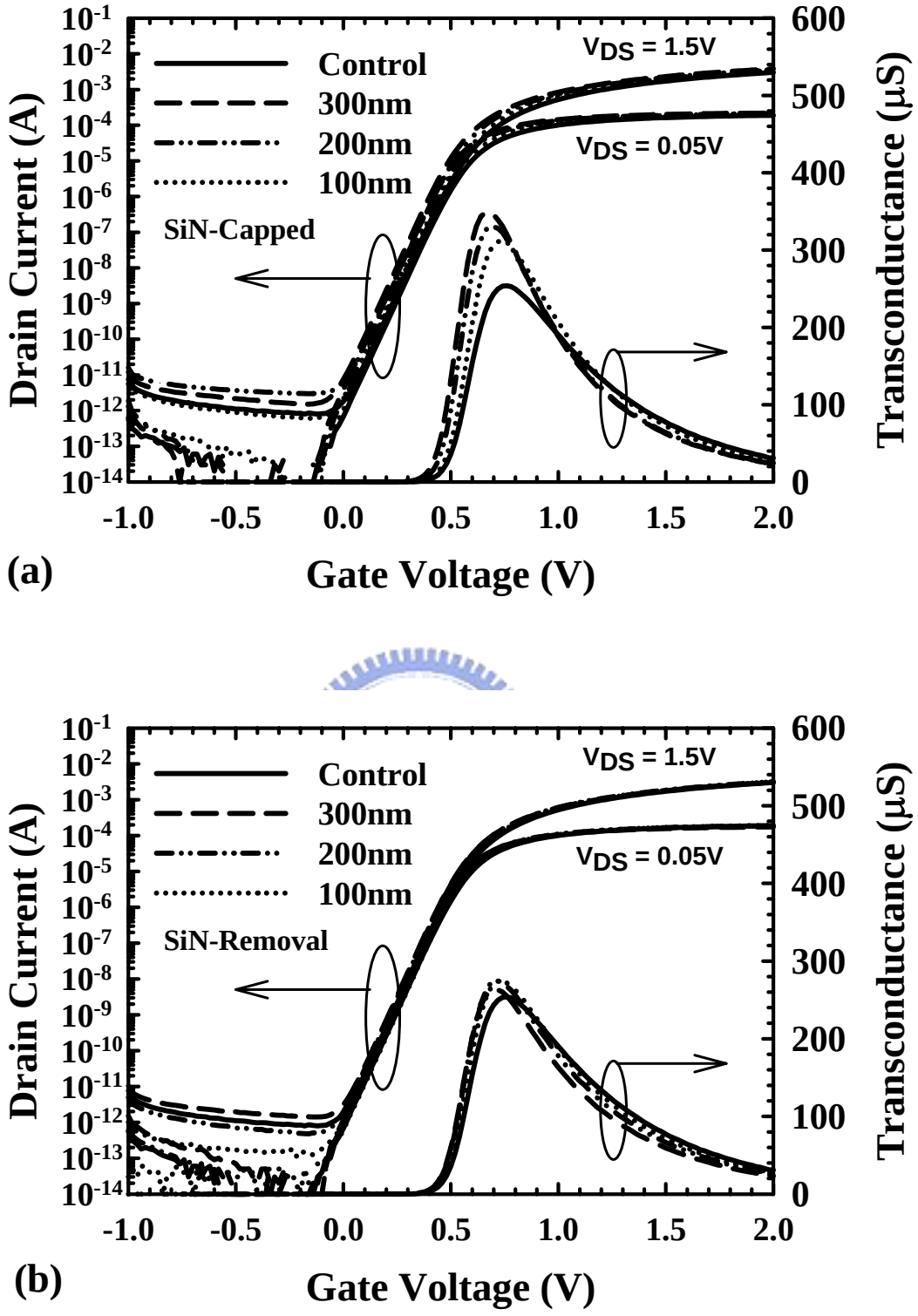


Fig.3.3 Subthreshold characteristics and transconductance of different splits of NMOSFETs. Channel length/width = 0.5μm /10μm. (a) Control and SiN-capped devices with three different thickness. (b) Control and SiN-removal devices.

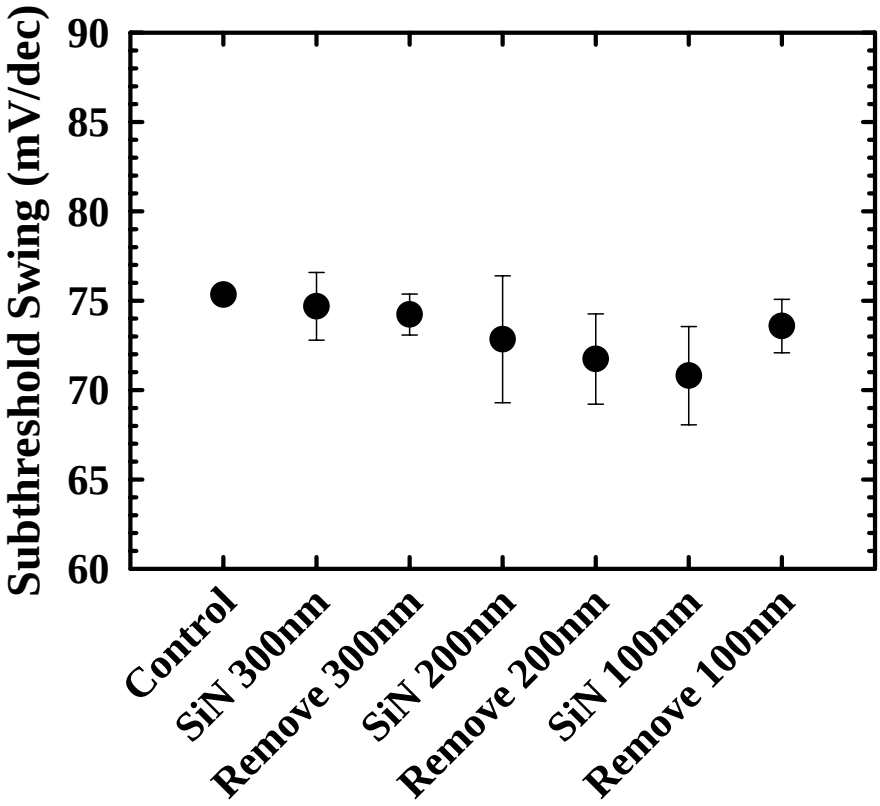


Fig.3.4 Subthreshold swing of different splits of NMOSFETs. Channel length/width = 0.5μm /10μm.

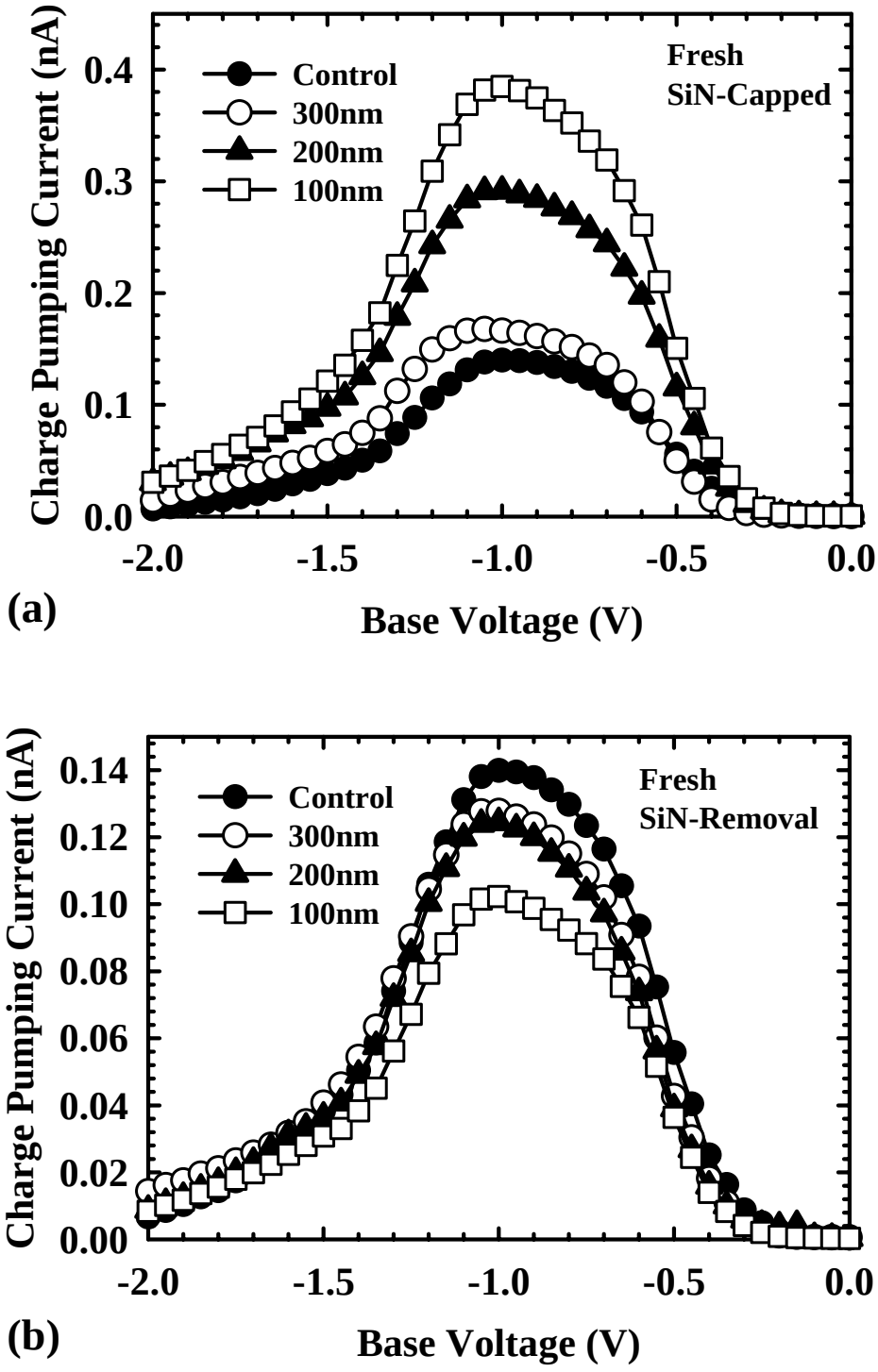


Fig.3.5 Charge pumping current of different splits of NMOSFETs. (a) Control and SiN-capped devices with three different thickness. (b) Control and SiN-removal devices.

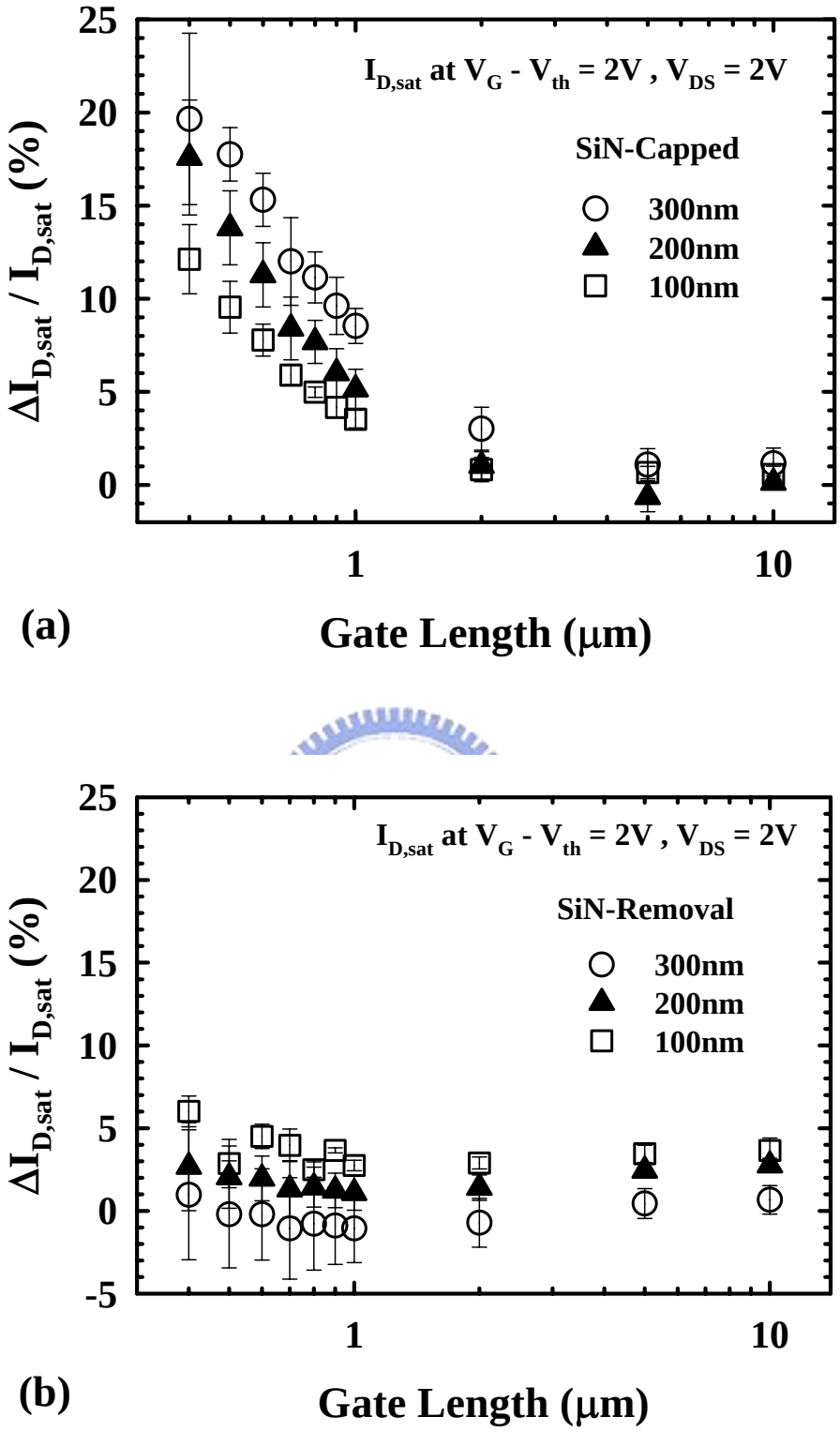
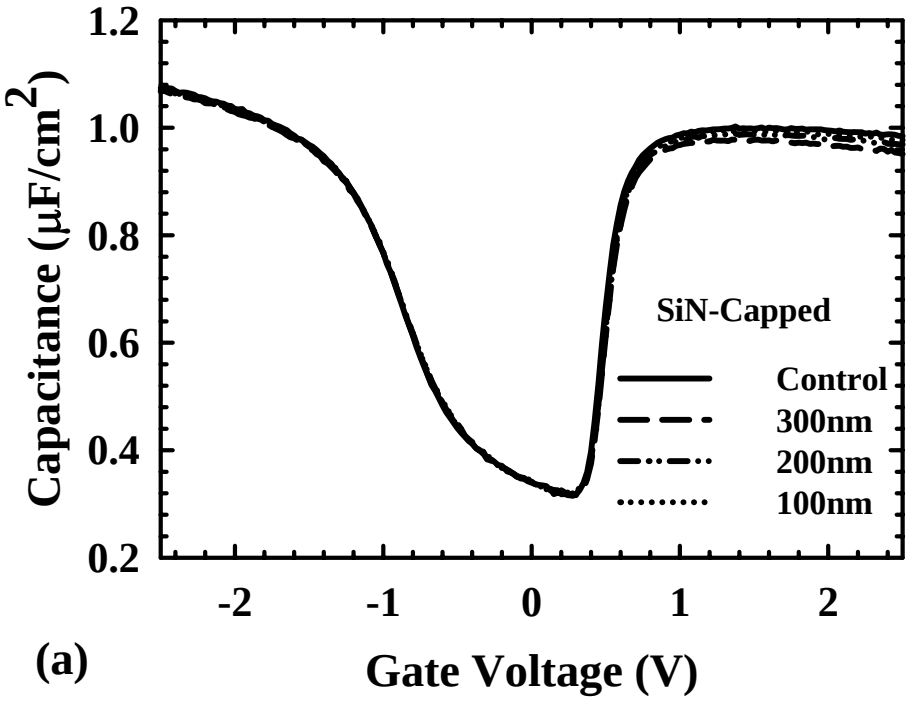


Fig.3.6 Increase in saturation current versus channel length. The saturation current was measured at $V_G - V_{th}$ = -2 V and V_{DS} = -2 V. (a) Control and SiN-capped devices with three different thickness. (b) Control and SiN-removal devices.



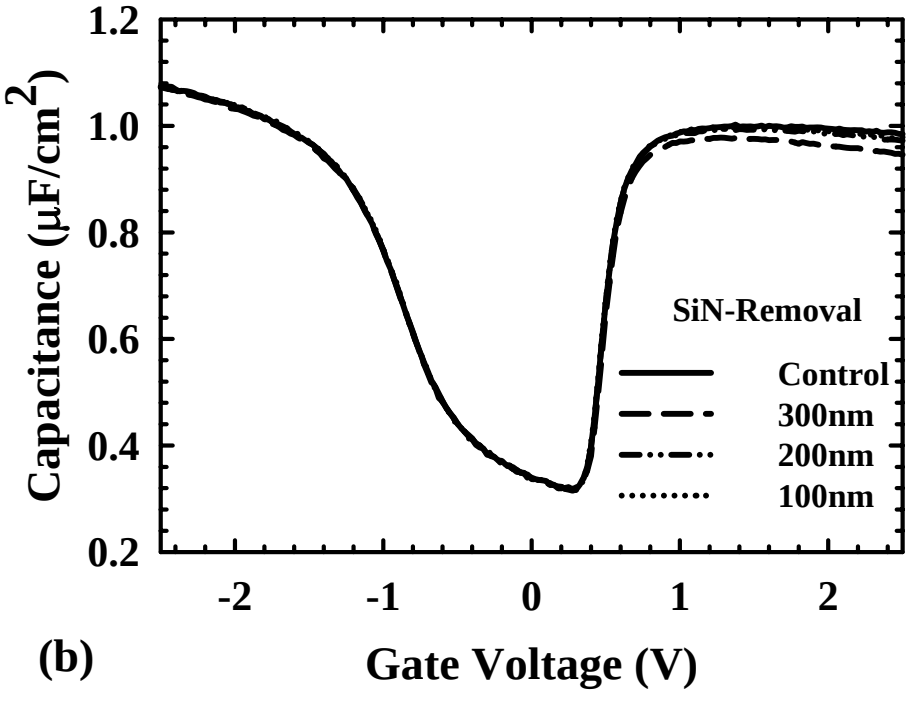


Fig.3.7 Capacitance-Voltage (*C-V*) characteristics of different splits of NMOSFETs. Channel length/width = 50μm /50μm. (a) Control and SiN-capped devices with three different thickness. (b) Control and SiN-removal devices.

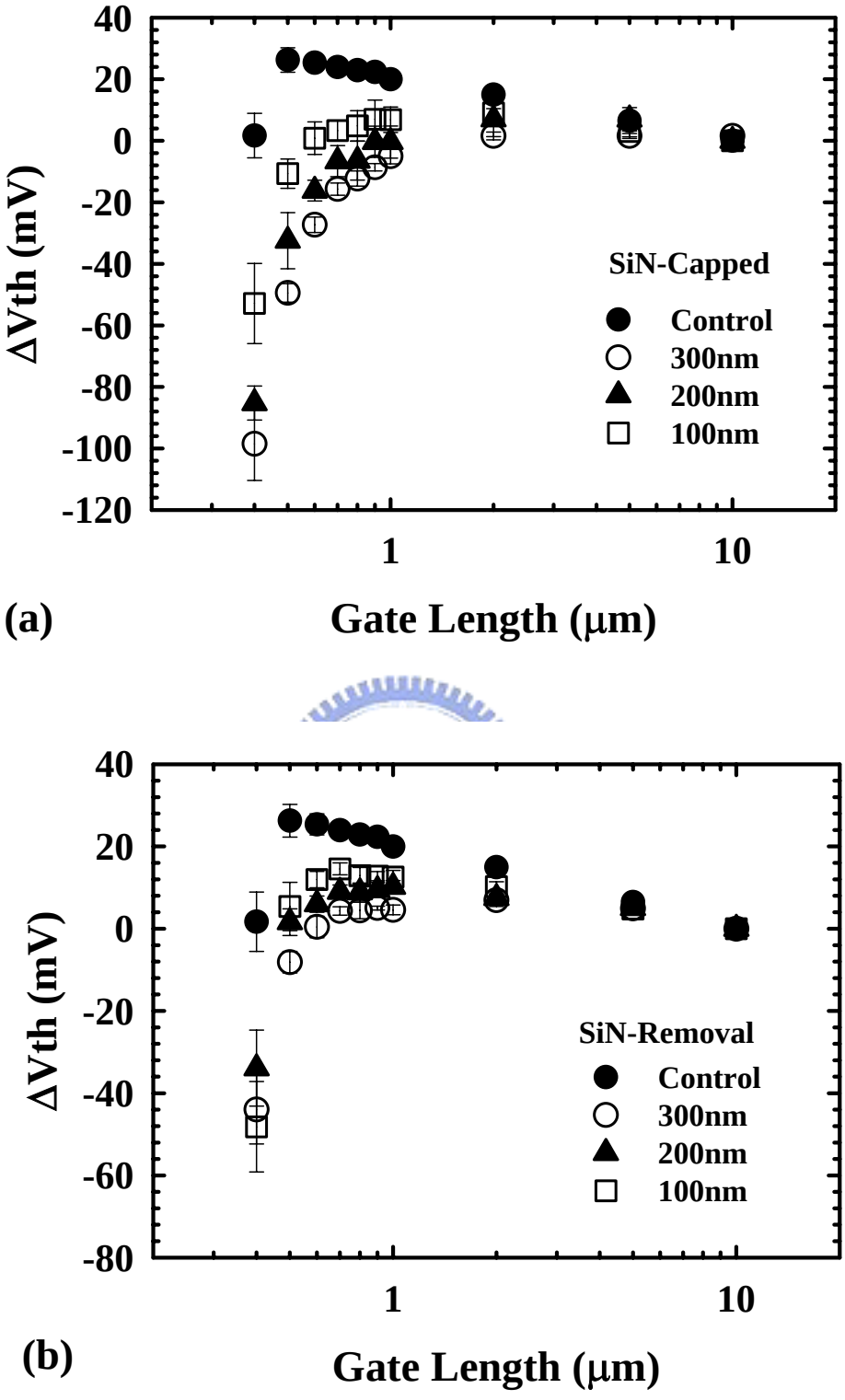


Fig.3.8 Threshold voltage roll-off as a function of channel length for different splits of samples. (a) Control and SiN-capped devices of three different thickness. (b) Control and SiN-removal devices.

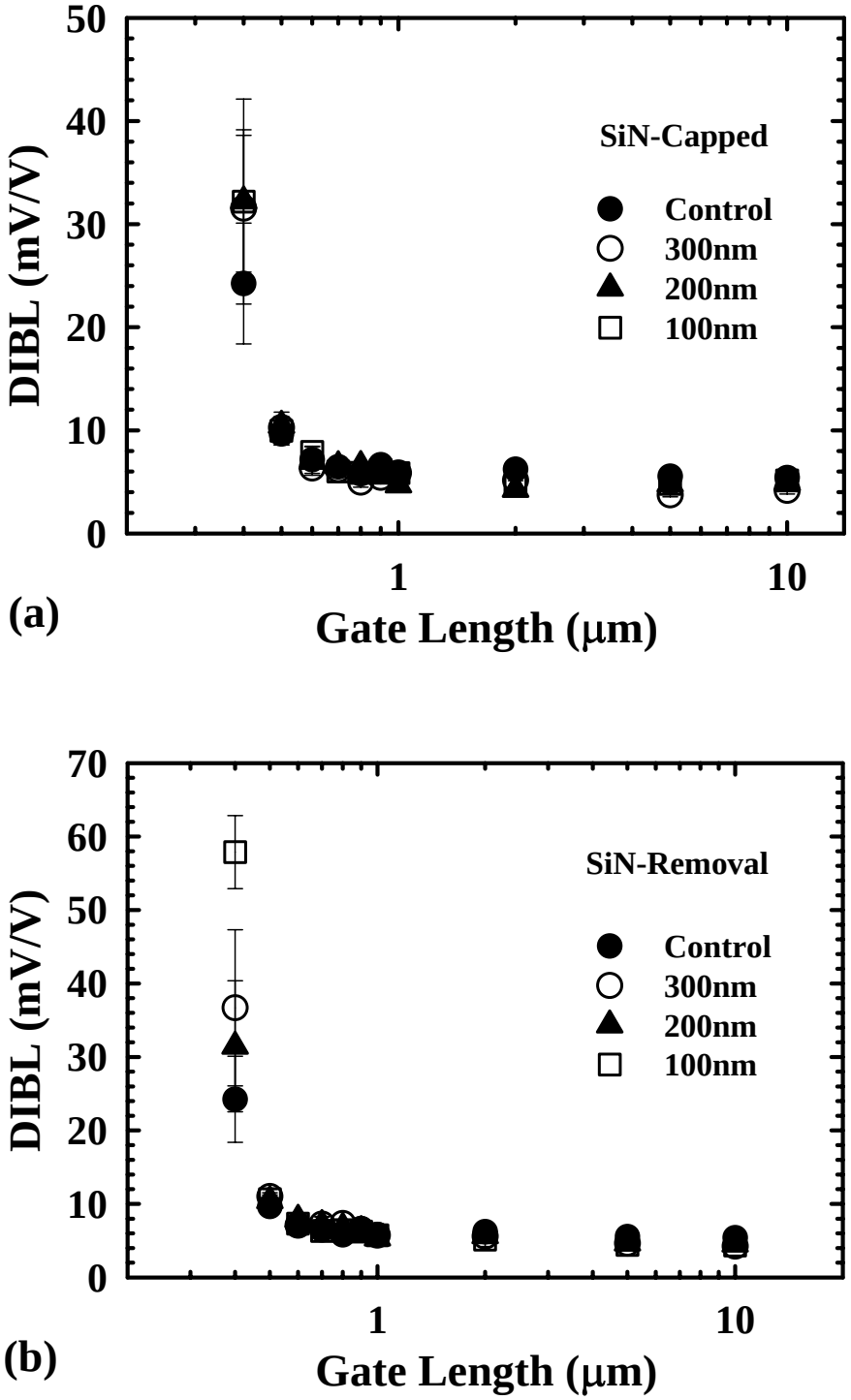


Fig.3.9 Drain induced barrier lowing (DIBL) for different splits of NMOSFETs as a function of channel length. DIBL was evaluated by measuring the drain current change as V_{DS} was increased at some fixed gate voltage below threshold voltage. (a) Control and SiN-capped devices with three different thickness. (b) Control and SiN-removal devices.

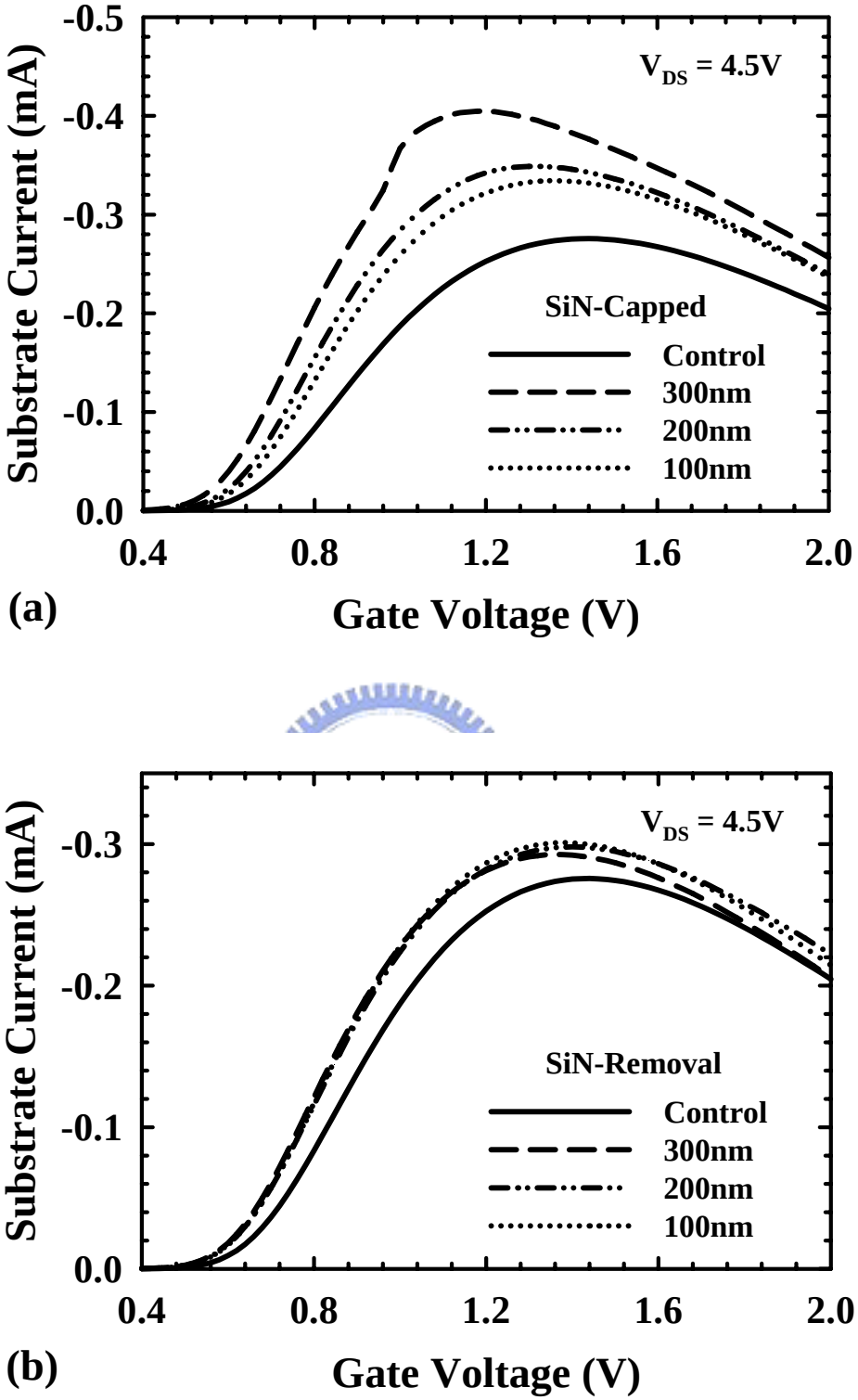


Fig.3.10 Substrate current versus gate voltage for different splits of NMOSFETs.. (a) Control and SiN-capped devices with three different thickness. (b) Control and SiN-removal devices.

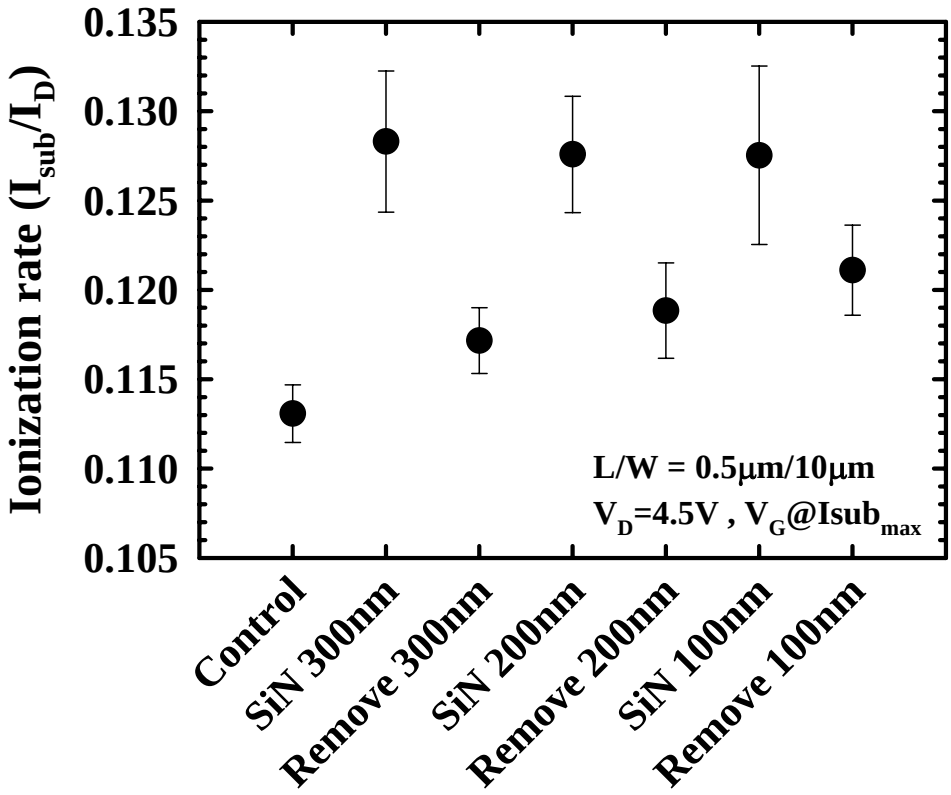


Fig.3.11 Impact ionization rate (I_{sub}/I_D) of different splits of NMOSFETs.

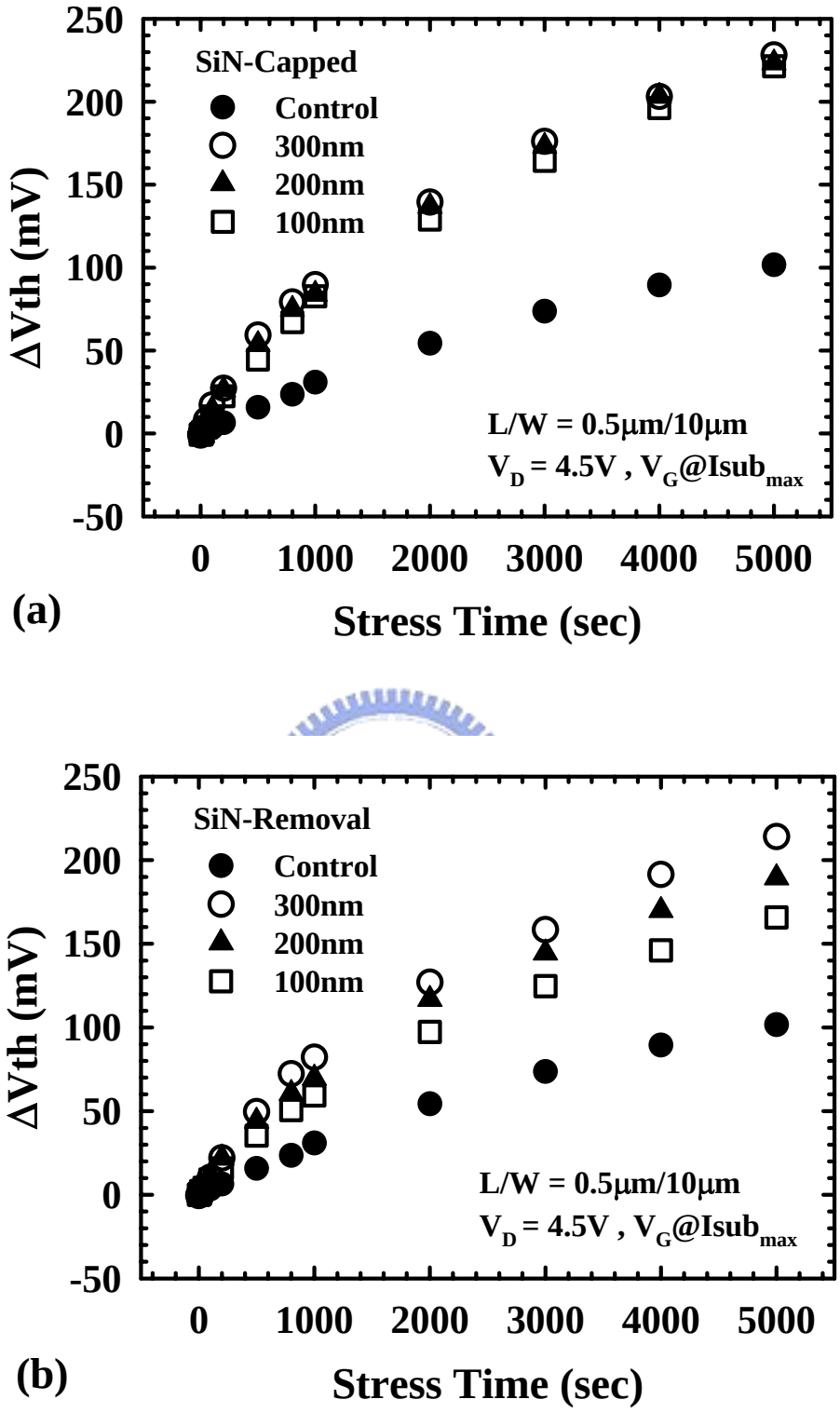


Fig.3.12 Threshold voltage degradation of hot-electron stressing performed at V_{DS} = 4.5 V and V_{GS} at maximum substrate current on all splits of devices with channel length/width = 0.5μm/10μm. (a) Control and SiN-capped devices with three different thickness. (b) Control and SiN-removal devices.

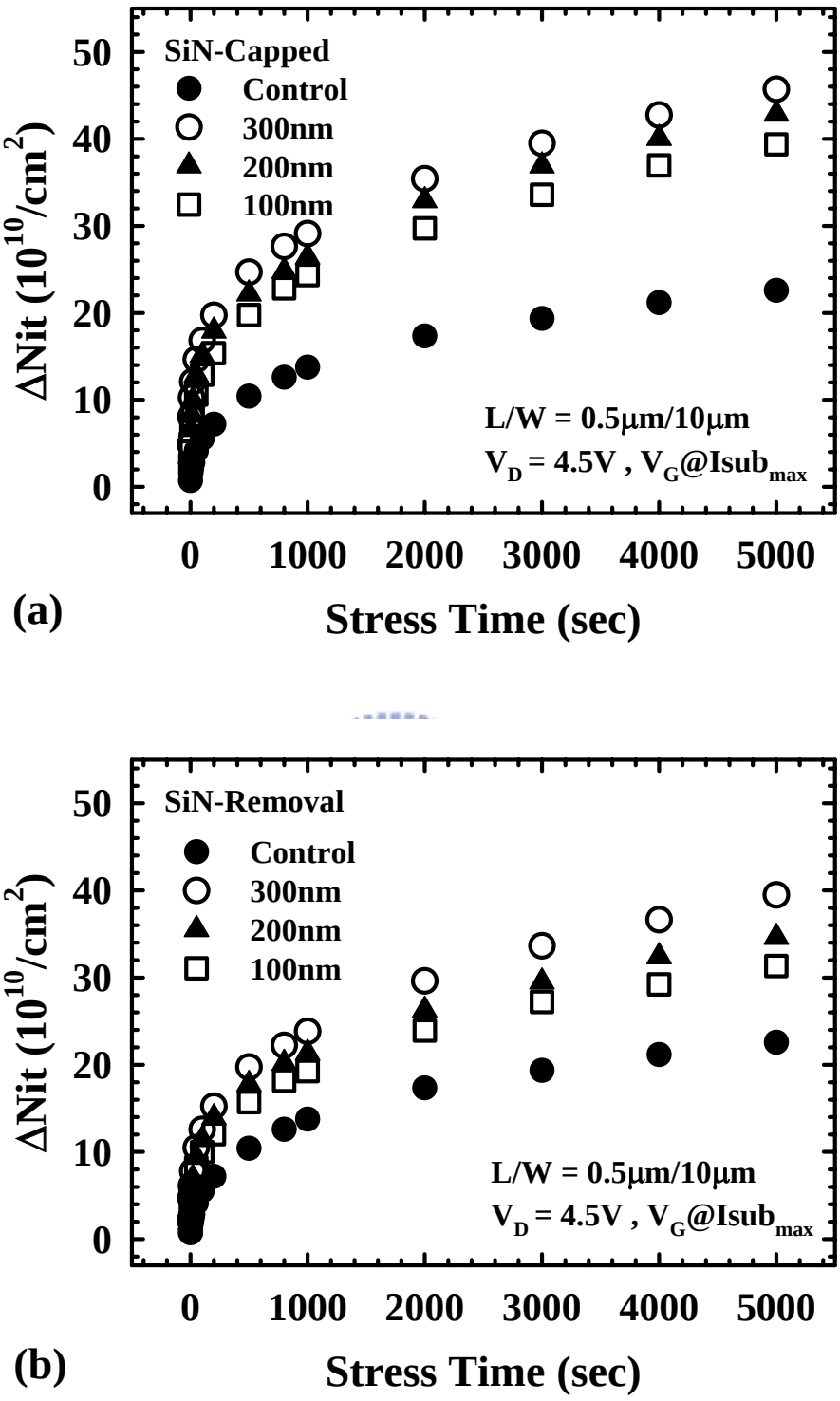
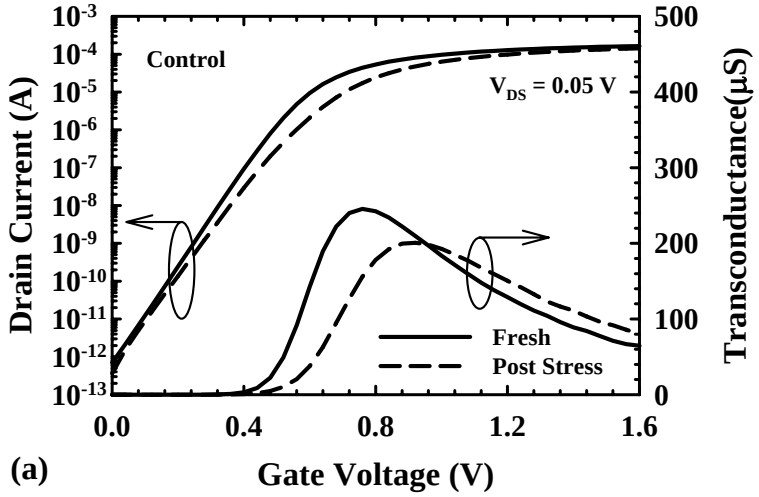
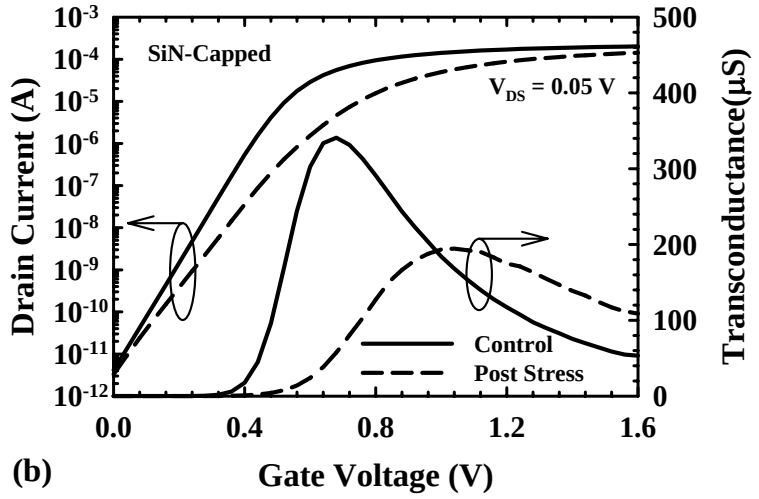


Fig.3.13 Interface trap density degradation of hot-electron stressing performed at V_{DS} = 4.5 V and V_{GS} at maximum substrate current on all splits of devices with channel length/width = 0.5μm/10μm. (a) Control and SiN-capped devices with three different thickness. (b) Control and SiN-removal devices.





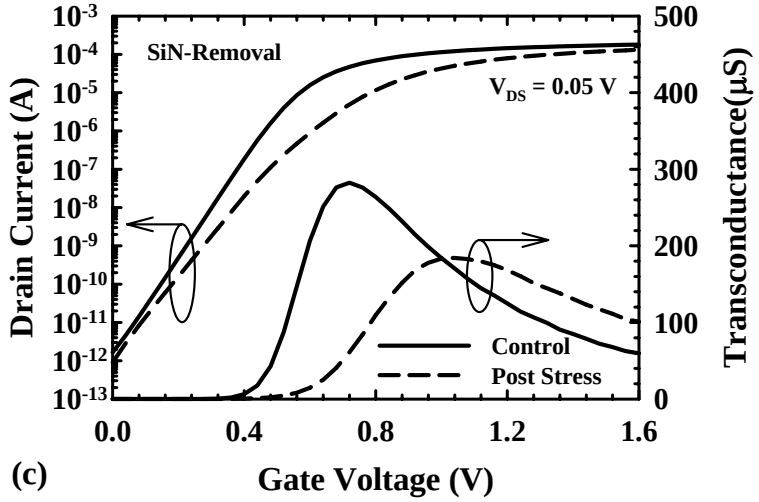


Fig.3.14 Subthreshold characteristics and transconductance of devices before and after 5000 sec hot-electron stressing. Channel length/width = 0.5μm/10μm. (a) Control sample. (b) SiN-Capped sample. (c) SiN-Removed sample.

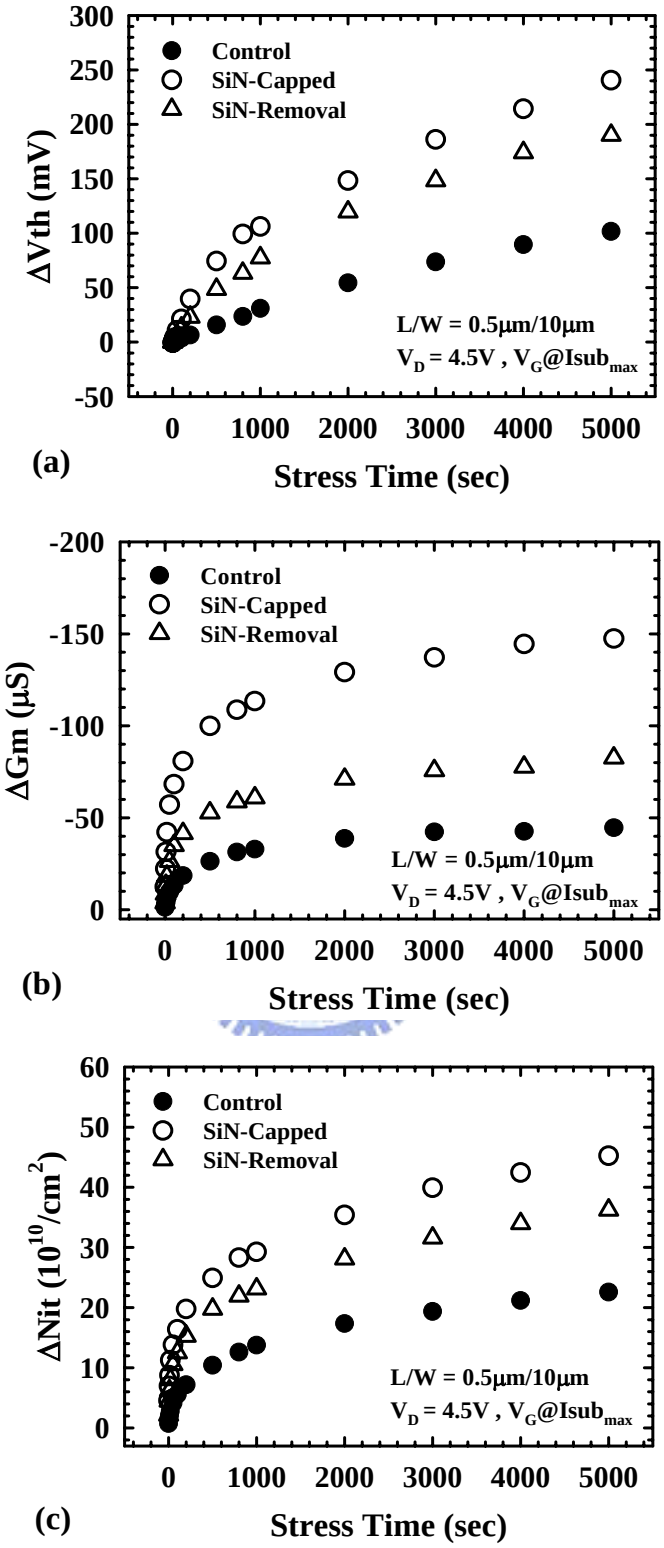


Fig.3.15 Results of hot-electron stressing at V_{DS} = 4.5 V and maximum substrate current performed on three splits (control, SiN 300nm and remove 300nm) of devices with channel length/width = 0.5μm/10μm. (a) Threshold voltage shift; (b) transconductance degradation; (c) interface state generation.

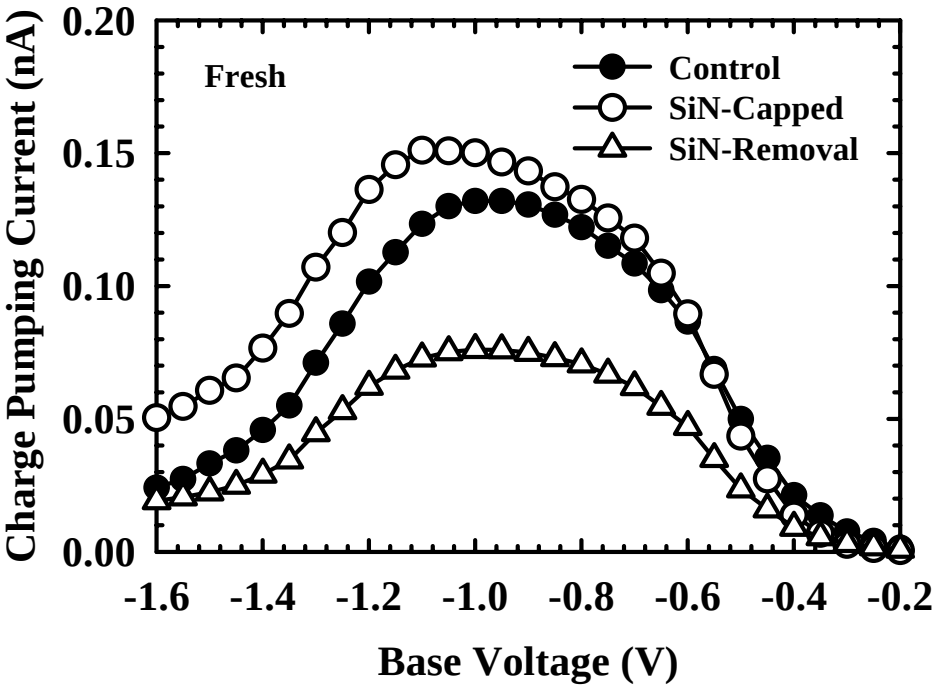


Fig.3.16 Charge pumping current for the three splits of fresh devices with channel length/width = 0.5μm/10μm. The measurement was performed under fixed amplitude of 1.5 V and frequency of 1 MHz.

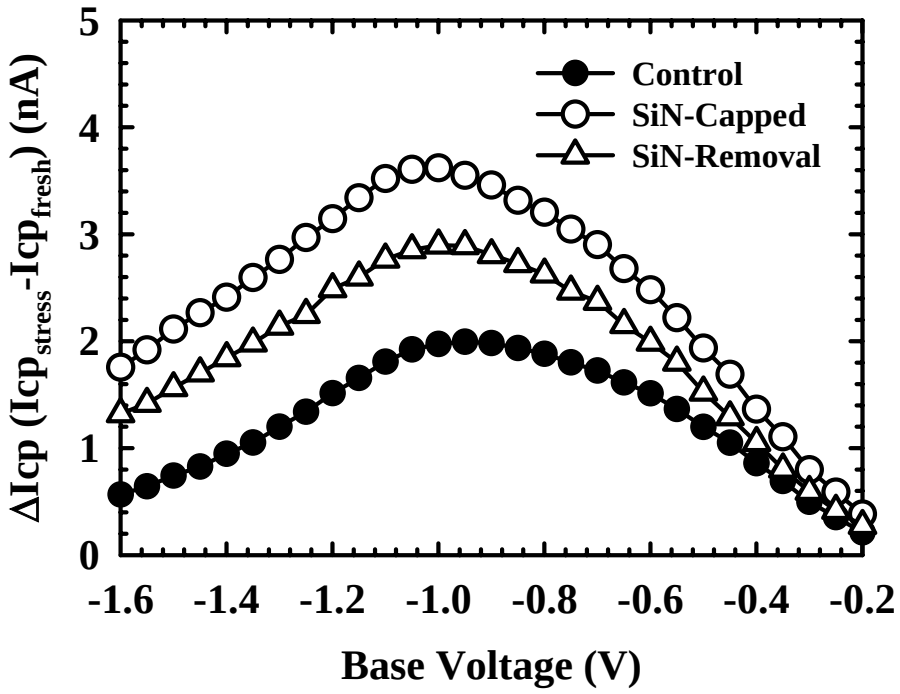


Fig.3.17 The increase in charge pumping current after 5000 second hot carrier stress (V_G@$Isub_{max}$ and V_{DS} = 4.5 V) for the three splits of devices with channel length/width = 0.5μm/10μm.

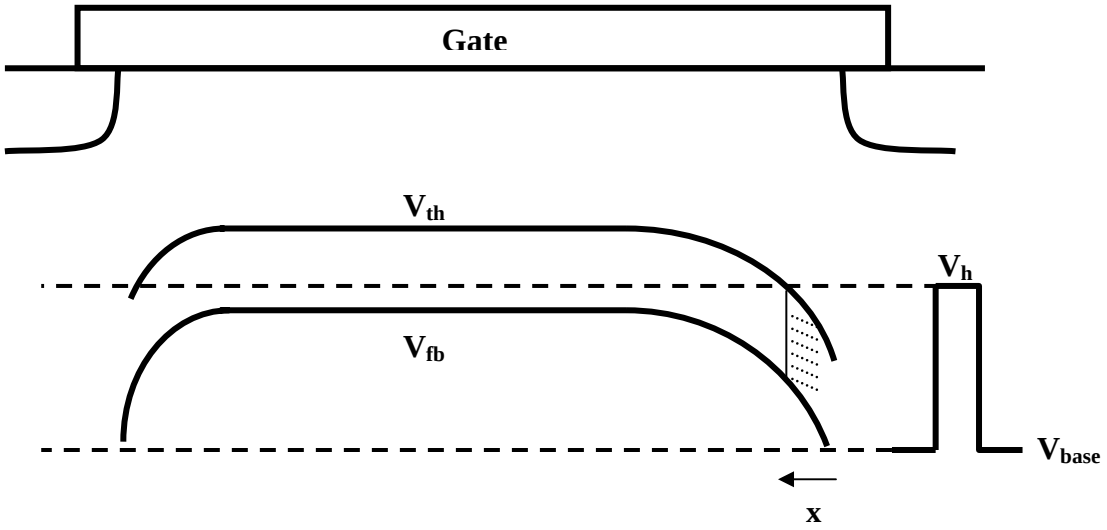


Fig.3.18 Non-uniform distribution of local threshold voltage and flat-band voltage across the device caused by variation of lateral doping concentration.

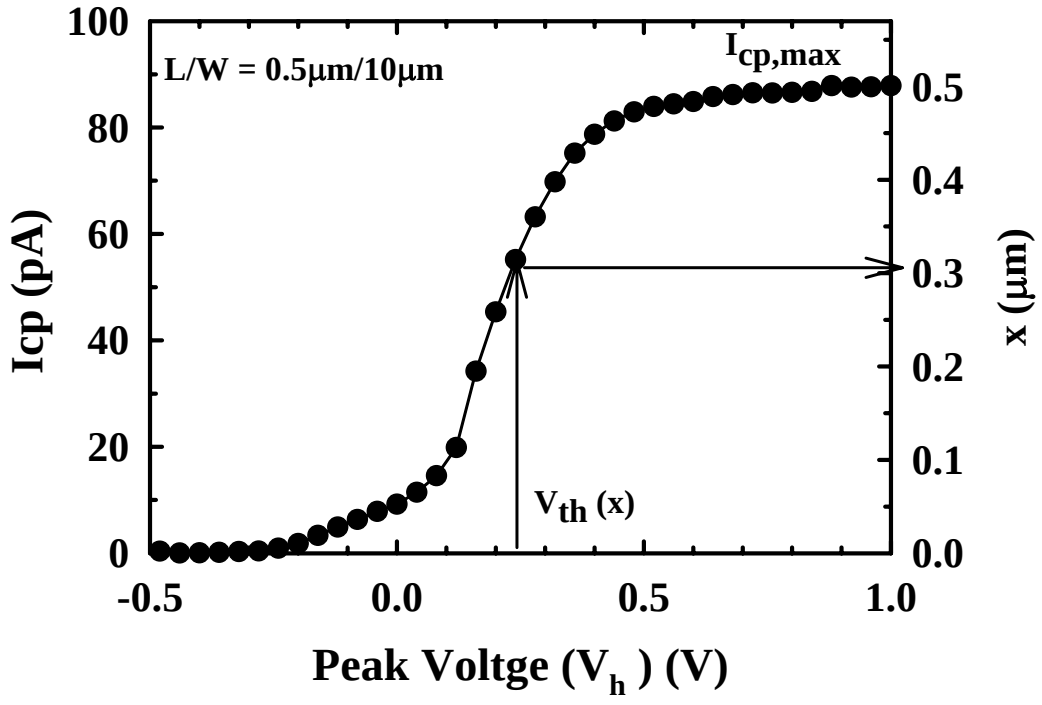


Fig.3.19 Derivation of the relationship between local threshold voltage and lateral distance x from the single-junction charge pumping data of the control device.

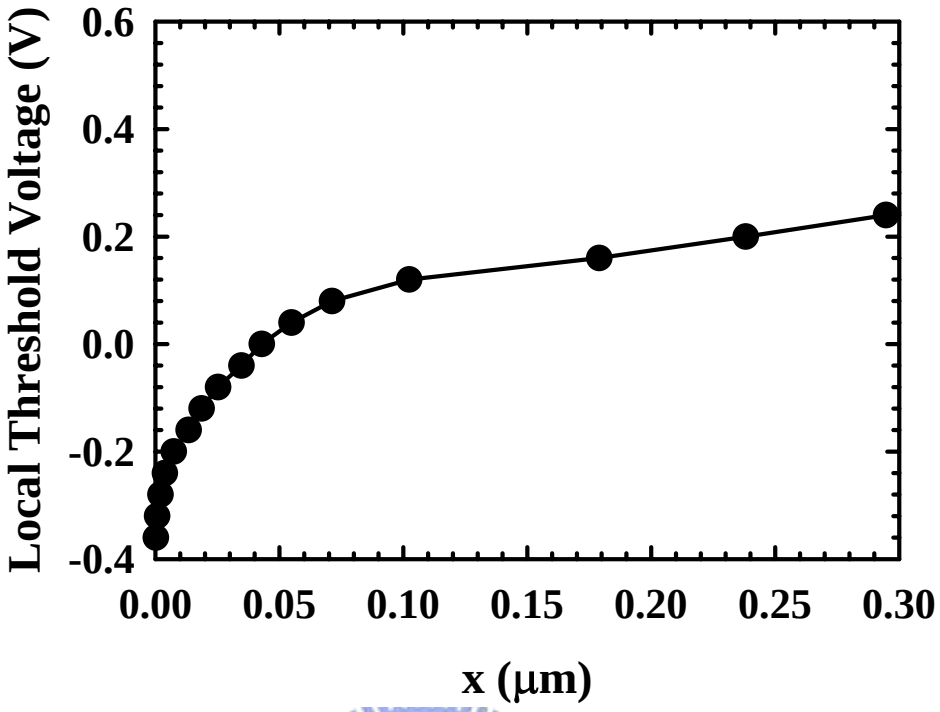


Fig.3.20 Extracted lateral profile of local threshold voltage near the graded drain junction in the control sample.

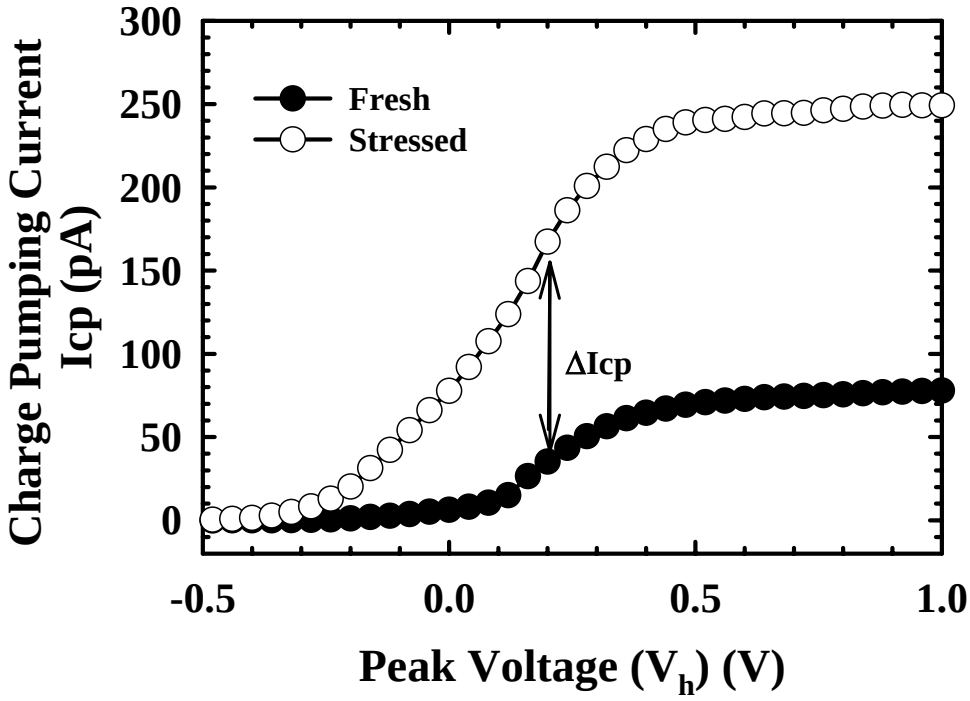


Fig.3.21 Charge pumping current before and after 10 second hot-electron stressing (V_G@$Isub_{max}$ and V_{DS} = 4.5 V). Channel length/width = 0.5μm/10μm.

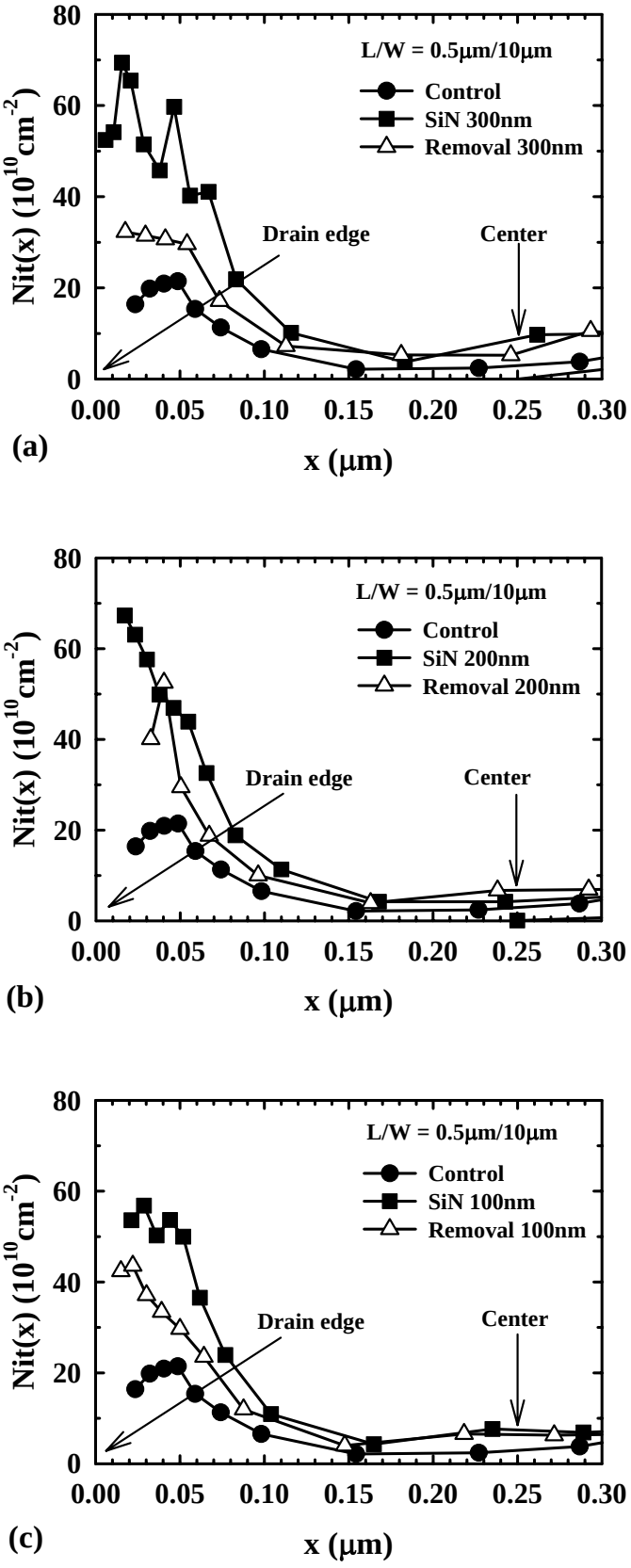


Fig.3.22 Lateral profile of interface state generation under three different SiN capping thickness. (a) 300 nm. (b) 200 nm. (c) 100 nm.

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論文題目：

具有氮化矽覆蓋層之形變 N 型金氧半場效電晶體之元件特性與熱載子退化效應

Device Characteristics and Hot Carrier Degradation of Strained NMOSFETs with SiN Capping Layer