

國立交通大學

電子工程學系 電子研究所

碩士論文

含鍺摻雜氮化矽薄膜在非揮發性記憶體  
應用之研究



**Study on the Application of Ge-Incorporated  
Silicon Nitride Thin Film for Nonvolatile  
Memory**

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指導教授：曾俊元 博士

中華民國九十五年六月

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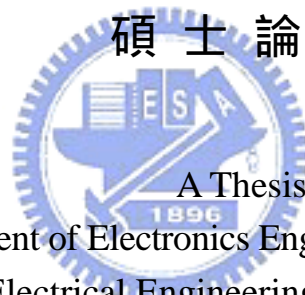
指導教授：曾俊元 博士

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碩士論文



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中華民國九十五年六月

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對最廣為使用的非揮發性記憶體——快閃記憶體而言，通常會遇到兩個瓶頸：一是在元件尺寸繼續微縮下之瓶頸，由於尺寸微縮後穿隧氧化層(或閘極氧化層)之厚度亦隨之下降，如此雖可得到較快的讀寫速度，但電荷保存時間亦隨之下降，故須在兩者之間取得平衡點；二是在多次讀寫後在穿隧氧化層品質容易劣化而產生漏電路徑，一旦有一條產生，所有儲存在浮動閘極(floating gate)的電荷都會經由此漏電路徑而全部流失掉。為了克服上述兩個瓶頸，主要有兩種改良的方法被提出，一是 SONOS 非揮發性記憶體，另一種是奈米晶體(量子點)非揮發性記憶體。

在本文中，一個將前述兩種非揮發性記憶體結合之新記憶體首次被提出。利用矽銻氮(SiGeN)三元薄膜來取代 SONOS 非揮發性記憶體中的氮化矽(Si<sub>3</sub>N<sub>4</sub>)薄膜，並藉由一系列的熱處理後，使銻量子點析出，並被氮化矽所包圍，如此便完成了將兩種記憶體結合之新記憶體。由於銻量子點及包圍銻量子點之氮化矽皆可儲存電荷，故新記憶體的記憶視窗比單純只有銻量子點或氮化矽薄膜來得更為大。在其它條件不變下，擁有大記憶視窗的元件比小記憶視窗的元件更容易達到

十年的電荷保存時間。

此外，乾式氧化及水氣處理步驟在阻擋氧化層形成時所扮演的角色也有進一步之探討。隨著乾式氧化的時間越長，更多的鍺原子會被析出並且聚集成核，因此，在拉曼分析中鍺的訊號也就越強。由於水分子比氧分子小，故水分子比氧分子更容易得鑽入阻擋氧化層(blocking oxide)中並修補阻擋氧化層中的懸鍵(dangling bands),所以，在乾式氧化後多加一個水氣處理的步驟則會改善阻擋氧化層的品質與增強其強度。實驗中發現，30 分鐘短時間乾式氧化後再加上水氣處理的元件，其抗漏電能力和 60 分鐘長時間乾式氧化的元件一樣好，故水氣處理步驟的引入不僅可改善阻擋氧化層的品質，同時，更可大幅的縮減製程所需之時間。

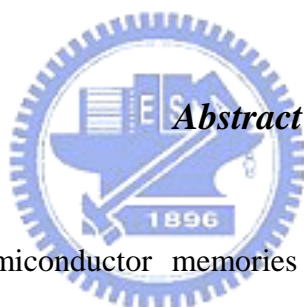


# Study on the Application of Ge-Incorporated Silicon Nitride Thin Film for Nonvolatile Memory

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For nonvolatile semiconductor memories (NVSM), there are two limitations encountered at the present time. (1) The limited potential for continued scaling of the device structure: this scaling limitation stems from the extreme requirements on the tunnel oxide layer. To balance between program/erase speed and retention time, there is a trade-off between speed and reliability for the optimal tunnel oxide thickness. (2) The quality and strength of tunnel oxide (or tunnel dielectric) after plenty of program/erase cycles, once a leaky path has been created in tunnel oxide, all charges stored in the floating gate will be lost. Therefore, two approaches, the silicon-oxide-nitride-oxide-silicon (SONOS) and the nanocrystal nonvolatile memory devices, have investigated to overcome this oxide quality limit of the conventional floating gate NVSM.

A combination of SONOS and nanocrystal NVSM is first proposed in this study. A

SiGeN film is introduced to replace the nitride film in SONOS structure. After several different thermal processes, Ge in the SiGeN film will be segregated to form Ge nanodots embedded in the SiN<sub>x</sub>/SiON film. Because there are two charge-storage node sources, the nodes in Ge nanodots and in SiN<sub>x</sub> dielectric film, comparing to SONOS and Ge nanocrystal NVMs, a larger memory window can be obtained. When a memory device has a larger memory window, it is easier to meet the requirement of 10-year retention. And, we hope this approach can improve the two limitations mentioned above.

Besides, the roles of dry oxidation and steam treatment during blocking oxide formation are also considered. With the extension of dry oxidation time, the Ge signal in Raman spectrum increases gradually because there are more Ge atoms to be segregated from the SiGeN film and more time for Ge atoms to nucleate. A 3-minute steam treatment is performed after 30 minutes dry oxidation. Owing to its smaller size and lower activation energy than O<sub>2</sub> molecules, H<sub>2</sub>O molecules are more permeable through the blocking oxide and can passivate dangling bonds in the blocking oxide. The purpose of steam treatment is to strengthen the blocking oxide and improve its quality. The I-V characteristic of the sample after 30 minutes dry oxidation plus 3 minutes steam treatment is comparable with that after 60 minutes long term dry oxidation. The introduction of steam treatment can not only improve the blocking oxide quality but also reduce the thermal process duration from 60 minutes to 33 minutes.

## 誌謝

兩年時光匆匆地逝去，轉眼間就到了離別的時候了，在這段期間的師長朋友們，在我的心中對你們總是抱著無限的感激。

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# Chapter 1

## Introduction

### 1.1 General Background

In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory (or flash memory) at Bell Labs [1.1]. To date, the flash memory device structure, as shown in Fig. 1-1, continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both standalone and embedded memories. The invention of flash memory creates a huge industry of portable electronic devices such as cellular phones, digital cameras, digital voice recorders, MP3 walkman, personal data assistants to compact smart cards, USB flash personal disc etc.

Although a huge commercial success, conventional FG devices have their limitations. Two of the most prominent limitations are: (1) the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer. The tunnel oxide must be thin enough to allow quick and efficient charge transport to and from FG. On the other hand, the tunnel oxide needs to provide superior isolation under retention, endurance, and disturbed conditions in order to maintain information integrity over periods of up to a decade. When the tunnel oxide is thinner for operation speed consideration, the retention characteristics may be degraded. And when the tunnel oxide is made thicker to take the isolation into account, the speed of the operation will be slower. Therefore, for mass production, there is a trade-off between speed and reliability for the optimal tunnel oxide thickness. (2) the quality and strength of tunnel oxide (or tunnel dielectric) after



plenty of program/erase cycles. Once a leaky path has been created in tunnel oxide, all the charges stored in the floating gate will be lost. Therefore, two suggestions, SONOS [1.2-1.4] and nanocrystal nonvolatile memory devices [1.5-1.7], are proposed to overcome this oxide quality limit of the conventional FG structure. These technologies replace the floating gate structure with a great number of charge-storage nodes in the dielectric or in the nanocrystal. Unlike the floating gate, stored charges in isolated nodes cannot easily redistribute amongst themselves and the local leaky path will not cause the fatal loss of information for the nanocrystal nonvolatile memory device. This effectively prevents the leakage of all the stored charges out of the floating gate.

### ***1.1.1 SONOS nonvolatile memory devices***

SONOS (silicon-oxide-silicon-oxide-silicon) nonvolatile memory devices structure shown in Fig. 1-2, the charge storage elements in SONOS memory are the charge traps distributed throughout the volume of the  $\text{Si}_3\text{N}_4$  layer. A typical trap has a density of the order  $10^{18}$ - $10^{19}$   $\text{cm}^{-3}$  according to Yang et al [1.8] and stores both electrons and holes (positive charges) injected from the channel.

Figure 1-3 illustrates the progression of device cross section, which has led to the present SONOS device structure. The nitride-base memory devices were extensively studied in the early 70s after the first metal-gate nitride device MNOS (Metal/Nitride/Oxide/Silicon) was reported in 1967 by Wegener et al [1.9]. Initial device structures in the early 1970s were p-channel metal-nitride-oxide-silicon (MNOS) structures with aluminum gate electrodes and thick (45 nm) silicon nitride charge storage layers. Write/erase voltages were typically 25-30 V. In the late 1970s and early 1980s, scaling moved to n-channel SNOS devices with write/erase voltages of 14-18 V. In the late 1980s and early 1990s, n- and p-channel SONOS devices emerged with write/erase voltages of 5-12 V. In the SONOS device, an oxide layer is introduced

between the gate and the nitride region. Thus, it forms the ONO ( $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ ) gate dielectric stack (Fig. 1-2) instead of capping the nitride layer with just a metal or semiconductor gate. The purpose of the top blocking oxide is to reduce the charge injection from the control gate into the nitride layer, limiting the memory window of both MNOS and SNOS devices.

The program/erase mechanism is shown in Fig. 1-4. During programming, the control gate is biased positively so that electrons from the channel can tunnel across the  $\text{SiO}_2$  into the nitride layer. Some electrons will continue to move through the nitride layer then across the control oxide finally into the control gate. The remaining trapped charges in the nitride layer provide the electrostatic screening of the channel from the control gate. Therefore, there is a threshold voltage ( $V_T$ ) shift resulting from trapped charges in nitride and because of that SONOS can be used as a memory device just like conventional floating gate devices.

### ***1.1.2 Nanocrystal nonvolatile memory devices***

Nanocrystal nonvolatile memories, shown in Fig. 1-5, are one particular implementation of storing charges by dielectric-surrounded nanodots, and were first introduced in the early 1990s by IBM researchers who proposed flash memory with a granular floating gate made from silicon nanocrystals [1.10]. In a nanocrystal NVSM (nonvolatile semiconductor memory) device, charge is not stored on a continuous FG poly-Si layer, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or dots. Each dot will typically store only a handful of electrons; collectively the charges stored in these dots control the channel conductivity of the memory transistor.

As compared to conventional stacked gate NVSM devices, nanocrystal charge storage offers several advantages, the main one being the potential to use thinner tunnel

oxide without sacrificing nonvolatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results not only from the distributed nature of the charge storage, which makes the storage more robust and fault-tolerant, but also from the beneficial effects of Coulomb blockade [1.11]. Quantum confinement effects (bandgap widening; energy quantization) can be exploited in sufficiently small nanocrystal geometries (sub-3 nm dot diameter) to further enhance the memory's performance.

Due to the less drain to FG coupling, nanocrystal memories suffer less from drain induced barrier lowering (DIBL). One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time. Of particular importance is the low capacitive coupling between the external control gate and the nanocrystal charge storage layer. This does not only results in higher operating voltages, thus offsetting the benefits of the thinner tunnel oxide, but also removes an important design parameter (the coupling ratio) typically used to optimize the performance and reliability tradeoff.

Unlike volume distributed charge traps (ex: nitride in SONOS NVM), nanocrystals be deposited in a two-dimensional 2-D) layer at a fixed distance from the channel separated by a thin tunnel oxide (Fig. 3). By limiting nanocrystals deposition to just one layer and adjusting the thickness of the top blocking dielectric, charge leakages to the control gate from the storage nodes can be effectively prevented.

## 1.2 Motivation

for Semiconductors (ITRS) indicates the difficult challenge, beyond the year 2005, for nonvolatile semiconductor memories is to achieve reliable, low-power, low-voltage performance [1.12]. For nonvolatile flash memories, two limitations encountered at the present time are: (1) the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirements put on the tunnel oxide layer. In order to get balance between program/erase speed and retention time, there is a trade-off between speed and reliability to get the optimal tunnel oxide thickness. (2) the quality and strength of tunnel oxide (or tunnel dielectric) after plenty of program/erase cycles. Once a leaky path has been created in tunnel oxide, all the charges stored in the floating gate will be lost. Therefore, two suggestions, the SONOS and the nanocrystal nonvolatile memory devices, are proposed to overcome this oxide quality limit of the conventional FG structure. These technologies replace the floating gate structure with a great number of charge-storage nodes in the dielectric or in the nanocrystal. Unlike the floating gate, the local leaky path will not cause the fatal loss of information for the nanocrystal nonvolatile memory device. This effectively prevents the leakage of all the stored charges out of the floating gate.

In this thesis, a combination of SONOS and nanocrystal nonvolatile memory devices is proposed. A SiGeN film is introduced to replace the nitride film in SONOS structure. After several different thermal processes, Ge in the SiGeN film will be segregated to form Ge nanodots embedded in the SiN<sub>x</sub> (or SiON) film. Because there are two charge-storage node sources, the nodes in Ge nanodots and in SiN<sub>x</sub> dielectric film, comparing to SONOS and Ge nanocrystal NVMs, a larger memory window can be obtained. When a memory device has a larger memory window, it is easier to meet the requirement of retention of 10 years. And, hope to solve the two limitations mentioned above.

### **1.3 Organization of This Thesis**

**In chapter 1**, general background of flash nonvolatile memory, SONOS nonvolatile memory and nanocrystal nonvolatile memory devices is introduced.

**In chapter 2**, basics of program and erase operation are introduced.

**In chapter 3**, sample structure, experimental methods and experimental process flow are stated.

**In chapter 4**, discuss the SiN<sub>x</sub>:Ge memory electric characteristics, reliabilities, mechanism of Ge dot formation in SiGeN film and role of steam treatment..

Finally, the conclusion is presented **in chapter 5**



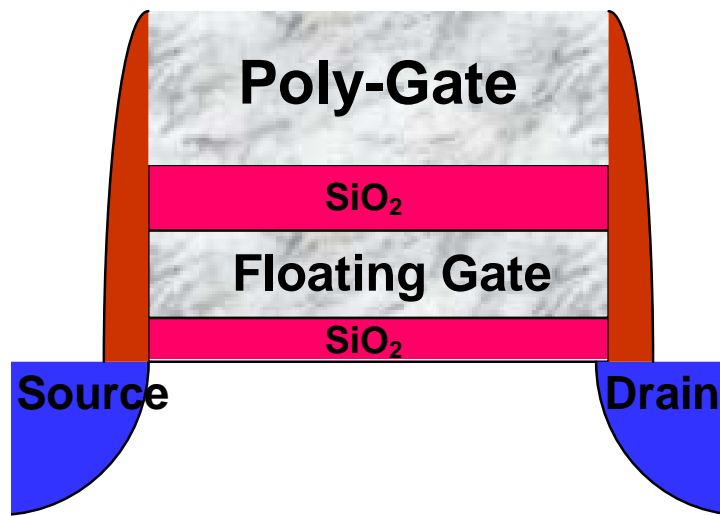


Fig.1-1 The device structure of conventional nonvolatile semiconductor memory.

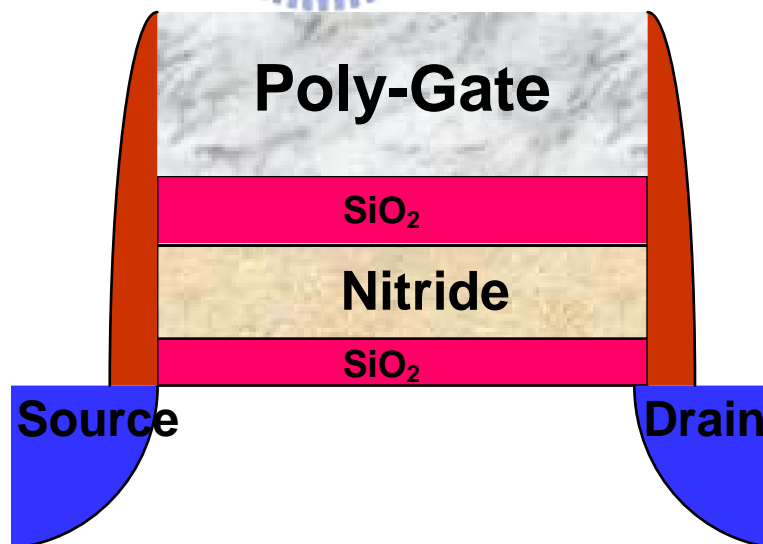


Fig.1-2 The device structure of SONOS nonvolatile memory.

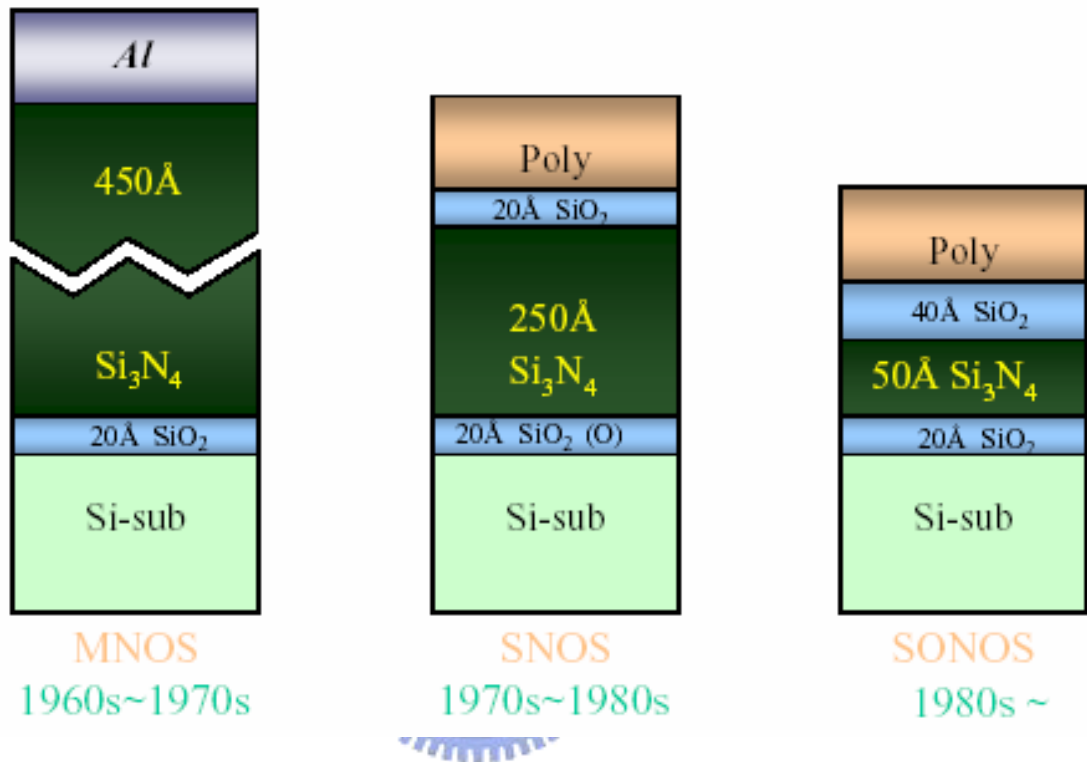


Figure 1-3 The development of the gate stack of SONOS EEPROM memory devices. The optimization of nitride and oxide films has been the main focus in recent years.

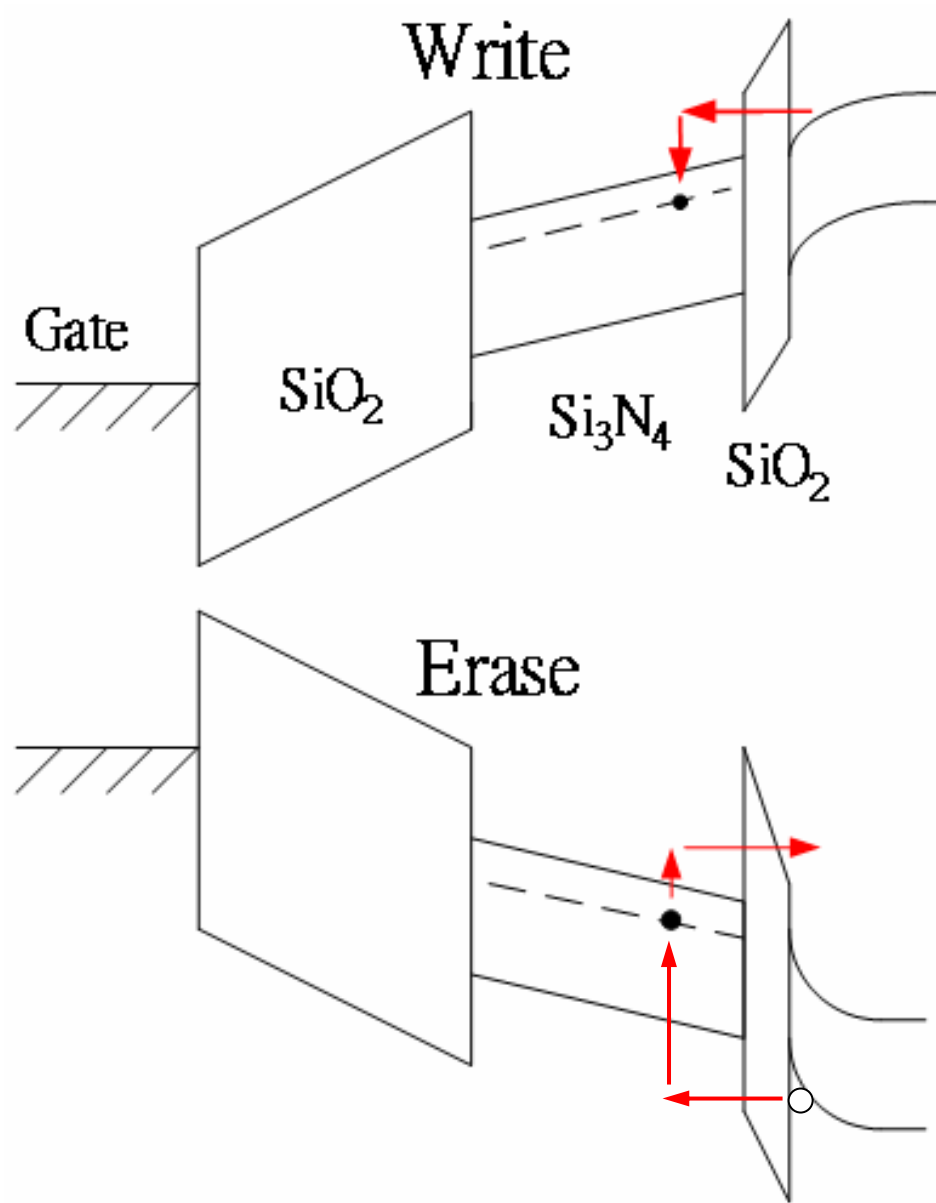


Figure 1-4 The energy band diagrams of the write/erase operation for a SONOS device.



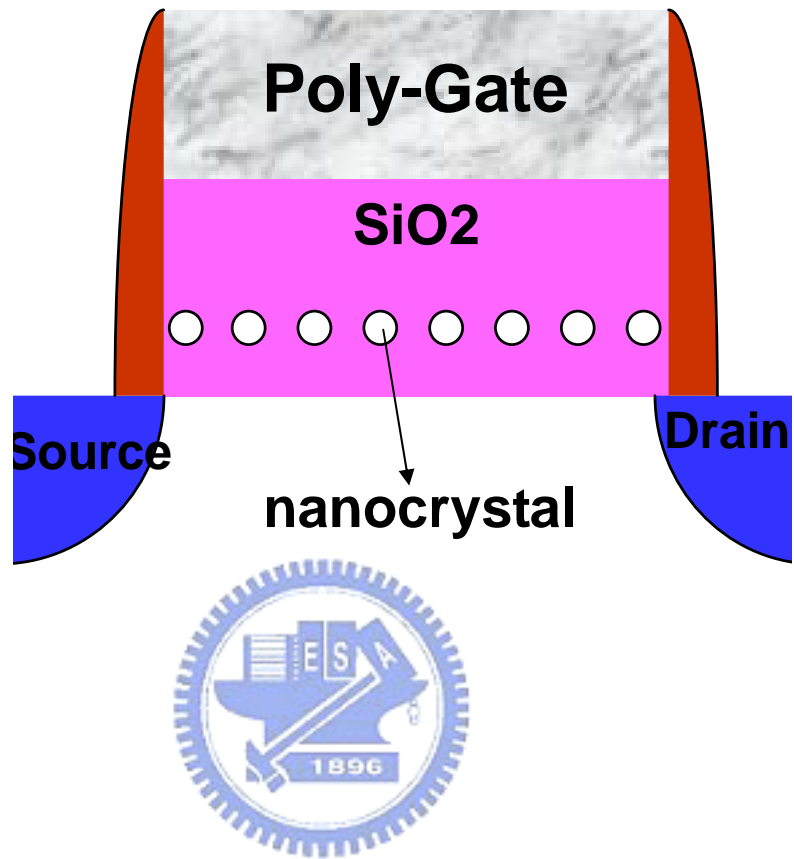


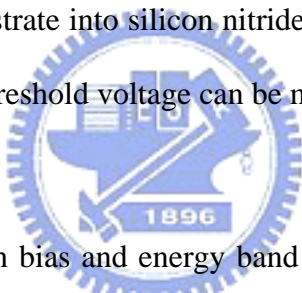
Figure 1-5 The device structure of nanocrystal (nano-dots) nonvolatile memory.

## Chapter 2

### Basics principle of nonvolatile memory

#### 2.1 Introduction

For SONOS NVSM, the basics operating principle of ONO structure is that electrons injected from the channel are trapped in the forbidden gap of the silicon nitride film during the program operation. On the other hand, during the erase operation, holes are injected from the substrate into silicon nitride film. If there are charges stored in the silicon nitride film, the threshold voltage can be modified to switch between two distinct values. [2.1]



The relation between bias and energy band bending is a key to understand basics program and erase mechanisms. Fig 2-1 shows energy band diagram of MONOS. The barrier of  $\text{SiO}_2$  is about 3.1 eV for electrons in the conduction band of silicon, and 4.78 eV for holes in valance band. The barrier of  $\text{Si}_3\text{N}_4$  is about 1.05 eV for electrons in the conduction band of nitride, and 2.85 eV for holes in valance band, the gap for electron between conduction band and trapping level is 0.7 eV, and, for hole between valance band and trapping level is 0.95 eV.

In this chapter, we will discuss program and erase mechanisms from the relation between bias and energy band bending. Fowler-Nordheim Tunneling, hot electron injection, band to band assisted hole injection, channel hole injection will be discussed briefly.

## 2.2 Basic program mechanisms

### 2.2.1 Fowler-Nordheim Tunneling

Fowler-Nordheim tunneling is a field-assisted carrier tunneling mechanism [2.2], when a large positive voltage is applied across a metal-ONO-substrate structure, its band structure will be influenced as indicated in figure 2-2. Due to high electrical field, electrons in the poly-Si conduction band as triangular energy barrier with a width dependent on applied electric field. At sufficient high fields, the width of barrier becomes small enough to tunnel through the barrier from the poly-Si conduction band into nitride electron trap layer.

### 2.2.2 Hot electron injection

At large drain bias, the minority carriers that flow in the channel are heated by the large electric fields occurred at the drain side of the channel and their energy distribution is shifted higher. This phenomenon gives rise to impact ionization at the drain, by which both minority and majority carriers are generated. The highly energetic majority carriers are normally collected at the substrate contact and from the so-called substrate current. The minority carriers heating occurs when some of the minority carriers gain enough energy to allow them to surmount the SiO<sub>2</sub> energy barrier. If the oxide field favors injection, these carriers injected over the barrier into the gate insulator and give rise to the so-called hot-carrier injection gate current [2.3-2.4]. Figure 2-3 shows the phenomenon of hot electron injection. This mechanism is schematically represented for the case of an n-channel nonvolatile memory.

In MOS devices, the drain voltage should increase beyond the saturation voltage

$V_{dsat}$  ( $V_d > V_{dsat}$ ), the mode can be named hot carrier effect. To distinguish from Fowler-Nordheim tunneling, the definition of hot carrier injection in this study is the only condition that the drain is applied bias.

## **2.3 Basic erases mechanisms**

There are three physical mechanisms that can be potentially responsible of erase method in nonvolatile memory with ONO structure, as indicated in figure 2-4. (1) electron escape from the nitride by tunneling through top and bottom oxides; (2) tunneling of holes generated by band-to-band into the nitride layer; and (3) the injection into the nitride of hot holes [5]. Electron almost can't escape from the nitride for the nitride deep trap. Holes injection is the dominate mechanism in erase operation. In this study, we'll discuss erase operation from this view.

### ***2.3.1 Fowler-Nordheim Tunneling***

Fowler-Nordheim tunneling is a field-assisted electron tunneling mechanism, when a large negative voltage is applied across a metal-ONO-substrate structure, its band structure will be influenced as indicated on Figure 2-5. Due to high electrical field, holes in the poly-Si valance band as triangular energy barrier with a width dependent on applied electric field. At sufficient high fields, the width of barrier becomes small enough to tunnel through the barrier from the poly-Si valance band into nitride hole trap layer.

### ***2.3.2 Band to band assisted hole injection***

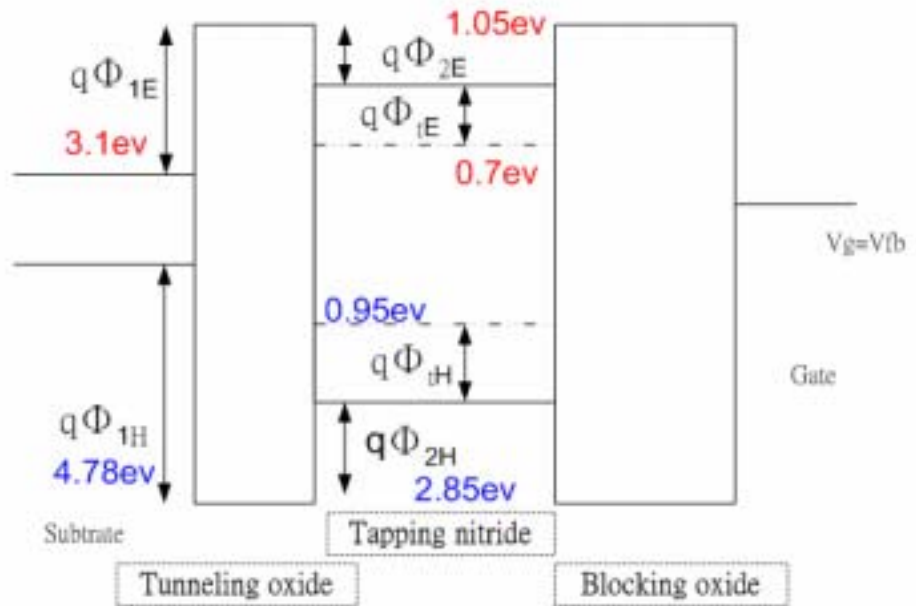
In N-channel, when a negative gate voltage and a positive drain voltage are applied

to the cell, electron-hole pairs are generated by BTBT in the drain region [2.6, 2.7]. The holes are accelerated by a lateral electric field toward the channel region and some of them obtain high energy. The injection of such hot holes [2.8] into nitride through the tunnel oxide is used for a new erase operation in N-channel.

### ***2.3.3 Hot hole injection***

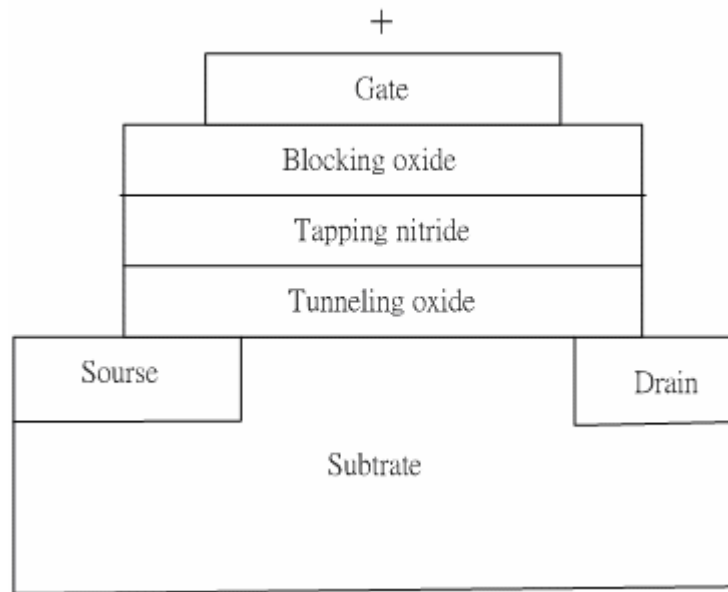
The mechanism of hot hole injection in P-channel is like to hot electron injection. Figure 2-7 shows the phenomenon of hot hole injection. It's reported that hole injection is a erase operation in P-channel device [2.9].



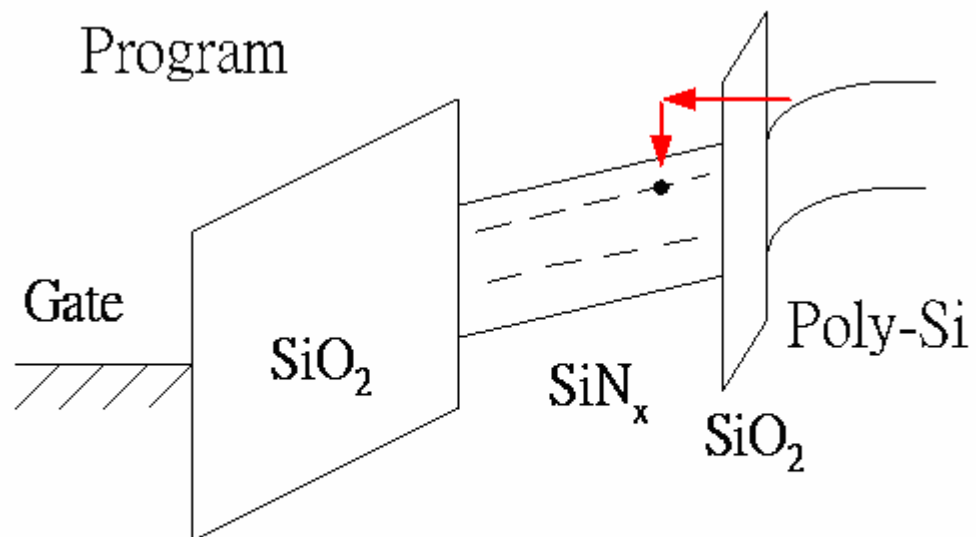


$$\begin{aligned}
 q\Phi_{1E} &= 3.1\text{ev} \\
 q\Phi_{1H} &= 4.78\text{ev} \\
 q\Phi_{2E} &= 1.05\text{ev} \\
 q\Phi_{2H} &= 2.85\text{ev} \\
 q\Phi_{tE} &= 0.7\text{ev} \\
 q\Phi_{tH} &= 0.95\text{ev}
 \end{aligned}$$

Figure 2-1 Energy band diagram of MONOS

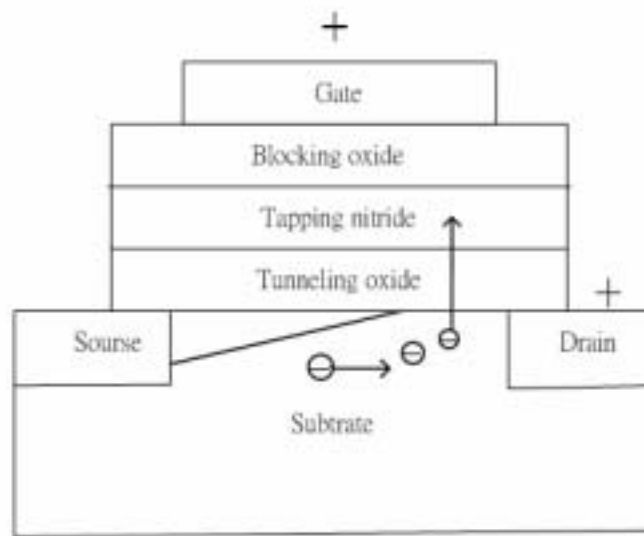


(a)

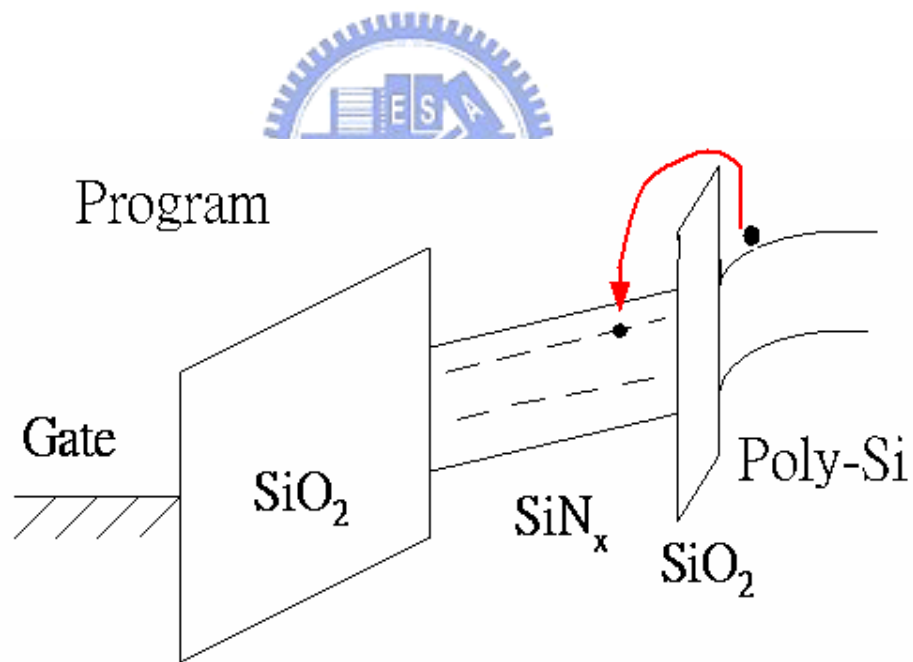


(b)

Figure 2-2 (a) Positive gate voltage applied when use Fowler-Nordheim tunneling to program (b) Energy band representation of Fowler-Nordheim tunneling. Electron in poly-Si conduction band tunnel through the triangular energy barrier.



(a)



(b)

Figure 2-3 (a) Positive gate voltage and Positive drain voltage applied when use hot carrier injection to program (b) Energy band representation of hot carrier injection



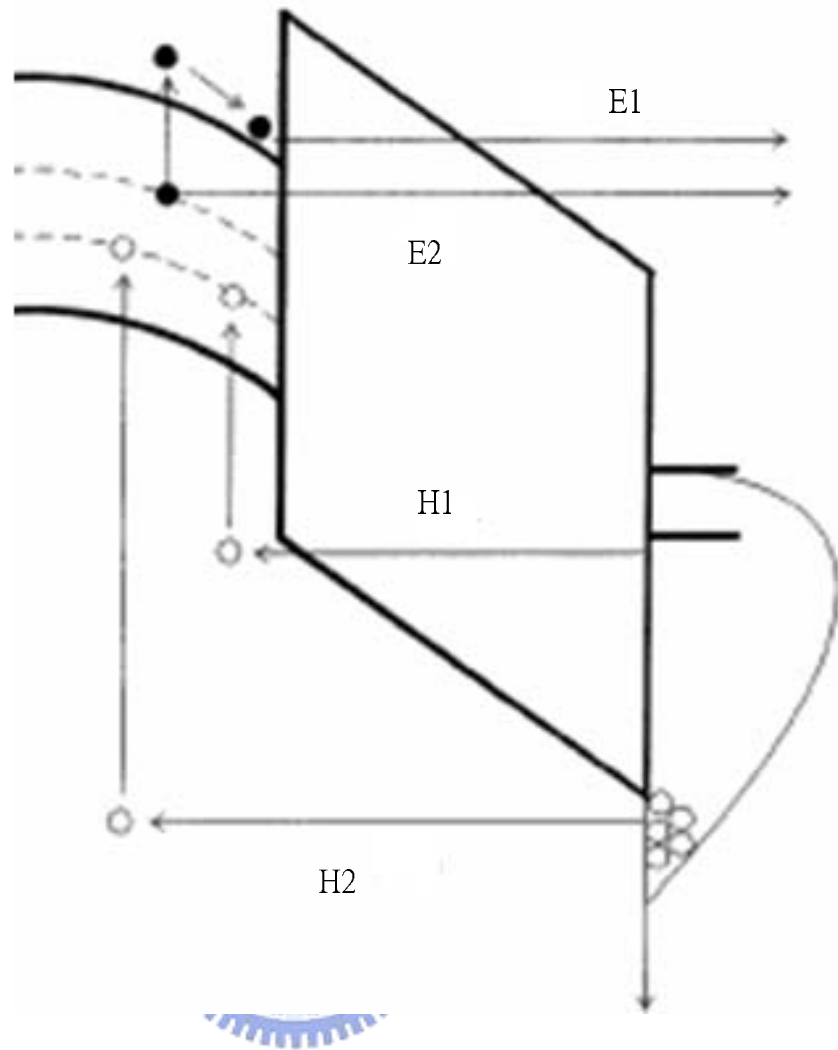
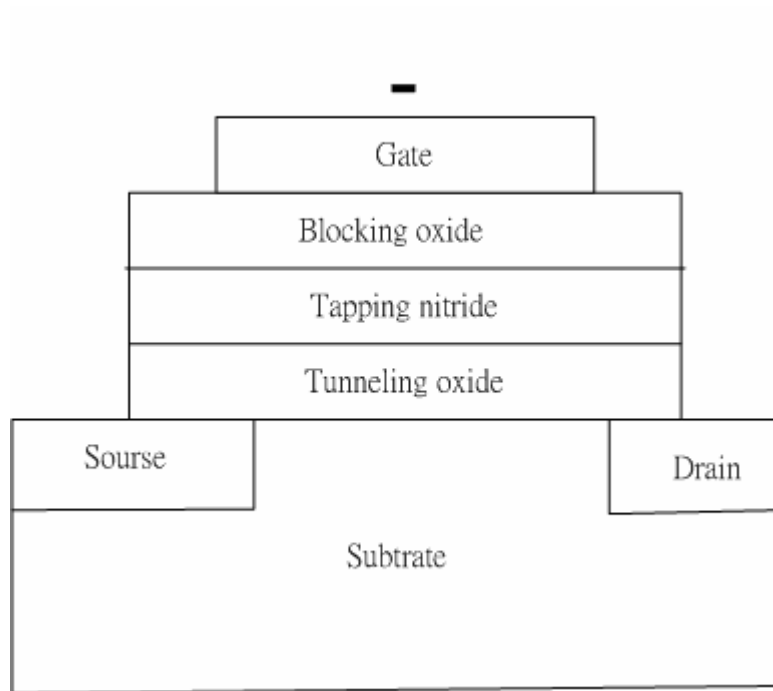
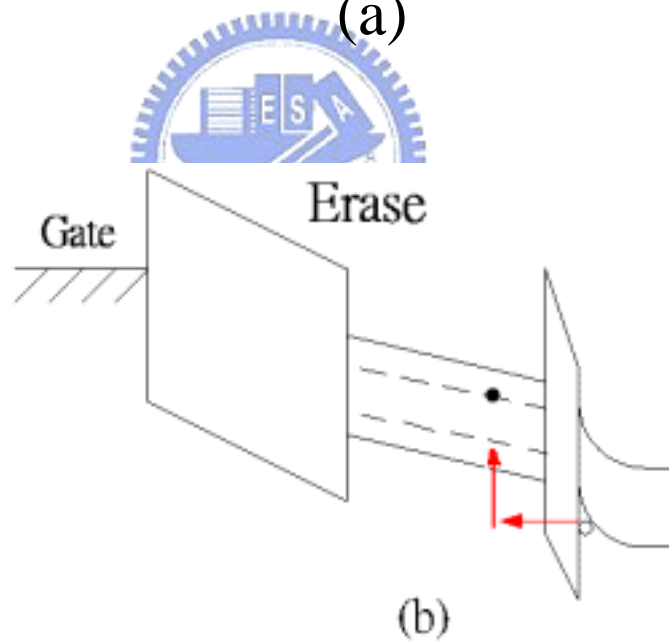


Figure 2-4 Schematic diagram sketching the possible MONOS erase mechanisms :  
 electron tunneling through tunneling oxides (E1), electron emission in the nitride and  
 subsequent tunneling through tunneling oxides (E2), hole tunneling into the nitride (H1),  
 injection of hot holes into the nitride (H2).



(a)



(b)

Figure 2-5 (a) Negative gate voltage applied when use Fowler-Nordheim tunneling to erase (b) Energy band representation of Fowler-Nordheim tunneling to erase.

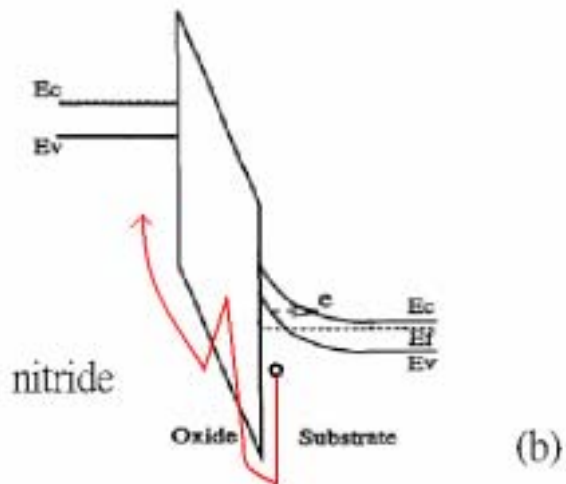
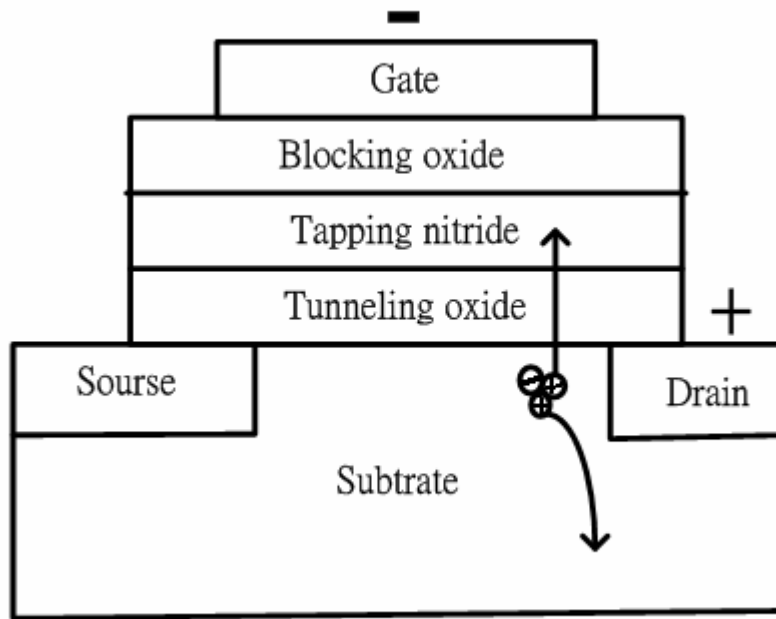


Figure 2-6 (a) Negative gate voltage applied when use band-to-band assisted injection to erase (b) Energy band representation of band to band assisted hole injection to erase.

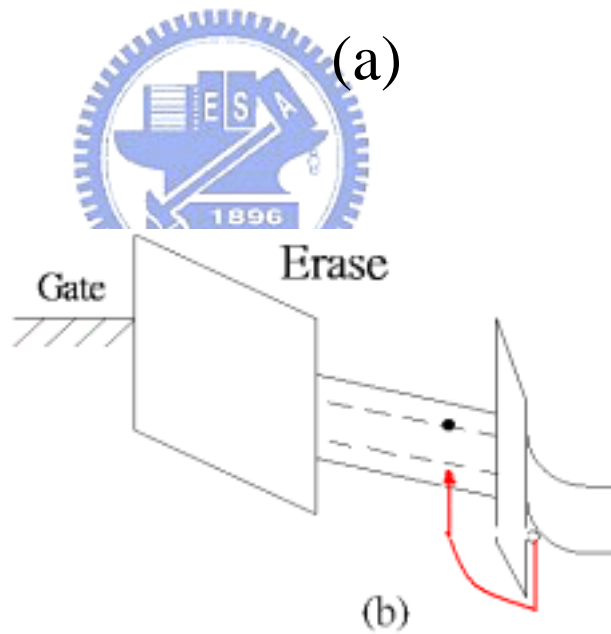
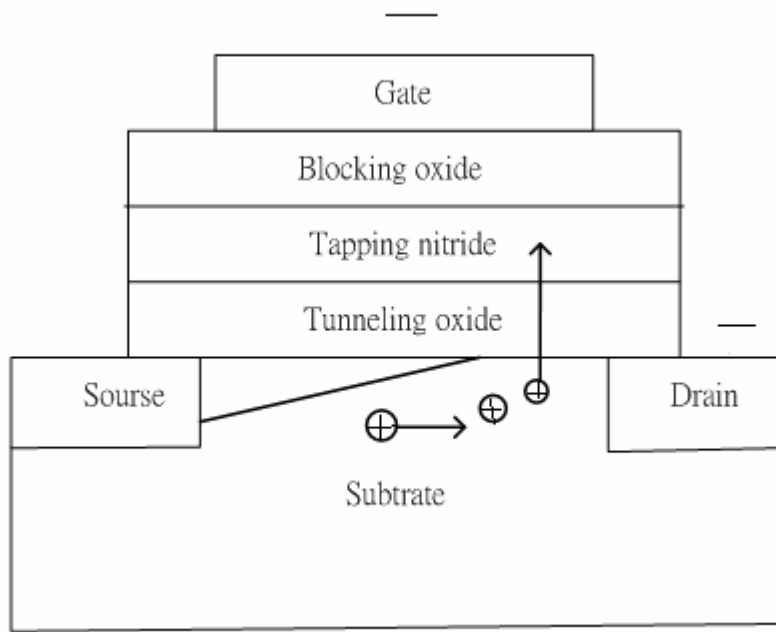


Figure 2-7 (a) Negative gate voltage and negative drain voltage applied when use hot hole injection to erase. (b) Energy band representation of hot hole injection to erase.

# Chapter 3

## Sample Structure and Thermal Process

### 3.1 Sample Structure

Figure 3-1 (a) and (b) show the two different pre-thermal sample structures, labeled as sample I and sample II, in this experiment. The transmission electron microscope (TEM) diagrams are shown in Fig. 3-2 and Fig. 3-3.

First, a 5-nm thermal oxide was grown on p-type Si substrate by dry oxidation in an atmospheric pressure chemical vapor deposition (APCVD) furnace as a tunnel oxide in both samples. Subsequently, **in sample I**: a 50-nm PECVD SiGeN was deposited on tunnel oxide; **in sample II**: a 20-nm PECVD SiGeN was deposited on tunnel oxide as charge-trapping layers, followed by the deposition of 20-nm PECVD a-Si layer.

The deposition of the PECVD SiGeN was kept at 200 °C in a low pressure of 6 mTorr with  $\text{SiH}_4 : \text{GeH}_4 : \text{NH}_3 : \text{N}_2 = 20 \text{ sccm} : 5 \text{ sccm} : 30 \text{ sccm} : 500 \text{ sccm}$  and a RF power of 20 W. The  $\text{N}_2$  gas was served as the carrier gas to adjust the chamber pressure and make the process gas can easily transport into the process chamber. The low pressure of 6 mTorr during deposition makes the mean free path of electrons and radicals increase, which will improve the uniformity of the thin film [3.1]. The sequent deposited a-Si was at 200 °C with  $\text{SiH}_4 : \text{H}_2 = 20 \text{ sccm} : 980 \text{ sccm}$ , and a 20W power. Then, the samples were oxidized in thermal furnace at 900 °C in oxygen ambient to form blocking oxide. Besides, a three minutes steam treatment is performed on some samples after blocking oxide formation. Finally, the Al gate was patterned and sintered

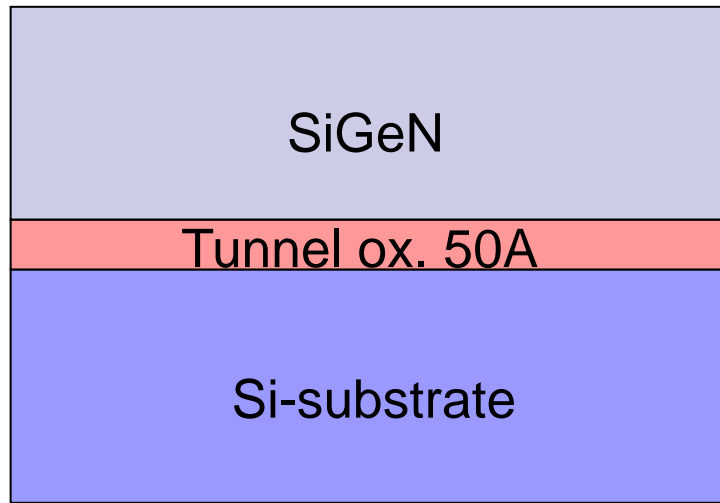
to form a metal/oxide/nitride/oxide/silicon (MONOS) structure.

In short, the difference between **sample I** and **sample II** is the thickness of SiGeN layer (thicker in sample I) and with/without capped amorphous Si layer (with Si cap layer in sample II).

### 3.2 Thermal Process

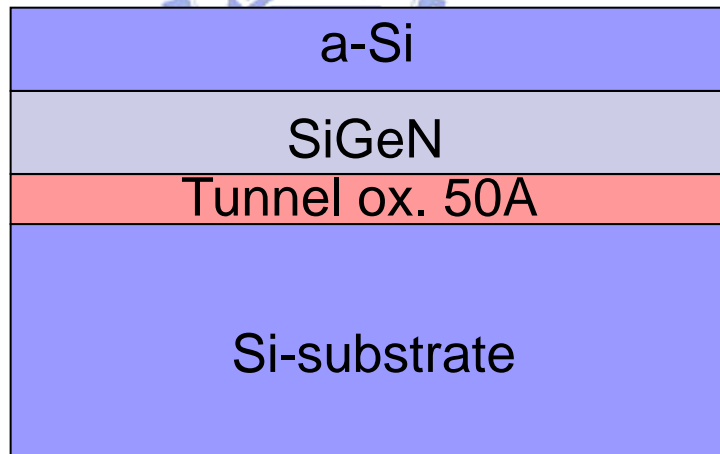
Fig. 3-4 and Fig. 3-5 indicate the thermal process flow in sample I and sample II. In sample I, directly oxidize a thick SiGeN layer (sample I) to form blocking oxide by a dry oxidation process with different time or by a 30 min dry oxidation process followed by a 3 minutes steam treatment in thermal furnace at 900 °C. In sample II, oxidize the amorphous Si layer capped on the SiGeN layer (sample II) to form blocking oxide by a dry oxidation process with different time or by a 30 min dry oxidation process followed by a 3 minutes steam treatment in thermal furnace at 900 °C. The steam treatment means let in H<sub>2</sub>O into thermal furnace, the same as wet oxidation. Owing to its smaller size and lower activation energy than O<sub>2</sub> molecules, H<sub>2</sub>O molecules are more permeable through the blocking oxide and can passivate dangling bonds in the blocking oxide. The purpose of steam treatment is to strengthen the blocking oxide and improve its quality.

### Sample I



(a)

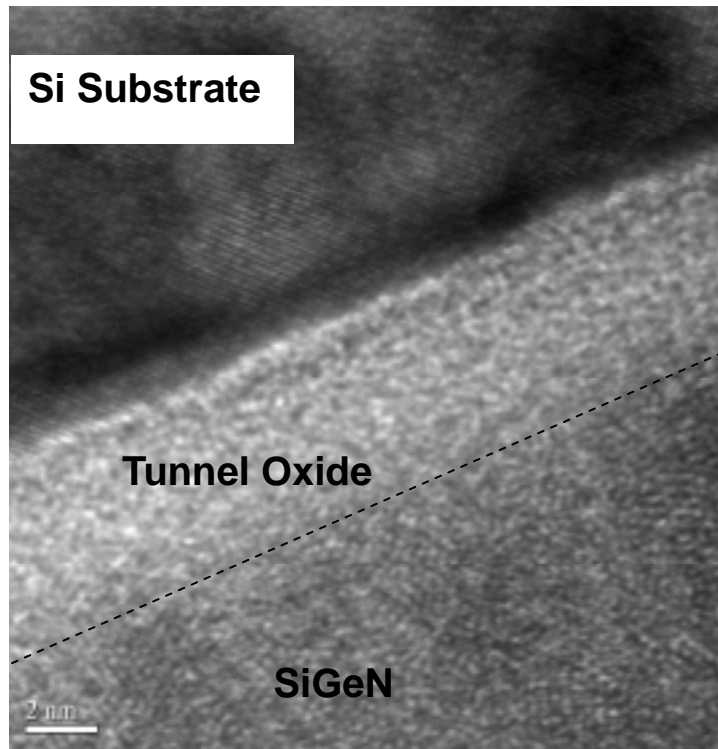
### Sample II



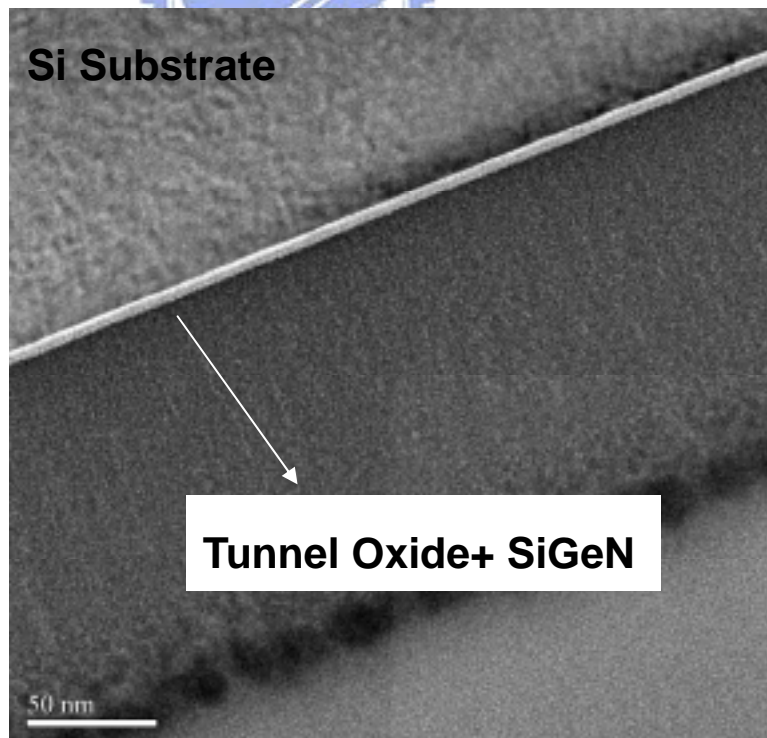
(b)

Figure 3-1 (a) Sample structure of sample I (b) Sample structure of sample II.

# Sample I



(a)



(b)

Figure 3-2 The TEM diagram of sample I before thermal oxidation.



## Sample II

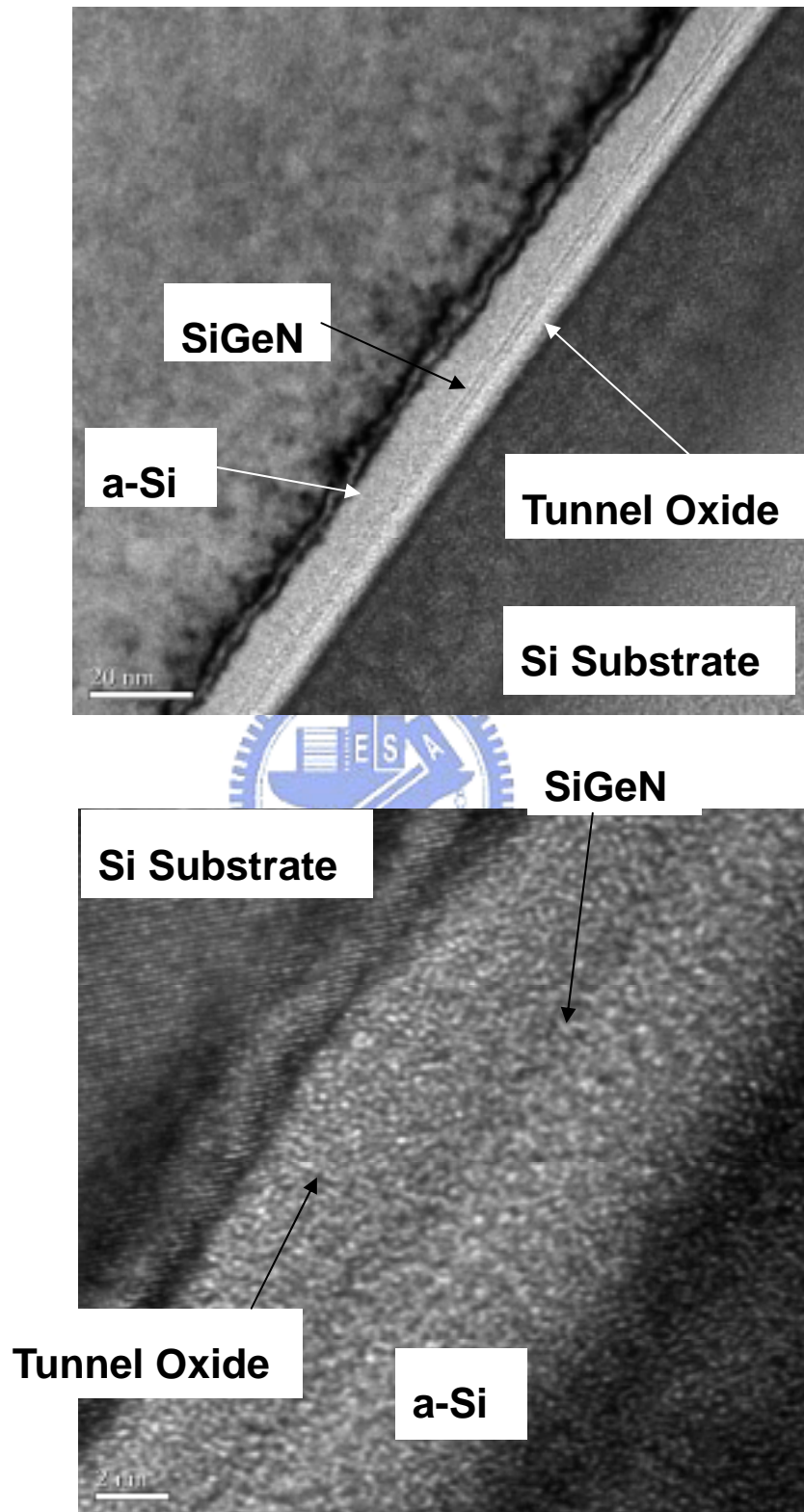


Figure 3-3 The TEM diagram of sample II before thermal oxidation.

# Sample I

**Directly Oxidize SiGeN Layer to Form Blocking Oxide**

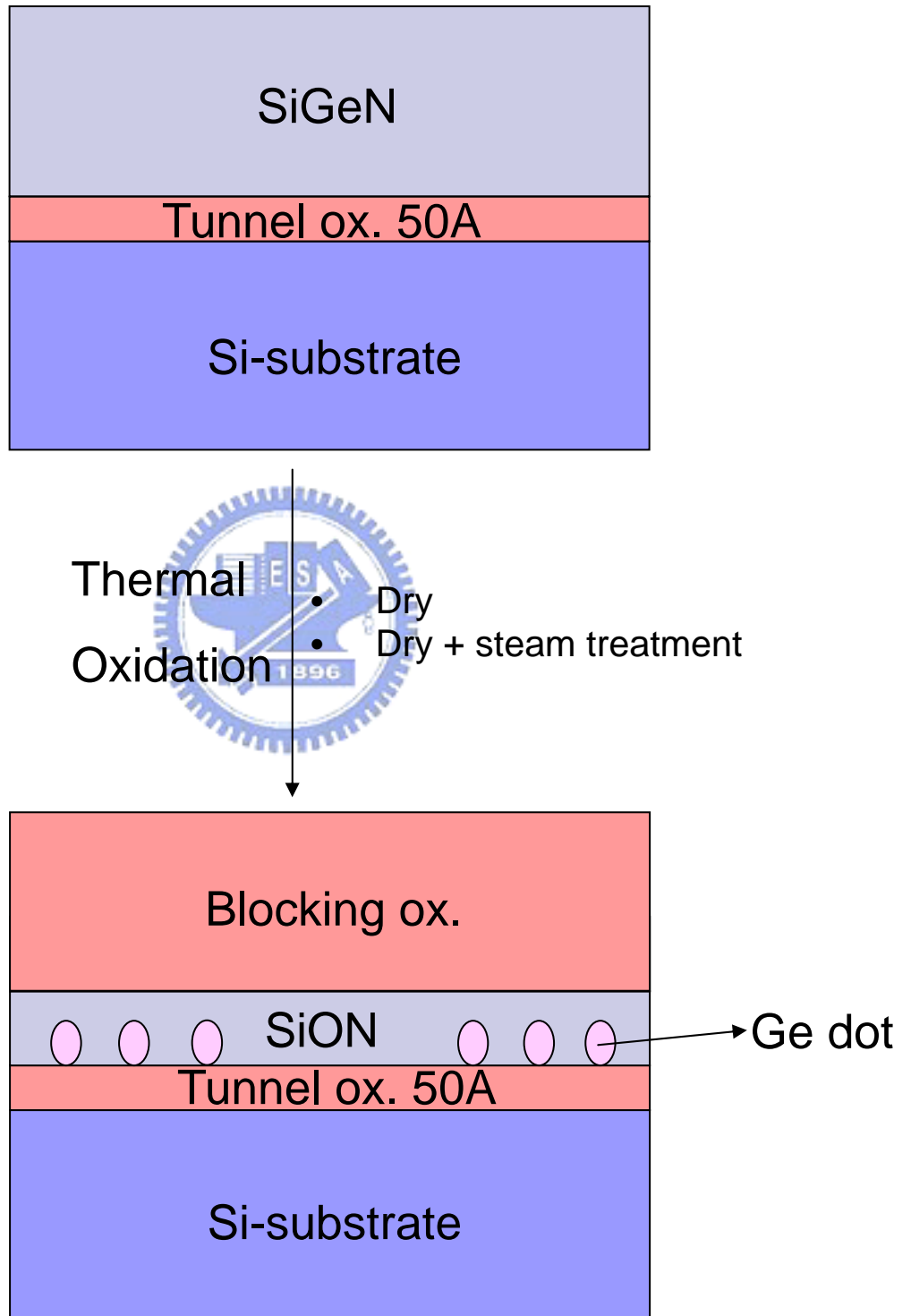


Figure 3-4 The thermal process flow of sample I.

## Sample II

**Oxidize The Amorphous Si Layer Capped on the  
SiGeN layer to Form Blocking Oxide**

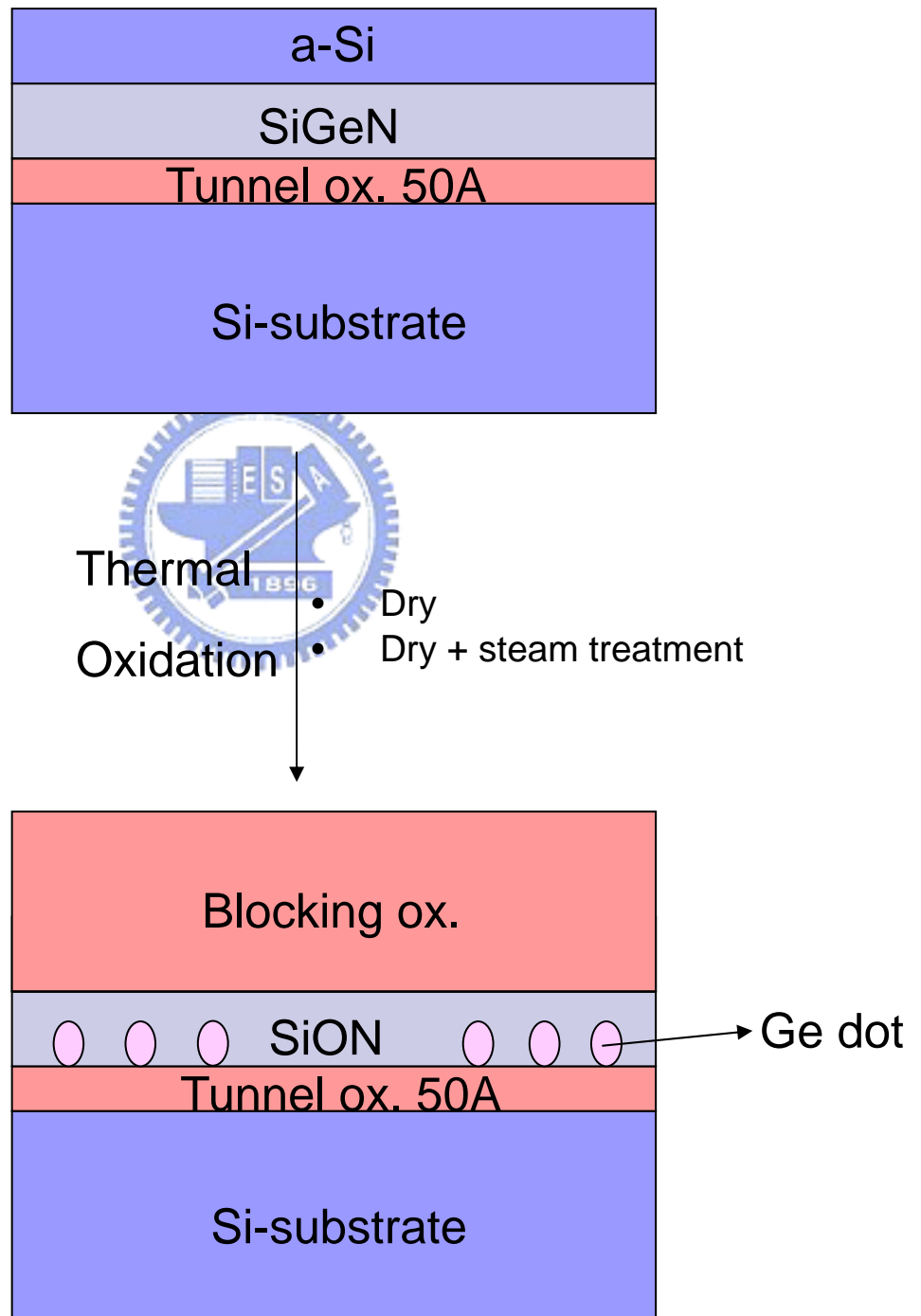


Figure 3-5 The thermal process flow of sample II.

## Chapter 4

### Experiment Results and Discussions

#### 4.1 Electrical Characteristics

In previous section, it has been mentioned that there are two methods used to form blocking oxide. In one method, only a dry oxidation process with different time in thermal furnace at 900 °C is adopted. In the other method, a dry oxidation process is followed by a 3 minutes steam treatment. Table 4-1 shows the difference conditions performed on sample I and sample II. The Ge nanocrystals embedded SiON layer (the charge storage layer) of a MOIOS memory device is utilized to capture the injected carriers from the channel. When the device is programmed, electrons directly tunnel from the Si substrate through the tunnel oxide by Fowler-Nordheim (F-N) tunneling. The tunneling electrons are trapped in the forbidden gap of SiON layer and conduction band of Ge nanocrystals in the SiON layer. For the erasion, the holes may tunnel from the valence band of the Si substrate. The tunneling hole recombine with the electrons trapped in the forbidden gap of SiON layer and conduction band of Ge nanocrystals in the SiON layer. The blocking oxide is utilized to prevent the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (F-N) tunneling. The capture of carriers will causes a variation in the threshold voltage and can serve as a memory device.

The capacitance-voltage (C-V) hysteresis of **sample I** (without capped Si layer) with three different conditions A, B, C and D are shown in Fig. 4-1 (a), (b) and Fig. 4-2 (a), (b), respectively. In 30 and 45 minutes short term dry oxidation (condition A and B),

because the thickness is not thick enough and the quality is not good enough, the blocking oxide can't block the carriers (electrons or holes) tunneling from gate to charge storage layer. When the dry oxidation time is extended to 60 minutes (condition C), the blocking oxide is thick enough to block the carriers from gate and therefore the way carrier injection turns from gate injection to substrate injection. In condition C, the memory windows are  $\sim 1.1\text{V}$  under  $\pm 3\text{V}$  C-V sweeping,  $\sim 2.4\text{V}$  under  $\pm 5\text{V}$  C-V sweeping and  $\sim 4\text{V}$  under  $\pm 7\text{V}$  C-V sweeping. In condition D (30 minutes dry oxidation followed by 3 minutes steam treatment), the memory window is  $0.9\text{V}$  under  $\pm 10\text{V}$  C-V sweeping. The retention character of sample I with condition C (60 minutes dry oxidation) is shown in Fig. 4-3. The program curve and erase curve in Fig. 4-3 shift toward positive voltage at the same time because positive oxide trapped charges are created during the program/erase cycles in tunnel oxide and they will de-trap with the retention time [4-1]. As the de-trapping of the positive oxide trapped charges, the threshold voltage will shift to positive side. The schematic plot and are shown in Figure 4-4. The endurance characteristic of sample I with condition C (60 minutes dry oxidation) is shown in Fig. 4-5. There is almost no shift in the threshold voltage after  $10^6$  program/erase cycles under  $\pm 3\text{V}$  operation.

The capacitance-voltage (C-V) hysteresis of **sample II** (with capped Si layer) with four different conditions A, B, C and D are shown in Fig. 4-6 (a), (b), and 4-7 (a), (b), respectively. The C-V properties are of the same trends as sample I. In 30 and 45 minutes short term dry oxidation (condition A and B) a gate injection is observed. Also, substrate injections are observed in 60 minutes dry oxidation (condition C) and 30 minutes dry oxidation plus a 3-minute steam treatment (condition D). In condition C, the threshold-voltage shift (memory window,  $\Delta V_t$ ) under  $\pm 7\text{V}$  C-V sweeping is  $\sim 1.7\text{V}$  and in condition D (30 minutes dry oxidation followed by 3 minutes steam treatment), the memory windows are  $\sim 0.6\text{V}$  under  $\pm 3\text{V}$  C-V sweeping,  $\sim 1.8\text{V}$  under  $\pm 7\text{V}$  C-V

sweeping and  $\sim 4.2\text{V}$  under  $\pm 10\text{V}$  C-V sweeping. The retention and endurance character of sample II with condition D are shown in Fig. 4-8 and Fig. 4-9. The Auger Electron Spectroscopy (AES) analysis of sample II with condition D is shown in Fig. 4-33 (b). There is a rise in oxygen signal after steam treatment in AES analysis. The SiON dielectric is oxidized by steam to form SiOx. As a result, the Ge nanocrystals are not embedded in SiON but in SiOx. The program and erase curves in Fig. 4-9 shift to negative voltage at the same time because positive oxide trapped charges are created during the program/erase cycles in both tunnel oxide and the SiOx oxidized from SiON film by steam treatment [4-1]. The schematic plot is shown in Figure 4-10. The positive trapped charges in SiOx oxidized from SiON film will increase with the P/E cycles because of its worse quality than tunnel oxide's. Therefore, the threshold voltage in the Fig. 4-9 will shift to negative side.

#### **4.1.1 Comparing to Other Memories**

Figure 4-11 shows the C-V hysteresis of Ge nanocrystals embedded in SiO<sub>2</sub> (Ge nanocrystal only) nonvolatile memory proposed by T. C. Chang et al. [4.2]. Fig. 4-12 shows the C-V hysteresis of SONOS memory and the SiN<sub>x</sub> layer in the ONO stack is deposited by the same PECVD used in this study. The memory windows in the Ge nanocrystal only NVSM are  $\sim 0.4\text{V}$  under  $\pm 5\text{V}$  C-V sweeping and  $\sim 2\text{V}$  under  $\pm 10\text{V}$  C-V sweeping. The memory windows in SONOS only NVSM are  $\sim 0.2\text{V}$  under  $\pm 5$  C-V sweeping and  $\sim 0.6\text{V}$  under  $\pm 10\text{V}$  C-V sweeping. In this study, a combination of Ge nanocrystal and SONOS NVSM is proposed. The memory windows of sample I with condition C are  $\sim 1.1\text{V}$  under  $\pm 3\text{V}$  C-V sweeping,  $\sim 2.4\text{V}$  under  $\pm 5\text{V}$  C-V sweeping and  $\sim 4\text{V}$  under  $\pm 7\text{V}$  C-V sweeping, as shown in Fig. 4-2 (a). Moreover, The memory windows of sample II with condition D are  $\sim 0.6\text{V}$  under  $\pm 3\text{V}$  C-V sweeping,  $\sim 1.8$  V under  $\pm 7\text{V}$  C-V sweeping and  $\sim 4.2\text{V}$  under  $\pm 10\text{V}$  C-V sweeping, as shown in Fig. 4-7 (b). The memory windows both in sample I and sample II are larger than Ge nanocrystal

only NVSM or SONOS only NVSM (table. 4-4) and even larger than the Ge nanocrystal NVSM plus SONOS NVSM. It's inferred that besides charge trapping units in the Ge nanocrystal and the SiON dielectric, there are additional charge trapping units at Ge/SiON interface. The band diagrams are shown in Figure 4-13.

## 4.2 Mechanism of Ge Nanocrystals Formation

Kan et al. adopted a two-step RTA process executed on a  $\text{Si}_{0.54}\text{Ge}_{0.46}$  film to form Ge nano-dots embedded in  $\text{SiO}_x$  dielectric [4.3-4.4] and the 950 °C  $\text{N}_2$  RTA would reduce the Ge atoms and the nanocrystals grew based on the Ostwald ripening mechanism [4.5]. Besides, a method of Ge nano-dots segregated downward until they reach the tunnel oxide surface by  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer being wet oxidized in an APCVD reactor has been proposed [4.6-4.8]. In this work, the formation of Ge nanocrystals is only by one step of oxidation of the silicon-germanium-nitride layer, which is simpler than the previous research [4.9] and high-throughput and low cost potentially for industrial consideration.

A thermal furnace process is introduced to form blocking oxide ( $\text{SiO}_x$  or SiON) and segregate Ge atoms in this study. During 900 °C dry oxidation process, Si in the SiGeN film more easily combine with  $\text{O}_2$  than Ge to form  $\text{SiO}_x$ . Because of the low solid solubility of Ge in silicon oxide, the Ge atoms will be segregated downward until they reach the tunnel oxide surface [4.6-4.8] and nucleate to form Ge nano-dots (or Ge nanocrystal) near the tunnel oxide(or gate oxide). Therefore, the SiGeN film will be oxidized to form  $\text{SiO}_x$  film (as blocking oxide); meanwhile, the Ge in the SiGeN film will be segregated to form Ge nano-dots (or Ge nano-crystal) embedded by SiON dielectric near the tunnel oxide.

#### 4.2.1 Directly Oxidize SiGeN Layer as Blocking Oxide ( Sample I )

The different bonds' wave numbers of Fourier Transform Infrared Rays (FTIR) spectrum are shown in table 4-2 and 4-3 [4.8]. The FTIR spectra of sample I before and after thermal oxidation process are shown in Figure 4-14. The weak bonds such as Si-H, Ge-H, N-H disappear after 900 °C dry oxidation and the appearance of Si-O after oxidation means the SiGeN layer has been oxidized to form SiO<sub>x</sub> as blocking oxide. The transmission electron microscope (TEM) diagrams and Auger Electron Spectroscopy (AES) analysis before oxidation and after oxidation with condition A(dry 30 minutes), C(dry 60minutes) are shown in Fig. 4-15 (a), (b) and Fig. 4-16 (a), (b), respectively. The TEM diagram as shown in Fig. 4-15 (a), there is no Ge nanocrystal present in the as-deposited SiGeN film before oxidation and Fig. 4-15 (b) shows that all of the three elements, Si, Ge and N are present in the as-deposited SiGeN film before oxidation. The Ge nanocrystals appear in the TEM diagram after oxidation as shown in Fig. 4-16 (a) and there is a rise of Ge and N signal between 500 and 1300 second in Fig. 4-16 (b), which reveals that the Ge nanocrystals are imbedded in SiON dielectric.

The Raman spectra of sample I before and after 30 minutes thermal oxidation process in O<sub>2</sub> ambiance are shown in Figure 4-17. In the Raman spectrum of SiGeN film in sample I before oxidation, there is a broad distribution signal which means that the as-deposited SiGeN film is amorphous and a signal peak of Ge crystal appears after 30 minutes thermal oxidation. The appearance of the signal peak of crystal Ge represents that the Ge atoms in SiGeN film were segregated and nucleated forming Ge nanocrystal while dry oxidation. The Raman spectra of 30 minutes short term and 60 minutes long term dry oxidation are shown in Fig. 4-18 (a) and (b). In comparison with crystal Si substrate signal peak (~520 cm<sup>-1</sup>), the intensity of crystal Ge peak (~300 cm<sup>-1</sup>) increase with the extension of dry oxidation time, which reveals that the longer oxidation time makes not only more Ge atoms to be segregated from the thickening



blocking oxide, but also more time for Ge atoms to nucleate. The intensity of crystal Ge after 60 minutes oxidation is even stronger than that of crystal Si substrate.

#### ***4.2.2 Oxidize Capped Amorphous Si Layer as Blocking Oxide ( Sample II )***

The FTIR spectra of sample II before and after thermal oxidation process are shown in Figure 4-19. The same as sample I, the weak bonds such as Si-H, Ge-H, N-H disappear after 900 °C dry oxidation and the appearance of Si-O after oxidation means the SiGeN layer has been oxidized to form SiO<sub>2</sub> as blocking oxide. The transmission electron microscope (TEM) diagrams and Auger Electron Spectroscopy (AES) analysis before oxidation and after oxidation with condition A(dry 30 minutes), C(dry 60minutes) are shown in Fig. 4-20 (a), (b), Fig. 4-21 (a), (b), Fig. 4-22 (a), (b), respectively. Also, the TEM diagram as shown in Fig. 4-20 (a), there is no Ge nanocrystal present in the as-deposited SiGeN film before oxidation and Fig. 4-20 (b) shows that all of the three elements, Si, Ge and N are present in the as-deposited SiGeN film before oxidation. In the Raman analysis as shown in Fig. 4-23, there is a Ge crystal peak but in the TEM diagram (Fig. 4-20(a)), there is no Ge nanocrystal present in the oxidized SiGeN film because the oxidation time is not long enough for Ge atoms to be segregated and to nucleate and this phenomenon is also observed by Kan et al. in their study [4.2]. After a longer oxidation period, the Ge nanocrystals appear in the TEM diagram, as shown in Fig. 4-22 (a) and there is a rise of Ge and N signal between 100 and 400 second in Fig. 4-22 (b), which reveals that the Ge nanocrystals are imbedded in SiON dielectric.

The Raman spectra of sample II before and after 30 minutes thermal oxidation process in O<sub>2</sub> ambiance are shown in Figure 4-24. In the Raman spectrum of SiGeN film in sample II before oxidation, there is a broad distribution signal which means that the deposited SiGeN film is amorphous and a signal peak of Ge crystal appears after 30 minutes thermal oxidation. The appearance of the signal peak of crystal Ge represents that the Ge atoms in SiGeN film were segregated and started to nucleate forming Ge

nanocrystal while oxidation. The Raman spectra of 30 minutes short term and 45 minutes longer term dry oxidation are shown in Fig. 4-25 (a) and (b). The same as sample I, in comparison with crystal Si substrate signal peak ( $\sim 520\text{ cm}^{-1}$ ), the intensity of crystal Ge peak ( $\sim 300\text{ cm}^{-1}$ ) increase with the extension of dry oxidation time, which reveals that the longer oxidation time makes not only more Ge atoms to be segregated from the SiGeN layer, but also more time for Ge atoms to nucleate. The intensity of crystal Ge after 45 minutes oxidation is even as strong as that of crystal Si substrate. Besides, there is a Si-Ge signal appear in Fig. 2-25 (a), (b) and the peak decays with the extension of oxidation time, but it's not present in sample I. Therefore, it's inferred that the Si-Ge bonds are produced in the amorphous/SiGeN interface during the PECVD film deposition process.

### 4.3 Role of Steam Treatment



The steam treatment means let in  $\text{H}_2\text{O}$  into thermal furnace at  $900^\circ\text{C}$ , the same as wet oxidation. After the dry oxidation, a 3-minute steam treatment is performed on both sample I and sample II; the results are demonstrated in this section. It's believed that owing to its smaller size and lower activation energy than  $\text{O}_2$  molecules,  $\text{H}_2\text{O}$  molecules are more permeable through the blocking oxide and passivate dangling bonds in blocking oxide. The purpose of steam treatment is to strengthen the blocking oxide and improve its quality.

#### 4.3.1 Directly Oxidize SiGeN Layer as Blocking Oxide ( Sample I )

The capacitance-voltage (C-V) hysteresis and I-V characteristics of sample I (without capped Si layer) with four different conditions (A, B, C, D) are shown in Fig. 4-26 (a), (b), (c), (d) and Fig. 4-27, respectively. With the extension of oxidation time from 30 minutes to 60 minutes, the C-V hysteresis turns from gate injection (clockwise)

to substrate injection (counterclockwise) and the leakage current density (J) in the I-V diagram decrease from  $10^{-3}$  order to  $10^{-9}$  order, which means the blocking oxide is thick enough and its quality is good enough after a long enough dry oxidation. However, the leakage current density characteristic of 30 minutes short term dry oxidation followed by a 3 minutes steam treatment is comparable with 60 minutes long term dry oxidation, which reveals that an extra 3 minutes steam treatment can improve the blocking oxide quality.

The TEM diagrams and Auger Electron Spectroscopy (AES) analysis after oxidation with condition D (30 minutes dry oxidation plus 3 minutes steam treatment) are shown in Fig. 4-28 (a) and (b). Owing to the rapid oxidation rate of steam treatment, the Si atoms in SiGeN film are oxidized so fast that there is not enough time for Ge atoms to be segregated toward the tunnel oxide and therefore the Ge clusters are present throughout the oxidized SiGeN film, as shown in Fig. 4-28 (a). Furthermore, the N signal in the AES spectrum, as shown in Fig. 4-28 (b), almost decays to zero after steam treatment. This represents that the SiON dielectric by which the Ge nano-crystal is surrounded is oxidized to become SiOx and also explains the endurance characteristic without steam treatment (Fig. 4-5) is better than that with a steam treatment (Fig. 4-9) because of the oxide trapped charges present in the SiOx dielectric after P/E cycles.

The Raman spectra before and after steam treatment are compared in figure 4-29. There is a dramatic drop in the Ge signal peak and there is also a rise in the germanium oxide ( $\text{Ge}_2\text{O}$ ) signal after a steam treatment. The same situation is also observed in 60 minutes dry oxidation with and without steam treatment cases, as shown in Fig. 4-30. These show that the introduction of steam treatment will oxidize a part of Ge nanocrystal to become germanium oxide by which the Ge nanocrystals are surrounded.

#### ***4.3.2 Oxidize Capped Amorphous Si Layer as Blocking Oxide ( Sample II )***

The capacitance-voltage (C-V) hysteresis and I-V characteristics of sample II (with capped Si layer) with four different conditions (A, B, C, D) are shown in Fig. 4-31 (a), (b), (c), (d) and Fig. 4-32, respectively. With the extension of oxidation time from 30 minutes to 60 minutes, the C-V hysteresis turns from gate injection (clockwise) to substrate injection (counterclockwise) and the leakage current density (J) in the I-V diagram decrease from  $10^{-2}$  order to  $10^{-9}$  order, which means the blocking oxide is thick enough and its quality is good enough after a long enough dry oxidation. The same as sample I (without capped Si layer), the leakage current density characteristic of 30 minutes short term dry oxidation followed by a 3 minutes steam treatment is comparable with 60 minutes long term dry oxidation, which reveals that an extra 3 minutes steam treatment can improve the blocking oxide quality. The TEM diagrams of 60 minutes dry oxidation and 30 minutes dry oxidation plus 3 minutes steam treatment are shown in figure 4-33 (a) and (b). The thickness of blocking oxide after 60 minutes dry oxidation ( $\sim 260$  Å) is thicker than that after 30 minutes dry oxidation ( $\sim 200$  Å) plus 3 minutes steam treatment but the I-V characteristic after 30 minutes oxidation ( $\sim 200$  Å) plus 3 minutes steam treatment is comparable with that after 60 minutes long term dry oxidation. This proves that the blocking oxide quality after 30 minutes dry oxidation followed by a 3-minute steam treatment is better than that after 60 minutes long term dry oxidation.

The TEM diagrams and Auger Electron Spectroscopy (AES) analysis after oxidation with condition D (30 minutes dry oxidation plus 3 minutes steam treatment) are shown in Fig. 4-34 (a) and (b). In Fig. 4-34 (a), because there is an amorphous capped Si layer in sample II before oxidation, the Ge nanocrystals are confined only between tunnel oxide and blocking oxide after oxidation. As a result, the distribution of Ge nanocrystals differ from the case in sample I with the same oxidation condition (Fig. 4-28 (a)). Furthermore, the same phenomenon is observed that comparing to the case

before steam treatment in Fig. 4-21 (b), the N signal in the AES spectrum, as shown in Fig. 4-34 (b), decreases after steam treatment. This means that the SiON dielectric by which the Ge nano-crystal is surrounded is oxidized to become SiO<sub>x</sub> and also explains the endurance characteristic without steam treatment (Fig. 4-5) is better than with a steam treatment (Fig. 4-9) because of the oxide trapped charges present in the SiO<sub>x</sub> dielectric after P/E cycles again.

The Raman spectra before and after steam treatment are compared in figure 4-35. Also, there is a dramatic drop in the Ge signal peak and there is also a rise in the germanium oxide (Ge<sub>2</sub>O) signal after a steam treatment. The same situation is also observed in 60 minutes dry oxidation with and without steam treatment cases, as shown in Fig. 4-36. These show that the introduction of steam treatment will make a part of every Ge precipitate formed during dry oxidation be oxidized to become germanium oxide by which the Ge nanocrystals are surrounded. Besides, the Si-Ge signal present in Fig. 4-25 (a), (b) disappears after steam treatment because of the good oxidizing ability of steam and the Si-Ge bonds are oxidized to form silicon oxide and germanium oxide.

## Conditions of Thermal Process

<b>Condition</b>	<b>O2 thermal oxidation</b>	<b>3 min steam treatment</b>
<b>A</b>	<b>30 min</b>	<b>No</b>
<b>B</b>	<b>45 min</b>	<b>No</b>
<b>C</b>	<b>60 min</b>	<b>No</b>
<b>D</b>	<b>30 min</b>	<b>Yes</b>

Table 4-1 Conditions of thermal process.

<i>Wave Number ( cm<sup>-1</sup> )</i>	<i>MODE</i>
3380	N-H stretch mode
650-900	N-H wagging mode
909,964,993	NH <sub>2</sub> bending mode
1568	NH <sub>2</sub> scissor mode
1042	C-N stretch mode
1468	C-H bending mode
2850,2922,2955	C-H stretch mode
2044	Si-H stretch mode
1543	Si-H bending mode
650	Ge-H bending mode
1779,1100	Ge-H
1090-1200	Si-O-Si
960-1020	Si-O-Ge
900-980	Ge-O-Ge
2700-3800	OH
420	Ge-O bending
800-1000	Ge-O stretch
1126-1128	Si-O stretch
503-505, 820	Si-O bending
450	Si-O rocking
3600, 3665	SiO-H stretch
3470,3515	GeO-H stretch

Table 4-2 The different bonds' wave numbers of Fourier Transform Infrared Rays (FTIR) spectra.

IR 光譜波段配置

波段位置	結構
3750(s)	$\nu$ (OH) zeolite-like hydroxyl
3680,3650,3520(w)	$\nu$ (OH) of Si-OH group
3400-3300(s)	$\nu$ (OH) of $H_2O$
2000(m),1875(w)	Combination band (SiO)
1640(w)	$2\nu$ (Si-O) overtone
1630(m)	$\delta_{H_2O}$ of $H_2O$
1200-1180(m,sh)	$\nu_{as}$ (Si-O)
1100-1070(s)	$\nu_{as}$ (Si-O)
1100	$\nu_{as}$ (Al-O) in Al-O-Si
965,935,890(w)	$\nu$ (Si-OH)
960	$\nu$ (Si-OH) for surface SiOH
950(mw)	$\nu$ (Si-OH)
950	$\nu_{as}$ (Al-O) in Al-O-Si
870(m)	$\delta$ (SiOH) of SiOH
870	$\nu$ (Si-OH) for surface OH <sup>-</sup>
810	$\delta$ (Si-O-Si) or $\delta$ (O-Si-O)
810(m)	$\nu_{as}$ (Si-O)
808	$\delta$ (Si-O-Si)
740,630,570(vw)	$\nu_{as}$ (Si-O)
475-460(s)	$\delta$ (O-Si-O)
450	$\delta$ (O-Al-O)
440	$\delta$ (Si-O-Si) or $\delta$ (O-Si-O)

$\nu$  : 伸展模式       $\delta$  : 彎曲模式      s : strong      m : medium  
 mw : medium weak      w : weak      vw : very weak      sy : 對稱性  
 as : 不對稱性

Table 4-3 The different bonds' wave numbers of Fourier Transform Infrared Rays (FTIR) spectra.



	$V_{TH}$ under 5V	$V_{TH}$ under 7V	$V_{TH}$ under 10V
Ge Nanocrystal NVM	0.4	X	1
SiN <sub>x</sub> NVM	0.2	0.6	X
Oxidized capped a-Si SiGeN NVM	X	1.8	3.2
Oxidized SiGeN NVM	2.4	4	X

Table 4-4 The memory windows of different memories.

# Sample I

(w/o Capped Si layer)

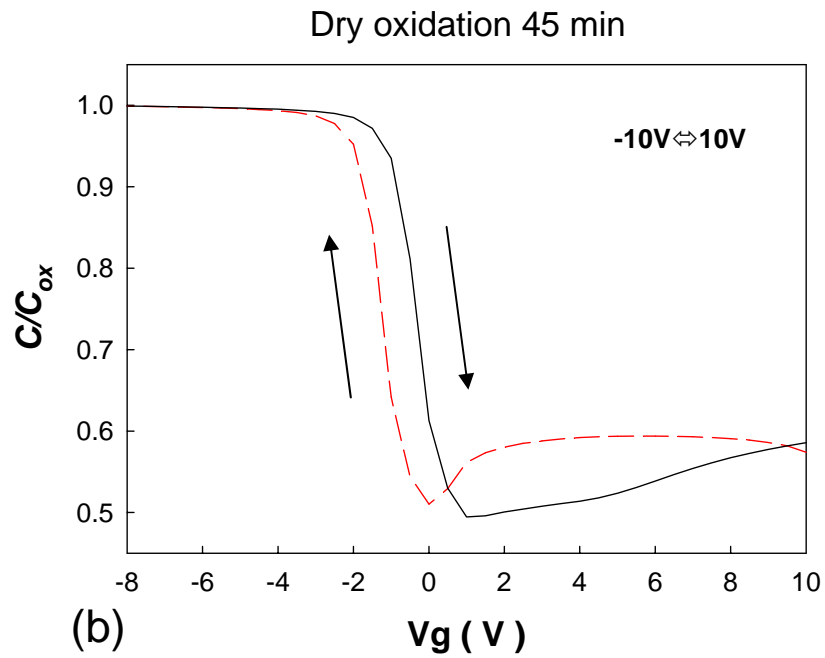
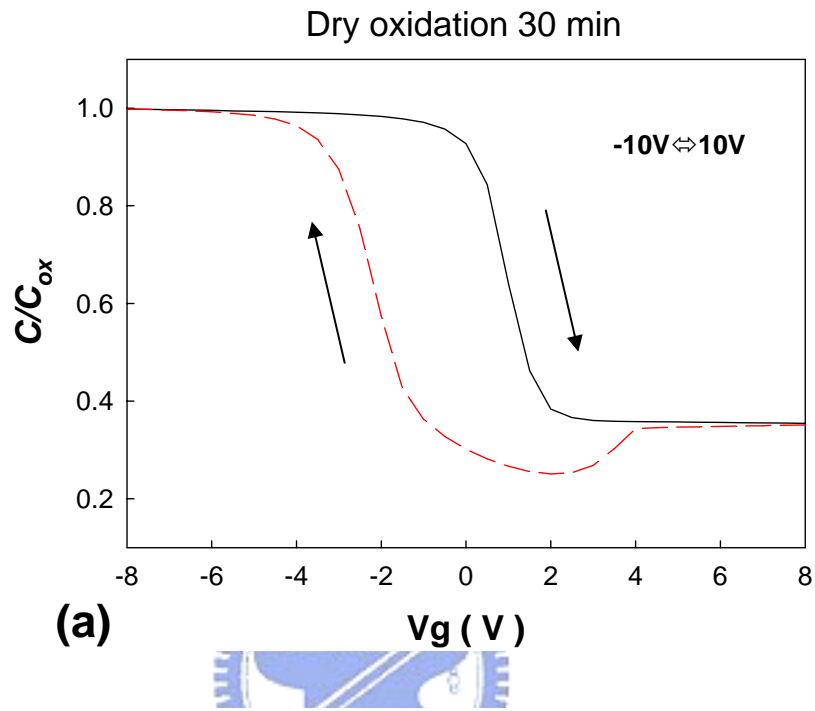
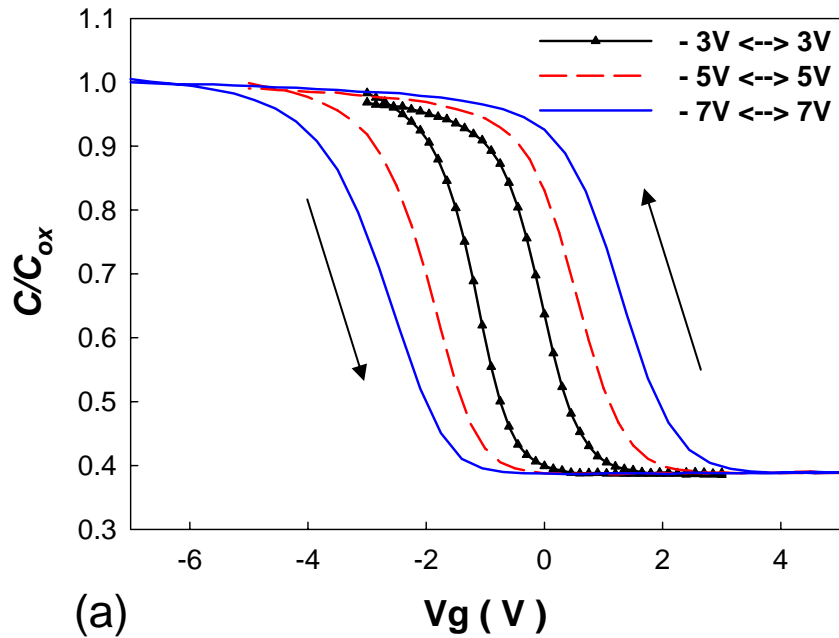


Figure 4-1 The C-V diagrams of sample I with (a) condition A and (b) condition B. Both diagrams are gate injection.

# Sample I

(w/o Capped Si layer)

Dry oxidation 60 min



Dry oxidation 30 min + steam treatment 3 min

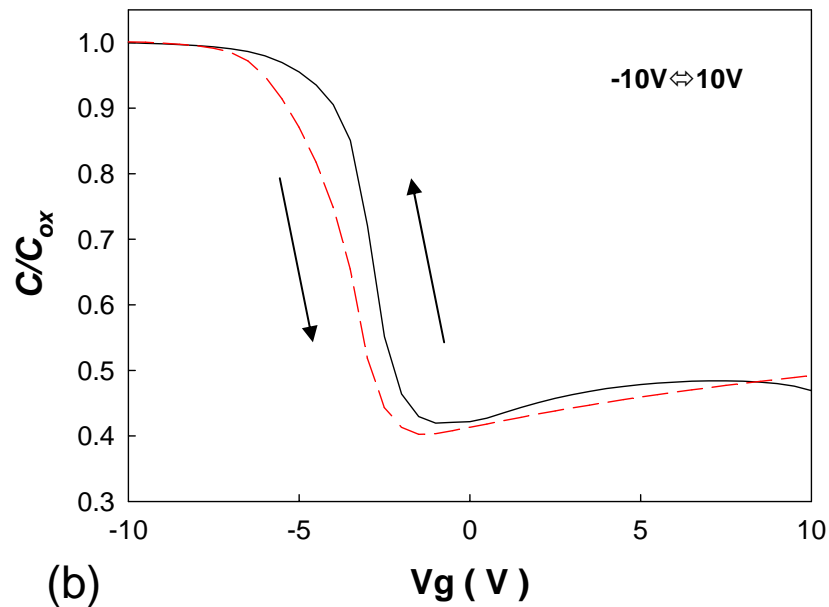


Figure 4-2 The C-V diagrams of sample I with (a) condition C and (b) condition D. Both diagrams are substrate injection.

# Sample I

(w/o Capped Si layer)

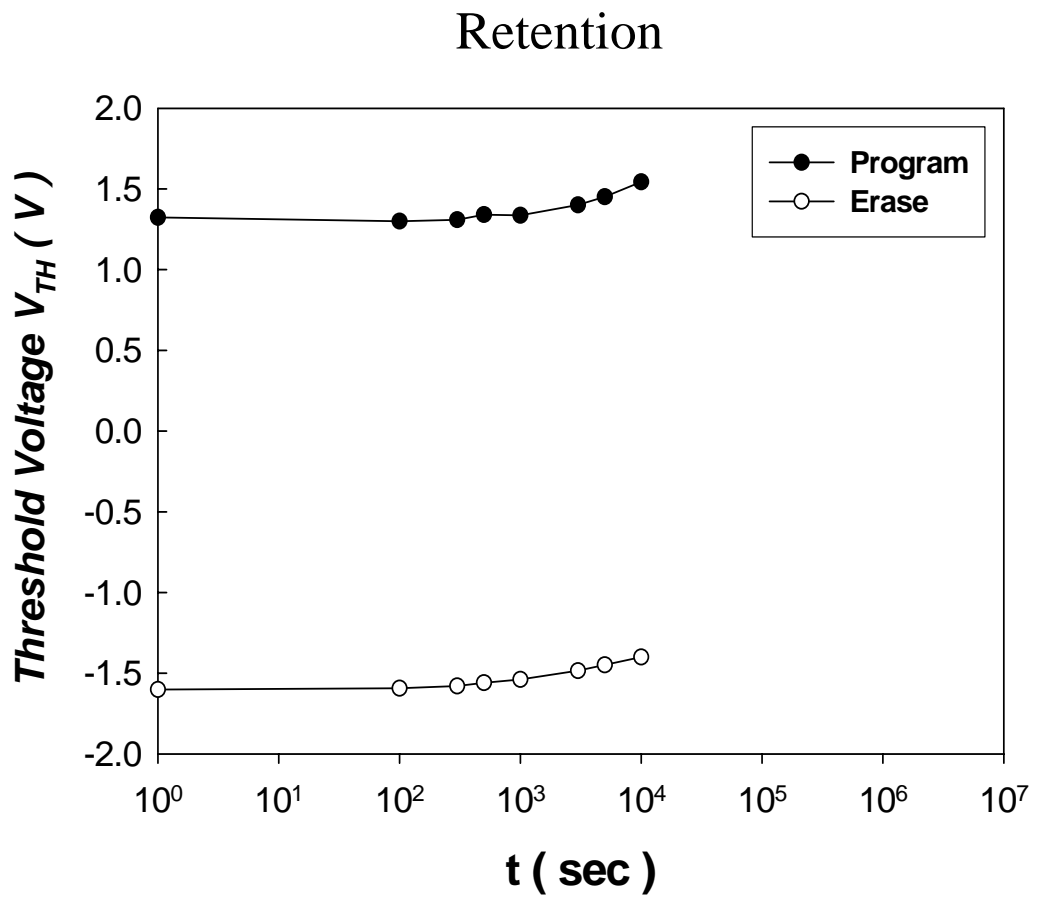


Figure 4-3 The retention character of sample I with condition C (60 min dry oxidation).

# Sample I

(w/o Capped Si layer)

After P/E cycles

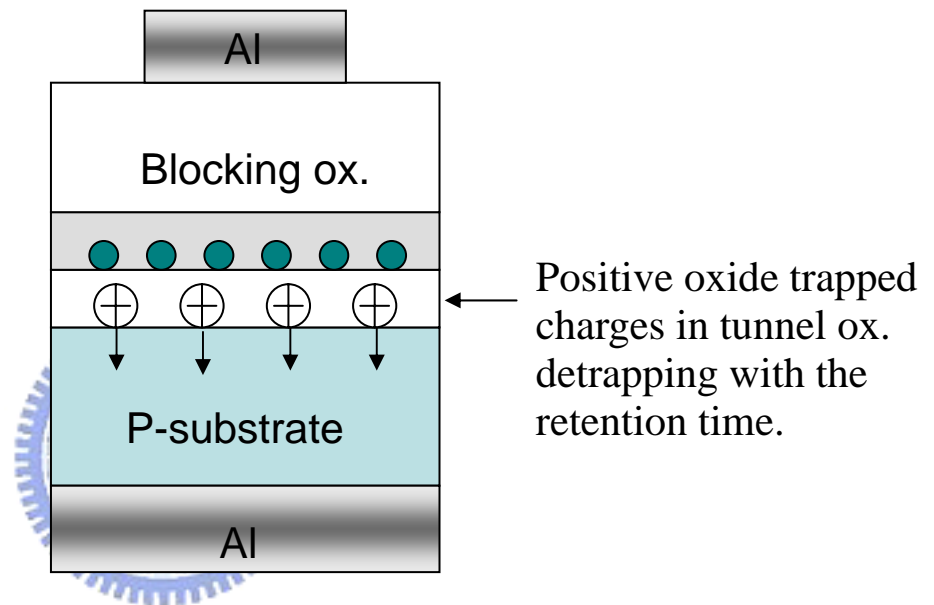


Figure 4-4 The de-trapping schematic plot of positive oxide trapped charges in tunnel oxide.

# Sample I

(w/o Capped Si layer)

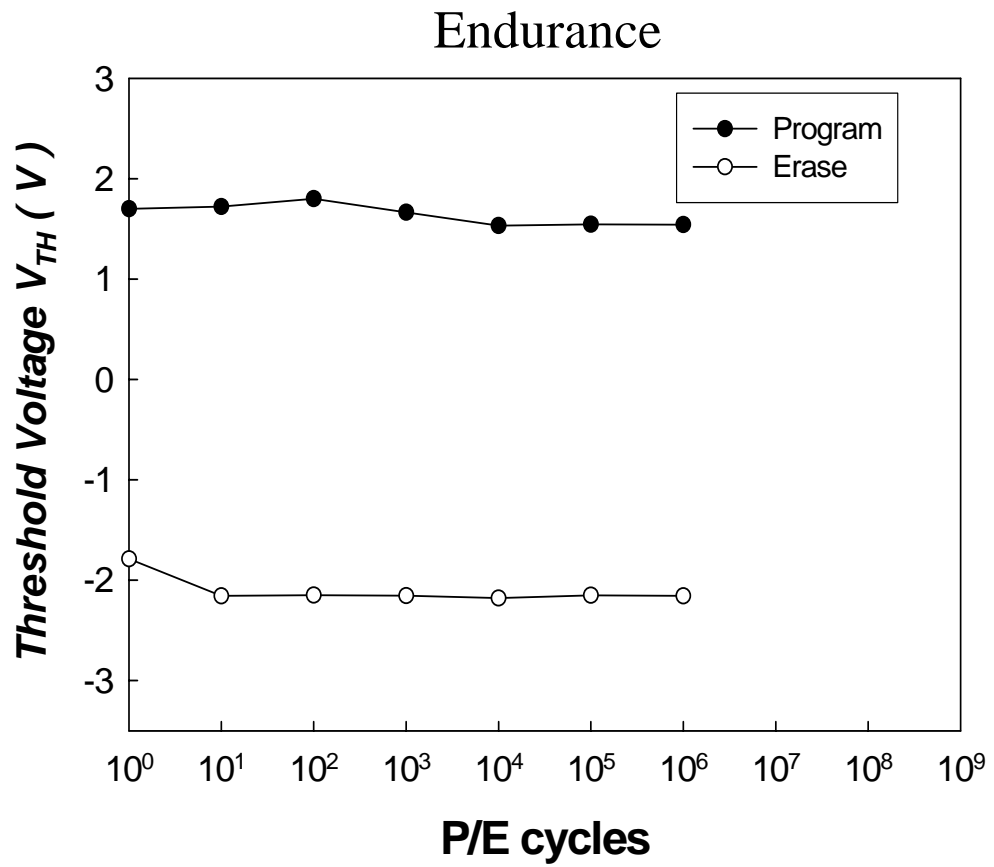
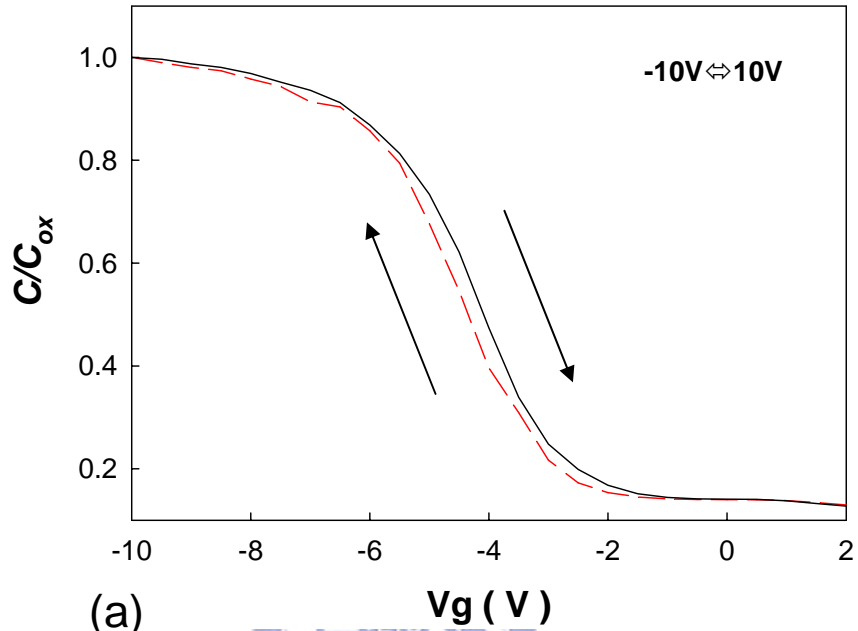


Figure 4-5 The endurance character of sample I with condition C (60 min dry oxidation).

# Sample II (with Capped Si layer)

Dry oxidation 30 min



Dry oxidation 45 min

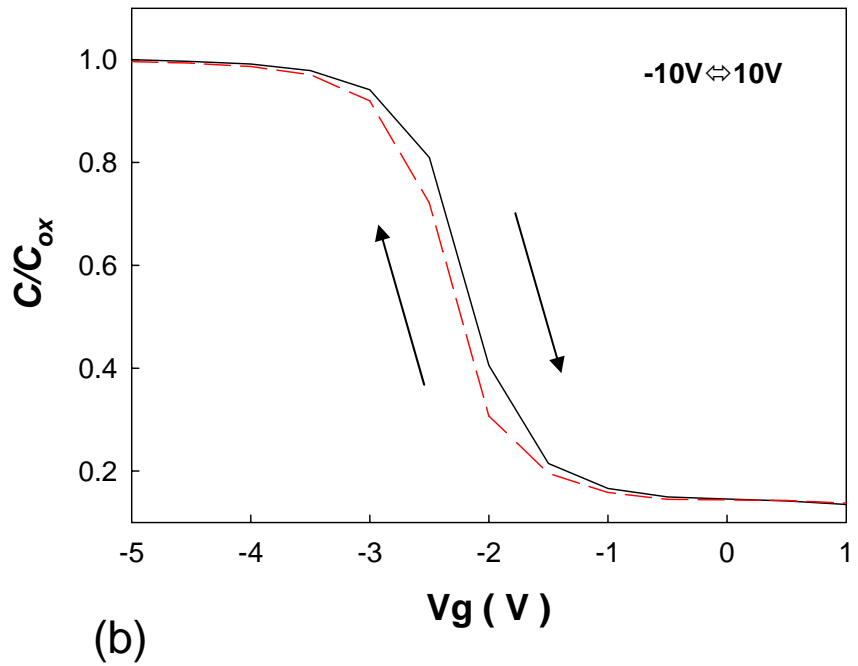
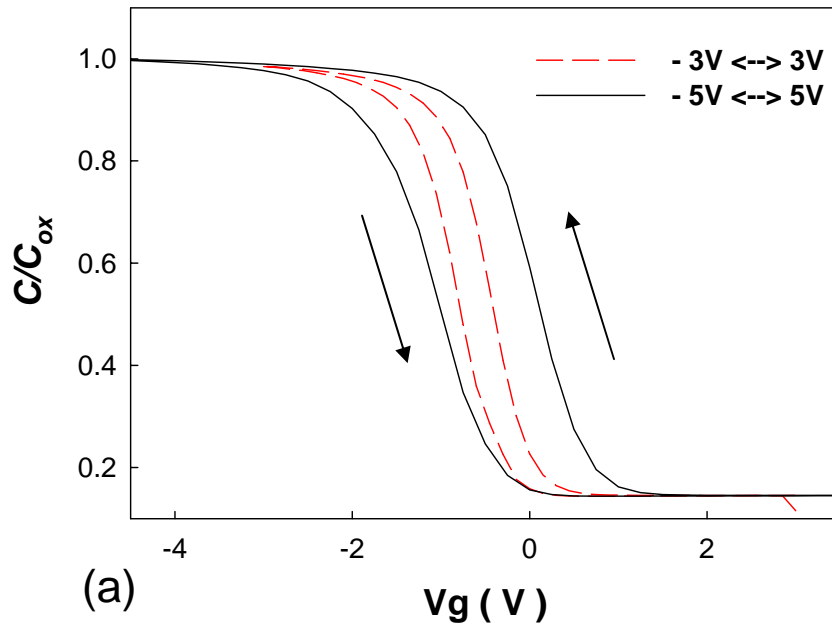


Figure 4-6 The C-V diagrams of sample II with (a) condition A and (b) condition B. Both diagrams are gate injection.

# Sample II

(with Capped Si layer)

Dry oxidation 60 min



Dry oxidation 30 min + steam treatment 3 min

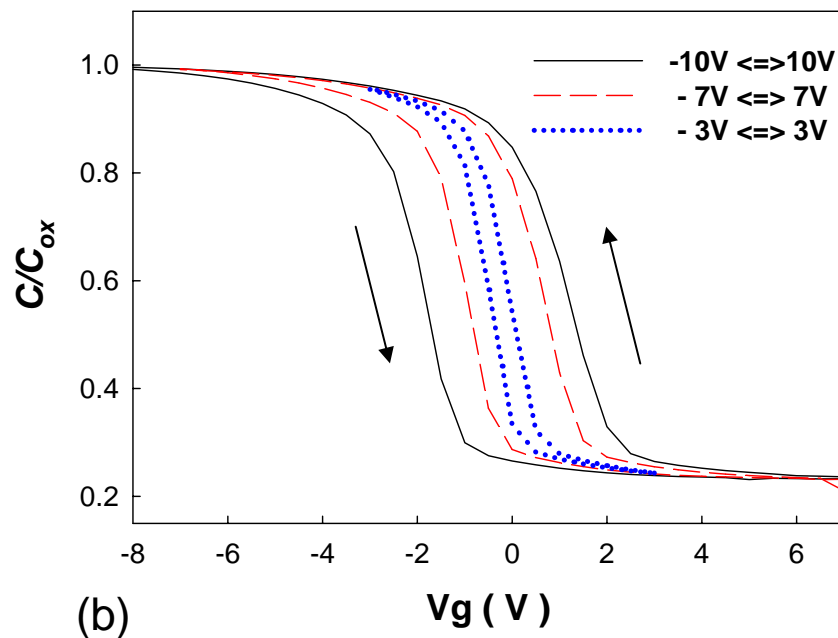


Figure 4-7 The C-V diagrams of sample II with (a) condition C and (b) condition D. Both diagrams are substrate injection.



# Sample II

(with Capped Si layer)

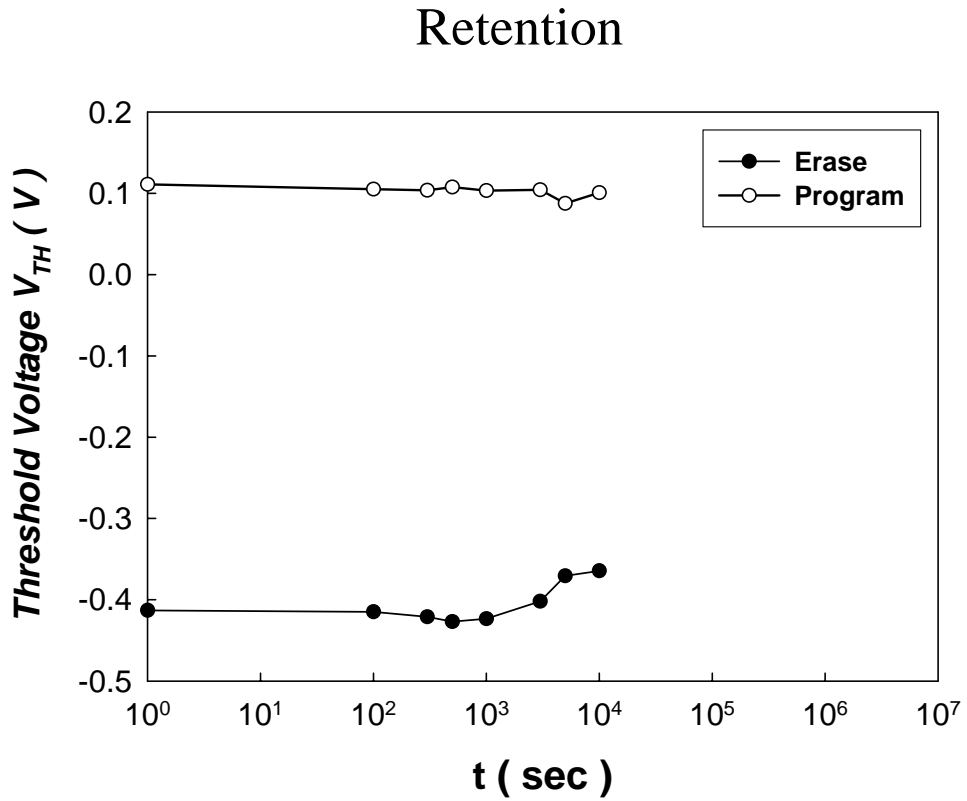


Figure 4-8 The retention character of sample II with condition D (30 min dry oxidation + 3 min steam treatment).

# Sample II

(with Capped Si layer)

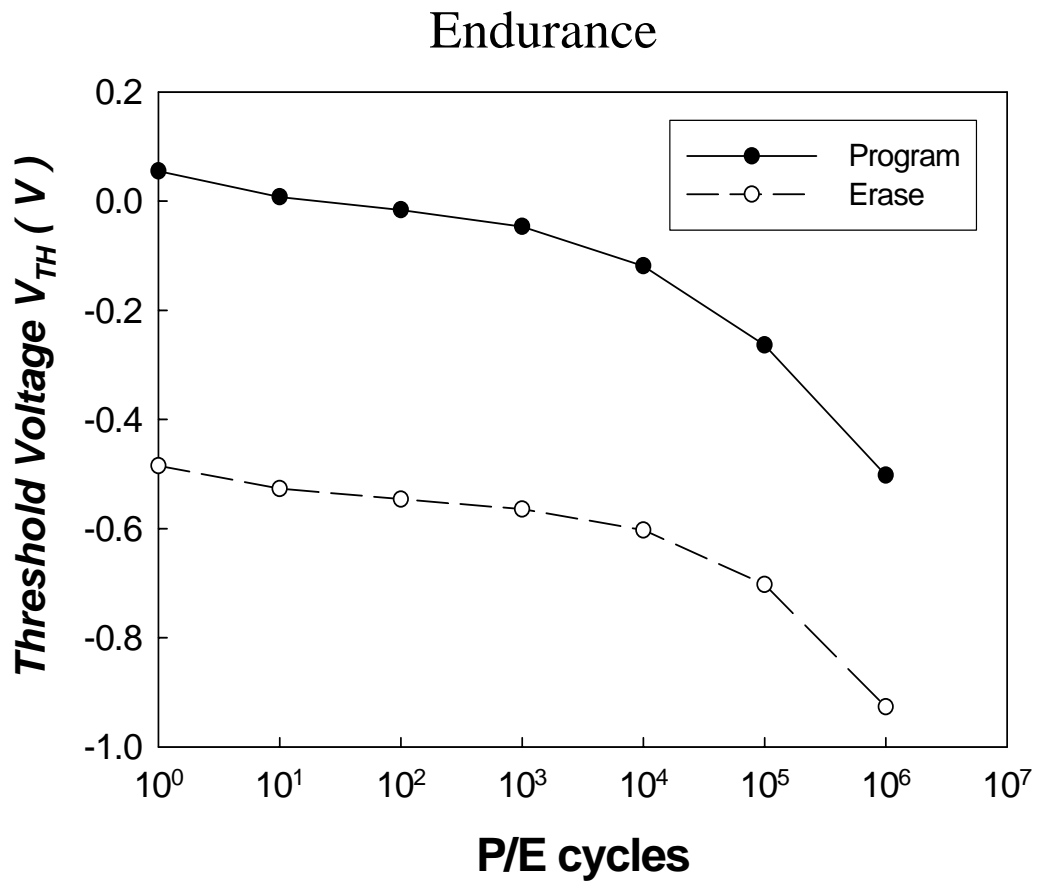


Figure 4-9 The endurance character of sample II with condition D (30 min dry oxidation + 3 min steam treatment).

# Sample I

(w/o Capped Si layer)

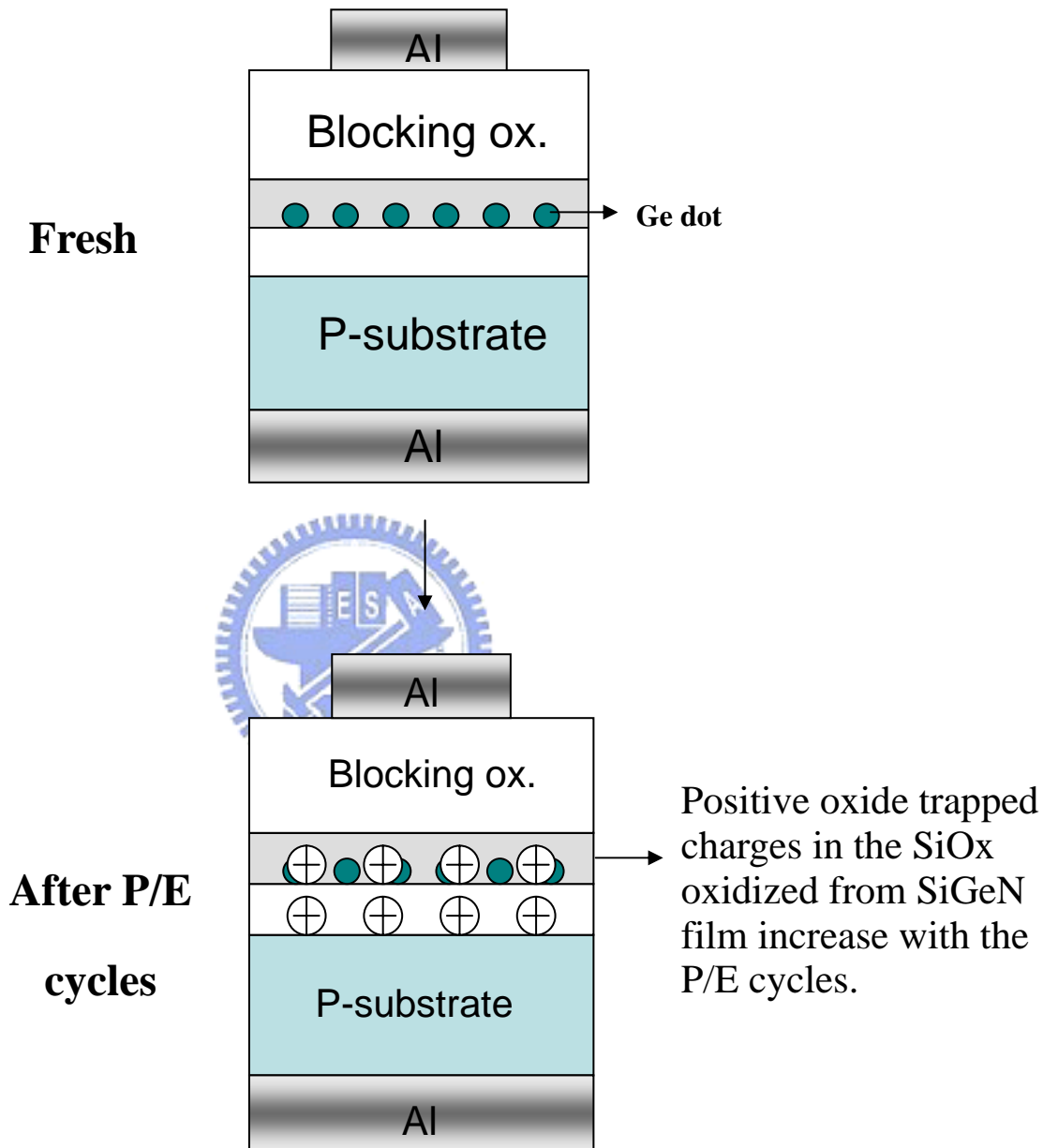


Figure 4-10 The schematic plot of positive oxide trapped charges in the SiOx oxidized from SiGeN film.

# The Ge Nanocrystal Only NVM

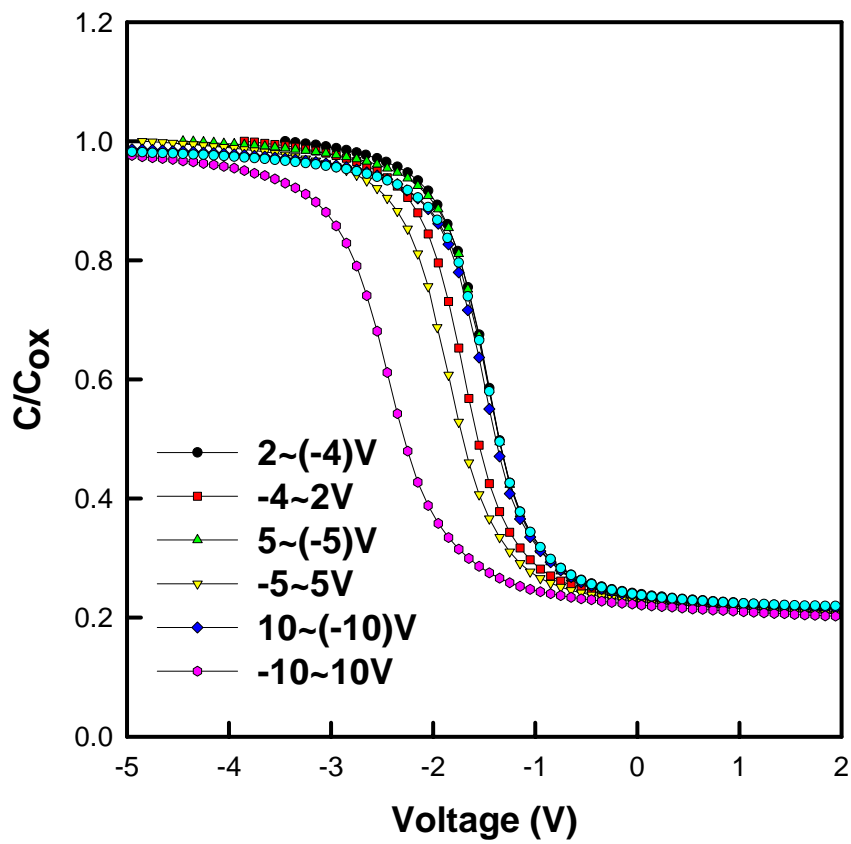


Figure 4-11 The C-V hysteresis of Ge nanocrystals embedded in  $\text{SiO}_2$  (Ge nanocrystal only) nonvolatile memory proposed by T. C. Chang et al. [3.1]

# The SONOS Only NVM

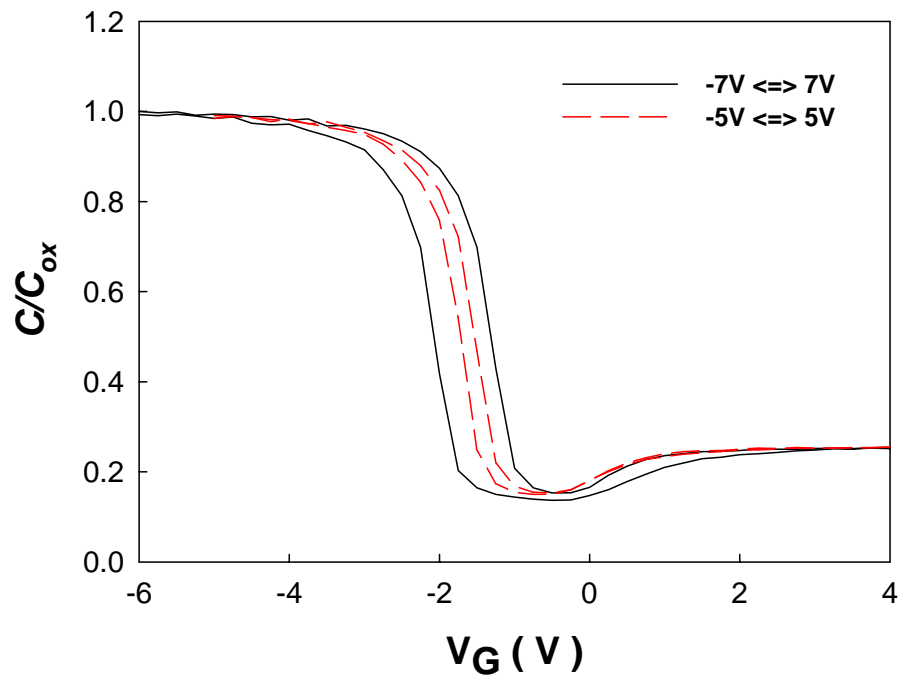


Figure 4-12 The C-V hysteresis of SONOS memory.

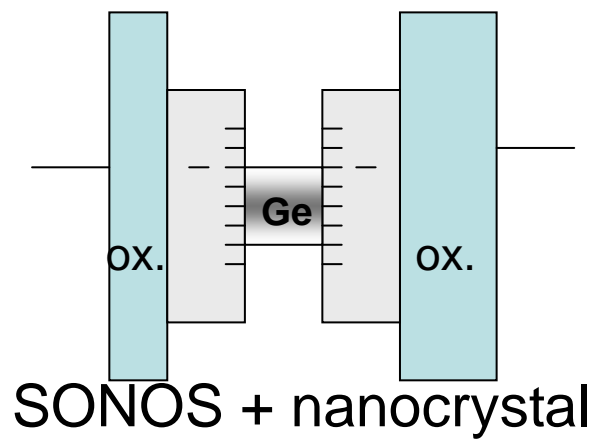
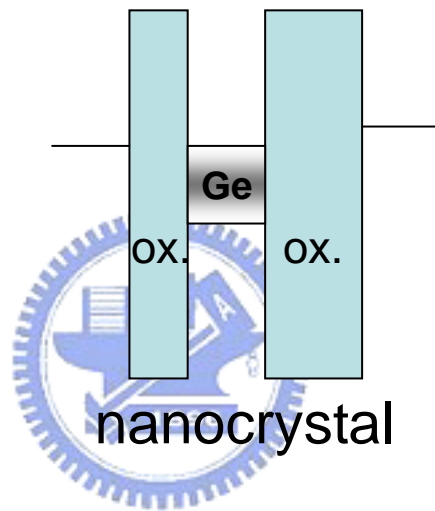
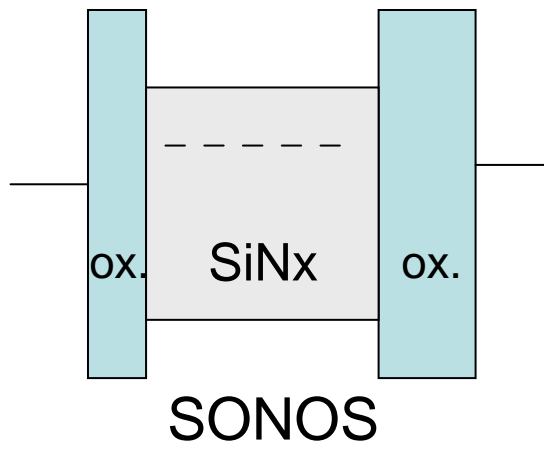


Figure 4-13 The band diagrams of SONOS, Ge nanocrystal and SONOS+ Ge nanocrystal NVSMs.

# Sample I

(w/o Capped Si layer)

## FTIR

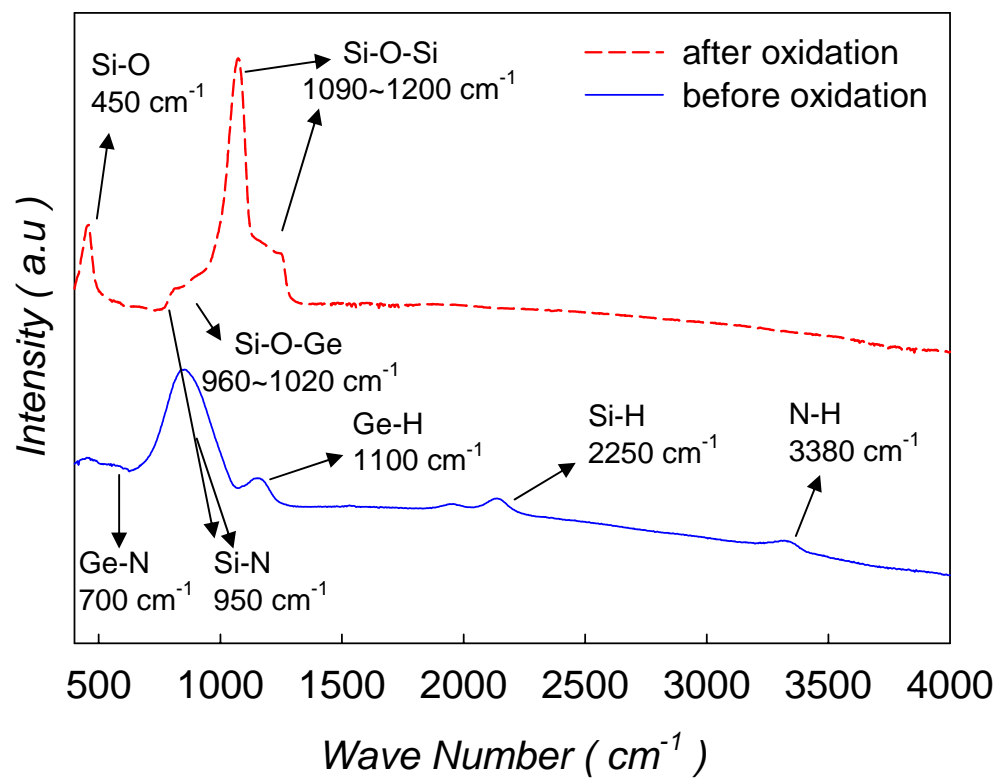
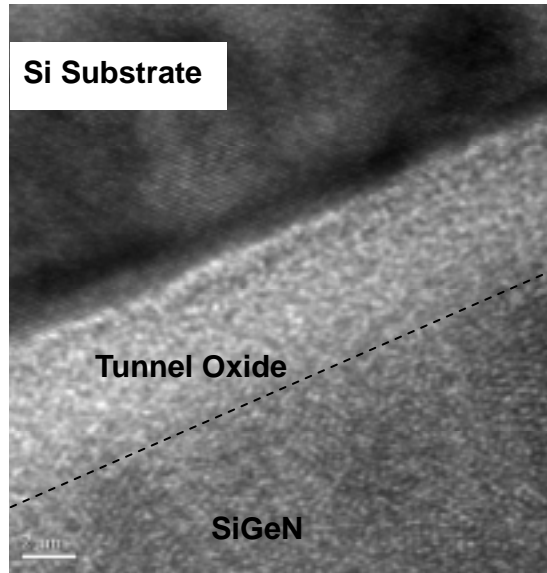


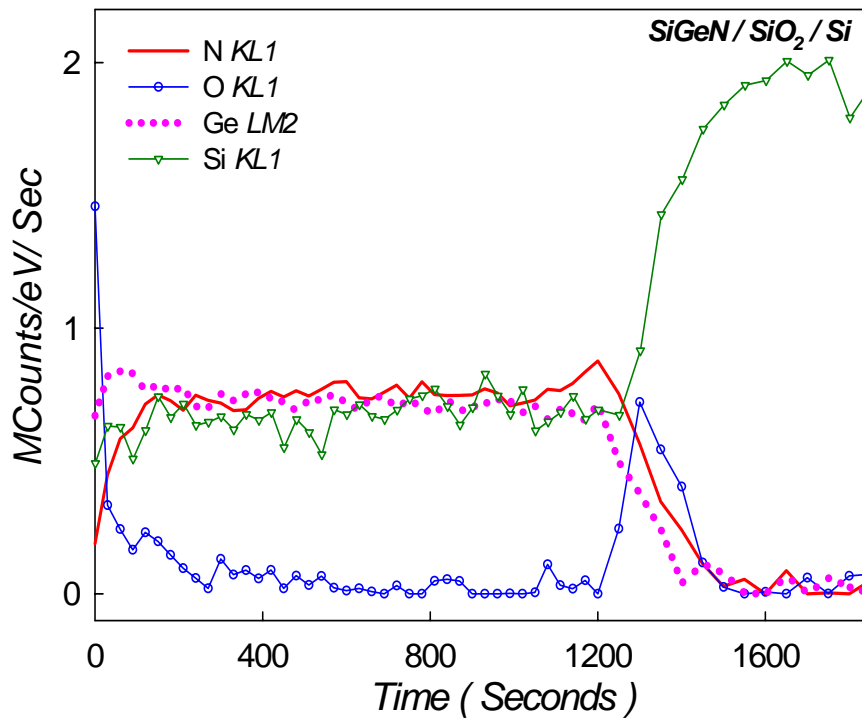
Figure 4-14 The Fourier Transform Infrared Rays (FTIR) spectra of sample I before and after thermal oxidation process.

# Sample I

(w/o Capped Si layer)  
Before Oxidation



(a)



(b)

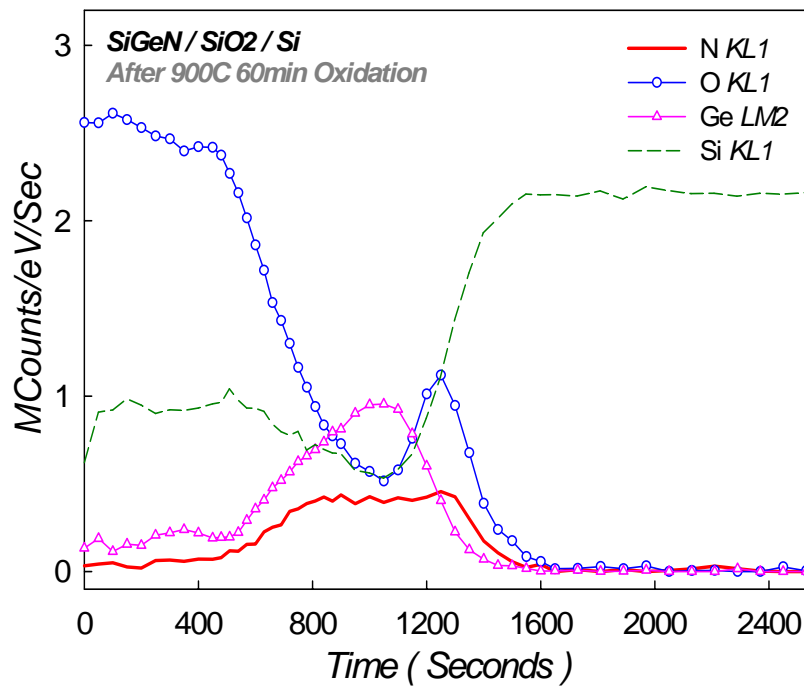
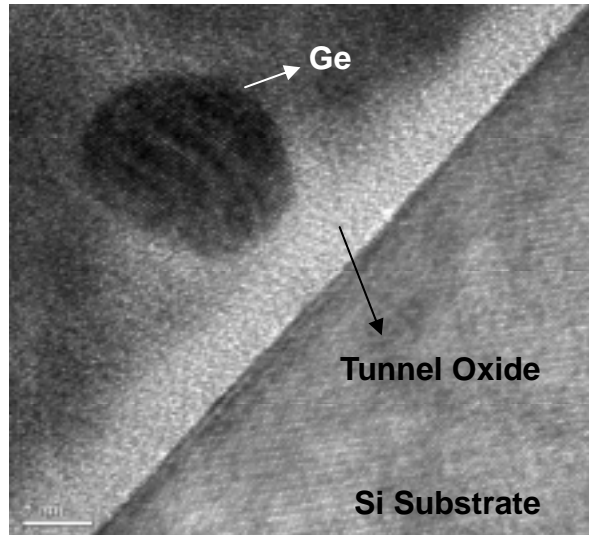
Figure 4-15 (a) The TEM diagram and (b) AES analysis of sample I before oxidation.



# Sample I

(w/o Capped Si layer)

After 60 min Oxidation



(b)

Figure 4-16 (a) The TEM diagram and (b) AES analysis of sample I after 60 min oxidation.

# Sample I

(w/o Capped Si layer)

## Raman Analysis

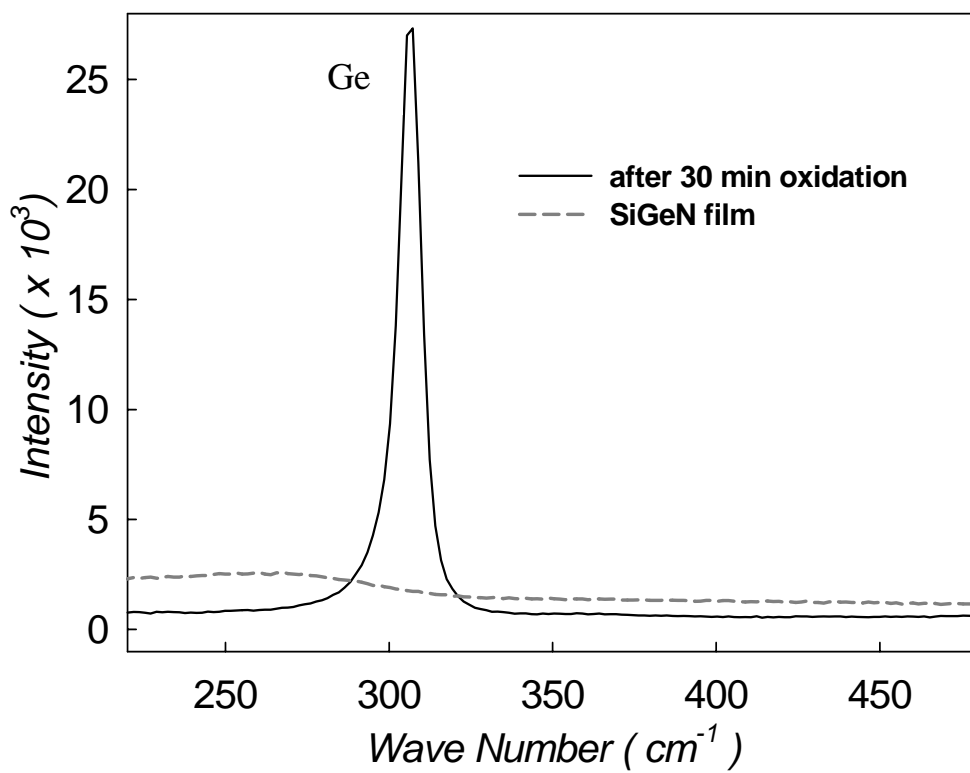


Figure 4-17 The Raman spectra of sample I before and after dry oxidation process. A peak of Ge crystal appeared after oxidation.

# Sample I

(w/o Capped Si layer)

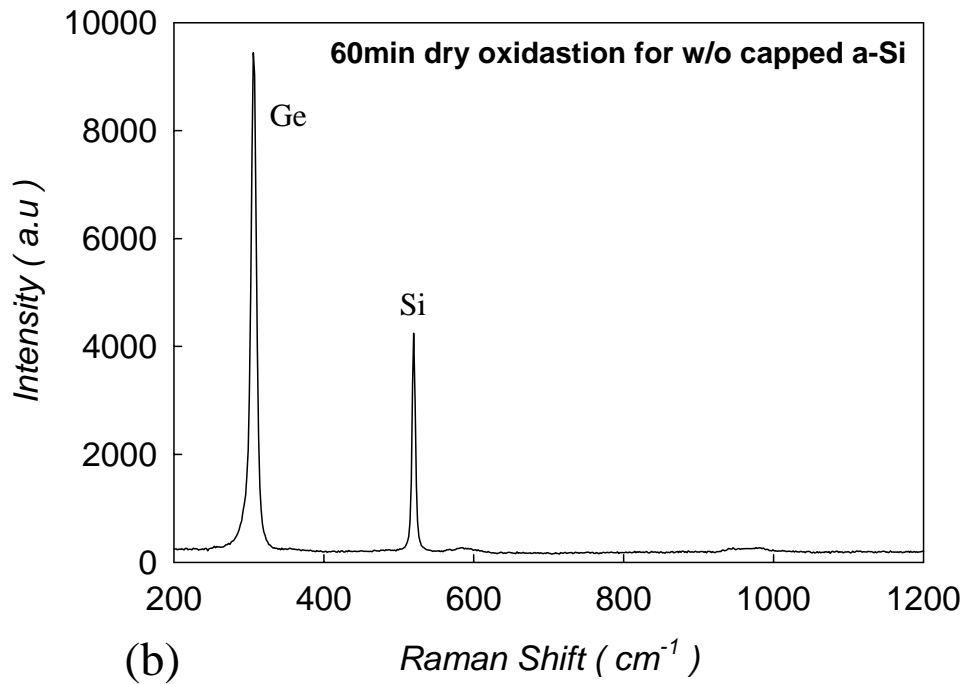
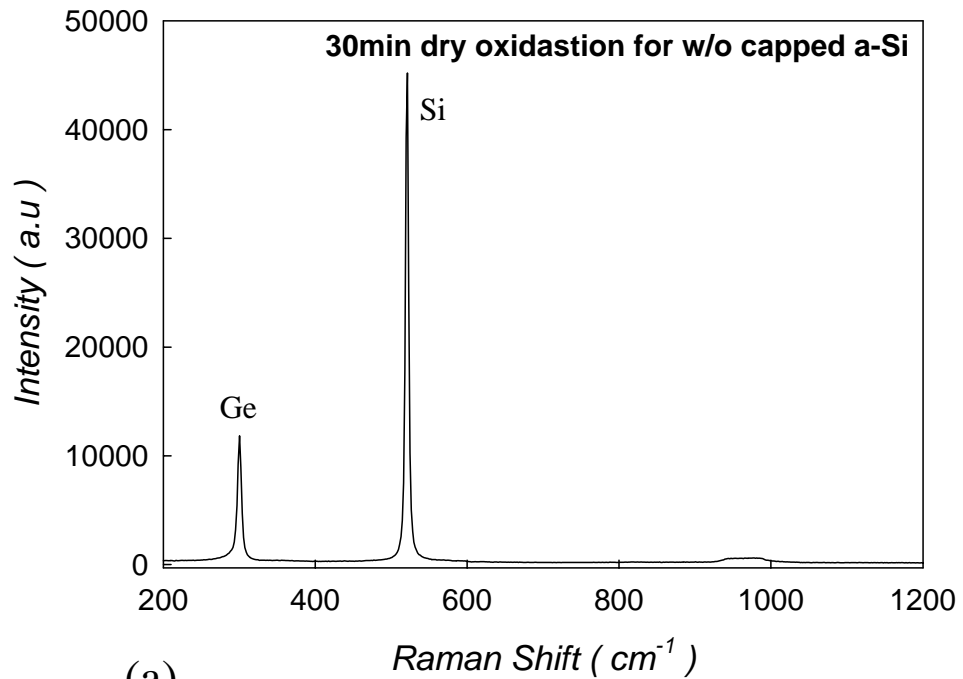


Figure 4-18 The Raman spectra of sample I with (a) 30 min short term and (b) 60 min long term dry oxidation.

# Sample II

(with Capped Si layer)

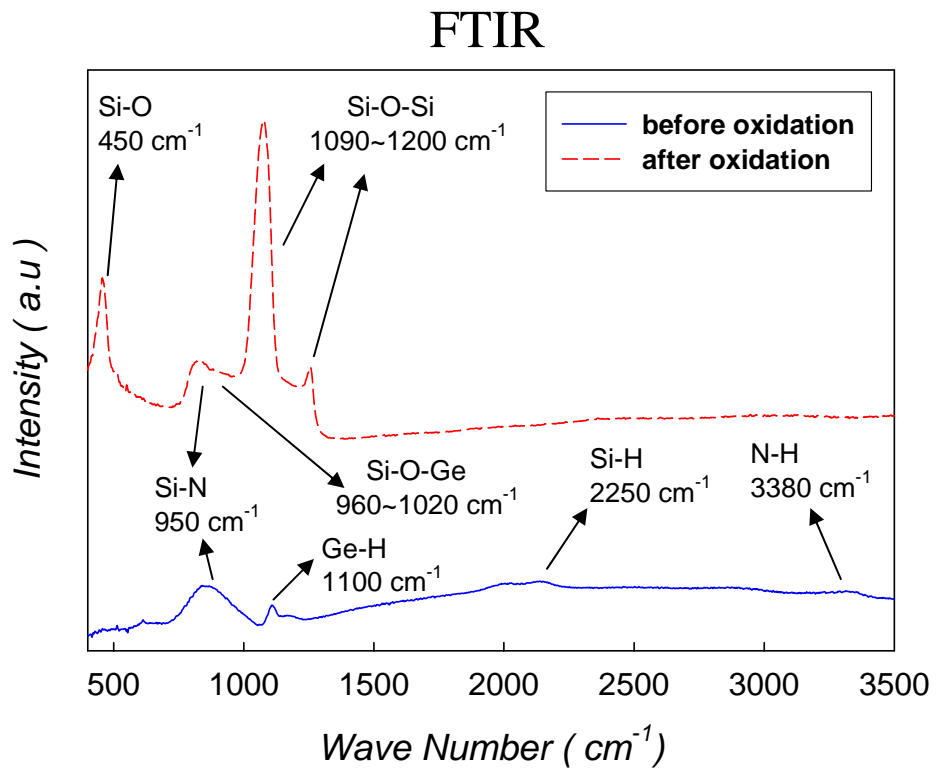
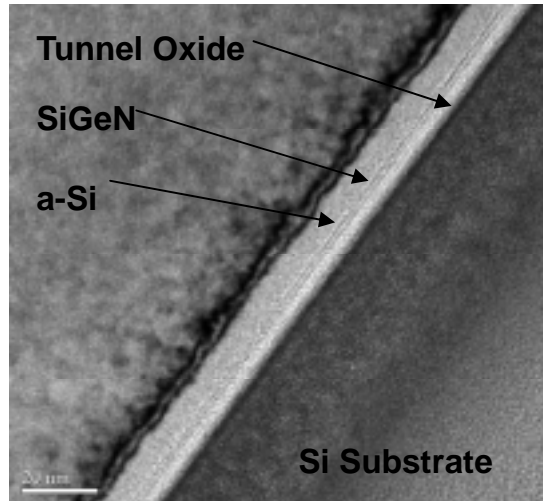


Figure 4-19 The Fourier Transform Infrared Rays (FTIR) spectra of sample II before and after 60 min thermal oxidation process.

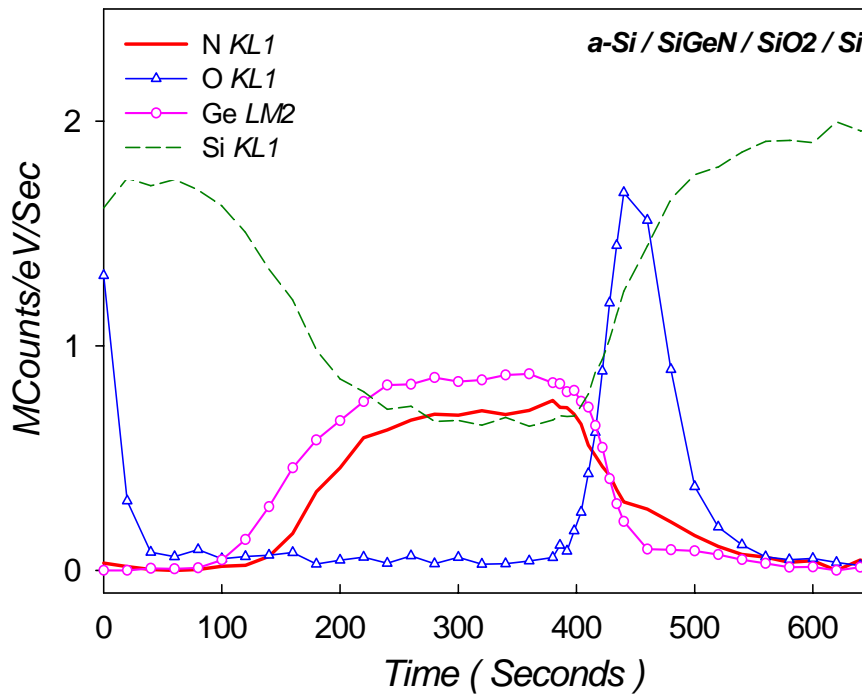
# Sample II

(with Capped Si layer)

## Before Oxidation



(a)



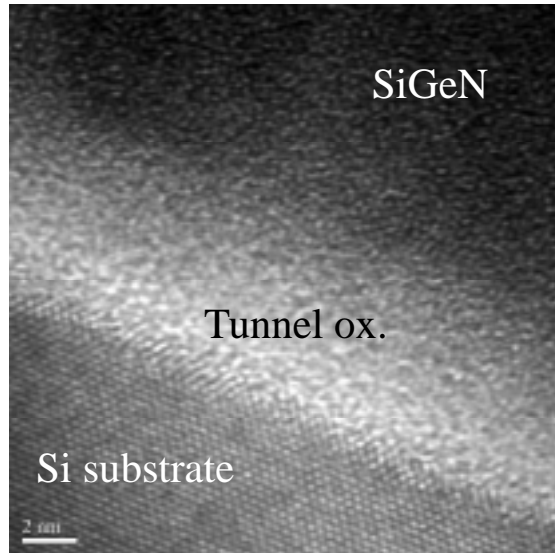
(b)

Figure 4-20 (a) The TEM diagram and (b) AES analysis of sample II before oxidation.

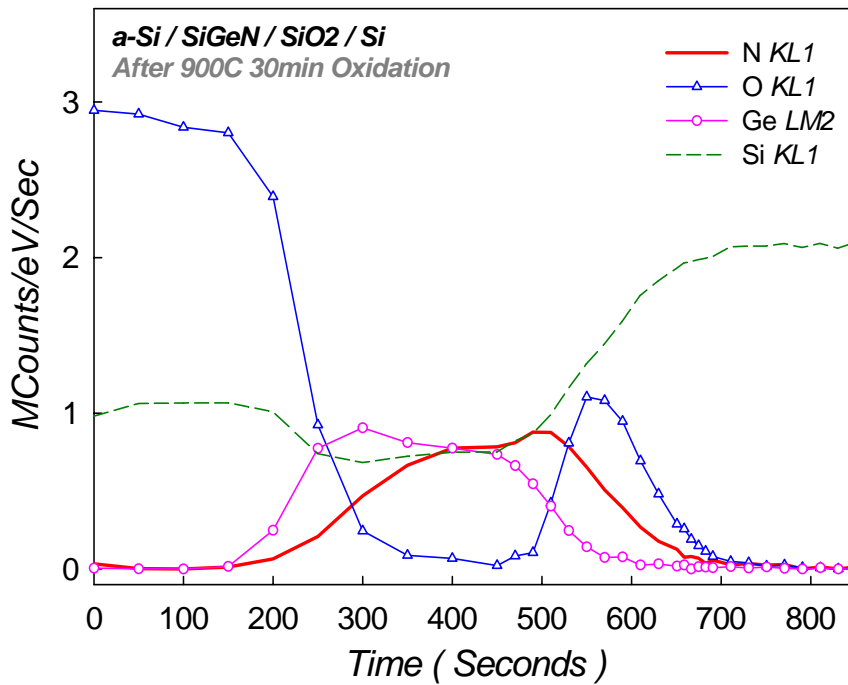
# Sample II

(with Capped Si layer)

After 30 min Oxidation



(a)



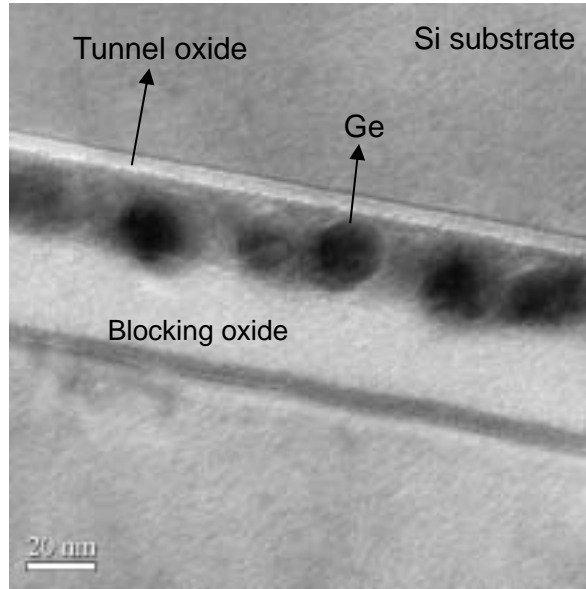
(b)

Figure 4-21 (a) The TEM diagram and (b) AES analysis of sample II after 30 min oxidation.

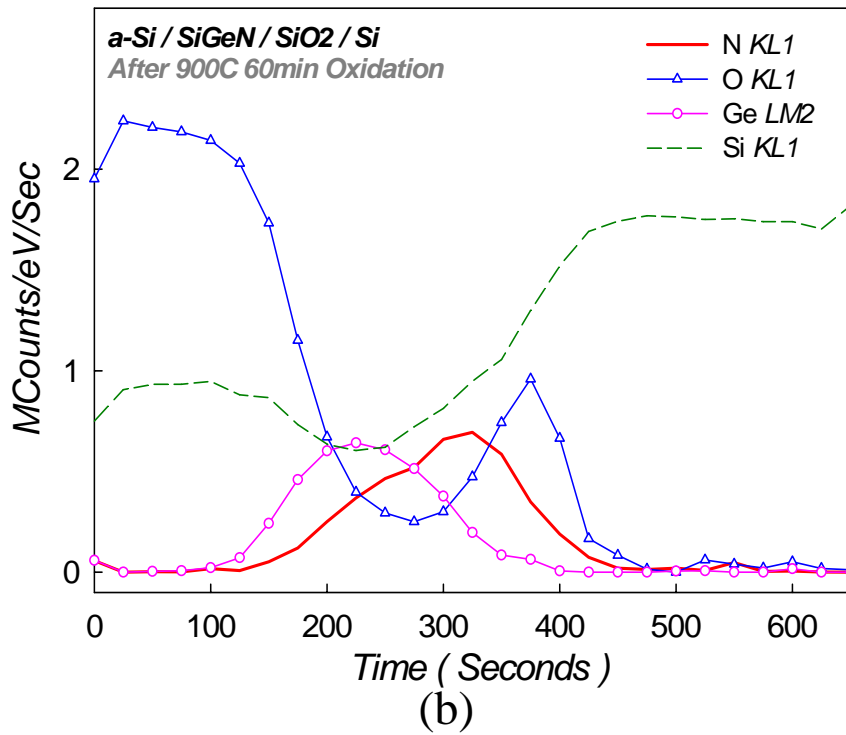
# Sample II

(with Capped Si layer)

After 60 min Oxidation



(a)



(b)

Figure 4-22 (a) The TEM diagram and (b) AES analysis of sample II after 60 min oxidation.

# Sample II

(with Capped Si layer)

## Raman Analysis

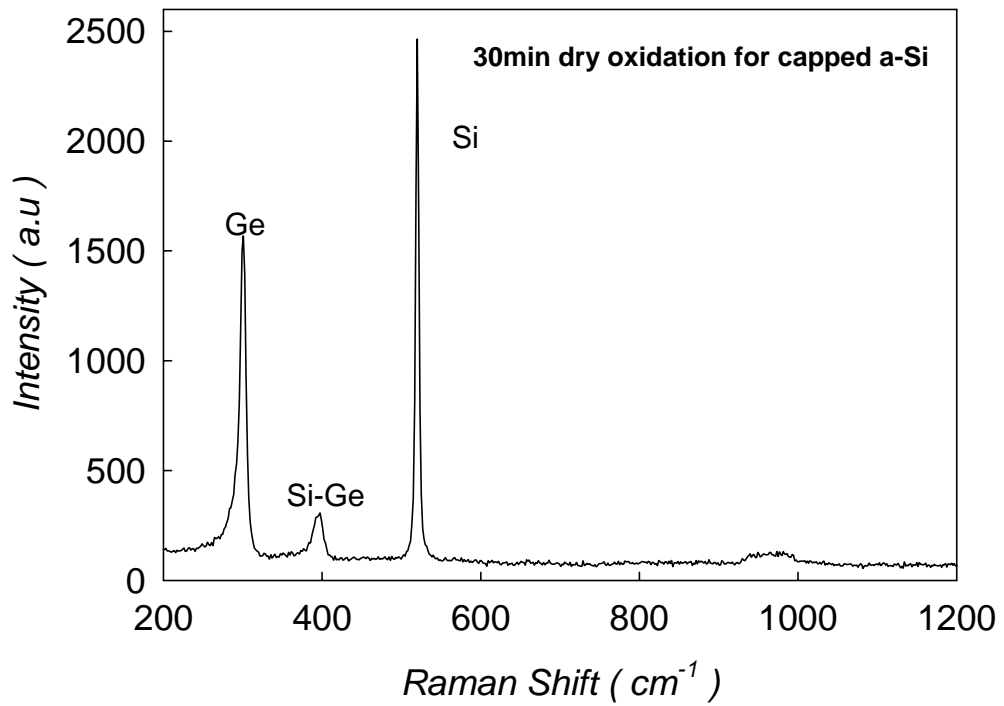


Figure 4-23 The Raman spectrum of sample II with 30 min dry oxidation.



# Sample II

(with Capped Si layer)

## Raman Analysis

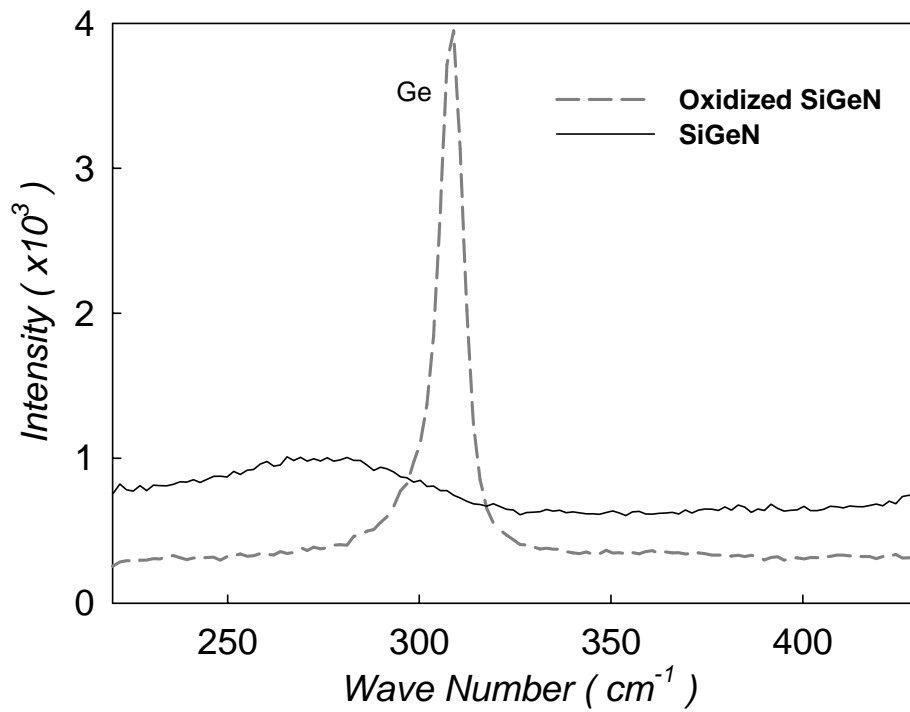
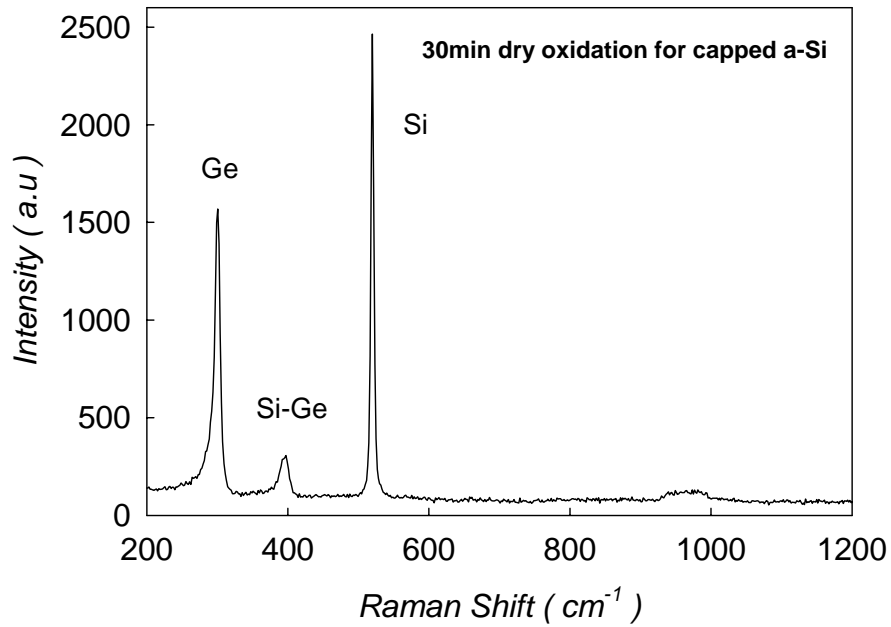


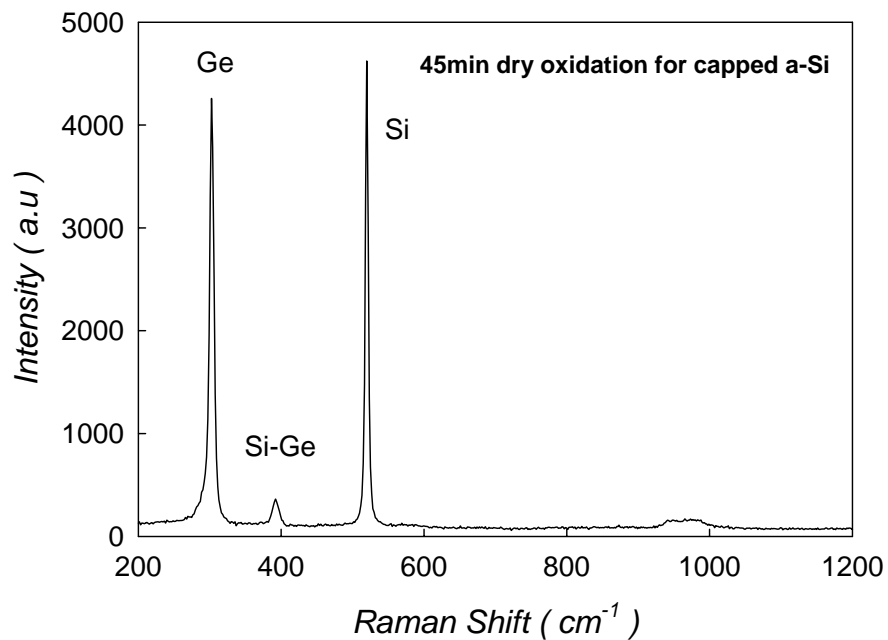
Figure 4-24 The Raman spectra of sample II before and after dry oxidation process. A peak of Ge crystal appeared after oxidation.

# Sample II

(with Capped Si layer)



(a)



(b)

Figure 4-25 The Raman spectra of sample II with (a) 30 min short term and (b) 45 min longer term dry oxidation.

# Sample I

(w/o Capped Si layer)

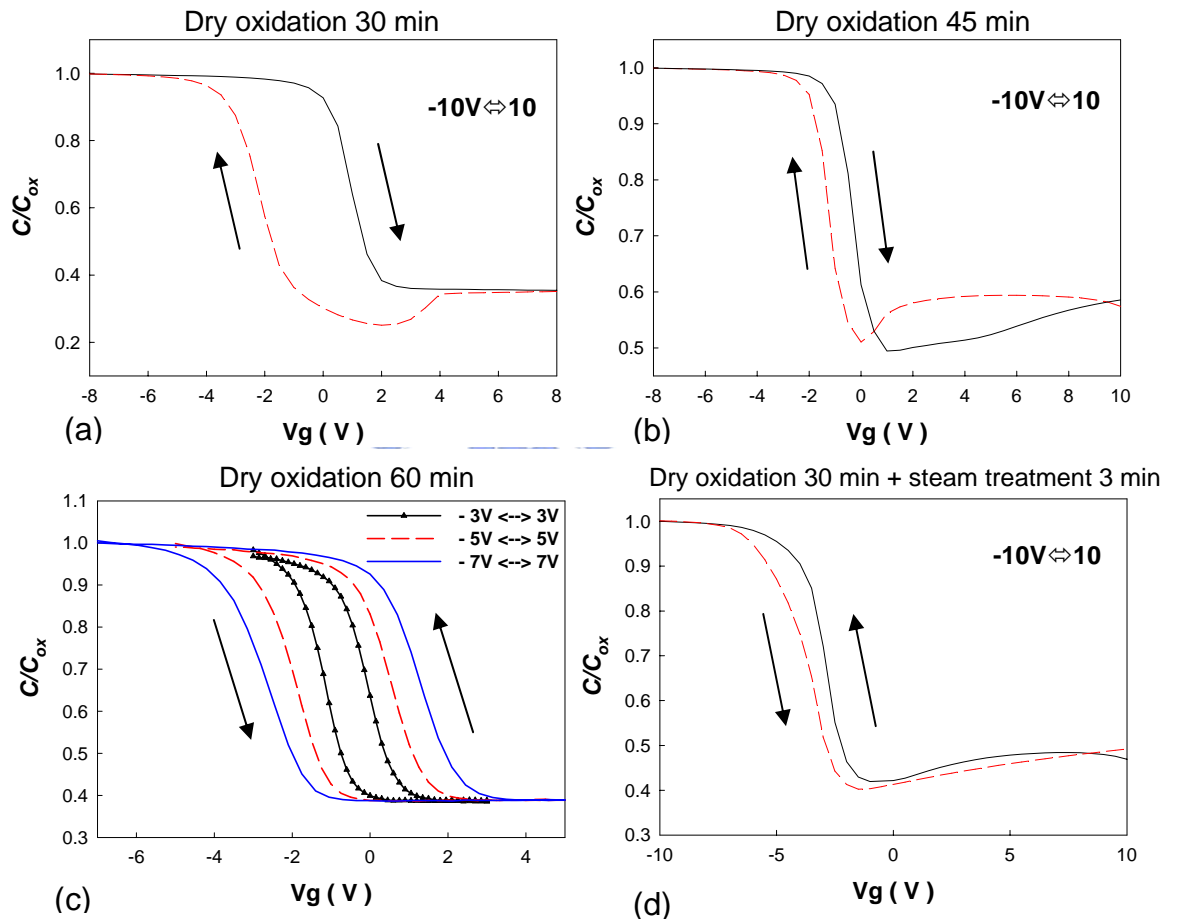


Figure 4-26 The C-V hysteresis of sample I with four different conditions (a) A, (b) B, (c) C, (d) D.

# Sample I

(w/o Capped Si layer)

## I-V Measurement

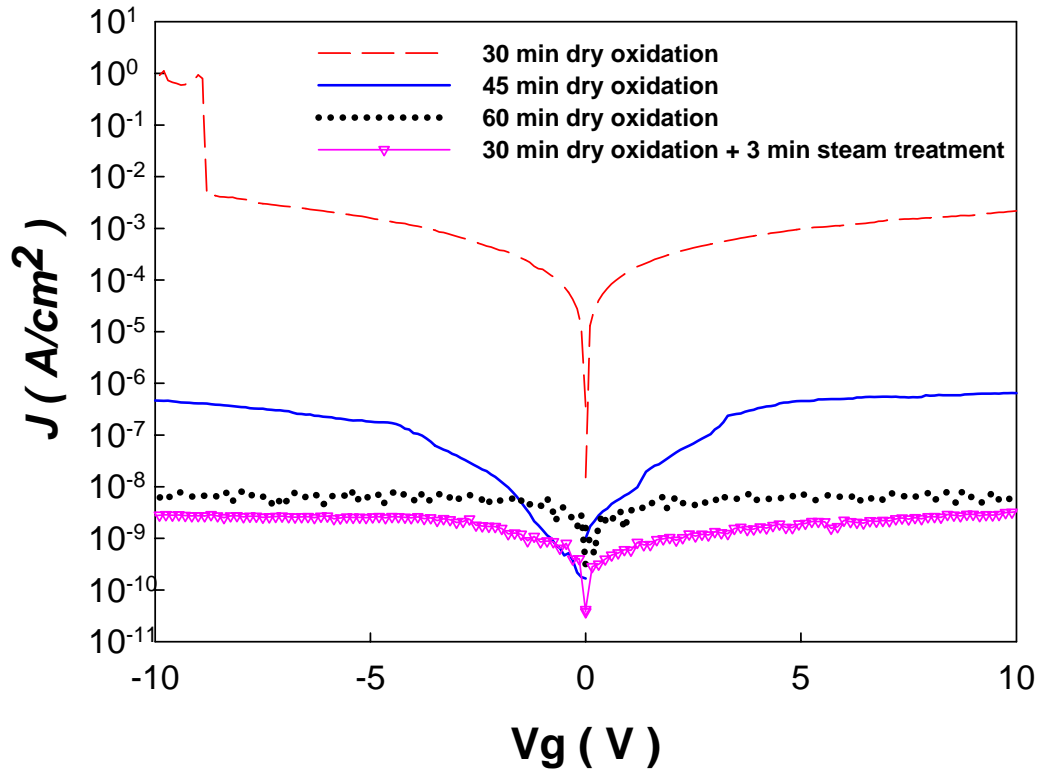
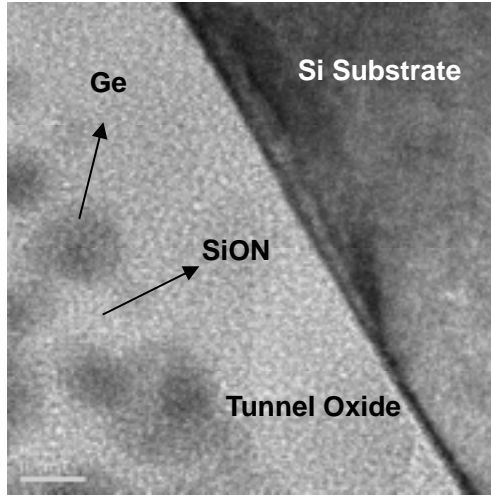


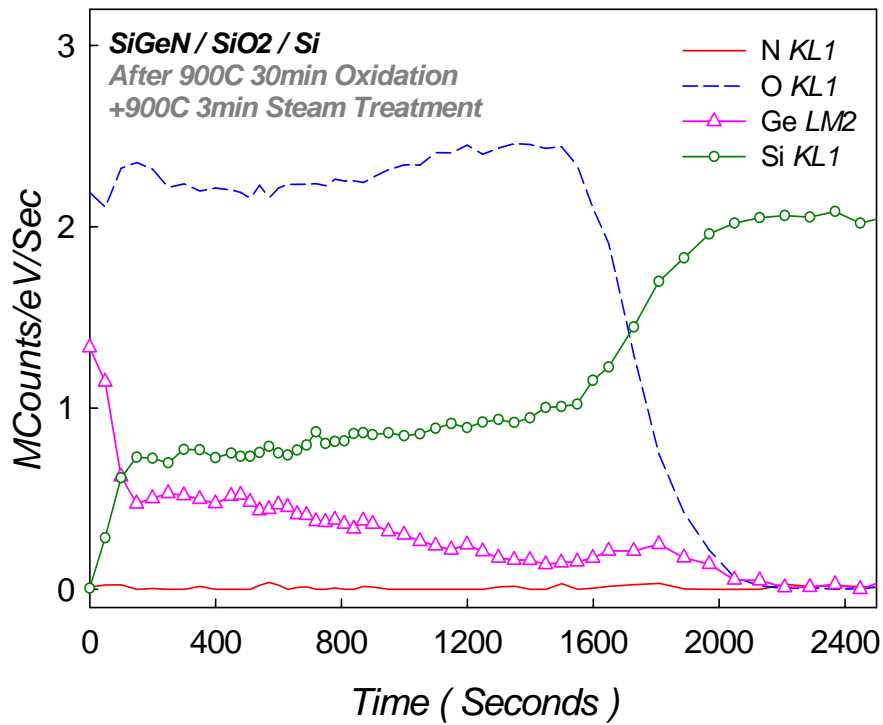
Figure 4-27 The I-V characteristics of sample I with four different conditions.

# Sample I

(w/o Capped Si layer)



(a)



(b)

Figure 4-28 (a)The TEM diagrams and (b) Auger Electron Spectroscopy (AES) analysis after oxidation with condition D (30 minutes dry oxidation plus 3 minutes steam treatment).

# Sample I

(w/o Capped Si layer)

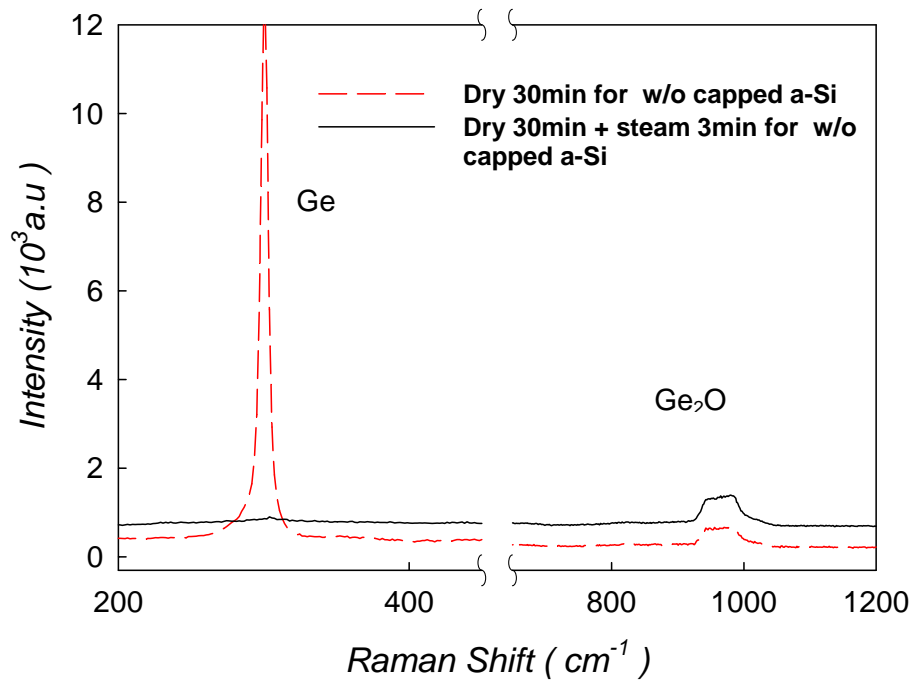


Figure 4-29 The Raman spectra of sample I after 30 min dry oxidation with and without 3 min steam treatment.

# Sample I

(w/o Capped Si layer)

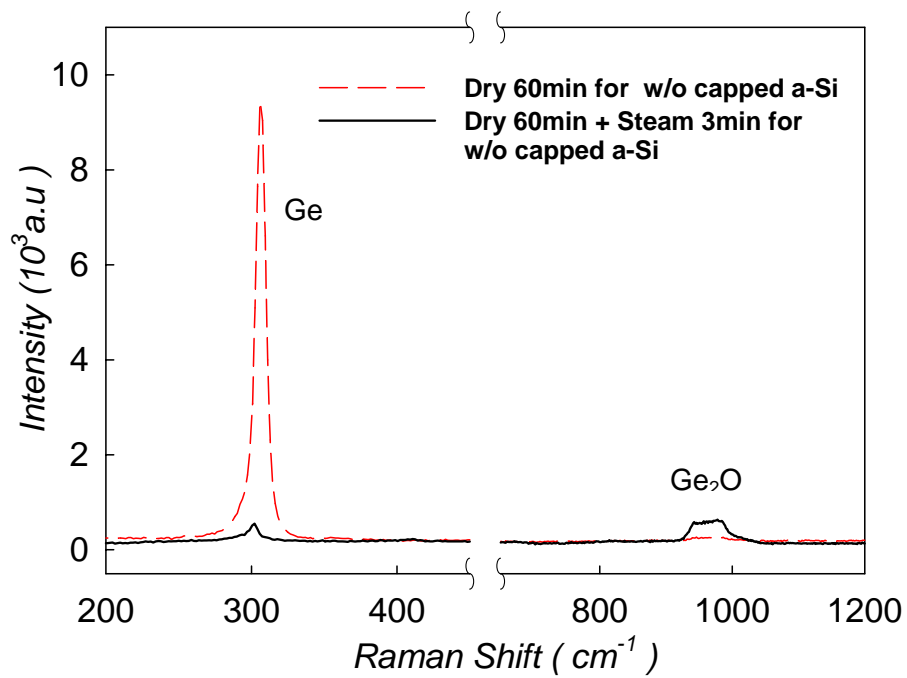


Figure 4-30 The Raman spectra of sample I after 60 min dry oxidation with and without 3 min steam treatment.

# Sample II

(with Capped Si layer)

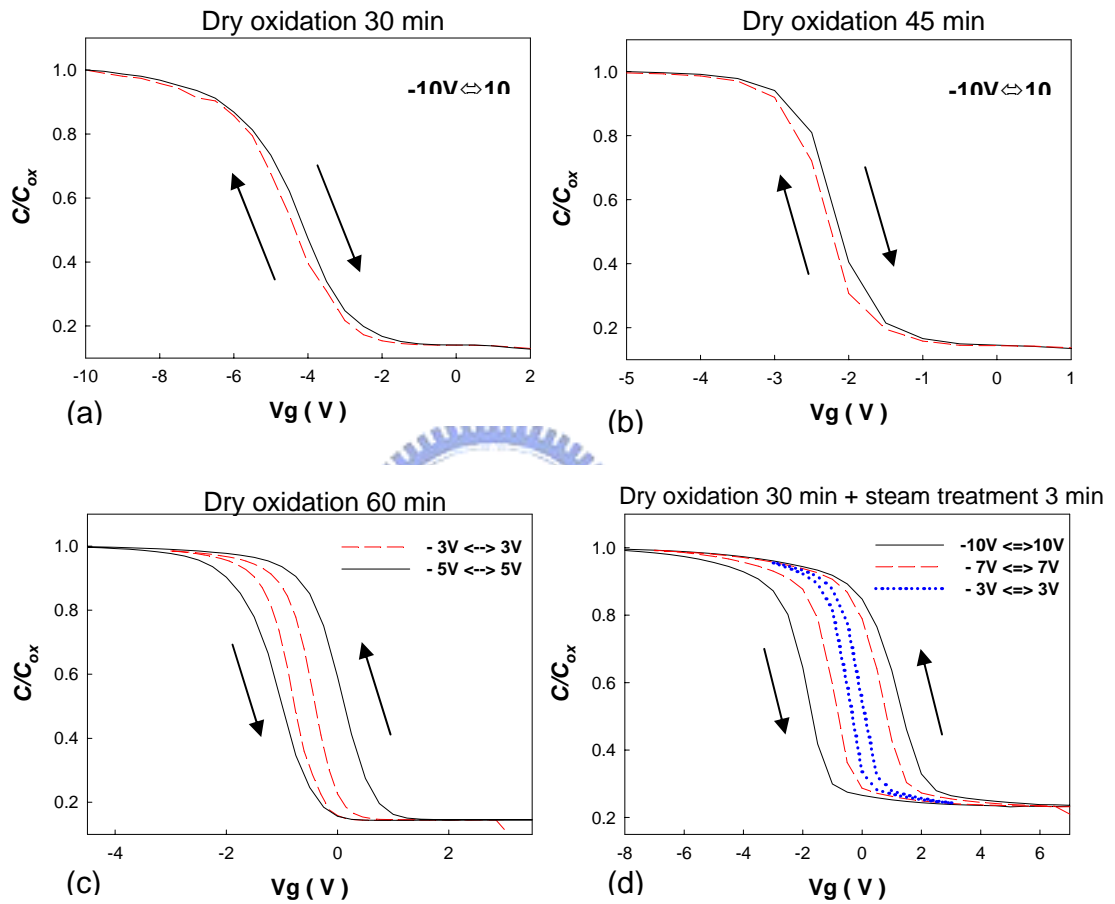


Figure 4-31 The C-V hysteresis of sample II with four different conditions (a) A, (b) B, (c) C, (d) D.



# Sample II

(with Capped Si layer)

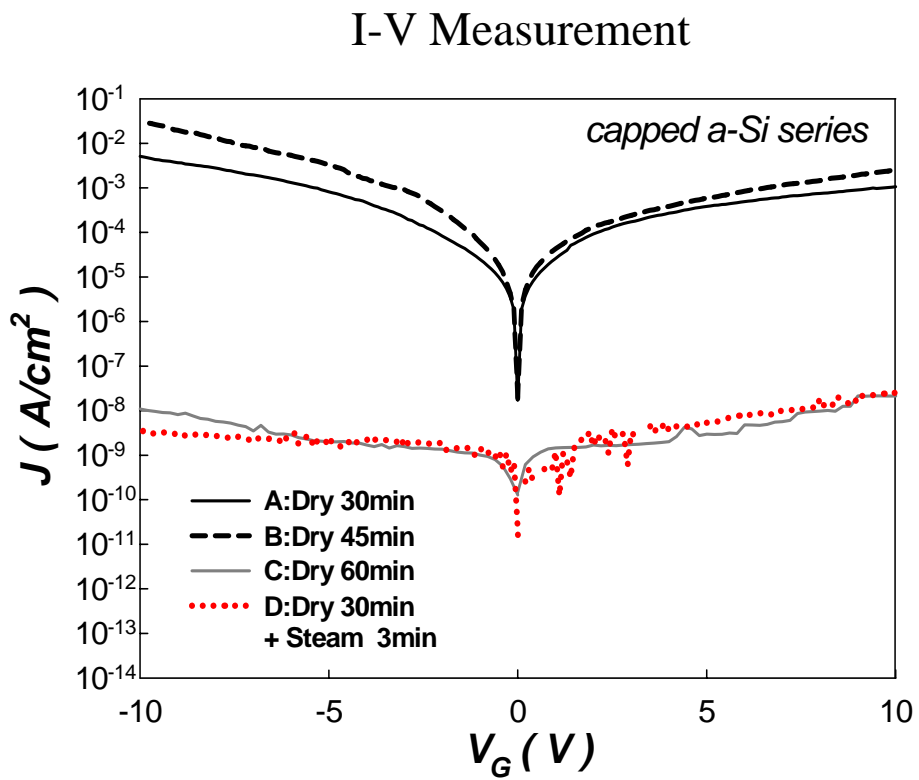
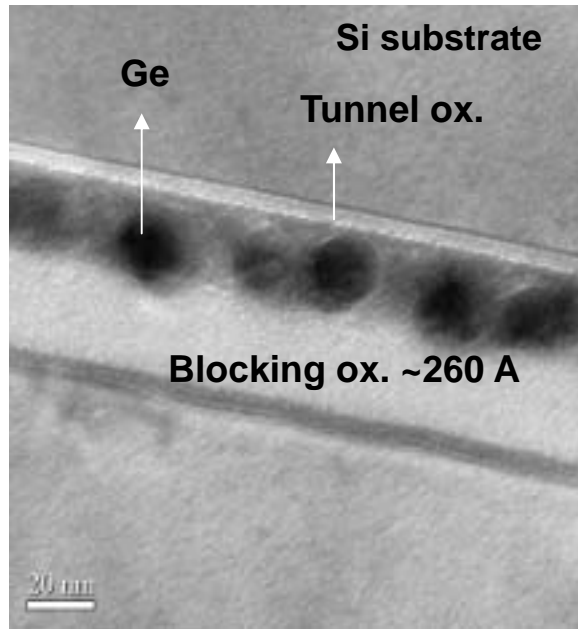


Figure 4-32 The I-V characteristics of sample I with four different conditions.

# Sample II

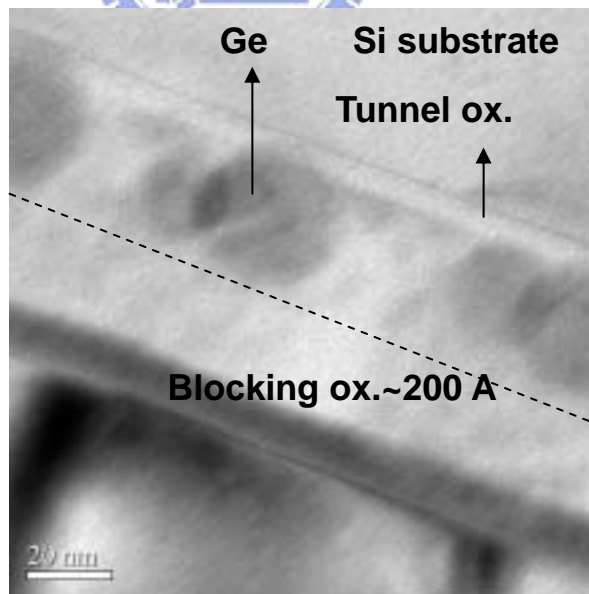
(with Capped Si layer)

After 60 min dry oxidation



(a)

After 30 min dry oxidation + 30 min steam treatment

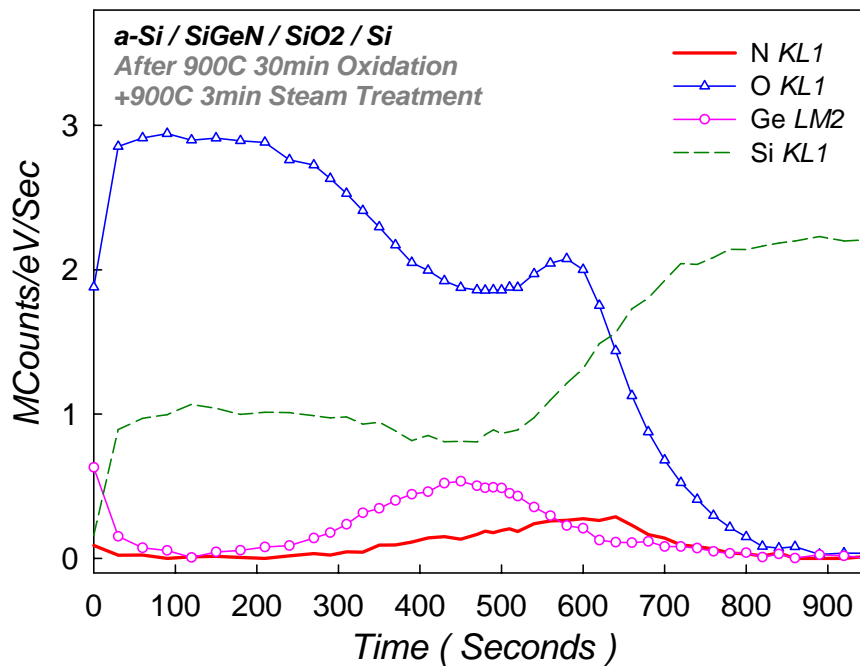
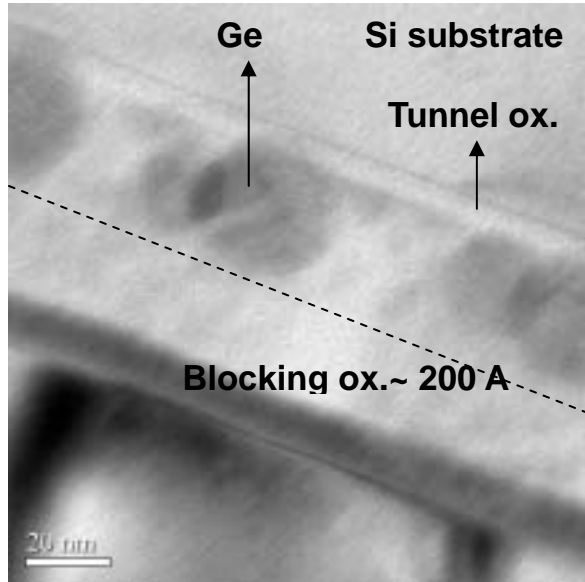


(b)

Figure 4-33 The TEM diagrams of (a) 60 minutes dry oxidation and (b) 30 minutes dry oxidation plus 3 minutes steam treatment.

# Sample II

(with Capped Si layer)



(b)

Figure 4-34 (a) The TEM diagrams and (b) Auger Electron Spectroscopy analysis after oxidation with condition D (30 minutes dry oxidation plus 3 minutes steam treatment).

# Sample II

(with Capped Si layer)

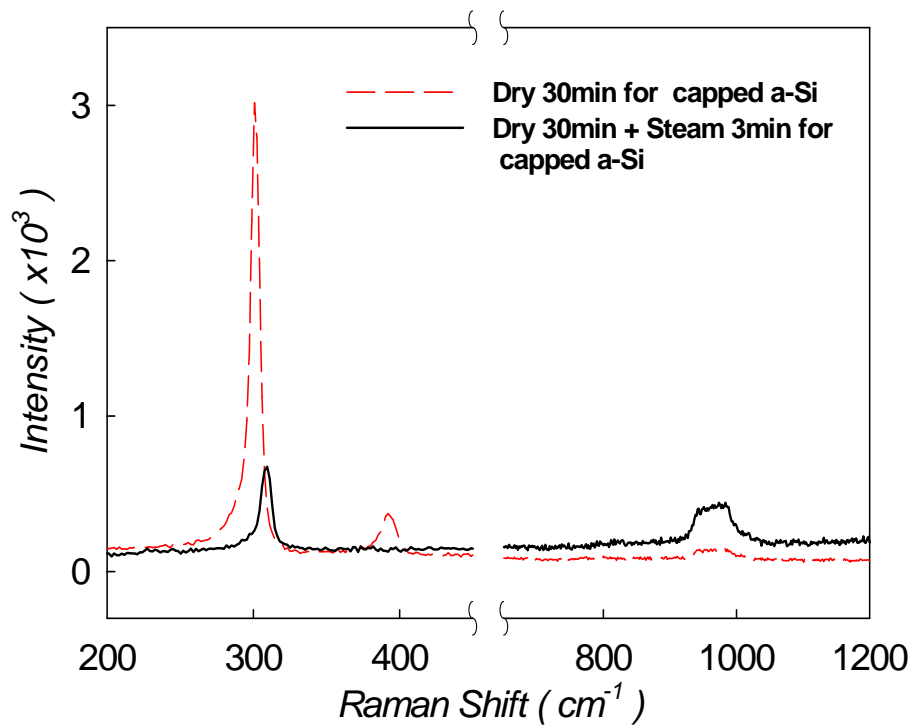


Figure 4-35 The Raman spectra of sample II after 30 min dry oxidation with and without 3 min steam treatment.

# Sample II

(with Capped Si layer)

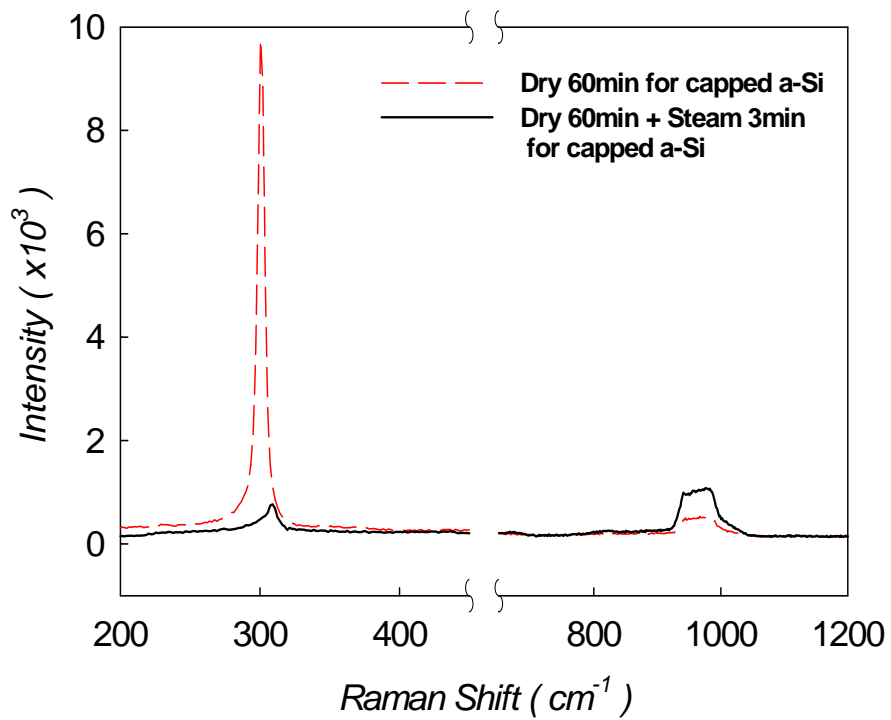


Figure 4-36 The Raman spectra of sample II after 60 min dry oxidation with and without 3 min steam treatment.

## Chapter 5

### Conclusions

#### 5.1 Conclusions

In this study, a new NVSM which combine the nanocrystal NVSM with the SONOS NVSM is proposed and has been successfully fabricated and investigated. The memory windows both in sample I and sample II are larger than the Ge nanocrystal only NVSM or the SONOS only NVSM because of the incorporation of the both charge trapping units, the Ge nanocrystal and the SiN<sub>x</sub>, and additional Ge nanocrystals/SiON interface trapping units. The fabrication processes are comparable with the main stream of semiconductor fabrication.

During 900 °C dry oxidation process, the Ge atoms will be segregated downward until they reach the tunnel oxide surface and nucleate to form Ge nano-dots (or Ge nanocrystals) near the tunnel oxide(or gate oxide). The SiGeN film will be oxidized to form SiON film and meanwhile, the Ge in the SiGeN film will be segregated to form Ge nano-dots (or Ge nanocrystals) embedded by SiON dielectric near the tunnel oxide.

The introduction of 3 minutes steam treatment can improve the blocking oxide quality by passivating the dangling bonds in blocking oxide and the I-V character is comparable with 60 minutes long term dry oxidation. The blocking oxide formed by 30 minutes dry oxidation plus 3 minutes steam treatment is thinner than that formed by 60 minutes dry oxidation and there is almost no difference between both I-V characteristics, which proves that the blocking oxide quality is indeed improved. The introduction of steam treatment can not only improve the blocking oxide quality but also reduce the thermal process duration from 60 minutes to 33 minutes. However, if the steam

treatment time is too long, Ge-Ge bonds and Si-N bonds will be oxidized by steam. Therefore, to prevent the steam across the blocking oxide to oxidize Ge nanocrystals and SiON dielectric, the steam treatment duration must change with the thickness of blocking oxide.

The memory of Ge nanocrystals embedded in SiON dielectric is a potential candidate for future NVSM applications.



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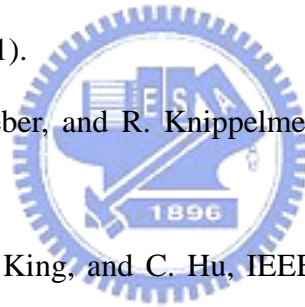
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論文題目：

**含鍺摻雜氮化矽薄膜在非揮發性記憶體應用之研究**

**Study on the Application of Ge-Incorporated Silicon**

**Nitride Thin Film for Nonvolatile Memory**