利用一種新穎結構進行複晶矽薄膜電晶體之熱載子可靠性分析

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摘　要

一種新穎測試結構被提出用來觀察複晶矽薄膜電晶體經過熱載子測試後所造成元件性能的衰退狀況。此新穎的元件結構，主要是在傳統結構通道的垂直方向額外做了三組感測電晶體。當測試元件在經過熱載子施壓時，利用感測電晶體來偵測通道不同區域的受損情況。除證實測試結構具有直接解析不同區域的受損差異外，實驗中也發現，由於感測電晶體能有效偵測元件早期受損的情形，因此具有提高偵測靈敏度之能力。

在實驗中將對此測試結構施以直流和交流應力去分析通道上不同區域的衰退機制。在直流應力的結果顯示，當施以閘極直流偏壓為汲極的三分之一時，此時元件受損程度最為嚴重，且受損位置主要位於靠近通道的汲極區域。在交流應力中，其頻率、上升時間、下降時間以及工作週率(duty cycle)等因素對於元件造成之影響進行深入研究與探討。在一個交流應力的週期中，除了當閘極和汲極偏

壓維持在高電壓會對元件造成影響外，訊號切換過程同樣也扮演很重要的角色。在交流偏壓施加在閘極的情況下，發現閘極電壓由高切換至低的階段會對元件造成額外的傷害，並且隨著下降時間的減少傷害會變的更加顯著。而在交流偏壓施加在汲極的情況下，汲極電壓由低切換至高的階段扮演關鍵的因素，尤其當上升時間愈短時則元件的傷害會隨之增加。在交流應力下訊號切換過程所產生額外的熱載子效應，可以用來解釋我們所觀察到元件衰退的現象。

A Study of Hot-Carrier Reliability for Poly-Si Thin-Film Transistors Using a Novel Test Structure

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ABSTRACT

A novel thin-film transistor test structure was fabricated and employed for monitoring the device hot-carrier (HC) degradations. Such test structure consists of three monitor transistors and one test transistor. The three monitor transistors have their source/drain pairs arranged in the direction perpendicular to the channel of the test transistor. This unique design allows us to monitor the degradation induced in different portions of the channel of the test transistor as it is undergone hot-carrier (HC) stress. Furthermore, it has been demonstrated that the unique design is capable of detecting the degradation characteristics of devices with very high sensitivity.

In the experiments both static and AC HC stress tests were applied to the test transistor of the structures. Results of the static stress test show that the damage is mainly induced near the drain-side of the stressed channel, and most serious

degradation of the test device occurs under static stress condition when V_G/V_D ratio is around 1/3. In the AC stress, the effects of several factors including frequency, rising time, falling time, and duty cycle, were investigated and discussed. In addition to the period while both gate and drain are being applied with high voltages, the transient stages are also found to play a major role in affecting the device characteristics. In the case when the pulsed voltage train is applied to the gate, extra degradation is induced in the voltage falling stage and becomes more significant as the falling time is decreased. When the pulsed voltage train is applied to the drain, voltage rising stages are the key factor for the degradation and the degradation increases with decreasing rising time. The generation of extra hot carriers during the transient stages is used to explain the findings.

誌　謝

首先要感謝的是我的指導教授，黃調元博士與林鴻志博士。謝謝你們這幾年來在研究上對我的細心指導，從你們身上我學習到做事應有的態度與研究的精神，令我受益良多。在當研究生這段時間，可以留在林博和黃老師身旁學習真的是讓我覺得是自己非常幸運。

同時還要感謝實驗室的其他夥伴們這幾年來給我的協助。首先感謝李明賢學長的照顧，謝謝你不厭其煩的教導我實驗上的事還有解答我生活中任何疑難雜症，對於剛進入實驗室的我幫助很大。再來還有感謝蘇俊榮學長在實驗上的幫助及研究上的建議，你對於研究的投入、熱忱及態度，都是我學習的榜樣。此外，還要感謝呂嘉裕學長、李耀仁學長、葉冠麟學長、盧文泰學長、林宏年學長、盧景森學長、林哲民學長、張伊鋒學長、藍文廷學長、李聰杰學長、房新原學長、林賢達學長們所給予的關懷與鼓勵。再來是同期的碩班夥伴們：趙志誠、謝雨霖、蔡銑泓、黃健銘、洪振家、呂建松，雖然你們早已畢業，但是曾經有過的情誼是無法輕易被抹滅的。而陪伴我四年的同學「徐行徽」，這些和你一起相處的日子，不論是在研究上或生活上，我從你身上學習到不少，而且我相信實驗室在你的帶領之下將來一定可以把 ADTL 的名號給發揚光大的。還有感謝我帶過的學弟們：王偉銘和洪文強，你們自主獨立的能力讓我在做研究時可以很專心並且你們認真的實驗態度與研究精神，身為帶你們的學長覺得很榮幸。再來我要感謝陳威臣學

弟，謝謝你每次都能不厭其煩的回答我英文方面的問題。還有我要謝謝蔡子儀、黃育峯、王子銘、黃建富、李克慧、Ally、大雄、小強、大偉、璋璋、林漢仲和球神等學弟妹們。由於你們的陪伴，讓我在研究所這段期間不感到寂寞並且充滿了歡樂，謝謝你們。接下來感謝我身旁的朋友們。謝謝美秀、妮瑩、鈺芳、宣如、佳鴻、光胤、竣祥、阿貴、阿志、洋A等。由於你們的鼓勵與打氣，讓我的碩士論文得以夠順利完成。

最後要感謝是我最重要的家人。感謝老爸、老母，謝謝你們提供我無虞的生活條件，讓我可以專注地安心學習，希望我的表現會讓你們感到驕傲；也感謝我兩個弟弟凱堯和耀仁，你們默默給予我的支持，還有不時的關心，也是讓我完成學業的最大功臣。而要感謝的人太多了，或許有沒提到的人，但你們在我心中依然佔了很重要的位置，在這裡獻上最誠摯的歉意與最大的感謝，謝謝你們，謝謝。

張凱翔

誌于風城交大 2008

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