Chapter 1
Introduction

1.1 An Overview of Low-Temperature Polycrystalline Silicon Thin-Film Transistors（LTPS-TFTs）

In the past decades, amorphous silicon thin-film transistors (a-Si TFTs) were mainly applied to active-matrix liquid-crystal displays (AMLCDs) where each pixel contains a TFT and a capacitor (the liquid crystal serving as the dielectric). The a-Si TFTs have many advantages, particularly its low-temperature fabrication process is compatible with the low-cost glass substrates and high off-state resistivity which results in low leakage current. However, the low electron field-effect mobility in a-Si TFTs has limited the device performance and thus the related circuit application is restricted. Recently, LTPS TFTs have been widely investigated for various applications such as the driver circuits of AMLCDs [1]-[4], memory devices [5]-[7], image sensors [8], and thermal printer heads [9]. Considering the much higher carrier mobility over that of a-Si TFTs and the low-temperature manufacturing with maximum process temperature lower than 600℃, LIPS TFTs have high potential of realizing system-on-panel (SOP), in which the peripheral circuitry can be integrated

on the glass substrates to minimize the panel size, improve the reliability and resolution of the displays, yield a light and thin display having a reduced number of connection pins, and reduce the fabrication cost. LTPS TFTs can be prepared by solid phase crystallization（SPC）[10], metal-induced lateral crystallization（MILC）[11] and excimer laser crystallization（ELA）[12] methods to transform the deposited a-Si into poly-Si. The improvement of mobility and reliability of poly-Si TFTs is the most important requirement in the realization of high performance display. Therefore, reliability testing is increasingly required.

In comparison with single-crystalline silicon, poly-Si is rich in structural defects distributed mainly in or near the grain boundaries. These defects act as charge-trapping centers and greatly affect the transport of carriers in the poly-Si TFTs. As a result, the device characteristics are much inferior to those of the single-crystalline counterparts. For example, poly-Si TFTs typically need a much larger gate voltage to effectively modulate the channel potential and turn on the channel conduction. Carrier mobility is also degraded due to the scattering with charge-trapping centers [13].

An anomalous leakage current has also been found in poly-Si TFTs, and the dominant leakage current mechanism is identified as the field emission via the traps caused by the high electric field near the drain junction [14]-[16]. In addition to

reducing the defect density, another approach to reduce the anomalous high leakage current is to adopt drain-field-relief structures, such as lightly doped drain (LDD) and offset-gate structure.

The floating-body architecture and charge trapping in defect states result in serious avalanche induced effects in poly-Si TFTs [17]. Due to the impact ionization occurring in the high electric field region at the drain end of the channel, holes are accumulated in the floating-body forcing further electron injection from the source, which are then collected by the drain. This extra drain current augments impact ionization which, in turn, forward-biases the floating body harder, thereby causing a regeneration action which leads to a premature breakdown. As a result, the output characteristics exhibit an anomalous current increase in the saturation region, and such phenomenon is often called “kink” effect [18].

Since defects greatly affect the electrical characteristics of poly-Si TFTs, the most effective approach to improve the performance of poly-Si TFTs is to reduce the defect density by promoting the crystallinity and quality of poly-Si thin films. The other important work is to reduce the undesirable effects, which result from the high drain electric field and floating body of poly-Si TFTs, by modifying the architecture of poly-Si TFTs.

1.2 Reliability Issues in LTPS TFTs

The stability of device characteristics under long-term operation is important for circuit application. So the reliability of LTPS TFTs must be carefully considered before they can be applied to advance circuitry such as data-driver in AMLCDs or driving elements in active matrix organic light emitting diodes (AMOLEDs). The special processes used in the fabrication of LTPS TFTs and the intrinsic properties associated with the granular structure of the channel layer make the reliability issues and focus in LTPS TFTs different from those in the conventional MOSFETs.

The gate oxide used in LTPS TFTs is generally deposited at low temperature by CVD methods. Consequently, it always exhibits poorer physical and electrical quality than the thermal oxide grown on Si wafers, such as more defects contained in the gate dielectric, higher gate leakage current, and lower breakdown field. Besides, the mobile ions, Si-H and/or Si-OH bonds as well as fixed charges existing in low-temperature deposited gate oxide are also potential causes for instability of LTPS TFTs [19]-[23].

In general, poly-Si is full of weak strained Si-Si bonds and dangling bonds. In order to improve the device performance of poly-Si TFTs, the hydrogenation process is usually applied after device fabrication. However, the hydrogenation process also creates a large amount of weak Si-H bonds in poly-Si. These weak bonds can easily

be broken during device operation, resulting in the drift in device characteristics [24]-[25].

As the glass substrate is a poor thermal-conducting material, heat generating during device operation is difficult to dissipate. Consequently, the device temperature may rise and enhance the breaking of weak bonds. Such phenomenon is called “self-heating”. The degradation rate caused by self-heating depends on the operation power and the capability of heat dissipation of the device. In general, wide-channel TFTs and/or small-size TFTs suffer from serious self-heating [26]-[28].

The surface roughness of poly-Si resulting form laser crystallization will enhance the local electric field at the interface between gate oxide and poly-Si channel, which will also degrade the reliability of TFTs under high gate bias operation [29].

The hot carrier effects which originate from high electric field near the drain junction were wildly investigated in MOSFETs. Meanwhile, hot carrier effect is another important reliability issue in LTPS TFTs. Conduction carriers can gain energy from high electric field and become “hot”. These high energy carriers can easily break weak bonds existing in poly-Si channel, creating many new defects in the channel and oxide charges. Serious degradation can be generated as a high drain bias is applied, and the degree of degradation depends on the strength of electric field which determines the energy of the hot carriers. Generally, introducing electric-field-relief

TFT structures, such as LDD, offset drain, and gate-overlapped LDD, can reduce hot carrier degradations.

1.3 Motivation

With their higher carrier mobility, poly-Si TFTs can be integrated with peripheral circuits in order to realize system-on-panel product. However, the reliability issues of poly-Si TFTs, like hot carrier effects, need to be addressed carefully before realization of SOC production manufacturing. Hence, reliability testing and understanding of reliability mechanisms become more and more important.

Hot carriers are generated during normal device operation by the high electrical field located near the drain. Charge trapped in the gate oxide and interface trap generation will lead to device degradation. In contrast to the MOSFETs, the situation becomes even more complex for poly-Si TFTs owing to the lack of substrate contact in typical device configuration, as well as the large mount of inter-/intra-grain defects contained in the channel. In the past few decades, there were many papers reporting the degradation mechanisms of poly-Si TFTs under static hot-carrier stress [30]-[32]. The results indicated that the damage regions could be situated in local regions of the channel which can be predicted using simulation and probed using measurement techniques, such as an emission microscope [33]-[35]. Nevertheless, all these

techniques proceed in an indirect manner and cannot directly resolve the location-dependent damage characteristics.

As thin film transistors in driver circuits are subject to high-frequency voltage pulses, the reliability of poly-Si TFTs under dynamic stress needs to be carefully examined, however. In recent years, there were also studies devoted to the investigation of the mechanisms of dynamic hot-carrier degradation [36]-[40]. The situation becomes more complicated than that during static operation. The dynamic operational conditions, like the voltages applied to the source/drain/gate, stressing time, frequency, falling/rising time, and duty cycle, all show dependence on the results of stressed device. Whether static stress or dynamic stress is employed, it is still not easy to clearly resolve and understand the detailed mechanisms responsible at different regions of the channel.

Recently, our group has proposed a novel test structure which is capable of spatially resolving the location-dependent damage of devices under static HC stress [41] [42]. The phenomena of hot-carrier degradation can thus be spatially resolved using such test structure. In this study, the novel test structure is further employed to investigate the HC degradation caused by both DC (static) and AC stress tests. The characteristics of such structure under various stress conditions, including the biases, stressing time, frequency, falling/rising time, and duty cycles, were explored and

identified to fully understand the degradation mechanisms.

1.4 Thesis Organization

The thesis is divided into four chapters. After the introduction of LTPS TFTs and talking about the motivation of this study given in this chapter, in Chapter 2, we describe the fabrication of a novel test structure. Furthermore, we examine the impacts of several static stress conditions on the test structure and discuss the associated degradation mechanisms based on the results we obtain.

In Chapter 3, we first give a brief description about the AC stress measurement setup and conditions. Then we show and analyze the electrical characteristics of the test structure under various AC stress conditions. Effects of stress configurations and the AC stress conditions, including frequency, duty cycle, and transient stages, are explored and addressed.

Finally, we summarize our conclusion and future work in Chapter 4.

Chapter 2
Device Fabrication and HC-TFTs under DC stress

2.1 Device Fabrication and Operating Principle of HCTFT

First, silicon wafers capped with 100nm wet oxide were used as the starting substrates, followed by the deposition of a low pressure chemical vapor deposition (LPCVD) amorphous silicon film with thickness of 100nm at 550℃ in a furnace tube. A solid phase crystallization (SPC) annealing step at 600℃ 24hr in N_2 ambient to transform the a-Si to poly-Si as the channel layer. The active region was then formed after lithography and etching. Next, the 30nm thick gate dielectric was deposited by LPCVD oxide. An in-situ n^+ doped poly-Si of 200nm thick was employed as the gate electrode. Source/drain doping was self-aligned by implanting phosphorous with a dosage of 5×10^{15} cm^{-2} for n-channel TFTs. An LPCVD oxide layer of 200nm was used as the passivation layer to isolate humidity and impurity, followed by contact-hole formation. After the metallization step, the test structure further received a plasma treatment in NH_3 ambient at 300℃ in order to improve devices performance.

Figure 2-1(a) is a top view of the test structure. The test structure is configured

with four pairs of n^+ electrodes at the edges of the channel. In Fig. 2-1(b), one pair of n^+ electrodes is placed along the x- (horizontal) direction to form the source and drain (S/D) of the normal (lateral) test transistor (TT) that will be undergone hot-carrier stressing, while the other three pairs are arranged along the y-(vertical) direction to form three separate monitor transistors (MTs) to observe spatial characterization of the hot-carrier degradations along the channel of test transistor after stressing, as shown in Fig. 2-1(c). The test transistor and three MTs share the common gate electrode lying over the entire channel. Since each pair of n^+ electrodes served as the S/D of the respective MT, the current-voltage (I-V) characteristics of the corresponding MT could be characterized. The pair of S/D placed along the x-direction, serving to the test transistor, is subjected to hot-carrier stressing by applying a high voltage to its drain for inducing the hot-carrier degradation in the test transistor. According to their respective location relative to the channel of the test transistor, the three MTs are denoted as S-MT (source-side MT), C-MT (central MT), and D-MT (drain-side MT), respectively. This unique configuration allows us to recognize the damage and identify the associated mechanisms at different locations along the channel of the test transistor after stressing.

2.2 Device Measurement and DC Stress Conditions

Figure 2-2 shows the cross-section of device. Applying different parts of voltage to gate/drain voltage and grounding the source, as DC stress condition. Then, we measure the characteristics of TT and other MTs before and after hot-carrier stressing at V_D=0.1V/3V.

The subthershold and output characteristics of the fabrication testers were measured by an Agilent^{TM} 4156A semiconductor parameter analyzer and Interactive Characterization Software (ICS) software.

From the measure I_D-V_G curve at V_D=0.1V, the parameters of HC-TFTs of on-current can be extracted according to its definition.

The on-current is defined as I_D current at V_G=10V and V_D=0.1V. The degradation (%) of the on-current is defined as $\Delta I_{on} / I_{on,0} \times 100\%$, where $\Delta I_{on} = I_{on,0} - I_{on}$, $I_{on,0}$ is the initial on-current and I_{on} is the on-current after being stressed.

In our research, degradation of on-current is an indicator for observing the characteristics of device under stress.

2.3 Degradation Mechanism in Poly-Si TFTs under Static Stress

Figure 2-3 illustrates the hot-carrier degradation scheme of poly-Si TFTs under DC stress condition of V_G=0.5V_D. Carriers can obtain energy from the high drain field

region and become “hot carriers”, which produce electron-hole pairs. The electrons generated by electron-hole pairs might be injected into gate oxide, which causes the characteristic of devices threshold voltage to shift. Moreover, these generated hot carriers may release their energy in the channel or near channel/oxide interface where defect traps are created. These generated defect traps will degrade the subthershold slope and mobility of devices leading to on-current degradation.

2.4 Results and Discussion

Subthershold characteristics of the lateral test, as shown in Fig. 2-1(b), were measured before and after DC stress, and the results are shown and compared in Fig. 2-4. In Fig. 2-4(a), the test transistor was stressed under high biases of V_G=10V and V_D=20V for 1000sec to induce hot-carrier degradations. The degradations in device characteristics in terms of increased subthershold swing and reduced on-current are indeed observed after DC stress, as can be seen in this figure. In both Figs. 2-4 (a) and (b), the post-stress ID-VG shift is more significant when the lateral test transistor was measured at low drain bias of V_D=0.1V after DC stress. These observations are consistent with the well-known belief that most of the damage events occur in the channel near the drain side of the test transistor. Hot-carrier stressing can generate additional interface states and/or grain-boundary defects, and form a defect-rich and

resistive region near the drain side. The hot-carrier induced traps can raise the grain boundaries barrier height near the drain side of the test transistor, which degrades on-current and subthershold swing. The potential barrier at the grain boundaries can be reduced by applying high bias of V_G or V_D. The test transistor was stressed under lower biases of V_G=7.5V and V_D=15V for 1000sec, as shown in Fig. 2-4(b). The post-stress I_D-V_G curve shows only a negligible shift relative to the fresh device under the milder stress condition.

The above-mentioned results of the conventional test transistor provide us the information about the major damage location in the stressed channel and the effect of stress voltages, as is well known in the literature. However, the detailed degradation mechanisms at different sections of the stressed could not be resolved by the conventional test structure. Moreover, the conventional test structure is also insensitive in detecting the induced damages while the applied stress voltages are low. To resolve these shortcomings, the subthershold characteristics of three separated monitor transistor (MTs) in the test structure were measured and the results are shown in Fig. 2-5. It is worth noting that the characteristics of the three MTs, as shown in Fig. 2-5, were measured using the same test structure with its test transistor DC-stressed and measured in Fig. 2-4 (b). It can be seen that among the three MTs, the D-MT shows the worst degradation and the other MTs (S-MT and C-MT) exhibit negligible

shift in I-V curves. The observed result in device under high biases stress (e.g., V_G=10V and V_D=20V) is also identical to that under low biases stress. Note that the post-stress I_D-V_G shift of the D-MT is very significant even when measured at a high V_D bias of 3V, indicating that hot-carrier induced traps are uniformly distributed along the entire channel of the D-MT. This observation simultaneously confirms the inference drawn above in analyzing the results of Fig. 2-4. Besides, the post-stress I_D-V_G shift of the D-MT is more obvious than that of TT under the milder stress. The phenomenon demonstrates the high sensitivity of the test structure in detecting the hot carrier effects.

Figure 2-6 shows the degradation of on-current of TT and MTs as a function of stress V_D with V_G=0.5V_D for 1000sec. The degradation of on-current of TT and D-MT become more severe when increasing the stress bias of V_D, since electrons gain more energy with increasing electric field at drain side. Figure 2-7 shows the degradation of on-current of TT and MTs after 1000-sec stress at V_D of 15V and various V_G. It can be seen that the trend of degraded on-current of TT and D-MT are similar, indicating that the damage region of test transistor under hot-carrier stress mainly locates near the drain side. Moreover, the drain-side damage is dominant in the low V_G regime, and peaks at around V_G=1/3V_D. That hot carriers can be generated is mainly determined by two factors. One is whether enough carries are induced; another is high electric

field requirement. When the gate voltage is lower than the threshold voltage, not enough electrons are induced. As the gate voltage gets larger, the horizontal electric field becomes lower with increasing gate voltage. It explains the result shown in Fig. 2-7.

Chapter 3
HC-TFTs under AC Stress

3.1 Experimental Setup and AC Stress Conditions

In this chapter, the hot-carrier degradation induced in TFTs under AC operations is investigated using the proposed HCTFT structure. The samples were prepared with the same method described in previous chapter and detailed process flow can be found in Sec. 2.1.1.

The measurements were performed on the setup consisting of an Agilent™ 8110A pulse generator, an Agilent™ 4156A semiconductor parameter analyzer, an Agilent™ E5250A switch, a probe station, and a personal computer (PC) installed with the HP VEE control program. The computer serves as the controller to coordinate the action of the connected equipment via GPIB bus. The schematics of the setup are illustrated in Fig. 3-1. The AC stress waveforms used in this work are illustrated in Fig. 3-2. During AC stress, a train of voltage pulses generated by the Agilent 8110A pulse generator is applied to either the gate or the drain. Rising time (t_r) is defined as the time that the voltage signal rises from 10% to 90% of the amplitude ($V_{P\_high} - V_{P\_low}$), and vice versa for falling time (t_f). Duty cycle is defined as the ratio of the time when

voltage pulse is V_{P_high} (t_{high} in Fig.3-2) to total time of one pulse cycle. It should be noted that the total stress time is defined as the summation of t_{high} during the stress period. Another thing that needs to be noticed is the symbol which represents the pulse voltage (V_{P_high}) in this work. When the pulse voltage is applied to the gate, the symbol that stands for V_P can be written as V_{G_high}. Similar to the situation as the pulse voltage is applied to the drain, the symbol of V_P can be written as $V_{D\_high.}$ Whether the pulse voltage is applied to gate or drain, V_{P_low} is set at 0V in this work.

3.2 Trap Density-of-state (DOS) Analysis

The performance of poly-Si TFTs is strongly affected by defects contained in the poly-Si channel. Characterization and analysis of density-of-states (DOS) in the gap of channel layer are thus essential for understanding the device characteristics and their dependence on the processing conditions. Moreover, accurate DOS extraction is required for the modeling of poly-Si TFTs. In line with this, it has been shown that field-effect conductance (FEC) method [43][44] can serve this purpose.

FEC method was originally proposed for characterizing the DOS in amorphous-Si TFTs. When applied to poly-Si TFTs, the presence of grain boundaries in the channel could be of great concern. Fortunately, it has been proven that, when the grain size is small enough, the poly-Si channel film can be modeled using the

"effective-medium" approach [43], in which the existence of grain-boundary defects and intragranular defects is assumed to be uniformly distributed throughout the material.

First, the temperature method [44] is used to determine the flat-band voltage (V_{FB}). In this approach the transfer characteristics were measured at various temperatures (shown in Fig. 3-3). Based on the measured data, plots of $T \cdot (d \log G / dV_G)$ at a specific gate voltage versus temperature (G is the field conductance) are plotted, as shown in Fig. 3-4, and V_{FB} is determined to be the gate voltage as $T \cdot (d \log G / dV_G)$ is independent of the temperature. In the present case shown in the figure, V_{FB} is corresponding to the gate voltage of -0.4 volt. Once V_{FB} is determined, the relationship between gate voltage and surface band-bending ($\psi(x = 0)$), where x is the vertical distance to the gate oxide/channel interface) can be constructed using the incremental method [43]. In this method, the electric field at the semiconductor surface is given, in the absence of surface states,

$$\left.\frac{d\psi}{dx}\right|_{x=0} = -\frac{\varepsilon_{OX}}{\varepsilon_{Si}} \cdot \frac{V_{OX}}{t_{OX}} = -\frac{\varepsilon_{OX}}{\varepsilon_{Si}} \cdot \frac{V_G - V_{FB} - \psi_S}{t_{OX}} \qquad (3\text{-}1)$$

From the FEC method, the DOS is given by

$$DOS(E_F+\psi_S)=\frac{\varepsilon_{Si}}{2q}\frac{\partial^2}{\partial\psi_S{}^2}\left(\left.\frac{d\psi}{dx}\right|_{x=0}\right)^2 \quad (3\text{-}2)$$

Afterwards, the resultant DOS was calculated and plotted in Fig. 3-5. In this chapter, the extraction of DOS was employed to analyze the devices before and after the AC stress and help understand the characteristics of degradation.

3.3 Degradation Induced by AC Stress with Pulsed Gate-Voltage

- 3.3.1 Effects of frequency and duty cycle

Characteristics of the transistors in a test sample stressed under the AC stress condition of V_{G_high}=7.5V with duty cycle of 50%, V_D=15V, frequency=500kHz, t_r = t_f = 100ns and total stress time=1000sec, are shown in Fig. 3-6. Figure 3-6 (a) shows the degradation characteristics of TTs in terms of increased subthreshold swing and reduced on-current observed after the AC stress. The deviation from the fresh device characteristics is more obvious as measured at V_D of 0.1V than at 3V. This is an indication that defect traps, like interface states and grain-boundary defects, are generated and formed a defect-rich and resistive region near the drain side after the AC stress. As the drain voltage is increased in the transfer characteristics measurements, the damage region is screened out by the depletion region of drain junction, so is the transfer characteristics. These observations are consistent with the well-known belief that most of the damage events occur in the channel near the drain side of the test transistor [36] [45]. With the unique design of the test structure, direct evidence is obtained. Comparing the characteristics of MTs before and after AC stress,

only the D-MT exhibits obvious changes while S-MT and C-MT show only negligible difference, as shown in Figs. 3-6 (b)-(d). Further, note that the subthreshold characteristics of D-MTs show more visible degradation as compared with the TT under the milder AC stress. This points out that, with the equipment of monitor transistors, the test structure also possesses greater sensitivity than conventional test structure in detecting the localized damaged region under the AC stress.

This data presented above indicate that the damage regions mainly are located near the drain side under AC stress, similar to the situation of devices under static stress presented in last chapter. This could be further confirmed by simply reversing the source and drain terminals in the device measurements. Comparisons of the transfer characteristics of the TT device under normal mode and "reversed S/D" mode are depicted in Fig. 3.7. As shown in Fig. 3.7(a), the subthreshold characteristics of TT measured under normal and the reversed S/D modes before the AC stress are almost identical. This is reasonable considering the symmetrical S/D formation process. The outcome becomes different as the AC stress is implemented, as shown in Fig. 3.7(b). In this case, when the device is measured under reversed S/D mode, the defects near the drain side under normal mode are now located near the source side. As a result the defect-rich region contributes a high resistance that cannot be screened out by the high drain bias, so the device exhibits obvious degradation in subthreshold I-V characteristics as measured at V_D = 3V.

Figures 3-8 (a) and (b) show subthreshold curves of TTs before and after 1000-sec AC stress with frequency of 100kHz and 1MHz, respectively. In the figure it can be seen that the degradation of device under high-frequency AC stress is much severe than that under low-frequency AC, especially as the drain voltage is low. This phenomenon is important since practical circuits needs to operate at a high frequency.

In the second half of this chapter more efforts are dedicated to comprehending this tendency. The DOS distribution extracted from the subthreshold characteristics of TTs shown in Figs. 3-8 (a) and (b) before and after the AC stressing under100kHz and 1MHz are shown in Figs. 3-9 (a) and (b), respectively. It can be seen that the generated defects are mainly in the band tail regime after the stress in the two cases. The tail states are presumably present in the form of strained bonds in the channel film, which are mainly located near the grain boundaries and affect mainly the device's mobility [46].

Figure 3-10 shows the degradation in on-current of TT and MTs after 1000-sec AC stress as function of duty cycle. The results indicate that the on-current of both TT and D-MT shows much more significant degradation than the case of static stress (duty cycle = 100%). The situation becomes even worse with decreasing duty cycle. Moreover, the D-MT always shows higher degree of degradation as compared with the TT. In contrast, the S-MT and C-MT exhibit negligible degradation and very weak dependence on the duty cycle. In the measurements the AC stress time is fixed at 1000sec which is the summation of t_{high} according to the definition mentioned above. If the devices degrade only during the periods when pulse voltage bias is at V_{G_high}, the degradation of on-current should yield similar result independent of frequency or duty cycle. The trend shown in the figure is clearly contradictory to such postulation and indicates that degradation induced in periods other than V_{G_high} also contributes to the degradation.

The periods when V_{G_low} (=0) are not likely to induce damage in the device due to the lacking of carriers inside the channel. It is thus postulated that the extra damage is caused during the voltage switching periods (related to t_r and t_f). To confirm this perspective, we check the dependence of on-current degradation of TT and D-MT on the number of the AC stress cycles. The results are shown in Figures 3-11 (a) and (b) for TT and DT, respectively. The stress was performed with V_{G_high} and V_D of 7.5 V and 15 V, respectively, and both t_r and t_f of 100 ns. The measurements are either with fixed frequency (500kHz) or fixed duty cycle (50%). The results presented in the figures clearly illustrate that the degradation induced in the devices is linearly proportional to the number of cycles. Furthermore, the data are almost distributed in a universal line regardless of whether they were measured under fixed frequency or fixed cycle. The results prove our inference that the damage would be induced in the switching periods and the resultant impact is even more significant than that caused as V_{G_high} is applied. However, the switching period consists of rising and falling stages. So the next task is to identify the effects of the two stages.

- ### 3.3.2 Effects of rising and falling times

The results of on-current degradation under AC stress with various rising time and falling time are shown in Figs. 3-12 and 3-13, respectively. In the measurement

the stress is with V_{G_high} of 7.5 V, V_D of 5 V, frequency of 500kHz, and duty cycle of 50 %.The total stress time is 1000 sec. In the two figures, it can be clearly seen that the major damage region is located near drain, which is represented by the data from D-MTs, and also reflects on the results of TT. In Fig.3-12 we can see that the dependence of rising time is not significant. However, the on-current degradation of TT and D-MTs under AC stress decreases dramatically with increasing falling time, as shown in Fig. 3-13.

To make it more clear, on-current degradation of D-MTs under AC stress with various rising and falling time as functions of AC stress cycles are shown in Figs. 3-14 (a) and (b), respectively. In Fig.3-14(a), the degradation increases with increasing cycle number but exhibits negligible dependence on the rising time. In Fig.3-14(b) the short falling time causes more significant degradation than the long one. These results unambiguously point out that the falling time dominates the degree of degradation.

- 3.3.3 **Degradation mechanism in Poly-Si TFTs under AC stress**

Considering the major findings presented above, Fig. 3-15 is proposed to illustrate a possible scenario for the damage process under AC stress. As shown in the

illustration, as a high pulse voltage is applied to the gate electrode while source is grounded and a high bias is applied to the drain. For gate pulse at V_{G_high} stage, the damage induced by on-state hot-carriers causes defect generation near the drain, as shown in Fig. 3-15(a), and results in on-current reduction. During the turning-off transient period, the inversion electrons remaining in the channel are attracted by the positive drain voltage and tend to be accelerated toward the drain, resulting in additional damages (Fig. 3-15(b)). This explains why the on-current degradation of TT and D-MTs is associated with falling time not rising time at transient regime during AC stress, and the tester receives more transient hot-carrier damage as the falling time is shortened, as shown in Fig. 3-13 and Fig. 3-14 (b). This is postulated to be due to the short falling time that is not sufficient for the electrons to relax, so excessive hot carriers would impact the region in the channel near the drain and lead to a higher level of damage. Moreover, the short falling time results in quicker change of the gate and drain difference voltage. That is, the carries gain larger energy during the short falling time, causing serious degradation, due to the higher lateral electric field as the falling time is shortened.

3.4 Degradation Induced by AC Stress with Pulsed Drain-Voltage

The subthreshold characteristics of a tester, which was stressed under AC stress bias conditions of V_G=7.5V, V_S=0V, pulsed voltage of V_D (V_{D_high}=15V), frequency= 500kHz, $t_r = t_f$ = 100ns, and total stress time=1000sec, are shown in Fig. 3-16. The degradation characteristics of the TTs and MTs are similar to those of TTs and MTs under the AC stress with pulsed gate-voltage (shown in Fig. 3-8). From the characteristics of the MTs shown in Figs.3-16 (b)-(d), it can be seen that the dominant damage region is located near the drain-side of the channel while the S-MT and C-MT have negligible difference. However, comparing the results with those under AC stress with pulsed gate-voltage, the degradations of device in the present case are significantly reduced. In other words, the configuration of AC bias conditions would draw an impact on the outcome. To understand the effect of transient stages in the AC pulse train, on-current degradation under AC stress with various rising time and falling time are shown in Figs. 3-17 and 3-18, respectively. By comparing the results with the former stress condition shown in Figs.3-12 and 3-13, we found interestingly opposite trend that the degradation in the present case is greatly affected by the rising time rather than the falling time. This can be explained with the following argument: Throughout this type of AC stress the gate voltage is fixed at 7.5V, and thus an inversion layer is always present in the channel. As the drain voltage is high, the carriers in the channel would be accelerated by lateral electric field near the drain side

and become hot to induce the damage. Such condition would change as the drain voltage is switched to a low value since the strength of lateral electric filed is dramatically lowered. This means that the population of hot carriers diminishes in the falling stage and no extra damage is expected to induce. As a result the damage shows negligible dependence on the falling time. On the other hand, as the drain voltage is raised from zero, the acceleration of carriers in the channel to the drain leads to the generation of hot carriers. When the drain voltage reaches the peak value, a high potential drop appears in the channel near the drain side. As the rising time is shorter the carriers present in this region are less likely to relax and may become “very hot” and induce severe damage. As a result the degradation dramatically increases with decreasing rising time.

Chapter 4
Conclusions and Future Work

4.1 Conclusions

In this work, we have employed a novel test structure proposed and developed by our group to investigate the reliability issues of poly-Si TFTs. Owing to the unique monitor transistors design, such a novel test structure is especially suitable for monitoring the spatial hot-carrier degradation in poly-Si TFTs. It also shows a high sensitivity in detecting the degradation even under mild DC/AC stress condition. Besides, the fabrication of the novel test structure is simple and compatible with standard TFT manufacturing without extra masking.

The test device after the static stress exhibits clear damage which is identified to be induced near the drain-side with the novel test structure. The extent to which test device degrades under static stress is associated with the ratio of the applied gate-voltage to the drain-voltage. In our experiments, most serious degradation of the test device occurs under static stress condition when V_G/V_D ratio is around 1/3.

The HCTFT was also employed for the analysis of the hot-carrier degradation under AC stress. The effect of several factors including frequency, rising time, falling

time and duty cycle, were investigated and discussed. The AC hot-carrier stress was applied with a train of voltage pulses applied to either the gate or the drain. The data indicate that the former case would result in much worse degradation than the latter one. By using such a tester for characterization of AC hot-carrier stress, the weighting of each stage in a cycle of the AC voltage pulse in inducing the damage can be understood. The experimental results provide unambiguous evidence that the major damage occurs during the voltage falling stage. A model is proposed to explain such tendency.

4.2 Future Work

In this study, only hot-carrier degradations in n-channel TFTs were investigated. It is also interesting to fabricate and study the effect in p-channel TFTs. The degradation may show a very different picture. Besides, our devices can be used to investigate the reliability issues associated with various re-crystallization methods, such as MILC and ELA, etc. Effects of post treatments after device completion, such as NH_3, O_2 , N_2, and F_2 plasma treatments, are also worth studying.

REFERENCES

[1] G. Lewis, I. -W. Wu, T. Y. Huang, A. Chiang, and R. H. Bruce, "Active matrix liquid crystal display design using low and high temperature processed polysilicon TFTs," in *IEDM Tech. Dig.*, 1990, pp. 843-846.

[2] M. G. Clark, "Current status and future prospects of poly-Si devices," *IEE Proceedings - Circuits, Devices and Systems*, vol. 141, pp. 3-8, Feb. 1994.

[3] G. Fortunato, "Polycrystalline silicon thin-film transistors: A continuous evolving technology," *Thin Solid Films*, vol. 296, pp. 82-90, 1997.

[4] S. H. Jung, W. J. Nam, J. H. Lee, J. H. Jeon, and M. K. Han, "A new low-power pMOS poly-Si inverter for AMDs," *IEEE Electron Device Lett.*, vol. 26, pp. 23-25, 2005.

[5] S. D. S. Malhi, H. Shichijo, S. K. Banerjee, R. Sundaresan, M. Elahy, G. P. Polack, W. F. Richardson, A. H. Shah, L. R. Hite, R. H. Womack, P. K. Chatterjee, and H. W. Lam, "Characteristics and three-dimensional integration of MOSFET's in small-grain LPCVD polycrystalline silicon," *IEEE Trans. Electron Devices*, vol. 32, pp. 258-281, 1985.

[6] T. Yamanaka, T. Hashimoto, N. Hasegawa, T. Tanaka, N. Hashimoto, A. Shimizu, N. Ohki, K. Ishibashi, K. Sasaki, T. Nishida, T. Mine, E. Takeda, and T. Nagano, "Advanced TFT SRAM cell technology using a phase-shift lithography," *IEEE Trans. Electron Devices*, vol. 42, pp. 1305-1313, 1995.

[7] M. Aoki, T. Hashimoto, T. Yamanaka, and T. Nagano, “Large 1/f noise in polysilicon TFT loads and its effects on the stability of SRAM cells,” *Jpn. J. Appl. Phys.*, vol. 35, pp. 838-841, 1996.

[8] T. Kaneko, Y. Hosokawa, M. Tadauchi, Y. Kita, and H. Andoh, “400 dpi integrated contact type linear image sensors with poly-Si TFTs analog readout circuits and dynamic shift registers,” *IEEE Trans. Electron Devices*, vol. 38, pp. 1086-1093, 1991.

[9] Y. Hayashi, H. Hayashi,M. Negishi, and T. Matsushita, “A thermal printer head with CMOS thin-film transistors and heating elements integrated on a chip,” in *Proc. Int. Solid-State Circuit Conf.*, 1988, pp. 266-267.

[10] A. Mimura, N. Konishi, K. Ono, J.I. Ohwada, Y. Hosokawa, Y. A. Ono, T. Suzuki, K. Miyata and H. Kawakami, “High performance low-temperature poly-Si n-channel TFT’s for LCD,” *IEEE Trans. Electron Devices*, vol. 36, pp. 351-359, 1989.

[11] S. W. Lee and S. K. Joo, ”Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization,” *IEEE Electron Device Lett.*, vol. 17 pp. 160-162, 1996.

[12] T. Sameshima, M. Hara and S. Usui, “XeCl excimer laser annealing used to fabricate poly-Si TFT’s,” *Jpn. J. Appl. Phys.*, vol. 28, pp. 1789-1793, 1989.

[13] Gi-Young Yang, Sung-Hoi Hur, and Chul-Hi Han,” A physical-based analytical turn-on model of polysilicon thin-film transistors for circuit simulation” *IEEE Trans. Electron Devices*, vol. 46, pp. 165-172, 1999.

[14] I. W. Wu, W. B. Jackson, T. Y. Huang, A. G. Lewis, and A. Chiang,” Mechanism

of device degradation in n- and p-channel polysilicon TFTs by electrical stressing," *IEEE Electron Device Lett.*, vol. 11, pp. 167-169, 1990.

[15] K.R. Olasupo, and M.K. Hatalis," Leakage current mechanism in sub-micron polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 43, pp. 1218-1223, 1996.

[16] M. Lack, I-W. Wu, T. J. King, and A. G. Lewis," Analysis of leakage currents in poly-silicon thin film transistors," in *IEDM Tech. Dig.*, pp. 385-388, 1993.

[17] M. Hack, and A.G. Lewis," Avalanche-induced effects in polysilicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 12, pp. 203-205, 1991.

[18] M. Valdinoci, L. Colalongo, G. Baccarani, G. Fortunato, A. Pecora, and I. Policicchio," Floating body effects in polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 44, pp. 2234-2241, 1997.

[19] N. Bhat, M. Cao, and K.C. Saraswat," Bias temperature instability in hydrogenated thin-film transistors," *IEEE Trans. Electron Devices*, vol. 44, pp. 1102-1108, 1997.

[20] C.A. Dimitriadis, P.A. Coxon, A.J. Lowe, J. Stoemenos, and N.A. Economou, "Control of the performance of polysilicon thin-film transistor by high-gate-voltage stress," *IEEE Electron Device Lett.*, vol. 12, pp. 676-678, 1991.

[21] N. D. Young, and A. Gill, "Water-related instability in TFTs formed using deposited gate oxides," *Semicond. Sci. Technol.*, Vol. 7, pp. 1103-1108, 1992.

[22] Kousuke Okuyama, Katsuhiko Kubota, Takashi Hashimoto, Shuji Ikeda, and Atsuyosi Koike, "Water-related threshold voltage instability of polysilicon

TFTs,” in *IEDM Tech. Dig.*, pp. 527-530, 1993.

[23] N. D. Young, A. Gill, and I. R. Clarence,” Mobile ion effects in low-temperature silicon oxides,” *J. Appl. Phys.*, vol. 66, pp. 187-190, 1989.

[24] I.-W. Wu, W.B. Jackson, T.-Y. Huang, A.G. Lewis, and A. Chiang,” Mechanism of device degradation in n- and p-channel polysilicon TFTs by electrical stressing,” *IEEE Electron Device Lett.*, vol. 11, pp. 167-170, 1990.

[25] M. Hack, A.G. Lewis, and I.-W. Wu,” Physical models for degradation effects in polysilicon thin-film transistors,” *IEEE Trans. Electron Devices*, vol. 40, pp. 890-897, 1993.

[26] Noriji Kato, Takayuki Yamada, So Yamadam, Takeshi Nakamura, and Toshihisa Hamano,” Degradation mechanism of polysilicon TFT’s under DC stress,” in *IEDM Tech. Dig.*, pp. 677-680, 1992.

[27] Satoshi Inoue, and Hiroyuki Ohshima,” New degradation phenomenon in wide channel poly-Si TFTs fabricated by low temperature process,” in *IEDM Tech. Dig.*, pp. 781-784, 1996.

[28] Y. Mishima, K. Yoshino, M. Takei, and N. Sasaki,” Characteristics of low-temperature poly-Si TFTs on Al/glass substrates,” *IEEE Trans. Electron Devices*, vol. 48, pp. 1087-1091, 2001.

[29] P.-T. Liu, H.-Y. Lu, Y.-C. Chen, and S. Chi,” Degradation of Laser-Crystallized Laterally Grown Poly-Si TFT under Dynamic Stress,” *IEEE Electron Device Lett.*, vol. 28, pp. 401-403, 2007.

[30] Y. Uraoka, K. Kitajima, H. Kirimura, H. Yano, T. Hatayana, and T. Fuyuki, ”Degradation in low-temperature poly-Si thin film transistors depending

on grain boundaries," *Jpn. J. Appl. Phys.*, vol. 44, pp. 2895-2901, 2005.

[31] G. Fortunato, A. Pecora, G. Tallarida, L. Mariucci, C. Reita, and P. Migliorato, "Hot carrier effect in n-channel polycrystalline silicon thin-film transistors: A correlation between off-current and tansconductance variations," *IEEE Trans. Electron Devices*, vol. 41, pp. 340-346, 1994.

[32] C. A. Kimitriadis, M. Kimura, M. Miyasaka, S. Inoue, F. V. Farmakis, J. Brini, and G. Kamarinos, "Effect of grain boundaries on hot-carrier induced degradation in large grain polysilicon thin-film transistors," *Solid-State Electron.*, vol.44, pp.2045-2051, 2000.

[33] Y. Uraoka, T. Hatayama, T. Fuyuki, T. Kawamura, and Y. Tsuchihashi, "Hot Carrier Effects in Low-Temperature Polysilicon Thin-Film Transistors," *Jpn. J. Appl. Phys.*, vol. 40, pp.2833-2836, 2001.

[34] A. T. Hatzopoulos, D. H. Tassis, N. A. Hastas, C.A. Dimitriadis, and G. Kamarinos, "An Analytical Hot-Carrier Induced Degradation Model in Polysilicon TFTs," *IEEE Trans. Electron Devices*, vol.52, pp. 2182-2187, 2005.

[35] Y. Uraoka, N. Hirai, H. Yano, T. Hatayama, and T. Fuyuki, "Hot Carrier Analysis in Low-Temperature Poly-Si TFTs Using Picosecond Emission Microscope," *IEEE Trans. Electron Devices*, vol.51 pp. 28-35, 2004.

[36] K. M. Chang, Y. H. Chung, and G. M. Lin, "Hot Carrier Induced Degradation in the Low Temperature Processed Polycrystalline Silicon Thin Film Transistors Using the Dynamic Stress," *Jpn. J. Appl. Phys.*, vol. 41, pp. 1941-1946, 2002.

[37] Y. Uraoka, H. Yano, T. Hatayama, and T. Fuyuki," Comprehensive Study on Reliability of Low-Temperature Poly-Si Thin-Film Transistors under Dynamic

Complimentary Metal-Oxide Semiconductor Operations," *Jpn. J. Appl. Phys.*, vol. 41, pp. 2414-2418, 2002.

[38] Y. Toyota, T. Shiba, and M. Ohkura, "Effects of the Timing of AC Stress on Device Degradation Produced by Trap States in Low-Temperature Polycrystalline-Silicon TFTs," *IEEE Trans. Electron Devices*, vol.52, pp. 1766-1771, 2005.

[39] D.H. Tassis, A.T. Hatzopoulos, N. Arpatzanis, C.A. Dimitriadis, and G. Kamarinos, "Dynamic hot-carrier induced degradation in n-channel polysilicon thin-film transistors," *Microelectronics Reliability*, vol.46, pp. 2032-2037, 2006.

[40] Y. Toyota, T. Shiba, and M. Ohkura, "A new model for device degradation in low-temperature N-channel polycrystalline silicon TFTs under AC stress," *IEEE Trans. Electron Devices*, vol.51, pp. 927-933, 2004.

[41] H. -C. Lin, M. -H. Lee and, K. –H. Chang, "Spatially Resolving the Hot Carrier Degradations of Poly-Si Thin-Film Transistors Using a Novel Test Structure", *IEEE Electron Device Lett.*, vol. 27, pp. 561-563, 2006.

[42] M. H. Lee, K. H. Chang, and H. C. Lin, "Spatially and temporally resolving the degradation of n-channel poly-Si thin-film transistors under hot-carrier stressing," in *J. Appl. Physics*, vol.101, 054518, 2007

[43] G. Fortunato, and P. Migliorato, "Field-effect analysis for the determination of gap-state density and Fermi-level temperature dependence in polycrystalline silicon," *Phil. Mag. B.*, vol.57, pp. 573-586, 1988.

[44] R. L. Weisfield, and D. A. Anderson, "Analysis of field-effect conductance measurements on amorphous semiconductors," *Phil. Mag. B.*, vol.43, pp. 93-103,

1981.

[45] K. Y. T. Yoshida, M. Takei, A. Hara, N. Sasaki, and T. Tsuchiya, “Experimental Evidence of Grain-boundary Related Hot-carrier Degradation Mechanism in Low-temperature Poly-Si Thin-film-transistors,” *IEDM Tech. Dig*, pp. 219-222, 2003.

[46] I-Wei Wu, Tiao-Yuan Huang, Warren B. Jackson, Alan G. Lewis, and Anne Chiang, “Passivation Kinetics of Two Types of Defects in Polysilicon TFT by Plasma Hydrogenation,” *IEEE Electron Device Lett.*, vol. 12, pp. 181-183, 1991.

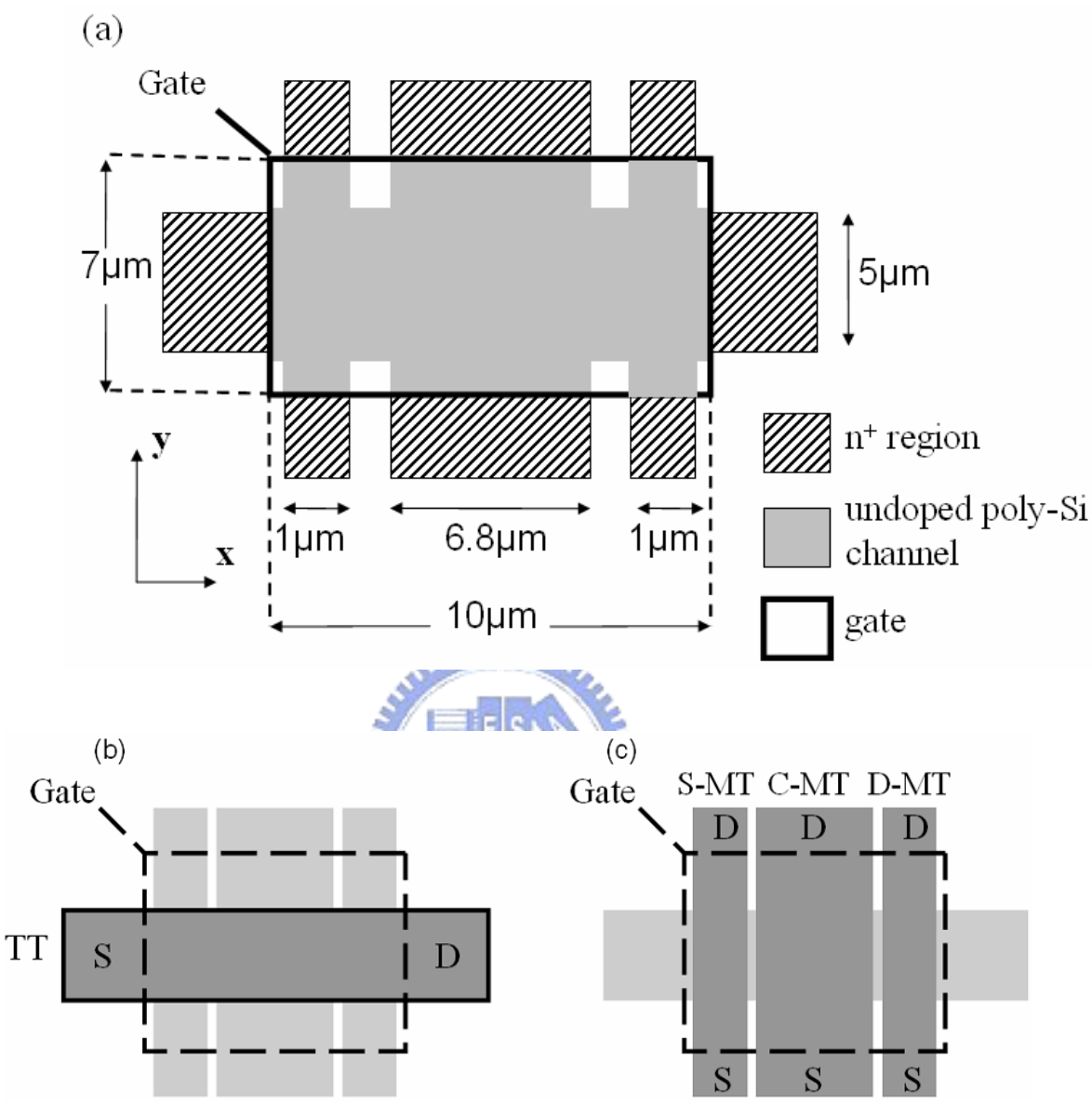

Fig. 2-1 (a) Top view and (b) (c) operational configurations of the test structure.

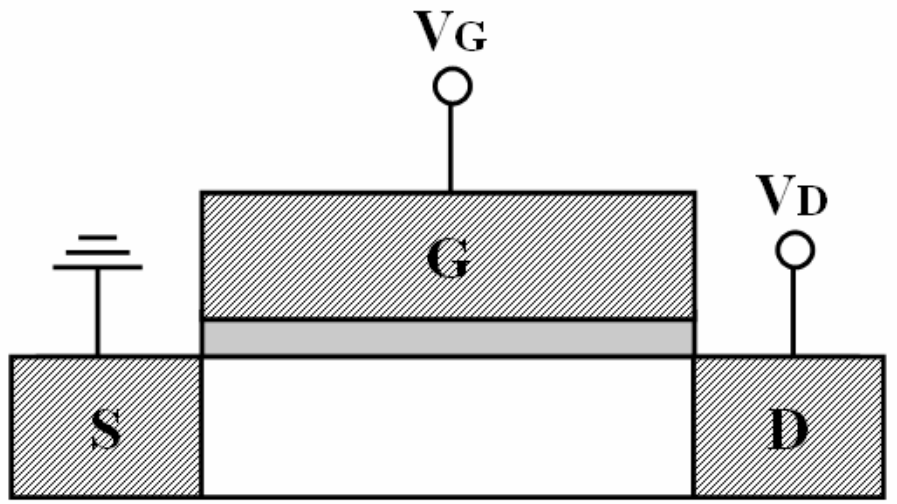

Fig. 2-2 Cross-sectional view of the test device.

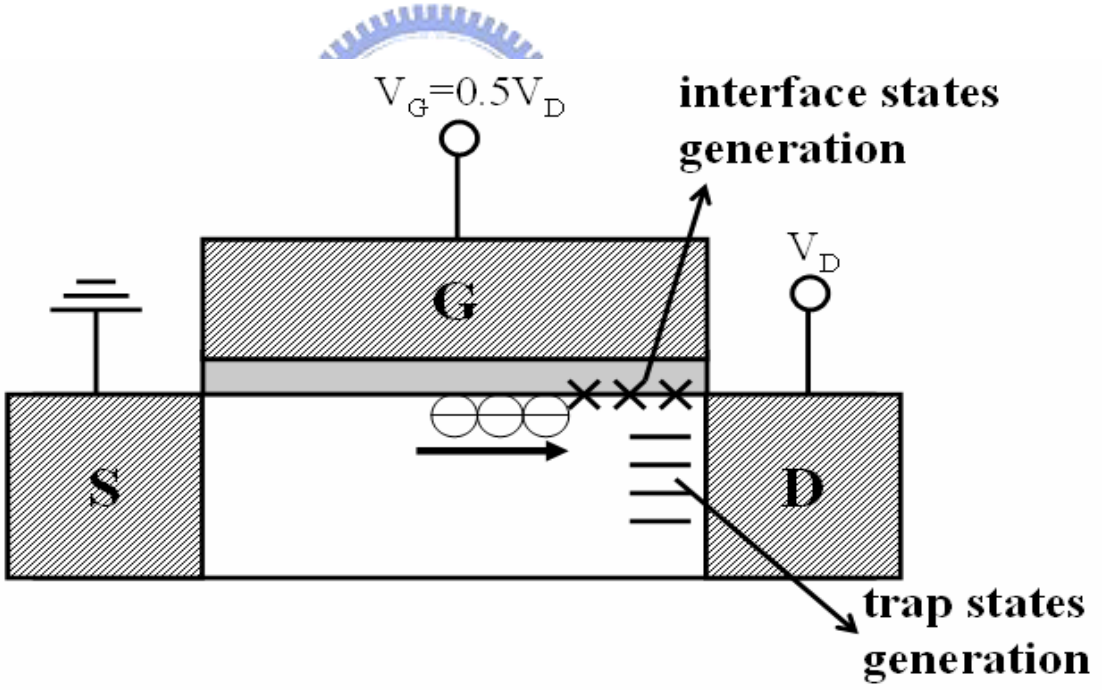

Fig. 2-3 Schematic illustration of defect creation in the device caused by hot carriers.

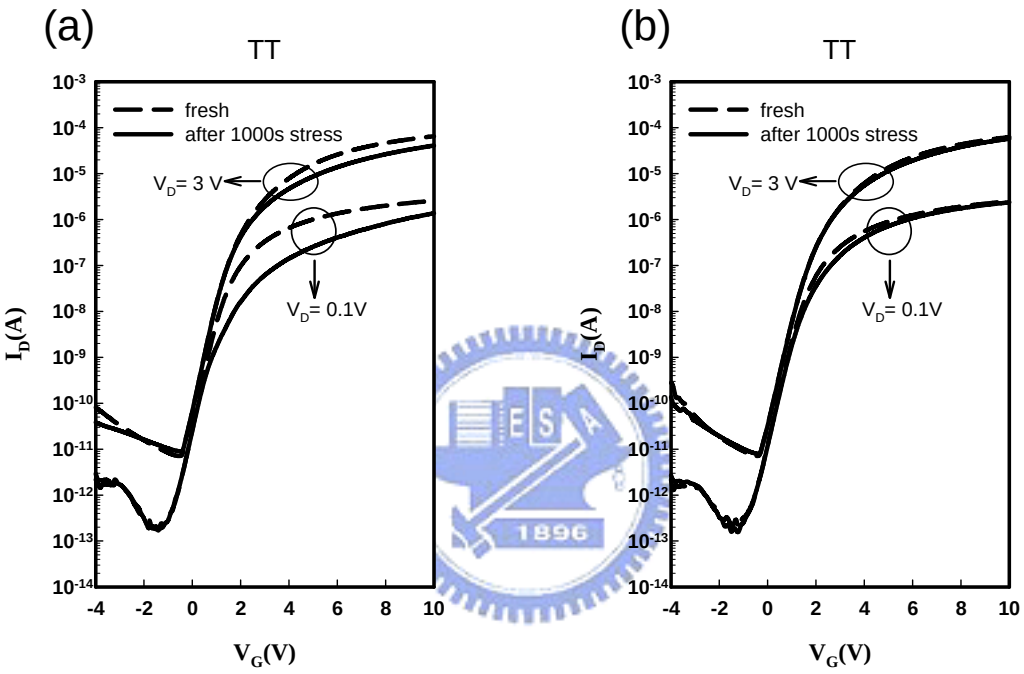

Fig. 2-4 Subthreshold characteristics of the test transistor before and after DC stressing at V_G/V_D of (a)10V/20V and (b)7.5V/15V for 1000sec.

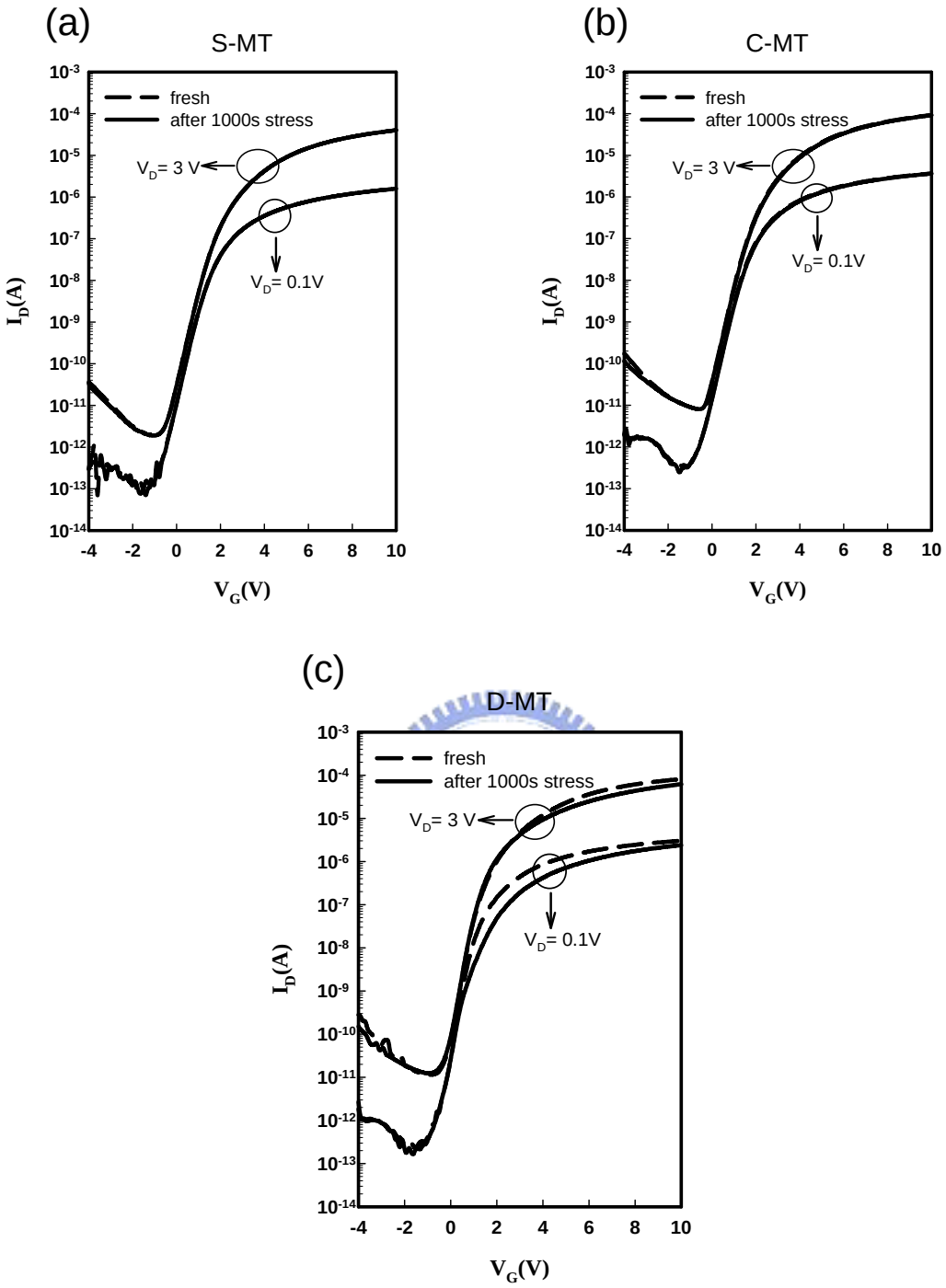

Fig. 2-5 Subthreshold characteristics of (a)S-MT, (b)C-MT, and (c)D-MT transistors contained in the same test structure characterized in Fig. 2-4(b) before and after DC stressing at V_G/V_D of 7.5V/15V for 1000sec.

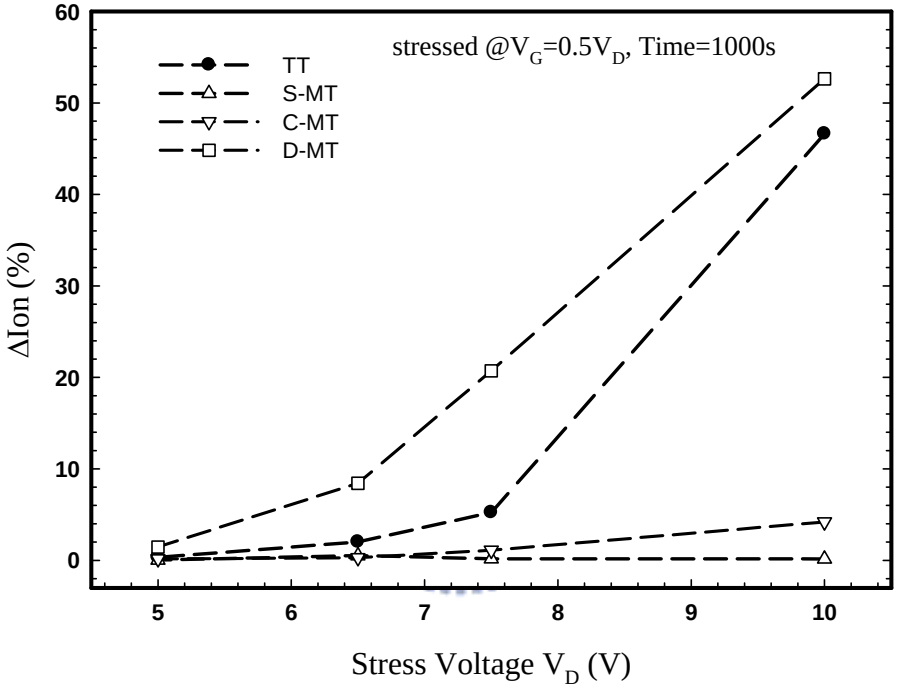

Fig. 2-6 On-current degradation of test structures under various hot-carrier stress conditions with constant V_G/V_D ratio of 0.5.

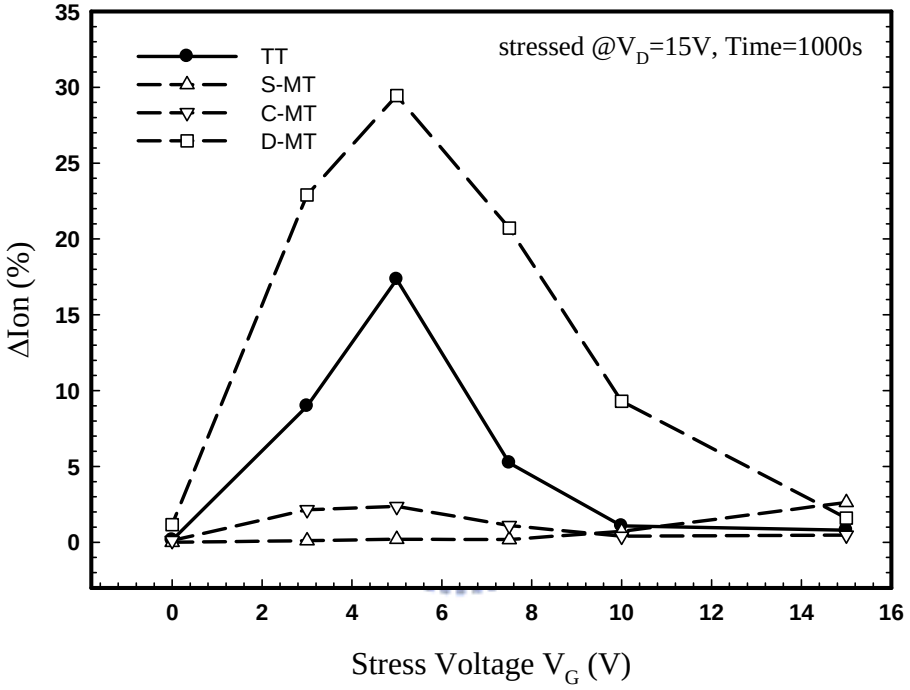

Fig. 2-7 On-current degradation of test structures as a function of V_G, V_D=15V during stress.

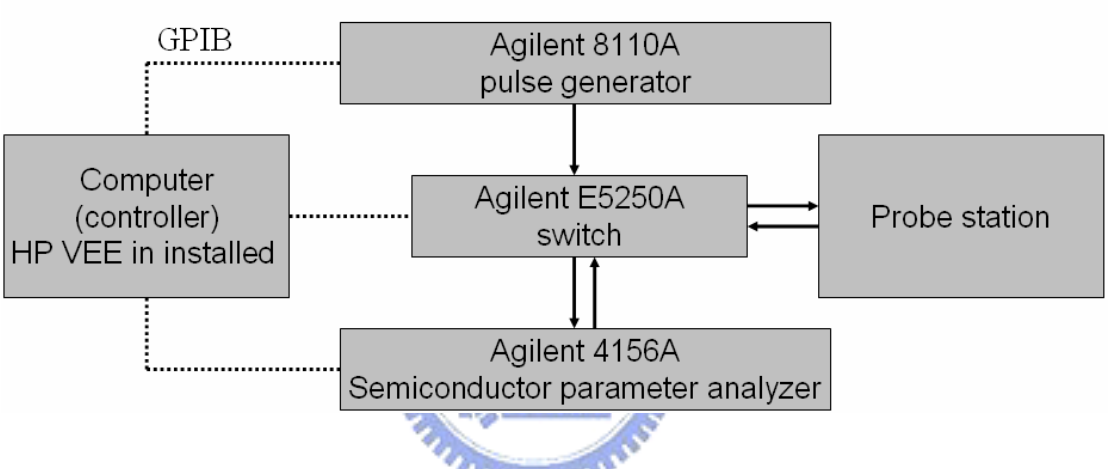

Fig. 3-1 Schematic illustrations of the measurement setup.

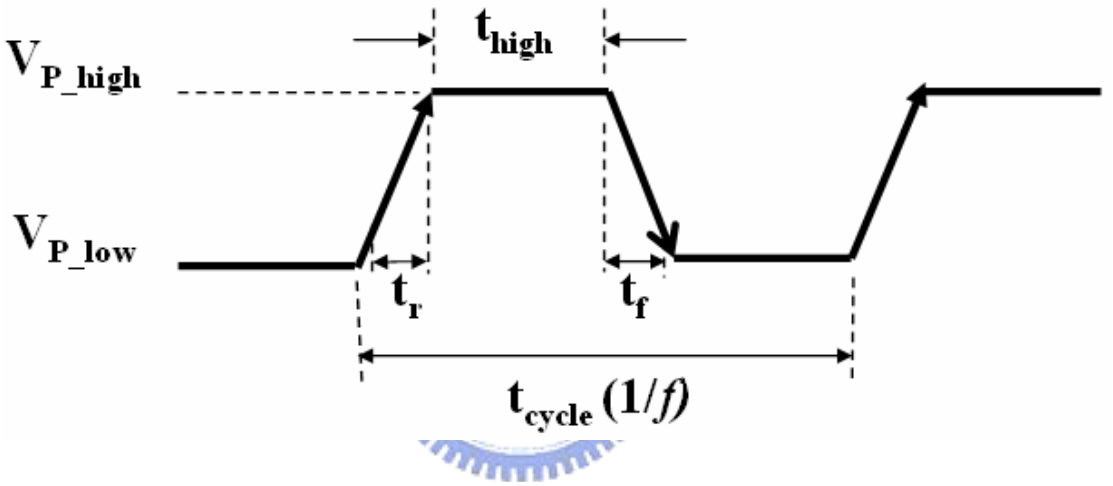

Fig. 3-2 Waveforms of the stress pulse generated by pulse generator.

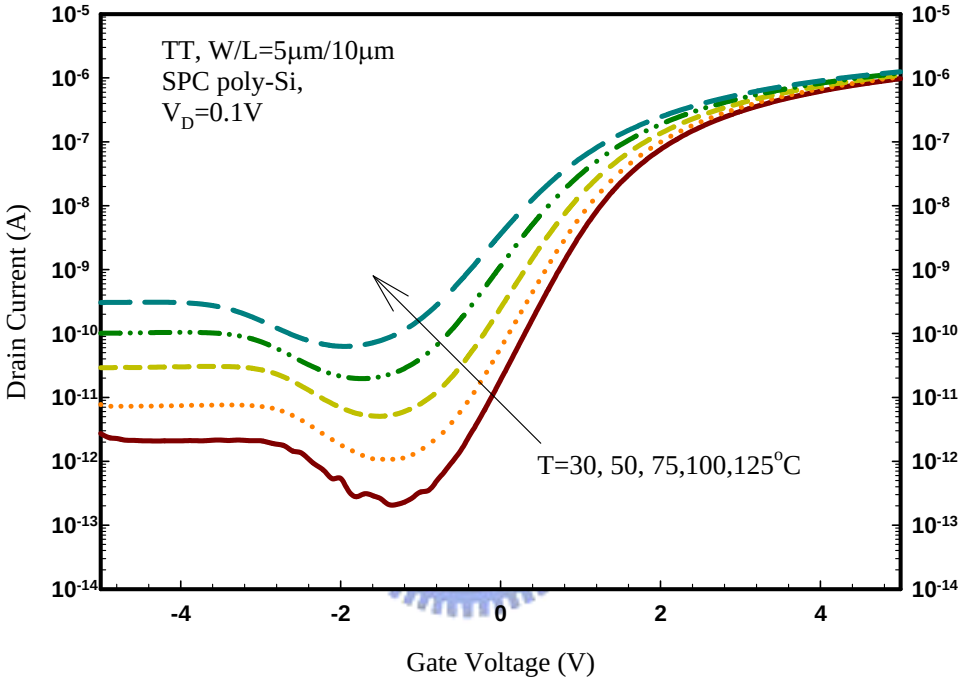

Fig. 3-3 Subthreshold characteristics of TT measured at different temperatures.

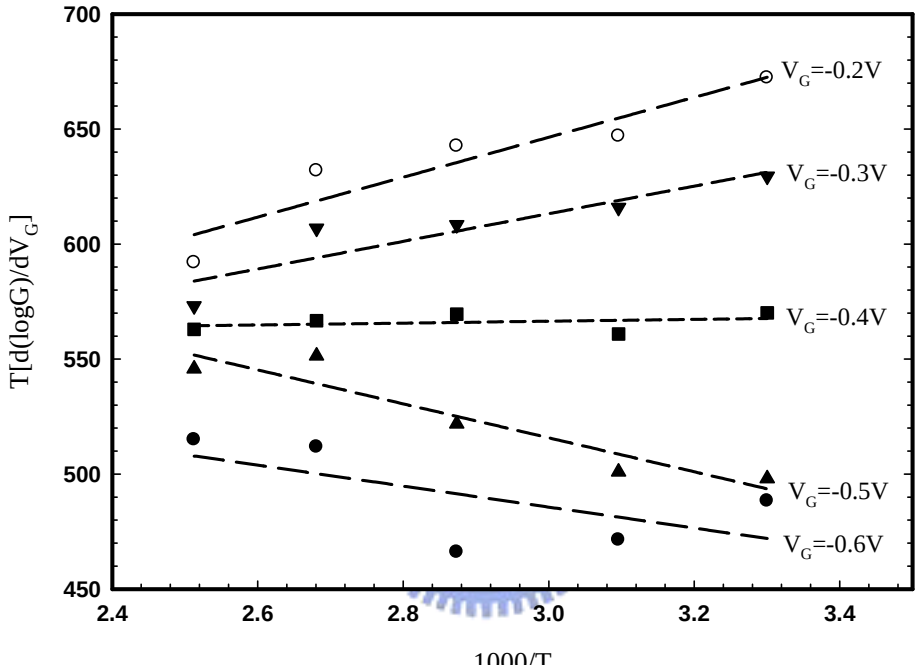

Fig. 3-4 Plots of $T \cdot (d \log G / dV_G)$ as a function of 1000/T.

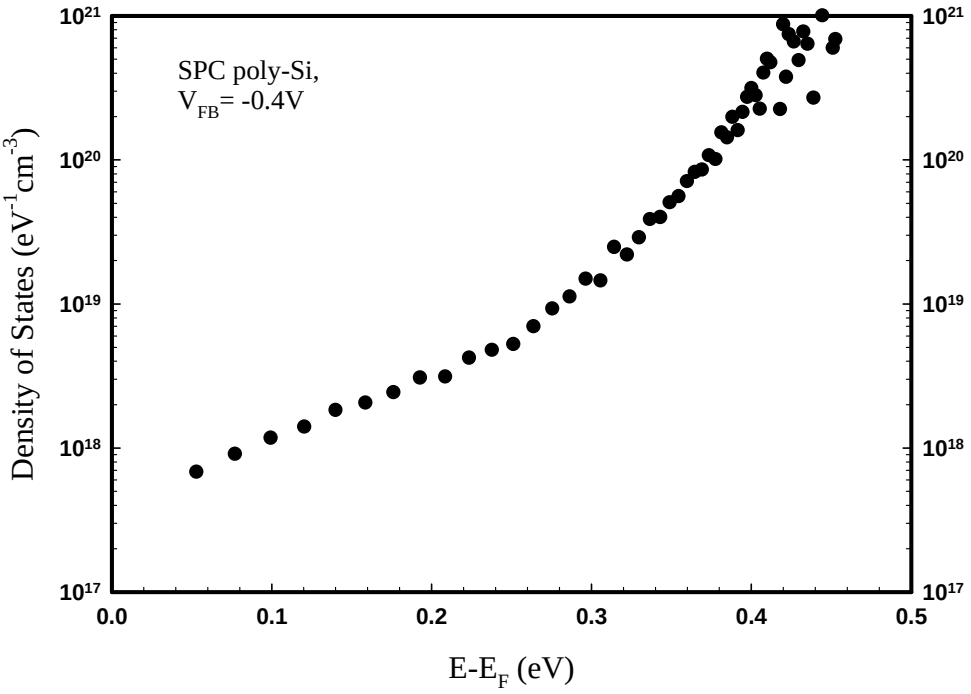

Fig. 3-5 Calculated density-of-states as a function of surface band-bending.

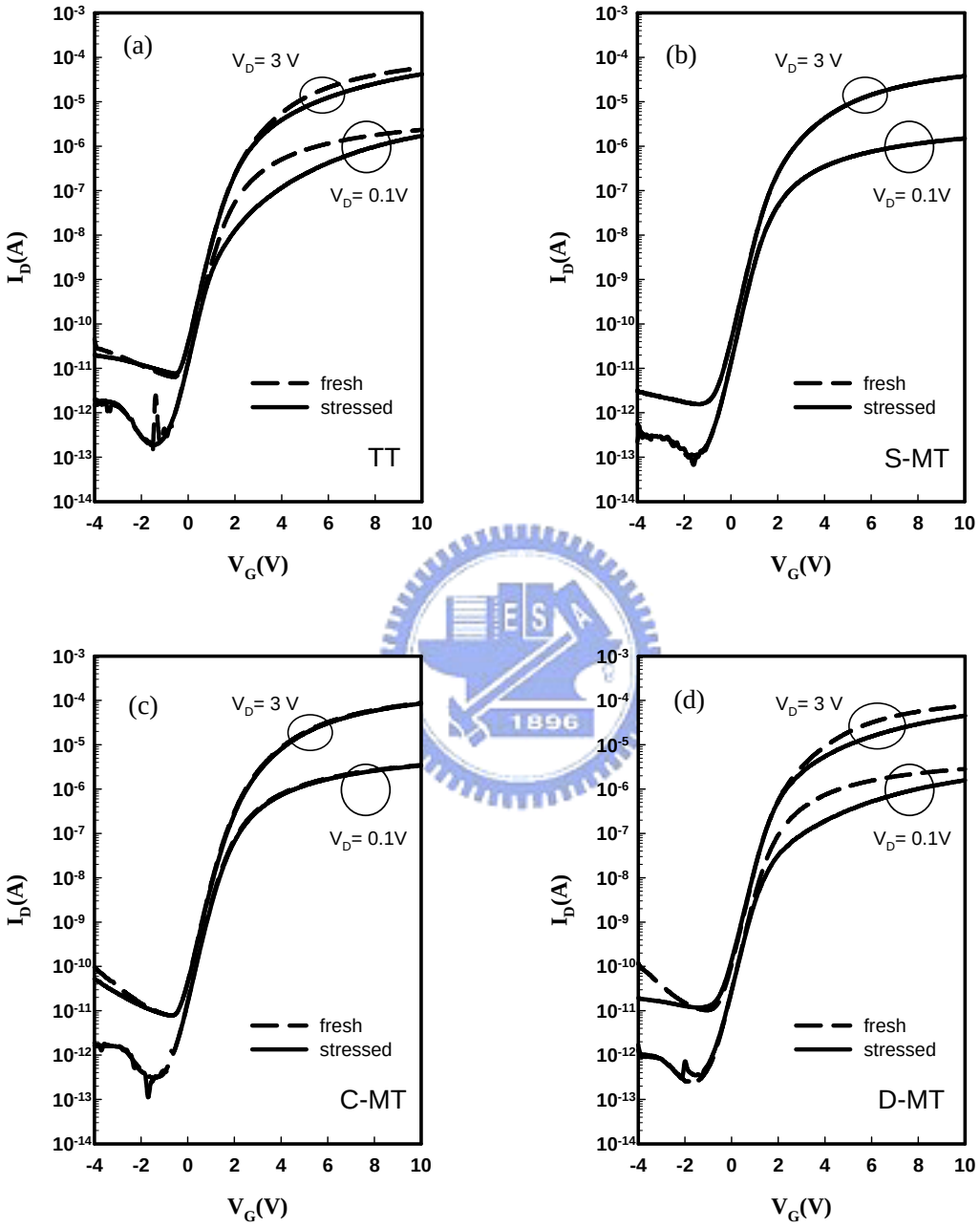

Fig. 3-6 Subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) D-MT transistors in the test structure before and after the AC stressing under V_{G_high}/V_D=7.5V/15V, freq.=500kHz, tr=tf=100ns and total stress time=1000sec.

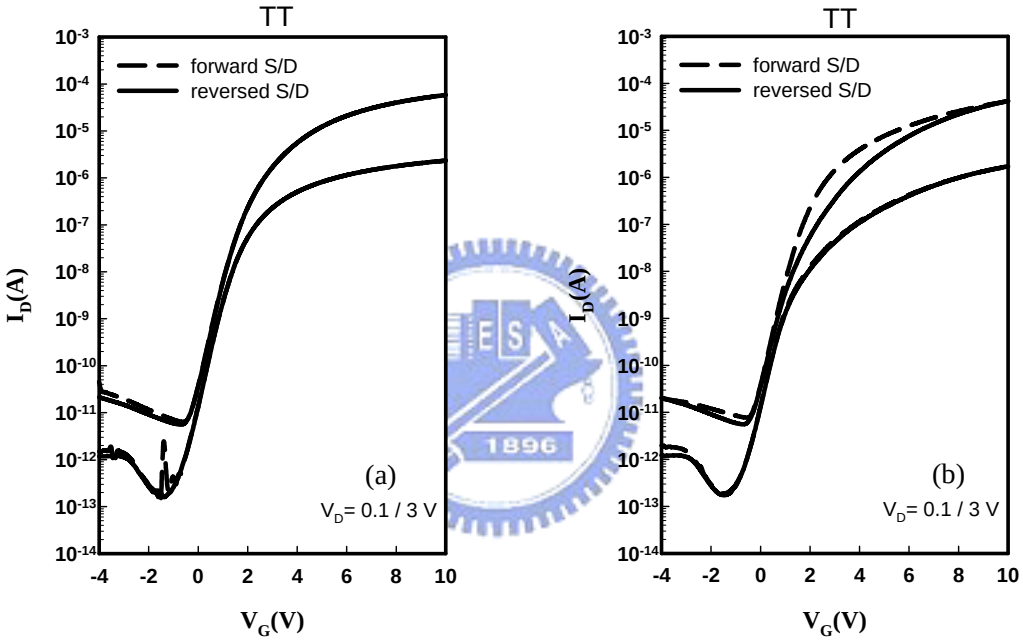

Fig. 3-7 Subthreshold characteristics of TT (a) before and (b) after AC stress measured under reversed S/D mode.

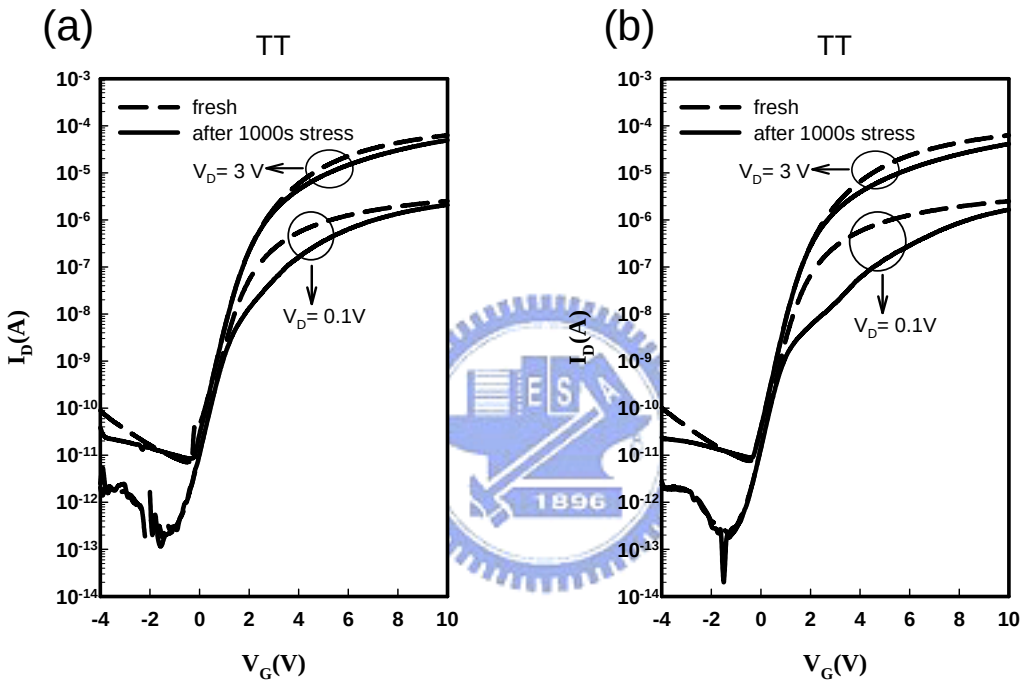

Fig. 3-8 Subthreshold characteristics of TTs before and after AC stress for 1000s with the frequency of (a) 100kHz and (b) 1MHz.

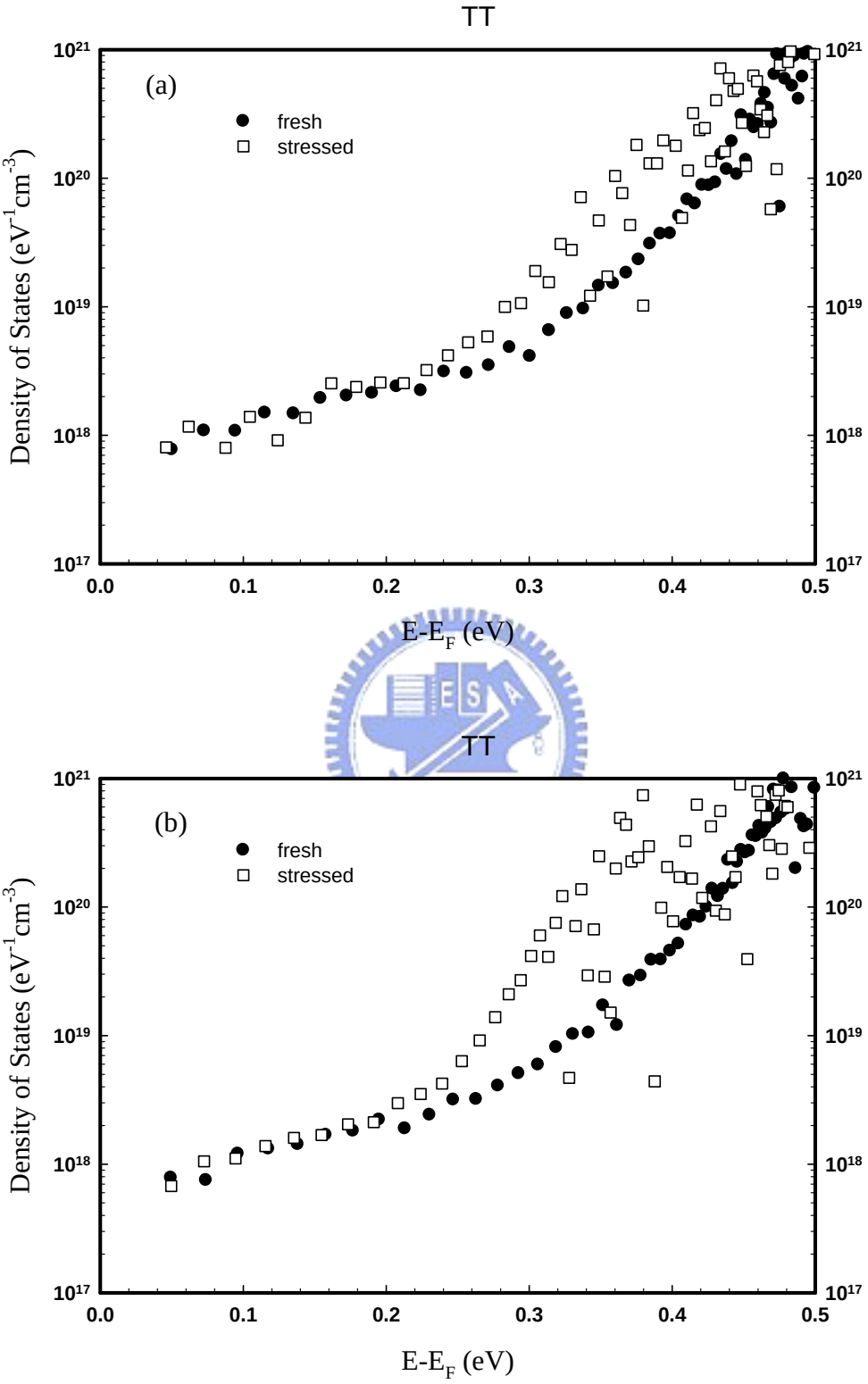

Fig. 3-9 Density-of-states distributions of TTs before and after AC stress for 1000s with the frequency of (a) 100kHz and (b) 1MHz.

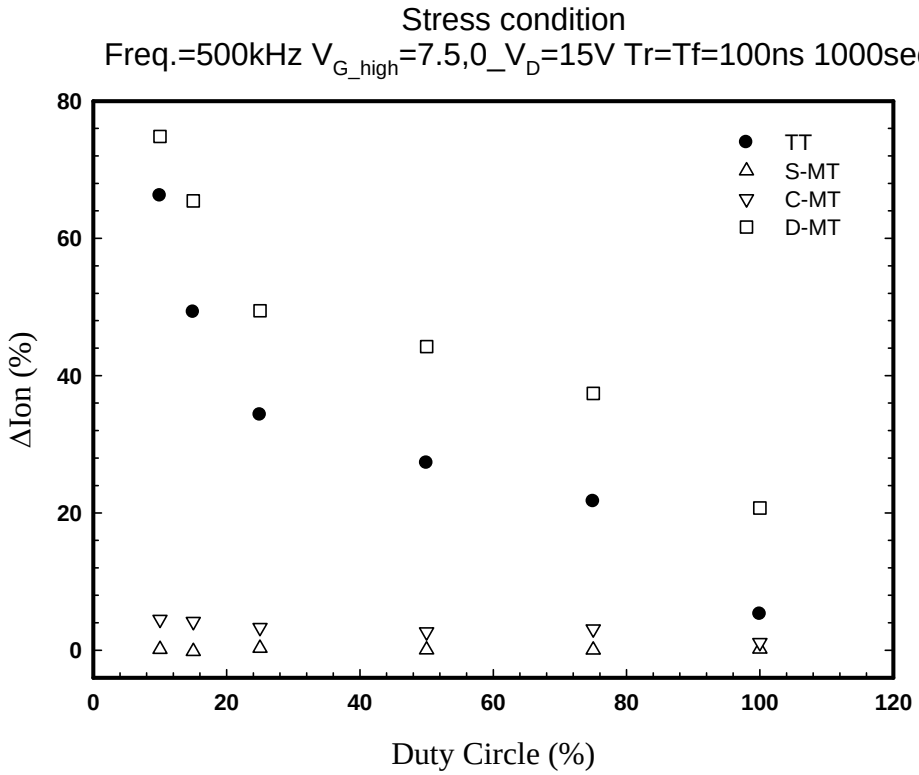

Fig. 3-10 On-current degradation of the testers after hot-carrier stressing as a function of duty cycle.

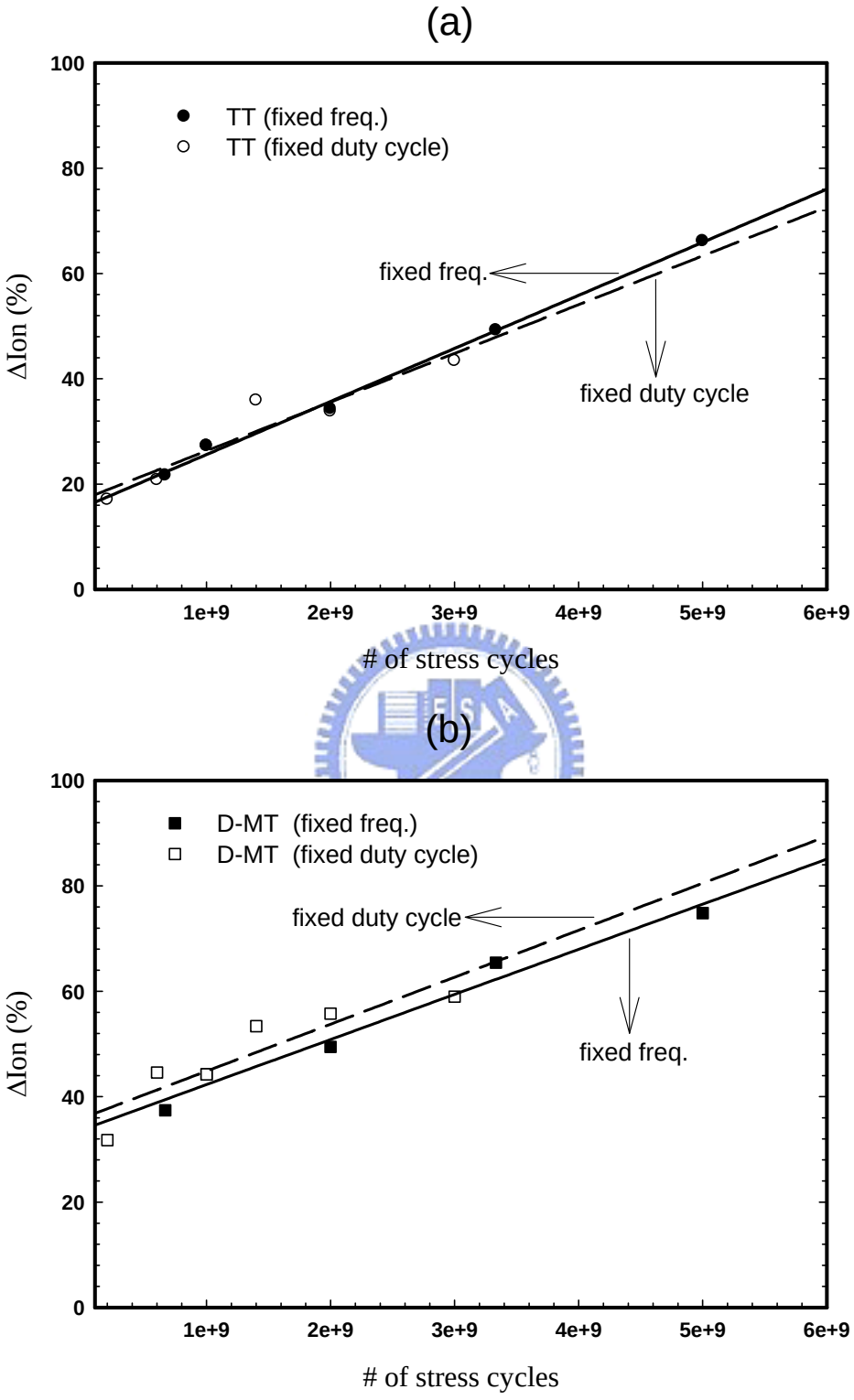

Fig. 3-11 On-current degradation of (a) TTs and (b) D-MTs after hot-carrier stressing as numbers of AC stress cycles.

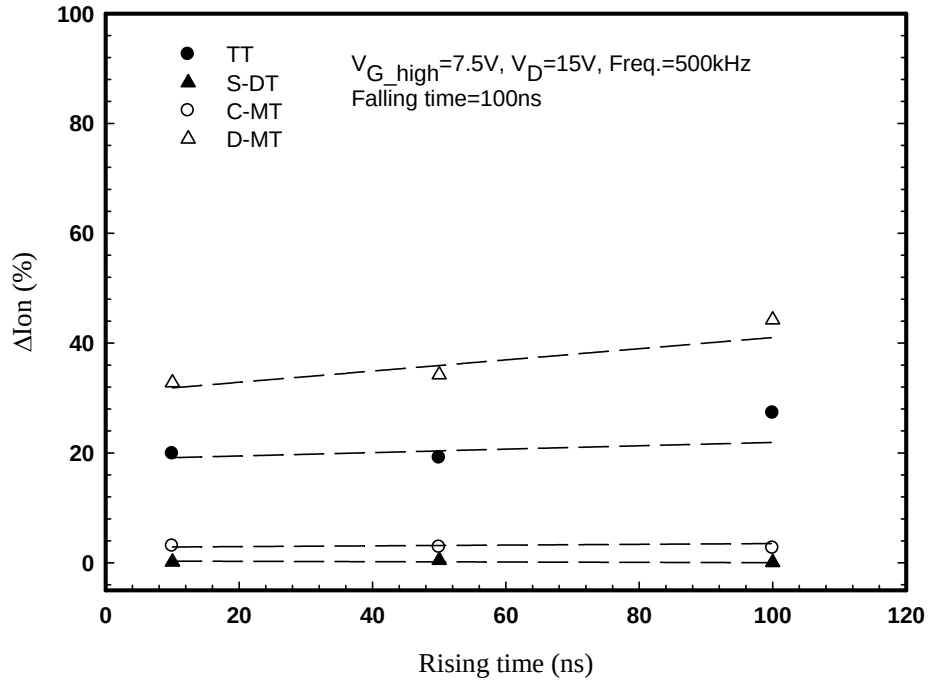

Fig. 3-12 On-current degradation of the testers after AC stressing, when applying a pulse voltage to gate, as a function of rising time.

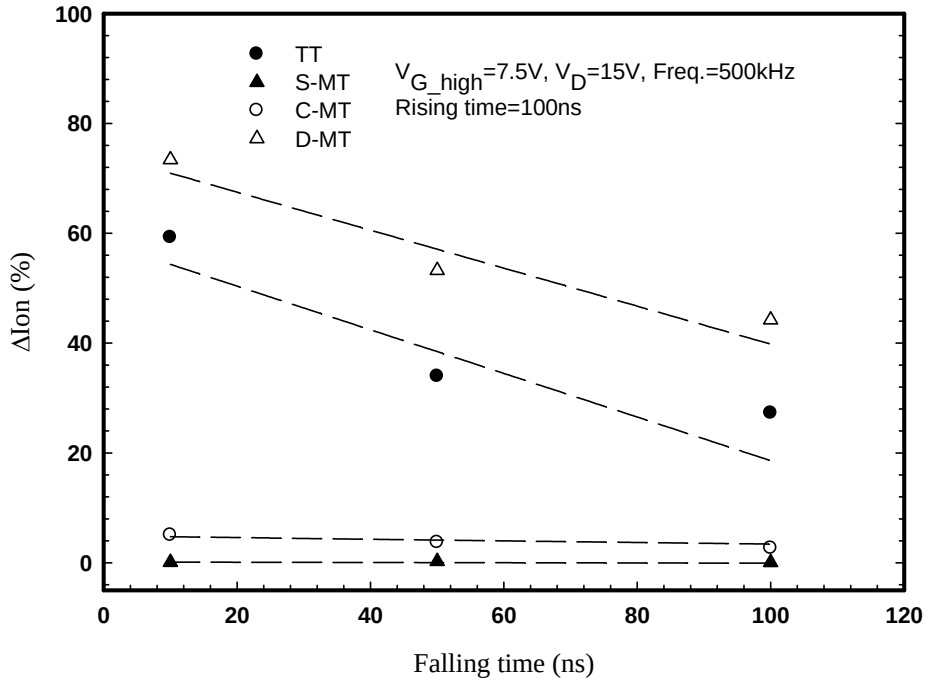

Fig. 3-13 On-current degradation of the testers after AC stressing, when applying a pulse voltage to gate, as a function of falling time.

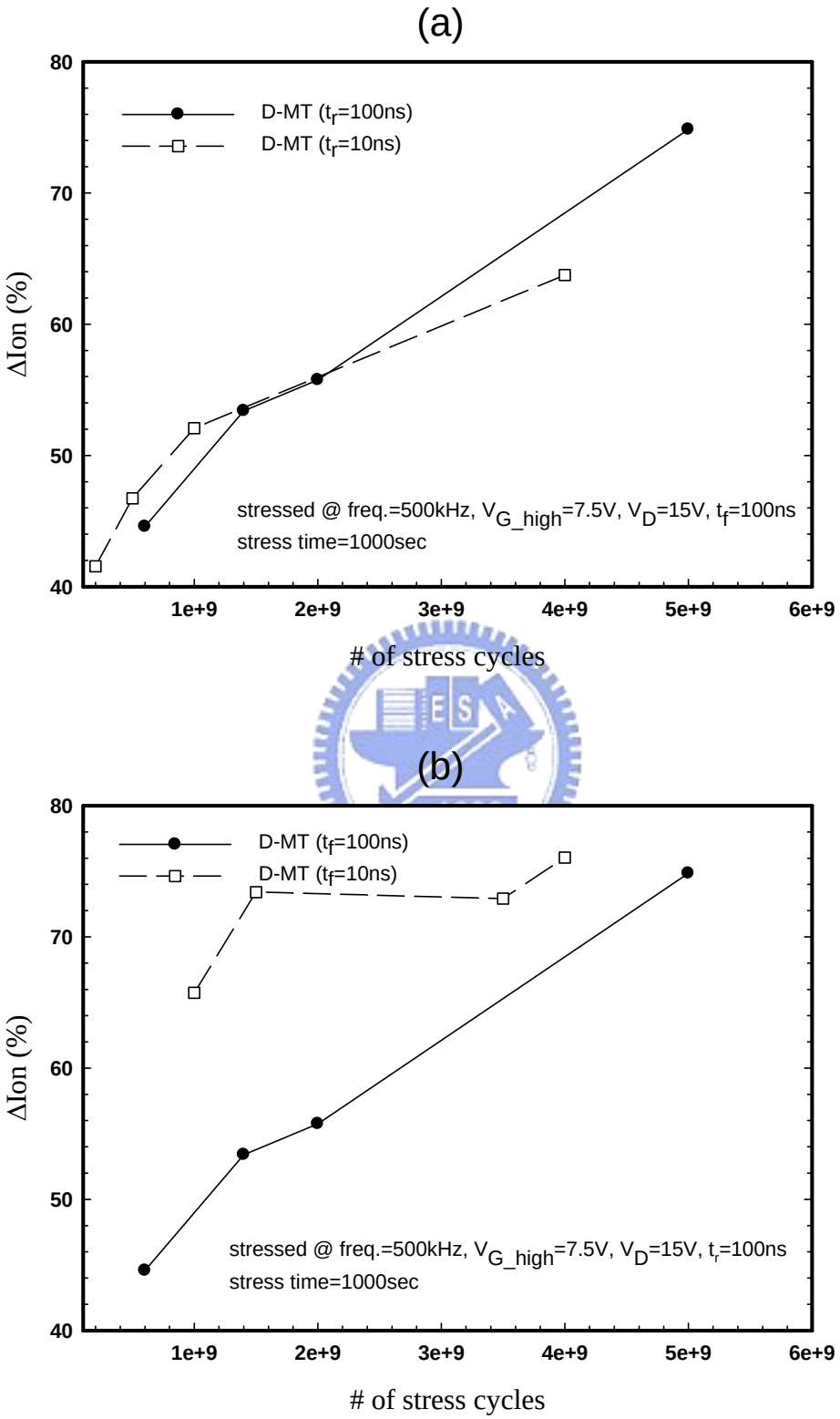

Fig. 3-14 On-current degradation of D-MTs with (a) fixed t_f=100ns and (b) fixed t_r=100ns after hot-carrier stressing as numbers of AC stress cycles.

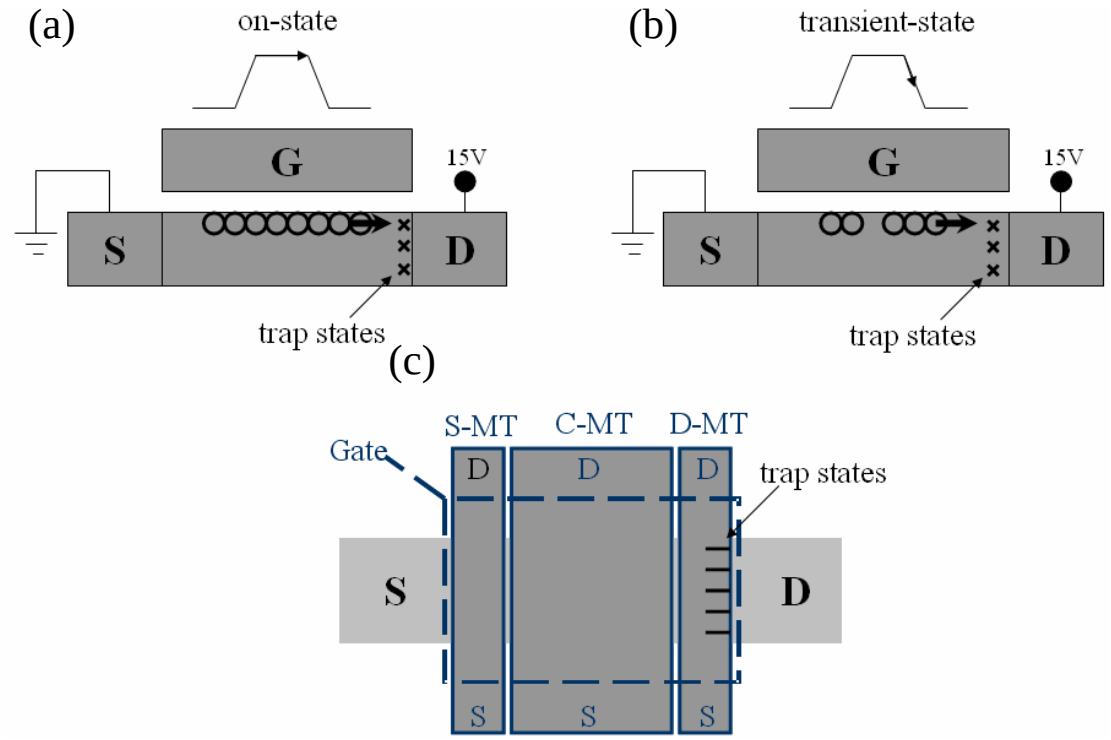

Fig. 3-15 Mechanisms of AC stress induced degradation.

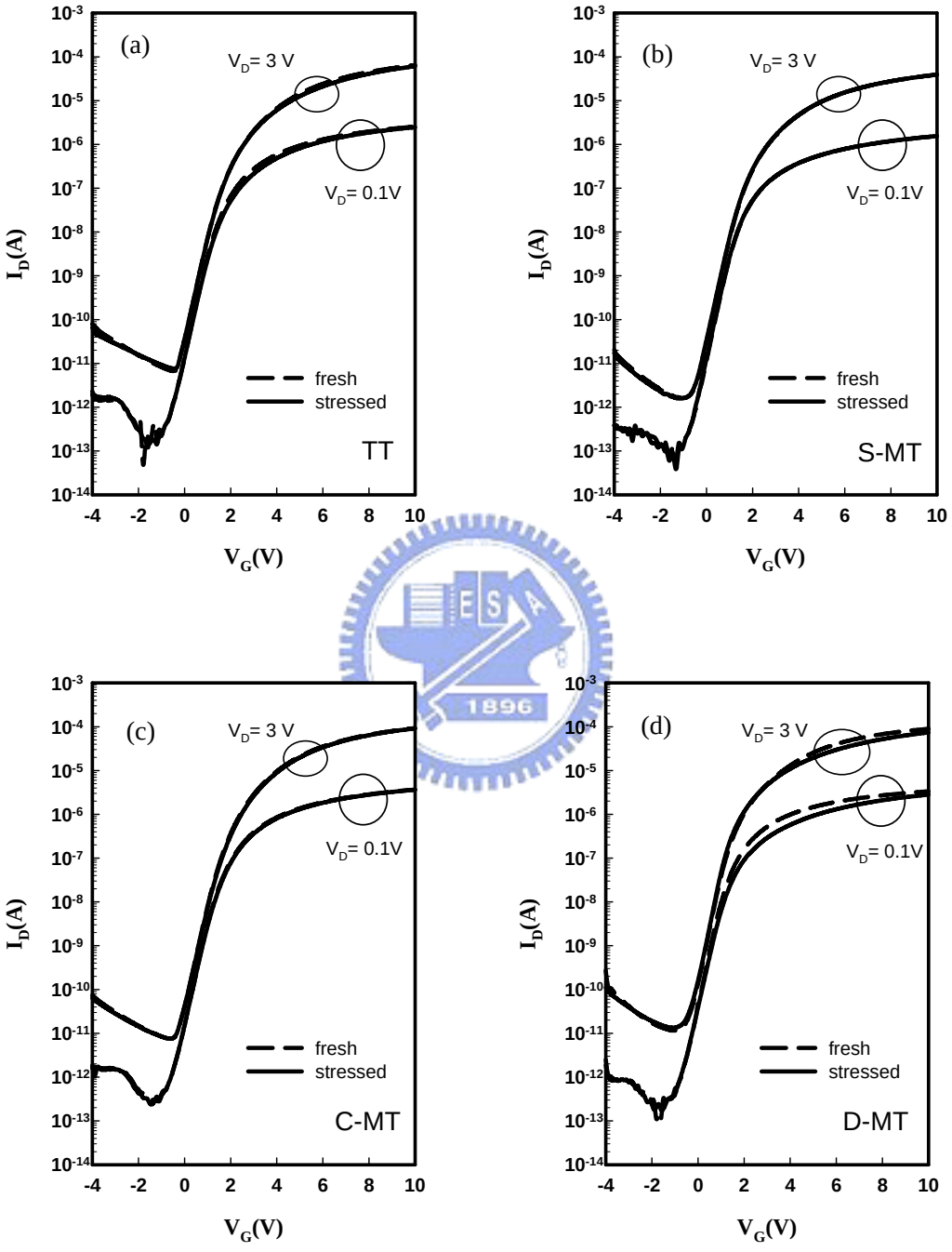

Fig. 3-16 Subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) D-MT transistors in the test structure before and after the AC stressing under V_G/V_{D_high}=7.5V/15V, freq.=500kHz, tr=tf=100ns and total stress time=1000sec.

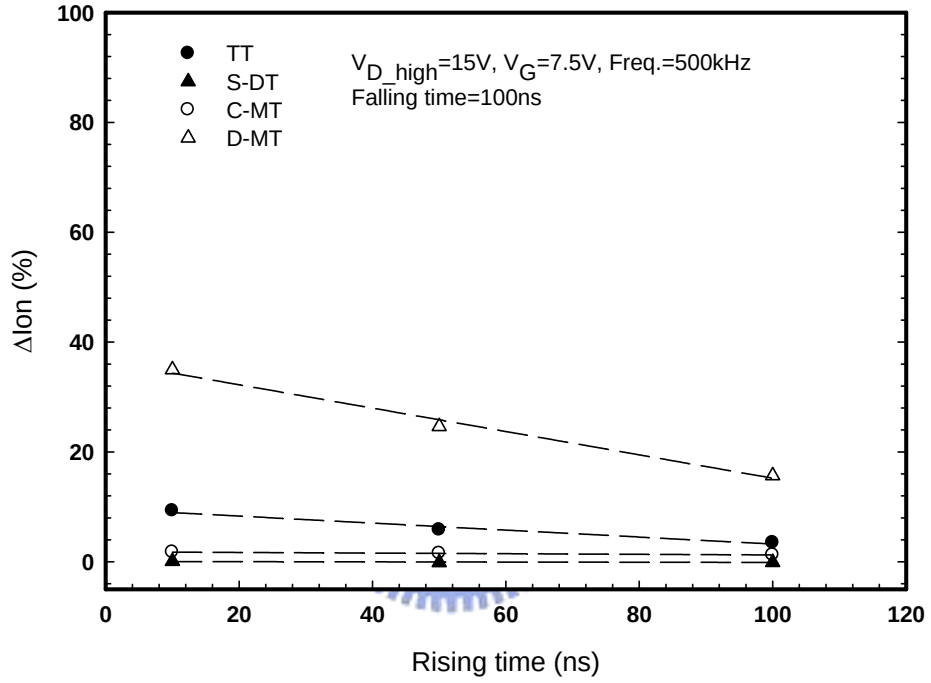

Fig. 3-17 On-current degradation of the testers after AC stressing, when applying a pulse voltage to drain, as a function of rising time.

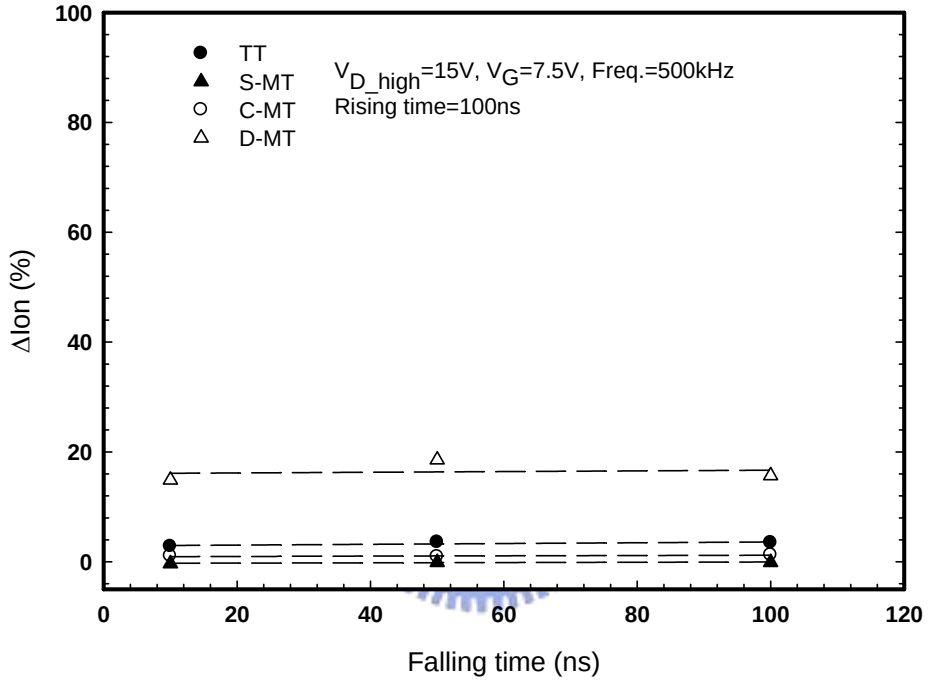

Fig. 3-18 On-current degradation of the testers after AC stressing, when applying a pulse voltage to drain, as a function of falling time.

簡 歷

姓名：張凱翔

性別：男

生日：70.11.11

籍貫：台灣省 台中市

住址：台中市南區永東街 73 號

學歷：

國立交通大學 電子工程研究所	2004.09～2008.08
國立中興大學 物理系	2000.09～2004.06
國立台中二中高級中學	1997.09～2000.06

論文題目：

利用一種新穎結構進行複晶矽薄膜電晶體之熱載子可靠性分析

A Study of Hot-Carrier Reliability for Poly-Si Thin-Film Transistors Using a Novel Test Structure