

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

基板材料對於堆疊式快閃記憶體寫入/

抹除效率的影響



**Effects of Substrate Materials on the
Programming/Erasing Efficiency of Stacked-Gate
Flash Memories**

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摘要

在半導體市場上，快閃記憶體因為不隨電源關閉而遺失資料的特性，近年來在可攜帶式商業產品上有了爆炸性的成長。各種元件尺寸隨著半導體世代而快速的微縮，但對於快閃記憶體而言，提供載子穿隧的氧化層若為了提高寫入/抹除速度而降低厚度，則會降低資料保存的期限，同時因為尺寸的微縮，即便是少量載子的損失，就會造成讀取資料時發生錯誤。從研究文獻得知，最適當的穿隧氧化層厚度約為 8 至 11 奈米。除非在元件結構、材料、或者操作機制上有所改變，否則無法改變目前快閃記憶體所面臨的窘境。近來銻相關的半導體元

件，因為較小的等效電子、電洞質量，而使得操作速度獲得了有效的提升。同時相較於矽基板，鍺基板擁有更為強烈因衝擊而游離產生電子、電洞對的效應，這使我們好奇是否將鍺材料應用於快閃記憶體，也同樣可以得到明顯的好處。

我們應用了軟體 ISE TCAD，來達成元件模擬的目的。由於該軟體是預設矽為主要製程、元件模擬對象，所以在進行模擬前，我們嘗試找出所有可以更改的參數，同時配合文獻中所提供的矽、鍺數學模型，來確保模擬結果的正確性。我們列出了所使用的數學模型包含：能帶模型、電致漂移率模型、衝擊離子化率模型、熱導模型、流體動力學模型、電容耦合模型；以及在寫入/抹除快閃記憶體時運用到的物理機制：F-N 穿隧機制、及熱載子穿隧機制。由於該軟體尚未提供鍺相關的製程模擬，所以我們僅藉由畫出元件結構後，再進行元件模擬。

我們利用通道熱電子穿隧以及 F-N 穿隧至浮閘的觀念分別寫入快閃記憶體；利用了 F-N 穿隧的概念，來進行記憶體的抹除。從通道熱電子穿隧寫入的模擬結果發現，由於控制閘極耦合電容的影響，加上電位移向量在半導體-氧化層界面連續的觀念，擁有較高介電常數的鍺反而得到較小的等效電場，決定了穿隧電流反倒是不如矽基板；在 F-N 穿隧寫入的模擬中，即便鍺基板擁有較大的總耦合電容，使得在浮閘的耦合電壓大於矽基板，但仍舊是半導體-氧化層界面的電場扮演了穿隧電流的決定性因素，得到的結果仍舊是矽基板的寫入速度高於鍺基板；在 F-N 抹除的模擬中，運用與 F-N 寫入相同的數學模型，仍舊看見在鍺基板上未能得到速度上的改善，同時用數學的計算展示了合理的解釋。

最後，我們提出了對於研究結果的簡單結論。同時對於模擬而言，最重要的還是需要實驗結果來驗證其正確性，並建立有效快速預測結果的數學型式，來省去大量的晶片耗損。最後列出了幾點將來研究的方向，以及尚需解決的問題。



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Abstract



A large amount of semiconductor markets are given by the semiconductor memories. The past decade in the field of Flash memories have been the explosive growth, driven by cellular phones and other portable equipments. In order to improve the speed of Flash cell, it is necessary to lower the tunneling oxide (TOX) thickness. However, this causes the loss of charges at the same time. According to the trade-off between speed and reliability, the thickness of TOX is compromised to about 8-11nm. Unless changing of device structures, materials, and operating mechanisms, we can't overcome the difficulty which Flash memories meet. Recently, germanium (Ge) has prompted renewed interest in Ge-based devices due to the lower effective mass and higher mobility of carriers in Ge as compared to silicon (Si). Ge also exhibits more serious impact ionization which is responsible for channel hot electrons (CHE) injection programming. We think the differences of Si and Ge in physical

characteristics may change the operating mechanisms, and bring some solutions to improve programming/erasing efficiency of Flash memories.

We use ISE TACD for our simulate work. The tool has set Si-related process and device simulation parameters as default. We have changed the parameters what we could found, basing on the published papers and books to make sure the simulate results. The models are: energy band model, mobility model, impact ionization rate model, thermal conductivity model, hydrodynamic model, and capacitive coupling model. The mechanisms are: Fowler-Nordheim (F-N) tunneling and hot carriers injection. All of the results are just gotten from device simulation but without process simulation since ISE still has no Ge-related process simulation.

We use CHE and channel F-N (CFN) to program the Flash cells respectively, and use F-N tunneling to erase the Flash cells. On CHE programming, the higher coupling ratio of control-gate (CG) makes the higher electrical field across TOX in Si than Ge. Also because of the continuity of displacement vector, the higher permittivity of Ge would cause the lower electrical field at interface. We get the higher gate current in Si than Ge. On CFN programming, the higher C_T in Ge would show the higher electrical field across TOX. However, the parameters of F-N tunneling are calculated and showing the gate current in Si is larger than Ge. On the same mechanism of F-N tunneling erasing, the parameters also show the higher electrical field (E_{inj}) of Si would cause the higher erasing speed. The continuity of displacement vector also explains the higher electrical field at interface for F-N tunneling programming/erasing.

Finally, we show the simple conclusions for our research. The simulate characteristics always need the experimental results to prove the correctness, and build the mathematical model. We also show recommendations for the future works.

誌 謝

碩士班兩年的生活，隨著論文寫作的完成，也將畫下最後的休止符。人生中每個階段的結束必然同時包含了一個嶄新的開始，然而意義非凡的是，這次的結束也將告別了習慣的學生生活，邁向全新的職場生活。

首先我要感謝我的父親及母親，一直以來在我成長的路上，總是默默的給予我支持，家裡的大小事總是怕影響我念書而一肩挑著，接下來我開始有能力幫你們負擔一些生活的壓力了；我要感謝我的姐姐，在我求學的路上給予我生活上的支助，讓我能專心於學業上；我要感謝我的指導教授葉清發博士、羅正忠博士，給予我專業以及為人處事態度上的教誨；我要感謝永裕學長、世璋學長，沒有你們的協助，我的碩士論文將無法順利完成，謝謝你們的照顧；我要感謝已經畢業的學長姐們，碩一時對於專業領域的陌生，是你們為我指引了一盞明燈；我要感謝實驗室的同伴：伯翰、文煜、國源、佳寧、建華、忠樂、國信、修豪，不管是學業上、生活上的幫助，還有一起走過的日子，記得要保持連絡；我要感謝碩一的學弟們，這一年來各方面的協助；我要感謝國家高速中心的羅仕京先生提供了我模擬軟體的協助；最後感謝我在電子所這兩年所結識的所有朋友，是你們豐富了我這兩年的回憶。

Contents

Abstract (in Chinese)	I
Abstract (in English)	IV
Acknowledgement	VI
Contents	VII
Figure Captions	X
Table Captions	XIV
Chapter 1 Introduction	1
1.1 Background.....	1
1.2 Motivation.....	2
1.3 Organization of the Thesis.....	3
Chapter 2 Physical and Mathematical Setting for Simulation	8
2.1 Simulate Tool.....	8
2.2 Modeling.....	8
2.2.1 Energy Band Model.....	8
2.2.2 Mobility Model.....	9
2.2.2.1 Constant Mobility Model.....	10
2.2.2.2 Hydrodynamic Canali Model.....	10

2.2.2.3 Driving Force Model.....	11
2.2.3 Impact Ionization Rate Model.....	11
2.2.4 Thermal Conductivity Model.....	13
2.2.5 Hydrodynamic Model.....	13
2.2.6 Capacitive Coupling Model.....	14
2.3 Programming and Erasing Mechanisms.....	14
2.3.1 Fowler-Nordheim (F-N) Tunneling.....	14
2.3.1.1 Programming.....	15
2.3.1.2 Erasing.....	16
2.3.2 Hot Carriers Injection.....	16

Chapter 3 Simulate Characteristics of Stacked-Gate Flash Memories with Silicon and Germanium Substrate.....31

3.1 Device Structure.....	31
3.2 Operating Conditions.....	31
3.3 Results and Discussions.....	31
3.3.1 I_d - V_g Characteristics of Silicon and Germanium Substrate.....	32
3.3.2 CHE Program Characteristics.....	32
3.3.2.1 Results.....	32
3.3.2.2 Discussions.....	32
3.3.2.3 Summary.....	34
3.3.3 CFN Program Characteristics.....	34
3.3.3.1 Results.....	34

3.3.3.2 Discussions.....	34
3.3.3.3 Summary.....	35
3.3.4 CFN and SFN Erase Characteristics.....	35
3.3.4.1 Results.....	35
3.3.4.2 Discussions.....	36
3.3.4.3 Summary.....	36
Chapter 4 Conclusions and Recommendations for Future Works.....	60
4.1 Conclusions.....	60
4.2 Recommendations for Future Works.....	61
Reference.....	63
Vita.....	67

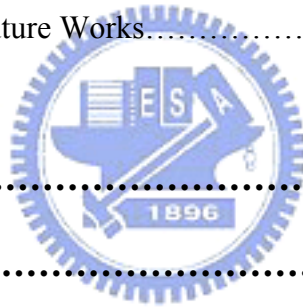


Figure Captions

Chapter 1

Fig. 1.1 Semiconductor market: revenues versus year. The bottom wave refers to the semiconductor memory amount.

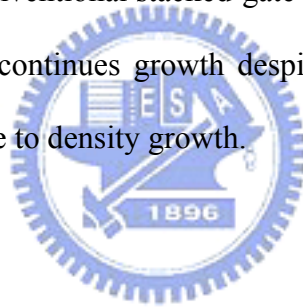
Fig. 1.2 MOS memory tree.

Fig. 1.3 Main memories attribute comparison.

Fig. 1.4 Semiconductor memory market for the main memories, i.e., DRAM, Flash, and SRAM.

Fig. 1.5 The structure of the conventional stacked-gate FG nonvolatile memory device.

Fig. 1.6 Nonvolatile memory continues growth despite the market's down cycle and falling average selling price due to density growth.



Chapter 2

Fig. 2.1 Energy band diagram of Si and Ge.

Fig. 2.2 A simplified energy band diagram used to describe semiconductor. Shown are the valence and conduction band as indicated by the valence band edge, E_v , and the conduction band edge, E_c . The vacuum level, E_{vacuum} , and the electron affinity, χ , are also indicated on the figure.

Fig. 2.3 Comparison of energy-band levels in Si and Ge.

Fig. 2.4 Temperature dependence of the energy bandgap of Si and Ge.

Fig. 2.5 The capacitive coupling model that using the capacitance between the FG and other electrodes.

Fig. 2.6 Energy band diagram of a FG memory during programming by F-N tunneling.

Fig. 2.7 A cross-section of a nonvolatile memory with electrons tunneling uniformly.

Fig. 2.8 Drain-side tunneling to program Flash.

Fig. 2.9 Energy band diagram of a FG memory during erasing by F-N tunneling.

Fig. 2.10 Uniform tunneling to erase Flash.

Fig. 2.11 Drain-side tunneling to erase Flash.

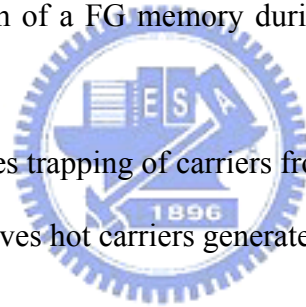
Fig. 2.12 DAHC injection involves impact ionization of carriers near the drain area.

Fig. 2.13 CHE injection involves propelling of carriers in the channel toward the oxide even before they reach the drain area.

Fig. 2.14 Energy band diagram of a FG memory during programming by hot-electron injection.

Fig. 2.15 SHE injection involves trapping of carriers from the substrate.

Fig. 2.16 SHGE injection involves hot carriers generated by secondary carriers.



Chapter 3

Fig. 3.1 Cross-section of the 0.5 μ m n-channel Flash structure. Asymmetric source/drain junction for enhanced source-side erasing efficiency.

Fig. 3.2 The definition of programming/erasing time.

Fig. 3.3 Drain current as a function of gate voltage when the cell is operated in linear region.

Fig. 3.4 Drain current as a function of gate voltage when the cell is operated in saturation region.

Fig. 3.5 CHE current injected to FG.

Fig. 3.6 CHE injection efficiency where the definition is $\frac{I_g}{I_d}$.

Fig. 3.7 The electrical field of TOX on CHE programming: (a) $V_g=0-20V$ (b) $V_g=0-5V$ (c) $V_g=5-10V$ (d) $V_g=10-15V$ (e) $V_g=15-20V$.

Fig. 3.7 The electrical field of IPD on CHE programming: (a) $V_g=0-20V$ (b) $V_g=0-5V$ (c) $V_g=5-10V$ (d) $V_g=10-15V$ (e) $V_g=15-20V$.

Fig. 3.9 Substrate current of stacked-gate Flash with Si and Ge substrate on CHE programming.

Fig. 3.10 CHE programming time as a function of CG voltage.

Fig. 3.11 The value of impact ionization for (a) Si (b) Ge.

Fig. 3.12 CHE programming electrical fields are shown as vector and probe some points of: (a) Si substrate (b) Ge substrate.

Fig. 3.13 CFN current injected to FG: (a) $V_g=0-20V$ (b) the zoom in of $V_g=9-10V$ to show the difference between Si and Ge.

Fig. 3.14 The electrical field of TOX on CFN programming: (a) $V_g=0-20V$ (b) the zoom in of $V_g=9-10V$ to show the difference between Si and Ge.

Fig. 3.15 The electrical field of IPD on CFN programming: (a) $V_g=0-20V$ (b) the zoom in of $V_g=9-10V$ to show the difference between Si and Ge.

Fig. 3.16 CFN programming time as a function of CG voltage.

Fig. 3.17 CFN programming electrical fields are shown as vector and probe some points of: (a) Si substrate (b) Ge substrate.

Fig. 3.18 The ϕ_b of Si and Ge.

Fig. 3.19 CFN and SFN current ejected from FG.

Fig. 3.20 The electrical field of TOX on CFN and SFN erasing.

Fig. 3.21 The electrical field of IPD on CFN and SFN erasing.

Fig. 3.22 CFN and SFN erasing time as a function of CG voltage.

Fig. 3.23 CFN and SFN erasing electrical fields are shown as vector and probe some points of: (a) Si substrate (b) Ge substrate.



Table Captions

Chapter 2

Tab. 2.1 Parameters used to calculate the energy bandgap of Si and Ge as a function of temperature.

Tab. 2.2 Lattice mobility constants.

Tab. 2.3 Canali model parameters.

Tab. 2.4 Default velocity saturation parameters.

Tab. 2.5 Coefficients for (2-15).

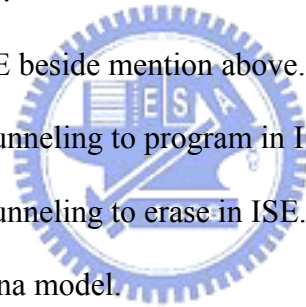
Tab. 2.6 Coefficients for (2-16).

Tab. 2.7 Parameters used in ISE beside mention above.

Tab. 2.8 Coefficients for F-N tunneling to program in ISE.

Tab. 2.9 Coefficients for F-N tunneling to erase in ISE.

Tab. 2.10 Coefficients for Fiegna model.



Chapter 3

Tab. 3.1 The operating voltage of electrodes for programming/erasing.

Tab. 3.2 The capacitances between the FG and other electrodes.

Tab. 3.3 The coupling ratios for (2-20).

Tab. 3.4 Electrical field at injection surface for CFN programming of Si and Ge substrate Flash.

Tab. 3.5 Electrical field at injection surface for CFN erasing of Si and Ge substrate Flash.