CHAPTER 1

Introduction

1.1 Background

Even if with some valleys and peaks, the semiconductor market has been continuously increasing, and this growing trend is expected to continue in the coming years. Semiconductor products have played a very important role in the electronics industry since its commercialization. A large amount of semiconductor markets, about 20% (Fig. 1.1), is given by the semiconductor memories in 2005 [1.1], based on the complementary metal-oxide-semiconductor (CMOS) technology. So, it is natural for research on memories going ahead with semiconductor generations.

CMOS memories can be divided into two main categories: (1) random access memories (RAM's), which are volatile, i.e., they lose stored information once the power supply is switched off, and (2) read-only memories (ROM's), which are nonvolatile, i.e., they keep stored information even when the power supply is switched off. The MOS memory tree could simply show the classification as Fig. 1.2. DRAM, SRAM, and Flash owned about 98% of the memory market in 2005 [1.2]. When we talk about the candidates of ideal memories, Flash memory shows owning all the advantages in density, nonvolatility, and electrical re-writablity (Fig. 1.3). The market of Flash memories almost overtakes DRAM's in 2006 and became higher amount than SRAM's in 1999 (Fig. 1.4) [1.1].

In 1960s', it was urgent to find a new kind of memory device to replace the magnetic-core memory which had high cost, large volume, and high power consumption. In 1967, K. Kahng and S. M. Sze invented the floating-gate (FG)

nonvolatile semiconductor memory at Bell Labs [1.3]. To date, the most widespread memory array organization has a byte-selectable write operation combined with a sector “flash” erase, so is so-called Flash memory. Fig. 1.5 shows the stacked-gate FG device structure. The phenomenon of this past decade in the field of semiconductor memories has been the explosive growth of the Flash memory market, driven by cellular phones and other types of electronic portable equipment (palm top, mobile PC, mp3 audio player, digital camera, and so on). Also with the worldwide shift to mobile appliances for communications, computing, and entertainment, electronic equipment manufacturers have increasingly required cost-effective nonvolatile memory solutions able to maintain data or software code without power, low-cost Flash memory devices just have satisfied this need, elevating Flash to an increasingly vital position in the semiconductor industry. As a critical component in market-leading mobile products, Flash memory has exhibited steady growth, even through the market’s down cycle (Fig. 1.6) [1.4].

1.2 Motivation

Although a huge commercial success, Flash memory devices have their limitations. As Flash scales into sub-100nm regime, challenges arise due to some problems. The tunneling oxide (TOX) exists not only for charges tunneling from channel to FG, but also for the isolation as charges have reached FG. If we want quick and efficient charge transfer, it is necessary to lower the TOX thickness. On the other hand, the charges need to maintain information integrity over periods of up to a decade, thicker oxide thickness is an intuitional choice. Therefore, there is a trade-off between speed and reliability and the thickness of TOX is compromised to about 8-11nm, which is barely reduced over more than five successive generations of the industry [1.5]. The programming/erasing mechanisms that Flash uses need high power supply. That’s

unsuitable for memory embedding in logic circuits if thinking about the system-on-chip (SOC) concept. In order to get the same operating speed, higher coupling ratio may lower the need of power. To solve the problems, there are two (or more) ways for Flash memories: (1) to change the structure of the conventional FG Flash cell (2) to change the materials of the TOX, inter-poly dielectric (IPD), or the substrate. For (1), two candidates are mostly mentioned, SONOS and nanocrystal nonvolatile memory devices [1.6-1.10]. For (2), the high-k materials used for TOX and IPD are suggested [1.11].

There is still no research about the substrate materials of stacked-gate Flash memories. Recently, germanium (Ge) has prompted renewed interest in Ge-based devices due to the lower effective mass and higher mobility of carriers in Ge as compared to silicon (Si) (two times higher mobility for electrons and four times for holes). By changing the Si substrate into Ge, the raising drive-in current may provide the chance of electrons (or holes) tunneling to FG. That may be good for improving programming speed. The differences of Si and Ge in physical characteristics may change the operating mechanisms, and bring some solutions to improve programming/erasing efficiency of Flash memories. In order to get the same speed in programming and erasing, Ge substrate Flash might lower the need of high voltage and high power consumption.

1.3 Organization of the Thesis

There are four chapters in the thesis. Chapter 1 shows the background about semiconductor memories market (CMOS memories market), and points out the classifications of CMOS memories: volatile and nonvolatile. Thinking about the advantages of nonvolatile memories, Flash attracts much attention because of its ideal characteristics. However, Flash memories also own some problems with the

scaling-down trend of semiconductor size. Obviously, the thickness of TOX couldn't follow the scale-down trend because of the reliability issues. So we want to find some ways of keeping TOX thickness and raising the speed at the same time. Ge-based devices attract much attention because of its low effective mass. We try to change substrate materials and check the feasibility of Ge substrate Flash memories.

Chapter 2, we list the models and mechanisms used in the simulation. The models are: Energy band model, mobility model, impact ionization rate model, thermal conductivity model, hydrodynamic model, and capacitive coupling model. The mechanisms include: Fowler-Nordheim (F-N) tunneling and hot carriers injection. All of the parameters that we could find to make differences in Si and Ge are shown in this chapter. The equations also give us some ideas to explain the results of simulation.

Chapter 3 shows the simulate results and discussions. The programming operation uses channel hot electrons (CHE) injection and channel F-N (CFN) tunneling mechanism, respectively. The erasing operation uses the CFN and source F-N (SFN) tunneling mechanism at the same time. All the discussions come after the simulation results, and summaries would be made in the end of each section.

Finally, the chapter 4, we make conclusions about this researching topic and describe the future works for existed problems and related topics.

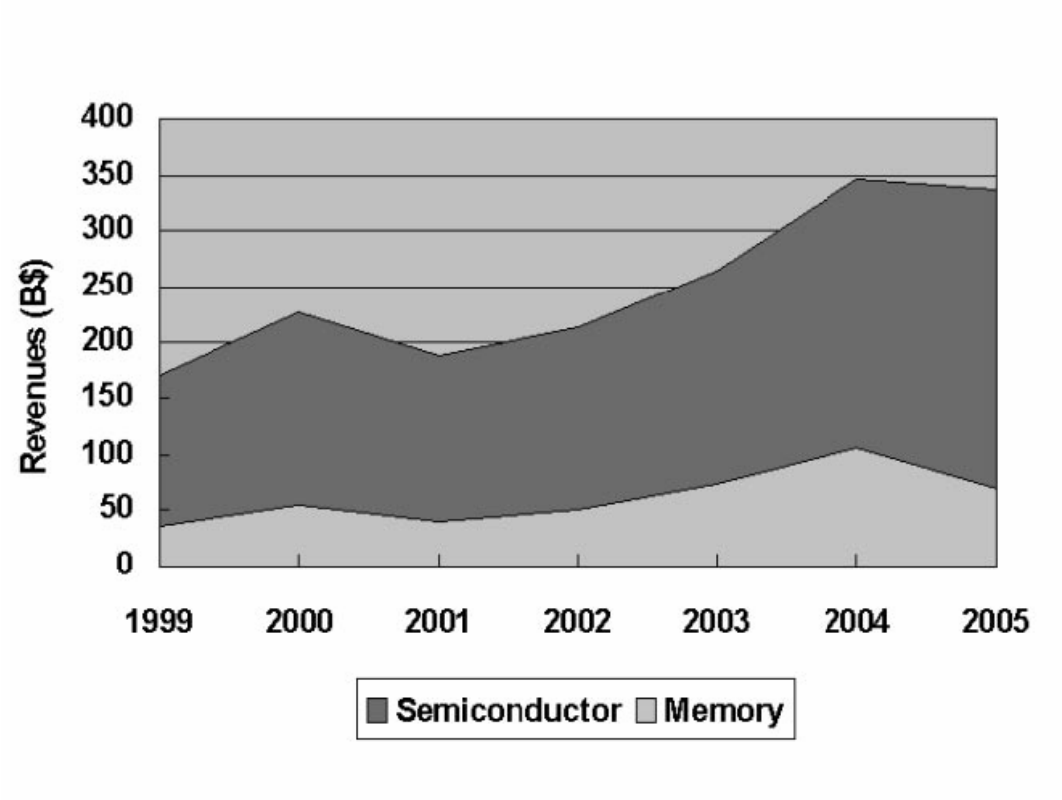


Fig. 1.1 Semiconductor market: revenues versus year. The bottom wave refers to the semiconductor memory amount.

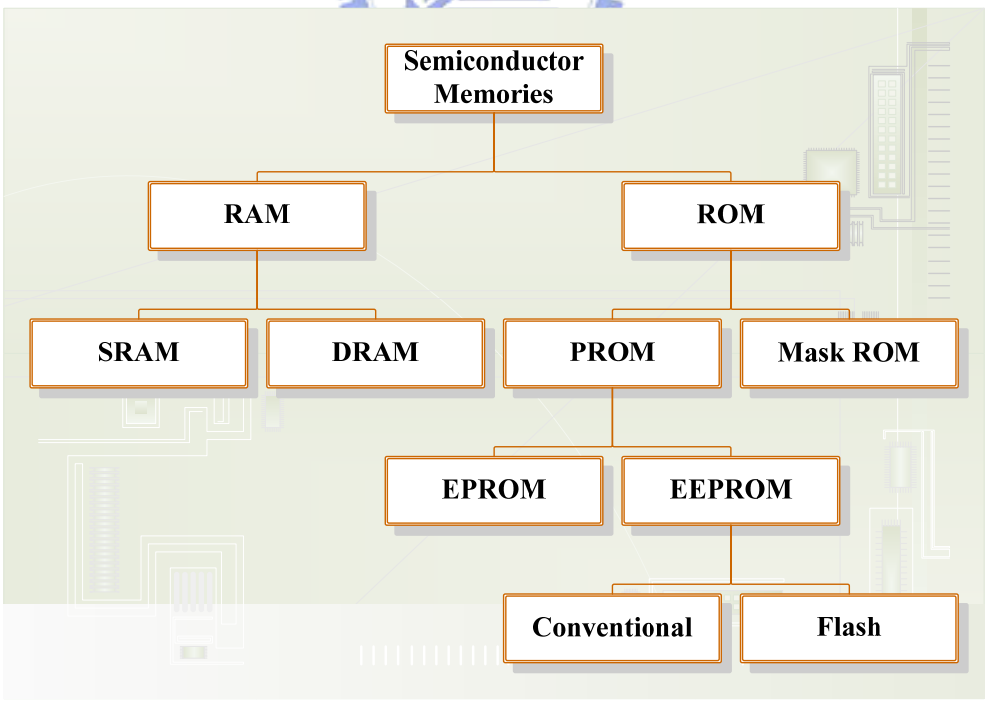


Fig. 1.2 MOS memory tree.

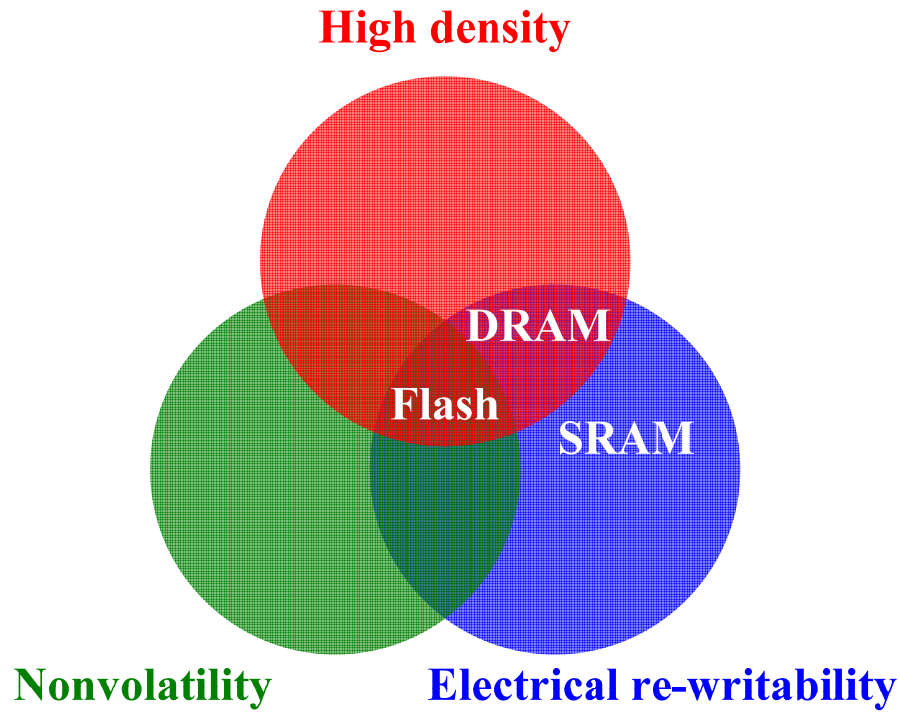


Fig. 1.3 Main memories attribute comparison.

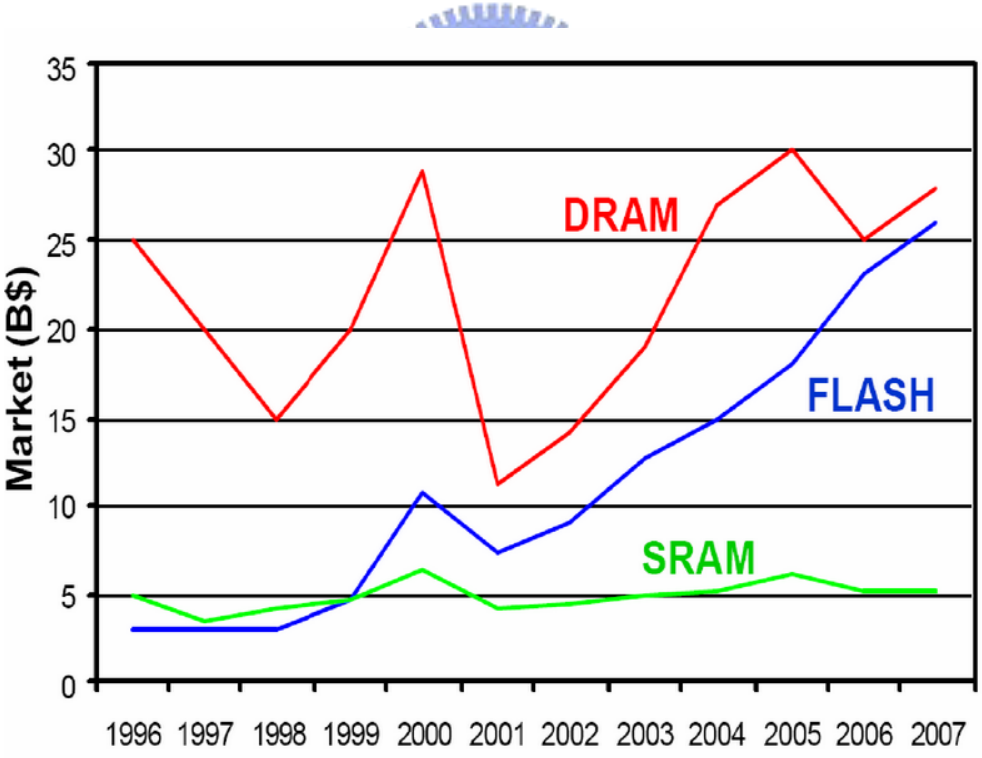


Fig. 1.4 Semiconductor memory market for the main memories, i.e., DRAM, Flash, and SRAM.

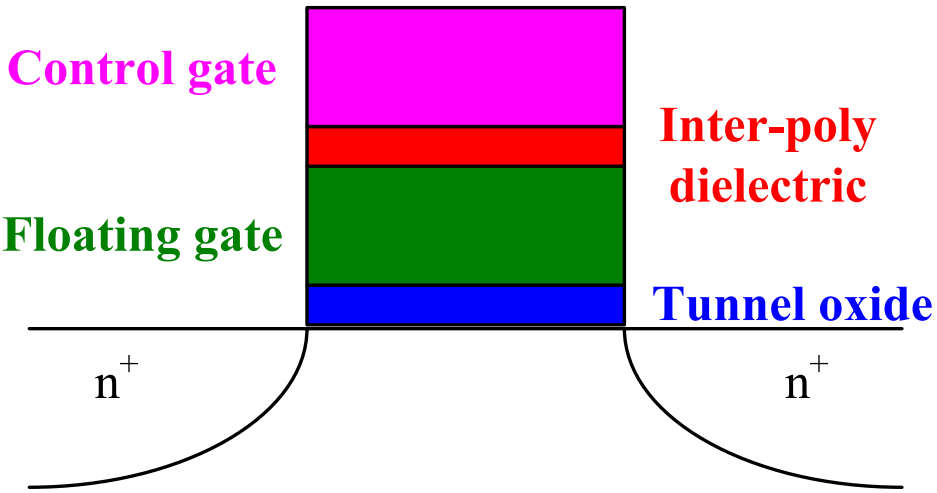
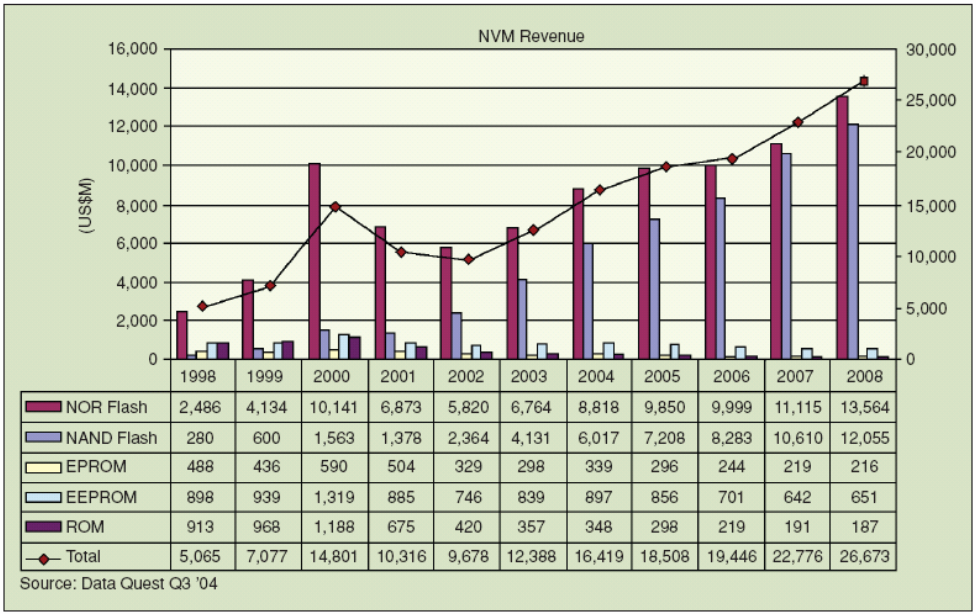


Fig. 1.5 The structure of the conventional stacked-gate FG nonvolatile memory device.



	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008
NOR Flash	2,486	4,134	10,141	6,873	5,820	6,764	8,818	9,850	9,999	11,115	13,564
NAND Flash	280	600	1,563	1,378	2,364	4,131	6,017	7,208	8,283	10,610	12,055
EPROM	488	436	590	504	329	298	339	296	244	219	216
EEPROM	898	939	1,319	885	746	839	897	856	701	642	651
ROM	913	968	1,188	675	420	357	348	298	219	191	187
Total	5,065	7,077	14,801	10,316	9,678	12,388	16,419	18,508	19,446	22,776	26,673

Fig. 1.6 Nonvolatile memory continues growth despite the market's down cycle and falling average selling price due to density growth.