CHAPTER 3

Simulate Characteristics of Stacked-Gate Flash Memories with Silicon and Germanium Substrate

3.1 Device Structure

We use 0.5μm stacked-gate n-channel Flash memory with silicon (Si) and germanium (Ge) substrate. SiO_2 is used to be tunneling oxide (TOX) and inter-poly dielectric (IPD) with thickness 100Å and 140Å, respectively. In order to achieve high speed operation for both programming and erasing, an asymmetric structure has been adopted in the source and drain regions. The junction depths of source and drain are 0.4μm and 0.3μm, respectively. The overlap of stack-gate and source/drain is about 0.05μm. N^+-type poly-Si was used as floating-gate (FG) and control-gate (CG). Fig. 3.1 shows the cross-sectional view of simulate device structure.

3.2 Operating Conditions

For comparison, we use channel hot electrons (CHE) injection or channel Fowler-Nordheim (CFN) tunneling to program the devices. All of the devices are erased by the CFN and source side F-N (SFN) ejection at the same time, assuming $(-1)\times10^{-15}$C/μm charges pre-existed in FG. All the operating voltages are listed in Tab. 3.1. We define the programming/erasing time as the shift of devices threshold voltage (V_{th}) reaching 1.5 volts during measurement. The Fig. 3.2 defines the programming/erasing time

3.3 Results and Discussions

3.3.1 I_d-V_g Characteristics of Si and Ge Substrate

If we treat the stack-gate of Flash memory as a conventional gate, the drain current as a function of gate voltage is shown in Fig. 3.3 and Fig. 3.4 for linear and saturation region, respectively. The Ge substrate Flash exhibits higher subthreshold swing (SS) when operating in high drain voltage, which is caused by inevitable drain turn-on. It is known drain turn-on is proportional to the drain coupling ratio α_d which is defined as $\alpha_d = \frac{C_D}{C_T}$. However, Ge Flash also has the higher off-state current (about 1 order higher than Si). It means that we often need spending power consumption to change the speed.

3.3.2 CHE Program Characteristics

3.3.2.1 Results

The CHE current injected to FG of stacked-gate Flash memories with Si and Ge substrate is compared in Fig. 3.5. Fig. 3.6 shows the injection efficiency that could give a sense about how many carriers turn into vertical path and have chance to form the gate current. The electrical fields across TOX and IPD are shown in Fig. 3.7 and Fig. 3.8, respectively. We often detect the substrate current to know the amount of hot carrier generation which is caused by impact ionization, and Fig. 3.9 shows the substrate current when we programming the Flash by CHE. The typical programming time is 10μs and Fig. 3.10 shows the programming time as a function of CG voltage.

3.3.2.2 Discussions

According to Fig. 3.7 and Fig. 3.8, the electrical field between TOX could explain the changing of gate current along with gate voltage. From (2-20), we know that the voltage of FG is composed by four terms. On CHE programming, only α_g and α_d influence the FG coupling voltage. The capacitances of the capacitive coupling model are shown in Tab. 3.2. The coupling ratios are calculated and shown in Tab. 3.3. For Si, α_g is bigger than Ge's. Even though the α_d of Ge is bigger than Si's, the applied CG voltage could reach four times higher than drain voltage. When CG voltage is small, the drain coupling voltage can make the higher FG voltage and electrical filed between TOX. When CG voltage exceeds 5V, the term $\alpha_g V_g$ is more critical.

From the Fig. 3.9, we see the more serious impact ionization of Ge. We also show the value of impact ionization in Fig. 3.11. It is necessary to remind that the colors representing the strength of impact ionization in the figure are not identical. The simulate tool would set red color as default for highest strength. It's obvious that the junction of drain for Ge substrate exhibits more impacting events. When hot carriers go reaching the interface of semiconductor-insulator, they need vertical electrical field for tunneling to FG. The Fig. 3.12 probes some points to show the electrical field between Si/Ge substrate Flash and oxide interface. We could see the Si-oxide interface exhibits higher electrical field than Ge-oxide interface. The reason could be explained by the continuity of displacement vector:

$$\varepsilon E = \varepsilon_{OX} E_{OX} \tag{3-1}$$

Supposing the same value of displacement vector is got, the higher permittivity of Ge would lower the electrical field at Ge-oxide interface. That's also telling the Ge substrate Flash has no expectable results of higher tunneling current.

In order to meet the typical programming time, according to Fig. 3.10, the operating CG voltage may reach about 11~12V, the results disagree with the supposition of high impact ionization would improve gate current and lower the need

of operating voltage.

3.3.2.3 Summary

When the voltage below 5V, drain coupling may cause FG voltage of Ge is higher than Si. But if the CG voltage exceeds 5V, the CG coupling voltage is more important for the electrical field between TOX and IPD. The continuity of the displacement vector also tells the interface electrical field of Si is higher than Ge. In order to meet the typical programming time, the high operating voltage (11~12V) is still a problem needing to solve.

3.3.3 CFN Program Characteristics

3.3.3.1 Results

The CFN current injected to FG of stacked-gate Flash memories with Si and Ge substrate is compared in Fig. 3.13. The electrical fields across TOX and IPD for tunneling current to FG are shown in Fig. 3.14 and Fig. 3.15, respectively. Fig. 3.16 shows the programming time as a function of CG voltage.

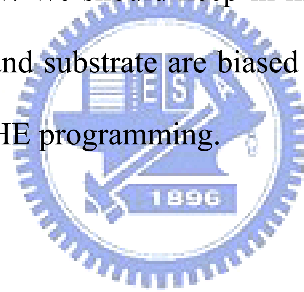
3.3.3.2 Discussions

According to Fig. 3.13, the Si substrate Flash gets little higher gate current than Ge. From the coupling ratios in Tab. 3.3, the CG voltage also plays the key role of FG coupling voltage. However, the differences between Si and Ge are not obvious. The same reason in (3-1), Si may get higher electrical field at interface. Fig. 3.17 probes some points and shows the electrical field of Si and Ge substrate Flash at semiconductor- insulator interface.

Further more, according to (2-21)-(2-23), the parameter ϕ_b which means energy

barrier at the injection surface is shown in Fig. 3.18, and the E_{inj}=Electric field at the injection surface $=\frac{V_{app}-V_{fb}}{t_{ox}}$. We use n^+-poly-gate, so the V_{fb} could be substituted by $-\left(\frac{E_g}{2e}+\phi_{fp}\right)-\frac{Q'_{ss}}{C_{ox}}$. For Si and Ge, we substitute the known values into the E_{inj} and show in Tab. 3.4. According to Fig. 3. 14, the electrical field of TOX (V_{app}) for Ge is larger than Si, however, we could see in Tab. 3.4, even if V_{app} of Ge is larger than Si, the term 0.9678 in Si and 0.5459 in Ge causes the E_{inj} of Si is larger than Ge when supposing the same Q'_{ss}. That shows again the electrical field at interface of Si is larger than Ge and causes the higher gate current on CFN programming.

In order to meet the typical 10μs programming time, according to Fig. 3.16, the operating voltage exceeds 15V. We should keep in mind that on CFN programming, the voltage of source, drain, and substrate are biased in (-5)V. That means the power need for CFN is much than CHE programming.



3.3.3.3 Summary

ϕ_b and E_{inj} are the most important two parameters for FN tunneling. From the calculating and simulating results, we get the higher electrical field across the TOX of Ge substrate Flash memory but lower gate current to FG. That's caused by the interface electrical field between semiconductor and insulator. Comparing with CHE programming, the CFN programming is much power spending.

3.3.4 CFN and SFN Erase Characteristics

3.3.4.1 Results

The CFN and SFN current ejected from FG of stacked-gate Flash memories with Si

and Ge substrate is compared in Fig. 3.19. The electrical fields across TOX and IPD for tunneling current from FG and are shown in Fig. 3.20 and Fig. 3.21, respectively. The typical erasing time is 10ms and Fig. 3.22 shows the erasing time as a function of CG voltage.

3.3.4.2 Discussions

According to Fig. 3.19, the erasing current of Si is larger than Ge. Differing from the CFN programming, the electrical field of TOX in Ge is lower than in Si. The reason is, when on CFN programming, the four electrodes are biased and would supply the coupling voltage for the FG, however, there are only two electrodes are used and the CG coupling ratio becomes critical. Then, we also take the E_{inj} into consideration, the known values of parameters are substituted and shown in Tab. 3.5. The term 0.9678 in Si and 0.5459 in Ge still strongly influence the electrical field at interface. The continuity of displacement vector, again, with Fig. 3.23 show the electrical field at interface.

In order to meet the typical 10ms erasing time, the operating voltage of CG needs about 11V which is too high to embed in logic circuits.

3.3.4.3 Summary

The same as CFN programming, the parameters of FN tunneling current mechanism give the reason of simulate results. The electrical field at interface also exhibits higher in Si and results the better speed in erasing.

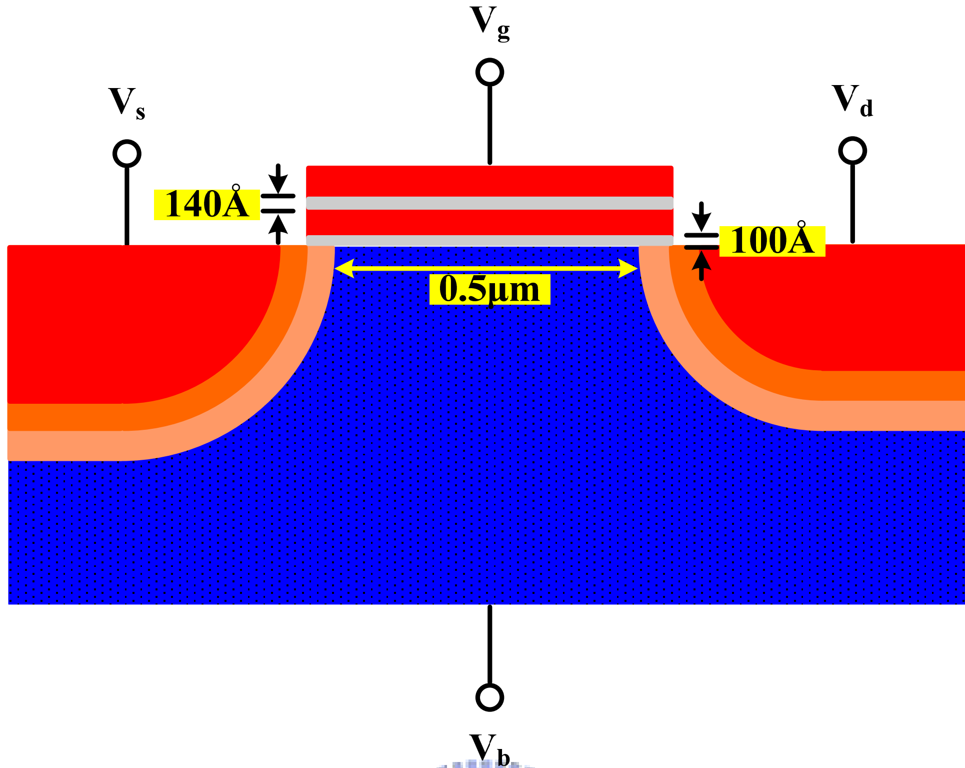


Fig. 3.1 Cross-section of the 0.5μm n-channel Flash structure. Asymmetry source/drain junction for enhanced source-side erasing efficiency.

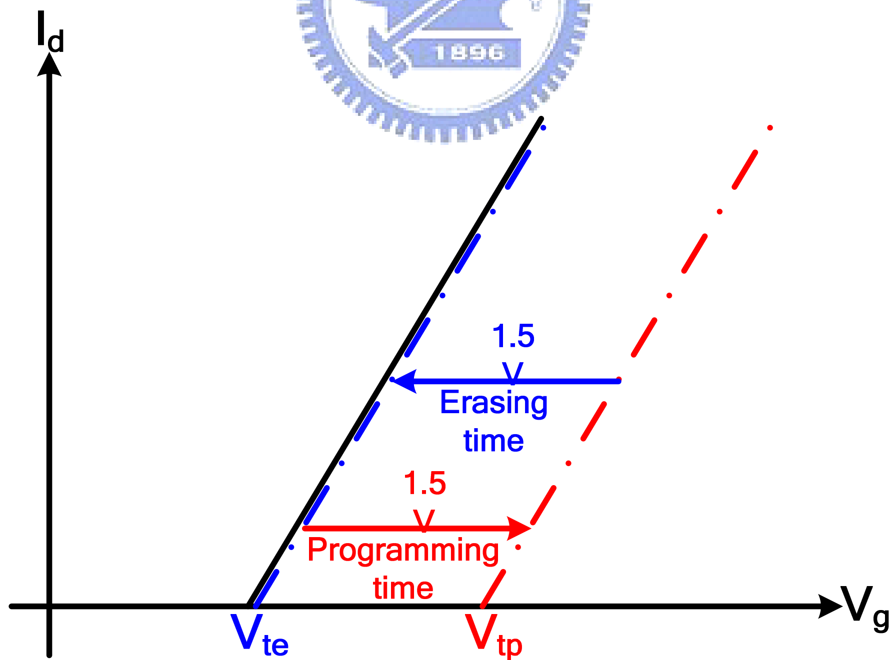


Fig. 3.2 The definition of programming/erasing time.

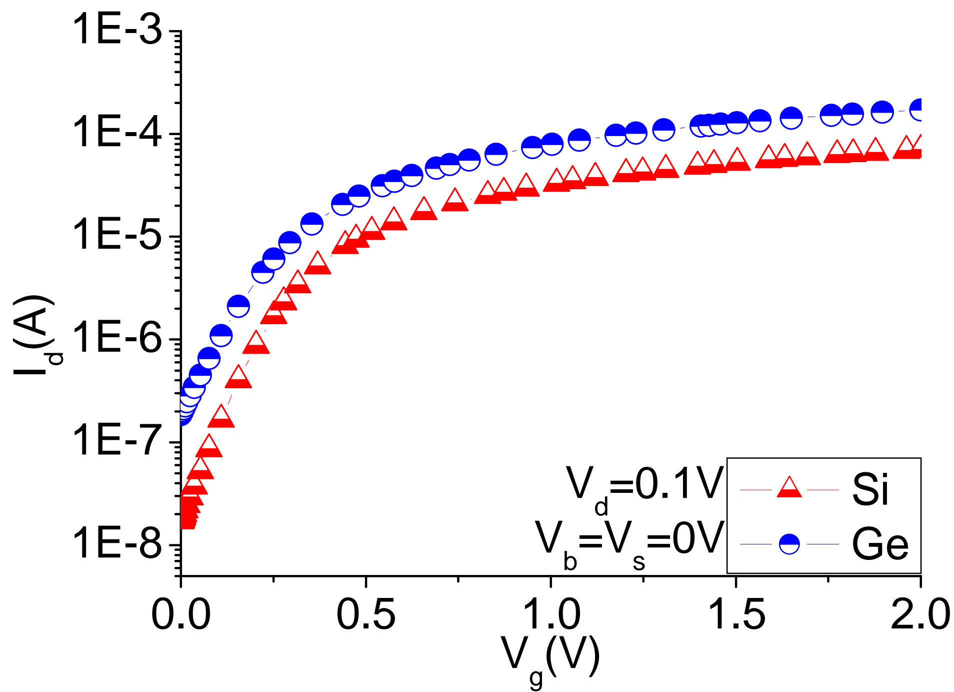


Fig. 3.3 Drain current as a function of gate voltage when the cell is operated in linear region.

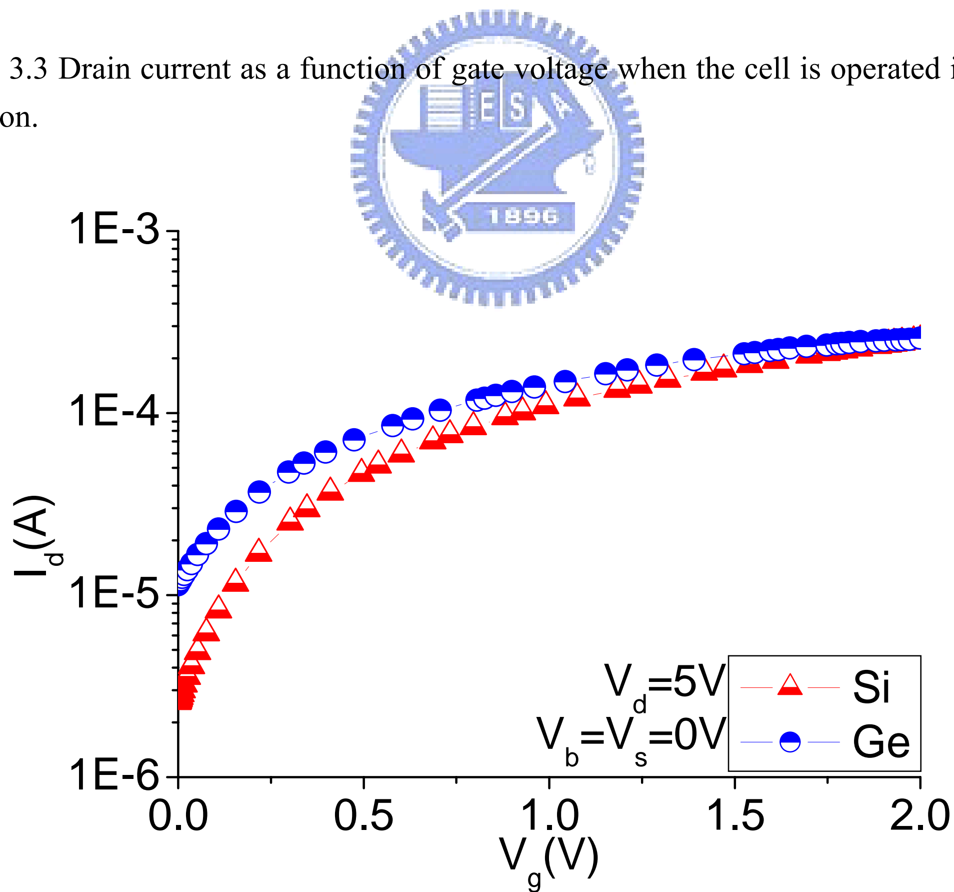


Fig. 3.4 Drain current as a function of gate voltage when the cell is operated in saturation region.

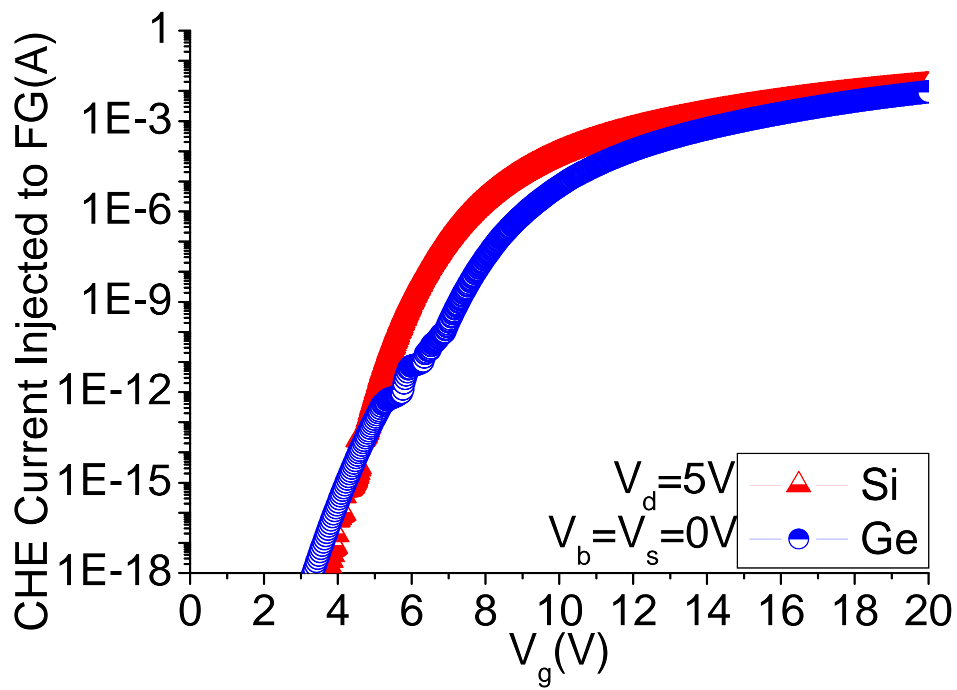


Fig. 3.5 CHE current injected to FG.

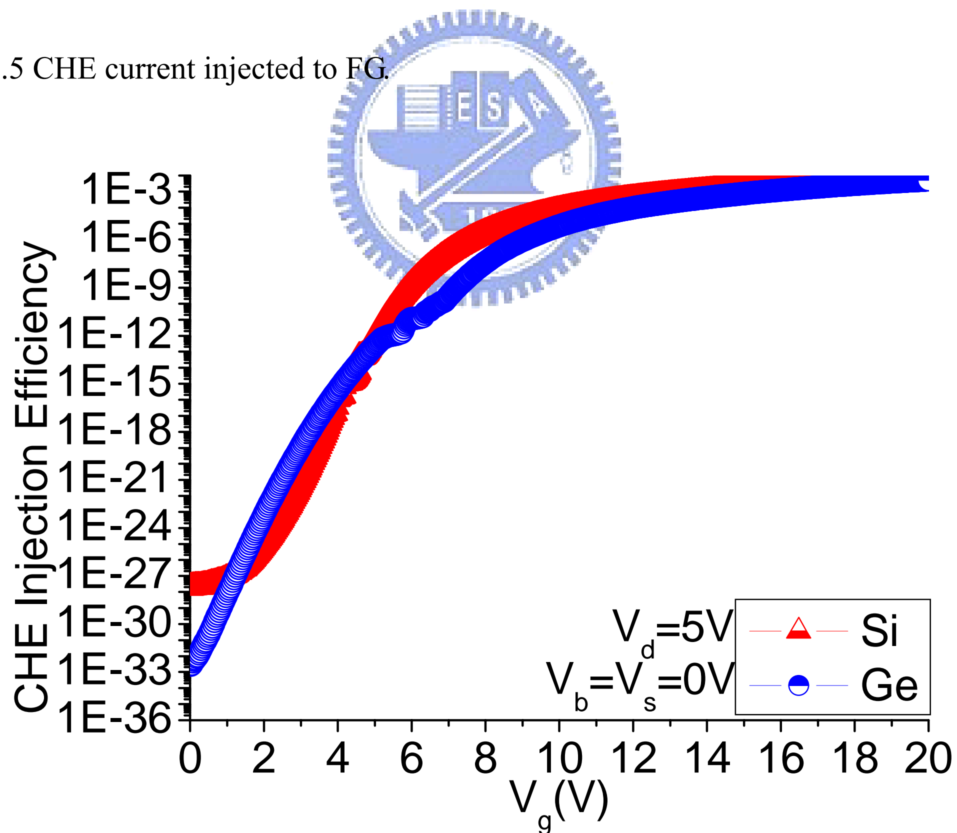
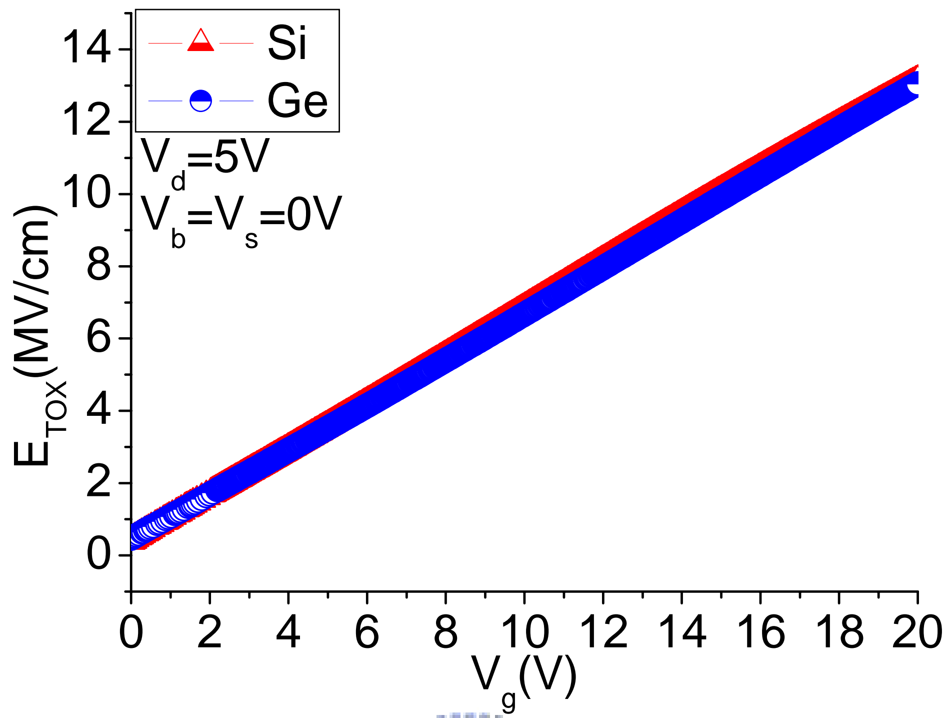
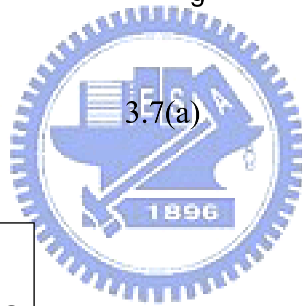
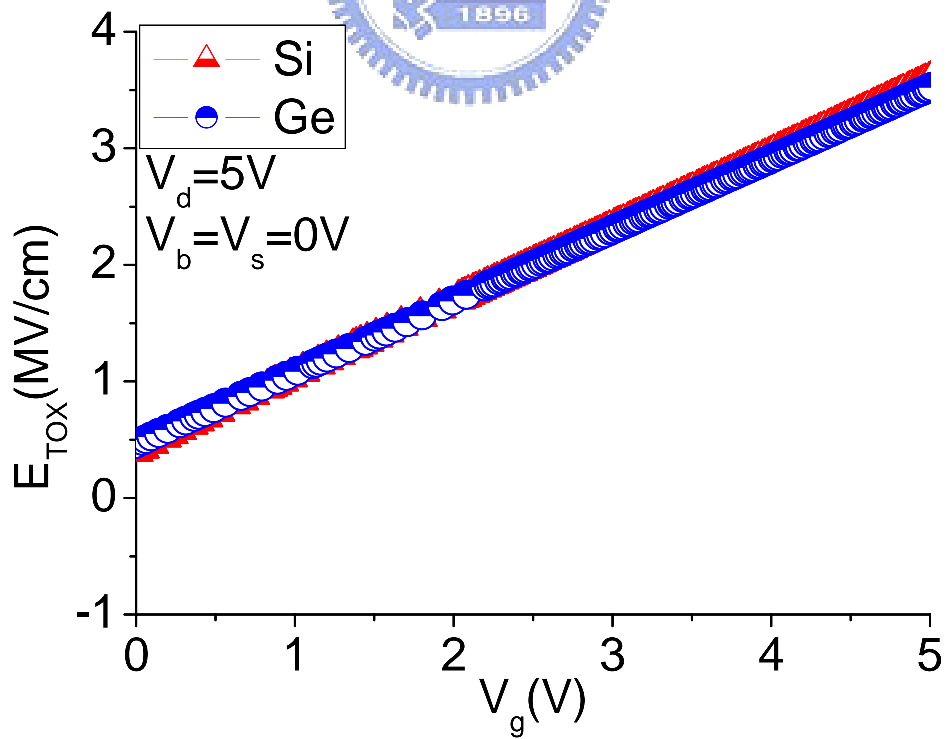


Fig. 3.6 CHE injection efficiency where the definition is $\frac{I_g}{I_d}$.

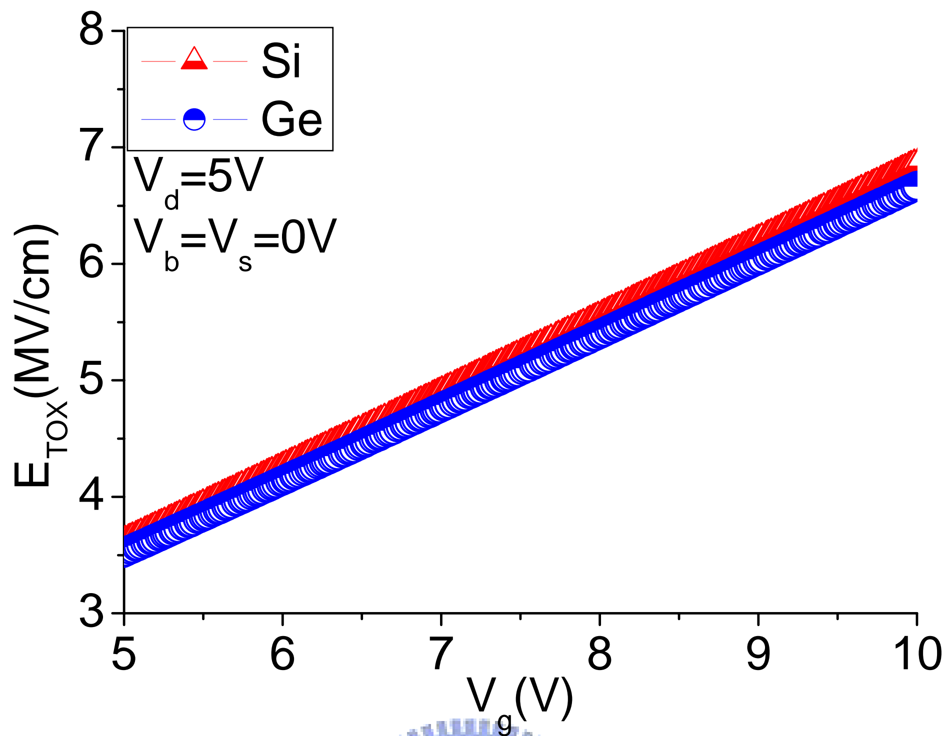


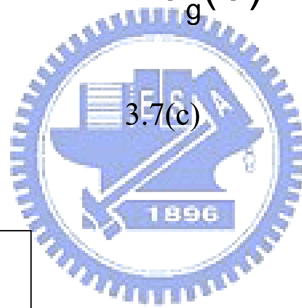


3.7(a)



3.7(b)





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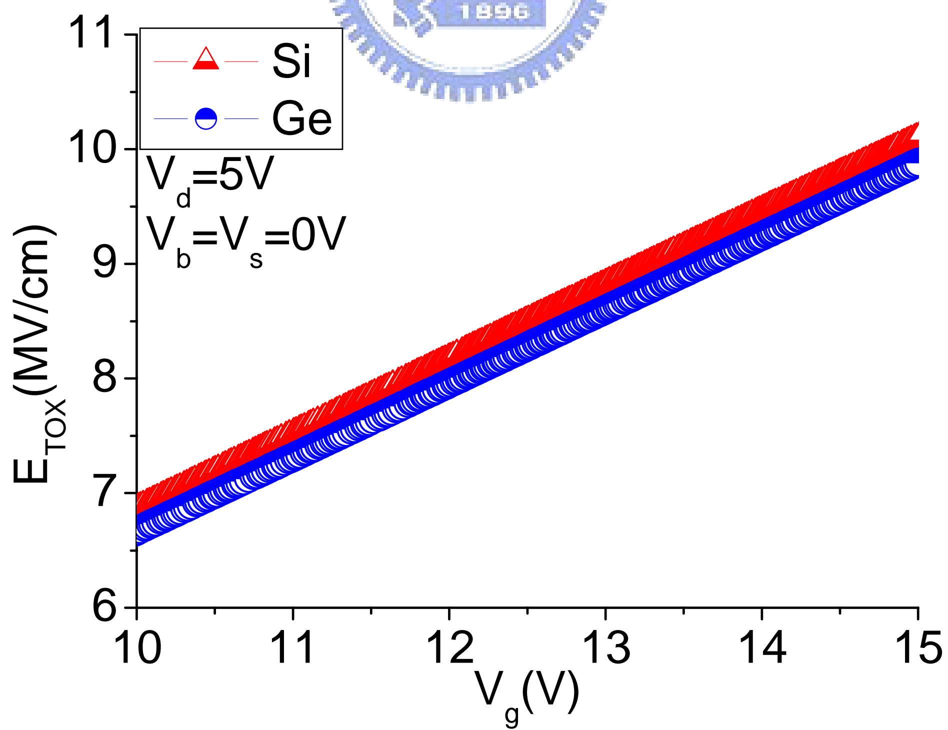

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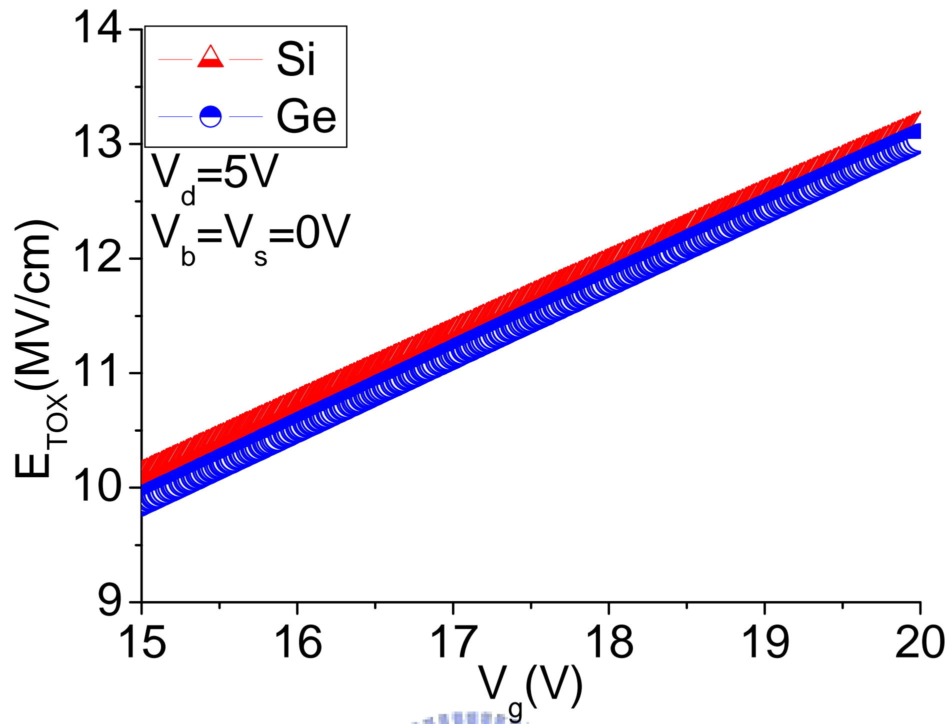
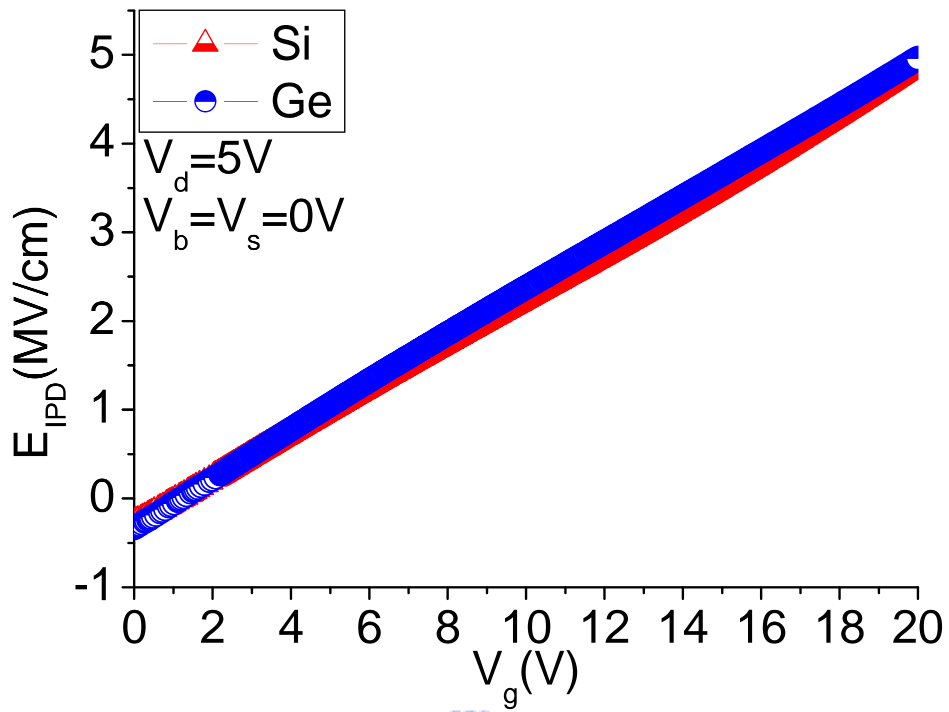
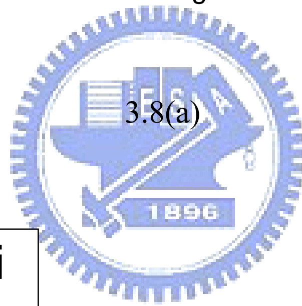


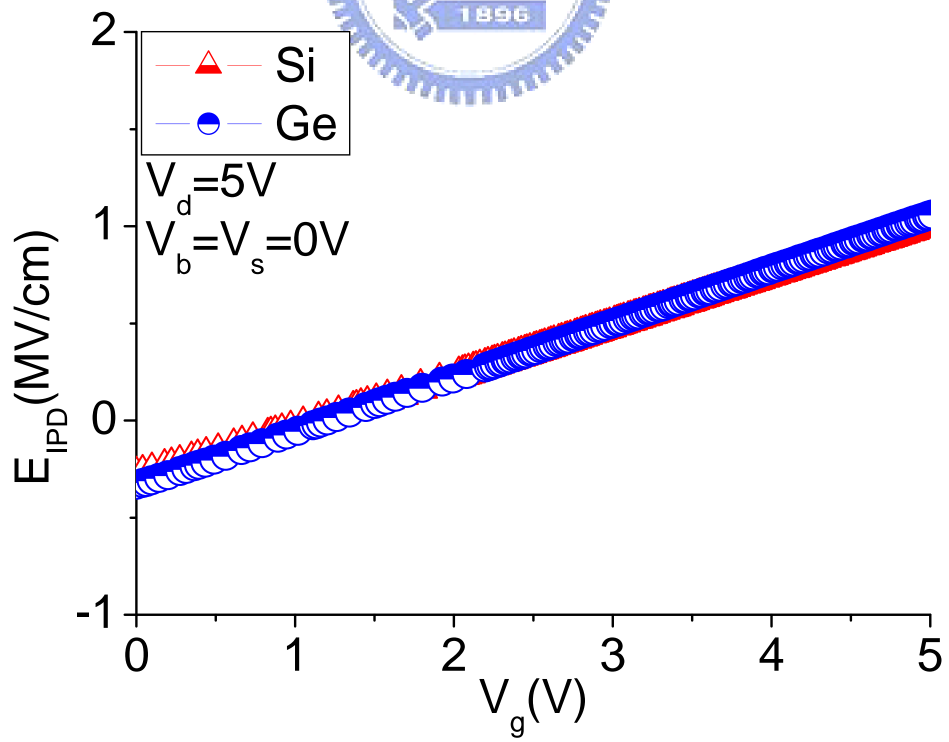
3.7(e)

Fig. 3.7 The electrical field of TOX on CHE programming: (a) V_g=0-20V (b) V_g=0-5V (c) V_g=5-10V (d) V_g=10-15V (e) V_g=15-20V.





3.8(a)



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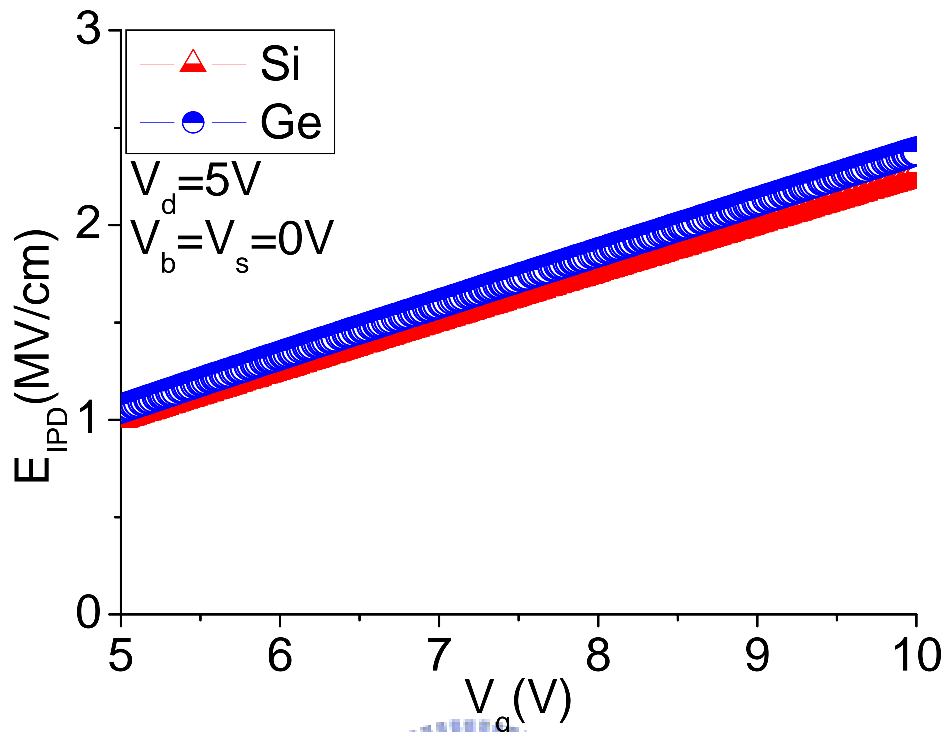

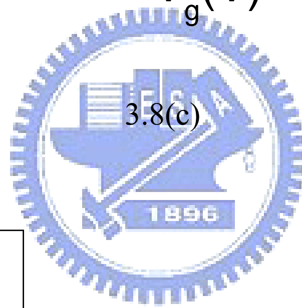

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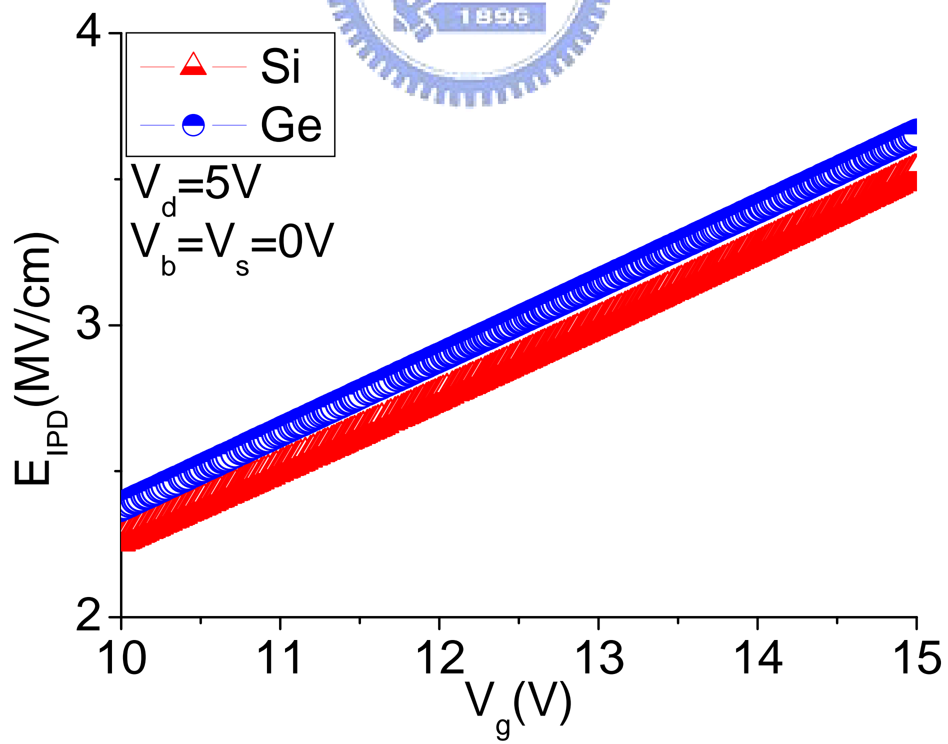
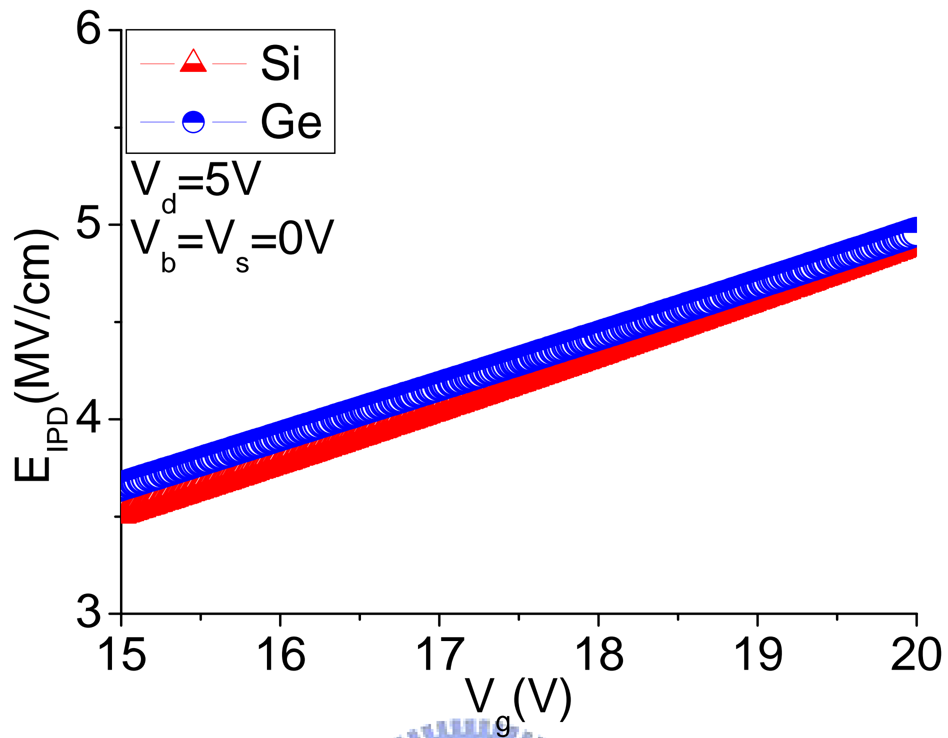


3.8(d)



3.8(e)

Fig. 3.8 The electrical field of IPD on CHE programming: (a) V_g=0-20V (b) V_g=0-5V (c) V_g=5-10V (d) V_g=10-15V (e) V_g=15-20V.

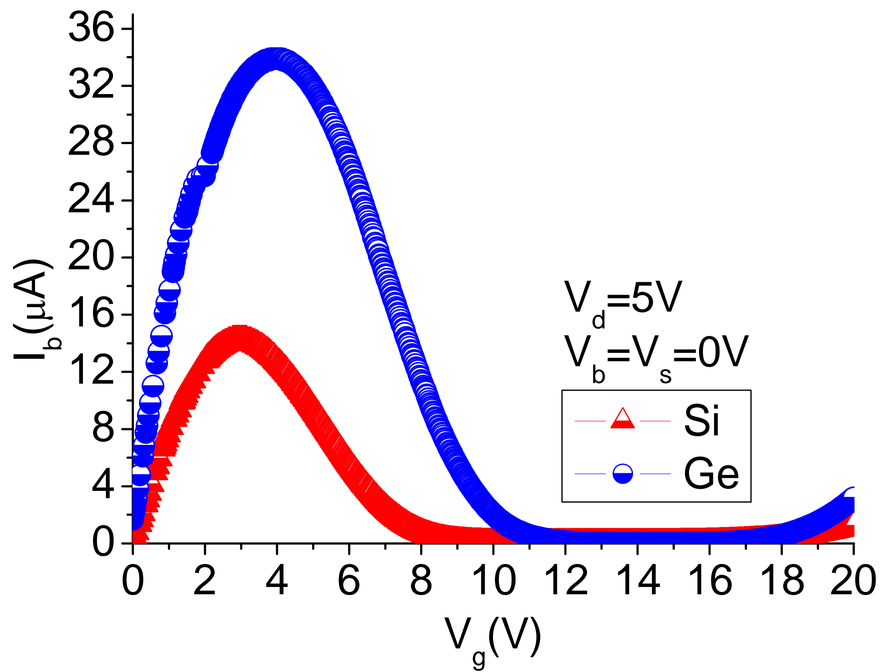


Fig. 3.9 Substrate current of stacked-gate Flash with Si and Ge substrate on CHE programming.

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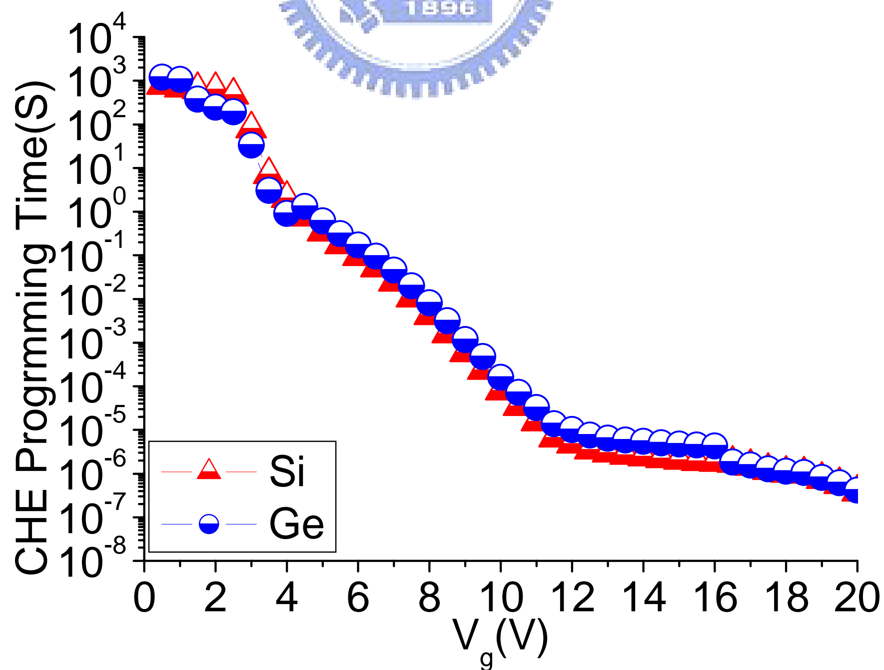
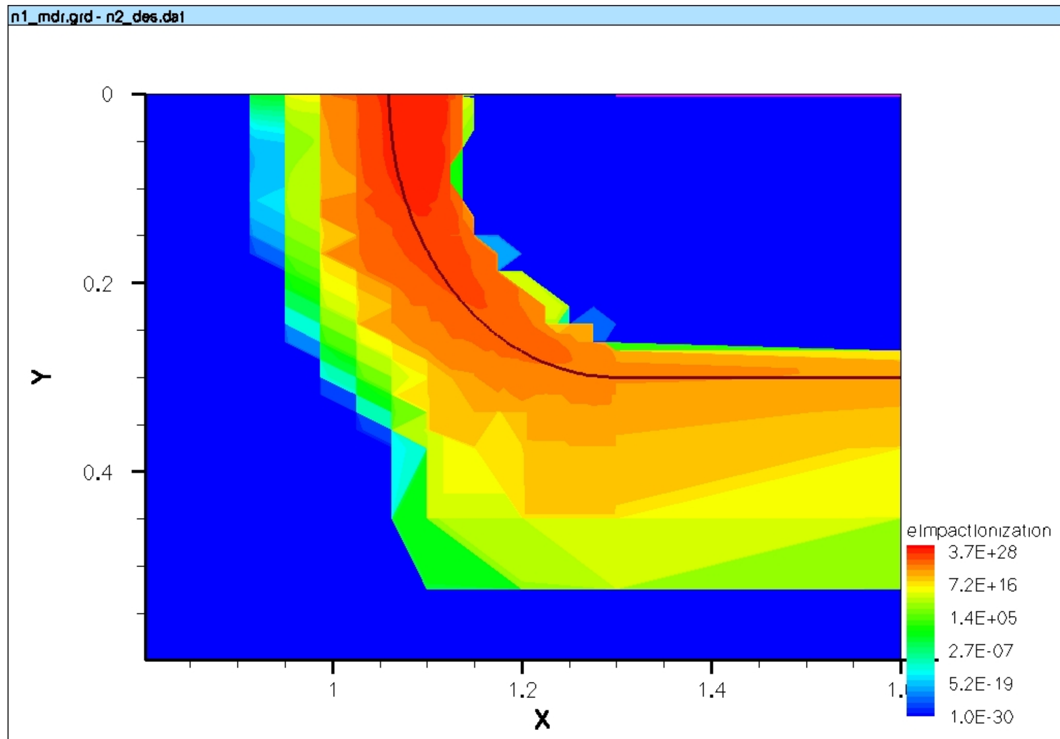
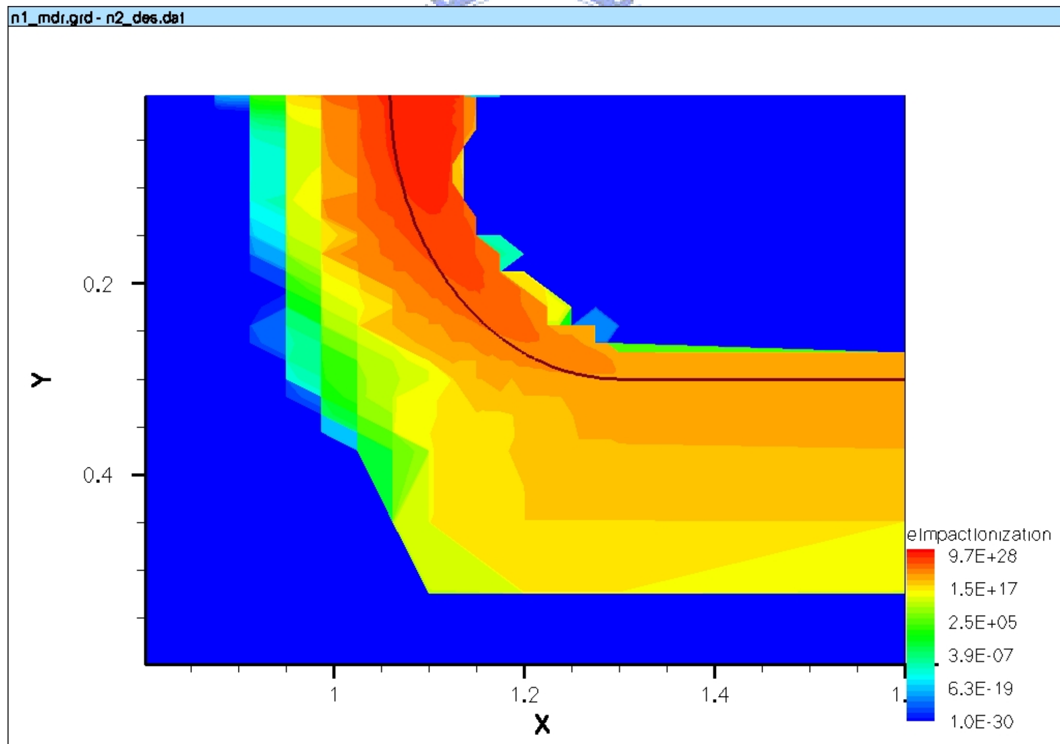


Fig. 3.10 CHE programming time as a function of CG voltage.

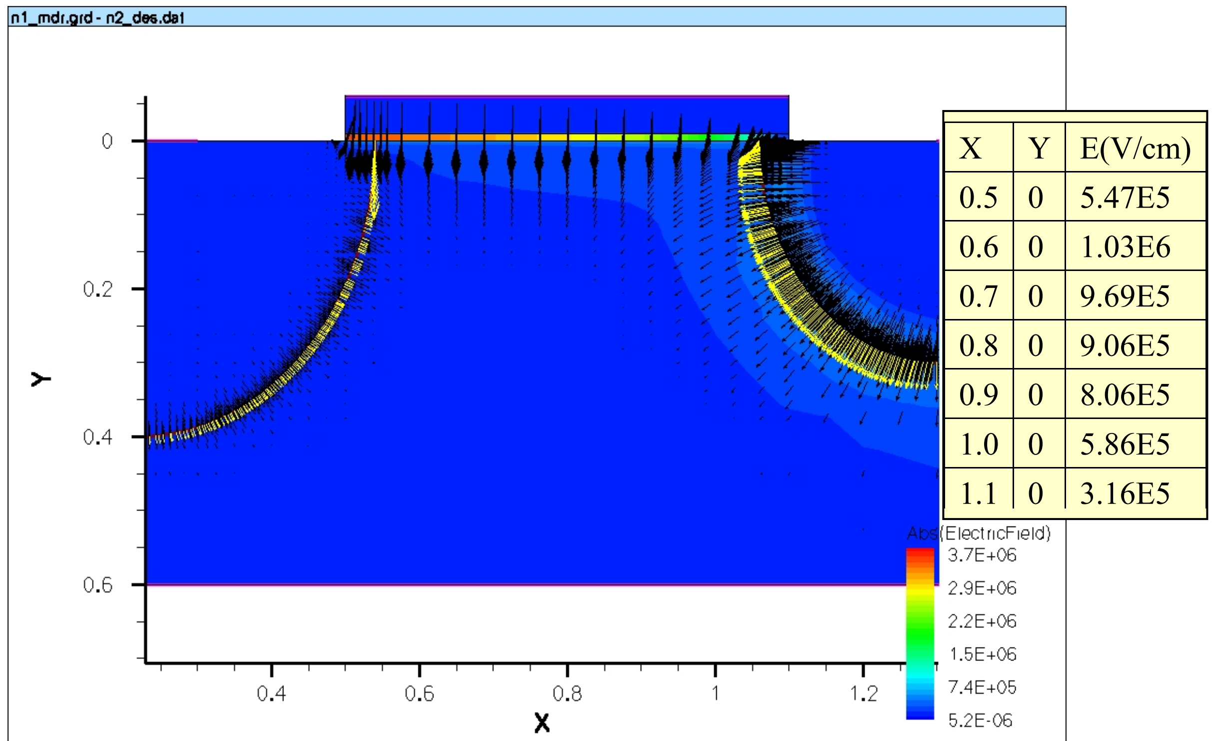


3.11(a)



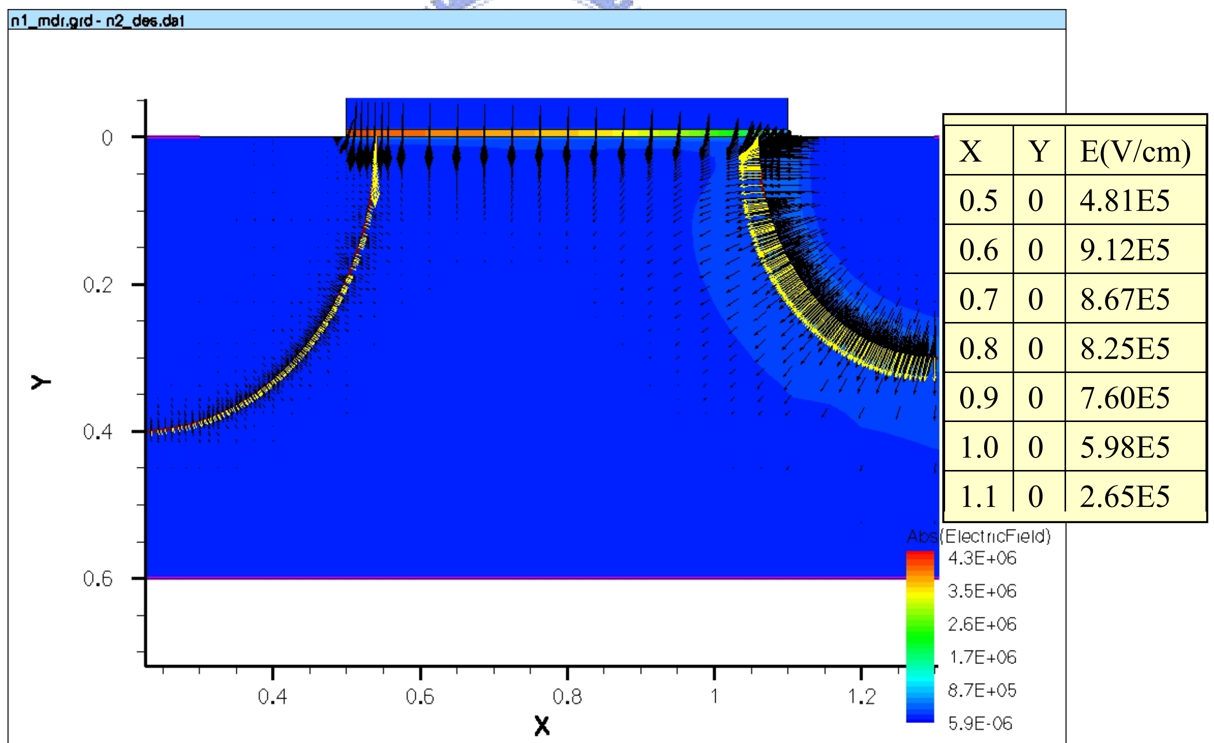
3.11(b)

Fig. 3.11 The value of impact ionization for (a) Si (b) Ge.



X	Y	E(V/cm)
0.5	0	5.47E5
0.6	0	1.03E6
0.7	0	9.69E5
0.8	0	9.06E5
0.9	0	8.06E5
1.0	0	5.86E5
1.1	0	3.16E5

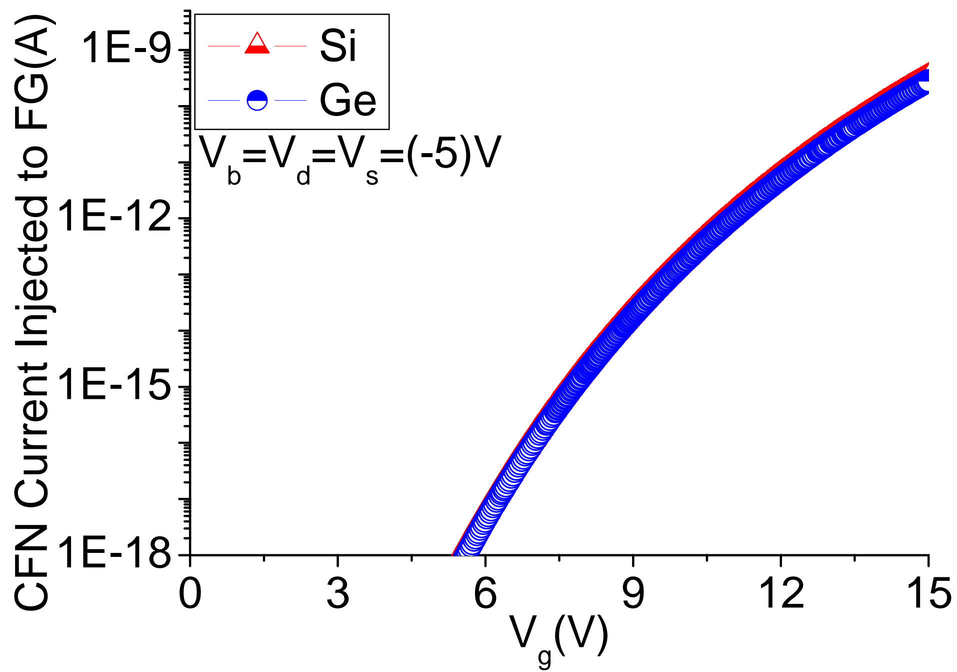
3.12(a)



X	Y	E(V/cm)
0.5	0	4.81E5
0.6	0	9.12E5
0.7	0	8.67E5
0.8	0	8.25E5
0.9	0	7.60E5
1.0	0	5.98E5
1.1	0	2.65E5

3.12(b)

Fig. 3.12 CHE programming electrical fields are shown as vector and probe some points of: (a) Si substrate (b) Ge substrate.



3.13(a)

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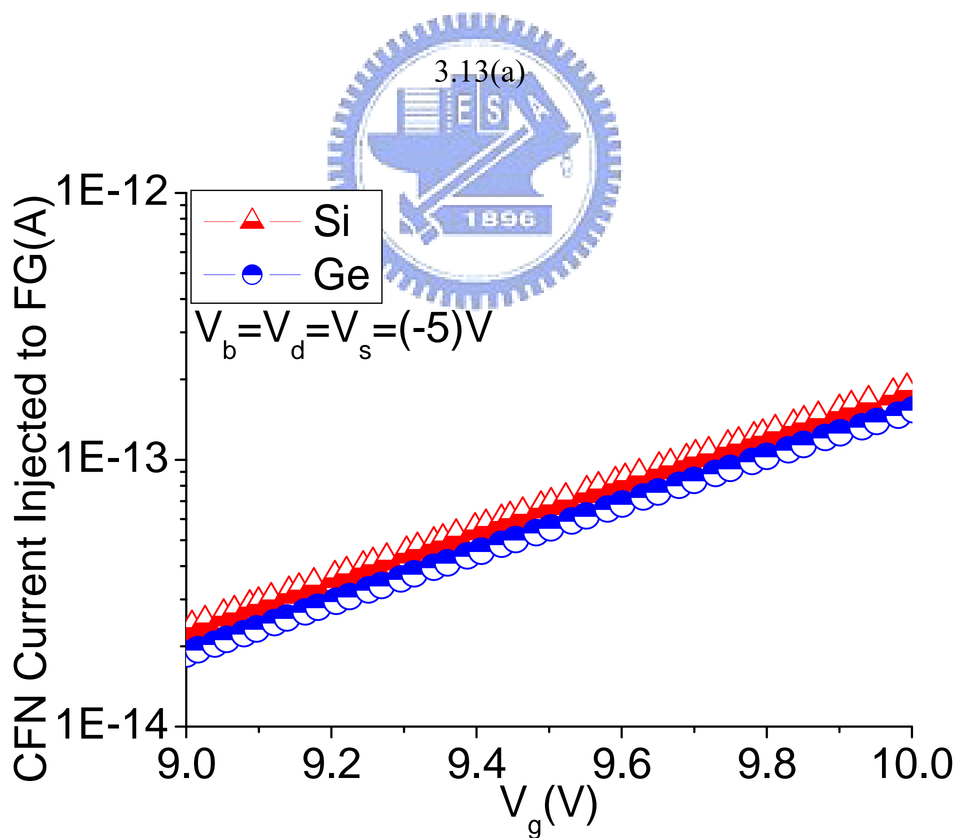
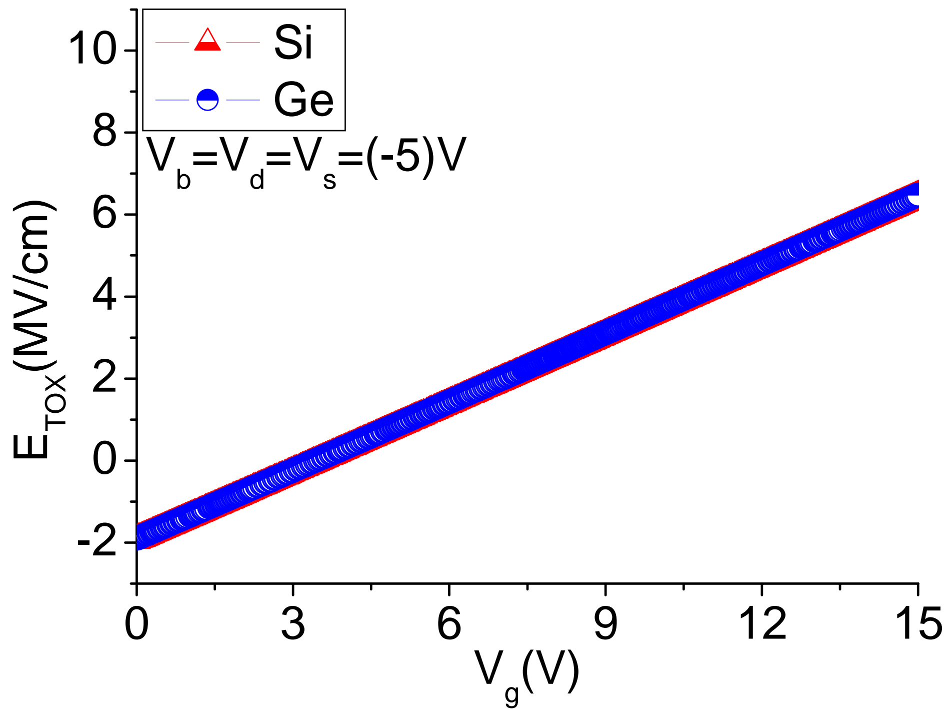
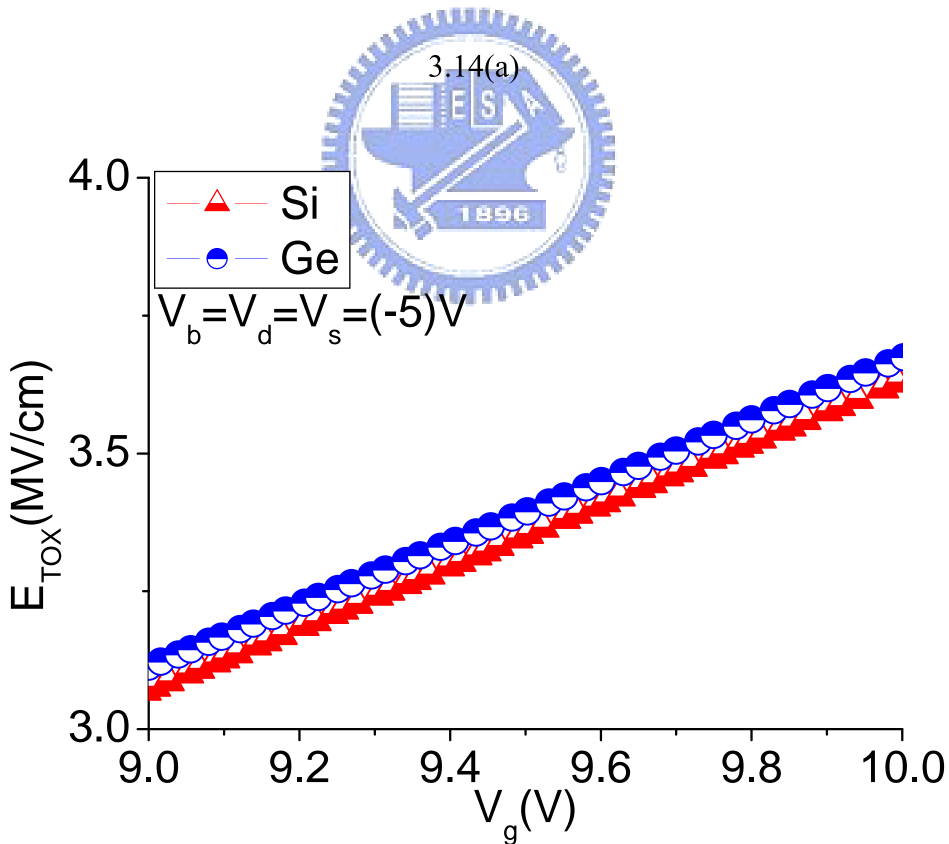


3.13(b)

Fig. 3.13 CFN current injected to FG: (a) V_g=0-20V (b) the zoom in of V_g=9-10V to show the difference between Si and Ge.

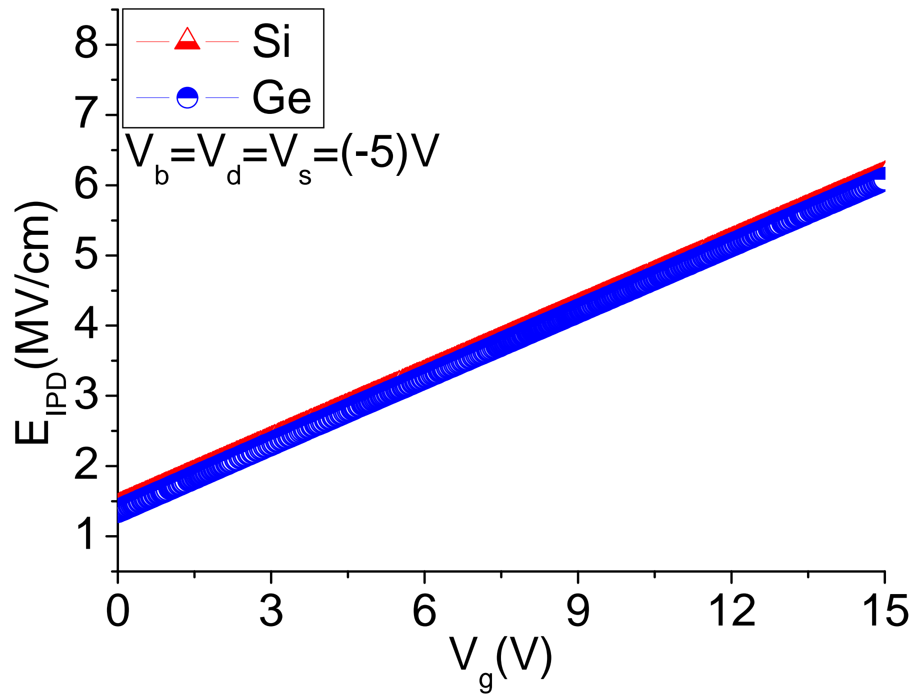


3.14(a)

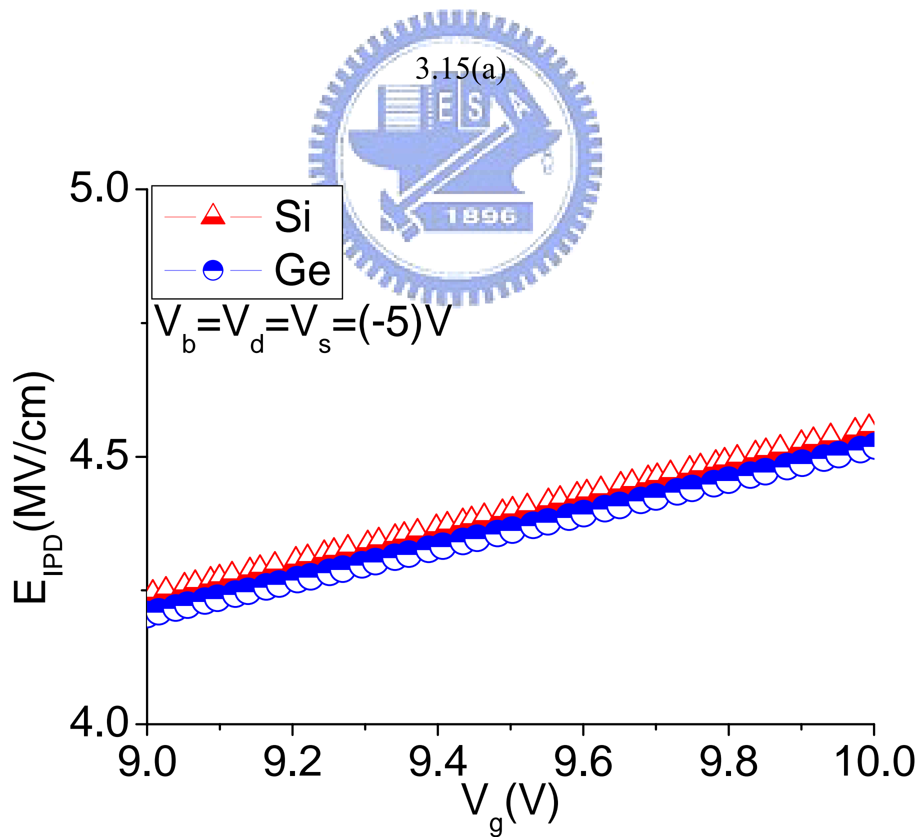


3.14(b)

Fig. 3.14 The electrical field of TOX on CFN programming: (a) V_g=0-20V (b) the zoom in of V_g=9-10V to show the difference between Si and Ge.



3.15(a)



3.15(b)

Fig. 3.15 The electrical field of IPD on CFN programming: (a) V_g=0-20V (b) the zoom in of V_g=9-10V to show the difference between Si and Ge.

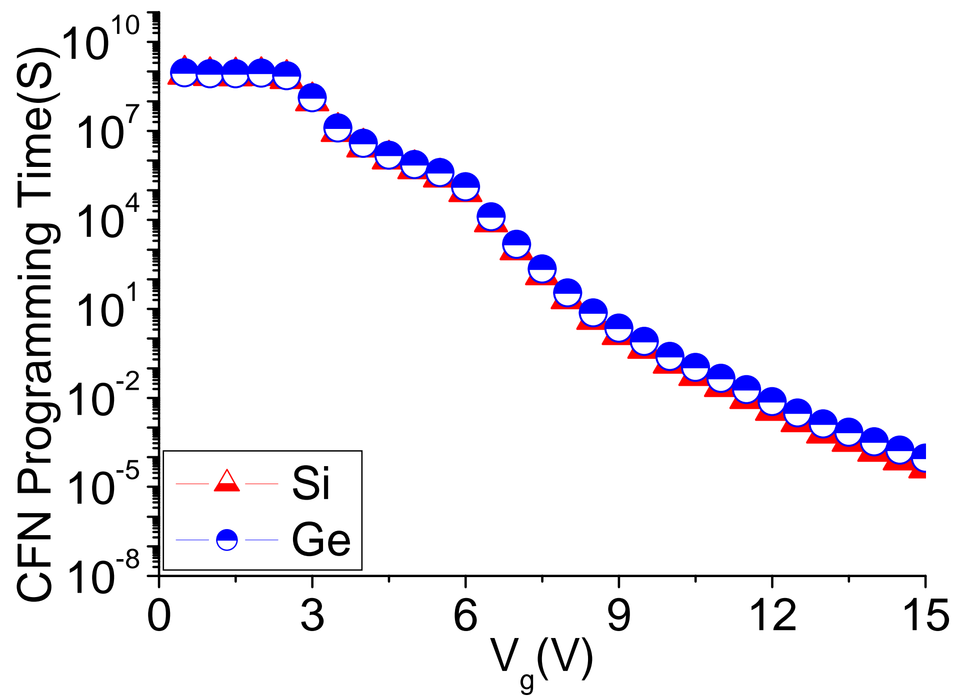
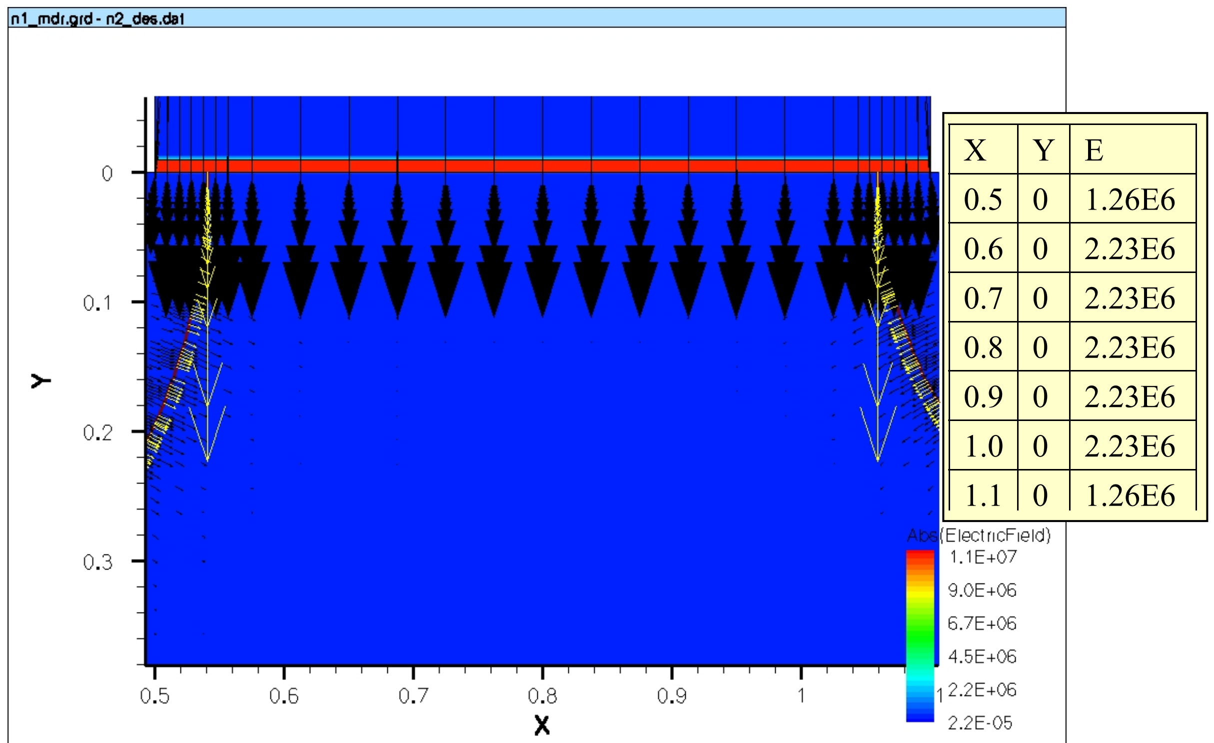
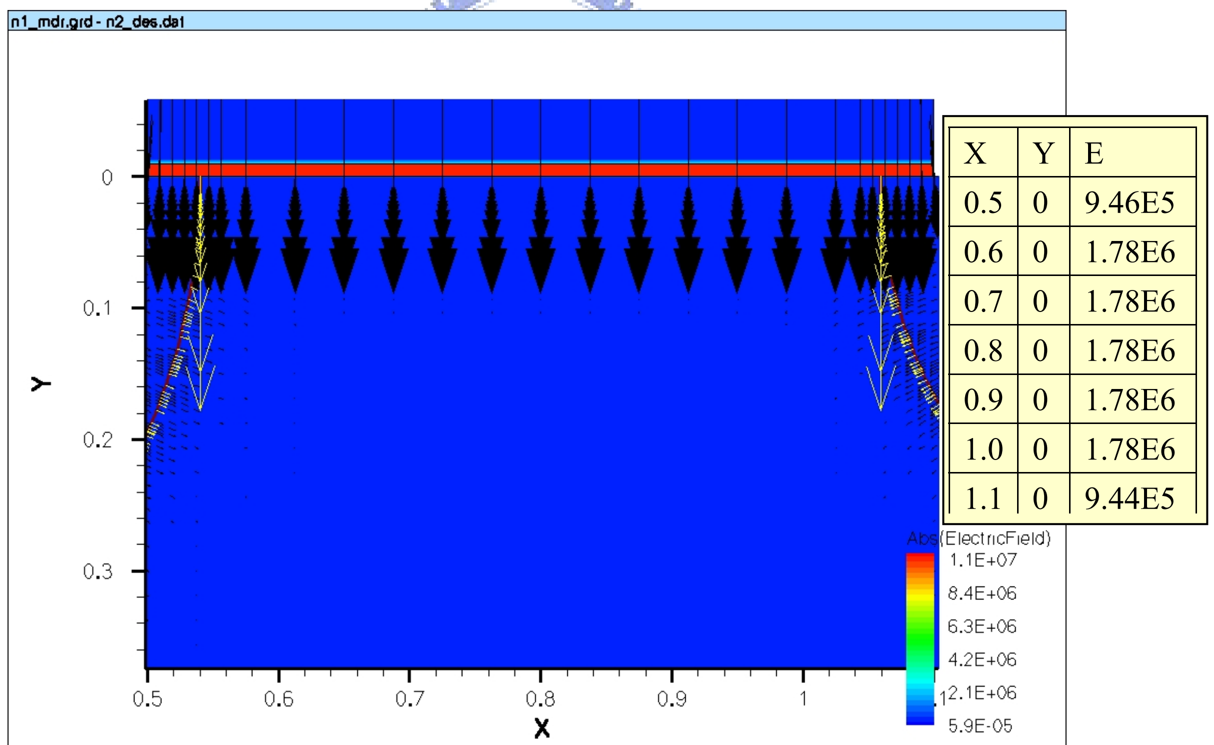


Fig. 3.16 CFN programming time as a function of CG voltage.



X	Y	E
0.5	0	1.26E6
0.6	0	2.23E6
0.7	0	2.23E6
0.8	0	2.23E6
0.9	0	2.23E6
1.0	0	2.23E6
1.1	0	1.26E6

3.17(a)



X	Y	E
0.5	0	9.46E5
0.6	0	1.78E6
0.7	0	1.78E6
0.8	0	1.78E6
0.9	0	1.78E6
1.0	0	1.78E6
1.1	0	9.44E5

3.17(b)

Fig. 3.17 CFN programming electrical fields are shown as vector and probe some points of: (a) Si substrate (b) Ge substrate.

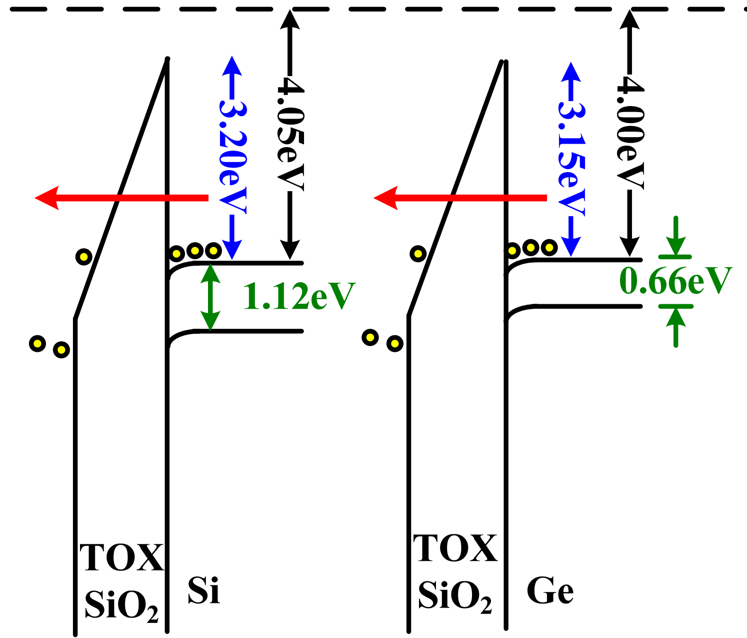


Fig. 3.18 The ϕ_b of Si and Ge.

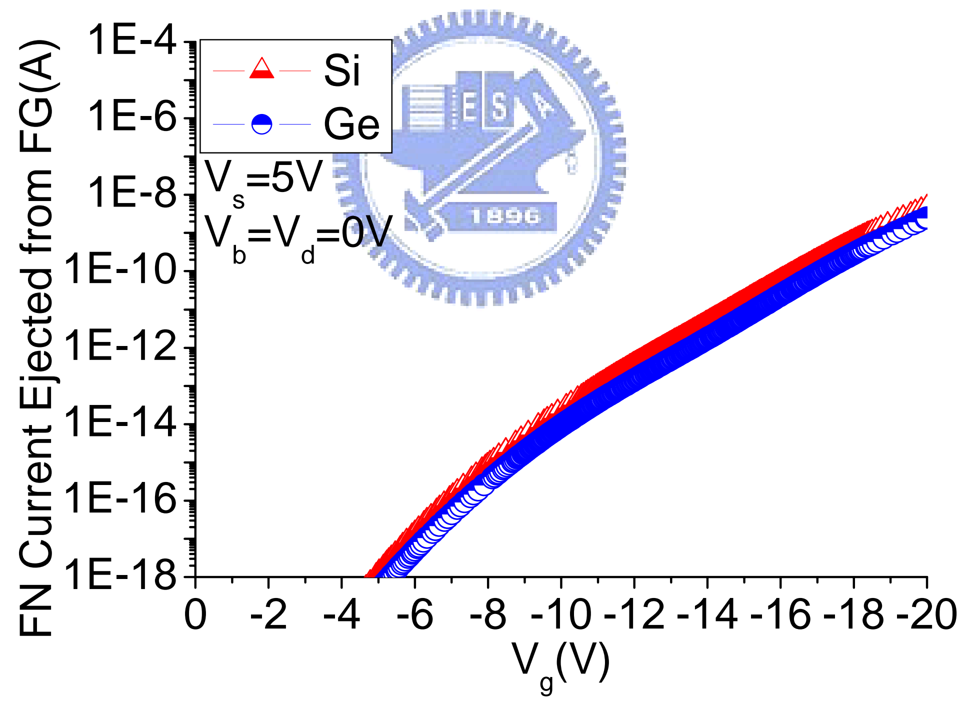


Fig. 3.19 CFN and SFN current ejected from FG.

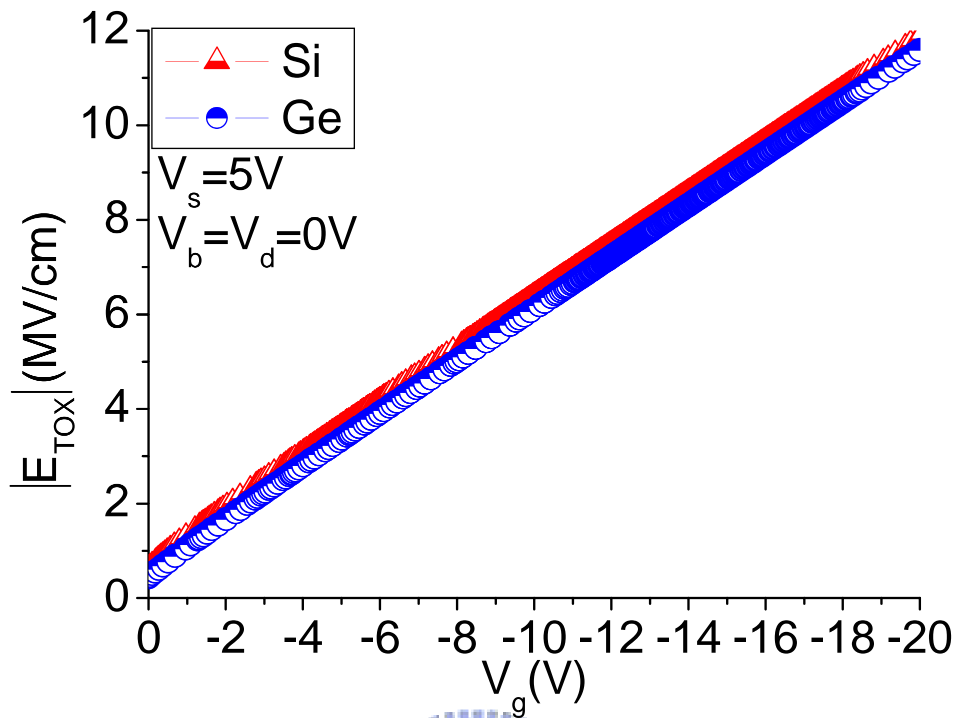


Fig. 3.20 The electrical field of TOX on CFN and SFN erasing.

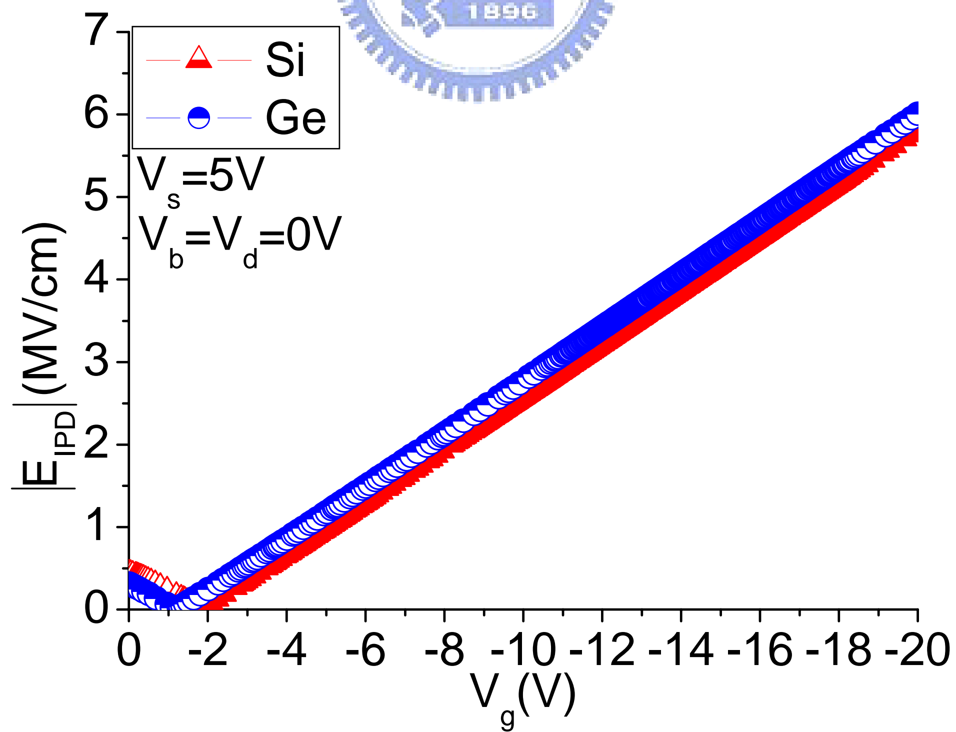


Fig. 3.21 The electrical field of IPD on CFN and SFN erasing.

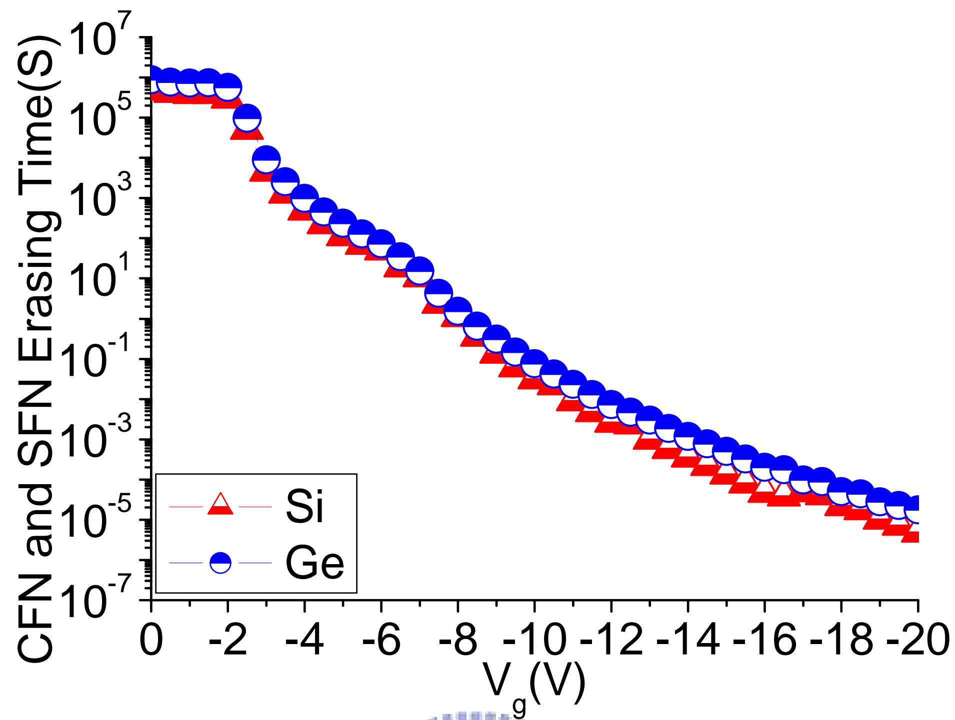
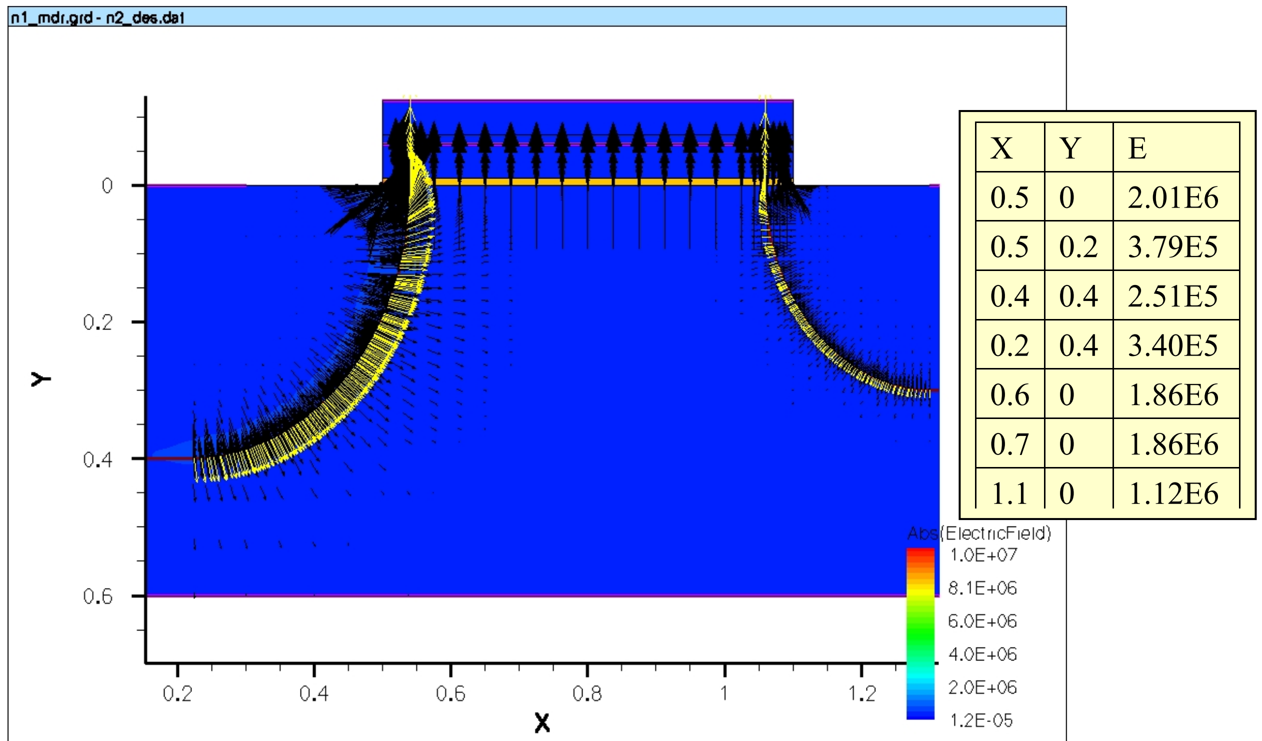
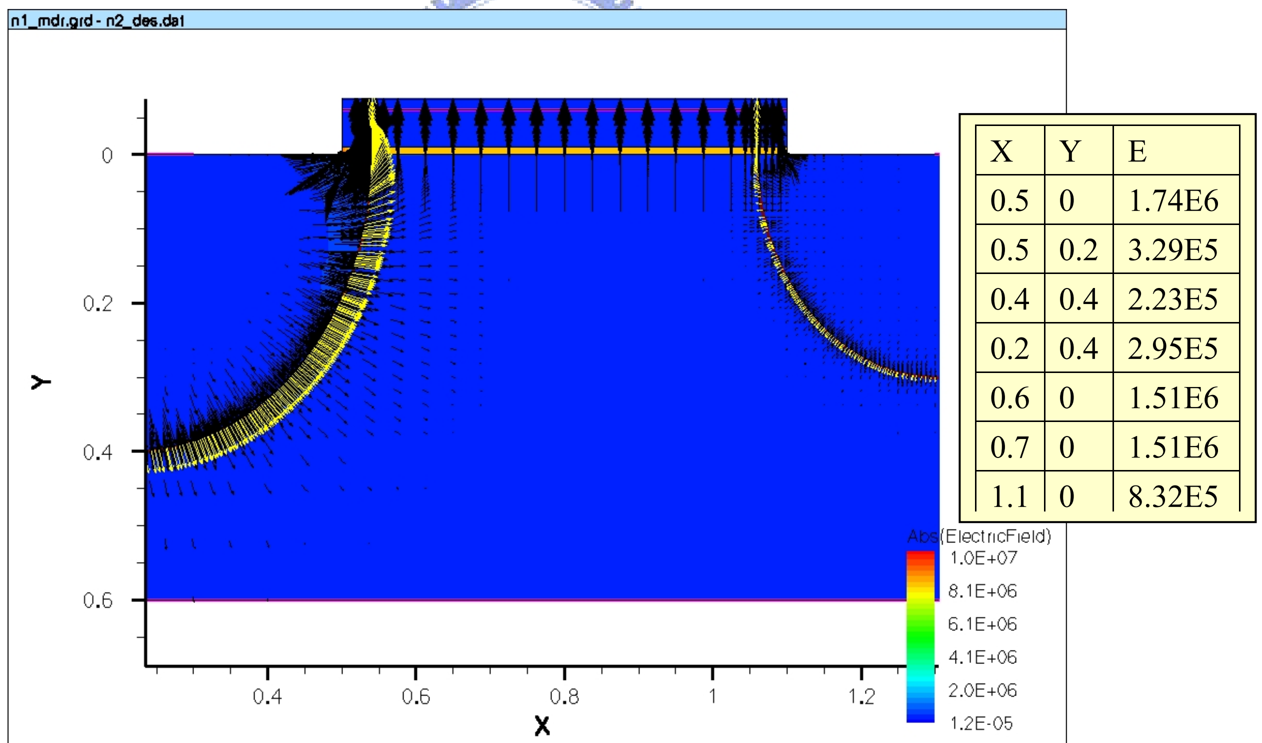


Fig. 3.22 CFN and SFN erasing time as a function of CG voltage.



X	Y	E
0.5	0	2.01E6
0.5	0.2	3.79E5
0.4	0.4	2.51E5
0.2	0.4	3.40E5
0.6	0	1.86E6
0.7	0	1.86E6
1.1	0	1.12E6

3.23(a)



X	Y	E
0.5	0	1.74E6
0.5	0.2	3.29E5
0.4	0.4	2.23E5
0.2	0.4	2.95E5
0.6	0	1.51E6
0.7	0	1.51E6
1.1	0	8.32E5

3.23(b)

Fig. 3.23 CFN and SFN erasing electrical fields are shown as vector and probe some points of: (a) Si substrate (b) Ge substrate.

	V_b	V_s	V_d	V_g
CHE program	0V	5V	0V	0-20V
CFN program	(-5)V	(-5)V	(-5)V	0-15V
CFN and SFN erase	5V	0V	0V	0-(-20)V

Tab. 3.1 The operating voltage of electrodes for programming/erasing.

	C_{IPD}	C_{TOX}	C_S	C_D	C_T
silicon	1.480fF	2.070fF	0.197fF	0.187fF	3.934fF
germanium	1.480fF	2.181fF	0.239fF	0.223fF	4.123fF

Tab. 3.2 The capacitances between the FG and other electrodes.

	α_g	α_b	α_d	α_s
silicon	0.376	0.526	0.047	0.050
germanium	0.359	0.529	0.054	0.058

Tab. 3.3 The coupling ratios for (2-20).

	CFN programming
silicon	$E_{inj}=\dfrac{V_{app}+0.9678V+\dfrac{Q'_{ss}}{2.070fF}}{100\mathring{A}}$
Germanium	$E_{inj}=\dfrac{V_{app}+0.5459V+\dfrac{Q'_{ss}}{2.181fF}}{100\mathring{A}}$

Tab. 3.4 Electrical field at injection surface for CFN programming of Si and Ge substrate Flash.

	CFN erasing
silicon	$$E_{inj}=\frac{V_{app}+\frac{1\times10^{-15}C}{C_{n^{+}-poly-gate}}+0.9678+\frac{Q'_{ss}}{2.070fF}}{100\mathring{A}}$$
Germanium	$$E_{inj}=\frac{V_{app}+\frac{1\times10^{-15}C}{C_{n^{+}-poly-gate}}+0.5459+\frac{Q'_{ss}}{2.181fF}}{100\mathring{A}}$$

Tab. 3.5 Electrical field at injection surface for CFN erasing of Si and Ge substrate Flash.