CHAPTER 4

Conclusions and Recommendations for Future Works

4.1 Conclusions

In chapter 2, we display all the used physical parameters, mathematical parameters, and equations for our simulations. We just simulate the Flash devices in room temperature (300K) and general conditions, not for special cases. The models and mechanisms would differ and need to change for satisfying user intention. The simulation tool (ISE) uses the silicon (Si) parameters as default, and we have changed them for germanium (Ge) in our best effort. However, there are some models and parameters are instituted by experimental fitting, that's remaining as future works of realizing the Ge substrate Flash memories. Because of this reason, it is necessary to find the A and χ in (2-26). The two parameters are determined by fitting gate currents measured on transistors obtained by shorting the floating-gate (FG) and control-gate (CG) of Flash cells [2.12]. In our simulations, we just use the default Si A and χ for Ge and want to check the influences which caused by the physical differences between Si and Ge.

In chapter 3, we display the simulate results of Si and Ge substrate Flash memories. If we treat the Flash memories as conventional gate MOSFET, the higher drive-in current both in linear and saturation region are shown. The higher coupling ratio of drain in Ge would cause the drain turn-on and the higher off current. The trade-off between speed and power consumption may need new structures or new materials to satisfy the urgent requirement of tunneling oxide (TOX) thickness scaling down.

On channel hot electrons (CHE) injection programming, the gate current

differences between Si and Ge results from the effective electrical field. For higher coupling ratio of α_g in Si, the higher electrical field across the TOX is shown. Also because of the continuity of the displacement vector, the higher permittivity Ge would cause the lower electrical strength at the semiconductor-oxide interface. The barrier of Si-oxide and Ge-oxide is a parameter of tunneling current, but the difference is less than 2% of Ge-oxide barrier. The higher gate current (speed) and smaller programming time of Si substrate Flash memory are shown. We also see the high operating voltage is needed for CHE programming to meet the typical 10μs programming time (about 11~12V).

On channel Fowler-Nordheim (CFN) programming, the E_{inj} is the key role of tunneling current. The electrical field of TOX for Ge is larger than Si, that caused by the higher C_T when the four electrodes are biased and supplying the coupling voltage of FG. However, according to Tab. 3.4 and simulate results, the CFN programming current of Si is larger than Ge. The voltage of satisfying 10μs programming time is about 15V, larger than CHE programming.

On CFN and source F-N (SFN) erasing, the CG coupling voltage is dominant for FG voltage and causing higher electrical field across TOX in Si than Ge. The mechanism of F-N tunneling shown in Tab. 3.5 tells the higher gate current of Si substrate Flash. The need of voltage for typical erasing time is about 11V.

In spite of programming or erasing, the Ge substrate Flash memories wouldn't show the expected results that thinking over the smaller effective mass and more serious hot carriers injection for Ge. The interface electrical field seems to be critical of gate current mechanisms, and the continuity of the displacement vector shows the disadvantage of Ge's high permittivity.

4.2 Recommendations for Future Works

1. Realize the Ge substrate stacked-gate Flash memories and find the fitting parameters for CHE tunneling in [2.12], and confirm the Q'_{ss} for Ge comparing to Si of F-N tunneling mechanism.
2. The overlaps of Si/Ge and stack-gate affect the coupling ratios, we would find the influence.
3. We want to know the influence that if the bulk Si/Ge substrate is changed to Si-on-insulator (SOI)/Ge-on-insulator (GOI).
4. The Flash modeling is a worthy part for researching, if the devices of Si and Ge substrate Flash memories are realized.
5. Implanting Ge into Si bulk substrate near the most serious impact ionization region and detects the changing of gate current.