References

[1.1] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, "Introduction to flash memory", *Proceedings of the IEEE*, vol. 91, no. 4, p. 489, Apr. 2003.

[1.2] B. McClean, B. Matas, and T. Yancey, *The McClean Report: 2001 Edition, IC Insights*, 2001.

[1.3] K. Kahng and S. M. Sze, "A floating gate and its application to memory devices", *IEEE Transactions on Electron Devices*, vol. 14, no. 9, p. 629, Sep. 1967.

[1.4] T. Trexler, "Flash memory complexity", *IEEE Instrumentation & Measurement Magazine*, vol. 8, no. 1, p. 22, Mar. 2005.

[1.5] J. D. Blauwe, "Nanocrystal nonvolatile memory devices", *IEEE Transactions on Nanotechnology*, vol. 1, no. 1, p. 72, Mar. 2002.

[1.6] S. Tiwari, F. Rana, K. Chan, H. Hanafi, Chan Wei, and D. Buchanan, "Volatile and non-volatile memories in silicon with nano-crystal storage", *International Electron Devices Meeting*, p. 521, Dec. 1995.

[1.7] J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, and Y. Lee, "Room temperature operation of a quantum-dot flash memory", *IEEE Electron Device Letters*, vol. 18, no. 6, p. 278, Jun. 1997.

[1.8] Y. C. King, T. J. K, and C. Hu, "MOS memory ustin germanium nanocrystals formed by thermal oxidation of $Si_{1-x}Ge_x$", *International Electron Devices Meeting*, p. 115, Dec. 1998.

[1.9] W. D. Brown and J. E. Brewer, "Nonvolatile semiconductor memory technology", *IEEE Press Series on Microelectronic Systems*, p. 590, Oct. 1997.

[1.10] M. H. White, Y. Yang, A. Purwar, and M. L. French, "A low voltage SONOS nonvolatile semiconductor memory technology", *IEEE Transactions on Components*

Packaging and Manufacturing Technology, vol. 20, no. 2, p. 190, Jun. 1997.

[1.11] Y. Y. Chen, “Investigation of nitrided oxides and high-k dielectrics on MOS devices and Flash memories”, *NCTU doctoral dissertation*, 2005.

References

[2.1] J. R. Chelikowsky and M. L. Cohen, "Nonlocal pseudopotential calculations for the electronic structure of eleven diamond and zinc-blende semiconductors", *Physical Review B 14*, p. 556, Feb. 1976.

[2.2] S. M. Sze, *Physics of Semiconductor Devices*, New York: Wiley, 1969.

[2.3] C. D. Thurmond, "Standard thermodynamic functions for the formation of electrons and holes in Ge, Si, GaAs and GaP", *Journal of the Electrochemical Society*, vol. 122, no.8, p. 1133, Aug. 1975.

[2.4] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices", *IEEE Transactions on CAD*, vol. 7, no. 11, p. 1164, Nov. 1988.

[2.5] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature", *IEEE Transaction on Electron Devices*, vol. 22, no. 11, p. 1045, Nov. 1975.

[2.6] A. G. Chynoweth, "Ionization Rates for Electrons and Holes in Silicon", *Physical Review 109*, no. 5, p. 1537, Mar. 1958.

[2.7] W. Shockley, "Problems related to p-n junctions in silicon", *Czechoslovak Journal of Physics*, vol. 11, no. 2, p. 81, 1961.

[2.8] P. A. Wolff, "Theory of multiplication in silicon and germanium", *Physical Review 95*, no. 6, p. 1415, Sep. 1945.

[2.9] G. A. Baraff, "Distribution functions and ionization rates for hot electrons in semiconductors", *Physical Review 128*, no. 6, p. 2507, Dec. 1962.

[2.10] Y. Okuto and C. R. Crowell, "Threshold energy effect on avalanche breakdown

voltage in semiconductor junctions", *Solid-State Electronics*, vol. 18, p. 161, Feb. 1975.

[2.11] C. J Glassbrenner and G. A. Slack, "Thermal conductivity of silicon and germanium form 3K to the melting point", *Physical Review 134*, no. 4A, A1058, May 1964.

[2.12] C. Fiegna, F. Venturi, M. Melanotte, E. Sangiorigi, and B. Ricco, "Simple and efficient modeling of EPROM writing, "*IEEE Transactions on Electron Device*, vol. 38, no. 3, p. 603, Mar. 1991.

個人簡歷

姓名 ： 謝致維

性別 ： 男

出生年月日 ： 民國 70 年 3 月 26 日

籍貫 ： 台灣省台東縣

住址 ： 台東縣池上鄉忠孝路 212 號

學歷 ：

國立中山大學電機工程學系學士 (88.9－93.6)

國立交通大學電子工程研究所碩士 (93.9－95.7)

碩士論文題目 ：

基板材料對於堆疊式快閃記憶體寫入/抹除效率的影響

Effects of Substrate Materials on the Programming/Erasing Efficiency of Stacked-Gate Flash Memories