國立交通大學

電子工程學系 電子研究所

碩士論文

低溫複晶矽薄膜電晶體之負偏壓溫度不穩定研究

The Study of Negative Bias Temperature Instability in Low Temperature Polycrystalline Silicon Thin-Film Transistors

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低溫複晶矽薄膜電晶體之負偏壓溫度不穩定研究

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摘　要

在本論文中，首先，我們提出負偏壓溫度不穩定對於低溫複晶矽薄膜電晶體的可靠度有不可忽視的影響，並且證明在負偏壓溫度不穩定的情況下，低溫負晶矽薄膜電晶體的裂化跟捕陷能階(trap state)的增加有關。實驗結果顯示，臨界電壓(threshold voltage)的增加跟晶粒邊界捕陷能階(grain boundary trap state)的增加有密切的關係，這兩者隨著時間的變化量有相似的次方律(power law)，此外也都與閘極電壓、溫度呈指數關係。負偏壓溫度不穩定同時也會降低驅動電流、載子遷移率和次臨界擺幅(subthreshold swing)。

接著，我們討論複晶矽薄膜電晶體在負偏壓溫度不穩定的情況下，離子傷害(plasma damage)對其可靠度的影響，實驗結果顯示較大的天線面積會造成較嚴重的傷害。在負偏壓溫度不穩定的量測下，離子傷害會降低元件的驅動電流、載

子遷移率和次臨界擺幅。

最後，我們探討有關複晶矽薄膜電晶體在負偏壓溫度不穩定和熱載子注入(hot carrier injection)兩種不同情況下的可靠度，在小的汲極電壓下，元件的裂化主要由負偏壓溫度不穩定所控制，當汲極電壓增加，元件的裂化會變成熱載子注入的所導致，然而溫度上升也會使元件有較嚴重的裂化，最後我們分別探討負偏壓溫度不穩定以及熱載子注入的模型，而此模型也和實驗結果相吻合。

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ABSTRACT

In this thesis, first, We proved negative bias temperature instability (NBTI) is an important reliability issue in low temperature polycrystalline silicon thin film transistors (LTPS TFTs), and demonstrated the degradation of LTPS TFTs under NBTI stress is closely related to trap state creation. Measurements revealed the threshold voltage shift is highly correlated to the generation grain boundary trap states. Both the two physical quantities follow almost the same power law dependence on stress time; moreover, exponential dependence on the stress voltage and reciprocal of the ambient temperature. In addition to the threshold voltage shift, NBTI also leads to the degradation of subthreshold swing, driving current and hole mobility. By analyzing thoroughly, we concluded the degradation is caused by hydrogen

depassivation, leading to the generation of fixed oxide charges, interface states and grain boundary trap states.

Then, the impact of plasma damage on NBTI in LTPS TFTs is explored. The experimental results confirm that LTPS TFTs with larger antenna degrade more than those with smaller antenna. Plasma damage is demonstrated to enhance the device degradation in carrier mobility, threshold voltage and drive current under NBTI stress. The enhanced device degradation is mainly attributed to accelerated generation rate of interface states, grain boundary trap states and fixed oxide charges.

Finally, we investigated degradation mechanism of LTPS TFTs upon NBTI stress and hot carrier injection (HCI) stress . Under fixed stress gate voltage (V_{GS}), the dependent of device degradation on the stress drain voltage (V_{DS}) was analyzed. At low V_{DS}, the device degradation shows to be dominated by NBTI stress; at high V_{DS}, NBTI is retarded and HCI stress dominates the degradation. The degradation is enhanced at elevated stress temperature regardless of the V_{DS}. This is due to the fact that NBTI and hot hole injection can be thermally enhanced at elevated temperature, leading to severe device degradation. To quantify the combined NBTI and HCI stress induced degradation, we proposed a modified model based on the empirical NBTI and HCI stress models, and the experimental results conformed to the model. Therefore, we can clearly identify the combined NBTI and HCI stress effects on p-channel LTPS TFTs.

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謝謝你們的支持與鼓勵，僅以此論文獻給你們。

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Introduction

1.1 Overview of Negative Bias Temperature Instability

Negative bias temperature instability (NBTI) occurs in p-channel MOS device stressed negative gate voltage at elevated temperature. Typical stress temperatures lie in the 100-250°C range. Either negative gate voltage or elevated temperatures can produce NBTI, but a stronger and faster effect is produced by their combined action. It occurs primarily in p-channel MOSFETs with negative gate voltage bias and appears to be negligible for positive gate voltage and for either positive and negative gate voltage in n-channel MOSFETs [1]. In MOS circuits, it occurs most commonly during the "high" state of p-channel MOSFETs inverter operation.

NBTI has been known since the very early days of MOS device development, having been observed as early as 1967 [2]. Deal named it Instability Number VI [3]. Goetz Berger et al. at Bell Labs were one of the first groups to show detailed characterization of negative bias, temperature stress [4]. They used metal gate devices on 100nm oxides, stressed at -10^6V/cm at 300°C and found an interface trap density D_{it} in the lower half of the band gap. The higher the starting D_{it}, the higher the final stress-induced $D_{it.}$ For positive gate voltage, they noted a very small D_{it} increase. D_{it} increased with gate voltage and with time with a time dependence of $t^{0.25}$. D_{it} (T=300°C) > D_{it} (T=250°C) and p-type substrates gave higher D_{it} than n-type substrate.

The interfaces trap density induced by NBTI increases with decreasing oxide thickness, whereas the fixed oxide charge density induced by NBTI appears to have no thickness dependence. This t_{ox}^{-1} dependence of interface-trap generation implies that NBTI becomes more severe for ultra-thin oxides.

1.2 Overview of Poly-Si Thin-Film Transistors

In 1966, the first polycrystalline silicon thin film transistors (Poly-Si TFTs) were fabricated by C. H. Fa *et al.* [5]. So far, numerous research reports have been proposed to study the conduction mechanism, fabrication processes and device structures of the poly-Si TFTs in order to enhance the device performance. However, the research in poly-Si TFTs fabrication with temperature below 600°C was not commenced until 1980s. In the past twenty years, low-temperature polysilicon (LTPS) TFTs have been widely investigated in industrial applications, such as active-matrix liquid-crystal displays (AMLCDs) [6-8], high density static random access memories (SRAMs) [9], electrical erasable programming read only memories (EEPROM) [10][11] and candidate for 3-D ICs' applications [12], etc. Within those applications, the application of active-matrix liquid-crystal displays (AMLCDs) is the major driving force to promote the developments of poly-Si TFT technology.

It is known that hydrogenated amorphous silicon (α-Si:H) TFTs were used for the pixel switching device at the first generation of AMLCDs. The advantages of α-Si:H TFTs are their compatibility with low processing temperature on large-area glass substrates and high off-stated impedance which result in a low leakage current. However, its low electron field effect mobility typically below 1 $cm^2V^{-1}sec^{-1}$ has limited the development for AMLCDs technology. So, poly-Si TFTs have attracted much attention, because the field effect mobility in poly-Si is significantly higher than that in α-Si, thus higher driving current can be achieved in poly-Si [13]. The higher driving current allows small-dimensioned TFTs to be used as the pixel switching elements, thus promoting the aperture ratio and the panel brightness, and therefore improving the performance of display.

The conduction mechanism and the performance of poly-Si TFTs are strongly related to grain boundaries and intracranial defects. For example, the defects in grain boundary would trap carriers and generate a potential barrier which degrades the on-stated current of poly-Si TFTs. Moreover, the grain boundaries also provide the path of leakage current. In order to obtain desirable electrical characteristics of poly-Si TFTs, several methods have been proposed to improve the device performance by enlarging the grain size of poly-Si films [14] and reducing the trap states in grain boundaries. It has been reported that the α-Si films can be crystallized by several techniques, such as SPC (solid-phase crystallization) [15], ELA (excimer laser annealing) [16] [17] and MILC (metal-induced lateral crystallization) [18] to obtain a large grain size of poly-Si to raise the field effect mobility. Additionally, there were other methods such as plasma treatments to passivate the defects in the channel or narrowing the channel width to reduce the trap state density. We will make a discussion in next section.

1.3 Motivation

In p-channel MOSFETs, NBTI has been found to be an important reliability problem and has been widely investigated. It has been reported the degradation of NBTI in MOSFETs is mainly due to the generation of interface states and fixed oxide charges, and NBTI can be thermally and electrically activated[19]-[22]. In poly-Si TFTs, due to poor thermal conductivity of the glass substrate and high operation voltage, NBTI must be the important issue in the reliability of poly-Si TFTs. However, NBTI is still not thoroughly studied in poly-Si TFTs and the mechanism is not well known. In addition, the degradation mechanism of NBTI stress in poly-Si TFTs, due to the grain boundaries in the channel region, may be different from MOSFETs. So, we will study the instabilities and mechanisms of p-channel LTPS TFTs upon NBTI stress.

Moreover, plasma process has been widely used in the manufacture of ULSI and LTPS TFTs. In PMOSFETs, NBTI has been widely studied and found to be an important reliability issue [23] [24]. Additionally, it has been reported that plasma damage leads to severe NBTI in PMOSFETs [25]-[28]. In TFTs, several researchers have showed NBTI occurs as well as in PMOSFETs [29] [30]. However, the correlation between plasma damage and NBTI in LTPS TFTs has not been explored. The purpose of the third chapter is to investigate the effect of plasma damage on the NBTI behaviors in LTPS TFTs.

In the fourth chapter, we will discuss the degradation between NBTI and hot carrier injection (HCI) stress. As we know, LTPS TFTs are now widely investigated for their potential application in AMLCDs and realization of system on panel (SOP). For the LTPS TFTs to be used in advanced analog and mixed signal circuit, the electrical stability becomes an important issue. To determine maximum threshold voltage (V_{th}) shift in an analog circuit over its operating lifetime, several factors, such as operating gate and drain voltage, that influence the conventional DC lifetime need to be considered. Therefore, this study aims at the device degradation mechanism under NBTI and HCI. Besides, a modified model will propose to explain the degradation mechanism.

1.4 Method of Device Parameter Extraction

In this thesis, all of the electrical characteristics of proposed poly-Si TFTs were measured by HP 4156B-Precision Semiconductor Parameter Analyzer.

Many methods have been proposed to extract the characteristic parameters of poly-Si TFTs. In this section, those methods are described.

1.4.1 Determination of Threshold Voltage

Threshold voltage (V_{th}) is an important parameter required for the channel length-width and series resistance measurements. However, V_{th} is not uniquely defined. Various definitions have been proposed and the reason can be found in I_D-V_{GS} curves. One of the most common techniques is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of 50~100mV to ensure operation in the linear region [31]. The drain current is not zero when V_{GS} below threshold voltage and approaches zero asymptotically. Hence the I_{DS} versus V_{GS} curve can be extrapolated to $I_D=0$, and the V_{th} is determined from the extrapolated intercept of gate voltage (V_{GSi}) by

$$V_{th} = V_{GSi} - \frac{V_{DS}}{2} \quad \text{-- (Eq. 1.1)}$$

Equation (1.1) is strictly only valid for negligible series resistance. Fortunately series resistance is usually negligible at the low drain current when threshold voltage measurements are made. The I_{DS}-V_{GS} curve deviates from a straight line at gate voltage below V_{th} due to subthreshold current and above V_{th} due to series resistance and mobility degradation effects. It is common practice to find the point of maximum slope of the I_{DS}-V_{GS} curve and fit a straight line to extrapolate to $I_D=0$ by means of finding the point of maximum of transconductance (Gm).

In this thesis, we use a simpler method to determinate the V_{th} called constant drain current method. The voltage at a specified threshold drain current is taken as the V_{th}. This method is adopted in the most studied papers of poly-Si TFTs. It can be given a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current is specified at (W/L)×10nA for $V_{DS}=0.1V$ and (W/L)×100nA for $V_{DS}=5V$, where W and L are channel width and channel length, respectively.

1.4.2 Determination of Subthreshold Swing

Subthreshold swing (S.S.) is a typical parameter to describe the control ability of gate toward channel, which reflects the turn on/off speed of a device. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude.

The S.S. should be independent of drain voltage and gate voltage. However, in reality, the S.S. increases with drain voltage due to channel shortening effect such as charge sharing, avalanche multiplication and punchthrough effect. The subthreshold swing is also related to gate voltage due to undesirable and inevitable factors such as the serial resistance and interface states.

In this thesis, the S.S. is defined as one-third of the gate voltage required to decrease the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

1.4.3 Determination of Field Effect Mobility

Usually, field effect mobility (μ_{eff}) is determined from the maximum value of transconductance (Gm) at low drain bias. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so that the first order of I-V relation in the bulk Si MOSFETs can be applied to poly-Si TFTs. The drain current in linear region ($V_{DS} < V_{GS} - V_{th}$) can be approximated as the following equation:

$$I_{DS} = \mu_{eff} C_{ox} \left(\frac{W}{L} \right) \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^{\ 2} \right] \quad \text{-------------------------- (Eq. 1.2)}$$

where W and L are channel width and channel length, respectively. C_{ox} is the gate oxide capacitance per unit area and V_{th} is the threshold voltage. Thus, the transconductance is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{eff} C_{ox} \left(\frac{W}{L} \right) V_{DS} \quad \text{-- (Eq. 1.3)}$$

Therefore, the field-effect mobility is

$$\mu_{eff} = \frac{L}{C_{ox} W V_{DS}} g_{m(\max)} \Big|_{V_{DS} \to 0} \quad \text{-- (Eq.1.4)}$$

1.4.4 Determination of ON/OFF Current Ratio

On/off current ratio is one of the most important parameters of poly-Si TFTs since a high-performance device exhibits not only a large on-current but also a small off-current (leakage current). The leakage current mechanism in poly-Si TFTs is not like that in MOSFET. In MOSFET, the channel is composed of single crystalline Si and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in poly-Si TFTs, the channel is composed of poly-Si. A large amount of trap state densities in grain structure attribute a lot of defect states in energy band gap to enhance the tunneling effect. Therefore, the leakage current is much larger in poly-Si TFTs than in MOSFET. When the voltage drops between gate voltage and drain voltage increases, the band gap width decreases and the tunneling effect becomes much more severe. Normally we can find this effect in typical poly-Si TFTs' I_{DS}-V_{GS} characteristics where the magnitude of leakage current will reach a minimum and then increase as the gate voltage decreases/increases for n/p-channel TFTs.

There are a lot of ways to specify the on and off-current. In this chapter, take n-channel poly-Si TFTs for examples, the on-current is defined as the drain current when gate voltage at the maximum value and drain voltage is 5V. The off-current is specified as the minimum current when drain voltage equals to 5V.

$$\frac{I_{ON}}{I_{OFF}} = \frac{Maximum\ \ Current\ \ of\ \ I_{DS}-V_{GS}\ \ Plot\ \ at\ \ V_{DS}=5V}{Minimum\ \ Current\ \ of\ \ I_{DS}-V_{GS}\ \ Plot\ \ at\ \ V_{DS}=5V} \text{ -------- (Eq. 1.5)}$$

1.4.5 Extraction of Grain Boundary Trap State Density

The Trap State Density (N_t), which can be determined by the theory established by Levinson *et al.* [32], which is based on Seto's theory [33].

For poly-Si TFTs, the drain current I_{DS} can be given as following:

$$I_{DS} = \mu_{FE} C_{ox} \left(\frac{W}{L}\right) V_{DS} V_{GS} \exp\left(\frac{-q^3 N_t^{\ 2} L_c}{8\varepsilon_{Si} k T C_{ox} V_{GS}}\right) \text{ ---------------------------- (Eq. 1.6)}$$

Where,

μ_{eff}	field-effect mobility of carriers
q	electron charge
k	Boltzmann's constant
ε_{Si}	dielectric constant of silicon
T	temperature
N_t	trap-state density per unit area
L_c	channel thickness

This expression, first developed by Levinson *et al.*, is a standard MOSFET's equation with an activated mobility, which depends on the grain-boundary barrier height. Levinson *et al.* assumed that the channel thickness was constant and equal to the thickness of the poly-Si film (t). This simplifying assumption is permissible only for very thin film (t<10nm). The trap-state density can be obtained by extracting a straight line on the plot of *ln*(I_{DS}/V_{GS}) versus $1/V_{GS}$ at low drain voltage and high gate voltage.

Proano *et al.* [34] thought that a barrier approximation is to calculate the gate induced carrier channel thickness by solving Poisson's equation for an undoped material and to define the channel thickness (L_c) as a thickness in which 80% of the total charges were induced by the gate. Doing so, one obtains

$$L_c = \frac{8kTt_{ox}\sqrt{\dfrac{\varepsilon_{Si}}{\varepsilon_{SiO_2}}}}{q\left(V_{GS} - V_{fb}\right)} \text{ ---------------------------------- (Eq. 1.7)}$$

which varies inversely with (V_{GS}−V_{fb}). This predicts, by substituting Eq.2.7 into Eq.1.6, that $ln[I_{DS}/(V_{GS}-V_{fb})]$ versus $1/(V_{GS}-V_{fb})^2$. We use the gate voltage at which minimum leakage current occurs as flat-band voltage (V_{fb}). Effective trap-state density (N_t) can be determined from the square root of the slope.

1.5 Organization of the Thesis

In the following sections, we will show our research efforts.

In Chapter 2, we proved NBTI is an important reliability issue in LTPS TFTs, and demonstrated the degradation of LTPS TFTs under NBTI stress is closely related to trap state creation. Measurements revealed the threshold voltage shift is highly correlated to the generation grain boundary trap states.

In Chapter 3, the impact of plasma damage on NBTI in LTPS TFTs is explored. The experimental results confirm that LTPS TFTs with larger antenna degrade more than those with smaller antenna. Plasma damage is demonstrated to enhance the device degradation in carrier mobility, threshold voltage and drive current under NBTI stress.

In Chapter 4, we investigated degradation mechanism of LTPS TFTs upon NBTI stress and HCI stress. To quantify the combined NBTI and HCI stress induced degradation, we proposed a modified model based on the empirical NBTI and HCI stress models, and the experimental results conformed to the model.

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Chapter 2

Characteristic of Negative Bias Temperature Instability in Low Temperature Polycrystalline Silicon Thin Film Transistors

2.1 Introduction

Polycrystalline silicon thin film transistors (poly-Si TFTs), the key devices for the use in the flat panel displays such as active matrix liquid crystal displays (AMLCDs), have attracted much research interest due to the possibility of realizing the integration of peripheral circuit and active matrix [1][2]. From the fabrication technology point of view and as a long-term reliability concern, the stability of poly-Si TFTs is of significant importance [3]. In p-channel MOSFETs, negative bias temperature instability (NBTI) has been found to be an important reliability problem and has been widely investigated. It has been reported the degradation of NBTI in MOSFETs is mainly due to the generation of interface states and fixed oxide charges, and NBTI can be thermally and electrically activated[4]-[7]. In poly-Si TFTs, due to poor thermal conductivity of the glass substrate and high operation voltage, we suppose NBTI is important in the reliability of poly-Si TFTs. Some researches have pointed out NBTI stress caused the performance degradation in poly-Si TFTs as well as in MOSFETs [8][9]. However, NBTI is still not thoroughly studied in poly-Si TFTs and the mechanism is not well known. In addition, the degradation mechanism of NBTI stress in poly-Si TFTs, due to the grain boundaries in the channel region, may be different from MOSFETs. Some studies have indicated that NBTI stress on poly-Si TFTs may generate trap states in the grain boundaries [9]. However, the correlation between the grain boundary trap state generation and the device degradation during NBTI stress in poly-Si TFTs has not been well explored.

In this chapter, the instabilities and mechanisms of p-channel low temperature poly-Si TFTs (LTPS TFTs) upon NBTI stress were studied. By measuring and analyzing the transfer and output characteristics before and after NBTI stress under different stress gate voltages and stress temperatures, we investigated the effects of NBTI in LTPS TFTs and proposed a new model to explain the experimental results.

2.2 Experimental

P-channel LTPS TFTs were fabricated on glass substrates with top-gate structures. In this study, a 40nm-thick a-Si layer was deposited by PECVD on a buffer layer and crystallized into poly-Si film by excimer laser annealing. After defining the active region, the gate dielectric was deposited with an equivalent 100nm-thick SiO_2 layer. Mo was then deposited and patterned as the gate electrode. Self-align source/drain was formed by plasma doping. Following that, the inter-layer dielectric was deposited and densified. The hydrogen atoms were also introduced during the deposition of the inter-layer dielectric to passivate the dangling bonds at the poly-Si/SiO_2 interface and in the grain boundaries. The dopants were activated during the densification of the inter-layer dielectric. Finally, inter-connection metal was deposited and patterned. The channel length (*L*) and channel width (*W*) of the device used in this study were 10um and 20um, respectively.

During NBTI stress, the glass substrate was heated to the stress temperature ranging from 25^{o}C to 150^{o}C, and the stress voltage in the range of -15V to -30V was applied the gate with the source/drain grounded. The stress was periodically stopped to measure the basic characteristics of the device to characterize the NBTI effect. All the measurements were taken at the stress temperature. Fowler-Nordheim current was not pronounced at these bias conditions; therefore, the extra trap state generation and device instability caused by the small current can be neglected. The schematic cross-section diagram of the LTPS TFT and NBTI stress setup is shown in Figure 2-1.

2.3 Results and Discussion

Figure 2-2(a)(b) show the transfer characteristics and output characteristics, respectively, of LTPS TFT before and after NBTI stress at 100^{o}C with the stress gate voltage of -30V for 1000sec. From Figure 2-2(a), it is observed the threshold voltage becomes larger in the negative direction after NBTI stress. In MOSFETs, the threshold voltage shift is attributed to the generation of fixed oxide charges and interface states [4]-[7]. In poly-Si TFTs, however, there are many grain boundaries in the channel regions and must be considered. Therefore, we suggested the threshold voltage shift in poly-Si TFTs is attributed to the generation of grain boundary trap states as well as the fixed oxide charges and interface states, and this will be discussed later.

In addition to the threshold voltage shift, NBTI stress also leads to the degradation of LTPS TFTs in subthreshold swing (*S.S.*), drive current (I_{ON}), and maximum transconductance ($G_{m,max}$).

Two parameters leading to the degradation of I_{ON} and $G_{m.max}$ are the threshold voltage (V_{th}) shift and field-effect mobility (μ_{eff}) decrease. The decrease of maximum transconductance indicates the field-effect mobility was degraded during the NBTI stress. The drain current significant decreased after NBTI stress as shown is Figure 2-2(b), which is due to the threshold voltage shift and field-effect mobility degradation.

Figure 2-3(a)(b)(c) show the dependence of the threshold voltage shift (⊿V_{th}) on the stress time (t) , stress voltage (V_G) and stress temperature (T), respectively. The gate voltage at a specified threshold drain current (I_{DS}), -(W/L)x10nA for V_{DS}=-0.1V, is taken as the threshold voltage. In Figure 2-3(a), the threshold voltage shift increases with the stress time and shows power law dependence. In Figure 2-3(b) and (c), it is observed NBTI will be enhanced at higher stress voltage or higher stress temperature, demonstrating NBTI can be electrically and thermally activated.

The behavior of the threshold voltage shift can be modeled as [10]

$$\Delta V_{th} \propto t^{n} e^{(-E_a/kT)} e^{C|V_G|} \qquad \text{---(Eq.2.1)}$$

where the exponent factor n is around 0.28 to 0.34 in our experiment, which is similar to the results of previous researches in poly-Si TFTs [8][9] and bulk MOSFETs [11]. The parameter C extracted from Figure 2-3(b) is between 0.10 and 0.13, which is dependent on the process and independent of stress voltage. The activation energy (E_a) extracted from the Arrhenius plot of Fig. 2-3(c) is about 0.14eV.

It is important to distinguish whether the devices degradation under NBTI stress is due to charge trapping in the gate dielectric or due to state creation. In some models of charge trapping in gate dielectric [12], it is revealed that when the device is under gate bias stress, charges may inject into the gate dielectric and generate extra trap states, leading to the threshold voltage shift. From the previous studies, the threshold voltage shift caused by charge trapping process shows exponential dependence on $1/V_{-G}$ and virtually temperature independent [12][13]. If the V_{th} shift is caused by charge trapping, it should have the same dependence on the stress gate voltage and stress temperature as the charge trapping model. However, the charge trapping model can't explain the exponential dependence of threshold voltage shift on V_G and 1/T as shown in Fig. 2-3(b) and (c), respectively. Besides, the charge trapping models [12] can't explain the linear fit of the log-log plot of the threshold voltage shift versus the stress time as shown in Fig. 2-3(a). In addition, the gate leakage current is less than the detection limit, which implies NBTI degradation is not related to the energetic holes [14]. Therefore, instead of charge trapping in the dielectric, we suggested the threshold voltage shift during NBTI stress is due to the state creation in the gate dielectric or channel region.

The lifetimes of LTPS TFTs are plotted as a function of the stress voltage with various stress temperatures as shown in Fig. 2-4. The lifetime is defined as the time taken for the device to reach a threshold voltage shift of 100mV under NBTI stress. Obviously, the lifetime degrades with the increase of stress voltage or temperature because NBTI can be electrically and thermally activated.

Fig. 2-5(a) and (b) reveal the correlation between the degradation of subthreshold swing, maximum transconductance, respectively, and the threshold voltage shift. The generation of interface states is reflected in both the subthreshold swing and maximum transconductance degradation. Furthermore, it has been reported that the subthreshold swing is more closely related to the trap states located near the midgap (deep states), while the mobility is more associated with the trap states located near the band edge (tail states) [15]. The deep states and tail states originate from the dangling bonds and strain bonds, respectively. In addition, the degradation of subthreshold swing is found to be severer than maximum transconductance degradation; accordingly, we suggested NBTI causes the generation of interface states, and the interface state creation is mainly attributed to the formation of dangling bonds.

Due to the grain boundaries in the channel region, the degradation mechanism of NBTI stress in LTPS TFTs may be different from MOSFETs. In MOSFETs, it has been reported NBTI is mainly due to the generation of interface states and fixed oxide charges [4]-[7]. In order to study the effects of the grain boundaries in LTPS TFTs during NBTI stress, the grain boundary trap state density (N_{trap}) before and after stress were estimated by Levinson and Proano method [16][17]. Fig. 2-6 exhibits the plots of $\ln[I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at low V_{DS} and high V_{GS}. The grain boundary trap state density can be determined form the square root of the slope

$$N_{trap} = \frac{C_{OX}}{q}\sqrt{|Slope|}\ . \text{ ---}\tag{Eq.2.2}$$

From Fig. 2-6, it is apparent the grain boundary trap state density increased after NBTI stress, indicating grain boundary trap state generation plays an important role in NBTI stress for LTPS TFTs. Therefore, in addition to the generation of fixed oxide charges and interface states, we have proved the threshold voltage shift of LTPS TFTs under NBTI stress is closely related to grain boundary trap state creation.

In order to learn more about the generation of grain boundary trap states, the dependence of the grain boundary trap state density variation on the stress time is shown in Fig. 2-7. The grain boundary trap state density variation, like the threshold voltage shift, also follows a power law dependence on the stress time with an exponent of 0.25 to 0.32, which is similar to the exponent factor extracted from Fig. 2-3(a). This means the, threshold voltage shift and grain boundary trap state generation show the same dependence on the stress time. In addition, we also studied the dependence of the grain boundary trap state density variation on the stress voltage and stress temperature (not shown here). It is found the grain boundary trap state density variation has the same function form as the threshold voltage shift, and the grain boundary trap state density variation can be represented as

$$\Delta N_{trap} \propto t^{n'} e^{(-E_a'/kT)} e^{C'|V_G|}. \quad \text{--(Eq.2.3)}$$

The parameters *n'*, E_a*'*, *C'* under various NBTI stress conditions are shown in Fig. 2-8, and compared with *n*, E_a, and *C* extracted from the threshold voltage shift. It is worth noting that *n'*, *Ea'* and *C'* are similar to *n*, E_a and *C*, respectively, which implies the grain boundary trap state generation and the threshold voltage shift show the same dependence on the stress time, stress voltage and stress temperature.

Fig. 2-9 illustrates the correlation between the grain boundary trap state density variation and threshold voltage shift, and both of the two physical quantities are closely related because they have the same dependence on the stress time, stress voltage and stress temperature as discussed above. Therefore, we have demonstrated the grain boundaries trap state generation is closely related to the threshold voltage shift during NBTI stress in LTPS TFTs.

In the channel region, we suggested the generation of trap states in the grain boundaries and near the poly-Si/SiO_2 interface occurs during NBTI stress. In order to study the correlation between the generations of the grain boundary trap states and trap states near the poly-Si/SiO_2 interface, by neglecting the depletion capacitance in the active layer, the effective interface trap state density (N_{it}) near the poly-Si/SiO$_2$ interface can be evaluated from the subthreshold swing (S.S.) [18]

$$N_{it} = \left[\left(\frac{S.S.}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1\right]\left(\frac{C_{OX}}{q}\right) \text{.--(Eq.2.4)}$$

Fig.2-10 shows the correlation between the generation of effective interface trap state density (N_{it}) near the poly-Si/SiO$_2$ interface and grain boundary trap state density (N_{trap}). It is observed the generation rates of N_{trap} and N_{it} during NBTI stress were almost the same. As a result, it is proved the grain boundary trap state generation during NBTI stress is accompanied with the trap state generation near the poly-Si/SiO$_2$ interface.

Fig.2-11 shows the dependence of the drive current degradation on the stress voltage after 1000sec NBTI stress with various stress temperatures. Due to the threshold voltage shift and mobility degradation, the drive current decreased with NBTI stress. In addition, NBTI can be thermally or electrically accelerated, thus the drive current decreases drastically at elevated stress temperature or higher stress gate voltage.

In our experiment, both the threshold voltage shift and grain boundary trap state generation have almost the same power-law dependence on the stress time. The exponent value is about 1/4 to 1/3, which is explained by the diffusion-controlled electrochemical reactions [5][19]. By expanding the model proposed for bulk-Si MOSFETs [19], we proposed a new model to explain the effect of NBTI on LTPS TFTs as shown in Fig. 2-12. We assume the Si dangling bonds at the poly-Si/SiO$_2$ interface and in the grain boundaries were passivated by hydrogen atoms initially. During NBTI stress, hydrogen atoms, being weakly bonded to the Si atoms, reacted with the holes from the inversion layer and dissociated from the Si atoms, resulting in the generation of interface states and grain boundary trap states. The released hydrogen species (atomic or molecular, or ionic or neutral) reacted with SiO_2, leaving positive fixed oxide charges in SiO_2. Finally, the hydrogen species diffused in SiO_2, which became the reaction-limiting factor.

2.4 Summary

Negative bias temperature instability of p-channel LTPS TFTs has been studied in this article, and we have proved NBTI is important in the reliability of LTPS TFTs. It is found the threshold voltage, subthreshold swing, maximum transconductance and drive current of LTPS TFTs degrade after NBTI stress. The device degradation caused by NBTI stress increases with temperature and electric field, indicating NBTI can be thermally and electrically activated. Due to the grain boundaries in the channel regions of LTPS TFTs, the grain boundaries trap state generation must be considered during NBTI stress. In this study, it is proved the threshold voltage shift is closely related to the grain boundary trap state generation, because both the two physical quantities follow almost the same power low dependence on the stress time; moreover, exponential dependence on the stress voltage and reciprocal of the ambient temperature. The exponent value of the power law dependence on the stress time is about 1/4 to 1/3, which is explained by the diffusion-controlled electrochemical reactions. Besides threshold voltage shift, NBTI also leads to the degradation of subthreshold swing, driving current and hole mobility. From the experimental results, we concluded that NBTI is caused by the generation of fixed oxide charges, interface states and grain boundary trap states in LTPS TFTs. Furthermore, a physical model is proposed and verified by the experimental results.

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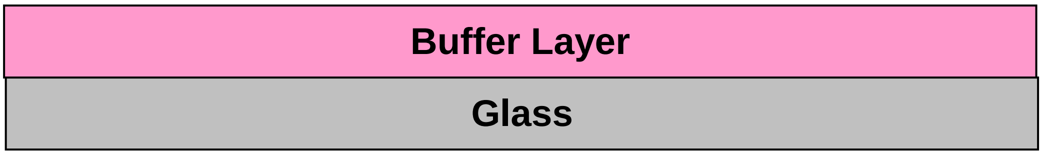
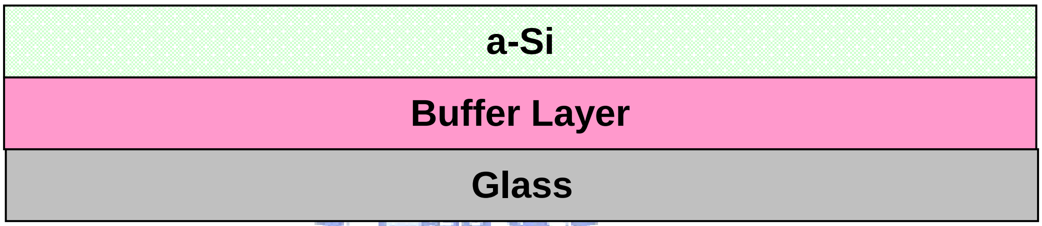
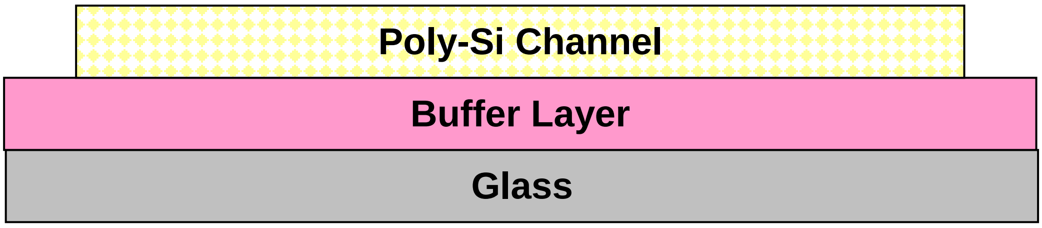


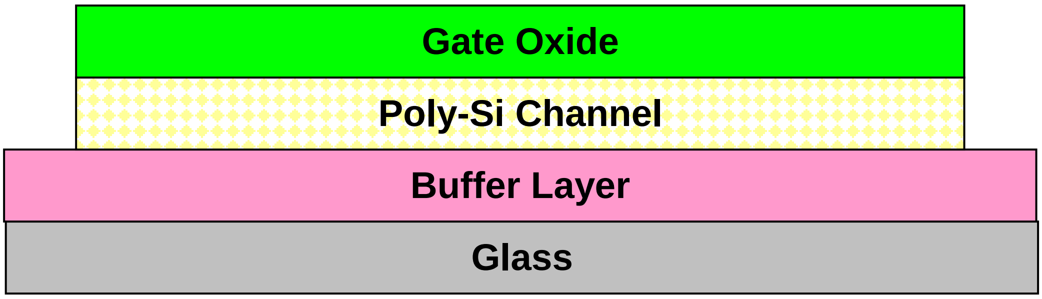
(a) Buffer layer deposition .on glass substrate.



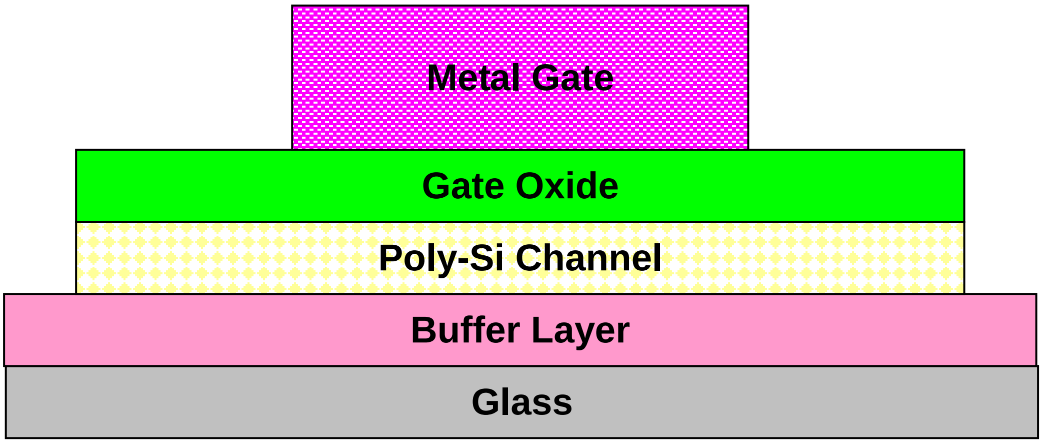
(b) Amorphous Si (a-Si) deposited by PECVD.



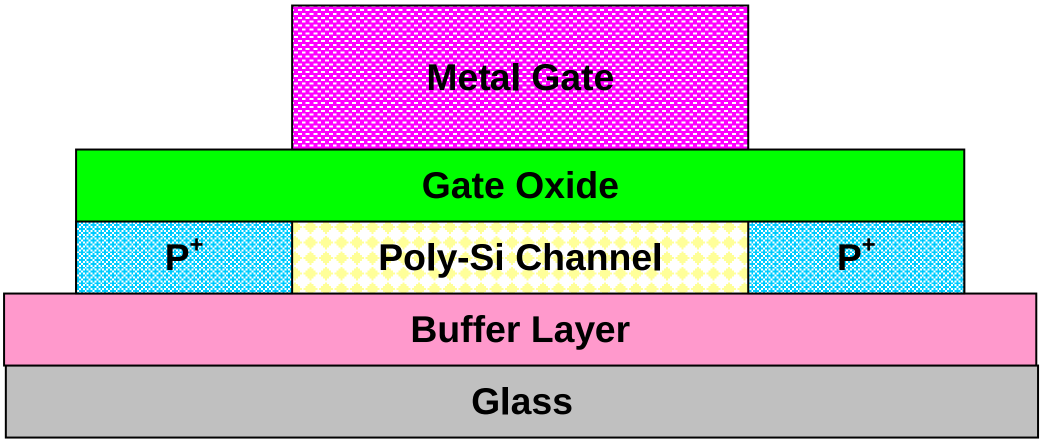
(c) Crystallization of a-Si film into poly-Si film by excimer laser annealing, and active region defined.



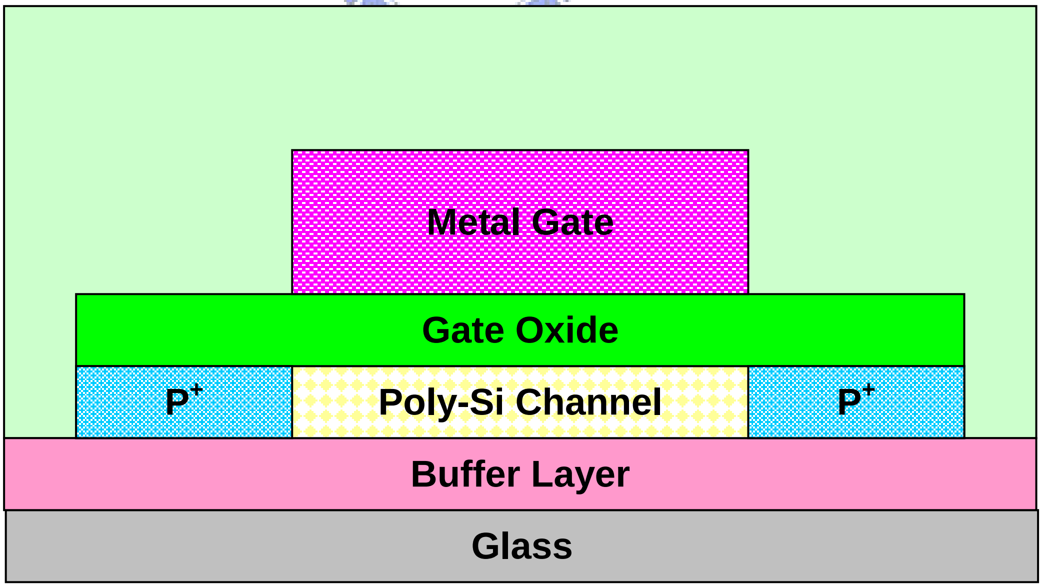
(d) Deposition .of gate oxide by PECVD



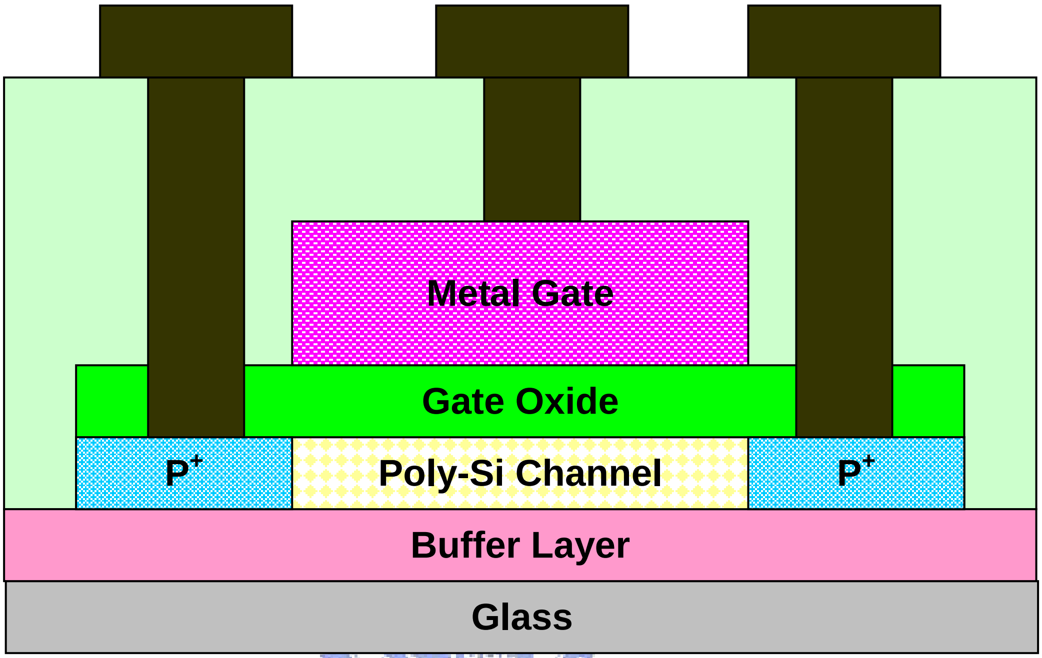
(e) Deposition Mo as the gate electrode.



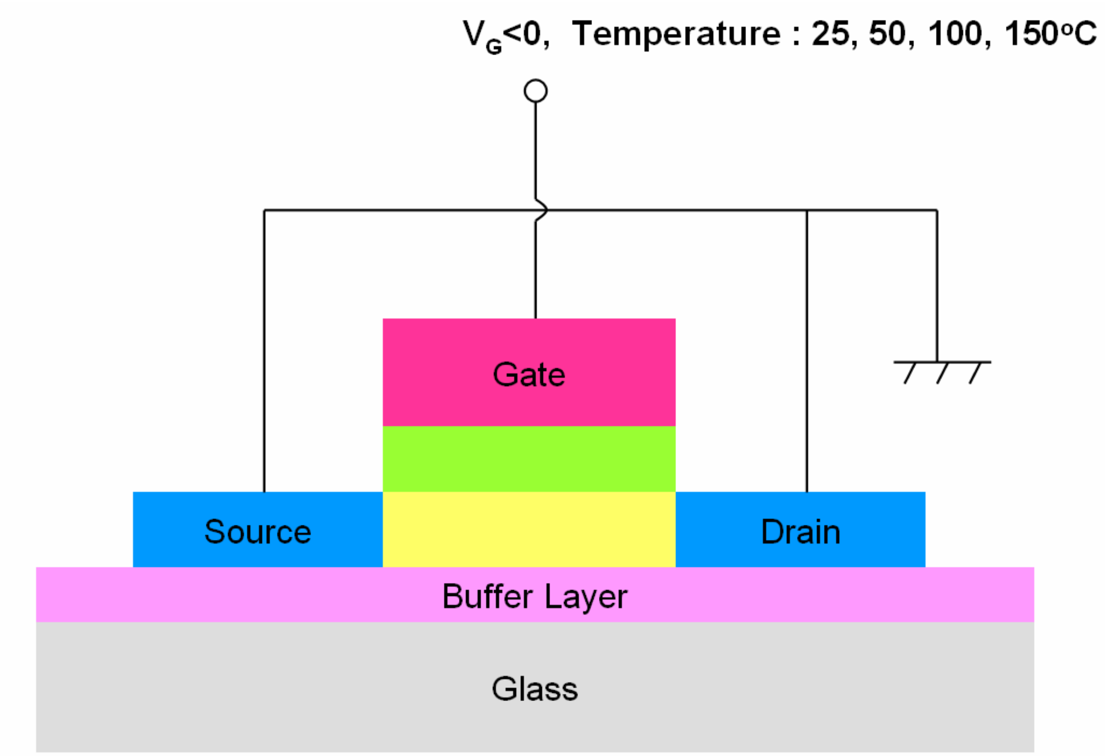
(f) Self-align Source/Drain was formed.



(g) Interface layer deposition and dopant activation..



(h) Contact holes was opened and inter-connection metal was deposited and patterned.



(i) Schematic cross-section diagram of LTPS TFT and NBTI stress setup. The stress temperature was performed from 25°C to 150°C, and the stress gate voltage was applied in the range of -15V to -30V with source and drain grounded.

Fig. 2-1 Process flow of the poly-Si TFT.

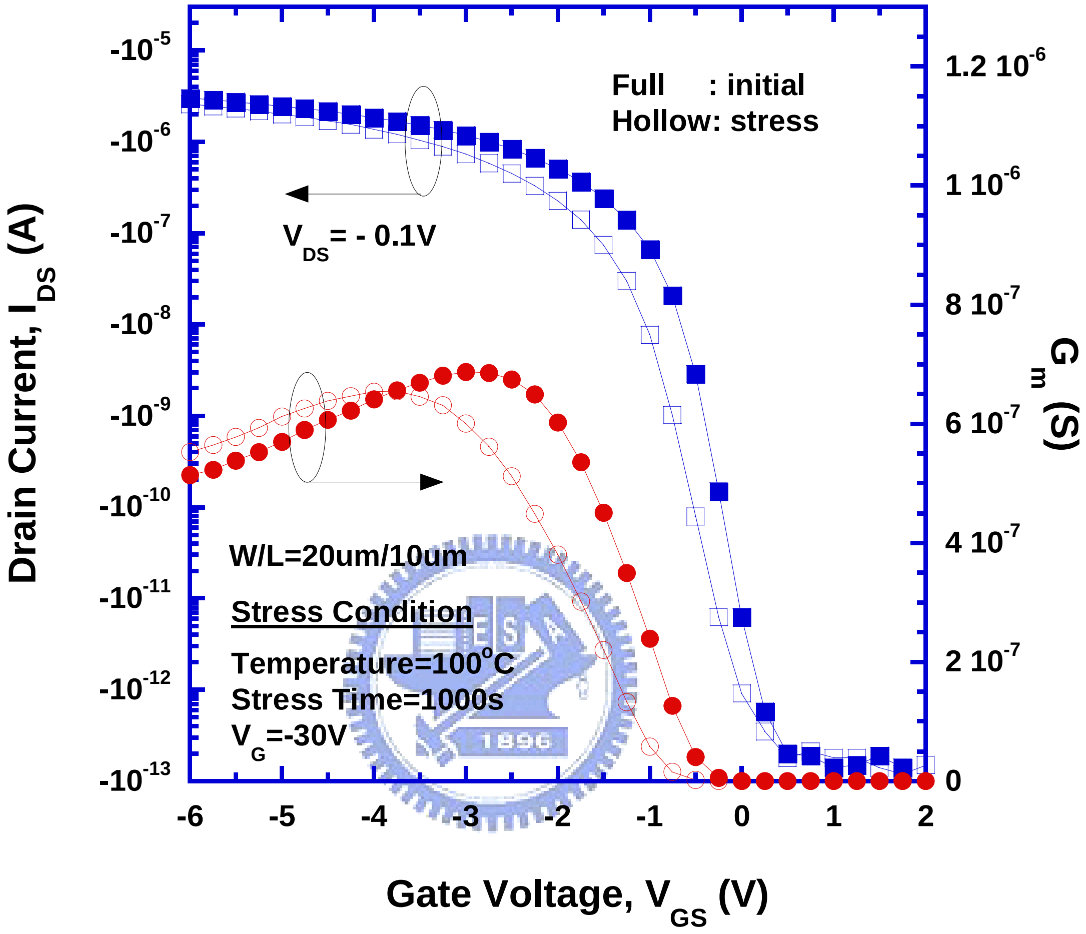


Fig. 2-2(a) Transfer characteristics of LTPS TFT before and after 1000sec NBTI stress at 100^{o}C with the stress voltage of -30V.

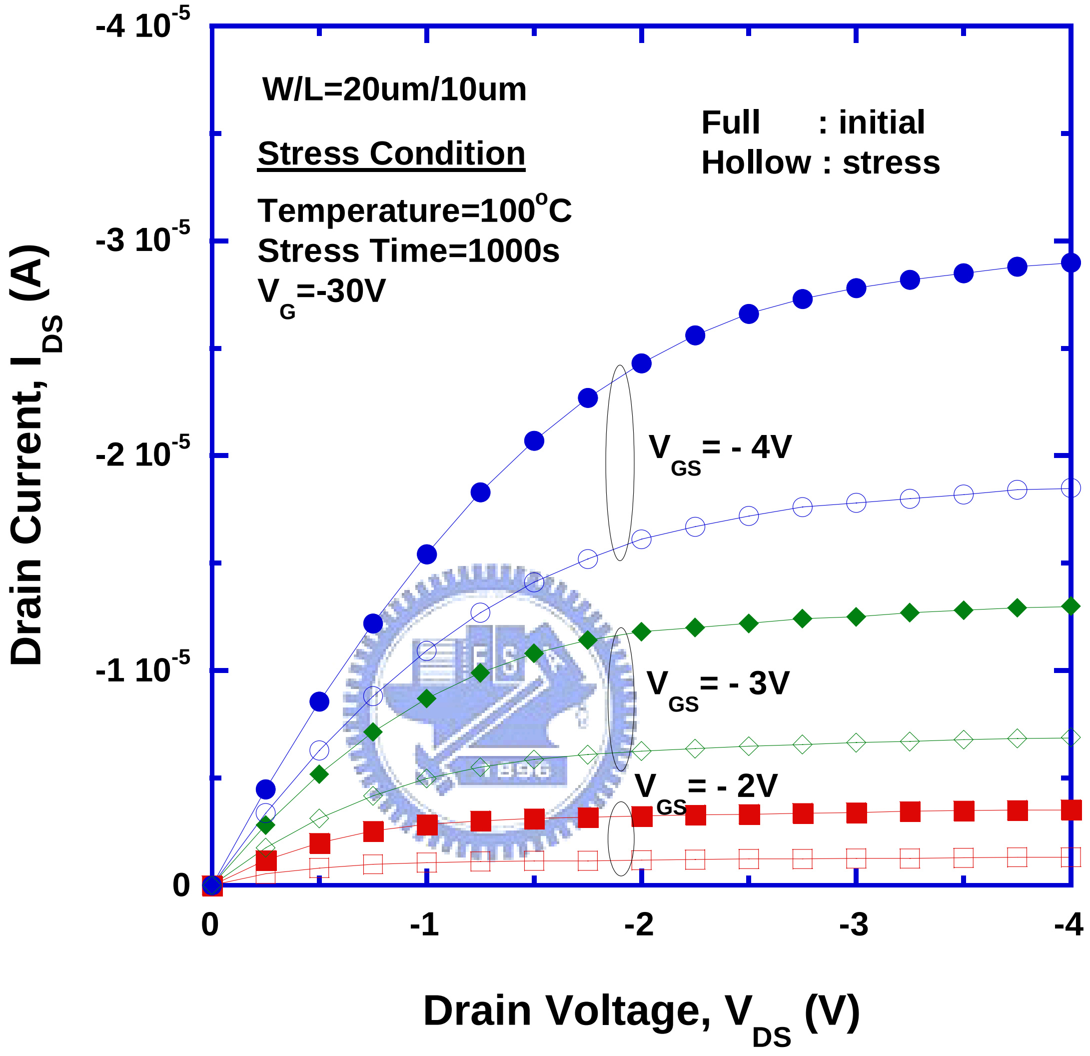


Fig. 2-2(b) Output characteristics of LTPS TFT before and after 1000sec NBTI stress at 100^{o}C with the stress voltage of -30V.

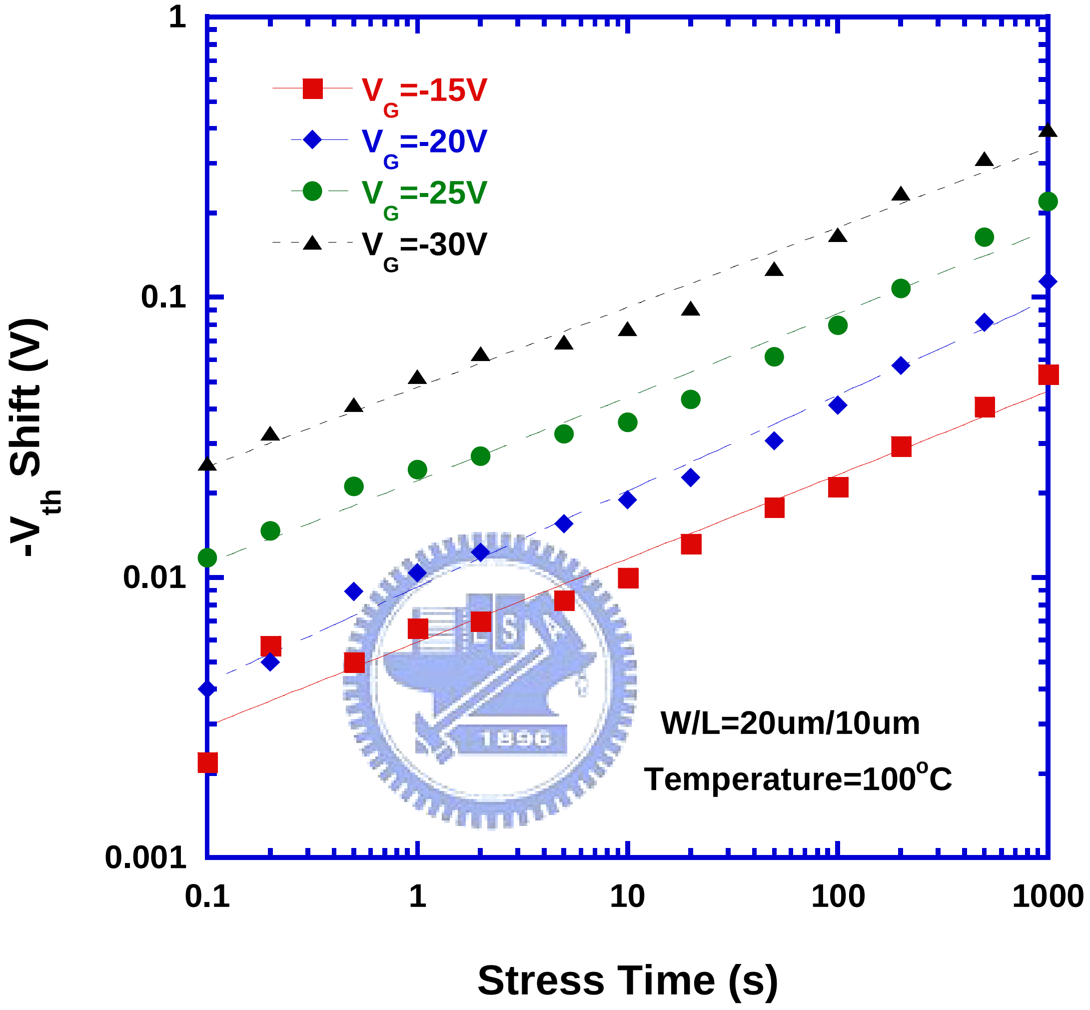


Fig. 2-3(a) Dependences of threshold voltage shift on the stress time of LTPS TFTs under various stress conditions.

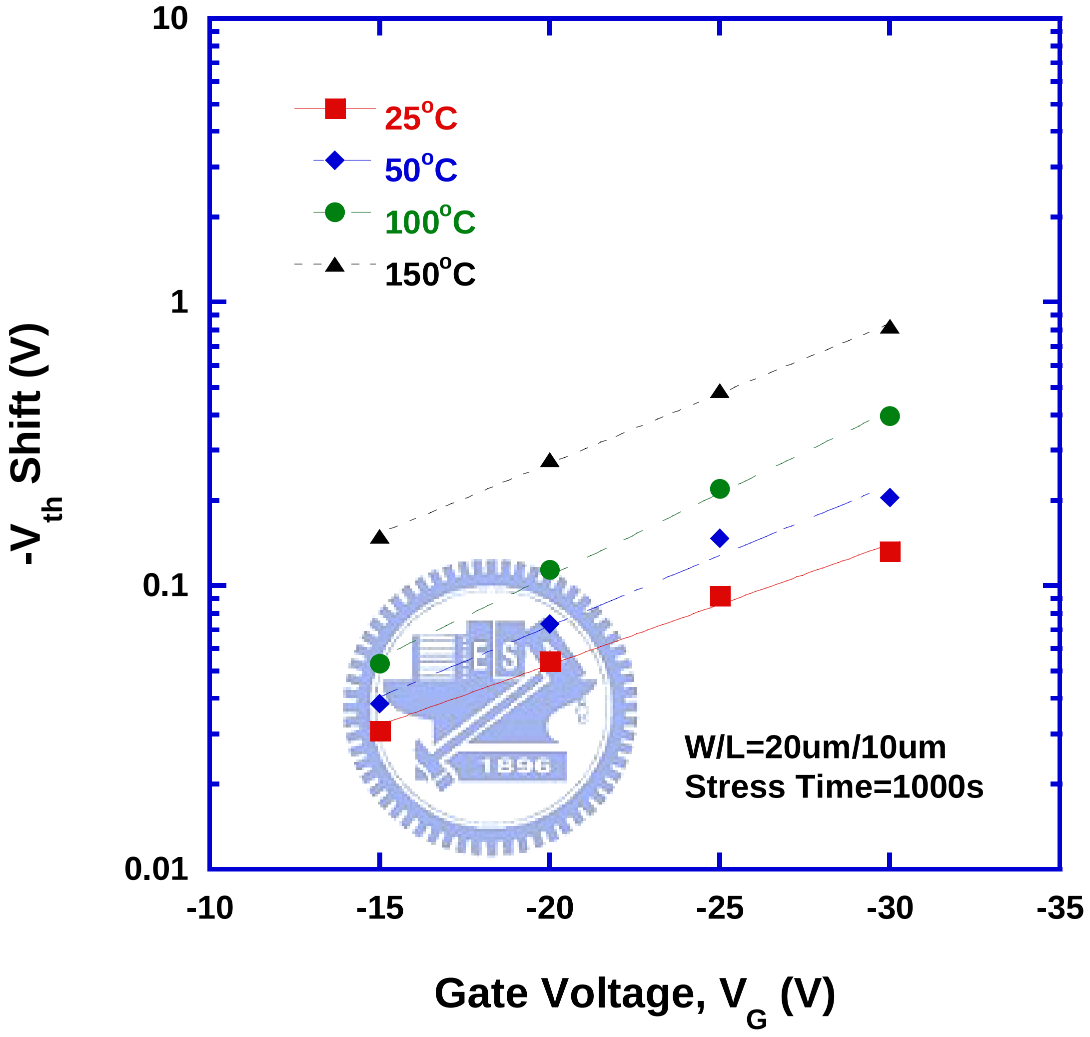


Fig. 2-3(b) Dependences of threshold voltage shift on the stress voltage of LTPS TFTs under various stress conditions.

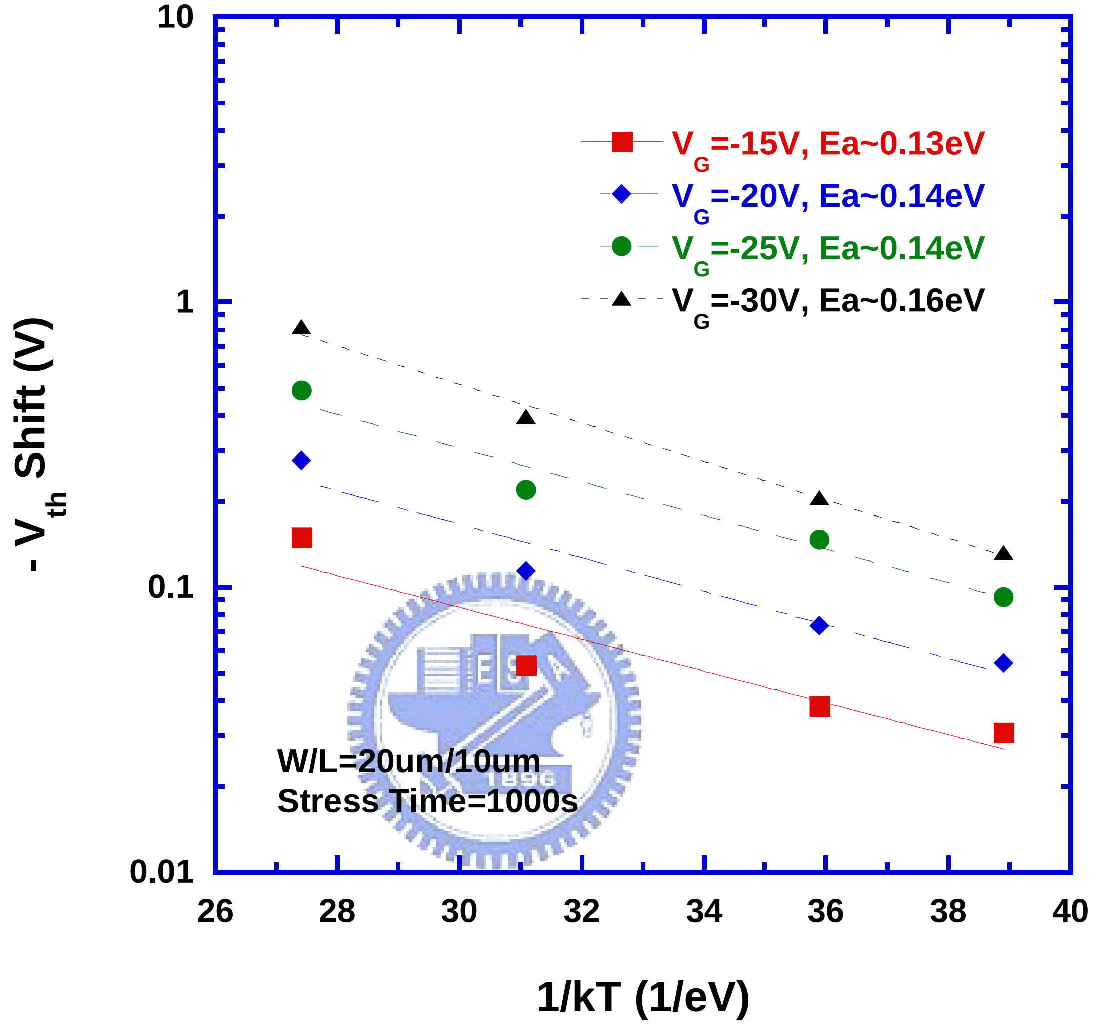


Fig. 2-3(c) Dependences of threshold voltage shift on the stress temperature of LTPS TFTs under various stress conditions.

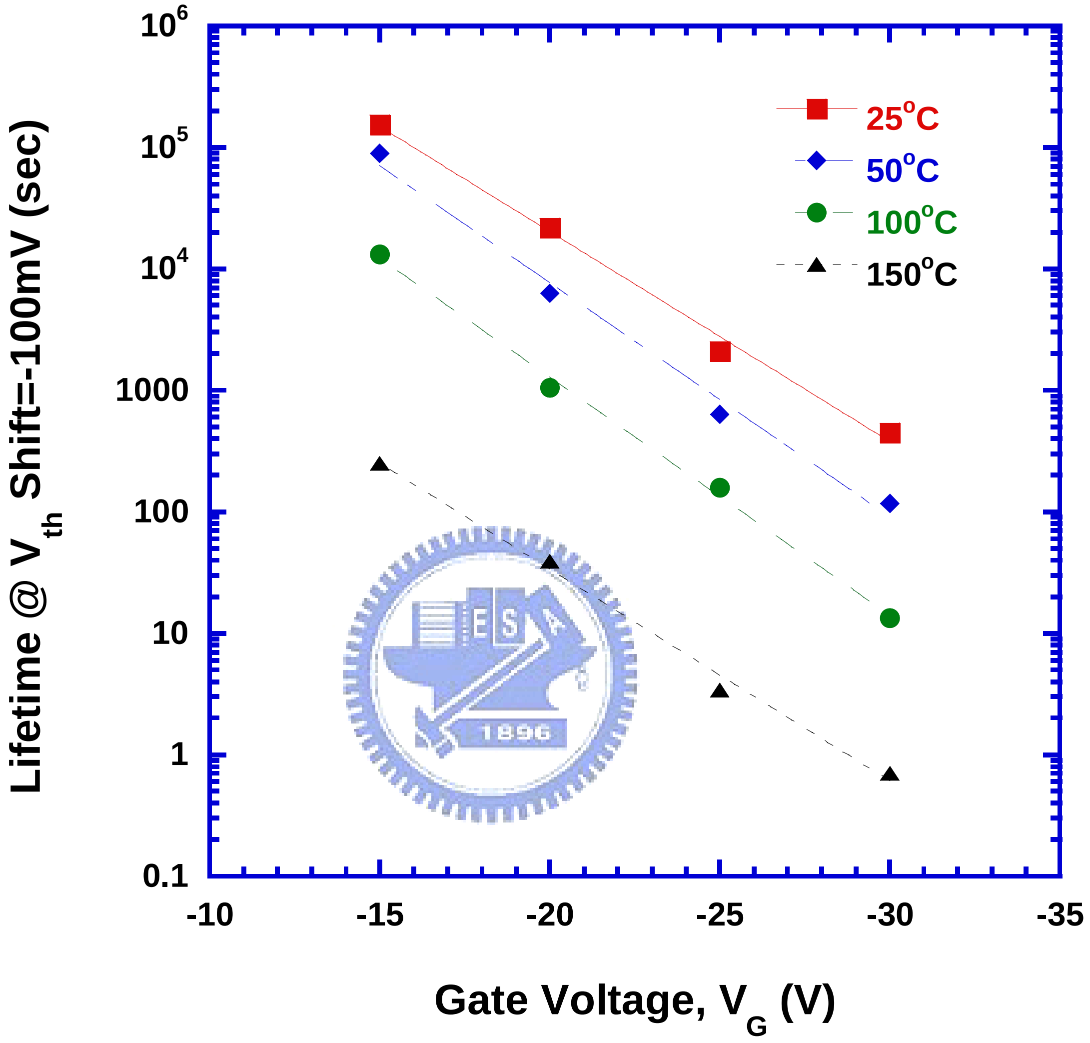


Fig. 2-4. Dependences of lifetime on the stress voltage with various stress temperatures. The lifetime is defined as the time taken to reach a threshold voltage shift of 100mV.

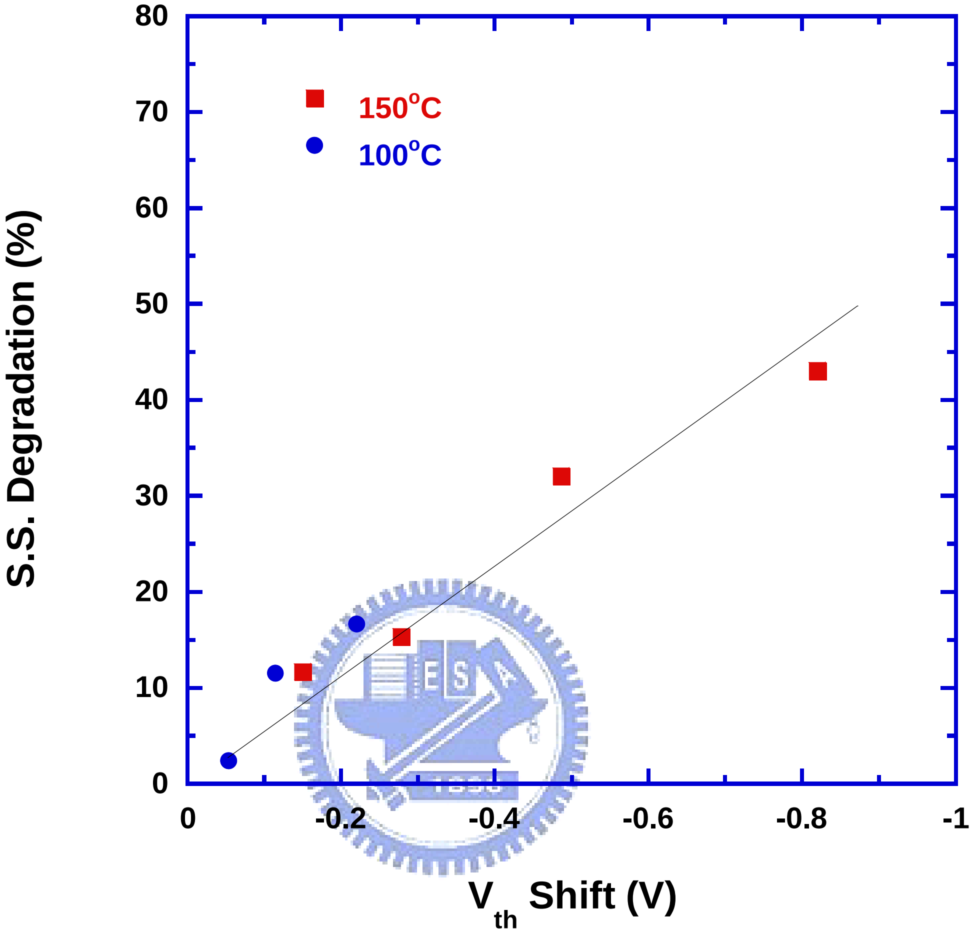


Fig. 2-5(a) Correlation between the degradation of subthreshold swing, and threshold voltage shift of LTPS TFTs after NBTI stress.

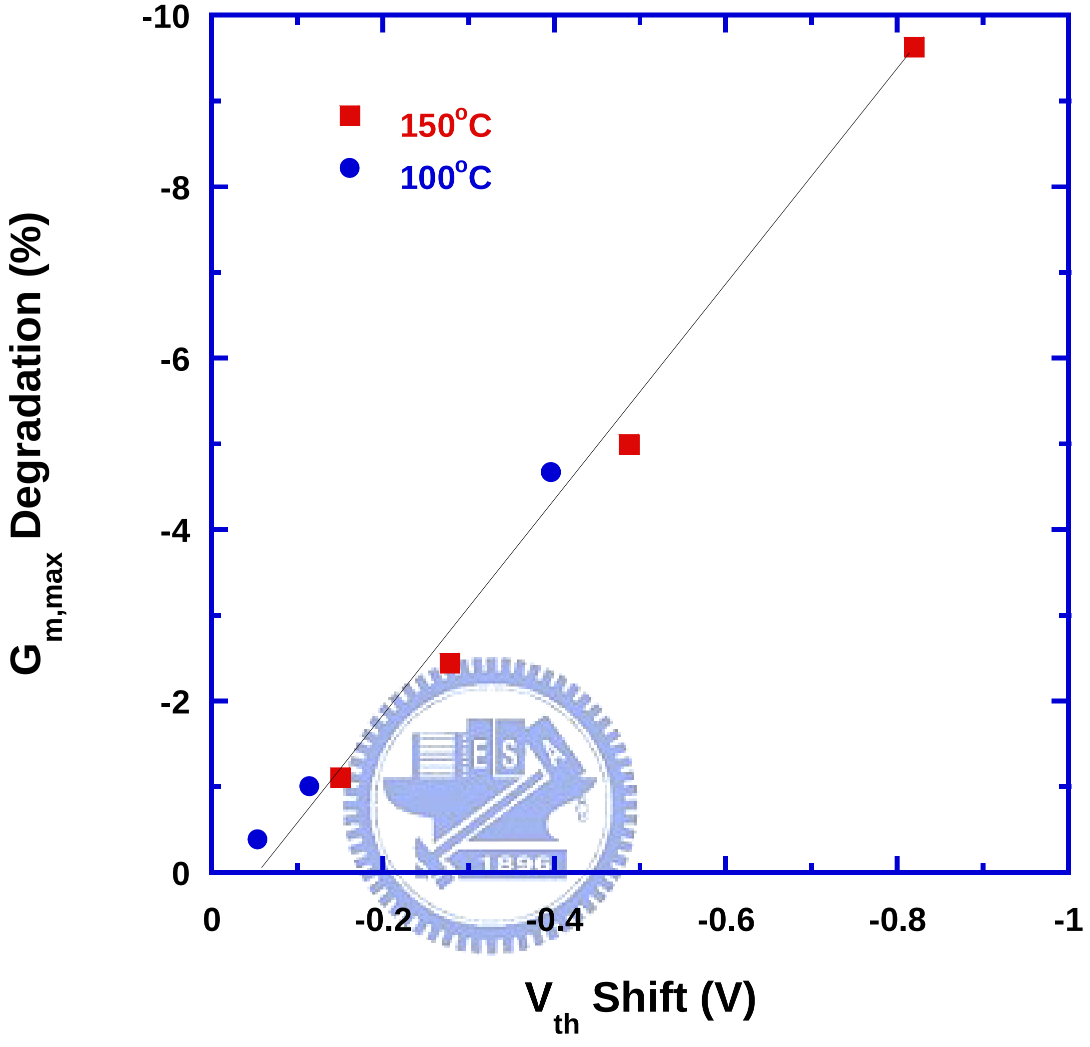


Fig. 2-5(b) Correlation between the degradation of maximum transconductance, and threshold voltage shift of LTPS TFTs after NBTI stress.

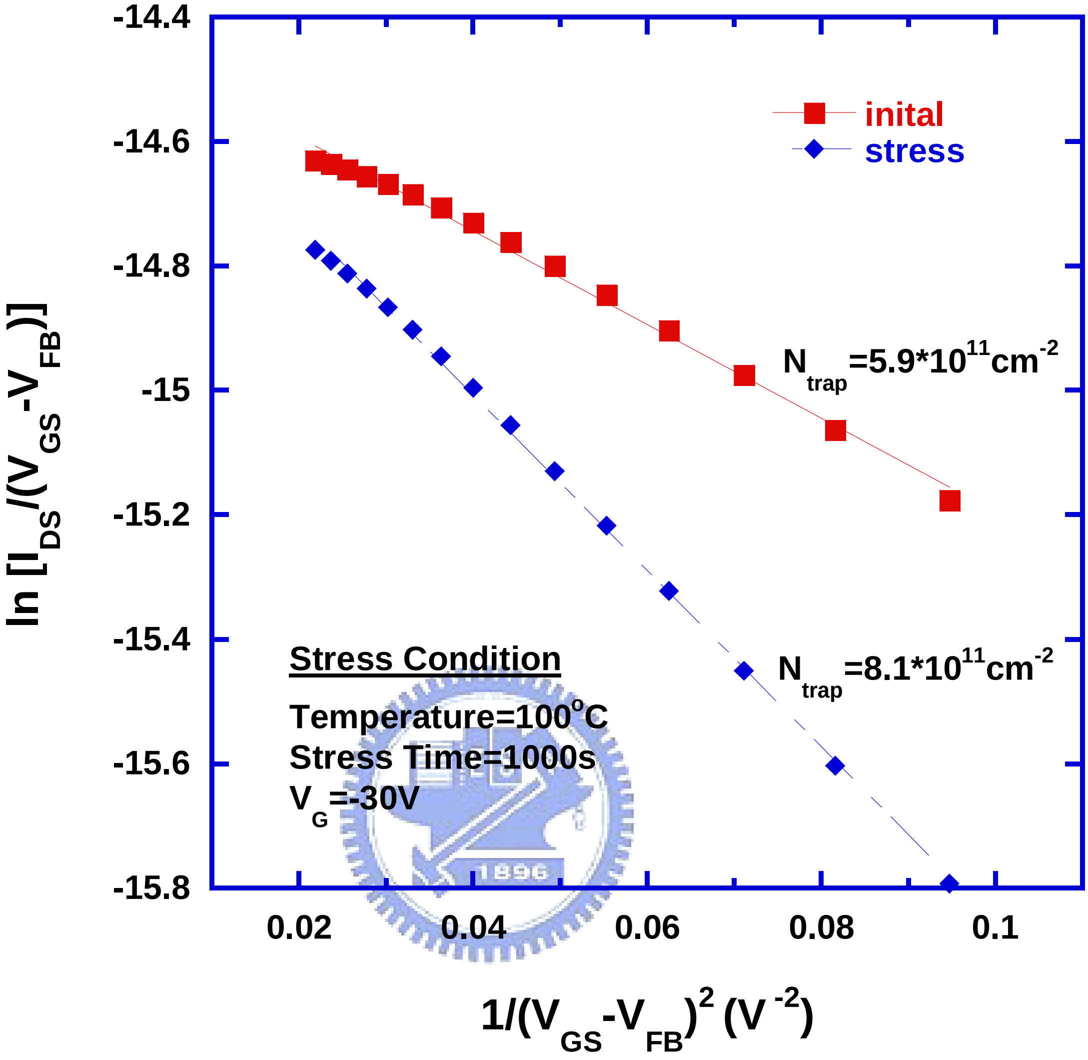


Fig. 2-6. Grain boundary trap state density extraction of LTPS TFT before and after 1000 sec NBTI stress at 100°C with the stress voltage of -30V.

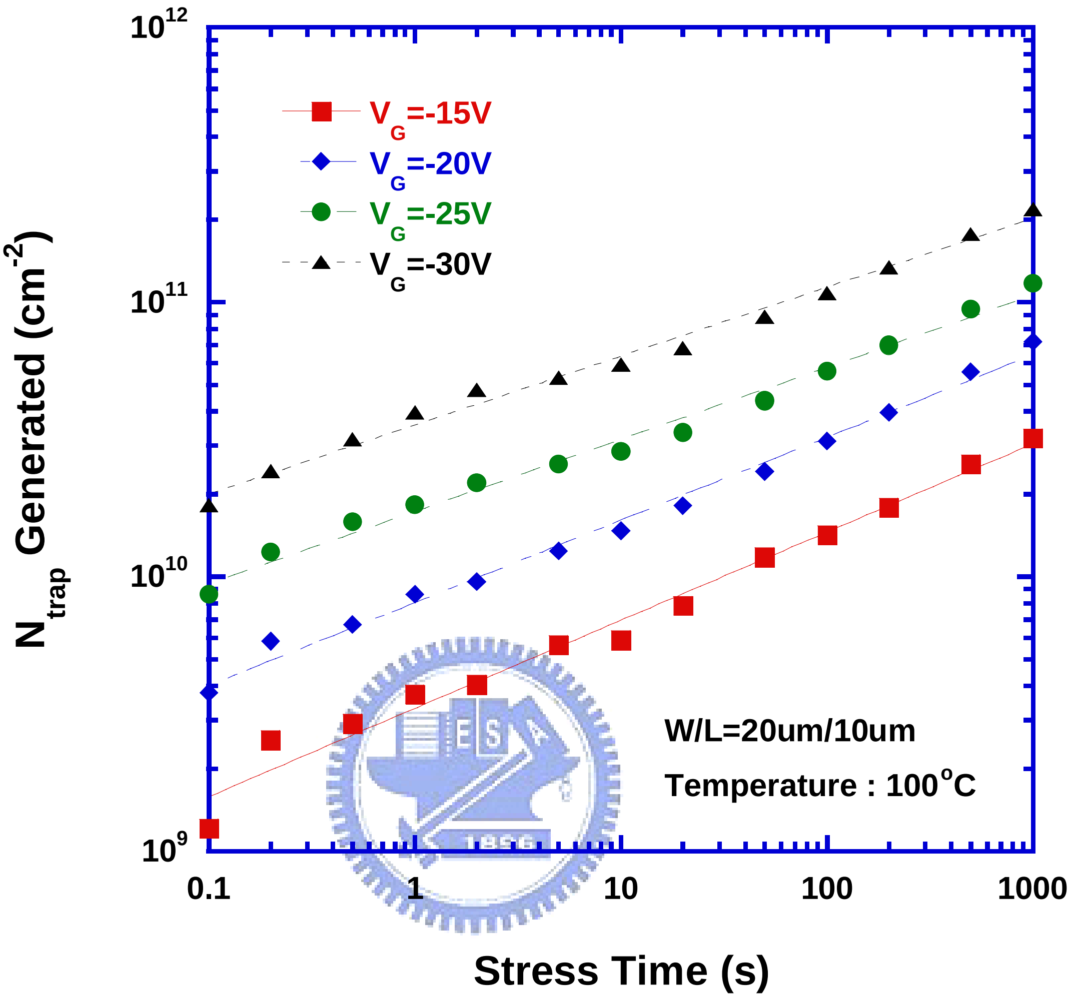


Fig. 2-7. Dependences of grain boundary trap state density variation on the stress time at 100°C with various stress gate voltages.

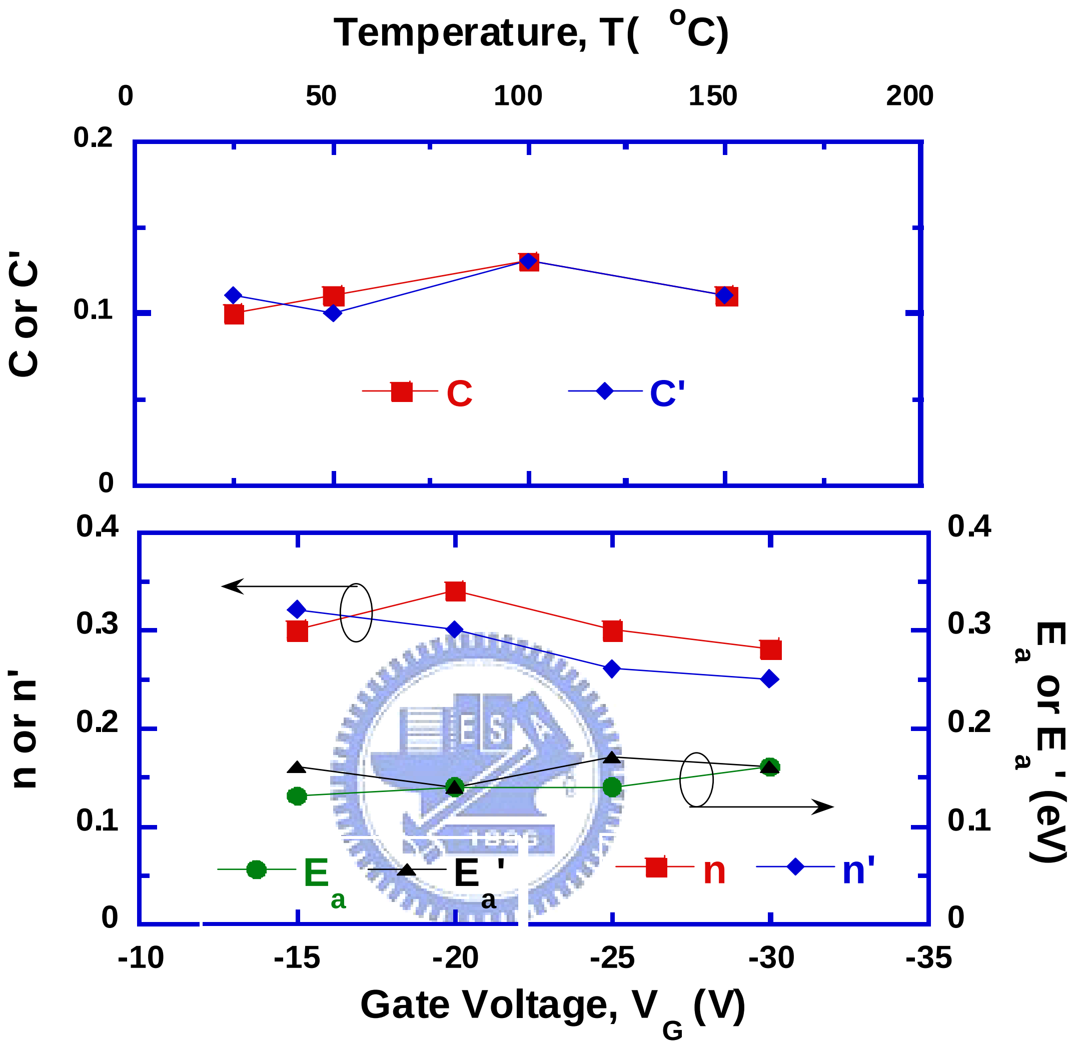


Fig. 2-8. Comparison of parameters of V_{th} shift and N_{trap} generated.

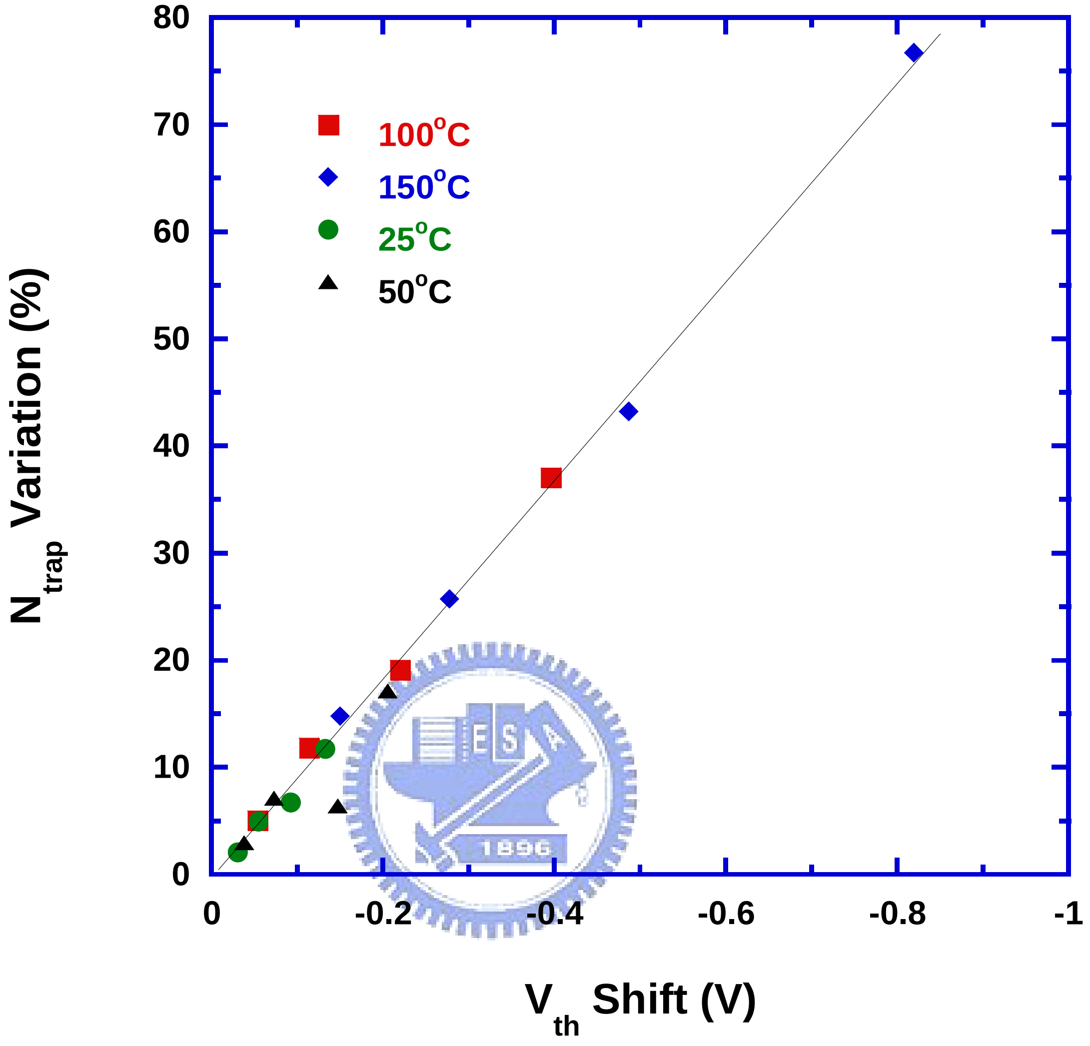


Fig. 2-9. Correlation between grain boundary trap state density variation and threshold voltage shift of LTPS TFTs after NBTI stress.

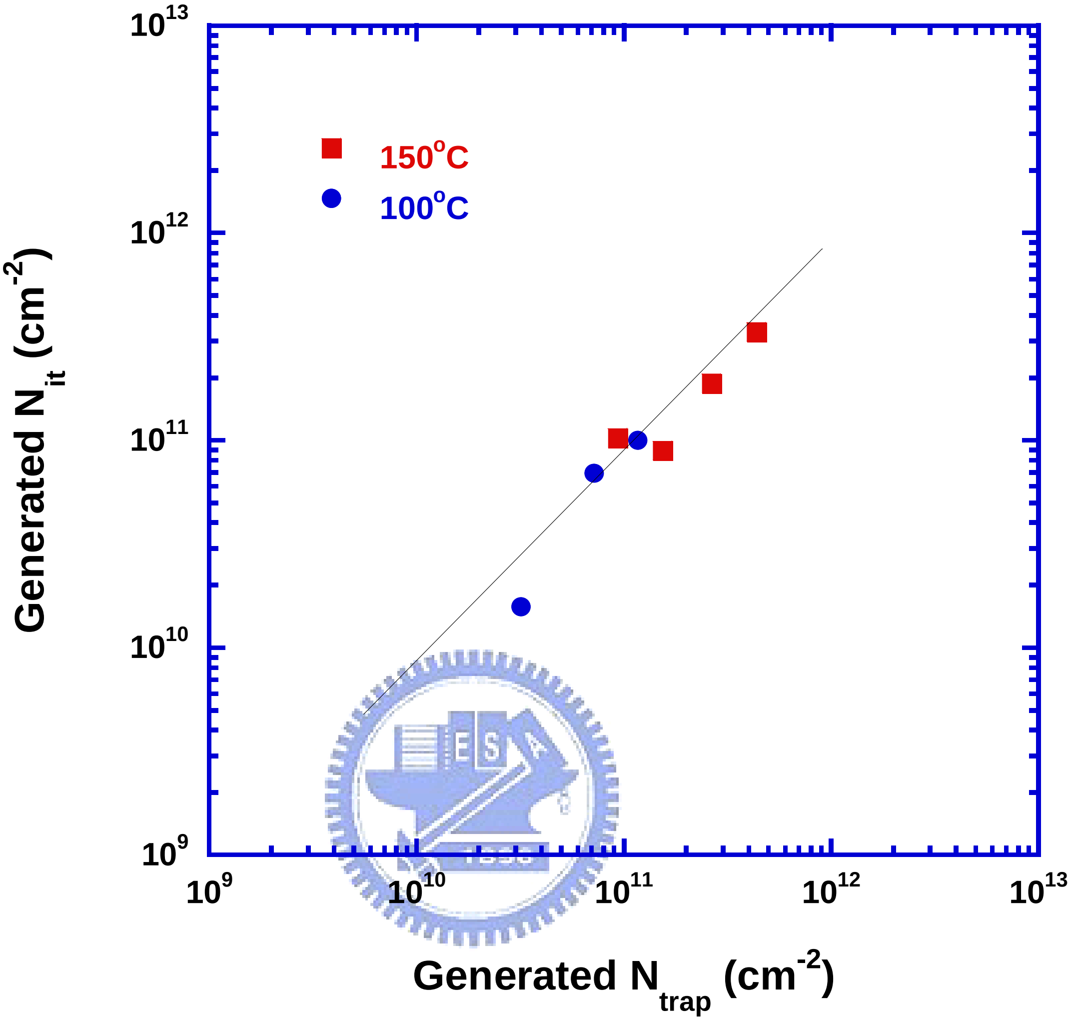


Fig. 2-10. Correlation between the generation of interface state density and grain boundary trap state density of LTPS TFTs after NBTI stress.

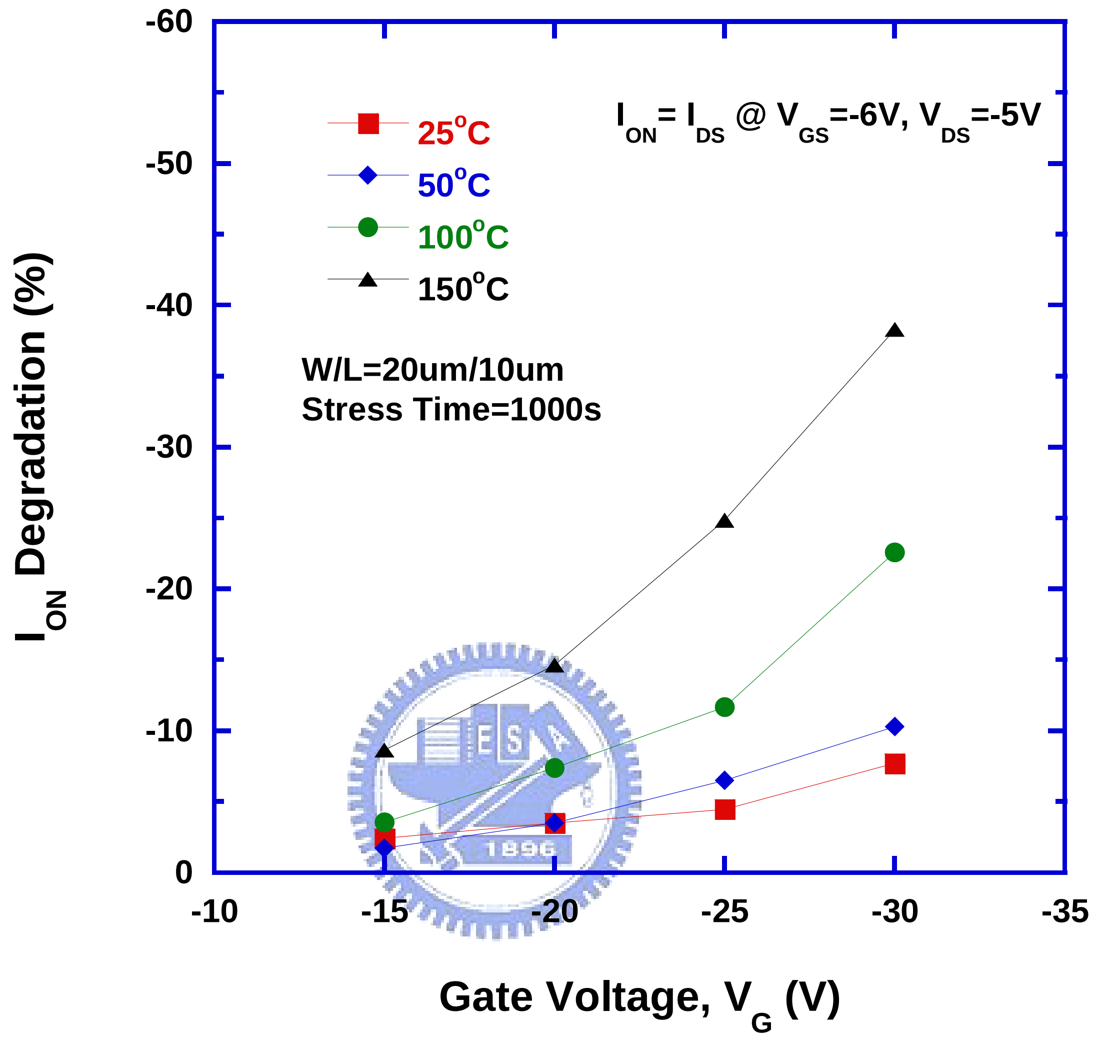


Fig. 2-11. Dependences of drive current degradation on the stress voltage with various stress temperatures.

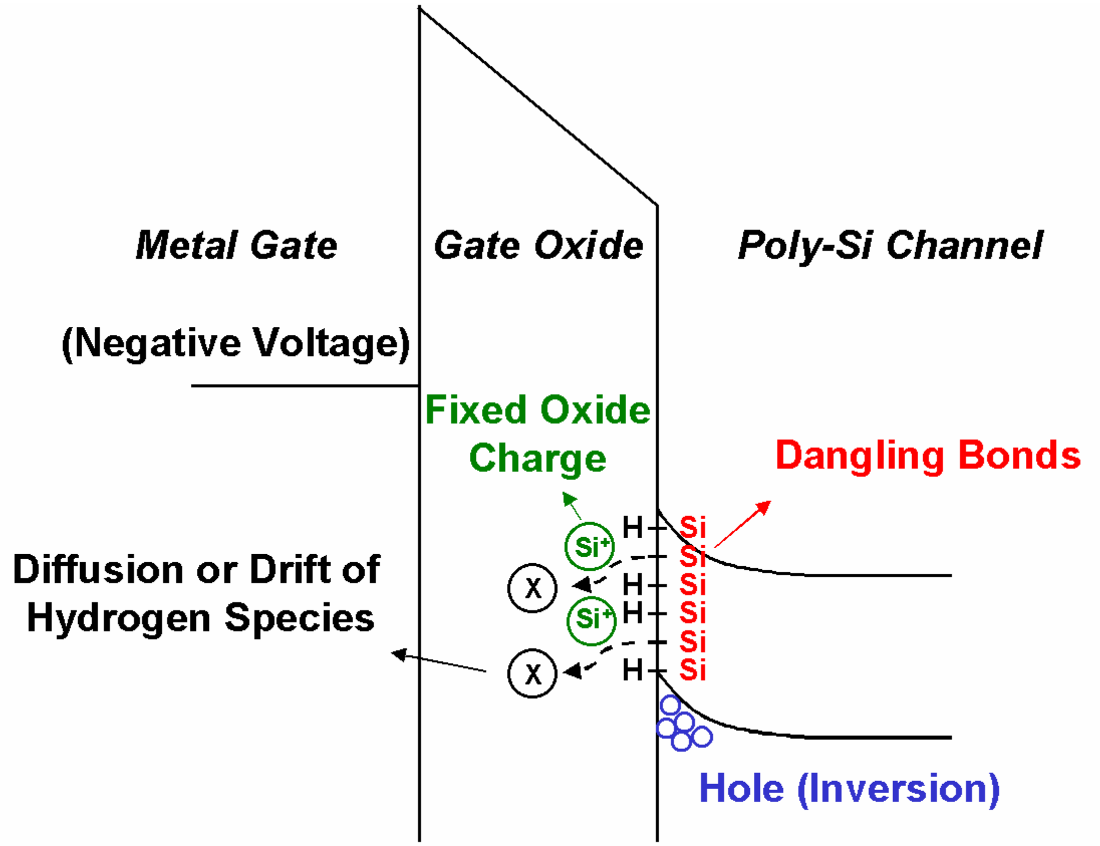


Fig. 2-12. Energy band diagram of p-channel LTPS TFT under NBTI stress.

Chapter 3

Plasma Damage Enhanced Negative Bias Temperature Instability in Low Temperature Polycrystalline Silicon Thin Film Transistors

3.1 Introduction

Recently, low temperature polycrystalline silicon thin film transistors (LTPS TFTs) have attracted much research interest. Due to its' high carrier mobility, the integration of driving circuits and pixels on a glass substrate can be performed, realizing system on panel (SOP) [1]. To achieve good process repetitiousness and precisely controlled of feature sizes, plasma process has been widely used in the manufacture of ULSI and LTPS TFTs. However, plasma damage has been reported to degrade the performance and reliability in thin film transistors [2]-[4].

In p-channel metal-oxide-semiconductor field effect transistors (PMOSFETs), negative bias temperature instability (NBTI) has been widely studied and found to be an important reliability issue [5] [6]. Additionally, it has been reported that plasma damage leads to severe NBTI in PMOSFETs [7]-[10]. In thin film transistors, several researchers have showed NBTI occurs as well as in PMOSFETs [11] [12]; however, the correlation between plasma damage and NBTI in LTPS TFTs has not been explored.

The purpose of this study was to investigate the effect of plasma damage on the NBTI behaviors in LTPS TFTs. Devices were designed with various antenna structures, and NBTI stress was performed on the devices to inspect the effect of plasma damage.

3.2 Experimental

P-channel LTPS TFTs were fabricated on glass substrates in this study. First, a 40nm-thick amorphous-Si layer was deposited and crystallized into poly-Si film by excimer laser annealing. After defining the active region, the gate dielectric was deposited with an equivalent 100nm-thick SiO_2 layer. Then, Mo was deposited and patterned as the gate electrode. Following source/drain formation, inter-layer dielectric was deposited and densified. Finally, inter-connection metal was deposited and patterned. The channel length (L) and width (W) of the devices mainly used were 10 and 20μm, respectively. The metal pads attached to the gate were designed with antenna area ratio (AR) of 100, 500 and 1000. The AR is defined as the ratio between antenna area and gate area on active region ($L\times W$). The schematic cross-section diagram of the test structure is shown in Fig. 3-1. NBTI stress was performed at 150°C, and stress voltage of -30V was applied to the gate with source/drain grounded.

3.3 Results and Discussion

Figure 3-2 shows NBTI induced transfer characteristic degradation for the LTPS TFTs with AR of 100, 500 and 1000, respectively. We found that NBTI stress will make the threshold voltage (V_{th}) shift to negative direction and simultaneously degrade the subthreshold swing ($S.S.$); additionally, the effects are getting worse for the devices with larger AR. According to the results shown in Fig. 3-2, it is reasonable to assume that the NBTI effects are highly correlated to the plasma damage in LTPS TFTs. The correlations can be further observed from the threshold voltage shift (ΔV_{th})

vs. the stress time for the LTPS TFTs with different AR drawn in Fig. 3-3, which significantly presents a fact that a larger AR do induce a greater ΔV_{th}. It has been demonstrated that the NBTI induced V_{th} shift in MOSFET is mainly caused by the generation of interface states and fixed oxide charges [5] [6]. In highly matching with the NBTI phenomena in LTPS TFTs, we can speculate that the plasma damage enhances threshold voltage shift due to higher generation rate of interface states and fixed oxide charges. Compared with theΔV_{th}, the on current (I_{ON}) degradation rates revealed in Fig. 3-4 present the same trend that confirms the proposed mechanisms.

It is well known that the ΔV_{th} of PMOSFETs under NBTI stress shows a power law dependence on the stress time, which can be explained by the diffusion-controlled electrochemical reactions [13] [14]. From the Fig. 3-5, we found that the ΔV_{th} of LTPS TFTs under NBTI stress also follows similar dependency on the stress time. Figure 3-6 exhibits the extracted exponent factors (n) for LTPS TFTs with different AR; it presents an interesting result that the value of n is getting larger for the device with higher AR. This result indicates that the plasma damage accelerates NBTI degradation in LTPS TFTs.

Figures 3-7 and Fig. 3-8 compares ln [I_{DS}/ (V_{GS}-V_{FB})] vs. 1/ $(V_{GS}-V_{FB})^2$ curves for the fresh and NBTI stressed LTPS TFTs with AR of 100 and 1000. The grain boundary trap state density (N_{trap}) can be estimated by Levinson and Proano method [15] [16]. Form the figure, it is found that N_{trap} is increased from 7.8×10^{11} to 1.5×10^{12} (cm^{-2}) for the device with AR of 100, and from 9.1×10^{11} to 1.3×10^{12} (cm^{-2}) for the device with AR of 1000. In summary, the overall generation rate of N_{trap} is enhanced for devices with larger AR; this signifies that plasma damage enhances NBTI not only through the previously mentioned mechanisms, but also by accelerating the generation rate of grain boundary trap states.

Table 3-1 compares the parameter variation of LTPS TFTs with AR of 100, 500 and 1000 under 1000 sec NBTI stress. As AR increases, the device shows more degradation in field effect mobility (μ_{eff}), *S.S.* and V_{th}. This implies that the plasma damage enhances NBTI stress by increasing the generation rate of both interface states and fixed oxide charges. Moreover, plasma damage also enhanced the generation rate of N_{trap} under NBTI stress. It could be concluded that the plasma damage is an important factor for NBTI degradation in LTPS TFTs.

3.4 Summary

In this study, we have confirmed that plasma damage is a significant factor for NBTI in LTPS TFTs. The experimental results show that the consequence of plasma damage will be presented under NBTI stress. The accelerating phenomena is mainly attributed to the generation rate increment of interface states, grain boundary trap states and fixed oxide charges. Therefore, in sustaining the LTPS TFTs with both the high reliability and yield, the antenna structures must be carefully designed.

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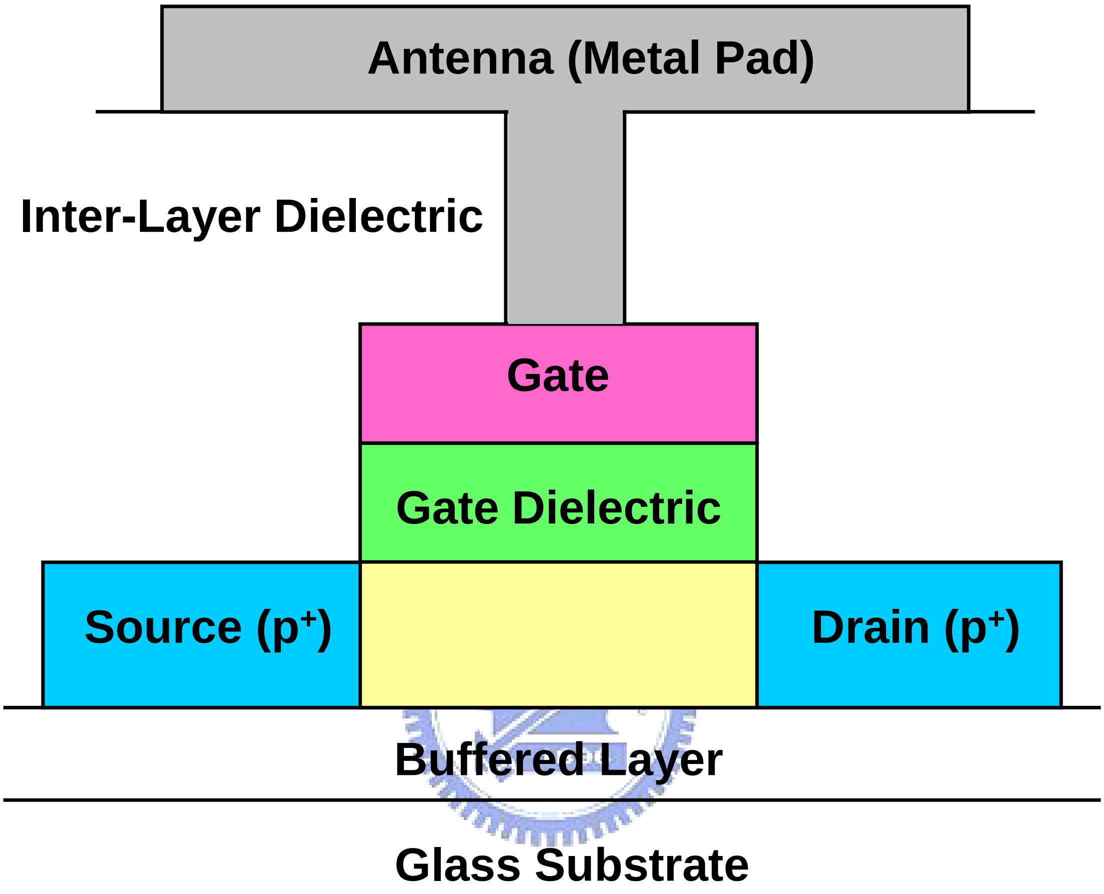

Fig. 3-1 The schematic cross-section diagram of the test LTPS TFT structure.

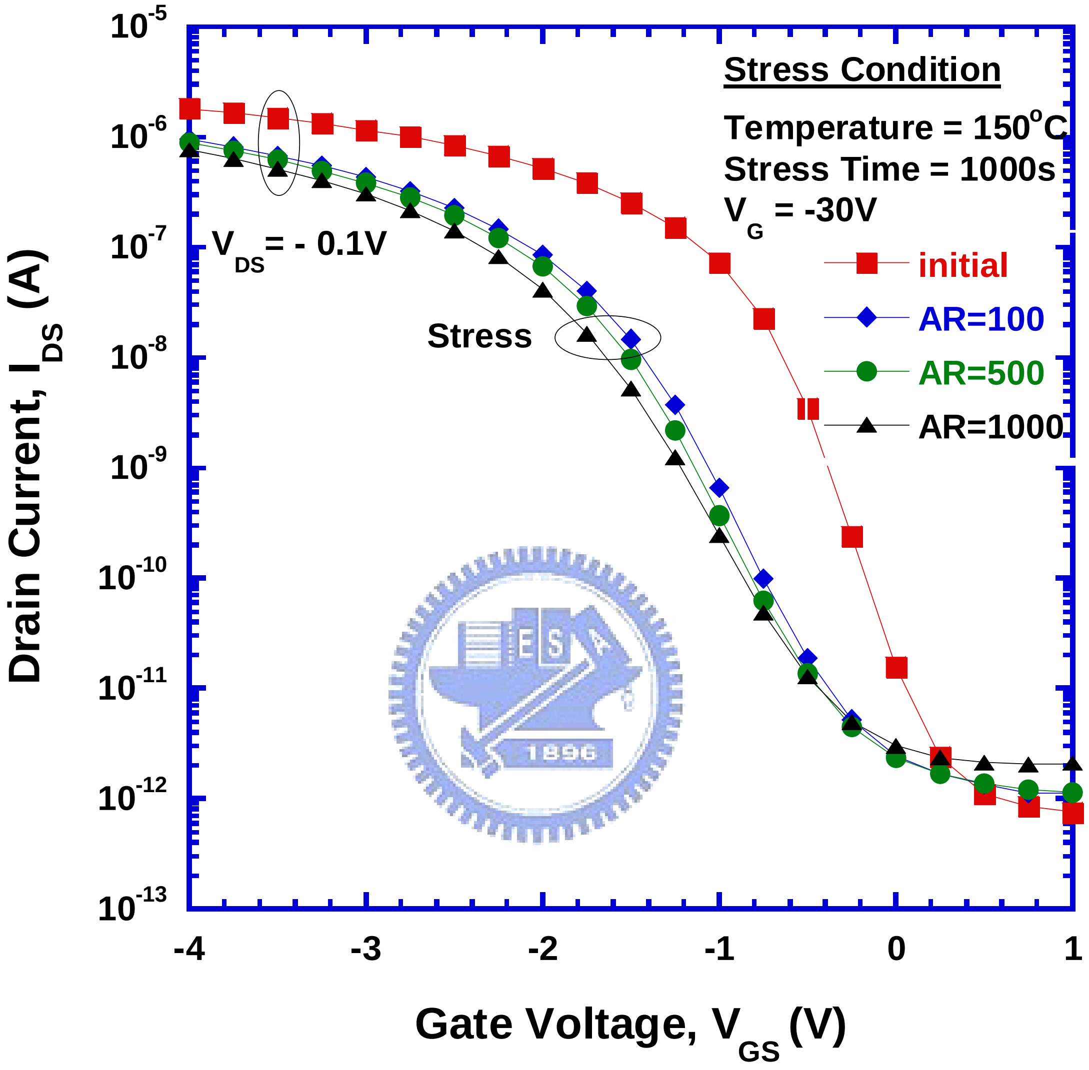

Fig. 3-2 Transfer characteristics of LTPS TFT with AR of 100, 500 and 1000 before and after 1000sec NBTI stress.

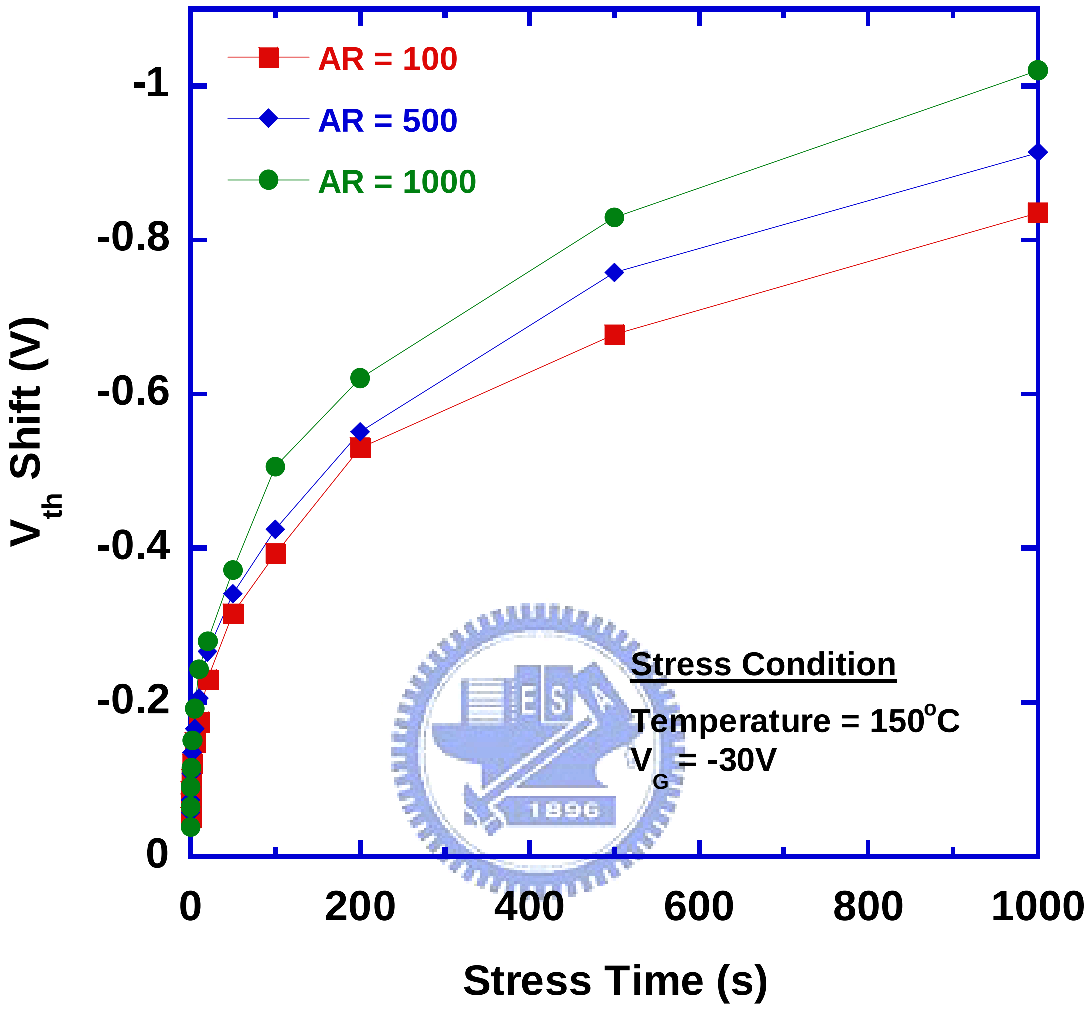

Fig. 3-3 Dependence of threshold voltage shift on the stress time of LTPS TFTs with AR of 100, 500 and 1000.

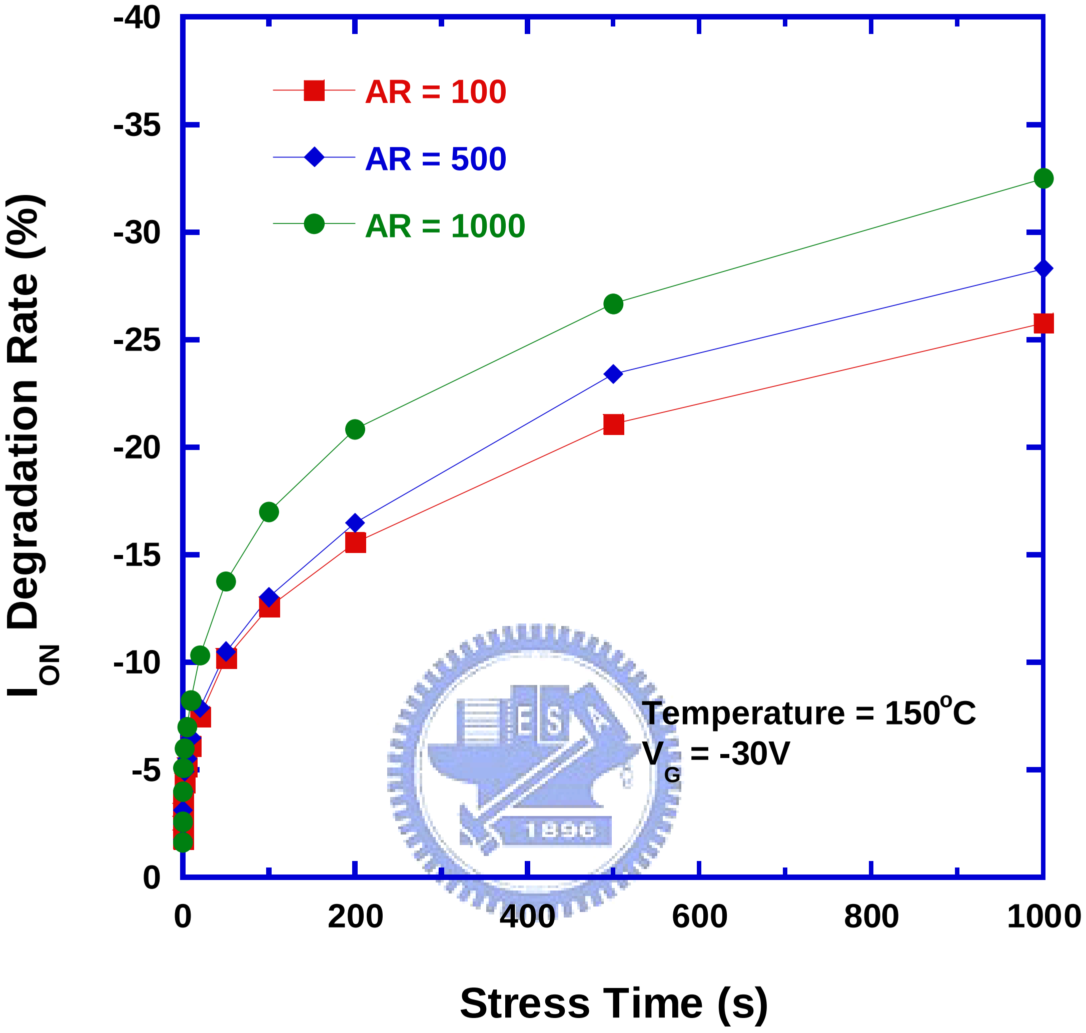

Fig. 3-4 Dependence of on current degradation rate on the stress time of LTPS TFTs with AR of 100, 500 and 1000.

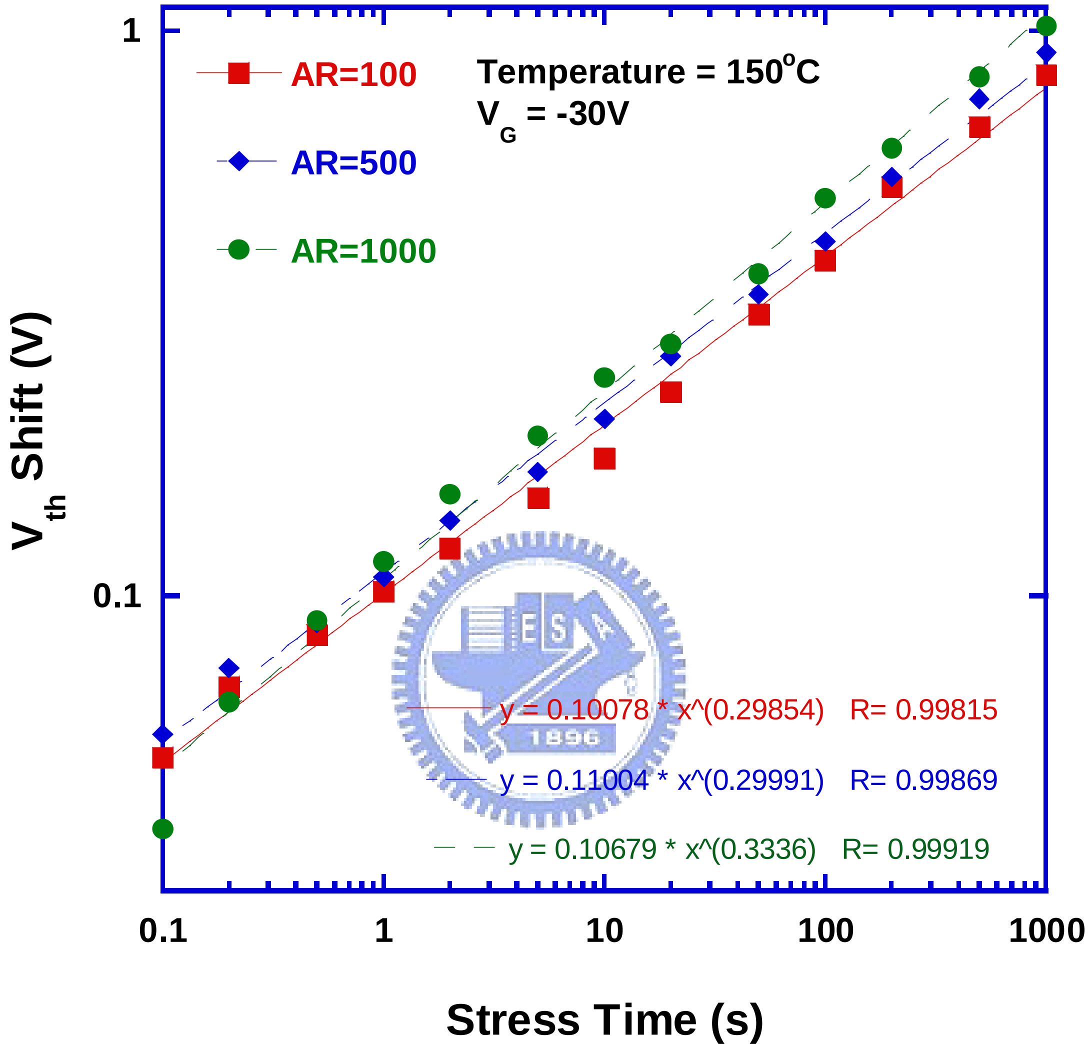

Fig. 3-5 The linear fit of the log-log plot of the threshold voltage shift versus the stress time of LTPS TFTs with AR of 100, 500 and 1000 under NBTI stress.

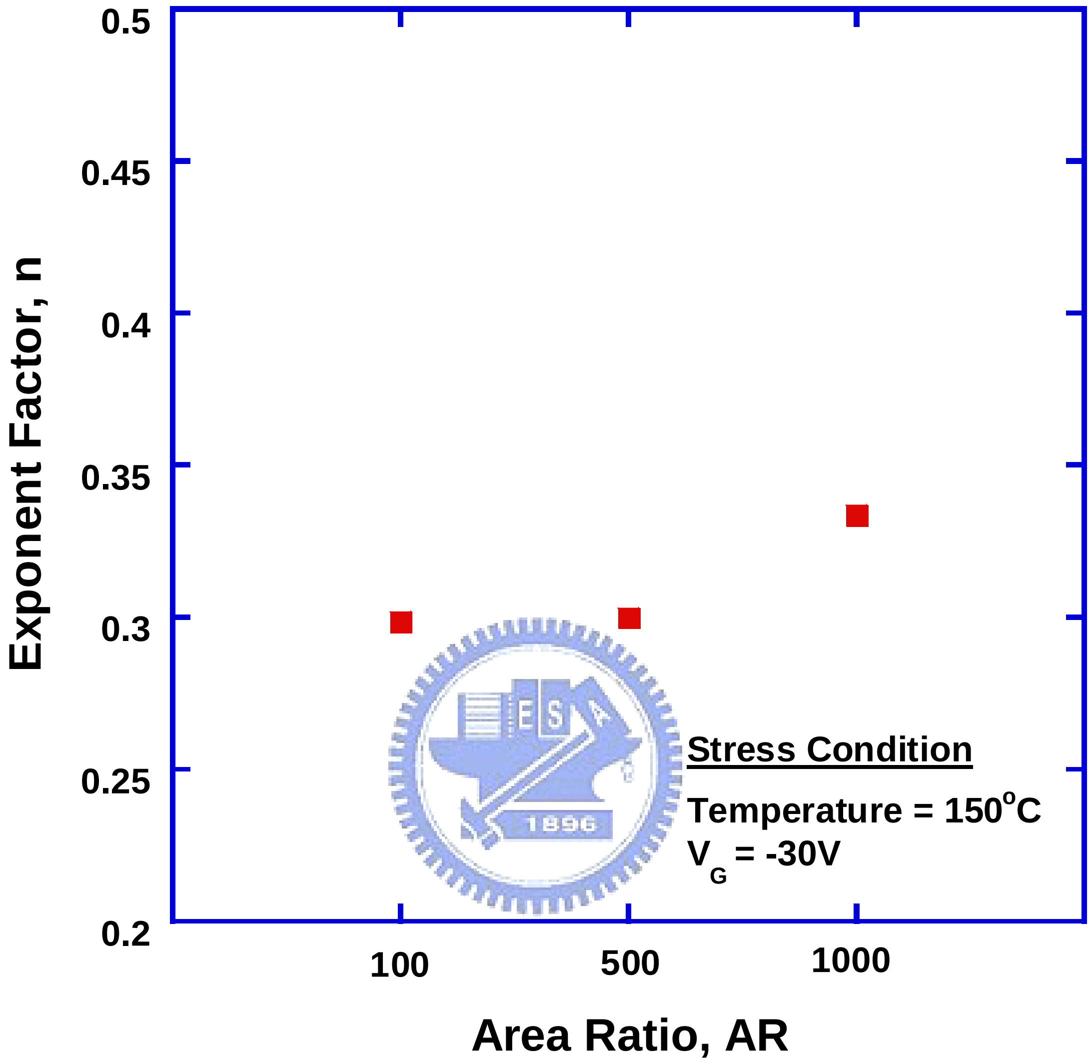

Fig. 3-6 Exponent factor *n* of LTPS TFTs with various AR.

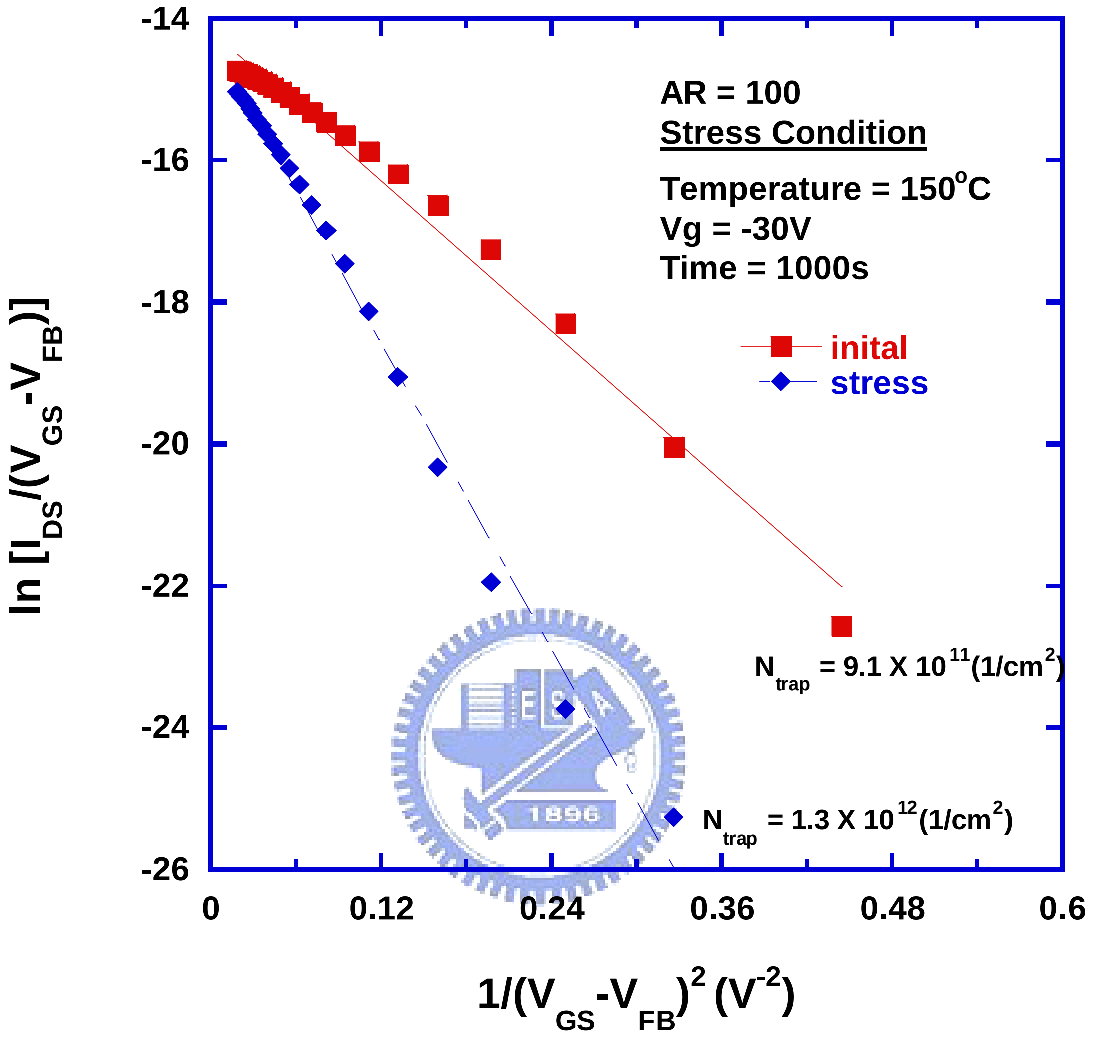

Fig. 3-7 Extraction of grain boundary trap state density of LTPS TFTs with AR of 100 before and after 1000 sec NBTI stress.

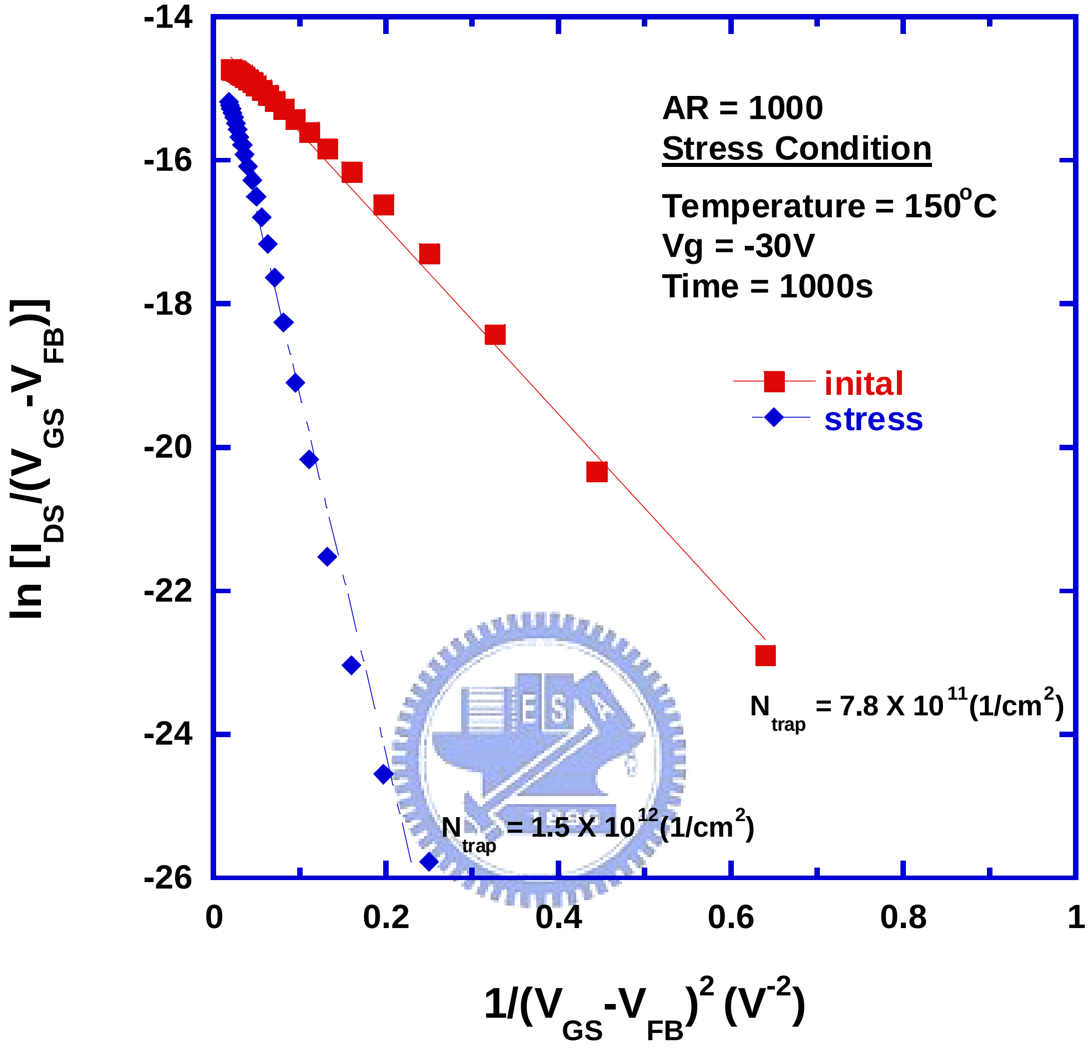

Fig. 3-8 Extraction of grain boundary trap state density of LTPS TFTs with AR of 1000 before and after 1000 sec NBTI stress.

Table 1

	AR=100	AR=500	AR=1000
$\triangle\mu_{eff}$ (%)	-6.7	-7.9	-9.0
$\triangle S.S.$(%)	52.3	64.2	78.7
$\triangle V_{th}$ (V)	-0.84	-0.91	-1.02
$\triangle I_{ON}$ (%)	-25.8	-28.3	-32.5
$\triangle N_{trap}$(%)	42.7	67.8	96.3

Table 3-1 Comparison of parameter variation of LTPS TFTs with AR of 100, 500 and 1000 after 1000 sec NBTI stress.

Chapter 4

Combined Negative Bias Temperature Instability and High Current Injection Stress Effects in Low Temperature Poly-Si Thin Film Transistors

4.1 Introduction

Low temperature poly-Si thin film transistors (LTPS TFTs) are now widely investigated for their potential application in active matrix liquid crystal displays (AMLCDs) and realization of system on panel (SOP). For the LTPS TFTs to be used in advanced analog and mixed signal circuit, the electrical stability becomes an important issue. In the pervious studies, NBTI induced device parameter degradation is a serious reliability concern in advanced analog and mixed signal technologies. NBTI induced threshold voltage shifts in p-channel TFTs is a critical issue for these analog circuits. To determine maximum threshold voltage (V_{th}) shift in an analog circuit over its operating lifetime, several factors that influence the conventional DC lifetime projection method need to be considered. Factors such as operating gate and drain voltage impact the DC lifetime extracted from conventional reliability measurements.

In this chapter, V_{th} shift due to NBTI and hot carrier injection (HCI) stress in p-channel LTPS TFTs is examined. It is observed that V_{th} shift are much greater under HCI stress conditions of $V_g = V_d = V_{stress}$ than under NBTI stress conditions of $V_g = V_{stress}$, $V_d = 0$. This is indicating a greater degree of trap generation under HCI stress.

Moreover, due to the poor conductivity of the buffer oxide, we suppose the temperature dependency of HCI stress induced degradation is an important reliability concern in LTPS TFTs, and compared with NBTI stress.[2] To quantify the combined NBTI and HCI induced degradation, we proposed a modified model based on the empirical NBTI and HCI models, and the experimental results conformed to the model. Therefore, we can clearly identify the combined NBTI and HCI effects on p-channel LTPS TFTs.

4.2 Experimental

P-channel LTPS TFTs fabricated on glass substrates were used in this work. A 40nm-thick amorphous silicon layer was deposited on a buffer layer by PECVD at 300°C. The silicon layer was then crystallized into polycrystalline silicon film by excimer laser annealing. Gate dielectric was deposited with an equivalent 100nm-thick SiO_2 layer and followed by Mo deposition as the gate electrode. After gate patterning, source and drain were doped by plasma doping. Then, the inter-layer dielectric was deposited and densified. Finally, inter-connection metal was deposited and patterned. Both the channel length (L) and width (W) of the device used in this work were 20μm.

The NBTI stress was performed with V_G of -20V, and the stress temperature was kept at 25 or 100°C. The V_{DS} was varied from 0 to -20V to study the combined NBTI and HCI stress effects on the device degradation. The threshold voltage (V_{th}) was measured under the criterion of $I_{DS} = (W/L) \times 10\text{nA}$ at $V_{DS} = -0.1\text{V}$. The schematic cross-section view of the LTPS TFT and the stress setup is shown in Fig. 4-1.

4.3 Results and Discussion

Figure 4-2(a) and (b) show the variations of transfer characteristics of the LTPS TFTs before and after stress. The stress was performed with V_{GS} of -20V, and V_{DS} of 0 or -20V. In Fig. 4-2(a), the device was stressed with source/drain grounded, so the device degradation was most caused by NBTI. This can be confirmed by the negative shift of V_{th} in Fig. 4-2(a), which is a typical characteristic of NBTI. In Fig. 4-2(b), V_{DS} of -20V was applied, as well as the V_{GS}, the effect of HCI stress must be considered. We supposed the device degradation as shown in Fig. 4-2(b) is caused by the combined NBTI and HCI stress effects. Unlike Fig. 4-2(a), the transfer characteristic in Fig. 4-2(b) shows severe degradation in the subthreshold swing (*S.S.*) after stress, indicating more interface states were generated by HCI.

Figure 4-3 reveals the ΔV_{th} of the devices after various stress conditions. The stress was performed with fixed V_{GS} of -20V and V_{DS} ranging from 0 to -20V, and the temperature was kept at 25 or 100^{o}C. The ΔV_{th} exhibits two degradation regimes. In the low V_{DS} regime, the ΔV_{th} decreases as V_{DS} increases to negative; while in the high V_{DS} regime, the ΔV_{th} increases with V_{DS}. At V_{DS} = 0V, the device degradation is primarily caused by NBTI. As V_{DS} increases from 0 to -2.5V, the ΔV_{th} slightly decreases. This decrease of ΔV_{th} implies NBTI was suppressed when V_{DS} is biased at low voltage. As V_{DS} continuously increases to -20V, the ΔV_{th} increases. The rise of ΔV_{th} with V_{DS} can be explained by the enhanced generation of hot carriers, especially for the stress condition of $V_{DS} = V_{GS} = -20V$.

From Fig. 4-3, the ΔV_{th} is found to larger for the devices stressed at 100^{o}C than those stressed at 25^{o}C. In the low V_{DS} regime, the ΔV_{th} is mainly caused by NBTI. Furthermore, NBTI has been reported to be thermally accelerated and thereby the ΔV_{th} is larger for the devices stressed at 100^{o}C in the low V_{DS} regime [5][6]. In the high V_{DS}

regime, the ΔV_{th} is dominated by HCI. The enlarged ΔV_{th} at 100°C can be explained by the enhanced hole injection, because both the vertical field and the thermal excitation are accelerated at higher temperature [7].

To quantify the combined effects of NBTI and HCS as we speculated above, both the empirical models for NBTI and HCS will be discussed. In the conventional NBTI stress, only the gate voltage was applied to the gate with source/drain grounded, and the ΔV_{th} can be modeled as [8]

$$\Delta V_{th} = At^n \exp(-\frac{E_a}{kT})\exp(C|V_G|) = A'\exp(C|V_G|) \quad \text{-----------------------------} \quad \text{(Eq. 4.1)}$$

where $A' = At^n exp(-E_a/kT)$ and can be calculated from the experimental results. In our stress condition, instead of grounded drain, a V_{DS} was applied; thus the conventional NBTI degradation model must be modified to be used in our case. As we can see from (Eq. 4.1), the ΔV_{th} is a function of V_{GS} (or the electrical field across the gate dielectric). We assumed that $V(y)$ is the hole quasi-Fermi potential at a point y along the channel with respect to the Fermi potential of the p^+ source. At low V_{DS}, $V(y)$ varies almost linearly between the source and drain [9]. Thus $V(y)$ can be concisely expressed as

$$V(y) = \left(\frac{y}{L}\right) \times V_{DS} \quad \text{---} \quad \text{(Eq. 4.2)}$$

And the ΔV_{th} can be rewritten as

$$\begin{aligned}
\Delta V_{th} &= A'\frac{1}{L}\int_0^L \exp[C(|V_{GS}| - |V(y)|)]dy \\
&= \frac{A'}{L}\exp(C|V_{GS}|)\int_0^L \exp[C(-\frac{y}{L}|V_{DS}|)]dy \\
&= \frac{A'}{C|V_{DS}|}\exp(C|V_{GS}|)[1-\exp(-C|V_{DS}|)] \quad \text{----------------------------------} \quad \text{(Eq. 4.3)}
\end{aligned}$$

This simple and analytic model can be used to interpret the NBTI effect under low V_{DS} bias. For the HCI stress in our experiment (high V_{DS}), the ΔV_{th} can be experimentally expressed as [10]

$$\Delta V_{th} = Bt^{n} \exp(-\frac{\alpha}{|V_{DS}|}) = B' \exp(-\frac{\alpha}{|V_{DS}|}) \text{ --- (Eq. 4.4)}$$

where $B' = Bt^{n}$ and can be calculated from the experimental results. The parameter α can be extracted from the experimental results as shown in Fig. 4-4(a).

By combining the ΔV_{th} in (Eq. 4.3) and (Eq. 4.4), the overall ΔV_{th} caused by NBTI and HCI stress can be predicted. Figure 4-4(b) and (c) show the predicted and measured ΔV_{th} as a function of the V_{DS} for stress temperatures of 100 and 25°C, respectively. The predicted ΔV_{th} consists of two components: NBTI and HCI stress, which dominate the degradation mechanism in low and high V_{DS} regime, respectively. As V_{DS} increases, the NBTI component decreases, while the HCI stress increases. The measured data follows the same trend as the model. This confirmed that the model we proposed can clearly identify the degradation mechanism of the combined NBTI and HCI stress effects.

Figure 4-5(a) and (b) show the degradation rate of field effect mobility (μ_{eff}) and *S.S.*, respectively. The two parameters have the same trend of degradation: as V_{DS} increases to negative, the degradation rates decrease firstly and then increase with the V_{DS}. Both the μ_{eff} and *S.S.* degradation reflect the interface states generation. At low V_{DS}, the interface states are mainly caused by NBTI; at high V_{DS}, the interface states are primarily generated by HCI stress. The interface state generation is also found to be severer for HCI than NBTI. As the stress temperature increases, the degradation rates are enhanced. This is due to the enhanced NBTI (at low V_{DS}) and accelerated hot hole injection (at high V_{DS}). Furthermore, the *S.S.* is closely related to the deep interface states (trap states located near the midgap), while the μ_{eff} is associated with the tail interface states (trap states located near the band edge) [11]. The deep states and tail states originate from the dangling bonds and strain bonds, respectively. From the experimental results, the degradation of *S.S.* is found to be severer than μ_{eff}

degradation, especially at high V_{DS}; therefore, we can conclude the interface states generated by NBTI or HCI are mainly attributed to the dangling bonds formation.

Figure 4-6 shows the on current (I_{ON}) degradation rate as a function of V_{DS} with fixed V_{GS} of -20V. Two kinds of measurement modes were used to study the instability mechanism: forward and reverse modes. In the forward mode, a voltage was applied to the drain with the source grounded; while in the reverse mode, the roles of source and drain were switched. At low V_{DS}, both the forward and reverse mode I_{ON} degradation rates show slightly difference, indicating the NBTI induced degradation is uniform in the channel. As V_{DS} increases, the I_{ON} degradation rate in the reverse mode is larger than that in the forward mode, signifying the damage caused by HCI stress is mainly located in the drain side. As the stress temperature rises, the I_{ON} degradation rate increases. This is due to the thermally enhanced NBTI and HCS stress effect at elevated temperature.

Figure 4-7(a) shows the ΔV_{th} versus the stress time with various V_{DS} at 25°C. The ΔV_{th} follows a power law dependence on the stress time ($\Delta V_{th} \sim t^{n}$). The devices stressed at 100°C also shows the same power law dependence and thus not shown here. The exponent factors (n) were extracted and shown in Fig. 4-7 (b). The n values are larger for the devices stressed at 100°C than those stressed at 25°C. This means the device degradation rate is enhanced at elevated stress temperature. At V_{DS} = 0V, the n values are about 0.2 and 0.3 for the devices stressed at 25°C and 100°C, respectively. These values are consistent with the previous studies in NBTI, and this can be explained by the diffusion-controlled electrochemical reactions [12][13]. The experimental results confirm that the degradation under V_{DS} = 0V is caused by NBTI. As V_{DS} increases form 0V to -5V, the n values decrease. The smaller n value can be explained by the retarded NBTI due to the application of V_{DS}. The V_{DS} lowers the electrical field across the gate dielectric, thus the overall NBTI is suppressed as we predicted above. As V_{DS} increases to more negative, the degradation rate is dominated by HCI stress, thus the n values increase with the V_{DS}.

4.4 Summary

The device degradation mechanism under NBTI and HCI stress were studied in this work. P-channel LTPS TFTs were stressed with V_{DS} ranging form 0 to -20V and fixed V_{GS} of -20V. The ΔV_{th} exhibits two degradation regimes: in the low V_{DS} regime, the ΔV_{th} decreases as V_{DS} increases; in the high V_{DS} regime, the ΔV_{th} increases with V_{DS}. The reduction of ΔV_{th} in the first regime is due to the retarded NBTI, because the application of V_{DS} lowers the effective electrical field across the gate dielectric. The rise of ΔV_{th} with V_{DS} in the second regime is caused by the enhanced hot hole injection in to the gate dielectric. We proposed an analytic model to quantify the combined NBTI and HCI stress effects, and the experimental results conformed to the model. The device degradation increases with the stress temperature, and this is due to the enhanced NBTI and accelerated hot hole injection at elevated temperature. Furthermore, in the low V_{DS} regime, NBTI dominates the degradation and the stress induced damage is symmetric between source and drain, while in the high V_{DS} regime, the degradation is dominated by hot carrier, and the asymmetric degradation across the channel indicates the damage is located near the drain side. From the analysis of the experimental results and the model we proposed, the combined NBTI and HCI stress effects on p-channel LTPS TFTs can be clearly identified.

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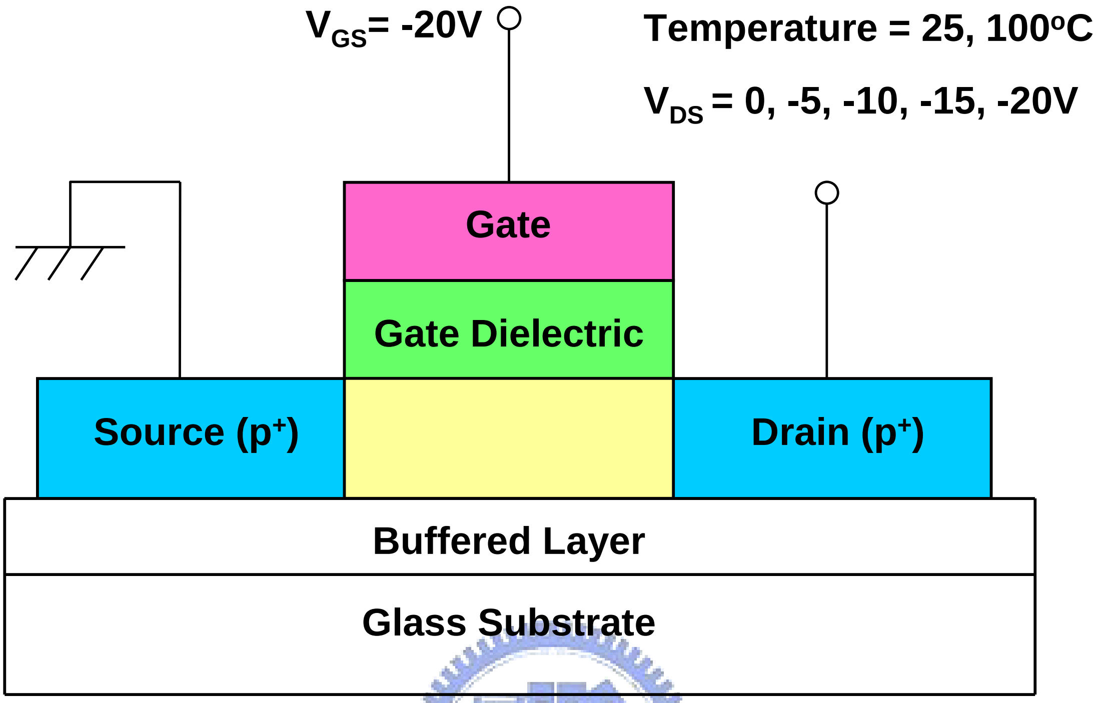

Figure 4-1 Schematic cross-section view of the LTPS TFT and the stress setup.

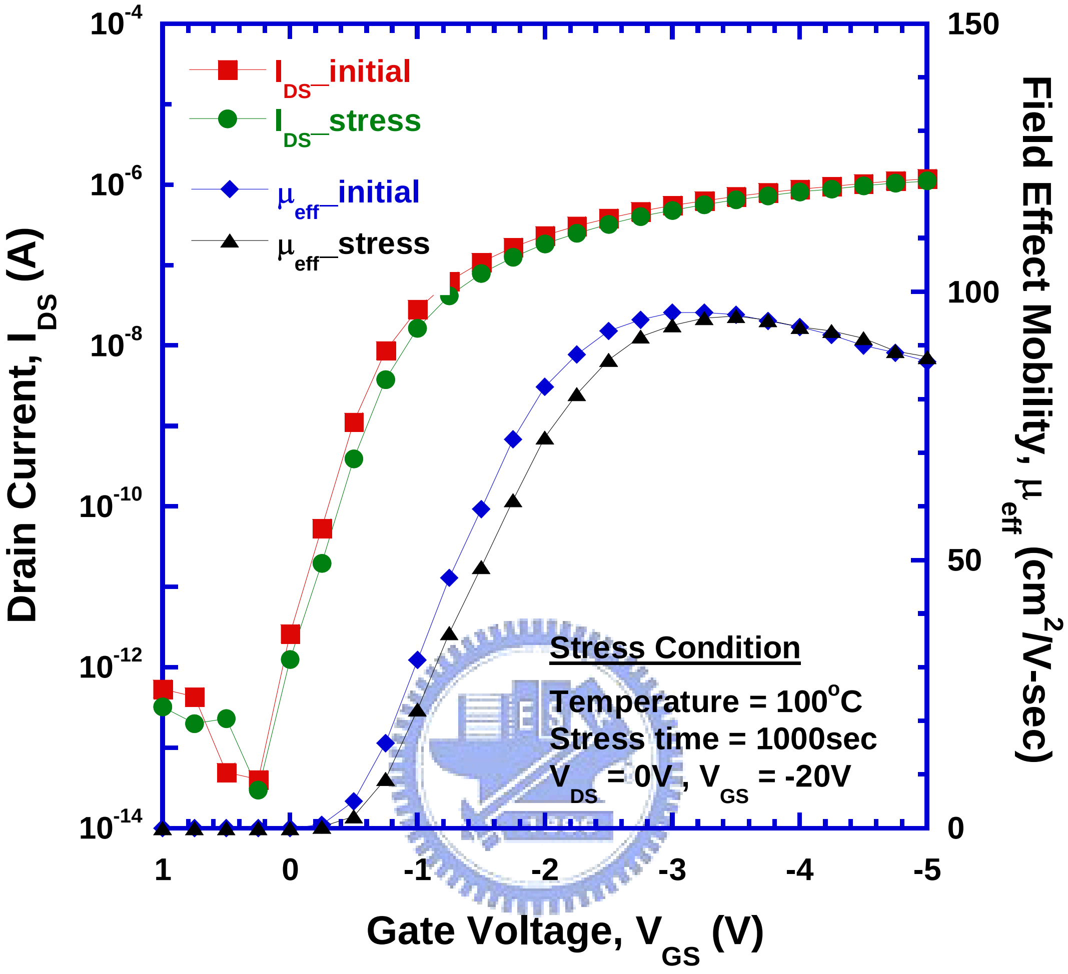

Figure 4-2(a) Transfer characteristics of the LTPS TFTs before and after stress. The stress was performed with V_{DS} of 0V and fixed V_{GS} of -20V.

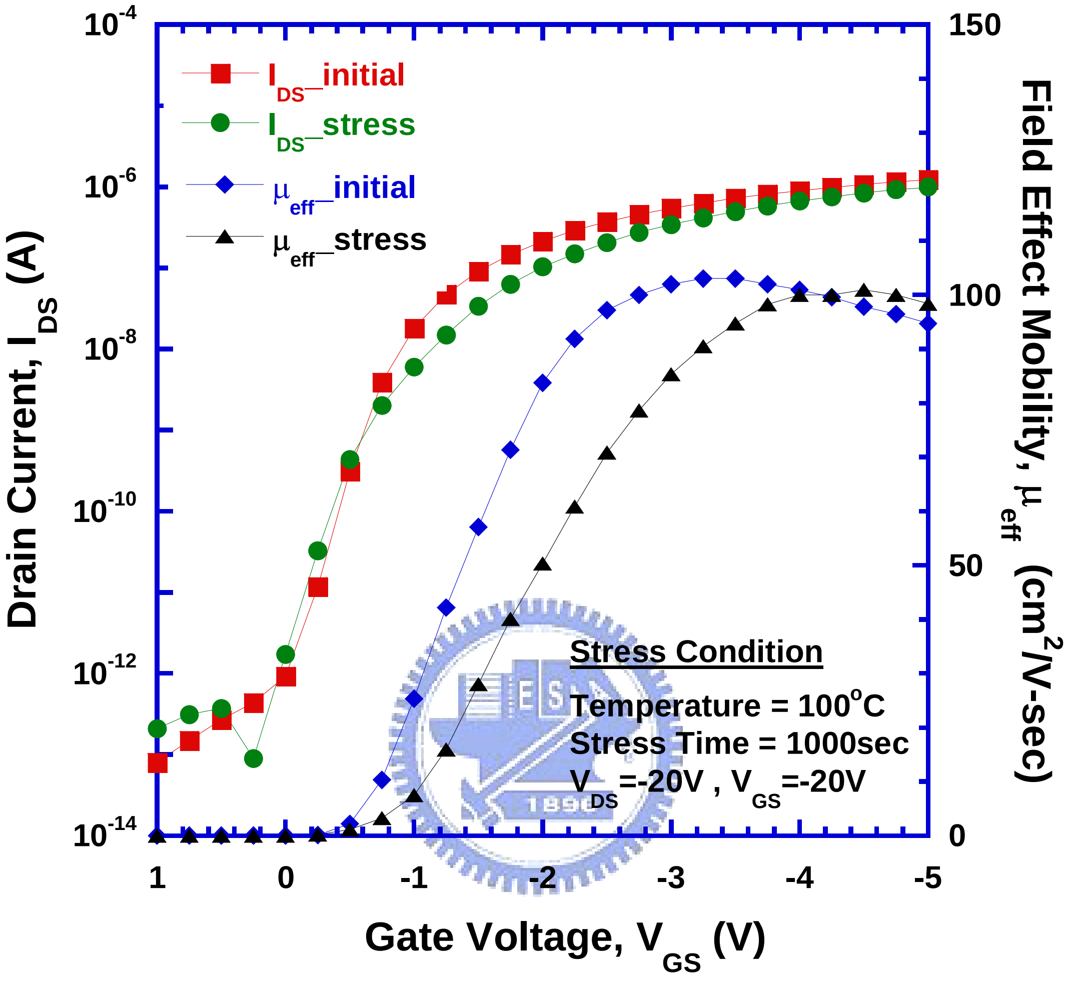

Figure 4-2(b) Transfer characteristics of the LTPS TFTs before and after stress. The stress was performed with V_{DS} of -20V and fixed V_{GS} of -20V.

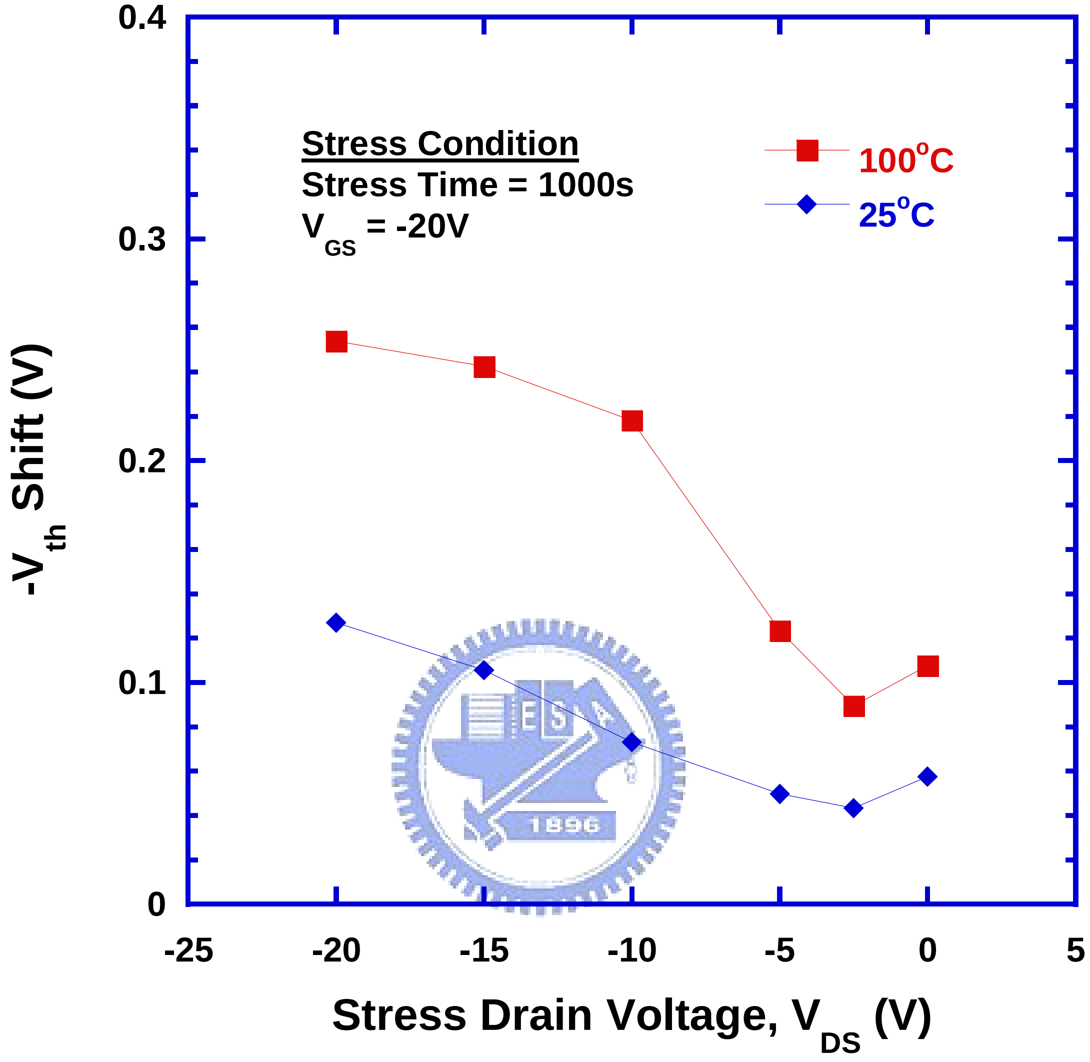

Figure 4-3 ΔV_{th} of the LTPS TFTs after various stress conditions. The stress was performed with fixed V_{GSs} of -20V and V_{DS} ranging from 0 to -20V, and the temperature was kept at 25 or 100°C.

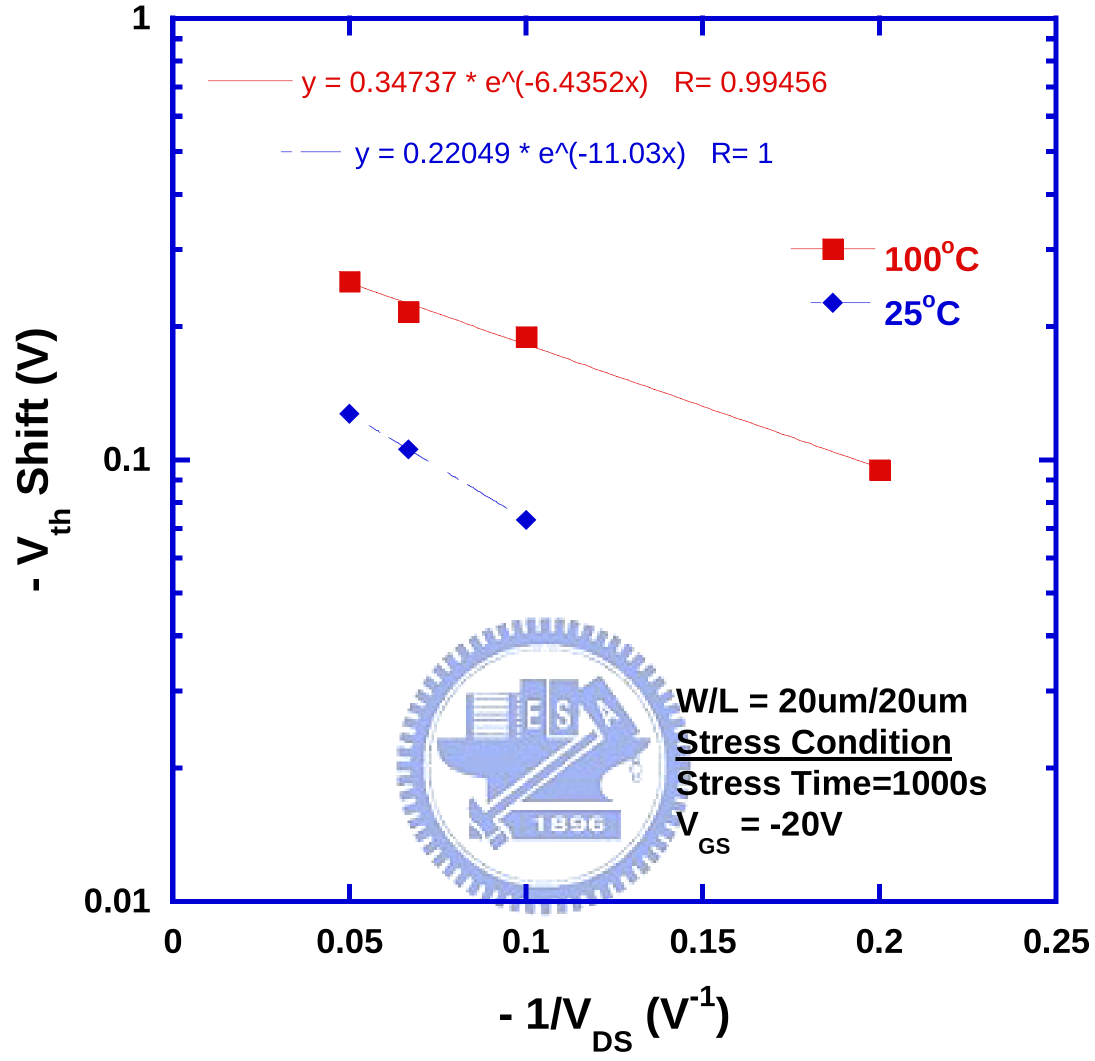

Figure 4-4 (a) Relationship between the magnitude of ΔV_{th} and V_{DS}.

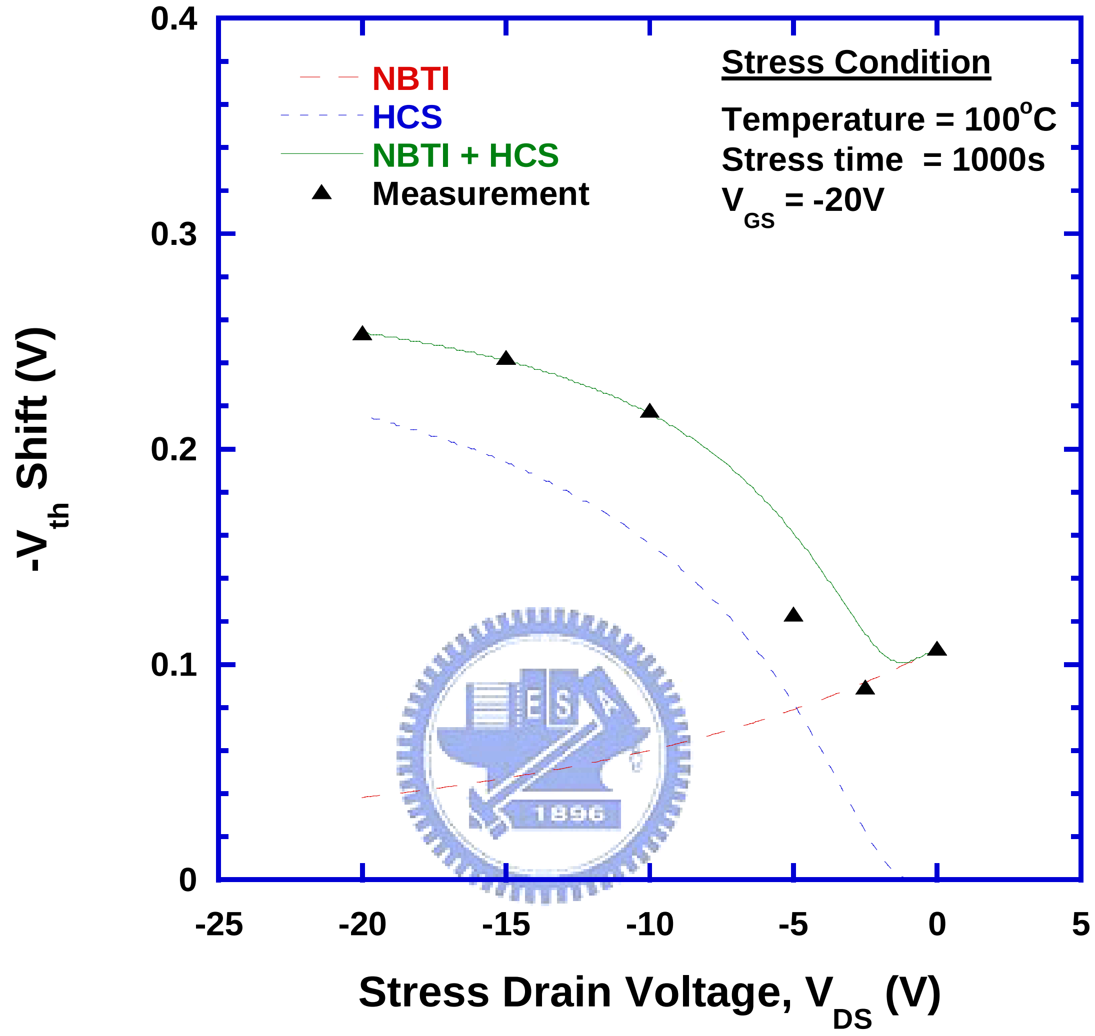

Figure 4-4(b) Comparison of the measured data with the predicted combined NBTI and HCS effects under 100°C stress.

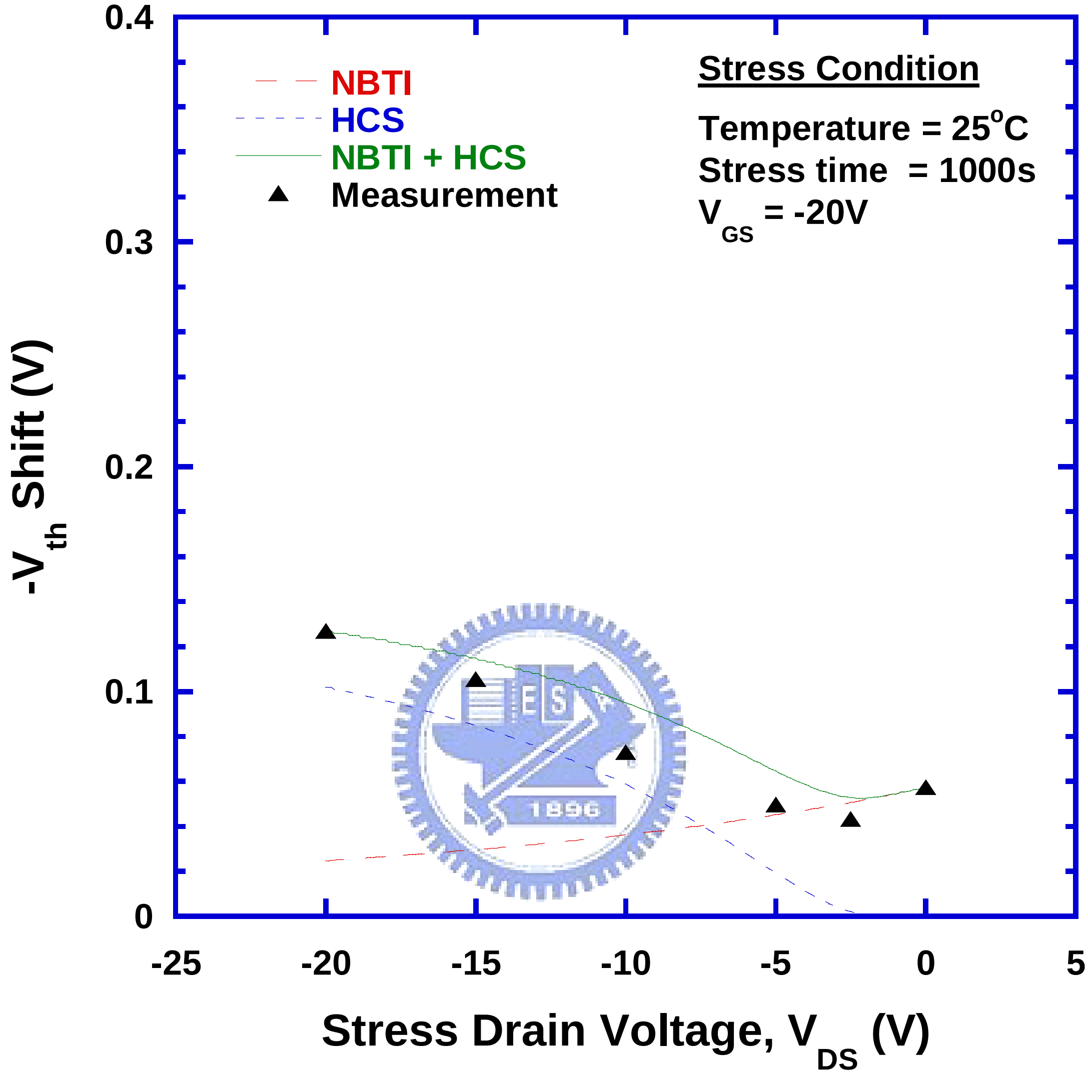

Figure 4-4(c) Comparison of the measured data with the predicted combined NBTI and HCS effects under 25°C stress.

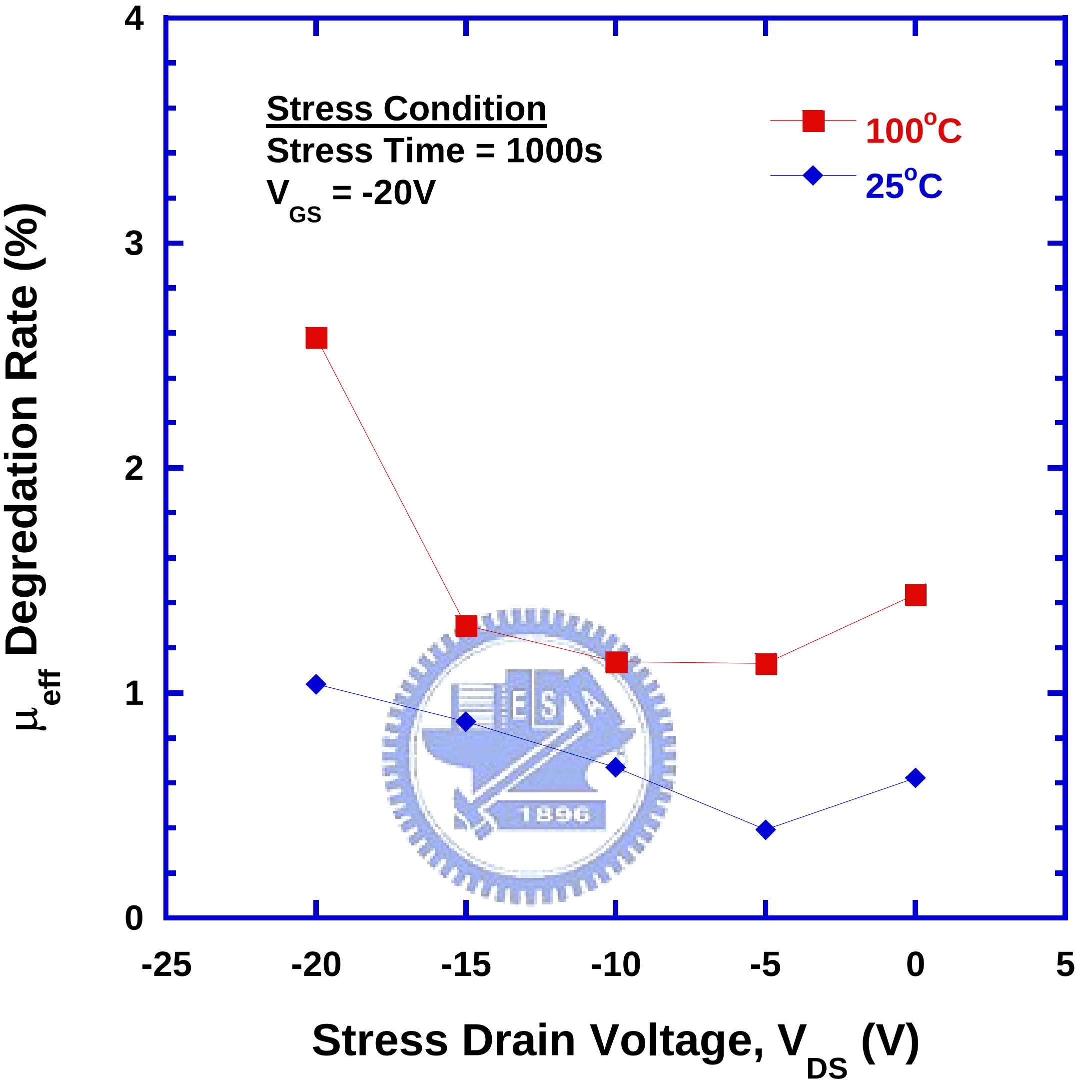

Figure 4-5(a) Degradation rates of field effect mobility as a function V_{DS}.

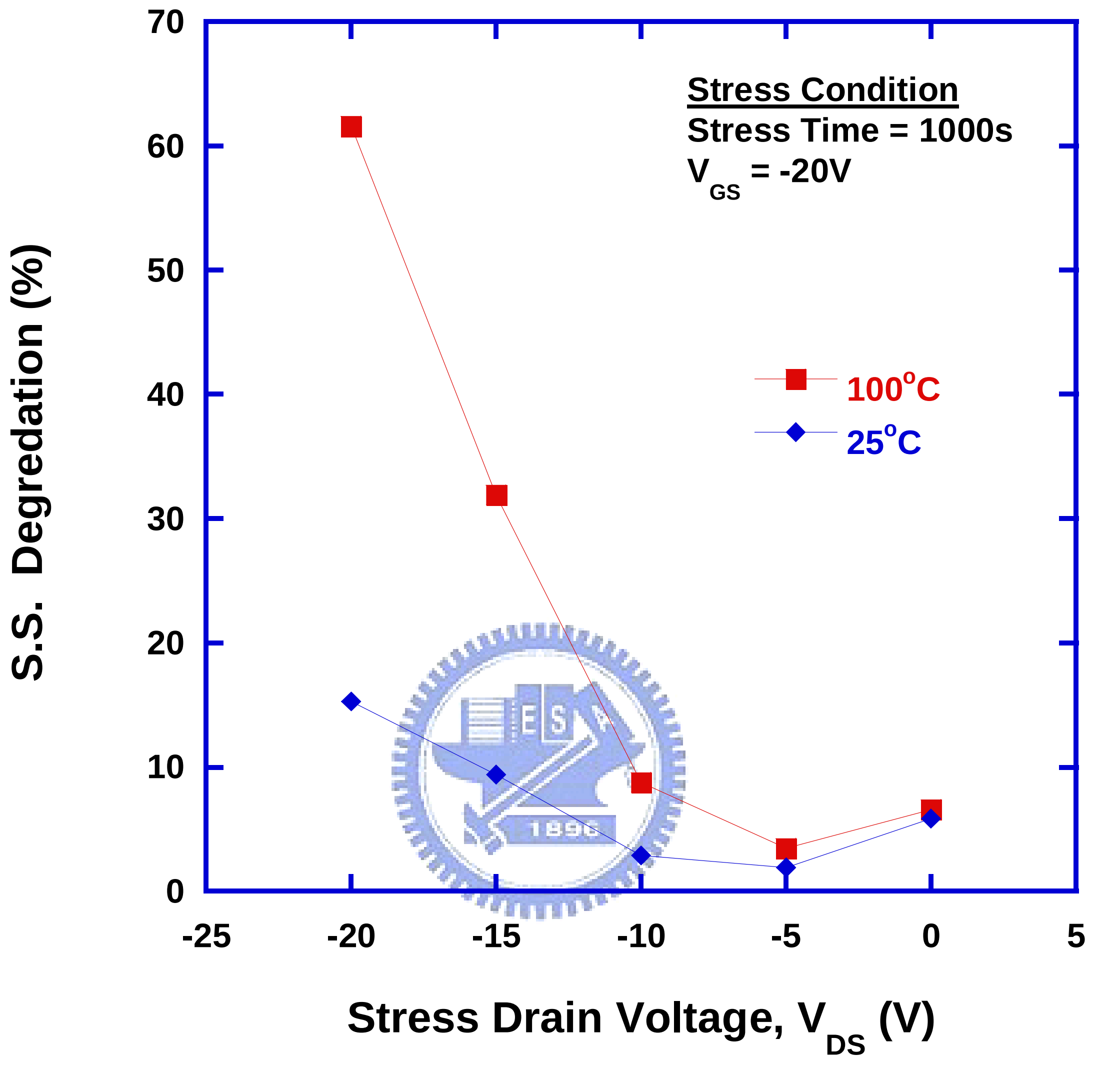

Figure 4-5(b) Degradation rates of subthreshold swing as a function V_{DS}.

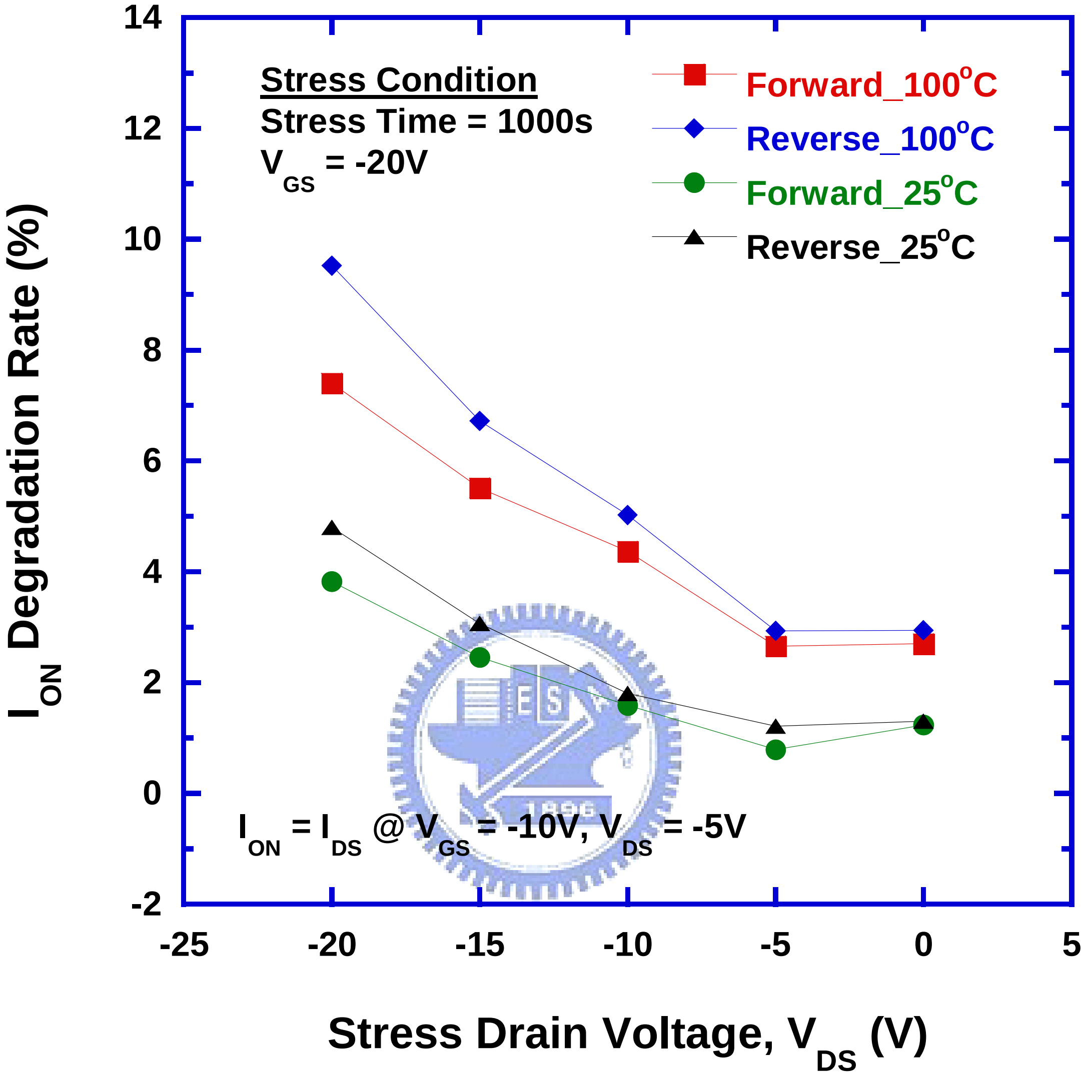

Figure 4-6 On current degradation rate as a function of V_{DS} with fixed V_{GS} of -20V.

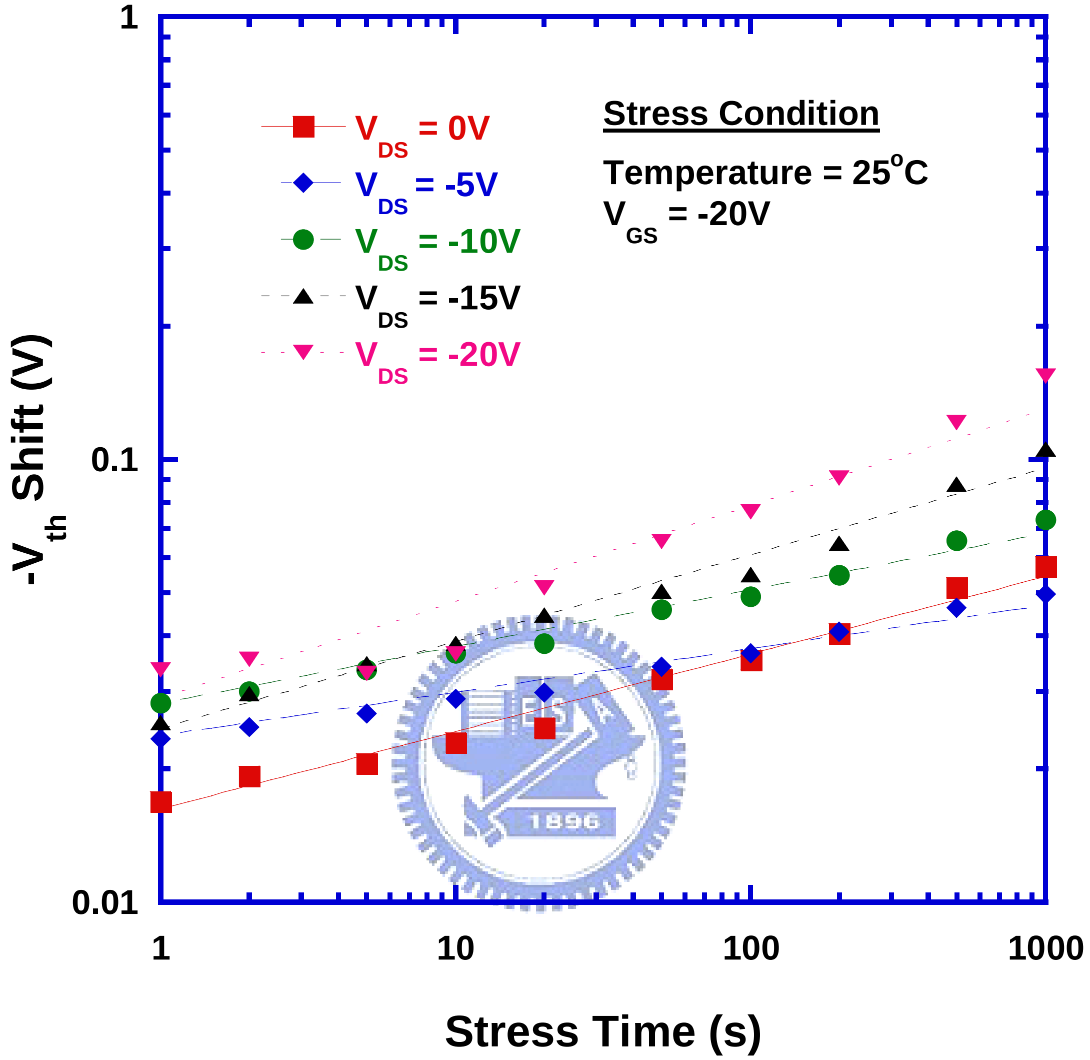

Figure 4-7 (a) Linear fitting of the log-log plot of the ΔV_{th} versus the stress time under 25°C stress condition.

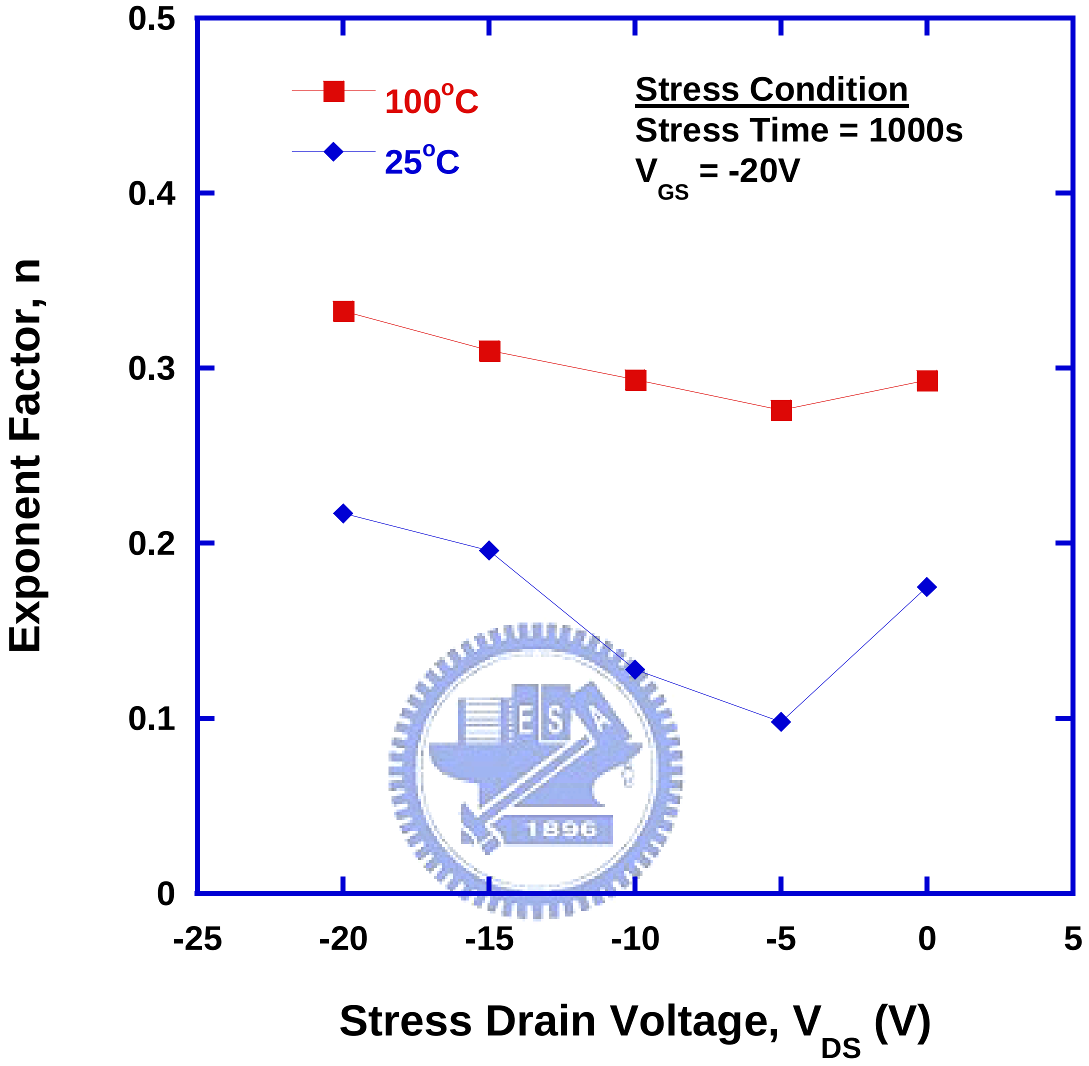

Figure 4-7(b) Comparison of the exponent factor with various V_{DS}.

Chapter 5

Conclusions

In this thesis, first, negative bias temperature instability of p-channel LTPS TFTs has been studied, and we have proved NBTI is important in the reliability of LTPS TFTs. It is found the threshold voltage, subthreshold swing, maximum transconductance and drive current of LTPS TFTs degrade after NBTI stress. The device degradation caused by NBTI stress increases with temperature and electric field, indicating NBTI can be thermally and electrically activated. Due to the grain boundaries in the channel regions of LTPS TFTs, the grain boundaries trap state generation must be considered during NBTI stress. In this study, it is proved the threshold voltage shift is closely related to the grain boundary trap state generation, because both the two physical quantities follow almost the same power low dependence on the stress time; moreover, exponential dependence on the stress voltage and reciprocal of the ambient temperature. The exponent value of the power law dependence on the stress time is about 1/4 to 1/3, which is explained by the diffusion-controlled electrochemical reactions. Besides threshold voltage shift, NBTI also leads to the degradation of subthreshold swing, driving current and hole mobility. From the experimental results, we concluded that NBTI is caused by the generation of fixed oxide charges, interface states and grain boundary trap states in LTPS TFTs. Furthermore, a physical model is proposed and verified by the experimental results.

Then, we have confirmed that plasma damage is a significant factor for NBTI in LTPS TFTs. The experimental results show that the consequence of plasma damage will be presented under NBTI stress. The accelerating phenomena is mainly attributed to the generation rate increment of interface states, grain boundary trap states and fixed oxide charges. Therefore, in sustaining the LTPS TFTs with both the high reliability and yield, the antenna structures must be carefully designed.

Finally, the device degradation mechanism under NBTI and HCI stress were studied. P-channel LTPS TFTs were stressed with V_{DS} ranging form 0 to -20V and fixed V_{GS} of -20V. The ΔV_{th} exhibits two degradation regimes: in the low V_{DS} regime, the ΔV_{th} decreases as V_{DS} increases; in the high V_{DS} regime, the ΔV_{th} increases with V_{DS}. The reduction of ΔV_{th} in the first regime is due to the retarded NBTI, because the application of V_{DS} lowers the effective electrical field across the gate dielectric. The rise of ΔV_{th} with V_{DS} in the second regime is caused by the enhanced hot hole injection in to the gate dielectric. We proposed an analytic model to quantify the combined NBTI and HCI stress effects, and the experimental results conformed to the model. The device degradation increases with the stress temperature, and this is due to the enhanced NBTI and accelerated hot hole injection at elevated temperature. Furthermore, in the low V_{DS} regime, NBTI dominates the degradation and the stress induced damage is symmetric between source and drain, while in the high V_{DS} regime, the degradation is dominated by hot carrier, and the asymmetric degradation across the channel indicates the damage is located near the drain side. From the analysis of the experimental results and the model we proposed, the combined NBTI and HCI stress effects on p-channel LTPS TFTs can be clearly identified.

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The Study of Negative Bias Temperature Instability in Low Temperature Polycrystalline Silicon Thin-Film Transistors

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