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電子工程學系　電子研究所碩士班

碩 士 論 文

一個用來改善形變通道N型金氧半場效電晶體熱載子可靠度的方法

A Novel Approach to Improve Hot Carrier Reliability of Strained-Channel NMOSFETs

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摘要

在本研究中，我們探討了使用薄緩衝層對於具有形變通道的 n-型深次微米電晶體的性能影響與可靠度分析。我們實驗發現，在氮化矽沉積前先沉積一層薄緩衝層(thin buffer layer)並不會使元件性能變差，這是使用薄緩衝層的優點之一。而沉積氮化矽覆蓋層時所帶來的熱預算(thermal budget)雖然可以降低界面的缺陷與減少逆短通道效應，然而卻會使多晶矽空乏現象變嚴重。在本研究中，我們分別探討了兩種緩衝層材質: 四乙氧基矽烷(TEOS)氧化矽與多晶矽。我們發現在形變元件中氫含量的多寡是影響元件可靠度最主要的因素。使用四乙氧基矽烷(TEOS)氧化矽緩衝層可以減緩沉積氮化矽的過程中氫擴散至閘極介電層的情形。另一方面，由於在沉積多晶矽緩衝層的過程中是使用含有氫的矽甲烷(SiH_4)先驅物(precursor)，所以多晶矽緩衝層沒有像四乙氧基矽烷(TEOS)緩衝層一樣佳

的阻隔效果。當元件含有氮化矽覆蓋層來增進其驅動電流時，熱載子退化效應會被嚴重地劣化，然而我們也證實：在氮化矽沉積前先沉積一層緩衝層，可以有效改善熱載子退化效應。

A Novel Approach to Improve Hot Carrier Reliability of Strained-Channel NMOSFETs

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Abstract

In this work, the effect of a thin buffer layer inserted between the gate and a SiN capping layer on the performance and reliability of deep-submicron n-channel MOS transistors with strained channel was studied. It is found that the insertion of a thin buffer layer would not degrade the device performance, which is important for the adoption of the approach to the mainstream ULSI manufacturing. The thermal budget associated with the deposition of the SiN capping layer could reduce the amount of interface states and alleviate the reverse short-channel effect, although the poly-depletion effect becomes worse. More importantly, we found that hydrogen species is the primary culprit for aggravated reliabilities in strained devices. Two types of buffer layers, namely, TEOS oxide and poly-Si, were characterized in this work. The TEOS

buffer layer could effectively block the diffusion of hydrogen species contained in the SiN layer into the channel region. On the other hand, poly-Si buffer layer does not depict the same blocking effect as TEOS, owing to the use of the H-containing precursor (e.g. SiH_4) in the deposition step. Hot-electron degradation is adversely affected when the SiN layer is deposited over the gate. The effectiveness of the inserted buffer layer for alleviating the hot-carrier degradation of devices is clearly demonstrated: when a buffer layer is capped prior to the SiN deposition, although still worse than the control ones, significant improvement over that without the buffer could be obtained.

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黃健銘

誌于風城交大　2006

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Chapter 1
Introduction

1.1 General Background

1.1.1 Introduction

The famous “Moore’s Law’’, proposed by Gordon Moore in 1964, states that the number of transistors on an integrated circuit may double every 24 months. For the past four decades, the advancement in IC industry more or less follows this intelligent foresight in its pursue of better performance with lower cost. It can be said that “Moore’s Law’’ is the basis for the overwhelmingly rapid growth of the computing power. In order to keep pace with “Moore’s Law’’, the shrinkage of the transistor dimensions is mandatory. Fig. 1.1 depicts the historical trends of scaling in feature size of CMOS devices [1].

Geometric scaling of silicon complementary metal-oxide semiconductor (CMOS) transistors has enabled not only an exponential increase in circuit integration density (Moore’s law), but also a corresponding enhancement in the transistor performance itself. Many methods have been adopted to improve the performance of CMOS integrated circuit. Recently, strain engineering on the channel has emerged as one of the most effective remedies to boost the drive current in the scaled devices [2-5]. This could

be done by either applying high biaxial tensile strain to the channel region with a SiGe virtual substrate [2], or by uniaxially straining the channel with strain boosters [3-5]. The latter approach is attractive since it can be incorporated seamlessly in state-of-the-art ULSI technology, and has received many attentions in the last few years.

Now that the knowledge base concerning mobility enhancement in strained-Si has been reasonably well established, it is time to turn the focus on such issues as integration and reliability. Device degradation induced by hot electrons represents one of the most critical reliability issues in deep sub-micron NMOSFETs [6-7]. The physical mechanisms and characteristics of hot electron degradation have been extensively examined [8-9]. The degradations in terms of threshold voltage shift (ΔV_{th}), drain current degradation (ΔI_{DS}), and transconductance degradation (ΔG_m), were studied using the accelerated stress test. From our group's previous studies, the extra hydrogen species incorporated during SiN deposition has significant impacts on hot carrier reliability [10]. In this work, we propose a novel fabrication process to prevent device channel from hydrogen encroachment.

1.1.2 Strain Technology

With the scaling of the device size, performance improvement of CMOS devices faces a number of obstacles. It is becoming more and more difficult to maintain high transistor performance because of mobility degradation caused by the increase in

substrate doping. To address this issue, mobility enhancement technology is essential. In order to realize high-speed performance, it is necessary to increase the carrier mobility for devices with the gate length down to the sub-100-nm and below. Strain improves MOSFET drive current by altering the band structure of the channel and can therefore enhance performance even at aggressively scaled channel lengths [11-13].

MOSFETs with biaxial tensile channel stress by growing a Si channel layer on a relaxed SiGe substrate has been demonstrated [14]. Drive current of both NMOSFET and PMOSFET was enhanced by the biaxial tensile stress when Ge is incorporated by more than 20% in the relaxed SiGe layer. It is noted that the thickness of the top strained-Si layer must be thinner than the critical thickness which depends on the Ge content of the underlying relaxed SiGe layer to avoid the generation of a large amount of dislocations. However, the yield issue associated with high threading dislocation density (typically > 10^4 cm^{-2}) of the virtual SiGe substrates still represents a major obstacle for practical applications. In addition, other concerns such as high Ge content and up-diffusion, fast diffusion of n-type dopants, and expensive wafer cost further blight the situation.

In contrast, uniaxial channel strain is free from the aforementioned concerns. Uniaxial strain can be engineered by modifying contact-etch-stop-layer (CESL) deposition [15], shallow trench isolation (STI) [16], source/drain (S/D) material [17],

silicidation [18], packing process [19], and so on. Furthermore, the behaviors of carrier mobility under uniaxial strain depend on the strength of the strain and the orientation [20]. Electron and hole mobilities respond to the complex three-dimensional mechanical stress in different and even opposite ways. The channel tensile and compressive stress can be applied separately to NMOS and PMOS devices to enhance performance, respectively (as shown in Fig. 1.2). Depending on the CESL deposition conditions, the SiN layer can generate either tensile or compressive stress [21]. The channel tensile and compressive stress can be applied on NMOS and PMOS devices to enhance performance, respectively [20].

The carrier mobility is given by $\mu = \frac{q\tau}{m^*}$, where $1/\tau$ is the scattering rate and m^* is the conductivity effective mass. Strain enhances the mobility by reducing the conductivity effective mass and/or the scattering rate. Both effective mass and scattering rate changes are important for mobility enhancement in electrons [22]. However, only effective mass change due to band warping and repopulation [23] plays a significant role in holes. For electron transports in bulk Si, the conduction band is composed of six degenerate valleys ($\Delta 6$) of the same energy. Strain removes the degeneracy between the four in-plane valleys ($\Delta 4$) and the two out-of-plane valleys ($\Delta 2$) by splitting them in energy. The energy difference (ΔE) between $\Delta 2$ and $\Delta 4$ sub-bands determines the total population of the bands. The enhancement caused by the splitting of conduction band

can suppress inter-valley phonon scattering [24]. The lower energy of the Δ2 valleys indicates that they are preferentially occupied by electrons. The electron mobility is improved partly by reducing in-plane and increasing out-of-plane effective mass due to the favorable mass of the Δ2 valleys, which results in more electrons with an in-plane transverse effective mass and out-of-plane longitudinal mass.

For holes, the valence-band structure of Si is more complex than the conduction-band structure. The complex band structure as well as valence-band warping under strain results in a much larger mobility enhancement of holes than electrons. These two factors also explain why strained-channel PMOSFETs is a key focus in advanced logic technologies. Holes occupy the top two (the heavy- and light- hole) bands for unstrained Si. With the application of strain, the hole effective mass becomes highly anisotropic due to band warping, and the energy levels become mixtures of the pure heavy, light, and split-off bands. Thus, the light and heavy hole bands lose their meaning, and holes increasingly occupy the top band at higher strain due to the energy splitting. To quantify the mobility enhancement of holes, changes of the scattering and effective mass depend on the altered valence band caused by the strain. From full-band Monte Carlo simulation [25], uniaxially compressive-strained PMOSFETs may have lighter in-plane effective mass thus improve hole mobility. But, for biaxial tensile stress, the effective mass is heavier than that in the unstrained case. Thus the hole mobility

enhancement is only possible through the reduction of inter-valley scattering [26]. This effect becomes significant only when the strain level is high enough (e.g., Ge > 20 %). Reducing the intra-band acoustic scattering by altering the density-of-states of the light- and heavy-hole bands is negligible for uniaxial strain in Si, even at several hundreds of mega-pascal.

Hole mobility at high vertical field with uniaxial compressive and biaxial tensile stresses would have different behaviors. Splitting of light- to heavy-hole band caused by uniaxial and biaxial stresses has no significant difference without considering surface quantization confinement. However, the splitting of light- and heavy-hole bands caused by biaxial tensile stress would be nullified at high electric field due to surface confinement [27]. In contrast, hole mobility enhancement under uniaxial compressive strain is not nullified by surface confinement, which represents a major advantage for MOSFETs operating at high electric fields. The splitting of the surface confinement depends on the relative magnitude of the stress-altered out-of-plane masses of the light and heavy holes. Recent reports [23] showed the interesting result that the out-of-plane effective mass of light hole is heavier than that of heavy hole for uniaxial stress, and causes the increase in the splitting of light- to heavy-hole bands. On the contrary, for biaxial stress the previously-reported out-of-plane effective mass of light hole is lighter than that of the heavy hole, leading to a reduced band splitting. This is why the biaxial

stress degrades hole mobility enhancement at high vertical electric fields (as shown in Fig. 1.3).

For NMOSFETs, it has been report that the threshold voltage shift caused by biaxial tensile stress is larger than the case with uniaxial tensile strain [28]. For PMOSFETs, larger shifts of light-hole band edge under biaxial tensile strain leads to larger shift in V_{th}, compared with the case with uniaxial compressive strain [23].

1.1.3 Hot Carrier Effect

One of the serious reliability problems posed by continuous shrinking of MOSFETs into the submicron regime is the hot-carrier effect [29-30]. If devices dimensions are reduced and the supply voltage remains constant, the lateral electric field in the channel increases. This would cause the inversion layer charge to be accelerated more significantly, and leads to a number of harmful devices phenomena, denoted as hot-carrier degradation. The most important hot-carrier effect is the damage inflicted to the gate oxide and/or the Si/SiO_2 interface. This causes a time-dependent degradation of various MOSFET characteristics, for example, threshold voltage, linear transconductance, subthreshold slope, and saturation current.

The location of the damage region due to hot-carrier stress is found to be adjacent to the drain of the device. The lifetime of devices is impacted by the spatial non-uniformity of this damage. The extent of the damaged region is a function of device

geometry, the duration and conditions of stress, and of spatial distribution of oxide and interfacial defects. However, it has also been reported that the length of damaged region is independent of channel length [31]. Thus, the damaged region becomes a larger fraction of the channel length as the device shrinks. This causes a dramatic increase in the percentage of drive current degradation as L_{eff} becomes smaller for the same stressing time and the same value of I_{sub}.

1.2 Motivation

The SiN layer (contact-etch-stop-layer) can be used to induce channel strain for mobility enhancement [4][23]. However, in typical SiN capping processes abundant hydrogen species will be incorporated into the channel, and significantly influences MOSFETs characteristics. In particular, despite the dramatic performance improvement in the strained devices, their hot-carrier reliability is however compromised, which has been shown to be closely related to the incorporated hydrogen species [10]. This motivates us to carry out this study on the hot carrier degradation of NMOSFETs devices with SiN capping layer. We also propose the use of a buffer layer inserted between the gate and SiN capping layer to prevent hydrogen diffusion during processing and thus alleviate its impacts on device reliability. Different buffer layers were employed and investigated.

1.3 Organization of This Thesis

This thesis is divided into four chapters.

In Chapter 2, we briefly describe the key process flow for fabricating the NMOS devices with buffer layers. In order to verify the effect of buffer layers under hot carrier stress, splits with different buffer layers were fabricated and characterized. In addition, we present the characterization method and the stress conditions.

In Chapter 3, we show and discuss the improvement on device performance with buffer layer. The effectiveness of the buffer layers on alleviating the hot-carrier degradation of the locally strained devices with buffer layers is evaluated and addressed.

Finally, important conclusions generated from our experimental results are summarized, and some recommendations and suggestions for future work are given in Chapter 4.

Chapter 2
Device Fabrication and Measurement Setup

2.1 Device Fabrication and Process Flow

The NMOSFETs were fabricated on 6-inch p-type (100) Si wafers with resistivity of 15~25Ω-cm and thickness of 655~695 μm. Additional p-type substrate doping was performed first by BF_2^+ implantation at 100 keV and 1×10^{-13} cm^{-2}. Next, standard local oxidation of silicon (LOCOS) process with channel stop implant (by BF_2^+ implantation at 120 KeV and 4×10^{-13} cm^{-2}) was used for device isolation. Threshold voltage adjustment and anti-punch through implantation were done by implanting 40 KeV BF_2^+ and 35 KeV B^+, respectively. After the growth of 3 nm thick thermal gate oxide, a 150nm undoped poly-Si layer was deposited by low-pressure chemical vapor deposition (LPCVD), followed by gate etch process to pattern the poly-Si film. The Source/drain (S/D) extension regions were then formed by As^+ implantation at 10 KeV and 5×10^{-14} cm^{-2}. After an 80nm TEOS spacer formation, S/D regions were formed by P^+ implantation at 15 KeV and 5×10^{-15} cm^{-2}. Then the patterning of the substrate doping regions was performed through lithography and etching processes, followed by a BF_2^+ implantation at 40 KeV and 5×10^{-15} cm^{-2}. Rapid thermal anneal (RTA) was subsequently

carried out in a nitrogen ambient at 900°C for 30 sec to activate dopants in the gate, S/D, and substrate regions.

Afterwards, some samples were capped with a TEOS or a poly-Si to serve as the buffer layer. The thickness of the buffer layer is 10 nm. Then a SiN capping layer (contact-etch-stop-layer, CESL) of 300nm was deposited on some wafers both with or without the buffer layer. The SiN deposition was performed at 780 ℃ with SiH_2Cl_2 and NH_3 as the reaction precursors using low-pressure chemical vapor deposition (LPCVD) system. After the SiN capping, a 300nm TEOS passivation layer was deposited by an LPCVD system.

To simulate the effect of deposition temperature during the SiN deposition, the control devices (i.e., without SiN capping) received a placebo treatment (i.e., the same temperature and treatment time as that used in the SiN deposition) in N_2 ambient. After contact hole etching, normal metallization was carried out for all samples. The final step was a forming gas anneal performed at 400°C for 30 min to mend dangling bonds and reduce interface state density in the gate oxide/Si interface. Cross-sectional view of the fabricated device was shown in Fig. 2.1.The five split conditions stated above are summarized in Table 2.1.

2.2 Electrical Measurement Setup

Current-voltage (I-V) and capacitance-voltage (C-V) characteristics were evaluated

by an HP4156A precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. Temperature-regulated hot chucks were used to maintain the measurement temperature at 25°C.

2.3 Charge Pumping Measurement

2.3.1 Basic Theory

The charge pumping principle for MOSFETs has been applied to characterize the fast interface traps in MOSFETs. The original charge pumping method was introduced by Brugler and Jespers [32], and the technique was then developed by Heremans [33]. This technique is based on a recombination process at the Si/SiO_2 interface involving the surface traps. It consists of applying a constant reverse bias at the source and drain, while sweeping the base level of the gate pulse train from a low accumulation level to a high inversion level. The frequency and the rise/fall time are kept constant. When the base level is lower than the flat-band voltage while the top level of the pulse is higher than the threshold voltage, the maximum charge pumping current occurs. This means that a net amount of charge is transferred from the source and drain to the substrate via the fast interface traps each time the device is pulsed from inversion toward accumulation. The charge pumping current is caused by the repetitive recombination at interface traps. As a result, the recombination current measured from the bottom

(substrate) is the so-called charge pumping (CP) current [34]. The CP current can be given by:

$$I_{CP} = q \cdot f \cdot W \cdot L \cdot N_{it}. \quad (2.1)$$

According to this equation, the current is directly proportional to the interface trap density in the channel, the frequency, and the area of the device. However, when the top level of the pulse is lower than the flat-band voltage or the base level is higher than the threshold voltage, the fast interface traps are permanently filled with holes in accumulation or the electrons in inversion in NMOSFETs. As a result, there is no recombination current and no charge pumping current can be detected.

2.3.2 Basic Measurement Setup

The basic setup of charge pumping measurement is shown in Fig. 2.2. In this thesis, “fixed amplitude sweep” is used to calculate interface trap density, and “fixed base sweep” is used to analyze the lateral distribution of interface trap, respectively. The source and drain are biased at 50mV. The substrate electrodes of tested devices are grounded. A 1MHz (the frequency can be modulated for different devices) square pulse waveform provided by HP8110A with fixed amplitude is applied to the NMOS gate. The base voltage is varied to let surface condition switch from inversion to accumulation, while keeping the pulse amplitude at 1.5V. In our measurement setup, V_{base} is varied from -2V to -0.2V in step of 0.05V. The parameter analyzer HP4156A is

used to measure the charge pumping current (I_{CP}).

2.4 Hot Carrier Reliability Measurement Setup

In our reliability measurement, the device was stressed with the drain voltage at a highly positive voltage, and the gate terminal biased at the voltage where maximum I_{sub} occurs to accelerate the degradation. So we must first measure the Isub-V_G with a fixed drain bias to find V_G@$Isub_{max}$, before stressing the device. To monitor the degradation caused by the hot electrons, the I_D-V_G characteristics at V_{DS} = 0.05 V (linear region) and charge pumping current were measured before and after the stress. The degradations in terms of threshold voltage shift (ΔV_{th}), interface trap density degradation (ΔN_{it}), and transconductance degradation (ΔG_m), were recorded in the accelerated stress test.

2.5 Extraction Procedure of Lateral Distribution of Nit

The lateral distribution of interface state after hot carrier stress of all splits was also discussed in this work. This method builds on [35] and the measurement setup is shown in Fig. 2.3. The experimental procedures are described below.

(1) Measure the Icp-V_h curve on a virgin MOSFET from the drain junction (with the source junction floating), and from which the relationship between V_h and V_{th}(x) near the junction of interest is established [36].

(2) Record the Icp-V_h curve after hot-carrier injection.

(3) The hot-carrier-induced interface state distribution, $N_{it}(x)$, is obtained from the difference of the Icp-V_h curves before and after the stress.

Chapter 3
Experimental Results and Discussion

3.1 Electrical Characteristics of Locally Strained NMOSFETs with Buffer Layer

3.1.1 Fundamental Electrical Characteristics

First of all, our goal is to investigate the effect of thermal budget associated with the SiN deposition. So, for the placebo split, we deliberately added an additional thermal treatment step in N_2 with an identical temperature and treatment time as those used in the SiN deposition (i.e., at 780℃ ambient for 3 hours) before the TEOS passivation layer deposition. Samples which were skipped both the SiN deposition and the thermal N_2 annealing steps were also fabricated for comparison, denoted as the REF (reference) split. Fig.3.1 shows the effect of such placebo thermal treatment on the capacitance-voltage(C-V) characteristics of devices without SiN capping. In this figure, the device with the additional thermal budget (placebo split) shows apparent poly-depletion effect. We believe this is caused by the temperature-dependent solid solubility of dopants in poly gates [37], as shown in Fig. 3.2. In other words, the original solid solubility (approaching the equilibrium value at 900℃, which is caused by the rapid thermal anneal (RTA) step) is lowered by the furnace SiN deposition step

due to the additional thermal budget. The placebo split shows larger threshold voltage due to the reduction of fixed charge in gate oxide. The C-V characteristics of MOSFETS are also important in verifying the oxide quality and the equivalent oxide thickness (EOT). Fig. 3.3 exhibits C-V characteristics of NMOSFETs for all splits (i.e. placebo (thermal budget), SiN, TEOS/SiN, POLY/SiN). The curves of four splits are basically identical. It gives an equal ground to compare the performance of all splits. So the split with placebo thermal budget (i.e., the placebo split) serves the role of the control split, and will also be called the control split interchangeably. Fig. 3.4 shows cumulative probability distributions of the sheet resistance of the poly gate for all splits. The REF (i.e., W/O thermal budget) split has lower sheet resistance values, while the other four splits exhibit almost same distribution of sheet resistance. This demonstrates that the additional thermal treatment step used in the SiN deposition indeed results in worse poly-depletion effect.

The Id-Vg characteristic of the split conditions are shown in Fig. 3.5. From the figure, there is no obvious difference in the transconductance (Gm) among all samples except the placebo split, clearly revealing the enhancement of transconductance by the strained technology. The off-state leakage current and the subthreshold slope show no distinguishable difference in Fig. 3.5, indicating that the devices with strained channel do not show major influence on the fundamental properties. Fig. 3.6 depicts the

subthreshold swing for all splits, and the results indicate that the values are confined in a narrow range between 74~75 mV/decade. The output characteristics of all splits are shown in Fig. 3.7. It is seen that the insertion of the buffer layer prior to SiN deposition (i.e., TEOS/SiN, POLY/SiN) does not degrade the current enhancement. Consistent with previous literature report [38], the NMOS drive current can be enhanced by a thicker SiN etch-stop layer which is tensile in nature.

Fig. 3.8 shows the percentage increase of the transconductance among different splits relative to the placebo devices (i.e., w/o SiN capping). The transconductance enhancement reaches about 29% and 33% at a channel length of 0.5μm and 0.4μm, respectively. We can see that when the channel length decreases, the strain effect enhances. In other words, the strain is distributed locally inside the channel and concentrated near the source and drain. As a result, the transconductance enhancement becomes more prominent with decreasing channel length. This is explained by the splitting of the degeneracy at the conduction band edges under uniaxial strain [24] as mentioned above. Fig. 3.9 exhibits the percentage increase of the saturation current for the split samples relative to the placebo devices (i.e., w/o SiN capping). From Fig. 3.9, it can be seen that similar trend to that shown in Fig. 3.8 is observed.

Fig. 3.10 shows the results of charge pumping measurement for some splits (i.e., placebo (thermal budget), REF, and SiN). First, we focus on the impact of thermal

budget associated with the SiN deposition. From the figure, we find that a large amount of interface states is generated during SiN capping process as compared with the samples without the capping layer, implying that the channel strain indeed causes the increase of interface states at the Si/SiO_2 interface. Nevertheless, it is well known that hydrogen species can effectively passivate the dangling bonds at the Si/SiO_2 interface. For the LPCVD system used for SiN deposition in this study, SiH_2Cl_2 and NH_3 were employed as the reaction precursors, so the reaction chamber would be filled with hydrogen species during the deposition process. The hydrogen species would in turn passivate the interface trap states at the Si/SiO_2 interface. Although this factor should not be ignored, in this figure such effect obviously is masked by the channel strain. In other words, the number of interface states passivated by the hydrogen species is much less than that generated by the channel strain.

On the other hand, the figure also proves that the annealing performed in N_2 tends to reduce the interface states density, indicating this factor (thermal budget of the deposition) alone is beneficial for improving the interface properties. From Fig. 3.10, impacts of the three factors, namely, channel, incorporated hydrogen species, and the thermal budget, on interface state density are identified.

Comparisons of charge pumping current between the strain and placebo samples are shown in Fig. 3.11. The placebo sample exhibits the lowest charge pumping current

among all splits, while the device with TEOS buffer layer exhibits the highest. The curve of the device with POLY/SiN is slightly higher than that with SiN, but less than that with TEOS buffer layer. The results indicate that the TEOS buffer layer can effectively block the diffusion of hydrogen into the channel region, while such barrier effect seems to be reduced for the POLY buffer layer. It has been pointed out previously that the poly-silicon is a diffusion barrier of the hydrogen [39]. But it should be noted that, the precursor gas (SiH_4) for deposition is also H-containing. Before the SiN deposition, the abundant hydrogen species may have spread to the Si/SiO_2 interface to passivate the interface states. In summary, TEOS buffer layer has been shown to be more effective in blocking the hydrogen diffusion into the Si/SiO_2 interface.

3.1.2 Short Channel effect

Threshold voltage (V_{th}) roll-off characteristics of the placebo (thermal budget) and REF splits are shown in Fig. 3.12. The results are obtained at V_{DS} = 0.05 V. From the figure, both splits depict reverse-short-channel-effect (RSCE). This can probably be explained by boron segregation at the implant-damaged regions located near the edge of the channel [40]. Devices with additional thermal budget show improved reverse-short-channel-effect [40]. It might be related to the redistribution of dopants that effectively reduces the boron segregation effect, explaining the suppression of the RSCE shown in Fig. 3.12.

In Fig. 3.13, it is worth noting that the placebo samples depict the reverse-short-channel-effect (RSCE). However, this phenomenon is not observed on three SiN-capped splits (SiN, TEOS/SiN, POLY/SiN). Instead, theses three splits exhibit similar and significant threshold voltage roll-off trend. It is believed that the bandgap narrowing effect is the culprit to accelerate the Vth roll-off in the strained channel device [28, 41]. The strain stress may also result in the channel dopants redistribution [42, 43]. In brief, the channel strain associated with the SiN capping devices (SiN, TEOS/SiN, POLY/SiN) would lead to aggravated Vth roll-off.

Drain induced barrier lowing (DIBL) is another pointer in evaluating the short channel effects. We use the interpolation method to calculate DIBL effect for all splits. The results are shown in Fig. 3.14. It is clearly seen that there is no distinguishable difference among all splits. It appears that devices with SiN capping and buffer layers will not complicate the DIBL effect of the samples.

3.2 Hot Carrier Degradation of Locally Strained NMOSFETs with Buffer Layer

A hot carrier with sufficient energy can create more charge carriers through impact ionization. For NMOSFET devices, holes generated by impact ionization are collected by the substrate. Fig. 3.15 shows the substrate current (I_{sub}) versus gate voltage for all splits of devices at V_D of 4.6 V. It can be seen that the three strained-channel splits

exhibit almost identical maximum substrate current which are much higher than that of placebo sample. This result shows clearly that the channel strain plays an important part in affecting the generation of channel hot electrons and the associated impact ionization process. Bandgap narrowing and mobility enhancement, both due to channel strain, are mainly responsible for enhancing the ionization rate [44]. So the SiN-capped devices show larger substrate current than the placebo samples.

Hot-carrier effects and the induced degradation were investigated to study the impact of the SiN capping and buffer layers. As discussed above, it is expected that the split with SiN capping (i.e. SiN) would show aggravated hot carrier degradation. Fig. 3.16 and Fig. 3.17 show threshold voltage shift and increased interface state density, respectively, as a function of stress time for all splits that received hot-electron stressing at V_{DS} = 4.6 V and V_{GS} at maximum substrate current. All devices are with channel width/length = 10μm/0.5μm. As expected, the split with SiN capping shows the worst hot carrier degradation, and the use of buffer layer apparently improves hot carrier degradation. We assume that the bandgap narrowing effect and the increased carrier mobility in the strained channel devices [44, 45] are the two primary culprits for the aggravated hot carrier degradations. These two factors may increase the substrate current in the device, as evidenced in Fig. 3.15, and lead to higher degradation.

The H-passivated bonds at the interface also play a role in the hot-carrier

degradation process. Since the hot carriers tend to break the Si-H bonds during the process, the higher the amount of the Si-H density, the severer the degradation. The TEOS buffer layer can block the diffusion of hydrogen species into the channel region, less broken Si-H bonds and thus less interface states are generated during the stressing as compared with the SiN-capped devices. As a consequence, better reliability is achieved, as evidenced in Fig. 3.16 and Fig. 3.17. For the devices with POLY buffer layer, less improvement is achieved due to higher amount of Si-H bonds, as stated above. Fig. 3.18 illustrates the 10-year reliability projections for the four splits. Lifetime is defined as 40mV of ΔV_{th}. The observed trend is the same as that shown in Fig. 3.16. Strained devices show poor hot carrier reliability than placebo device, although the use of buffer layer can alleviate hot carrier degradation.

Typical results of hot-electron stressing for the four splits of samples are shown in Fig. 3.19 and Fig. 3.20. Channel width and length of the test devices are $10\,\mu m$ and 0.5 μm, respectively. The devices are stressed at V_{DS} = 4.9 V and V_{GS} at maximum substrate current. The I_D-V_G characteristics at V_{DS} = 0.05 V are measured before and after the stress to evaluate the degradation caused by the hot electrons. As shown in Fig. 3.19 and Fig. 3.20, the degradation is the worst in the SiN-capped sample without buffer layer among the four splits. The aggravation is alleviated in the devices with buffer layer (i.e. TEOS/SiN, POLY/SiN), though the resultant degradation is still worse than

that of the placebo counterpart.

3.3 Analysis of the Lateral Distribution of Interface Trap Density

The measurement methods presented in Section 2.5 was used to extract lateral distribution of interface trap state. It should be noted that the local V_{th} and V_{fb}, across the channel of MOSFET, are not uniform due to the lateral doping variation, as shown in Fig. 3.21. In order to detect the interface state, the voltage pulses applied during measurement must undergo alternating accumulation and inversion cycles. Therefore, there should be no Icp when the high-level voltage (V_h) is lower than the minimum V_{th} under the gate. Only after V_h starts to exceed the local V_{th} in the channel will Icp begin to grow. Before V_h reaches the maximum local V_h in the channel, only interface states residing near the drain side will contribute to Icp, as the needed electrons cannot yet flow to the drain side from the source.

We choose the placebo split as an example. If we assume that the interface state density is spatially uniform along the channel, which can be written as

$$I_{CP} = q \cdot f \cdot W \cdot L \cdot N_{it}. \quad (3\text{-}1)$$

where f is the gate pulse frequency, W is the channel width, and L is the channel length. Since V_{th} is not uniformly distributed, when V_h reaches the maximum local V_{th} in the channel, only interface state residing near the drain side (i.e., the shadow region

in Fig. 3.21) will contribute to Icp. In Fig. 3.22, the corresponding Icp(V_h) comes from the interface state distributed in the region between the gate edge and the position where its local V_{th} equals V_h, i.e.,

$$I_{cp}(V_h) = q\, f\, N_{it}\, W\, x \tag{3-2}$$

where x represents the distance from the gate edge to the position where $V_{th}(x) = V_h$. Comparing (3-1) and (3-2), we can derive

$$x = \frac{LI_{cp}(V_h)}{I_{cp,\max}} \tag{3-3}$$

Fig.3.23 shows the local V_{th} versus distance x of the placebo sample. The local V_{th} decreases sharply as x is smaller than 0.09 μm. We can therefore presume that the drain junction is near x = 0.09 μm.

After subjecting to 100 second of hot carrier stress (V_G@$Isub_{max}$ and V_{DS} = 4.9 V), the incremental charge pumping current (ΔIcp), as shown in Fig. 3.24, at a given V_h is proportional to the number of generated interface traps from the gate edge to the point x. ΔIcp can be written as

$$\Delta I_{cp} = q\, f\, W \int_0^x N_{it}(x)\, dx \tag{3-4}$$

Therefore, the Nit(x) generated by the hot carrier stress can be expressed as follows:

$$N_{it}(x) = \frac{d\Delta I_{cp}}{dx}\frac{1}{q\, f\, W} = \frac{d\Delta I_{cp}}{dV_h}\frac{dV_h}{dx}\frac{1}{q\, f\, W} \tag{3-5}$$

The relationship of $\frac{dV_h}{dx}$ versus x can be derived from V_h versus x, so the lateral distribution, Nit (x), could be obtained from the procedure mentioned above.

By the same procedure, the derived profiles of the interface states for all splits of devices could be extracted by Eq.(3-5), and the result are shown in Fig. 3.25. From this figure we can directly probe the position-dependent damage characteristics by calculating the amount of interface states generated by the hot-carrier stress at different regions. We can see that the major damage region is confined within 0.1 μm near the drain edge in all splits. This is reasonable since the hot-carrier effect is known to be localized in nature. It is obviously seen that the interface state generation sharply increases in SiN-capped sample (i.e. SiN, TEOS/SiN, POLY/SiN) near the drain region, but the buffer layer samples show smaller degradation than the SiN-capping split without buffer layer. These results are consistent with those mentioned above in Section 3.2. In short, channel strain is responsible for the aggravated hot carrier degradations observed in SiN-capped samples. However, the devices with buffer layer show alleviated hot carrier degradation and improved device reliability.

Chapter 4
Summary and Conclusion

4.1 Summary and Conclusion

In this thesis, the effects of LPCVD SiN layer and the associated deposition process on the device characteristics and hot-electron degradation are investigated. A novel scheme involving the insertion of a buffer layer between the SiN and the gate for improving the device reliability was proposed and demonstrated. Several important phenomena are observed and summarized as follows:

(1) The buffer layer before SiN deposition would not degrade the device performance. For example, the enhancement ratio of transconductance in the device with the buffer layer is found to be around to 33% at a channel length of 0.4 μm, which is essentially identical to the enhancement ratio observed in the SiN-capped device.

(2) The thermal budget associated with the deposition of the SiN capping layer could reduce the interface states and alleviate the reverse short-channel effect, although the poly-depletion effect becomes worse. The bandgap narrowing effect due to the channel strain may result in further lowering in V_{th} as the channel length is shortened.

(3) The TEOS buffer layer could prevent hydrogen species from diffusion during processing. POLY buffer layer does not depict the same barrier effect as TEOS, owing

to the use of the H-containing precursor (e.g. SiH_4) in the deposition step.

(4) Hot-electron degradation is adversely affected when the SiN is deposited over the gate as compared with the placebo samples. When a buffer layer is capped prior to the SiN deposition, although still worse than the placebo ones, significant improvement over that without the buffer could be obtained. From the measurement of the distribution of interface trap density, enhance edge effects caused by the hot carrier stress are resolved.

In this work, we found that hydrogen species is the primary culprit for aggravated reliabilities in strained devices. The insertion of a buffer layer serves to alleviate the device hot-carrier degradations. Optimization of SiN deposition process and/or use of the new buffer layer (e.g., high-*k* film) are thus essential for the implementation of the uniaxial strain in NMOS devices.

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Gate		Buffer Layer	CESL	PassivationLayer	Index
Oxide 30Å	Undoped Poly-Si 1500Å	w/o	w/o	TEOS 3000 Å	REF
		w/o(control)	Placebo thermal budget		Placebo (control)
		w/o	SiN 3000Å		SiN
		TEOS 100 Å	SiN 3000Å		TEOS/SiN
		Poly-Si 100 Å	SiN 3000Å		POLY/SiN

Table 2.1 Split table of buffer layer and CESL.

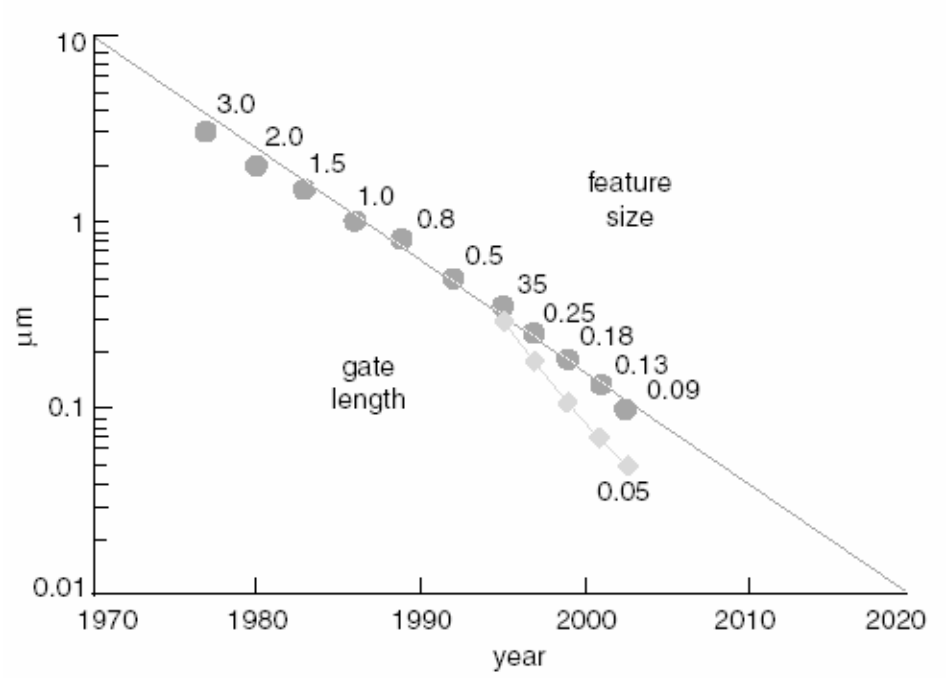
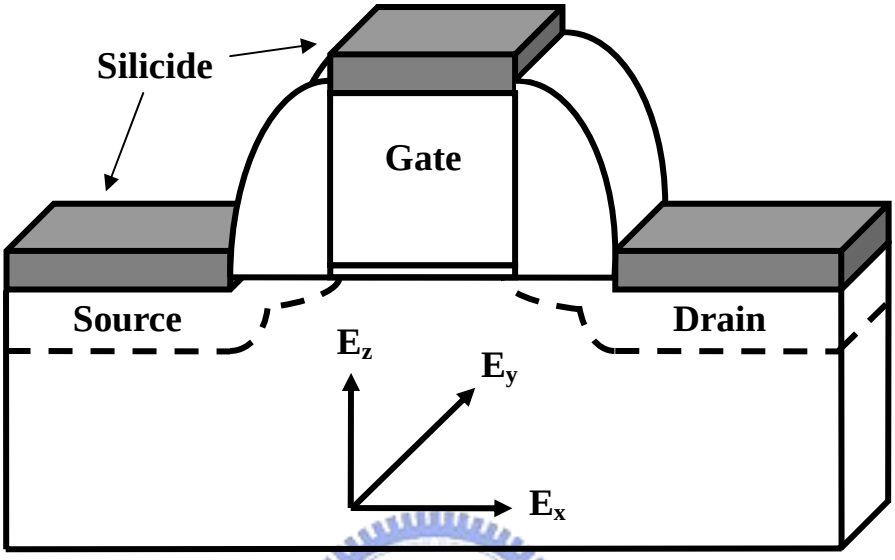


Fig. 1.1 Gate length scaling as a function of the year of introduction for technology node [1].

Process-induced Strain



Direction of Strain Change*	CMOS Performance Impact	
	NMOS	PMOS
X	Improve	Degrade
Y	Improve	Improve
Z	Degrade	Improve

* Strain change = Increased tensile or decreased compressive strain

Fig. 1.2 Schematic illustration for 3D process-induced strain components [19].

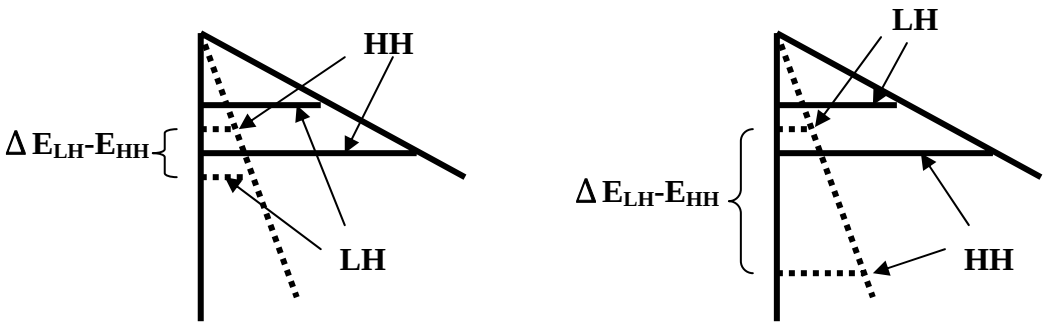


Fig. 1.3 Splitting of light hole band and heavy hole band with biaxial and uniaxial strains in low electric field (solid line) and high electric field (dash line) [22].

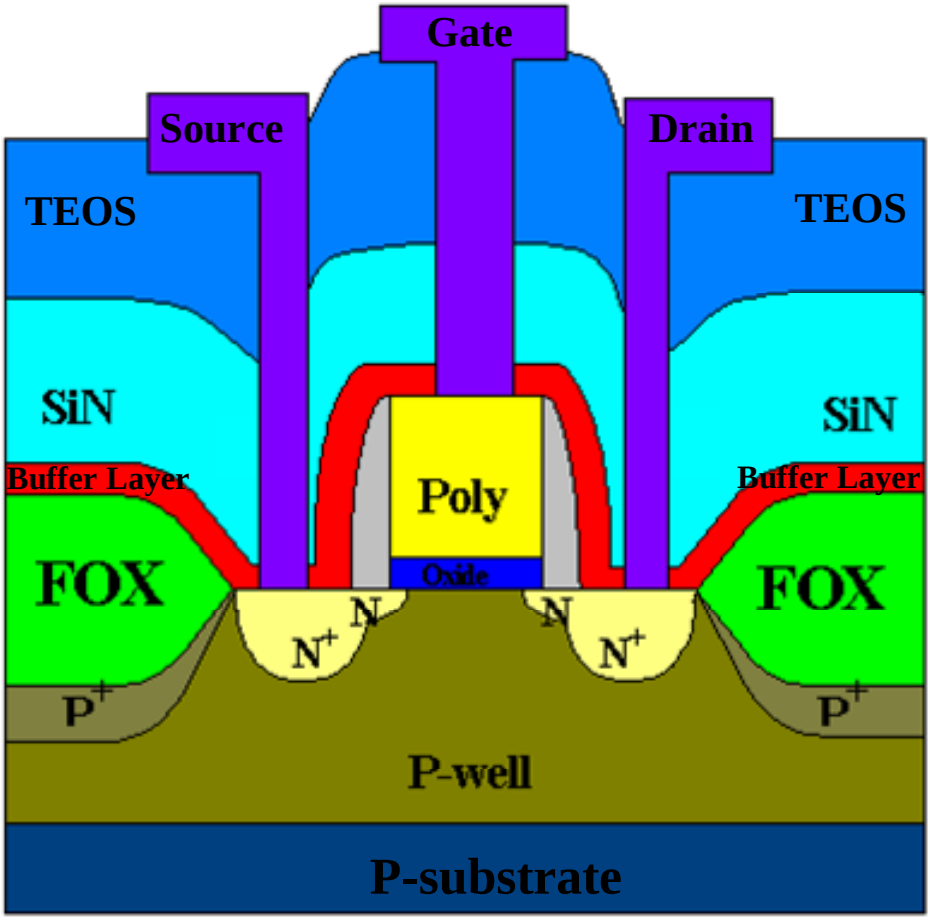


Fig. 2.1 Schematic cross section of the locally-strained-channel NMOSFT.

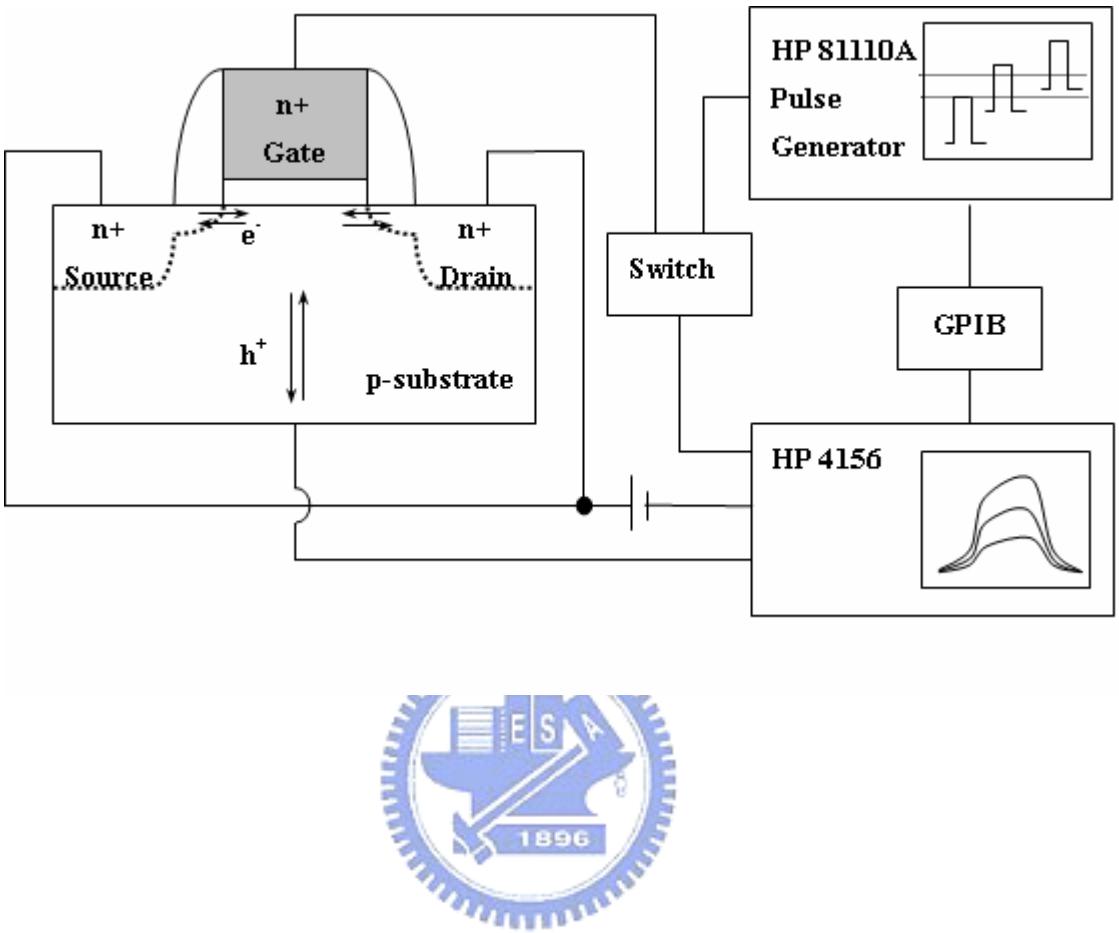


Fig. 2.2 Setup structure for charge pumping measurement.

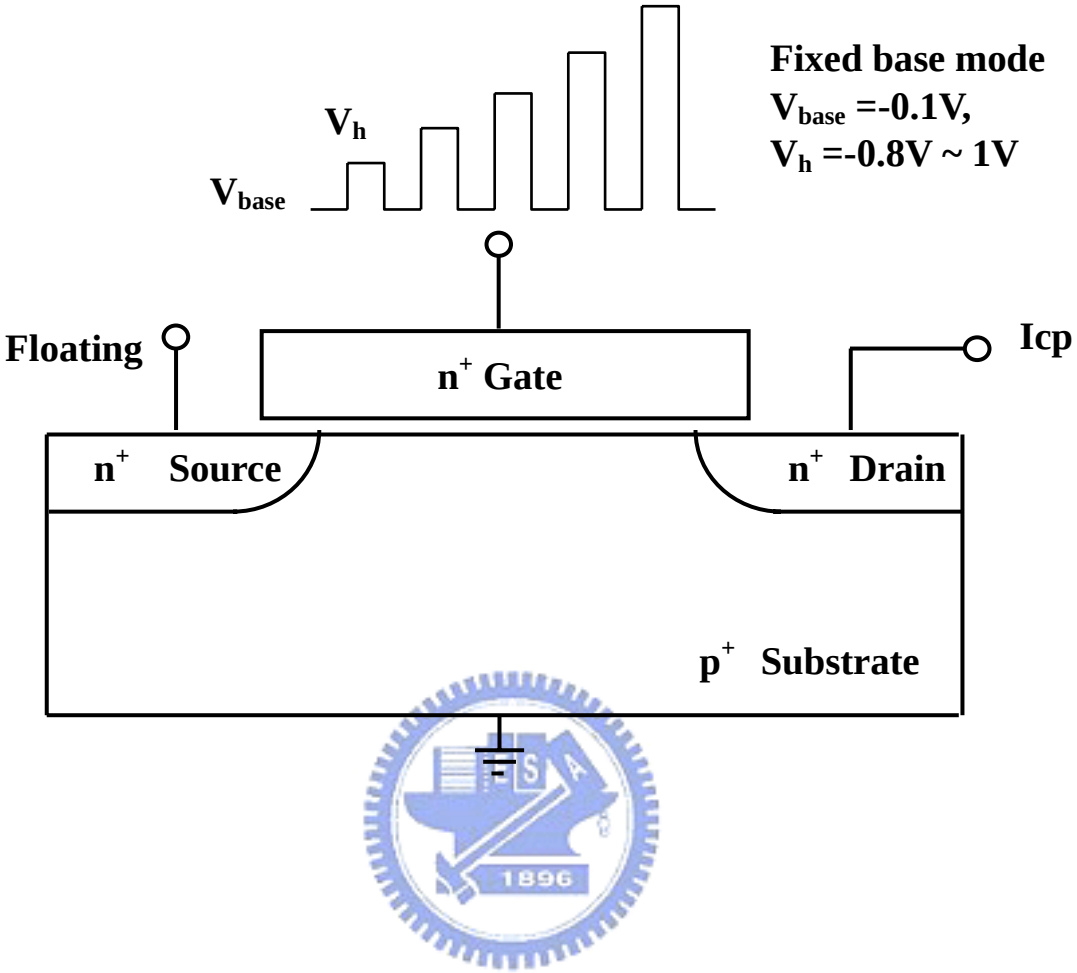


Fig. 2.3 Measurement setup of single-junction charge pumping measurement.

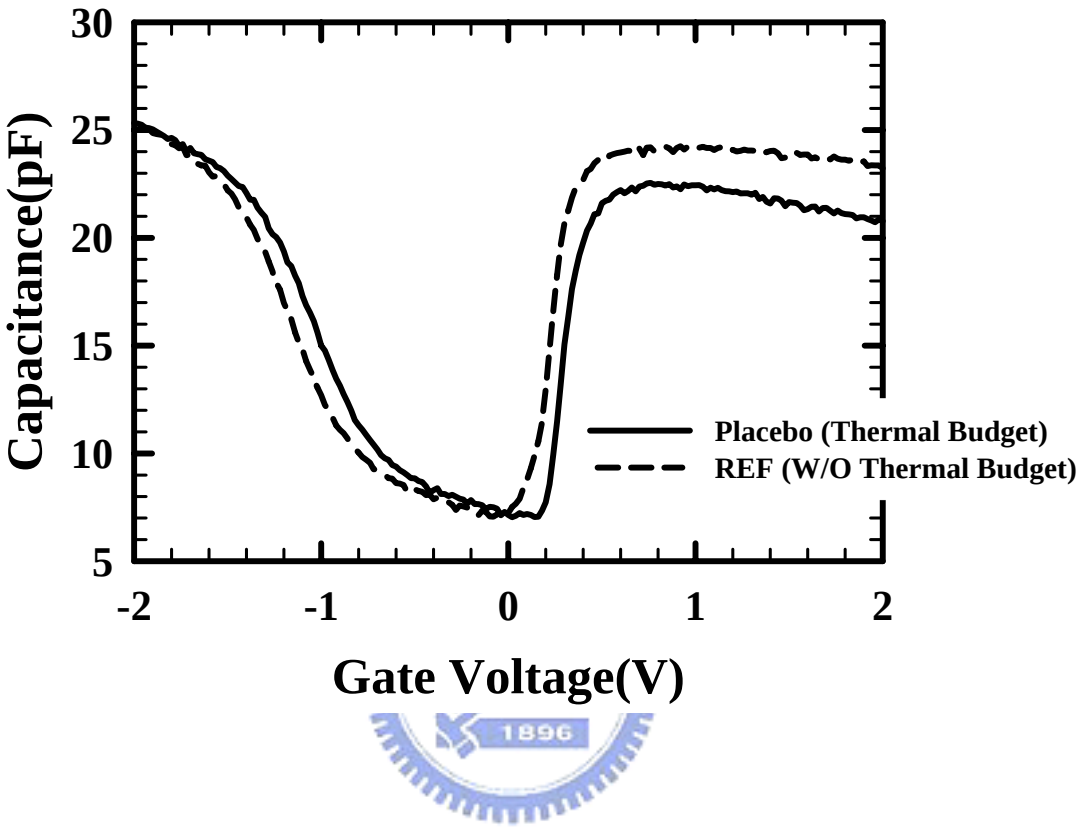


Fig. 3.1 Capacitance-Voltage(C-V) characteristics of NMOSFETs processed with different thermal budgets. Channel width/channel length = 50 μ m/50 μ m.

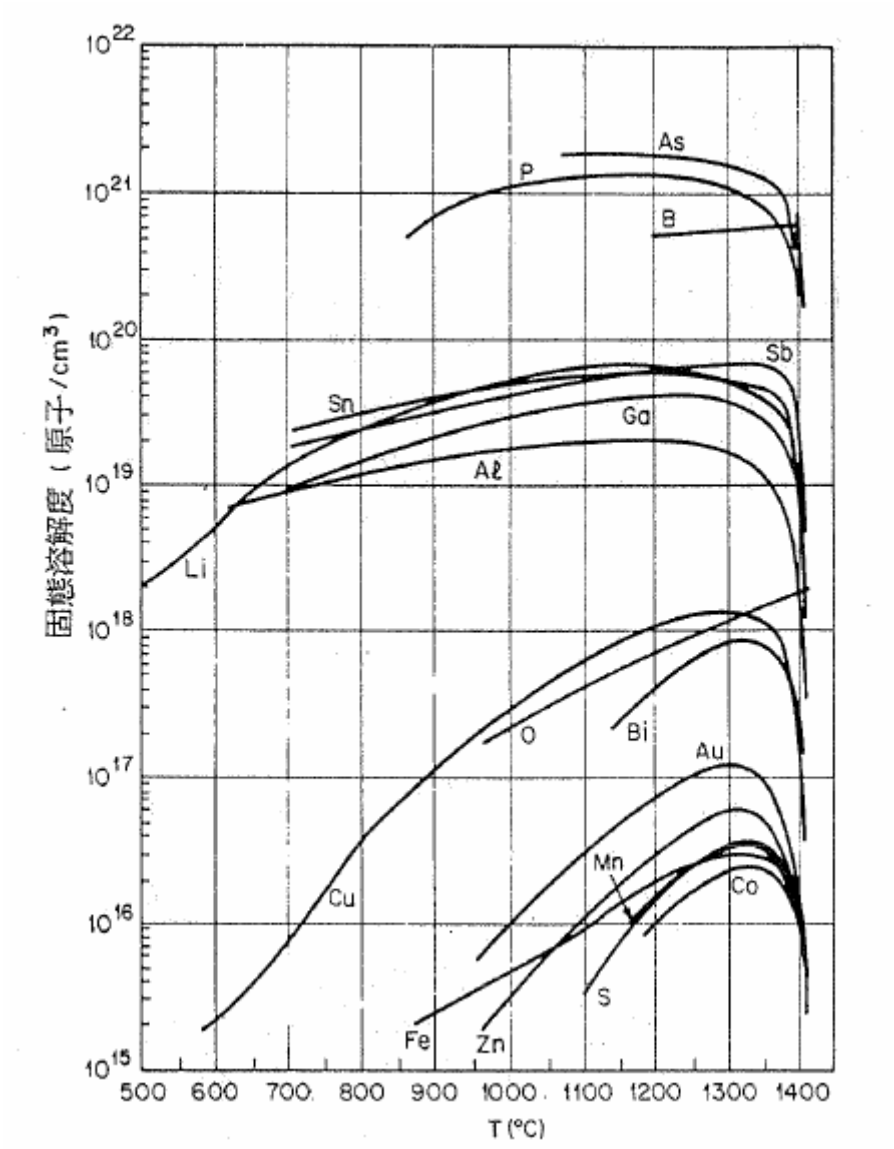


Fig. 3.2 Solid solubility of various elements in Si as a function of temperature [37].

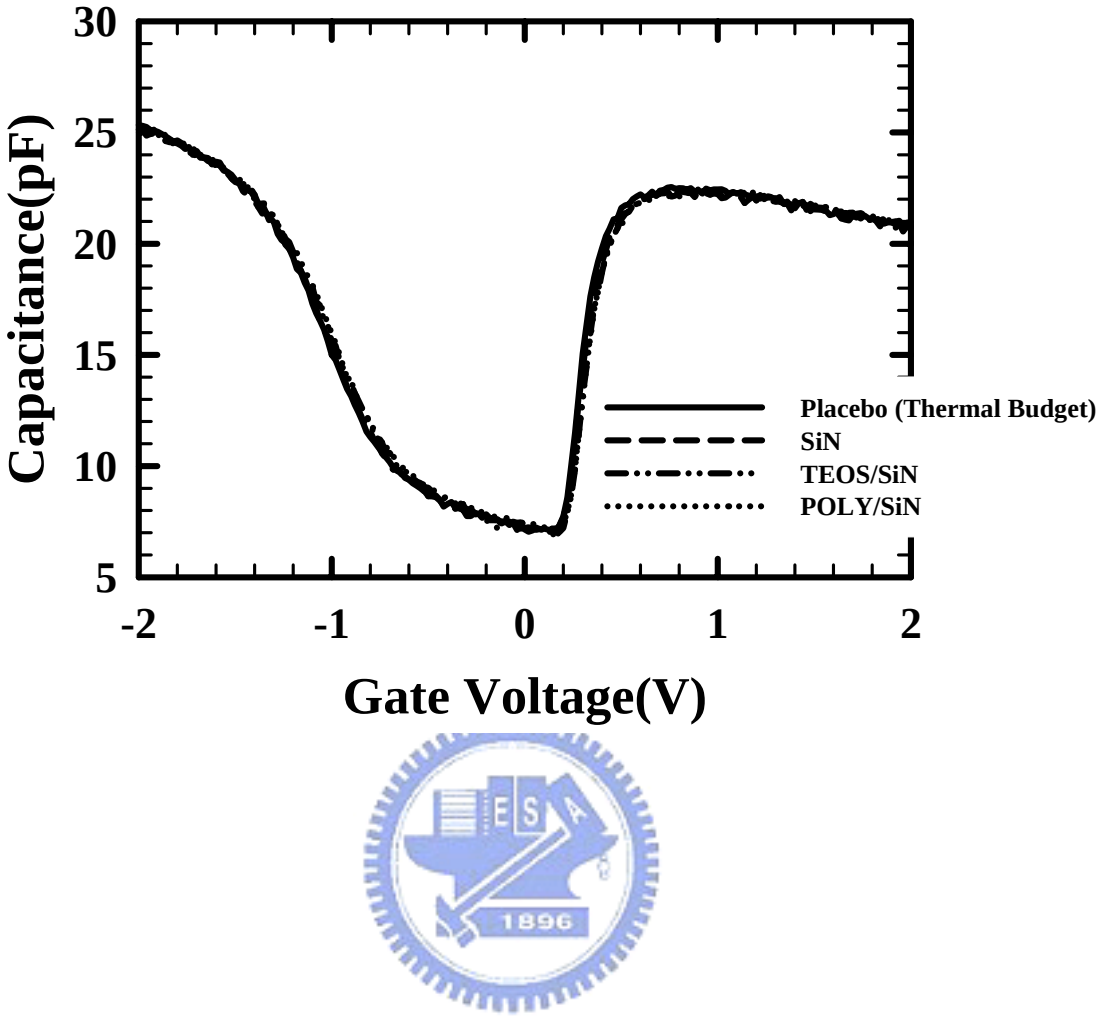


Fig. 3.3 Capacitance-Voltage(C-V) characteristics of different splits of NMOSFETs. Channel width/channel length = 50 μ m/50 μ m.

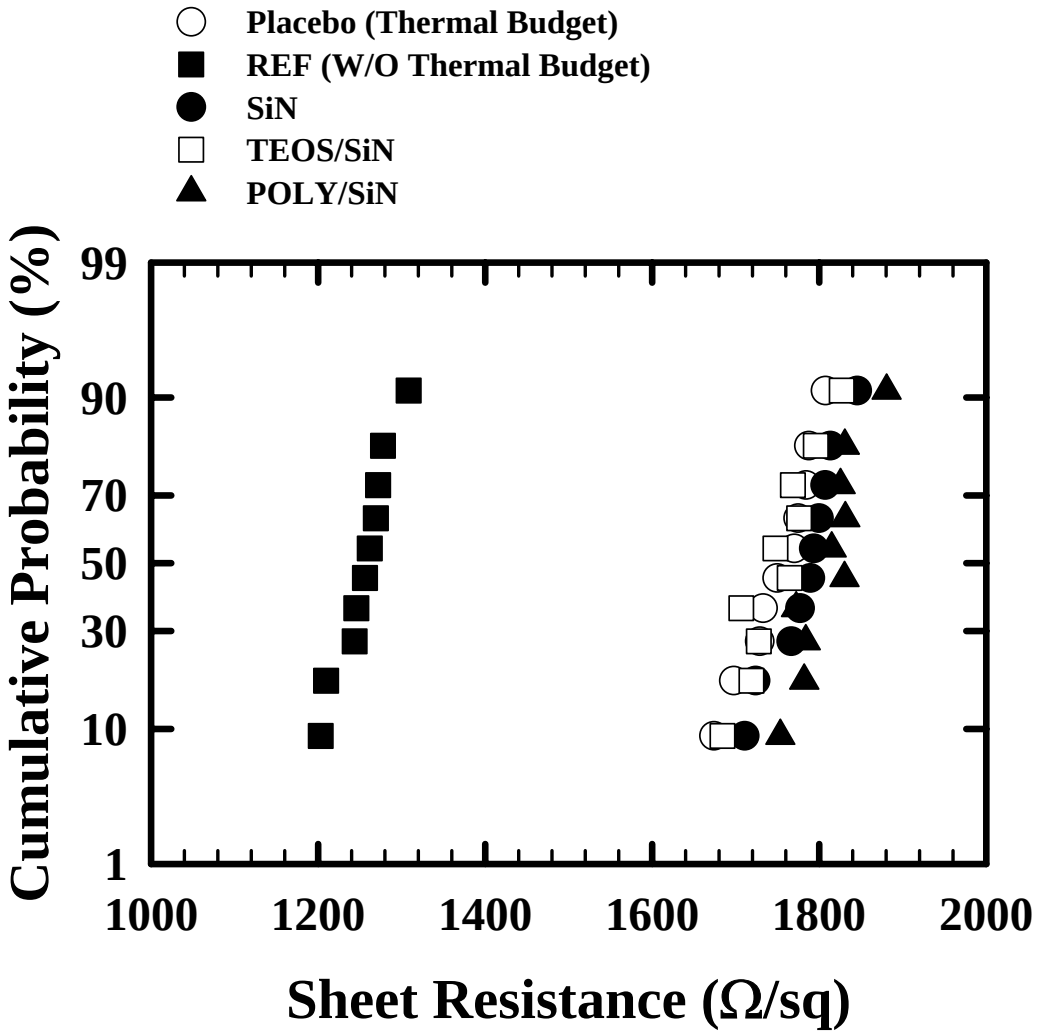


Fig. 3.4 Cumulative probability distribution of poly-gate sheet resistance for all splits of samples. The film thickness is 150nm. Doping was done by As-ion implantation at a dose of $3x10^{15}$ cm^{-2} and an energy of 10KeV. All samples received an RTA at 900℃ for 30sec. Note that the REF split skips the thermal treatment associated with the SiN deposition.

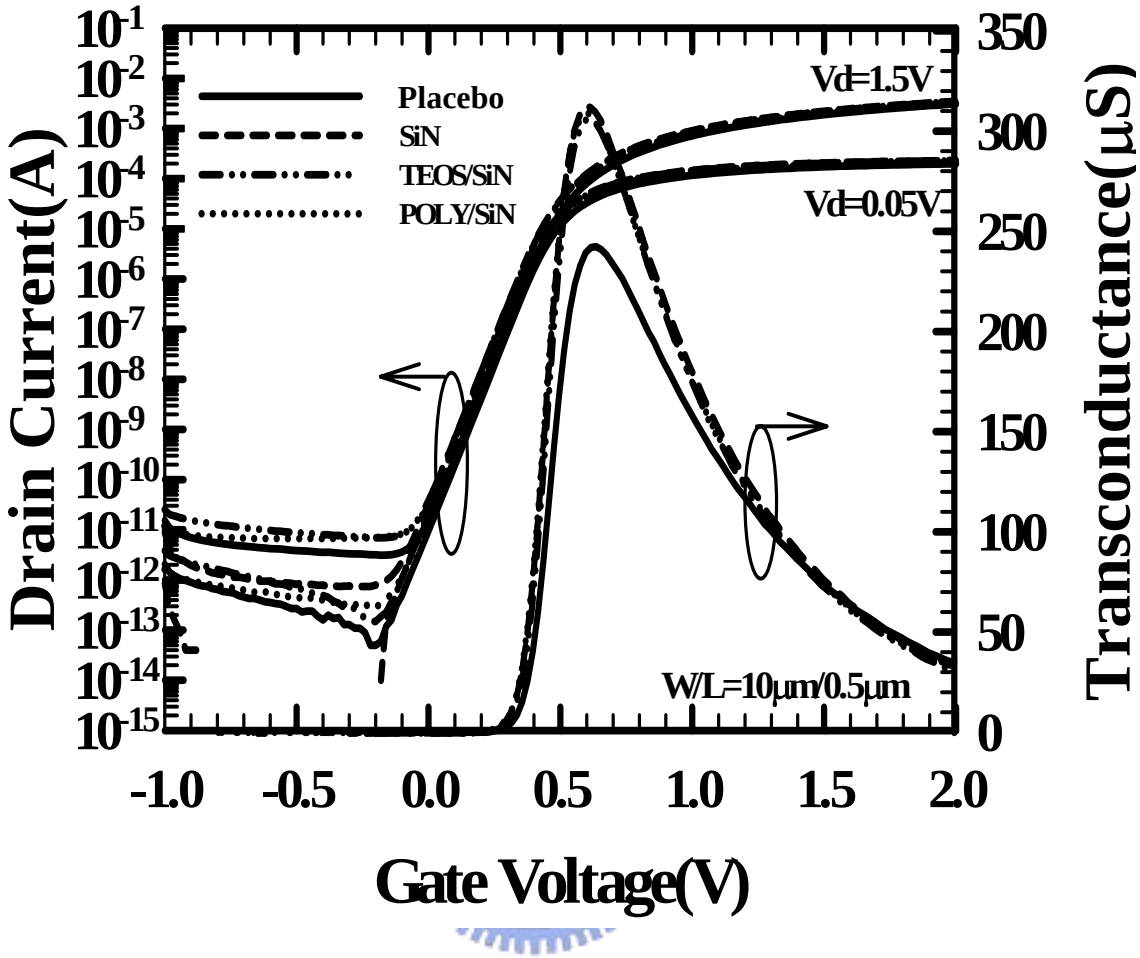


Fig. 3.5 Subthreshold and transconductance characteristics of different splits of NMOSFETs characterized at 25℃. Channel width/channel length = 10 μm/0.5 μm.

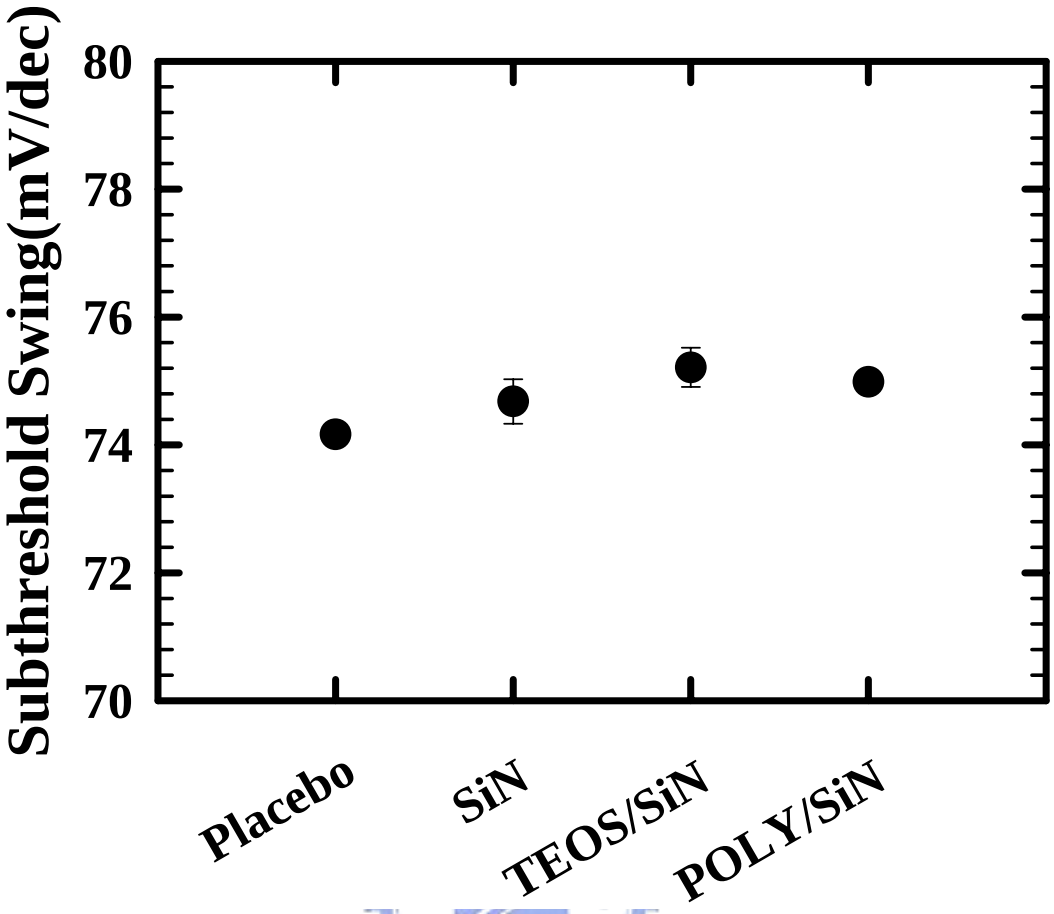


Fig. 3.6 Subthreshold swing for different splits of NMOSFETs. Channel width/channel length = 10 μ m/0.5 μ m.

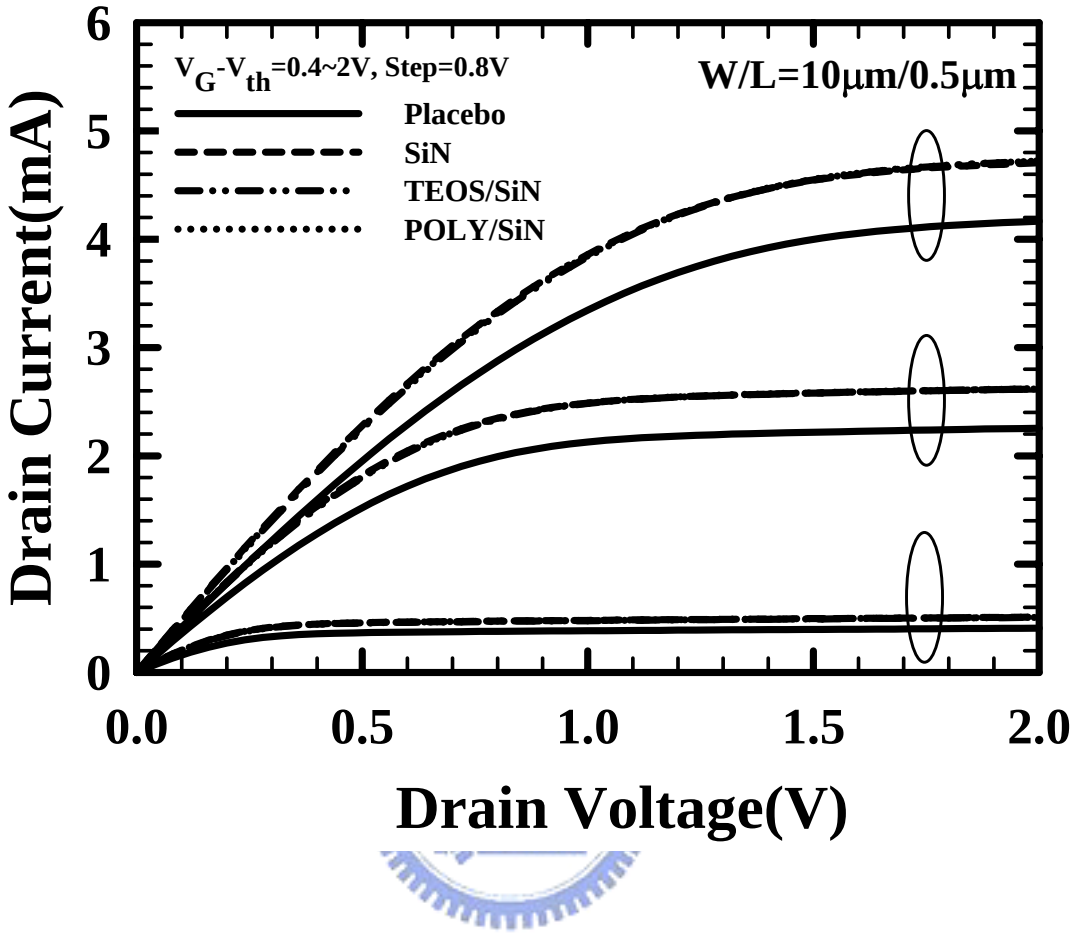


Fig. 3.7 Output characteristics of NMOSFETs for different splits, measured at 25℃. Channel width/channel length = 10 μ m/0.5 μ m.

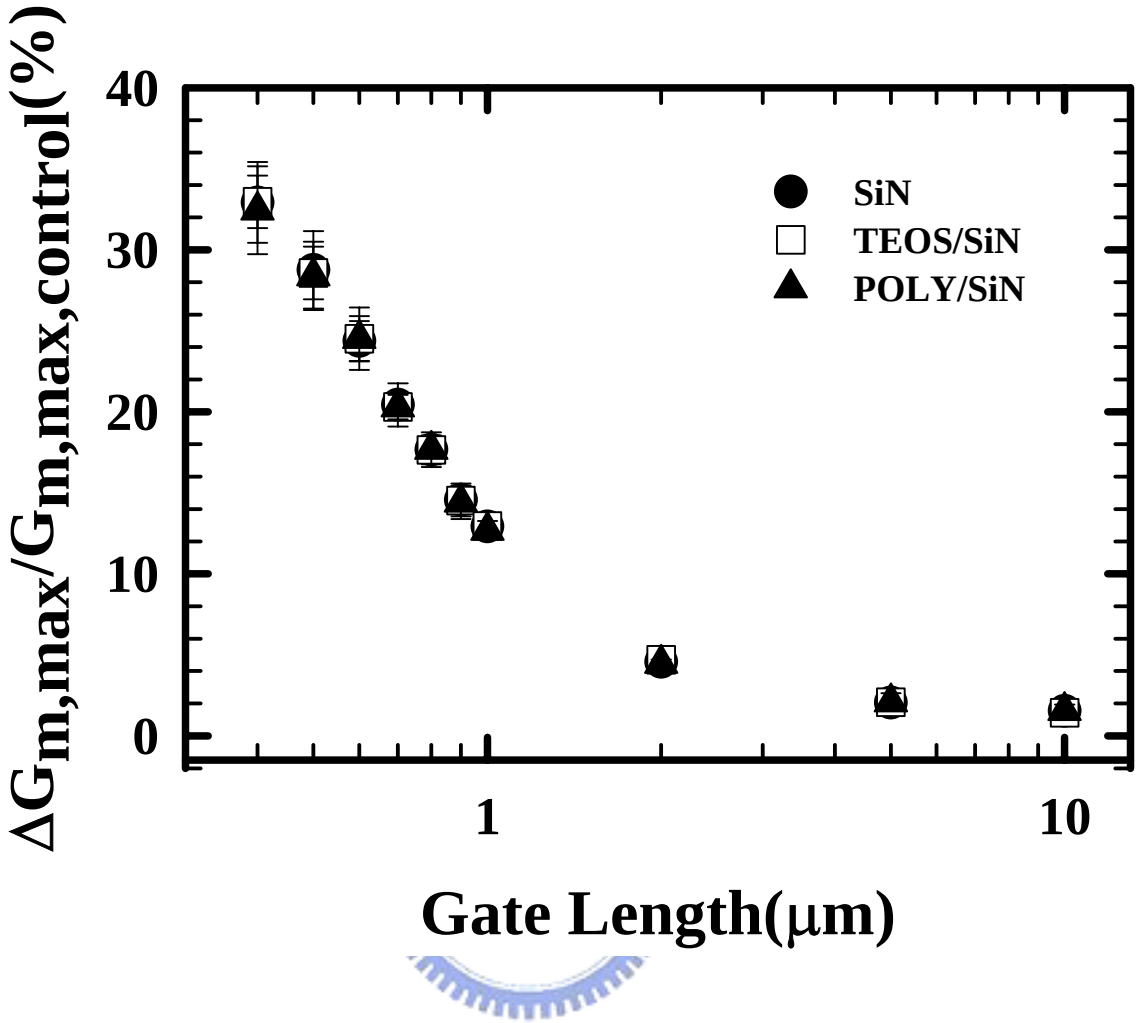


Fig. 3.8 Transconductance enhancement for different splits as a function of channel length, measured at 25°C.

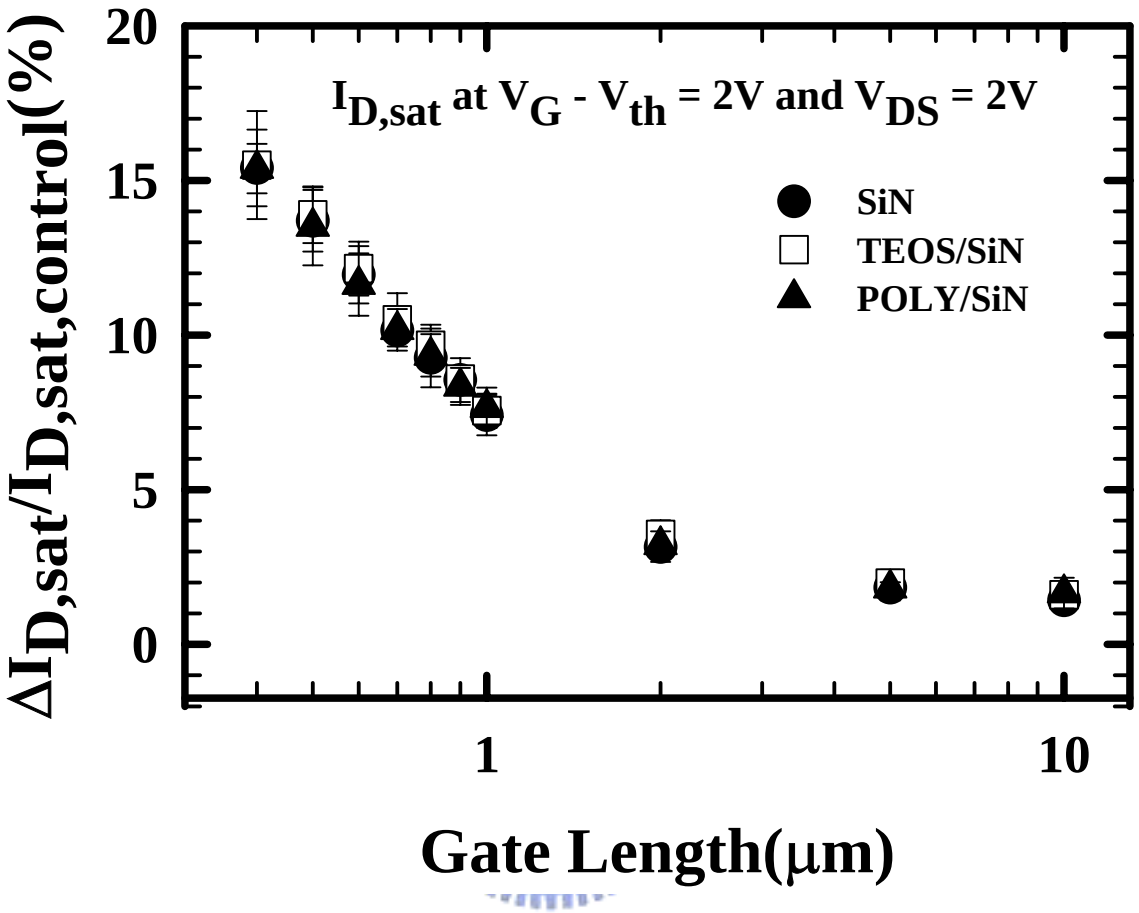


Fig. 3.9 Drain current enhancement for different splits as a function of channel length, measured at 25°C. The saturation current was measured at V_G-V_{th} = 2V and V_{DS} = 2V.

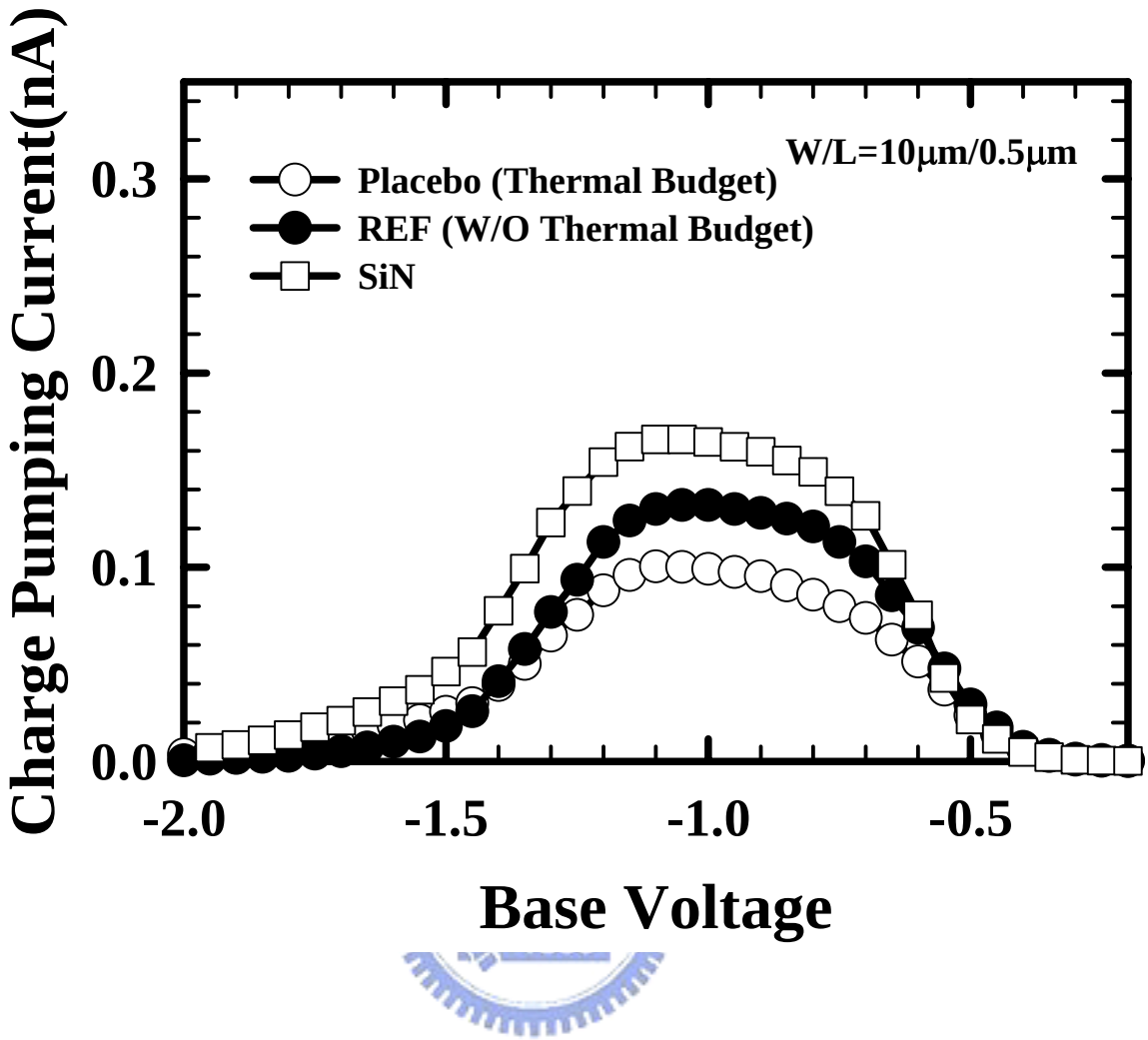


Fig. 3.10 Charge pumping current for the placebo, REF, and SiN splits. Channel width/channel length = 10μm/0.5μm.

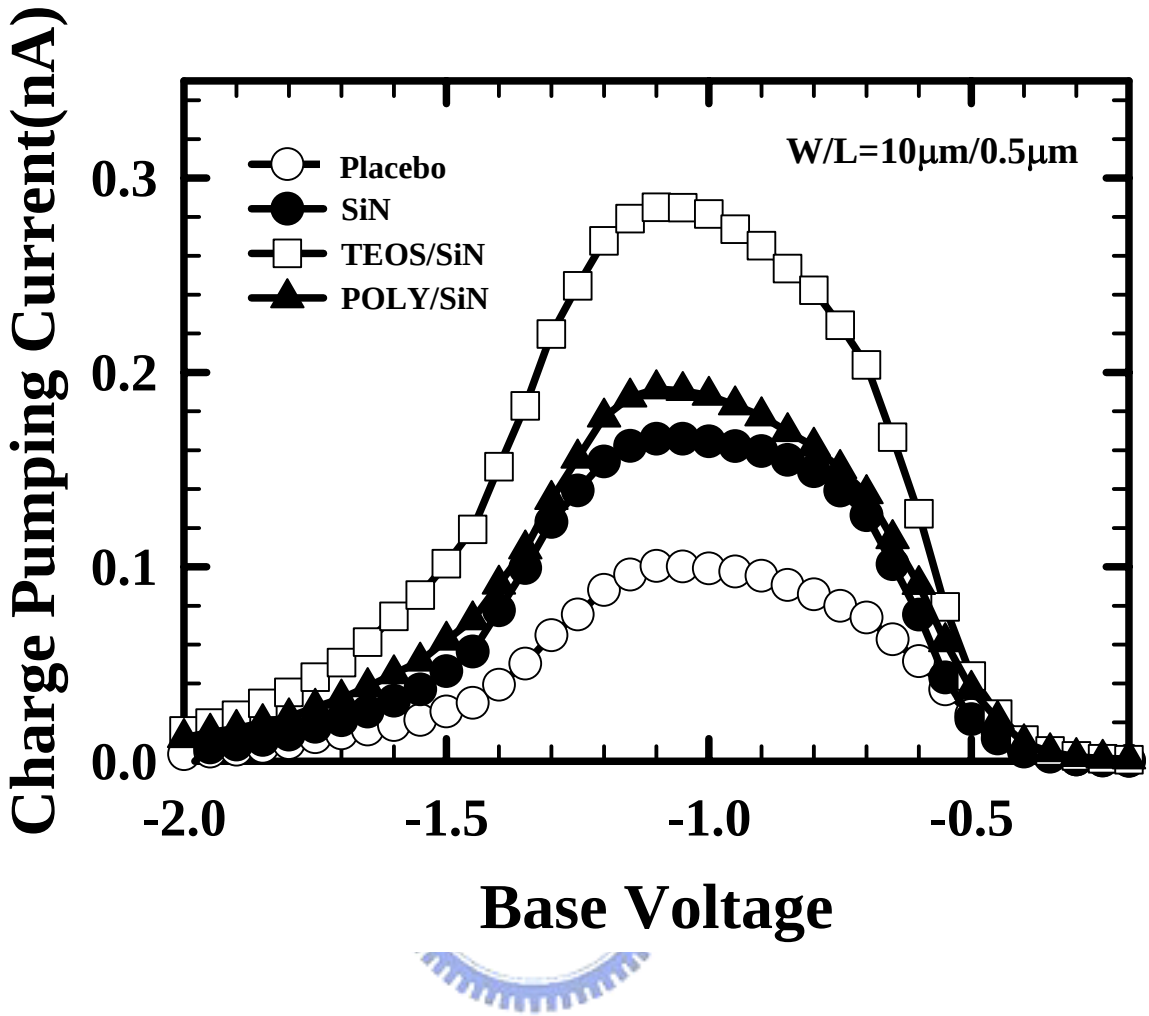


Fig. 3.11 Charge pumping current for different splits of NMOSFETs. Channel width/channel length = 10 μ m/0.5 μ m.

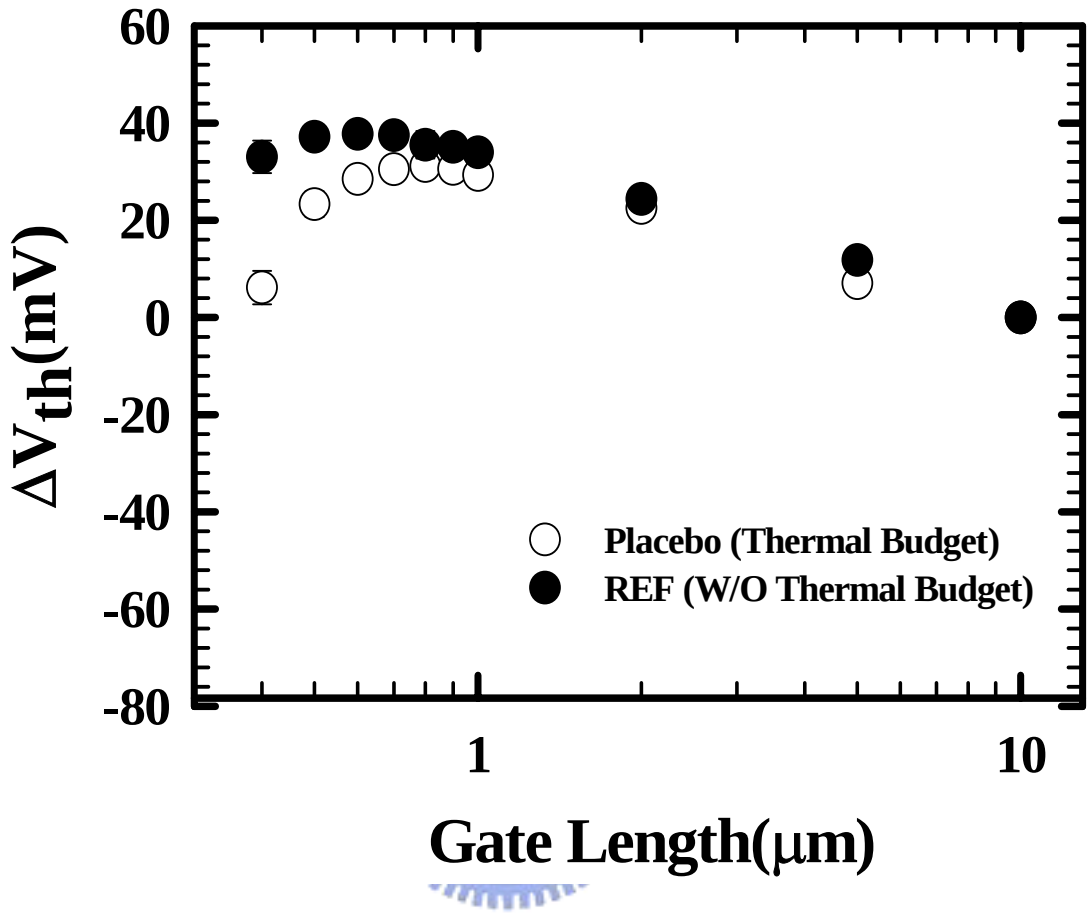


Fig. 3.12 Threshold voltage roll-off as a function of channel length for the placebo and REF splits.

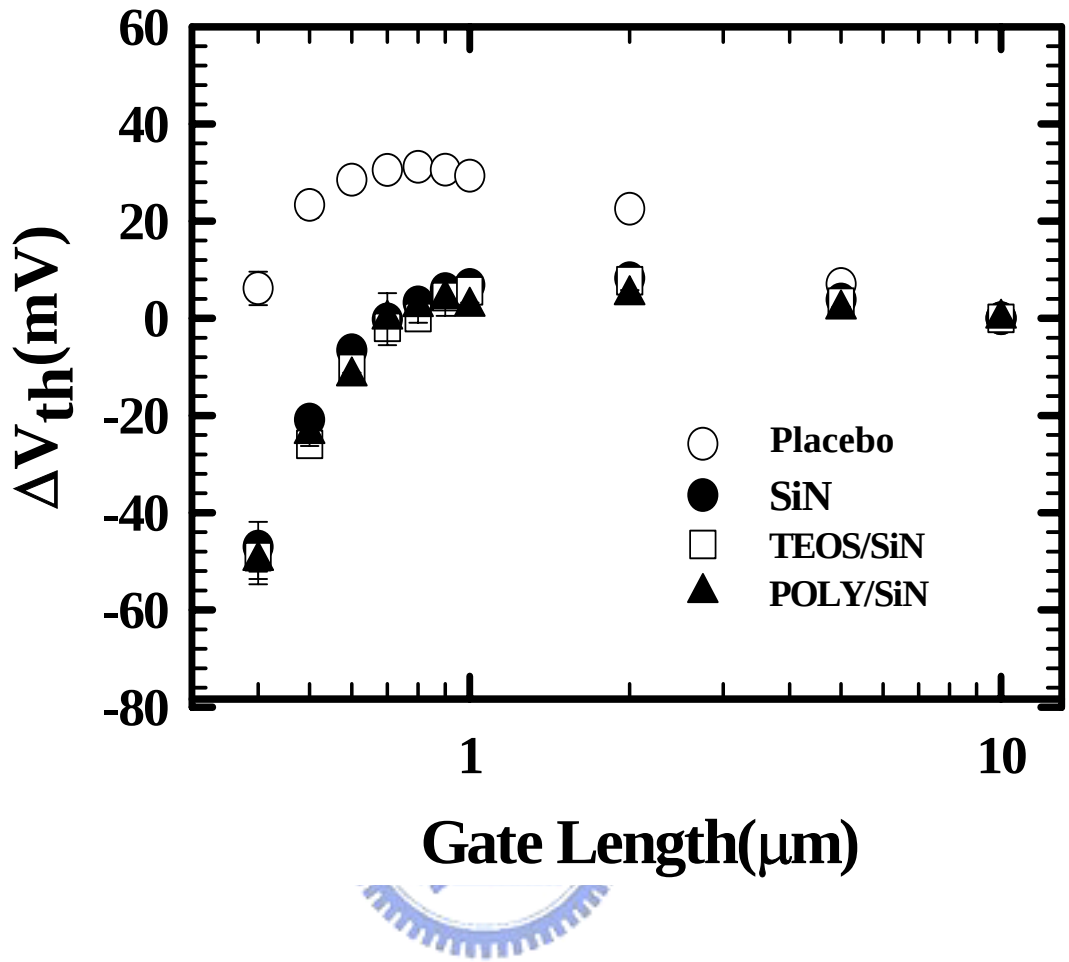


Fig. 3.13 Threshold voltage roll-off as a function of channel length for all splits.

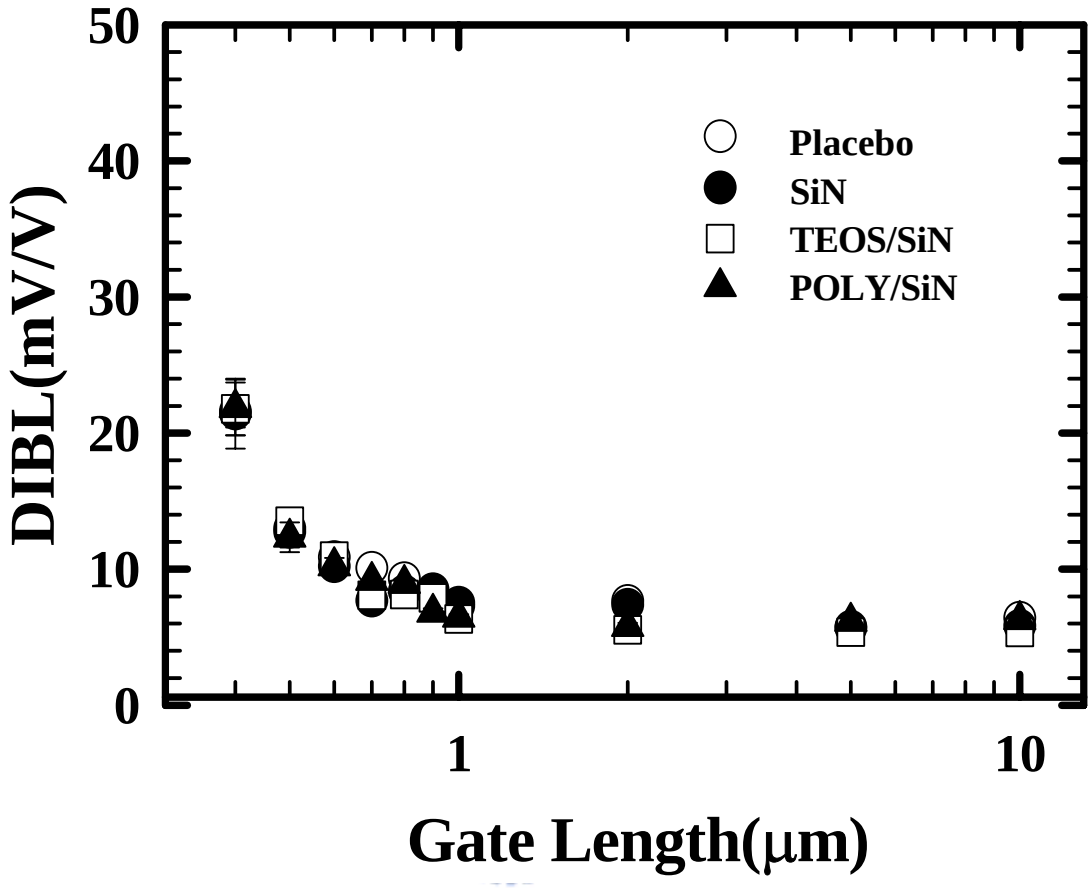


Fig. 3.14 Drain induced barrier lowing (DIBL) for different splits of NMOSFETs as a function of channel length. DIBL was evaluated by measuring the drain current change as V_{DS} was increased at some fixed gated voltage below threshold voltage.

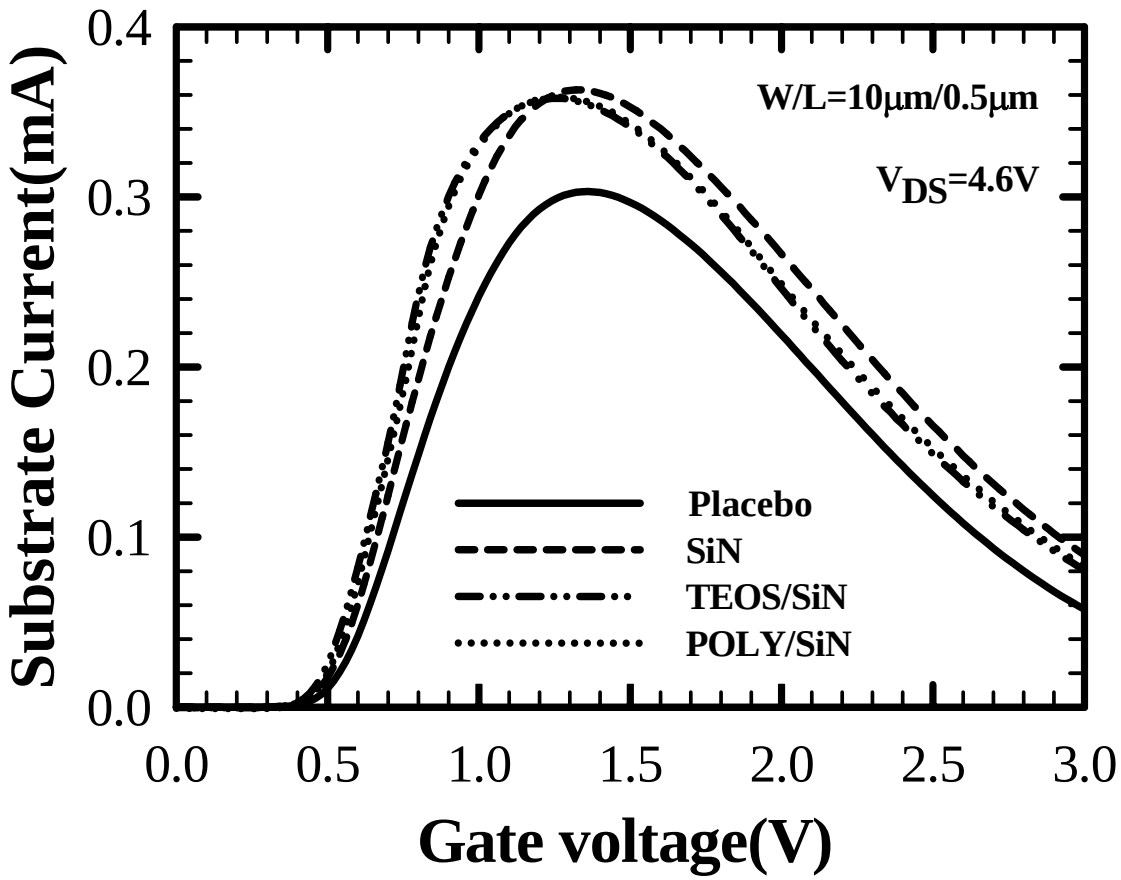


Fig. 3.15 Substrate current versus gate voltage for different splits of NMOSFETs. Channel width/channel length = 10 μ m/0.5 μ m.

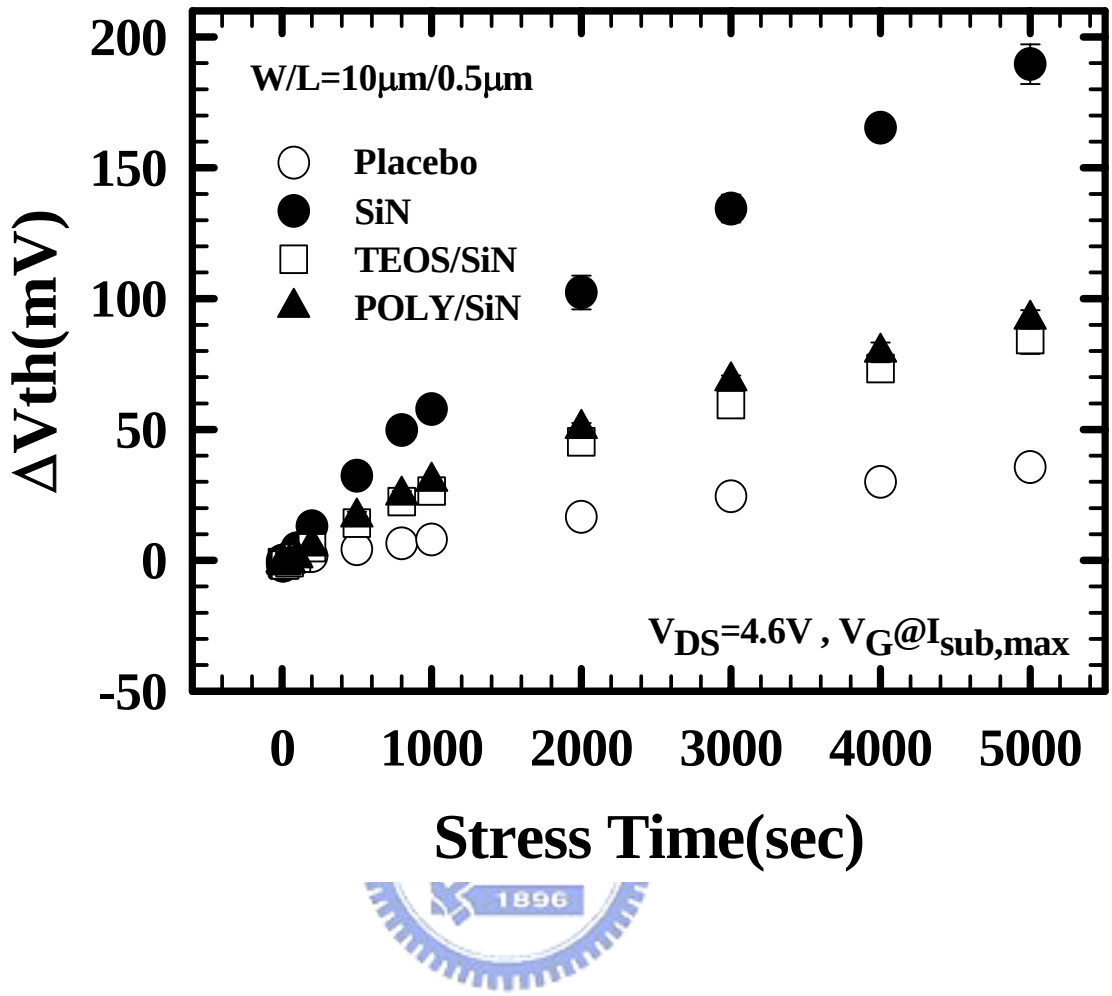


Fig. 3.16 Threshold voltage shift after hot-electron stressing performed at V_{DS}=4.9V and V_{GS} at maximum substrate current for all splits of devices with channel width/channel length = 10 μ m/0.5 μ m.

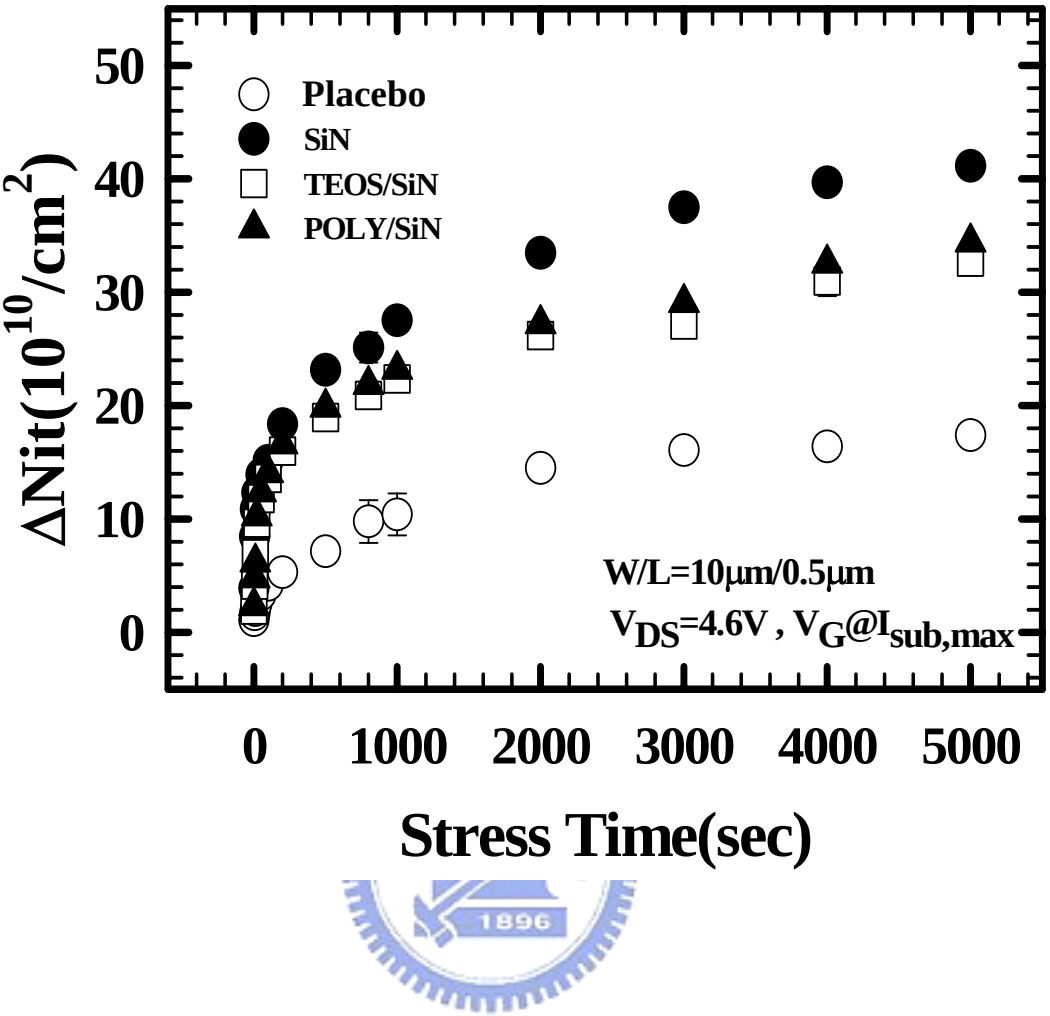


Fig. 3.17 Interface trap density generation measured after hot-electron stressing performed at V_{DS}=4.9V and V_{GS} at maximum substrate current for all splits of devices with channel width/channel length = 10 μ m/0.5 μ m.

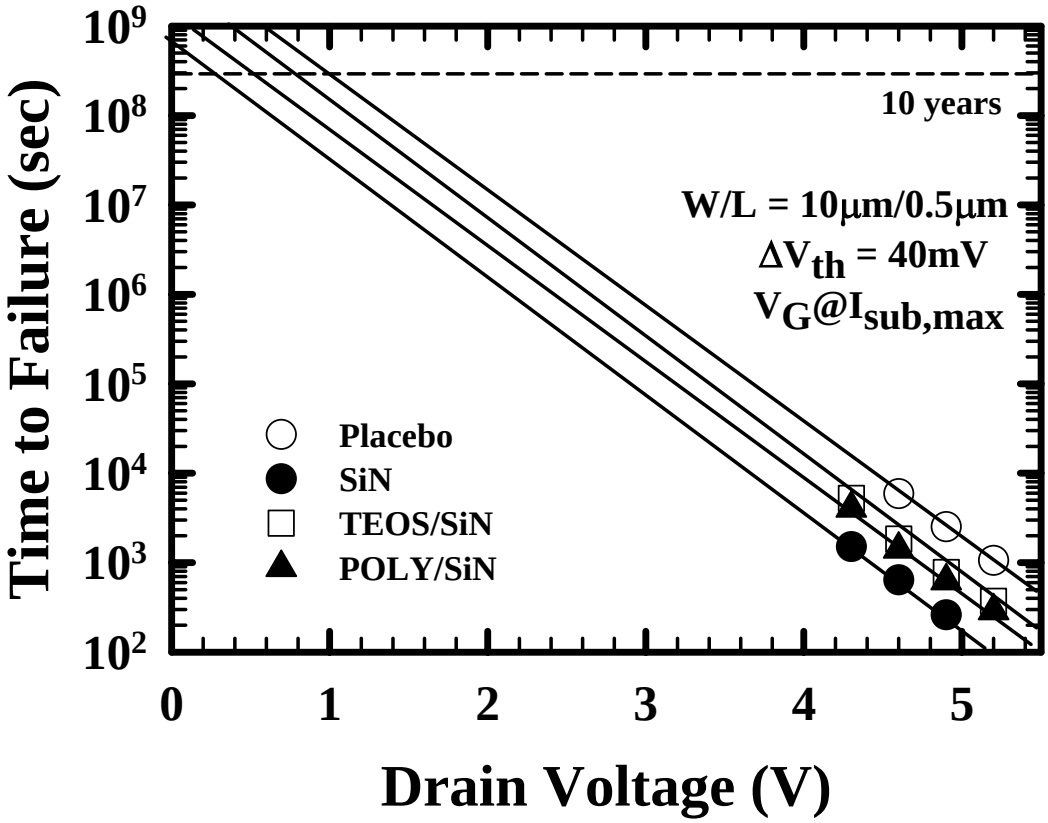
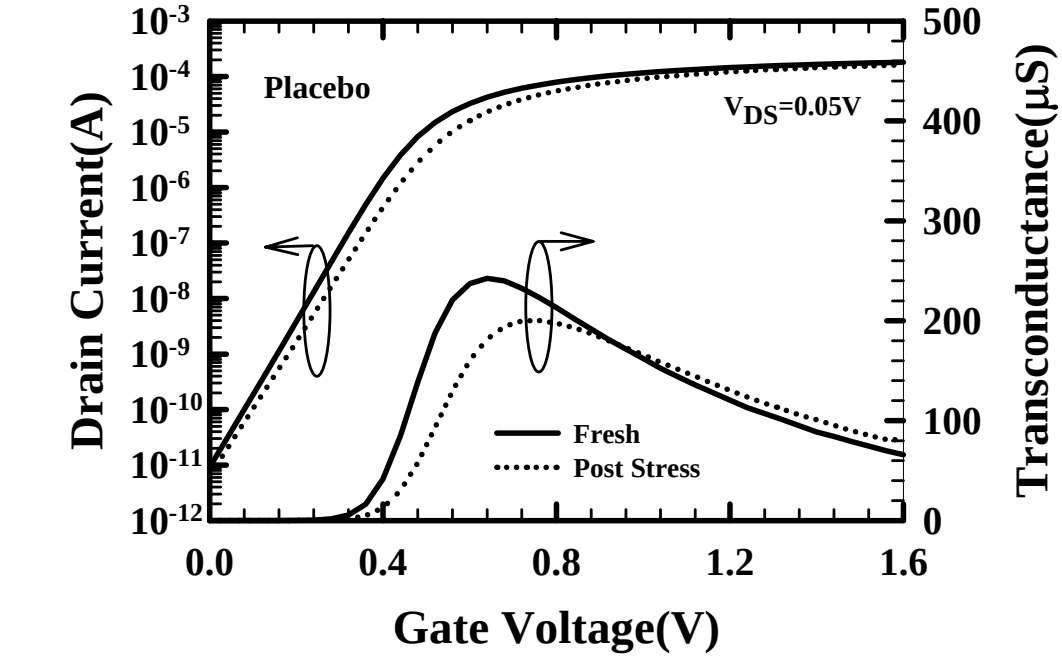
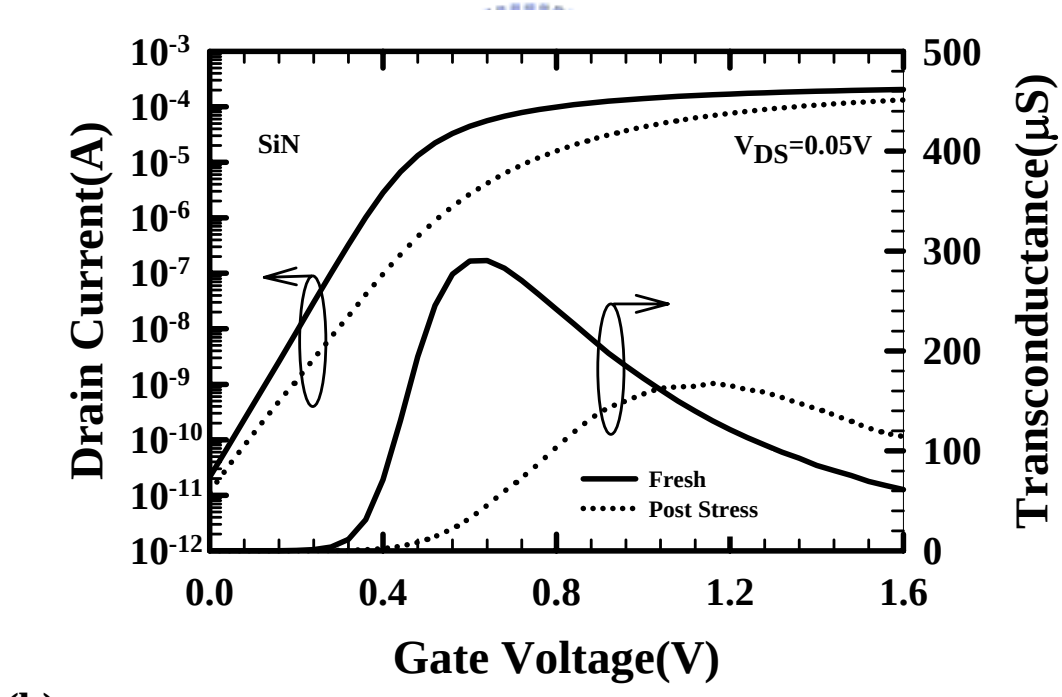


Fig. 3.18 10-year lifetime projection for the placebo, SiN, TEOS/SiN, and POLY/SiN samples.

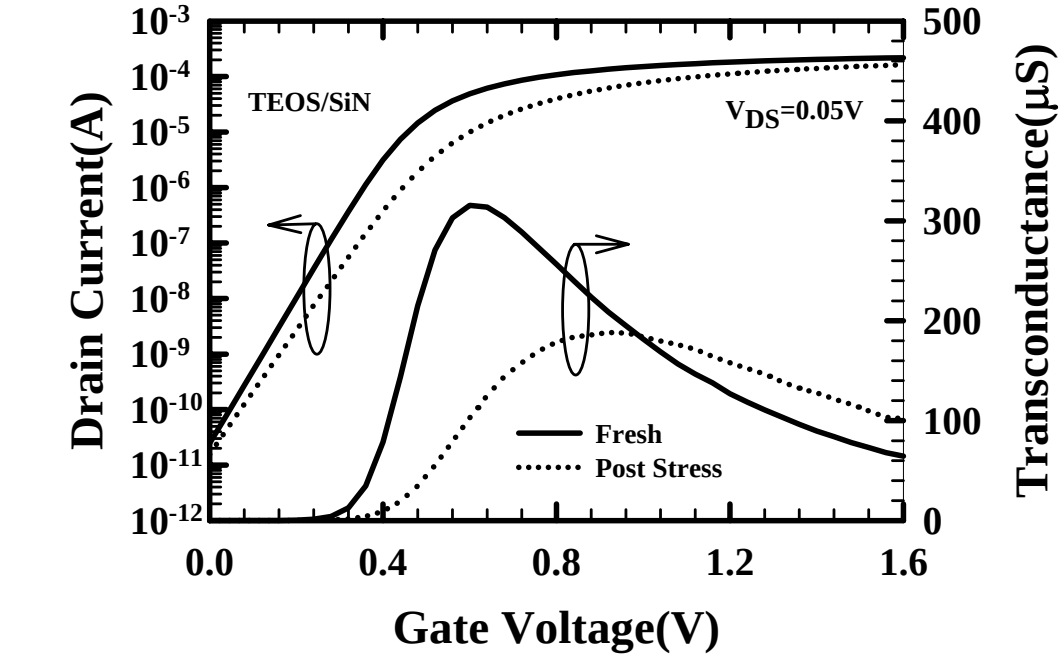


(a)

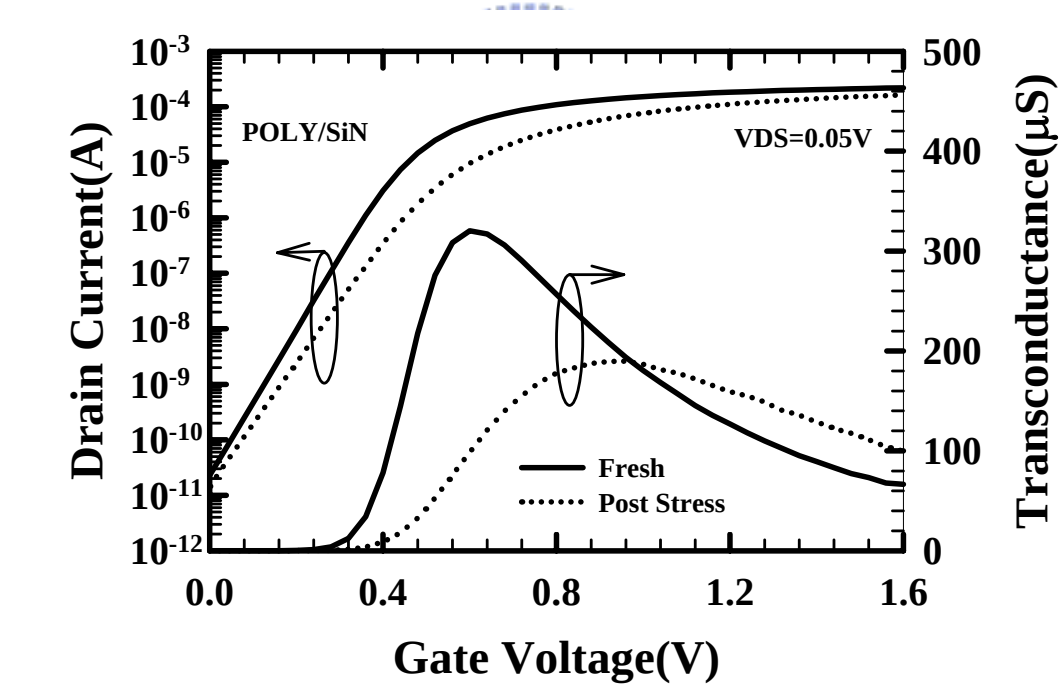


(b)

Fig. 3.19 Subthreshold characteristics and transconductance of devices before and after 5000 sec hot-electron stressing. Channel width/channel length = 10 μm/0.5 μm. (a) Placebo sample. (b) SiN sample.



(a)



(b)

Fig. 3.20 Subthreshold characteristics and transconductance of devices before and after 5000 sec hot-electron stressing. Channel width/channel length = 10 μm/0.5 μm. (a) TEOS/SiN sample. (b) Poly/SiN sample.

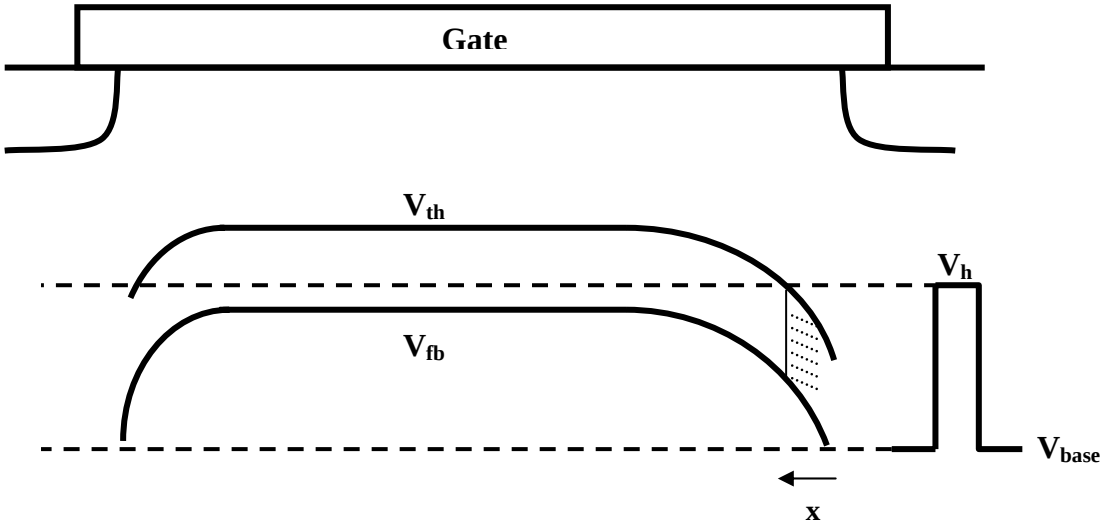


Fig. 3.21 Variation of local threshold voltage and flat-band voltage across the device channel caused by the variation of lateral doping concentration.

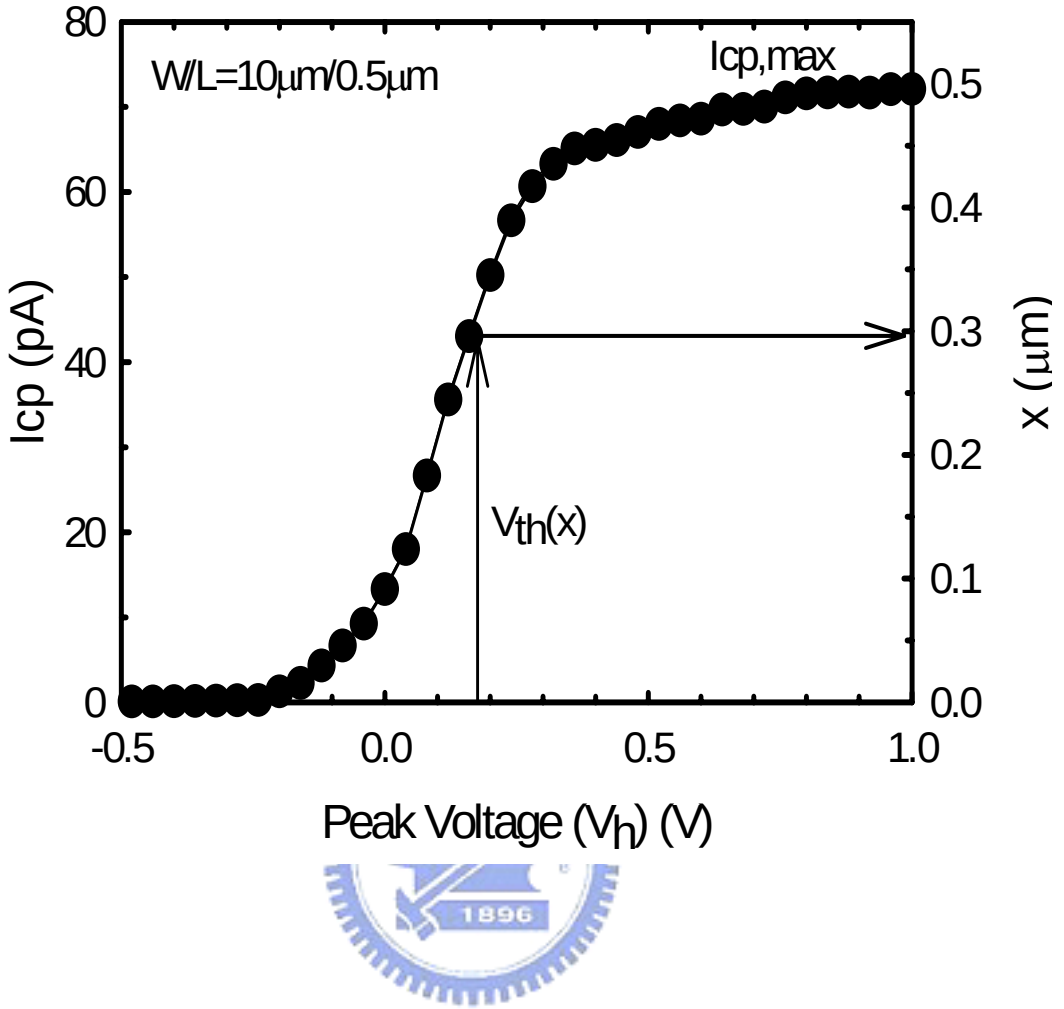


Fig. 3.22 Derivation of the relationship between local threshold voltage and lateral distance x from the single-junction charge pumping data of the Placebo device.

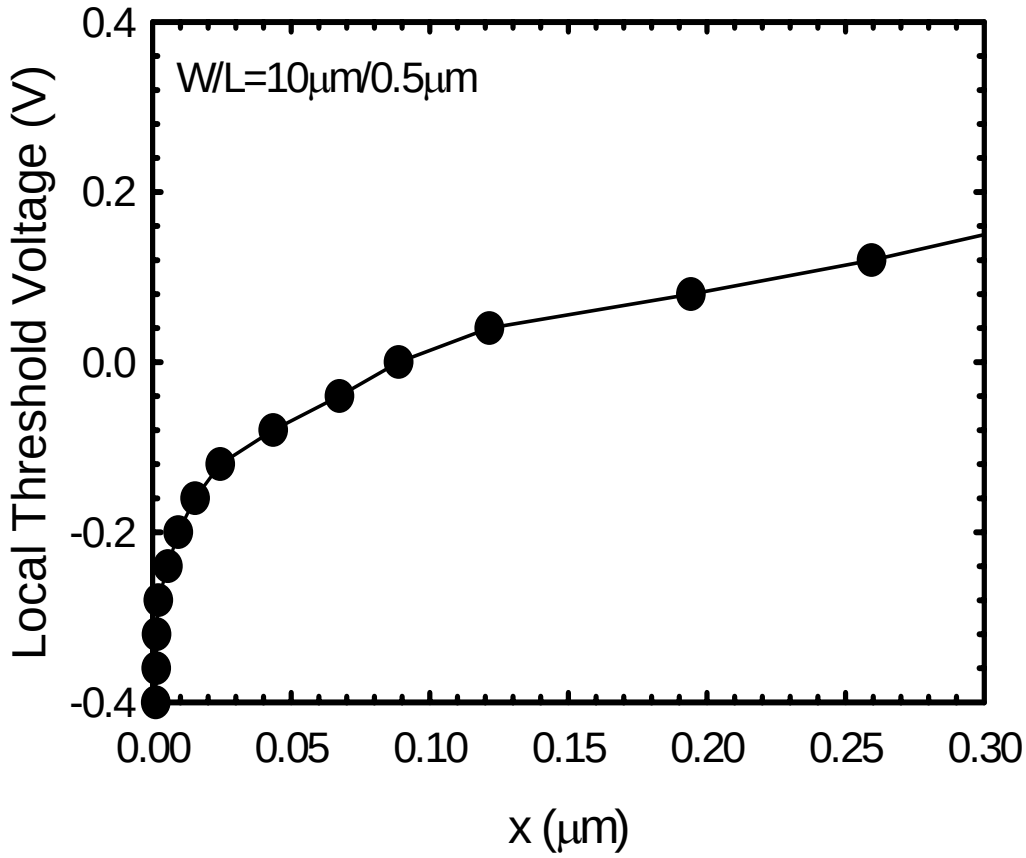


Fig. 3.23 Extracted lateral profile of local threshold voltage near the graded drain junction in the placebo sample.

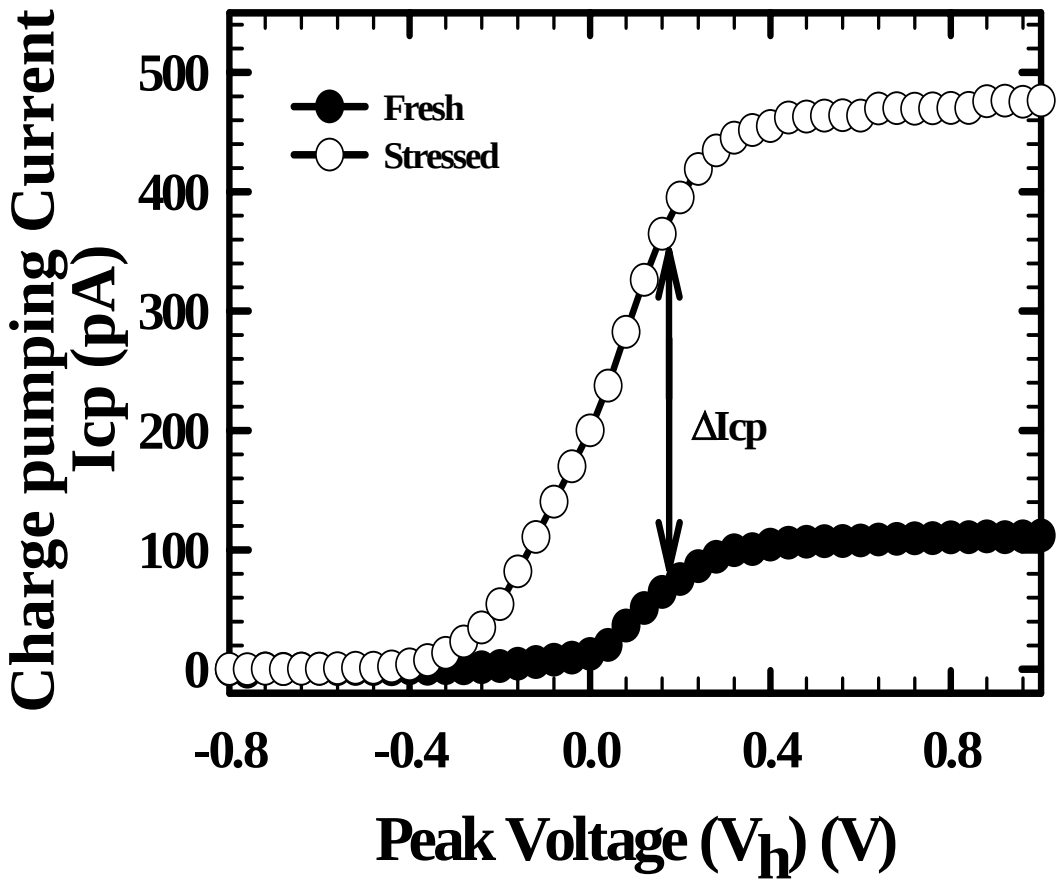


Fig. 3.24 Charge pumping current before and after 100 second hot-electron stressing (V_G@$Isub_{max}$ and V_{DS}=4.9V). Channel width/channel length = 10 μ m/0.5 μ m.

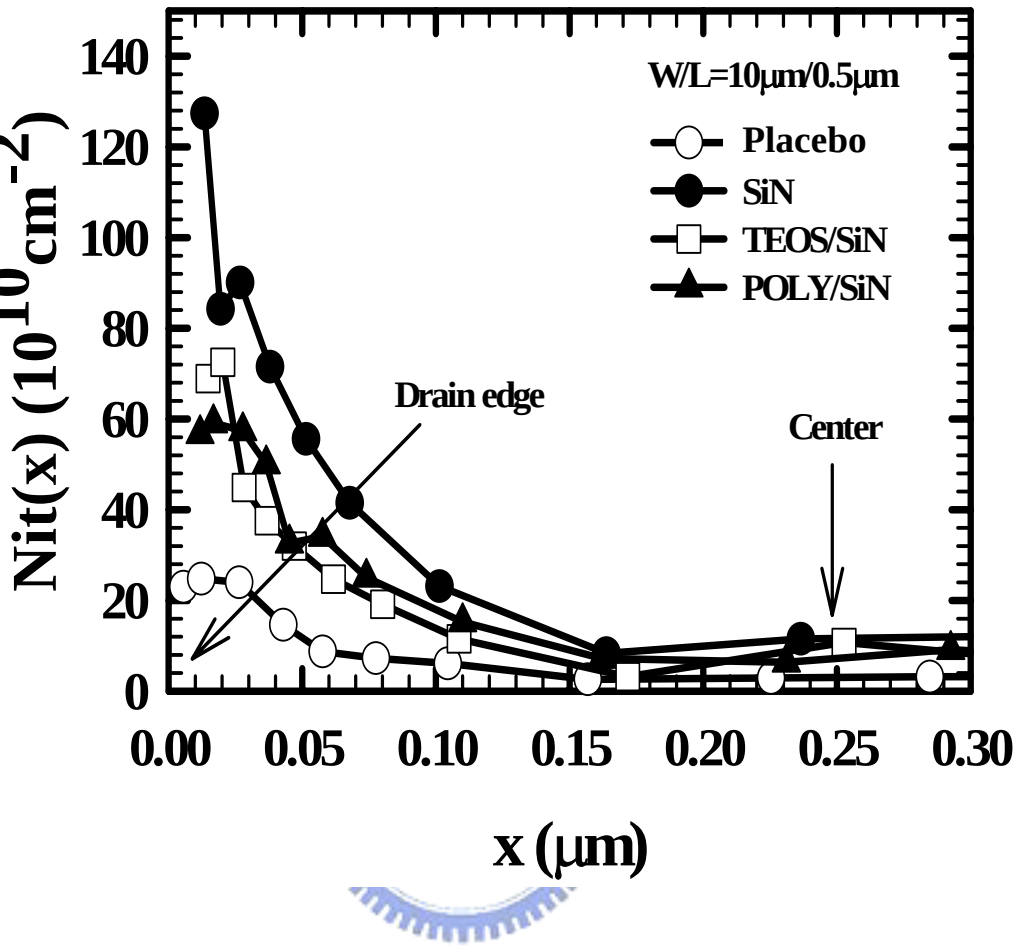


Fig. 3.25 Lateral profile of interface state generation under different split conditions.

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論文題目: 一個用來改善形變通道 N 型金氧半場效電晶體熱載子可靠度的方法

A Novel Approach to Improve Hot Carrier Reliability of Strained-Channel NMOSFETs