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## 碩 士 論 文

紫 外 光 在 非 晶 矽 薄 膜 電 晶 體 特性 影 響 之 研 究 E Fls) Effect of UV Illumination on Physical

Characteristics of a-Si:H Thin Film Transistors

研 究 生:陳忠樂 指導教授:羅正忠 博士 李義明 博士

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# 紫 外 光 在 非 晶 矽 薄 膜 電 晶 體 特性影響之一研究 Effect of UV Illumination on Physical

## Characteristics of a-Si:H Thin Film

## Transistors

研 究 生:陳忠樂 Student:Chung-Le Chen 指導教授:羅正忠 博士 Advisor:Dr. Jen-Chung Lou 李義明 博士 Advisor:Dr. Yiming Li



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學生:陳忠樂 指導教授:羅正忠 博士 李義明 博士

國立交通大學 電子工程研究所 碩士班



 本論文首度研究非晶矽薄膜電晶體經紫外光照射後電性變化的物理機制, 包括陷阱 的狀態、濃度以及載子復合產生速率。 為了使分析的元件特性更符合實際現象, 模擬上, 非晶矽層中陷阱的分佈與濃度耦合於泊松方程式;而載子復合產生速率則耦合於電子/電洞 連續方程式, 以及晶格熱流方程式。

 此反轉堆疊式非晶矽薄膜電晶體模擬的電流電壓曲線在不同的紫外光照射次數大小 皆配合量測實驗被仔細校估過。 主要的電性結果顯示, 在紫外光照射後, 主要有三個現 象產生, 即臨限電壓的增加、 漏電流的下降以及驅動電流的下降。 隨著紫外光照射次數 增加, 非晶矽層中陷阱增加。 這會使有效穿遂電子質量增加以及費米能階降低。 此研究 提供了光照射後的影響及機制之模型化以改善非晶矽薄膜電晶體之開關特性。

## **Abstract (in English)**

I n this study, the physical mechanisms of UV illumination for a-Si:H TFTs including the state and density of traps are for the first time studied and calibrated. To characterize and optimize the characteristics of devices, Poisson, electron/hole continuity, and lattice heat flow equations are solved coupling with density and distribution of trap states in the a-Si:H layers. The I-V characteristics of the inverted staggered a-Si:H TFTs with different magnitude of UV light illumination is calculated and calibrated with experimental  $\mu$  and  $\mu$ measurements. The preliminary result shows that the traps states in the a-Si:H layer alter the effective mass of electrons and the movement of Fermi level after UV illumination. This study provides an insight into the impact of photo-illumination and the mechanism for device modeling to improve the switching characteristics of amorphous silicon thin-film transistors.

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陳忠樂 謹誌

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## **Chapter 1**

## **Introduction**

I n this chapter, we introduce the background, consisting of device characteristics and stability mechanism, and motivation. There are more discussions about a-Si TFTs, such as photodegradation, technologies, static characteristics, dynamic characteristics, stability, and so on. Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) have recently been widely used as switching devices for large-area electronics such as active matrix liquid crystal displayers (LCD). Unfortunately, a-Si:H TFT is high photoconductivity and may result in high leakage current under light illumination, especially those projectors and displays with high intensity backlight illumination. The leakage current thus causes a voltage drop and then induces insufficient rotation angle of liquid crystal. There are some solutions to this problem.

### **1.1 Background**

In this section, we describe the effect of photoillumination on a-Si TFT. The structure of a-Si TFT may be divided into four types, in which the inverted-staggerd type is the most popular one. The electric characteristics may be influenced by two kinds of trap states. Others such as effects of redistribution, gate insulators and bias-temperature stress on a-Si TFTs are also discussed in this section.

#### **1.1.1 Device Characteristics**

Amorphous silicon thin-film transistors were first proposed for device applications LeComber in 1979 [1]. Since then, there has been enormous amount of activity, worldwide, that has resulted in the utilization of these devices in a variety of applications. In recent years, the hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) have been widely used as switching devices for large-area electronics such as active matrix liquid crystal displayers, linear arrays of image sensors for facsimile readers [2], and linear arrays for driving new page-width printers [3]. For these applications, one requires a large area, lowtemperature technology compatible with cheap glass substrates. As the TFT turns on, both the liquid crystal capacitance and the associated capacitance are charged, which have to sustain enough voltage for the rotation of liquid crystal. Unfortunately, a-Si:H TFT is high

photoconductivity and may result in high leakage current under light illumination, especially those projectors and displays with high intensity backlight illumination. The leakage current thus causes a voltage drop and then induces insufficient rotation angle of liquid crystal. Therefore, when employing an a-Si:H layer, the main objectives are to enhance the field effect mobility and to reduce the off-state leakage current under light illumination. Mobility has a direct influence on the display performance, particularly in high-resolution displays or sensors. On the other hand, a-Si:H has high photoconductivity which results in high off-state leakage current of a-Si:H TFTs under light illumination [4].

The observation of metastable changes in a-Si:H goes back to the work of Staebler and Wronski [5], who found in 1977 that the dark conductivity and photoconductivity of glowdischarge deposited amorphous silicon can be reduced significantly by prolonged illumination with intense light (600-900 nm), and can be reversible with low-anneal temperature  $(\geq 150 \degree C)$ . Also, they think that the effect of the optical exposure is to increase the density of gap states. The authors proposed that these effects were due to reversible changes in the bulk density of states which caused a shift of the Fermi level and, hence changed the dark conductivity. Thereafter, in 1982, Powell, Easton, and Nicholls [6] presented the results of the measurements of the field-effect conductance of amorphous silicon, which was subjected to the same cycle of annealing and illumination reported by Staebler and Wronski. The cycle of annealing and illumination has two effects: to change the threshold voltage and to change the off conductance. Moreover, they considered the changes in fieldeffect conductance due to annealing and illumination that would be expected according to the bulk [7] and surface models [8]. According to the bulk model, illumination causes a metastable increase in the bulk density of states in the semiconductor. The charge state and energy position of the defect states must be such that they cause the Fermi level to move away from the conduction band after illumination. And the surface state density is negligible [6]. On the other hand, according to the surface model, it is proposed that there is positive fixed charge density in nitride, leading to an accumulation layer in the semiconductor. Illumination leads to a high density of mobile electrons in the semiconductor, some of which tunnel into traps in the insulator, thereby neutralizing the positive fixed charge and reducing the space-charge region in the semiconductor. And the off conductance would be determined by a space-charge region at the opposite side of the film, which would not be much affected by the gate electrode. On the other hand, if the surface effect occurred only at the silicon-nitride interface, this would result in only a change in the threshold voltage and no change in the off conductance [6]. Therefore, the field-effect of a-Si TFTs may be explained by either the density of states in amorphous silicon layer or surface states at both sides of the amorphous silicon layer, i.e. front and rear sides.

In addition to above description about photodegradation, there are more discussions

about a-Si TFTs, such as technologies, static characteristics, dynamic characteristics, stability, and so on [9].

Amorphous silicon thin-film transistors can be made with a wide variety of structures and materials. Basically there are four types of planar TFT, i.e. staggered, coplanar, inverted-staggered, and inverted-coplanar types, defined by the order of deposition of the semiconductor layer, the gate insulator layer, the source-drain contacts, and the gate electrode. The staggered TFT structures have the gate source and drain contacts on one side of the semiconductor and the gate electrode on the opposite side, while the coplanar structures have all three electrodes on the same side of the semiconductor film. In the "inverted" structures, the gate electrode is the first layer deposited on the glass substrate. For a-Si TFTs, the most popular structure and the one responsible for the state of art performance, is the inverted-staggered TFT, which uses silicon nitride as the gate insulator [10, 11]. In contrast to poly-Si TFTs, which are usually coplanar, which is the nearest thin-film analog of crystalline Si MOSFET.

The application of a gate voltage leads to an approximately exponential increase in the source-drain current, at first, followed by a linear increase in current at higher gate voltages. Typical threshold voltages are in the range 2-4 V and state of the art mobilities are in the range  $0.4$ -1.0 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>. Also, for most transistors, the threshold voltage (given by the intercept of the linear region) and the effective mobility (given by  $\mu_{fe}$ =

 $(d_{ins}L/\varepsilon V_D W)(dI_D/dV_G)$ , where  $dI_D/dV_G$  is the slope of the linear region). The density of states in amorphous silicon layer can be divided into two types, tail states and deep states [6]. The tail states are the Si conduction band states broadened and localized by the disorder to form a "tail" of localized states just below the conduction band mobility edge. These states are so-called the weak silicon bond. The deep states originate from defects in the a-Si network. These are thought to mostly consist of Si dangling bonds, which have wide range of energies because of the variations in local environments, and this can be improved by incorporating hydrogen, forming hydrogenated amorphous silicon (a-Si:H). For positive gate volts, less than the threshold voltage, the energy bands bend downward and the Fermi level moves through the deep states, which are than occupied. At the same time, some space charge is located in the band-tail states, but the occupancy of these states is low, since they are well above the Fermi level and so the total space charge is dominated by the deep states. And this leads to approximately exponential increase in the source-drain current. Above the threshold, the space charge in the band-tail states exceeds the space charge in the deep states, even though the Fermi level is still below the tail states. And this leads to a linear increase in source-drain current.

In most applications, the thin-film transistor acts as a switch, where typically the transistor is switched on for tens of microseconds and then switched off for tens of milliseconds. Shortly after switch on, the deep states begin to trap charge but the rate of trapping is much

higher near the gate insulator interface, due to much higher density of free carriers, and thermal equilibrium occupancy of the deep states is soon established in that region. However, trapping of free carriers in the region far from the gate insulator interface continues, leading a transfer of charge from the region near the gate insulator interface to the region far from the gate insulator interface and a change in the band-bending profile, i.e. reducing the downward band bending [12]. As a result, the redistribution of charge between the tail states and the deep states can be described as an effective dynamic threshold voltage shift, causing the reducing source-drain current [12]. When after switch off, the energy bands are pushed up and the band-tail electrons are rapidly swept out to the source and drain contacts. After that, electrons begin to emit from the deep states at a rate determined by their energy depth. This continues, building up a uniform space charge in the amorphous silicon, until the positive space charge in the silicon equalizes the negative charge on the gate. At this point thermal equilibrium is established in the region far from the gate insulator interface, but the deep states in the region near the gate insulator interface continue to emit, leading to a slow transfer of charge from the region near the gate insulator interface to the region far from the gate insulator interface and again a change in the band-bending profile, i.e. enhancing the upward band bending [12].

Stability influences the lifetime of the device, which is the most important issue. Subjecting MOS capacitor and transistors to bias-temperature stress is often used to investigate the stability of devices, by measuring the resulting threshold voltage shift. The bias-temperature stress applies constant gate voltage and constant temperature annealing for a period of time. When it comes to the stability of a-Si TFTs, two models have been proposed to account for this threshold voltage shift, namely charge trapping in the silicon nitride gate insulator [13, 14] and the metastable creation of new states in the amorphous silicon [15–17]. If charge is trapped in the nitride under higher positive bias stress (higher than  $V_{GC}$ ), then the threshold voltage for both electron and hole conduction shifts to more positive values [13]. This is because of positive fixed charge in the nitride, leading electron to be trapped. It is interesting that silicon nitride is used in memory devices utilizing this charge trapping phenomenon. However, the crucial difference with a-Si TFTs is that these devices operate with relatively low fields in the dielectric, by hopping at the Fermi level, but not by direct tunneling from valence band, Fowler-Nordheim injection, trap-assisted injection, constant energy tunneling from conduction band, or tunneling from conduction band to the Fermi level [13]. Both memory devices trapping and a-Si TFTs hopping occur in the middle of the band gap of nitride [14]. On the other hand, when we apply lower positive bias stress (lower than  $V_{GC}$ ), if extra deep states are created in the amorphous silicon and the Fermi level moves through these states in establishing the hole accumulation layer,

then the threshold voltage for hole conduction will shift to negative value, while the threshold voltage for electron conduction will still shift to a more positive value. There may be two models to explain the state creation, i.e. local reaction of a silicon-silicon bond with nearby hydrogen (involving breaking a Silicon-Silicon bond) and emission of hydrogen out of a silicon-hydrogen bond (involving long-range hydrogen diffusion) [18]. Moreover, because the prethreshold slope in the transfer characteristics of n-channel transistors does not change after the bias stress, the newly created states must be located below the flat-band Fermi level. Finally, the threshold shift is independent of temperature for the charge trapping, but is thermally activated for the state creation [19]. The logarithmic time dependence is observed for the charge trapping, but the power law time dependence is observed for the state creation [19].

In order to understand effects of the bias-temperature stress on a-Si TFTs, the defect pool must be first described. In previous statements, both conduction and valence tail states are described as exponential distribution [20]. Thereafter, we continue to describe the defect in a-Si:H layers. The weak bond state is converted to dangling bond, which is either positively charged or negatively charged, depending on whether the states are created under electron or hole accumulation  $[21, 22]$ . In n-type a-Si TFTs, because there are more electrons, the density of states in amorphous silicon layer contains more  $D_e$  states (negatively charged Si dangling-bond states and located in the lower part of the gap) than  $D_h$  states

(positively charged Si dangling-bond states and located in the upper part of the gap). In p-type a-Si TFTs, because there are more holes, the density of states in amorphous silicon layer contains more  $D_h$ , states than  $D_e$  states. Hence, for the reason of neutral condition, the Fermi level in n-type devices is at the position close to conduction band edge, while the Fermi level in p-type devices is at the position close to valence band edge. The equilibrium density of dangling-bond states depends on the Fermi level energy, which leads to a higher density of dangling bonds in doped amorphous silicon than undoped amorphous silicon [23]. We can also make use of a relationship between the subthreshold slopes and density of states at the Fermi level, which allows comparison of the density of states in the upper part of the gap (related to the electron subthreshold slope) to that in the lower part of the gap (related to the hole subthreshold slope) [24]. Also, the fewer  $D_h$  states, the smaller values of the electron subthreshold slope. The fewer  $D_e$  states, the smaller values of the hole subthreshold slope. Most current applications of a-Si:H TFTs use them as a simple switches , where we need a high on-off ratio for the lowest possible switching voltage. This means good n-channel transistors, with no hole conduction at moderate negative bias. For the lowest prethreshold slope, we require a low density of  $D<sub>h</sub>$  states and for the suppression of the hole conduction we require a large density of  $D_e$  states [21]. Moreover, the density of states has dependence on the gate insulator of a-Si TFTs [24, 25]. For example, when employing nitride as gate insulator, more deep states occupy in the lower part

of amorphous silicon gap. On the contrary, when employing oxide as gate insulator, more deep states occupy in the upper part of amorphous silicon gap. This is because of positive fixed charge in nitride, inducing an electron accumulation layer in the amorphous silicon, like n-type amorphous silicon, even the amorphous silicon is undoped. In the case of oxide, there is negative fixed charge, inducing an electron depletion layer in the amorphous silicon, like p-type amorphous silicon, even the amorphous silicon is undoped. Therefore, the electron threshold voltage is lower and the subthreshold slope is steeper when we use nitride as gate insulator but not oxide, which is the most suitable switch. Now, effects of the bias-temperature stress on a-Si TFTs can be perfectly described. The following description does not include the charge trapping in the gate insulators. For transistors made with silicon oxide as gate dielectric, the threshold voltage shift induced under positive bias stress is due to the creation of  $D_e$  states. The threshold shift induced by negative bias stress is due to the creation of  $D_h$  states. In transistors made with silicon nitride as gate dielectric, positive bias stress causes an increase in the density of  $D<sub>e</sub>$  states, but negative bias stress causes mainly a reduction in the density of  $D_e$  states. This is why that when we apply lower positive bias stress, the threshold voltage for electron conduction will still shift to a more positive value. Positive bias annealing of both oxide and nitride transistors leads to an increase in the density of  $D_e$  states and a reduction in the density of  $D_h$  states. Negative bias annealing leads to a reduction in the density of  $D_e$  states and an increase in the density

of  $D<sub>h</sub>$  states. Hence, the nitride TFT could be altered by negative bias annealing to become more like the oxide TFT and the oxide TFT could be altered by positive bias annealing to become more like the nitride TFT [25].

The density of states in the mobility gap of a-Si:H has been extensively studied using different experimental techniques such as field-effect measurement [26], transient and steady-state photoconductivity measurements [27], and deep-level transient-capacitance spectroscopy (DLTS) [28]. In addition, other methods such as capacitance-voltage characteristics (*C-V*) [29], and dependence of capacitance on temperature and frequency in Schottky diodes and metal-oxide-semiconductor (MOS) structures [30] are also used for study of the density of states in a-Si:H. The localized states in a-Si:H mobility gap may be modeled by exponential distributions of deep and tail states for both acceptor-like and donor-like states [31–33]. The localized states in the upper half of the mobility gap closer to the conduction band edge behave as acceptor-like states, while the states in the lower part of the gap closer to the valence band edge behave as donor-like states. Acceptor-like states are neutral when empty and negatively charged when filled with an electron, whereas donor-like states are positively charged when empty and neutral when filled with an electron. The density of states is asymmetrical in a-Si:H, i.e. the number of donor-like states in the mobility gap is higher than the number of acceptor-like states. As a result, following the neutrality condition, the position of the Fermi level in an intrinsic a-Si:H sample in the dark is closer to the conduction band edge.

#### **1.1.2 Stability Mechanism**

The degradation kinetics, i.e. the threshold voltage shifts of a-Si:H TFTs during applied gate bias, have been unified for different times and temperatures by the thermalizationenergy concept and modeled by a nonstretched exponential two-parameter fit, as described in the equation  $(1.1)$  [34].

$$
\Delta V_t(E_{th}) = [V_{bias} - V_t(0)] \times [1 - \frac{1}{\exp\left(E_{th} - E_a\right)/kT_0 + 1}],\tag{1.1}
$$

where the parameter  $kT_0$  exhibits a clear correlation to the Urbach energy, the more important parameter  $E_a$  exhibits no simple correlation on the Urbach energy, the hydrogen content, nor the hydrogen diffusion coefficient, but is believed to depend on the some deposition-induced microstructure of the material, in other words, respective of condition of the deposition [35]. Two main regimes have been identified for the rf PECVD of a-Si:H. The first is the so-called  $\alpha$  regime, in which the growth rate is lower and the partial pressure of SiH<sub>4</sub> is also lower. On the other hand, the other one is  $\gamma$  regime, in which the growth rate is higher and the partial pressure of  $SiH<sub>4</sub>$  is also higher. In addition to above description, there are more characteristics in both regimes, e.g. mobility,  $kT_0$ , and  $E_a$  [18]. Mobility has a direct influence on the display performance, particularly in high-resolution displays or sensors. It is observed that the mobility is higher in  $\alpha$  regime. From the equation (1.1),

it is found that the most stable TFT corresponds to the maximum of the ratio  $E_a$  / $kT_0$ , which corresponds the boundary of the two regimes. Luckily, the mobility still maintains a high value. In the section 1.1.1, it is referred that there may be two models to explain the state creation by bias stress. In the first model, local reaction of a silicon-silicon bond with nearby hydrogen, for example,  $Si-Si + SiHHSi \rightarrow 2SiHD$ . SiHD is a singly hydrogenated Si-Si bond, electrically indistinguishable from an isolated Si dangling bond. This rearrangement will involve the energy to break a silicon-silicon bond, which is known to be exponentially distributed in energy [36]. It is related with the defect creation. In the second model, emission of hydrogen out of a silicon-hydrogen bond (SiHHSi or  $H_2$ ) to the hydrogen mobility edge, followed by long-range hydrogen diffusion and final trapping of the hydrogen in a silicon- silicon bond, creating a SiHD defect [37]. The SiHHSi are exponentially distributed in energy based on the hydrogen density of states model [38]. This reaction path will only involve the Si-H bonding energy. It is related with the defect removal.

#### **1.2 Motivation**

Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) have recently been widely used as switching devices for large-area electronics such as active matrix liquid crystal displayers (LCD). As the TFT turns on, both the liquid crystal capacitance and the

associated capacitance are charged, which have to sustain enough voltage for the rotation of liquid crystal. Unfortunately, a-Si:H TFT is high photoconductivity and may result in high leakage current under light illumination, especially those projectors and displays with high intensity backlight illumination. The leakage current thus causes a voltage drop and then induces insufficient rotation angle of liquid crystal. A well-known popular approach to reduction of the leakage current is to reduce the thickness of a-Si:H. However, the production yield of large size TFT-LCD is decreased . Recently, Fluorine and Chlorine incorporated a-Si:H have been proposed to suppress the off-state leakage current by the shift of the Fermi level toward the valence band edge due to the increase of acceptor-liked states in a-Si:H (Fluorine) material. Observation of the increase of acceptor-liked states motivates us to explore the reduction mechanism of the off-state leakage current for a-Si:H TFTs. The influence of prolonged illumination with intense light (wavelength 600-900 nm) on the metastable changes in a-Si:H film was observed. However, seldom attention was drawn on studying the ultraviolet (UV) illumination induced metastable increase in hydrogenated materials.

Also, for transmissive LCD panel, under environmentally scattering ambient light illumination, the UV light influences the devices through black matrix with certain dosage and probability. The general RPI model is lack of photo-induced phenomenon and mechanism for numerical device simulation. It is, therefore, worth investigating the inside qualitatively

and quantitatively physical mechanism for the device compact model.

### **1.3 Outline**

The thesis is organized as follows. The fabricated process, simulation, and characterization for analyzing the device characteristics are introduced in the chapter 2, where the corresponding density and distribution of trap states and the recombination-generation mechanisms consisting of Shockley-Read-Hall recombination and band-to-band tunneling recombination are included. In the chapter 3, the variation of *I-V* characteristics under different UV illumination exposure are for the first time measured and calibrated. The UV illumination induced electrical and physical characteristic variations are studied. Finally we draw conclusions in the chapter 4.

## **Chapter 2**

## **Fabrication and Simulation**

I n this chapter, we introduce the fabrication, consisting of properties of some layers in a-Si:H TFT and process flow, simulation models and numerical methods. Physical models contain the two-dimensional thermodynamic model, the mobility model, the trap model, and the recombination model. Numerical methods include the Gummel's decoupling, adaptive finite volume, and newton's iterative methods.

### **2.1 Fabrication**

In this section, we discuss some properties of a-Si:H,  $\sin x_x$ , and n<sup>+</sup>- a-Si:H layers. For undoped a-Si:H, the deposition temperature is about 220-350°C, while for  $\text{SiN}_x$  is about

300-350◦C. In addition to temperature, RF power and gas dilution also influence the performance of a-Si TFT. Besides, the best material for the TFTs is a N-rich  $\sin x$ . The n<sup>+</sup>a-Si:H layers formation are used to allow the formation of an ohmic contact.

#### **2.1.1** Characteristics of a-Si:H,  $\text{SiN}_x$ , and  $n^+$ - a-Si:H layers

The TFT performance depends on the preparation conditions, such as substrate temperature, RF power, and gas dilution. Typically, undoped a-Si:H for TFT application is prepared at a substrate temperature of 220-350◦C. Films of a-Si:H deposited by PECVD at lower RF power have better step coverage and low defect density, whereas a-Si:H films deposited at higher RF power have poor step coverage and high defect density. Moreover, increasing the RF power decreases the surface diffusion length of precursor radicals and increases the sticking coefficient to the substrate. Hydrogenated amorphous silicon has short-range order, which means that the coordination Si within 2 or 3 atomic distances, but there is no periodicity in the long range. Because of this there are a considerable number of localized states in the gap. The hydrogen in the a-Si:H reduces the dangling bonds by passivation. Therefore, the dangling bond density of  $10^{20}$  cm<sup>-3</sup> in vacuum-evaporated a-Si or sputtered a-Si is reduced to  $10^{15} \sim 10^{16}$  cm<sup>-3</sup> in PECVD a-Si:H, where hydrogen content is 10-30 at  $\frac{8}{10}$ . The hydrogen reduces the tail-state density in addition to the reduction of of dangling bonds, because the disorder is decreased by hydrogen incorporation. The

hydrogen in a-Si:H may be incorporated as  $SiH$  or  $SiH<sub>2</sub>$ ; however, only films with hydrogen bonded as Si-H are suitable for TFT application [39]. The role of hydrogen during the deposition in the PECVD chamber can be summarized as follows: Hydrogen atoms cover the growing surface and increase the diffusion length of the Si precursors, and the precursor for a-Si:H depositions is  $SiH<sub>3</sub>$  [40]. Therefore, the precursors can migrate to a more stable position [41]. Atomic hydrogen diffuses into the silicon network down to a few nanometers and thus enhances the relaxation of Si atoms, leading to the more stable structure [42]. Atomic hydrogen etches the weak Si-Si bonds and thus more stable Si-Si bonds are formed [43]. Moreover, the hydrogen content decreases with increasing substrate temperature because of the enhanced out-diffusion of hydrogen from the film. Therefore, the optical band gap deceases when increasing the substrate temperature, since the optical band gap increases with hydrogen content in the a-Si:H [18].

Plasma-deposited silicon nitride,  $\sin x$  is used for the passivation film, silicon nitride protects against the diffusion of water vapor, sodium, and oxygen into the active device. Silicon nitride has an amorphous structure, and properties depending on the relative atomic concentrations of silicon, nitrogen, and hydrogen. For good-electrical-quality a-Si:H TFTs, PECVD-deposited  $\sin x$  is much more suitable than stoichiometric  $\sin x_4$ . Silicon nitride deposited at 300-350°C (abbreviated as  $\text{SiN}_x$  or  $\text{SiN:H}$ ) is quite different material from  $Si<sub>3</sub>N<sub>4</sub>$  produced by CVD at 700-900 $^{\circ}$ C [44]. Hydrogen in saturates the traps, so the defect

is much less than that of a CVD  $Si<sub>3</sub>N<sub>4</sub>$ . The interface charge density between a-Si:H and SiN<sub>x</sub> is typically in the range of 2x10<sup>11</sup> to 7x10<sup>12</sup> eV<sup>-1</sup>cm<sup>-2</sup>, and it strongly depends on the deposition conditions: it increases with decreasing substrate temperature or decreasing RF power. Note that the trap density in  $\text{SiN}_x$  increases on heating above 400°C, because the hydrogen is out-diffused as a result of breaking of hydrogen bonds in Si-H and /or N-H modes. The ability to form a good insulating film at low temperature (less than 350◦C) having a low interface state density with a-Si:H ( $\sim$ 10<sup>11</sup> eV<sup>-1</sup>cm<sup>-2</sup> makes a good insulator., and the best material for the TFTs is a N-rich  $\sin x$  [45]. The interface between  $\sin x$ and a-Si:H affects the field-effect mobility; in particular, the surface roughness of the  $\text{SiN}_x$ layer is important because it affects the initial growth of a-Si:H, which forms the active channel layer for the TFT [46].

Deposition of an  $n^+$ - a-Si:H layer between undoped a-Si:H and a metal allows the formation of an ohmic contact between them. The ohmic contact also acts to depress the position of the metal. For typical AMLCD TFT channel lengths ( $\sim$ 10  $\mu$ m) and for thickness of a-Si:H below ~100 nm, the used of n<sup>+</sup> poly-Si or n<sup>+</sup> a-Si contact layers dose not appreciably increase the drain current over that of standard  $n^+$  a-Si:H contact.

#### **2.1.2 Process Flow**

A back-channel-etched (BCE) , inverted-staggered a-Si:H TFTs fabricated on glass substrate was used for electrical measurement. First, the gate electrode of 350 nm thick Mo/AlNd (GE) alloy was deposited by physical vapor deposition method on the glass substrate and was patterned. Thereafter, the 330 nm thick silicon-nitride  $(SiN_x)$ , 110 nm thick undoped a-Si:H layer, 90 nm thick  $n^+$  a-Si:H were successively deposited by chemical vapor deposition method and the a-Si:H layers were patterned. The silicon-nitride layer is served as the gate insulator. The undoped a-Si:H layer is served as the active layer. The  $n^+$ a-Si:H layer is used to form the ohmic contacts at source/drain junction on the top side. The 200 nm thick Mo source/drain electrodes were also deposited by physical vapor deposition method and were patterned. The  $n^+$  a-Si:H layer in the TFT channel region was etched off by dry etching method and was overetched until the undoped a-Si:H layer to avoid the short between source and drain because of high conductivity of  $n^+$  a-Si:H layer. The back channel passivation layer  $(Si_3N_4)$  of 200 nm thick was deposited by chemical vapor deposition method and was patterned. Finally, the contact hole was defined and was deposited with 50 nm ITO layer by physical vapor deposition method, as a pixel electrode (connected with source or drain). All the process is depicted in the figure 2.4. The SEM picture of fabricated sample is shown in the figure 2.2. The device is with 18  $\mu$ m channel width, 5  $\mu$ m channel length, and 100 nm channel thickness. The electron affinity of the undoped a-Si:H layer ranges from 3.40 to 4.05 eV and the thickness of nitride is 330  $\mu$ m with 6.7 dielectric constant and 5.2 eV bandgap. The source/drain contacts on the side walls of the a-Si:H layer are the schottky contacts because the workfunction of Mo is higher than the electron affinity of the undoped a-Si:H layer. The back-channel-etched (BCE), inverted-staggered a-Si:H TFTs are used as a switch to control the pixel in AMLCD.





Figure 2.1: Process of inverted amorphous thin-film transistor



Figure 2.2: The SEM image.
## **2.2 Device Models**

In this section, models including thermodynamic, mobility, recombination, and trap models are discussed. The thermodynamic model is consist of four PDEs. The mobility model contains lattice scattering, ionized impurity scattering, and velocity saturation. The recombination model contains both trap-assisted tunneling (by adjustment of lifetime in SRH recombination) and band-to-band tunneling (occurring at high electric fields). The trap model is implemented by accept-like and donor-like states in a-Si:H layers.

### **2.2.1 Thermodynamic Model**

In this section, we state a 2D steady state mathematical model of TD equations. It is known that classical DD equations consist of three coupled PDEs, the Poisson's equation, the current continuity equation of electron, and the current continuity equation of hole [47,48].

$$
\nabla \varepsilon \cdot \nabla \psi = -q(p - n + N_{D^+} - N_{A^-}),\tag{2.1}
$$

$$
\nabla \cdot \overrightarrow{J_n} = qR + q\frac{\partial n}{\partial t},\tag{2.2}
$$

$$
-\nabla \cdot \overrightarrow{J}_p = qR + q\frac{\partial p}{\partial t},\qquad(2.3)
$$

where  $\psi$  is the electrostatic potential,  $\varepsilon$  is the silicon permittivity, *q* is the elementary charge, *n* and *p* are the electron and hole densities respectively,  $N_D$ <sup>+</sup> and  $N_A$ <sup>-</sup> are the number of ionized donors and acceptors respectively,  $J_n$  and  $J_p$  are the electron and hole current densities respectively, and *R* is the net electron -hole recombination rate. Both the equations  $(2.4)$ ,  $(2.2)$ , and  $(2.3)$  come from the Maxwell's equations.

$$
\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t},\tag{2.4}
$$

$$
\nabla \cdot \overrightarrow{D} = \rho,\tag{2.5}
$$

$$
\nabla \times \overrightarrow{H} = -\overrightarrow{J} + \frac{\partial \overrightarrow{D}}{\partial t},
$$
\n(2.6)

$$
\nabla \cdot \overrightarrow{B} = 0,\t\t(2.7)
$$

where *E* and *H* are the electric and magnetic fields respectively, *D* and *B* are the electric and . JAMARA . magnetic flux densities respectively, and  $\rho$  and  $J$  are the electric charge and total conduction current density respectively. It can be proved that the equation (2.4) comes from the equations (2.4), (2.5) and (2.7), while the equations (2.2) and (2.3) come from the equations (2.5), (2.6) [49]. Moreover, the electron and hole current densities  $J_n$  and  $J_p$  are

$$
J_n = -nq\mu_n \nabla \phi_n,\tag{2.8}
$$

$$
J_p = -pq\mu_p \nabla \phi_p,\tag{2.9}
$$

where  $\mu_n$  and  $\mu_p$  are the electron and hole mobilities, and  $\varphi_n$  and  $\varphi_p$  are the electron and hole quasi-Fermi potentials respectively. It can be proved that both  $J_n$  and  $J_p$  consist of carrier diffusion and drift phenomena in semiconductor transport, by Boltzmann Transport Equation on momentum conservation part, and the part to express carrier drift is  $\mu$  while

#### 2.2. DEVICE MODELS 27

the other is  $D$  (defined as diffusion coefficient) [49].

The TD [50] model is defined by the basic set of partial differential equations (2.4),  $(2.2)$ , and  $(2.3)$ , and the lattice heat flow equation  $(2.10)$ . The relations  $(2.8)$  and  $(2.9)$  are generalized to include the temperature gradient as a driving term:

$$
c\frac{\partial T}{\partial t} - \nabla \cdot k \nabla \cdot T = -\nabla \cdot \left[ (P_n T + \phi_n) J_n + (P_p T + \phi_p) J_p \right]
$$

$$
-(E_C + \frac{3}{2} k_B T) \nabla \cdot J_p + (E_V - \frac{3}{2} k_B T) \nabla \cdot J_p + qR(E_C - E_V + 3k_B T), \qquad (2.10)
$$

$$
J_n = -n q \mu_n (\nabla \phi_n + P_n \nabla T), \qquad (2.11)
$$

$$
J_p = -pq\mu_p(\nabla\phi_p + P_P\nabla T),\tag{2.12}
$$

where *k* is the thermal conductivity, *c* is the lattice heat capacity,  $P_n$  and  $P_p$  are the absolute thermoelectric powers [51], and  $E_C$  and  $E_V$  are the conduction and valence band energies, respectively. In this paper, we use TD model as a fundamental solution to the device simu $n_{\rm H\,III}$ lation.

As we know, only PDEs can not be solved to derive the exact solution, there must be some boundary conditions. There are two main types of boundary conditions, i.e. Dirichlet and Neumann types. Either Dirichlet or Neumann boundary condition on the bounding surface can be obtained by means of Green's theorem and so-called Green functions [52]. Ohmic contacts are usually described by Dirichlet boundary conditions where potential and carrier concentrations are pre-defined at the contact. Schottky contacts may be modeled using Dirichlet conditions which approximate the reverse bias condition or Neumann

boundary conditions based on thermionic emission theory. The absence of current flow through surfaces may be modeled by assuming that the potential and carrier gradients normal to the surface are zero, which means that the type is Neumann boundary condition [49]. Hence, in the device structure, source/drain (on the top) and gate contacts are fit the type of Dirichlet boundary conditions. The source/drain on the side wall is either Dirichlet or Neumann boundary condition depending on the bias conditions. The others are fit the type of Neumann boundary condition. For the interface of nitride and a-Si:H, there are no normal components of electron and hole current, so this is Neumann boundary condition.

According to the PDEs and the boundary conditions, this problem can be solved per-

fectly.



#### **2.2.2 Mobility Models**

In the following sections, we introduce some models used in thermodynamic model, e.g. mobility, recombination, traps model, and so on.

When it comes to the mobility, there are several concepts. First, there are two primary mechanisms affecting the carrier transport ability, i.e. lattice scattering and ionized impurity scattering [53]. Because Si atoms in a semiconductor crystal have a certain amount of thermal energy at temperature above absolute zero that causes the atoms to randomly

vibrate about their lattice position within the crystal, this phenomenon results in an interaction between the electrons or holes and the vibrating lattice atoms. This is so-called the lattice scattering (or phonon scattering), which is dominated in light doped semiconductors. On the other hand, when in heavily doped semiconductors, there may be some coulomb interactions between electrons or holes and the ionized impurities, as is the ionized impurity scattering. Moreover, with the higher field in semiconductors, the carrier drift is no longer proportioned to the electric field strength, instead, the velocity saturates to a finite value  $v_{sat}$  [53]. Finally, in the channel region, the high transverse electric field forces carriers to interact strongly with the semiconductor-insulator interface, meaning the surface scattering [53].

In this work, we employed the following models to describe the mobility.

$$
\mu_{dop} = \mu_{min1} \exp(-\frac{P_c}{N_i}) + \frac{\mu_{const} - \mu_{min2}}{1 + (N_i/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s/N_i)^{\beta}},
$$
(2.13)

where the equation (2.13) describes the doping-dependent mobility degradation proposed by Masetti et al. [54]. Moreover,  $N_i = N_A + N_D$  denotes the total concentration of ionized impurities, the reference mobilities  $\mu_{min1}$ ,  $\mu_{min2}$ , and  $\mu_1$ , the reference doping concentration  $P_c$ ,  $C_r$ , and  $C_s$ , and the exponents  $\alpha$  and  $\beta$  are accessible in the table 2.1, and the lowdoping reference mobility  $\mu_{const}$  is 1417 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> for electrons and 470.5 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> for holes.

$$
\mu_{ac} = \frac{B}{F_{\perp}} + \frac{C(N_i/N_0)^{\lambda}}{F_{\perp}^{1/3}(T/T_0)^k},
$$
\n(2.14)

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$$
\mu_{sr} = \left[\frac{(F_{\perp}/F_{ref})^{A^*}}{\delta} + \frac{F_{\perp}^3}{\eta}\right]^{-1},\tag{2.15}
$$

$$
A^* = A + \frac{\alpha_\perp (n+p) N_{ref}^\nu}{(N_i + N_1)^\nu},\tag{2.16}
$$

$$
\frac{1}{\mu_{low}} = \frac{1}{\mu_{dop}} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}},
$$
\n(2.17)

$$
D = \exp(-x/l_{crit}),\tag{2.18}
$$

where the equations (2.14), (2.15), and (2.16) describe the mobility degradation at interface proposed by Lombardi et al. [55] and Darwish et al. [56], equations (2.17) and (2.18) describe the Mathiessen's rule to include both the doping-dependent mobility degradation and the mobility degradation at interface. The surface scattering includes both acoustic surface phonons ( $\mu_{ac}$ ) and surface roughness ( $\mu_{sr}$ ). Moreover, *T* is the lattice temperature,  $T_0 = 300$  K, the reference field  $F_{ref} = 1$  Vcm<sup>-1</sup>,  $F_{\perp}$  is the transverse electric field normal to the semiconductor-insulator interface,  $D(x)$  is the distance from the interface and  $l_{crit}$  a fit parameter) is a damping that switches off the inversion layer terms far away from the interface, *n* and *p* denote the electron and hole concentrations, respectively, and  $N_{ref} = 1$ cm<sup>−</sup><sup>3</sup> . All the other parameters are in the table 2.2.

$$
\mu(F) = \frac{\mu_{low}}{[1 + (\frac{\mu_{low}F}{v_{sat}})^{\beta}]},
$$
\n(2.19)

$$
\beta = \beta_0 \left(\frac{T}{T_0}\right)^{\beta_{exp}},\tag{2.20}
$$

$$
v_{sat} = v_{sat,0} \left(\frac{T_0}{T}\right)^{v_{sat,exp}},\tag{2.21}
$$

where the equation  $(2.19)$ ,  $(2.20)$ , and  $(2.21)$  describe the high field saturation of mobility proposed by Canali et al. [57]. All the parameters are in the tables 2.3 and 2.4.

#### **2.2.3 Recombination Models**

The recombination model consisting of Shockley-Read-Hall recombination and band-toband tunneling recombination is included in continuity and lattice heat flow equations, i.e. the equations (2.2), (2.3), and (2.10) to describe the characteristic of schottky contact with negative gate bias.

Trap-assisted tunneling [58] (also known as defect-assisted tunneling or field-enhanced recombination) results in a reduction of SRH recombination lifetimes in regions of strong electric fields. It must not be neglected if the electric field exceeds a value of approximately 3x10<sup>5</sup> Vcm<sup>−</sup><sup>1</sup> in certain regions of the device. For example, the *I-V* characteristics of reverse biased pn-junctions are extremely sensitive to defect-assisted tunneling, which causes electron-hole pair generation before band-to-band tunneling or avalanche generation sets in. Therefore, it is recommended that this model is included in the simulation of drain reverse leakage and substrate currents in MOS transistors. The parameter  $g_p(F)$  is derived by replacing  $m_{\Theta,e}$  with  $m_{\Theta,h}$  and  $E_t$  with  $E_g$  *- E<sub>t</sub>*. The upper sign in the equation (2.30) represents the condition of electrons, while the lower one in the equation (2.30) represents condition of holes.

$$
R_{Et}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)},
$$
\n(2.22)

$$
\tau_p = \frac{\tau_{max,p}}{\left[1 + g_p(F)\right]},\tag{2.23}
$$

$$
\tau_n = \frac{\tau_{max,n}}{[1 + g_n(F)]},\tag{2.24}
$$

$$
g_n(F) = \left[1 + \frac{(\hbar \Theta)^{3/2} \sqrt{E_t - E_0}}{E_0 \hbar \omega_0}\right]^{-1/2}
$$

$$
\times \frac{(\hbar \Theta)^{3/4} (E_t - E_0)^{1/4}}{2\sqrt{E_t E_0}} (\frac{\hbar \Theta}{k_B T})^{3/2} A(E_t, E_0, T, \varepsilon_R, \omega_0, \Theta), \tag{2.25}
$$

$$
E_0 = 2\sqrt{\varepsilon_F} \left[ \sqrt{\varepsilon_F + E_t + \varepsilon_R} - \sqrt{\varepsilon_F} \right] - \varepsilon_R,
$$
\n(2.26)

$$
\varepsilon_F = \frac{2\varepsilon_R k_B T}{\hbar \Theta},\tag{2.27}
$$

$$
\varepsilon_R = S\hbar\omega_0 = \sqrt{3.28}
$$

$$
\Theta = \left(\frac{e^2 F^2}{2\hbar m_{\Theta,e}}\right)^{1/3},\tag{2.29}
$$

$$
E_t = \frac{1}{2} E_{g,eff} \pm \frac{3}{4} k_B T \ln(\frac{m_c}{m_v}) \mp E_{trap} - (32 R_{C,V} \hbar^3 \Theta^3)^{1/4}, \tag{2.30}
$$

$$
R_C = m_c(\frac{Z^2}{\varepsilon^2})R_y,
$$
\n(2.31)

where  $E_0$  is the energy of an optimum horizontal transition path,  $\varepsilon_R$  is the lattice relaxation energy, *S* is the Huang-Rhys factor,  $\hbar\omega_0$  is the effective phonon energy,  $E_t$  is the energy level of the recombination center,  $\Theta$  is the electro-optical frequency,  $m_{\Theta,e}$  is the electron tunneling mass in the field direction,  $R_C$  and  $R_V$  are the effective Rydberg constants for electrons and holes respectively,  $R_Y$  is the Rydberg energy,  $\varepsilon$  is the relative dielectric constant, and *Z* is a fit parameter.

Phonon-assisted band-to-band tunneling [59] cannot be neglected in steep pn-junctions (with a doping level of  $1x10^{19}$  cm<sup>-3</sup> or more on both sides) or in high normal electric fields of MOS structures. It must be switched on if the field, in some regions of the device, exceeds (approximately)  $8x10^5$  Vcm<sup>-1</sup>. The upper sign in the equations (2.32) and (2.34) refers to tunneling generation ( $np < n^2_{i,eff}$ ) and the lower sign refers to recombination  $(np > n^2_{i,eff}).$ 

$$
R_{net}^{bb} = AF^{7/2} \frac{\widetilde{n}\widetilde{p} - n_{i,eff}^2}{(\widetilde{n} + n_{i,eff})(\widetilde{p} + n_{i,eff})} B(F_C, F, \omega, T),
$$
\n(2.32)

$$
\widetilde{n} = n \left( \frac{n_{i,eff}}{N_C} \right)^{\frac{\nabla E_{F_n}}{F}},
$$
\n(2.33)

$$
F_c^{\pm} = B(E_{g,eff} \pm \hbar \omega)^{3/2},
$$
\n(2.34)

where  $\hbar\omega$  denotes the energy of transverse acoustic phonon.

#### **2.2.4 Trap Models**

To include the influence of charge distribution in device characteristics, we have to couple the influence of trap states into our device simulators mentioned above. The influence of trap state is feed in the right hand side of Poisson equation, as shown in below, to study the

effects of trap states in a-Si:H layer.

$$
\nabla^2 \phi = -\frac{q}{\varepsilon} [p - n + N_D - N_A + \sum (N_{Dt} - n_{Dt}) - \sum (N_{At} - p_{At}) + \sum p_t - \sum n_t], \tag{2.35}
$$

$$
n_{Dt} = N_{Dt}f_n, n_t = N_{Et}f_n, p_{At} = N_{At}f_p, p_t = N_{Ht}f_p,
$$
\n(2.36)

$$
f_n = \frac{v_{th}^n \sigma_n n + v_{th}^p \sigma_p p_1}{v_{th}^n \sigma_n (n + n_1) + v_{th}^p \sigma_p (p + p_1)},
$$
\n(2.37)

$$
f_p = 1 - f_n,\t\t(2.38)
$$

$$
v_{th}^{n,p} = v_0^{n,p} \sqrt{\frac{T}{T_0}},
$$
\n(2.39)

$$
n_1 = n_{i,eff} \exp(E_{trap}/k_B T), \qquad (2.40)
$$

$$
p_1 = n_{i,eff} \exp(-\frac{E_{trap}}{k_B T}),
$$
\n(2.41)

where  $\phi$  is the electrostatic potential, *q* is the elementary charge,  $\varepsilon$  is the semiconductor permittivity,  $E_t$  represents the energy levels of trap,  $p$  is the hole density,  $n$  is electron density,  $N_D$  is the donor doping concentration,  $N_A$  is the acceptor doping concentration,  $N_{Dt}$  is the donor trap concentration,  $N_{At}$  is the acceptor trap concentration,  $n_{Dt}$  is the electron concentration of the donor trap level,  $p_{At}$  is the hole concentration of the acceptor trap level,  $p_t$ is the hole concentration of the neutral hole trap level,  $n_t$  is the electron concentration of the neutral electron trap level,  $N_{Et}$  is the neutral electron trap concentration,  $N_{Ht}$  is the neutral hole trap concentration,  $f_n$  is the occupation probability for electrons,  $f_p$  is the occupation probability for holes,  $v^n_{th}$  is the electron thermal velocity,  $v^p_{th}$  is the hole thermal velocity,  $\sigma_n$  is the electron capture cross section,  $\sigma_p$  is the hole capture cross section,  $n_{i,eff}$  is the

effective intrinsic carrier concentration, and  $E_{trap}$  is the difference between the defect level and intrinsic level. The trap models used in this study is irrespective of acceptor and donor types.

$$
\sum (N_{At} - p_{At}), \qquad (2.42)
$$

$$
\sum (N_{Dt} - n_{Dt}),\tag{2.43}
$$

According the previous study [31–33], the localized states in a-Si:H mobility gap can be modeled by the exponential distributions of deep and tail states for both acceptor-like and *<u>ALLELIAN AND ALLELY AND ARTISTS , and a series , and a*</u> donor-like states:

$$
N_{Et} = g_{tc} \exp(\frac{E - E_C}{E_{tc}}) + g_{dc} \exp(\frac{E - E_C}{E_{dc}}),
$$
\n(2.44)

$$
N_{Ht} = g_{tv} \exp(\frac{E_V - E}{E_{tv}}) + g_{dv} \exp(\frac{E_V - E}{E_{dv}}),
$$
\n(2.45)

where  $E_C$  is the conduction band edge,  $g_{tc}$  and  $g_{dc}$  are the densities of states at the conduction band edge for the tail and deep acceptor-like states, respectively.  $E_{tc}$  and  $E_{dc}$  are the associated slope of the exponential distribution of the tail and deep acceptor-like states.  $E_V$ is the valence band edge,  $g_{tc}$  and  $g_{dc}$  are the densities of states at the valence band edge for the tail and deep donor-like states.  $E_{tv}$  and  $E_{dv}$  are the associated slope of the exponential distribution of the tail and deep donor-like states, respectively, and *E* is the energy in the a-Si:H mobility band gap.

## **2.3 Simulation Method**

In this section, the simulation methods include the Gummel's decoupling method, the adaptive finite volume method, and the newton's iterative method. For the purpose of timeconsuming, we use the TCAD device simulator to realize the simulation of a-Si TFTs under different magnitude of UV illumination.

#### **2.3.1 The Gummel's Decoupling Method**

The Gummel's decoupling method controls an iterative loop over two or more coupled equations. It is used when a fully coupled method would use too many resources of a given machine, or when the problem is not yet solved and a full coupling of the equations would diverge. 1111111111

To explore the transport behavior of a-Si TFTs, the three coupled PDEs are numerically solved with Gummel's decoupling method. With a given initial guess  $(\phi^{(0)}, n^{(0)}, p^{(0)})$ and for each Gummel's iteration index  $q, q = 0,1,...$ , we first solve the nonlinear Poisson equation

$$
\Delta \phi^{(g+1)} = \frac{q}{\varepsilon_s} (n^{(g)} - p^{(g)} + D(x, y) + \sum n_t - \sum p_t).
$$
 (2.46)

The nonlinear Poisson equation is solved for  $\phi^{(g+1)}$  given the previous states  $n^{(g)}$  and  $p^{(g)}$ . The current continuity equation of electron is then solved for  $n^{(g+1)}$ , with now the known

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functions  $\phi^{(g+1)}$  ,  $p^{(g)}$  , and  $T^{(g)}$ 

$$
\frac{1}{q}\nabla \cdot (-q\mu_n n^{(g+1)}\nabla \phi^{(g+1)} + qD_n^{(g+1)}\nabla_n^{(g+1)} + P_n\nabla T^{(g)}) = R(n^{(g+1)}, p^{(g)}). \tag{2.47}
$$

Thereafter, we solve the current continuity equation of hole with  $\phi^{(g+1)}$ ,  $n^{(g+1)}$ , and  $T^{(g)}$ known

$$
\frac{1}{q}\nabla \cdot (-q\mu_p p^{(g+1)}\nabla \phi^{(g+1)} + qD_p^{(g+1)}\nabla_p^{(g+1)} + P_p\nabla T^{(g)}) = -R(n^{(g+1)}, p^{(g+1)}), \quad (2.48)
$$

Finally, we solve the heat flow equation with  $\phi^{(g+1)}$ ,  $n^{(g+1)}$ , and  $p^{(g+1)}$ .

$$
c\frac{\partial T^{(g+1)}}{\partial t} - \nabla \cdot k \nabla \cdot T^{(g+1)} = \nabla \cdot \left[ (P_n T^{(g+1)} + \phi_n^{(g+1)}) J_n + (P_p T^{(g+1)} + \phi_p^{(g+1)}) J_p \right]
$$

$$
-(E_C + \frac{3}{2} k_B T^{(g+1)}) \nabla \cdot J_p + (E_V - \frac{3}{2} k_B T^{(g+1)}) \nabla \cdot J_p + qR(E_C - E_V + 3k_B T^{(g+1)}) Q.49)
$$

$$
J_n = -q\mu_n n^{(g+1)} \nabla \phi_n^{(g+1)} + qD_n^{(g+1)} \nabla_n^{(g+1)} + P_n \nabla T^{(g+1)}, \tag{2.50}
$$

$$
J_p = -q\mu_p p^{(g+1)} \nabla \phi^{(g+1)} + q D_p^{(g+1)} \nabla_p^{(g+1)} + P_p \nabla T^{(g+1)},\tag{2.51}
$$

for  $T^{(g+1)}$  until all preset stopping criteria are satisfied. The equations (2.46), (2.47), (2.48), and (2.49) are associated with proper boundary condition, respectively. We note that the equations (2.46), (2.47), (2.48), and (2.49) are now four individual semilinear PDEs to be solved for each Gummel's iteration. An outer iteration in the procedure of a-Si TFT simulation is then defined by Gummel's decoupling method.

The Gummel's decoupling method

Begin

While  $\phi$ , *n*, *p*, and *T* in outer loop (Gummel's loop) are not convergent

If  $\phi$  is convergent

Solve the nonlinear Poisson equation

with adaptive computing technique.

End If

If  $n$  is convergent

Solve the current continuity equation of electron

with adaptive computing technique.

End If

If  $p$  is convergent

Solve the current continuity equation of hole

with adaptive computing technique.

End If

If  $T$  is convergent

Solve the heat flow equation

with adaptive computing technique.

End If

End While

Call for next calculation.

End The Gummel's decoupling algorithm

A computational procedure for Gummel's decoupling method is shown above, and the flow char is shown in the figure 2.3. We solve each decoupled PDE with adaptive computing technique.

#### **2.3.2 The Adaptive Finite Volume Method**

Based on adaptive 1-irregular mesh and finite volume (FV) approximation. The finite volume method is a numerical method for solving partial differential equations. It calculates the values of the conserved variables across the volume. Before using adaptive  $u_{\rm min}$ finite volume method to solve Poisson equation, we must understand the follow steps:

- (1) Weak Formulation transforms into weak problem;
- (2) Discretize the simulation area by one-irregular mesh;
- (3) Form the equation  $A x = B''$  by using FV method; and
- (4) Error estimation and mesh refinement.

The example of FVM with Poisson equation is shown in the figure 2.4.

$$
\int \int \nabla \cdot \nabla \phi dy dx = \int \int \left[ \frac{qn_i}{\varepsilon_{Si}} (ucxp(\frac{\phi}{V_T}) - vexp(\frac{-\phi}{V_T})) - \frac{qD}{\varepsilon_{Si}} \right],\tag{2.52}
$$

$$
\left(\frac{\phi_{i+1,j} - \phi_{i,j}}{h_i}\right)\left(\frac{k_{j-1} + k_j}{2}\right) + \left(\frac{\phi_{i,j-1} - \phi_{i,j}}{k_j}\right)\left(\frac{h_{j-1} + h_j}{2}\right)
$$

$$
+\left(\frac{\phi_{i-1,j} - \phi_{i,j}}{h_{i-1}}\right)\left(\frac{k_{j-1} + k_j}{2}\right) + \left(\frac{\phi_{i,j-1} - \phi_{i,j}}{k_{j-1}}\right)\left(\frac{h_{j-1} + h_j}{2}\right)
$$

$$
= \left[\frac{qn_i}{\varepsilon_{Si}}\left(u_{i,j}exp\left(\frac{\phi_{i,j}}{V_T}\right) - v_{i,j}exp\left(\frac{-\phi_{i,j}}{V_T}\right)\right) - \frac{qD_{i,j}}{\varepsilon_{Si}}\left[\left(\frac{k_{j-1} + k_j}{2}\right)\left(\frac{h_{j-1} + h_j}{2}\right),\right] \quad (2.53)
$$

The flow char of FVM is shown in the figure 2.5. The discretized step divides into structured mesh and unstructured mesh. If according to geometry, it divides into rectangle mesh and triangle mesh. But the rectangle mesh is easier to build than the triangle mesh.

## **2.3.3 The Newton's Iterative Method**

The starting solution of initial guess is determined by using a predetermined algorithm. An initial guess of each variable (at each mesh point) in a device required by the solution method including electrostatic potential and quasi-Fermi potentials for electrons and holes. To determine an initial guess for the electrostatic potential and quasi-Fermi potentials, the device is subdivided into wells of n- and p-type doping, such that pn-junctions serve as dividers between wells. Every well is uniquely associated with a contact. The quasi-Fermi potentials in that well are set to the corresponding contact voltage, and the potentials are set to the contact voltage adjusted by the built-in voltage at the contact. For wells that have no contacts, the following equations define the quasi-Fermi potential for the majority carriers:

$$
\phi_p = k_{Float} V_{max} + (1 - k_{Float}) V_{min},\tag{2.54}
$$

#### 2.3. SIMULATION METHOD 41

$$
\phi_n = (1 - k_{Float})V_{max} + k_{Float}V_{min},\tag{2.55}
$$

where  $k_{Float}$  is equal to 0. For wells with more than one contact, the well is further subdivided, such that no well is associated with more than one contact.

Newton's method uses the first and second derivatives when the initial point is closed to the solution. In this sections,first, we will show the full coupled solution. This scheme tries to solve the nonlinear system  $g(z) = 0$  by the Newton method:

$$
\overrightarrow{g} + \overrightarrow{g}' \overrightarrow{x} = 0, \qquad (2.56)
$$

$$
\overrightarrow{z}^{j} - \overrightarrow{z}^{j+1} = \lambda \overrightarrow{x}, \qquad (2.57)
$$

where  $\lambda$  is selected such that  $||g_{k+1}|| < ||g_k||$ , but is as close as possible to 1. It handles the error by computing an error function that can be defined by two methods.The Newton iterations stop if the convergence criteria are fulfilled. One convergence criterion is the norm of the right-hand side, that is,  $||g||$  in the equation 2.51. Natural criterion may be the relative error of the variables measured, such as  $\left\|\frac{(\lambda x)}{x}\right\|$  $rac{(x)}{z}$ ||.



Figure 2.3: A flow chart of the Gummel's decoupling algorithm.



Figure 2.4: The example of FVM with example of Poisson equation.



Figure 2.5: The flow char of FVM.







Table 2.2: Lombardi model: Default coefficients for silicon. Ę ģ

Ω





Table 2.3: Canali model parameters (default values for silicon).



Table 2.4: Default velocity saturation parameters (for silicon).



## **Chapter 3**

# **Characterization and Simulation**

n this chapter, we discuss the effect of backlight, activation energy, and simulation I results. Activation energy is used to find the position of the Fermi level. The simulation results include calibration of  $I_D$ - $V_G$  curve with different magnitude of shot.  $u_{\text{trans}}$ 

## **3.1 Effects of Backlight Illumination**

An important application for hydrogenated amorphous silicon thin-film transistors is in switching elements for active-matrix liquid crystal displays. Particularly, a-Si:H TFT is advantageous to the production of large screen displays and facilitates mass-production. When employing a-Si:H layer, one of the main issues is to improve the production throughput and to reduce the off-state leakage currents under light illumination. In order to reduce the parasitic capacitance between the gate and source/drain electrodes, a self-aligned a-Si:H TFT structure has been proposed. However, the higher off-state leakage current under light illumination compared to a conventional TFT has been observed [60]. TFT off-current increases by photoillumination, where a-Si decreases the charge stored on the pixel during the TFT off-time, and results in gray-scale shading, flicker, crosstalk and other display nonuniformity in the LCD. Because the voltage across the capacitor of liquid crystal has relationship with the transmittance and the transmittance has relationship with the gray level, the off-current during holding after finishing charging has an influence on the gray level. The off-state leakage current of a-Si:H TFT is mainly due to holes induced at the a-Si:H interfaced to a gate insulator. However, under light illumination, electrons are the majority carriers when a negative gate voltage is applied to the TFT because electron mobility is much higher than that of holes [61]. Much attention has been given to the TFT off-current under illumination from the gate side, because backlight illuminates the TFT from the gate side during TFT-LCD operation. In the case of the inverted a-Si TFT, which is the most widely employed structure, most of the light is shield by the gate electrode and only the source/drain regions are illuminated from the gate-side illumination [62].

There are some solutions for reducing photo leakage current. The off-state leakage current can be lowered by reducing the thickness of undoped a-Si:H, however, this also decreases the field effect mobility of the TFT [63]. This is because the transmittance for thin a-Si:H

layer is higher than that for thick a-Si:H layer, fewer electron-hole pairs generate, resulting in lower photo leakage current [64]. The off-state leakage current of a-Si:H TFT under light illumination is related with its photoconductivity. The photoconductivity of a-Si:H(:Cl) is at least two orders of magnitude lower than that of undoped a-Si:H [65]. Recently, Cl incorporated hydrogenated amorphous silicon has been prepared by various deposition methods using  $SiH<sub>2</sub>Cl<sub>2</sub>$  mixtures to improve film quality [66], stability [67] or to increase deposition rate [68]. However, the performance of the a-Si:H(:Cl) TFT was found to degrade with increasing  $[SiH_2Cl_2]/[SiH_4]$  ratio which was used to deposit the a-Si:H(:Cl) [69]. The a-Si:H(:Cl) films show p-type conduction, leading to lower photoconductivity, while the a-Si:H films show n-type conduction. The lower off-state dark leakage current of a-Si:H(:Cl) TFTs is due to the position of the Fermi level of a-Si:H(:Cl). The Fermi level of a-Si:H(:Cl) that exists is lower than that of a-Si:H. But, with increasing  $[SiH_2Cl_2]/[SiH_4]$ , the field effect mobility decreases slightly and the threshold voltage increases. The increases in the threshold voltage may be due to the increase in the defect density by incorporation and/or due to the shift of the Fermi level in the band gap towards the valence band edge. The position of the Fermi level can be lowered by a reduction of donor-like states or by an increase of acceptor-like states. Therefore, the photoconductivity of a-Si:H is strongly related to the position of the Fermi level [70]. Finally, it should be noted that the photoconductivity of p-type a-Si:H is much lower than that of n-type a-Si:H because the mobility of electrons is higher than that of holes. Because of the low photoconductivity a-Si:H(:Cl), a double amorphous silicon active layer (a-Si:H(:Cl)/ a-Si:H TFTs) is also proposed to suppress the photo leakage current, but the leakage is higher than a-Si:H(:Cl) TFTs, while the mobility is higher and the threshold voltage is lower than a-Si: $H([C])$  TFTs [71]. In addition to Cl incorporation in hydrogenated amorphous silicon, F incorporation in hydrogenated amorphous silicon was used to suppress the photo leakage current [72]. Moreover, it is explained that the increase of acceptor-like deep states in a-Si:H(:F) material leads to slight electrical degradation on a-Si:H(:F) TFTs and results in the shift down of Fermi level.

# **3.2 Activation Energy**



The activation energy measurement is a useful way to find the position of the Fermi level. By changing sample's temperature and measurement the  $V_G-I_D$  characteristics, we can work out the activation energy-gate voltage  $(E_a-V_a)$  plot to finding the position of the Fermi level. By further calculation, we can work out the density of states, which make more recombination centers for electrons and holes.

The activation energy is estimated with the following equation:

$$
I_D \cong \exp(-\frac{qE_{act}}{kT}).\tag{3.1}
$$

The active energy is strongly related to the position of the Fermi level. If the position of the Fermi level shifts toward the valence band edge, the active energy increases. The shift rate can be used for the evaluation of the density of states in the forbidden gap applying the method proposed by Globus et al [73]. The Fermi level shift with the gate voltage is strongly dependent on the density of states. At higher density of states more carriers must be induced in order to fill the states from  $E_F$  upward and it is necessary to apply higher gate voltage in order to induce more carriers in the channel. On the contrary, when the density of states is low, the states from  $E_F$  upward are easily filled at low gate voltage. This correlation between the density of states and the gate voltage allows to obtain the shape of the density of states by study the dependence of  $E_a$ - $V_G$ . The shape of density of states is related to the threshold voltage, subthreshold slope, field mobility, and the stability of TFTs. Globus et al. [73] proposed a method for evaluation of density of states from the dependence of  $E_a$ - $V_G$ . If it is assumed that the charge of acceptor-like states  $Q_t$ , filled by the gate bias is given by

$$
Q_t = q \int_{E_C - E_{Fi}}^{E_C - E_{Fi} + qV_s} g(E) dE,
$$
\n(3.2)

where *q* is the electric charge,  $V_s$  is the surface potential,  $E_{Fi}$  is the equilibrium Fermi level in the silicon layer, and  $g(E)$  is the density of states. The  $Q_t$  can also be expressed as

$$
Q_t = \frac{qn_t}{t_{scl}} = \frac{\varepsilon_{ins}}{t_{ins}t_{sd}}(V_{GS} - V_{FB}),
$$
\n(3.3)

where  $q_{nt}$  is the surface charge,  $V_{FB}$  is the flat-band voltage,  $\varepsilon_{ins}$  and  $t_{ins}$  are the gate dielectric constant and insulator thickness. From the equations (3.2) and (3.3), taking deriviative with respect to  $V_{GS}$ , we can obtain

$$
\frac{d}{dV_{GS}}\left(\frac{n_t}{t_{scl}}\right) = g(E_{act})\frac{dqV_s}{dV_{GS}} = -g(E_{act})\frac{dE_{act}}{dV_{GS}},\tag{3.4}
$$

where  $E_{act} = E_C - E_{Fi} - qV_s$  is the activation energy as the figure 3.1 shown. So we can note that

$$
\int_{E_C - E_{Fi}}^{E_C - E_{Fi} + qV_s} g(E) dE = \int_{E_C + qV_s}^{E_C + 2qV_s} g(E) dE \cong g(E_{act}) qV_s.
$$
\n(3.5)

Hence, the density of localized states can be related to the derivative of the activation energy with respect to gate bias:

$$
g(E_{act}) = -\frac{d}{dV_{GS}} \left(\frac{n_t}{t_{sel}}\right) \left(\frac{dE_{act}}{dV_{GS}}\right)^{-1}.
$$
 (3.6)

If we assume that the band bending in the a-Si layer is small compared to the characteristic energy of the density of states variation, then  $t_{sd}^{\simeq}$ <sub>a−Si</sub> where  $t_{a-Si}$  is the a-Si layer mines thickness and the equation (3.6) reduces to

$$
q(E_{act}) = -\frac{\varepsilon_{ins}}{qt_{ins}t_{a-Si}\frac{dE_{act}}{dV_{GS}}}.
$$
\n(3.7)



Figure 3.1:  $E_{act}$ - $E_C$ - $E_{Fi}$ - $qV_S$  is the activation energy.

## **3.3 UV Light Illumination Experiment**

In the UV laser illumination experiment, the TFT was measured after fabricated (0 shot), thereafter the a-Si:TFT was exposed with UV laser beam (355 nm) with particular shot and again measured. Also, the inverted staggered a-Si:H TFTs was exposed from the top side of the a-Si:H layer (i.e. the side of source/drain contacts), but not the bottom side of the a-Si:H layer (i.e. the side of gate contact), as depicted in the figure 3.2. This all includes 1 shot, 10 shots, 22 shots, 50 shots, and 101 shots. The current-voltage characteristic measurement of thin film transistor devices was performed by HP4156C with source grounded and body floating. The electrical test setup of HP4156C semiconductor parameter analyzer, as depicted in the figure 3.3 (a), a probe station situated inside a dark box. The current-voltage (*I-V*) characteristics measurements were gotten by using n-TFT structure with Agilent 4156C precision parameter analyzer. Agilent 4156C can measure the minimum leakage current: 1f (A) The UV laser illumination experiment was performed by the instrument of the figure 3.3 (b).



Figure 3.2: Schematic representation of the inverted staggered a-Si:H TFT with UV illumination from the top side.



Figure 3.3: (a) Instrument to extraction  $I_D$ - $V_G$  curve with source-drain voltage of 12 V from 0 shot to 101 shots. (b) Instrument to UV illumination with wavelength of 355 nm.

## **3.4 Electrical Characteristics**

Figure 3.5 shows the measured *I-V* characteristics of the inverted staggered a-Si:H TFTs exposed with different shots of UV laser. It is observed that there are positive shift of threshold voltage  $(V_{th})$ , reduction of off-state leakage current, and reduction of on-state current due to UV illumination in inverted staggered a-Si:H TFTs. According to the bulk model, illumination causes a metastable increase in the bulk density of states in the a-Si:H layer. The charge state and energy position of the defect states may be such that they cause the Fermi level to move away from the conduction band after illumination [7]. The changes in the dark conductance of amorphous silicon due to annealing at temperatures between 150◦C and 200◦C were observed, which were reversed by illumination with white light [5]. The cycle of annealing and illumination has two effects: to change the threshold voltage and the off conductance.

## **3.5 Simulation Results**

In this section, both the measured and simulated data are showed. The trap models are coupled in the Poisson equation when positive gate voltage applies. The recombination models are coupled in the electron/hole continuity equations and the lattice heat flow equation when when negative gate voltage applies. The transient analysis is also included in this section.

#### **3.5.1 To Include Traps in a-Si:H Layer**

The simulated  $I_D-V_G$  curves are shown in the figure 3.6, which show a good agreement with measured data. The acceptor-like states form 0 shot to 101shots are calibrated, and the threshold voltage is increased about 1.2 V from 0 shot to 101 shots. The corresponding densities of states at the conduction band edge for the tail and deep acceptor-like states are shown in the figures 3.7 and 3.8, which show a significant increase of both  $g_{tc}$  and  $g_{dc}$ at 22 shots and then saturated for more magnitude of shot. The tail states  $(g_{tc})$  are the Si conduction band states broadened and localized by the disorder to form a tail of localized states just below the conduction band mobility edge. These states are so-called the weak silicon bond [21]. The deep states originate from defects in the a-Si:H network. These are thought to mostly consist of Si dangling bonds, which have wide range of energies [21]. After UV laser illumination, the bonds in a-Si:H network is weakened, then broken. Hence, both  $g_{tc}$  and  $g_{dc}$  increase apparently. The simulation results of acceptor-like states from 0 shot to 101 shots are summarized in the table 3.1.

The figures 3.9, 3.10, 3.11, 3.12, and 3.13 show the simulated density of states (DOS)

in the a-Si:H layer after fabricated (0 shot), 1 shot, 10 shots, 22 shots, 50 shots, 80 shots, and 101 shots. It is observed that when employing nitride as gate insulator, more deep states occupy in the lower part of amorphous silicon gap. On the contrary, when employing oxide as gate insulator, more deep states occupy in the upper part of amorphous silicon gap. Moreover, it is also observed that with the number of shots, both tail states and deep states increase. It is because that the energy of UV illumination is higher than that of Si-H bond. Therefore, more recombination centers form in the band gap of a-Si:H. This may cause the reduction of leakage. The tail states are weak bonds of Si and the deep states are dangling bonds. In order to find position of the Fermi level in a-Si:H band gap, we work out the activation energy-gate voltage  $(E_a-V_a)$  plot, as depicted in the figure 3.15. It is observed that the Fermi level at zero bias shifts toward the valence band with the magnitude of shot. It is also observed that the Fermi level is shifted from 1.167 eV to 1.055 eV. The position of the intrinsic Fermi level energy is 600 meV beneath the conduction band edge [74]. Because of positive fixed charge in nitride, inducing an electron accumulation layer in the amorphous silicon, like n-type amorphous silicon, even the amorphous silicon is undoped. Therefore, the Fermi level is larger than 0.9 eV for every shot of UV illumination. The results of location of Fermi level is summarized in the table 3.2. Based on the neutral condition, there are two ways to lower the position of Fermi level for positive threshold voltage shift, i.e. by reducing donor-like states or increasing acceptor-like states. However,

the prethreshold slope is relative with the acceptor-like states [9]. Therefore, in conclusion, we increase the acceptor-like states but not reducing the donor-like states.

#### **3.5.2 To Include Generation-Recombination in a-Si:H Layer**

In addition to the turn-on characteristics of a-Si:H TFTs, the recombination models, including both trap-assisted tunneling and band-to-band tunneling mechanisms, are calibrated to study the off-state characteristics of a-Si:H TFTs. In this study, the equations (2.22) and (2.32) are used to simulate and calibrate the off-state characteristics. The figures 3.15 (a) and (b) show the generation rates of trap-assisted tunneling and band-to-band tunneling respectively of 22 shots at  $V_D = 12$  V and  $V_G = -20$  V. Because the maximum electric field occurs at the position near the junction of drain, the maximum probability of trap-assisted tunneling and band-to-band tunneling occur near the junction of drain [75]. The off-current is interpreted in terms of field-enhanced generation mechanisms, which predominately take place at the drain depletion region [76].

At room temperature, both the trap-assisted tunneling, and band-to-band tunneling contribute to the off-current. At larger temperature, the trap-assisted tunneling will play a major role. The maximum values of the trap-assisted tunneling and band-to-band tunneling generations with different UV illumination for off-current calibration are studied in the figure 3.16 (a). For devices under fewer UV illumination (less than 50 shots), the generation and
recombination mechanism is dominated by the effect of band-to-band tunneling. However, with increasing number of UV exposure, the trap density in undoped amorphous silicon film is increased significantly, as shown in the figures 3.7 and 3.8. Figure 3.16 (b) shows the relation between leakage current and trap density at 1.2 eV higher than valence band. As the numbers of exposure is increased, especially larger than 50 shots, the increment of trap density is saturated and the improvement provided by UV illumination is decreased. The relationship between leakage current and trap density is linear when the generation and recombination mechanism is dominated by trap-assisted tunneling effect. However, for the shots 22 and 50, the generation and recombination mechanism is dominated by band-to-band tunneling; therefore, the relation is nonlinear.

#### **3.5.3 Transient Analysis**

Because traps in a-Si:H layer have obvious influence on the characteristics of amorphous silicon thin-film transistors, we simulate the transient process when the traps is filled with carriers. The figure 3.17 shows the  $I_D$ - $V_G$  without carriers filling in traps. It is observed that there is no difference with the number of shots. The figure 3.18 shows the  $I<sub>D</sub>$ -time with the number of shots. It is found that the time to the steady state increases with the number of shots because of more traps in the larger number of shots.



Figure 3.4: Measured drain current versus the gate voltage for the source-drain voltage of 12 V from 0 shot to 101 shots.



Figure 3.5: Calculated and measured drain current as a function of gate voltage for the source-drain voltage of 12 V.



Figure 3.6: Simulated acceptor-liked states of  $g_{tc}$  with different numbers of UV illumination shot.



Figure 3.7: Simulated acceptor-liked states of  $g_{dc}$  with different UV illumination.



Figure 3.8: Model density of states used in a-Si:H with 0 shot.



Figure 3.9: Model density of states used in a-Si:H with 10 shots.



Figure 3.10: Model density of states used in a-Si:H with 22 shots.



Figure 3.11: Model density of states used in a-Si:H with 50 shots.



Figure 3.12: Model density of states used in a-Si:H with 101 shots.



Figure 3.13: Model density of states used in a-Si:H with 0, 22, and 101 shots, respectively.



Figure 3.14: Activation energy versus the gate voltage for the source-drain voltage of 12 V from 0 shot to 101 shots.



Figure 3.15: (a) Simulated generation rates of the trap-assisted tunneling with 22 shots at  $V_D = 12$  V and  $V_G = -20$  V. (b) Simulated generation rates of the band-to-band tunneling with 22 shots at  $V_D$ = 12 V and  $V_G$  = -20 V.



Figure 3.16: (a) Simulated maximum generation rates of the trap-assisted tunneling (TAT) and band-to-band tunneling (BBT) from 0 shot to 101 shots at  $V_D = 12$  V and  $V_G = -20$ V. (b) Relation between leakage current and trap density at 1.2 eV which is higher than valence band.



Figure 3.17: Simulated drain current as a function of gate voltage without traps filled for the source-drain voltage of 12 V.



Figure 3.18: Simulated drain current as a function of time with traps filled for the source-drain voltage of 12 V.

<b>Number of Shots</b>	0	10	22	50	<b>101</b>
$g_{tc}(10^{21}cm^{-3}eV^{-1})$	1.2	1.2	14	15	13.5
$g_{dc} (10^{16} \text{cm}^{-3} \text{eV}^{-1})$		10	2400	3900	4400
${\bf E}_{tc}$ (meV)	50	50	30	30	30
${\bf E}_{dc}$ (meV)	<b>100</b>	<b>100</b>	95	95	95
$\sigma_n$ (cm <sup>2</sup> )	$10^{-8}$	$10^{-8}$	$10^{-8}$	$10^{-9}$	$10^{-9}$
$\sigma_p$ (cm <sup>2</sup> )	$10^{-10}$ 10 <sup>-10</sup>		$10^{-10}$	$10^{-11}$	$10^{-11}$

Table 3.1: Simulated acceptor-like states including  $g_{tc}$ ,  $g_{dc}$ ,  $E_{tc}$ ,  $E_{dc}$ ,  $\sigma_n$ , and  $\sigma_p$  from 0 shot to 101 shots.



Table 3.2: Position of Fermi level from 0 shot to 101 shots.

<b>Number of Shots</b>	10	-50	101
Fermi level $E_F$ (eV)   1.167   1.149   1.081   1.065   1.055			

## **Chapter 4**

# **Conclusions**

### **4.1 Summary**



In this study, effect of UV Illumination on improving device switching characteristics has been experimentally observed and theoretically studied. The device characteristics are investigated by solving a set of Poisson, electron/hole continuity, and lattice heat flow equations, coupling with trap state models and recombination models. The *I-V* characteristics of the inverted staggered a-Si:H TFTs with different magnitude of UV light illumination is calculated and carefully calibrated with experiment measurement data. It has been found that the acceptor-like states and the electron tunneling effective mass in a-Si:H increase with UV exposure increased. The positive threshold voltage shift and reduction of off-state leakage are observed due to the movement of Fermi level away from the conduction band

to the valence band after UV illumination. The preliminary result shows the effect of traps states in the a-Si:H layer and the movement of Fermi level from the conduction band after UV illumination. Both the trap-assisted tunneling and band-to-band tunneling effects are considered and calibrated to study the influence of UV illumination on leakage current. This study provides an insight into the effect of UV illumination and the mechanism to improve the switching characteristics of amorphous silicon thin-film transistors.

#### **4.2 Suggestion for the Future Work**

Listed below, some topics are suggested for further investigation. The source/drain schottky contact induced leakage current can also be further studied in the future. Moreover, the UV illumination with different wavelength on amorphous silicon thin-film transistors can be manual further studied.

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### **VITA**

Name: Chung-Le Chen, 陳忠樂

Permanent address: No.96, Mingfong 16th St., Cianjhen City, Kaohsiung County 806,

Taiwan

Degree and date to be conferred: Master of Institute of Electrics, Feb., 2008

Date of birth: January 8<sup>st</sup>, 1980

Place of birth: Kaohsiung, Taiwan



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