國 立 交 通 大 學

電 子 工 程 學 系 電 子 研 究 所

碩 士 論 文

# 背向散射理論應用於金氧半場效電晶體在飽和區之不匹配效應之物理模型

# A Physical MOSFET Saturation Current Mismatch Model Based on Backscattering Theory

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指導教授：陳明哲　　Prof. Ming-Jer Chen

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## 摘　要

本論文研究金氧半場效電晶體在過臨界區的不匹配效應以及利用背向散射理論推導出一個物理模型。我們首先量測各種不同尺寸的電晶體，並且在飽和區計算其匹配誤差。我們發現隨著閘極電壓的增大，電流的誤差會逐漸變小。接著我們考慮背向散射理論的三個參數，背向散射係數, 臨界電壓, 以及汲極電壓導致位障下降, 組成一個以這三個參數為變數的函數來計算電流的不匹配效應。

# A MOSFET Saturation Current Mismatch Model Based on Backscattering Theory

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## Abstract

This thesis investigates the current mismatch in above-threshold regions and derives a physical mismatch model based on backscattering theory. We have extensively characterized measured MOSFETs in above-threshold regions with different gate widths and lengths to determine the current mismatch. We have observed that the current mismatch decreases with increasing gate voltage. We have also derived a backscattering based mismatch model with three key parameters, drain-induce-barrier-lowering (DIBL), quasi-equilibrium threshold voltage $V_{tho}$, and backscattering coefficient $r_C$. We can calculate the current mismatch in above-threshold regions by using the new mismatch model.

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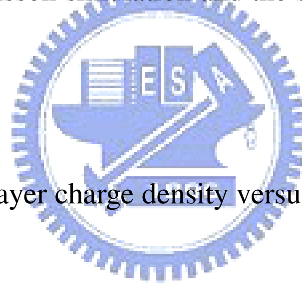

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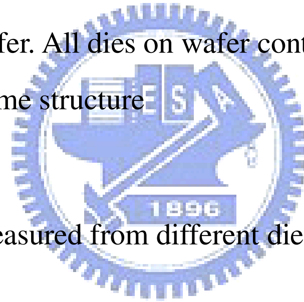

0.24um/0.065um, and the fitting curves from Eq. (3.9) are shown for comparison.

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# Chapter 1

# Introduction

It is well recognized that no two things in the world are exactly the same. This is why everything comes with tolerance. The same situation can be applied to MOSFET: no two transistors can be the same even they are identically drawn. For example, threshold voltages are different, drain currents are different, etc. Mismatch reflects the different performance of two or more devices under the same operation. It is widely recognized that mismatch is a key to precision analog IC design. If not properly controlled, mismatch results in the performance degradation, the circuit malfunction, and even the drop of yield. Thus as device becomes smaller in today's VLSI technology, mismatch analysis becomes more and more important.

**Mismatch in above threshold region**

Because most of the transistors in the circuit operate under the saturation region, the mismatch in the saturation region is noticed. From the traditional drain current model:

$$ID = \frac{W}{L}\mu C_{OX}(V_{GS} - V_{th})^2$$

We derive the current mismatch formula by using the drain current model based on backscattering model to resplace the traditional drain current model.

### Mismatch model

Although many mismatch models based on process parameters have been reported, the physical mismatch model using backscattering theory has never been discussed. As stated in backscattering theory, the nanoscale device performance is ultimately limited by the injection velocity and backscattering coefficient. The concept of channel backscattering is shown in Fig. 1. Both the carrier injection velocity and backscattering coefficient determine the current drive in nanoscale devices in the saturation region as given by [1,2]

$$I_{D,sat} = WC_{eff}v_{inj}[V_G - (V_{tho} - DIBL \times V_D)]\frac{1-r_c}{1+r_c}$$

where $v_{inj}$, $r_c$, and $V_{tho}$ are the thermal injection velocity at the top of source-channel junction barrier, the channel backscattering coefficient through the $k_BT$ layer, and the near thermal equilibrium threshold voltage, respectively. We derive a new simple analytic statistical mismatch model

in saturation region based on backscattering theory that has successfully reproduced the mismatch data in strong inversion for different dimensions. With this model included, the current mismatch can be expressed as a function of the coefficient of variation in the parameters : $V_{tho}$, $r_c$, and DIBL.

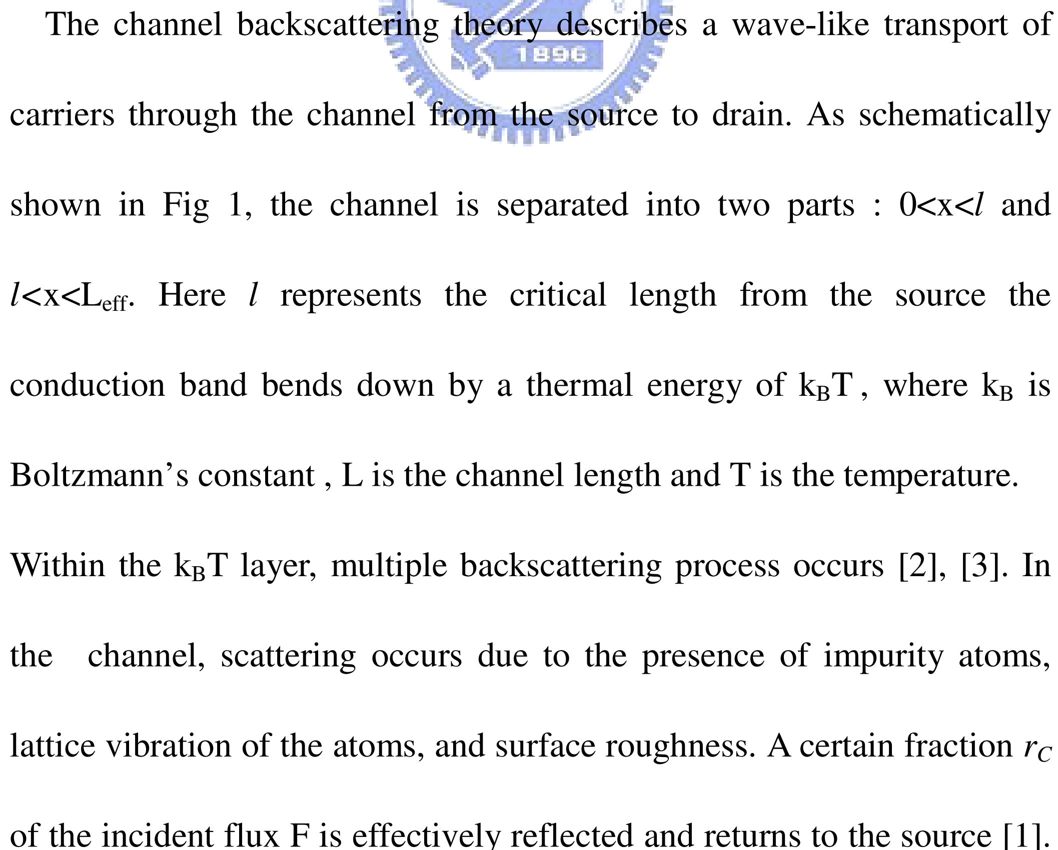
# Chapter 2

## Backscattering Theory and Parameter Extraction

In this section, we will explain the backscattering theory and the method of extracting the parameters. The main extraction procedure is demonstrated on the device size of W=1um and L= 0.1 $\mu$m with the measurement conditions: $V_G$ = 0~1.2V; $V_D$ = 0.01, 0.1, 0.5, and 1.0V; and the operating temperature = 298 $^{\circ}$K

### Section 2.1 Backscattering Theory

The channel backscattering theory describes a wave-like transport of carriers through the channel from the source to drain. As schematically shown in Fig 1, the channel is separated into two parts : 0<x<$l$ and $l$<x<$L_{eff}$. Here $l$ represents the critical length from the source the conduction band bends down by a thermal energy of $k_BT$ , where $k_B$ is Boltzmann's constant , L is the channel length and T is the temperature.



Within the $k_BT$ layer, multiple backscattering process occurs [2], [3]. In the channel, scattering occurs due to the presence of impurity atoms, lattice vibration of the atoms, and surface roughness. A certain fraction $r_C$ of the incident flux F is effectively reflected and returns to the source [1].

The total charge in the inversion layer comprises the injected and reflected components, is controlled by MOS electrostatics. The transmitted flux (1- $r_C$)F out of the $k_BT$ layer undergoes no net reflections to $k_BT$ layer due to significant potential gradient in the remainder of channel. Consequently, the drain current per unit channel width can be expressed as

$$I_D = Q_{inv} v_{inj} \frac{1 - r_C}{1 + r_C} \qquad (1)$$

Where $Q_{inv}$ is the inversion-layer charge density per unit area and $v_{inj}$ is the thermal injection velocity.

Experimentally, $r_C$ can be extracted by current-voltage (I-V) fitting [3]-[5]. Owing to multiple backscatterings in the $k_BT$ layer, both the quasi-equilibrium mean-free-path $\lambda$ and the width of $k_BT$ layer are functionally coupled through a single $r_C$ [2]

$$r_C = \frac{1}{1 + \frac{\lambda}{l}} \qquad (2)$$

In the saturation region, the formula of drain current region based on backscattering theory can be described as

$$I_{Dsat} = WC_{eff}(V_G - V_{th})v_{inj} \frac{1 - r_c}{1 + r_c} \qquad (3)$$

In real devices, the terminal drain current involves the drain / source series resistances, $R_D$ and $R_S$, and (Drain-Induced-Barrier-Lowering) DIBL. Thus the expression (3) is augmented into

$$I_{Dsat} = WC_{eff}[(V_G - I_D R_S) - (V_{tho} - DIBL \times (V_D - I_D R_S - I_D R_D))]v_{inj}\frac{1-r_c}{1+r_c} \qquad (4)$$

Here we neglect $R_S$ and $R_D$, the formula can be expressed as

$$I_{Dsat} = WC_{eff}[(V_G - (V_{tho} - DIBL \times V_D)]v_{inj}\frac{1-r_c}{1+r_c} \qquad (5)$$

## Section 2.2 Parameter Extraction

Flow-chart

Fig. 2 summarizes schematically the procedure of extracting $r_C$. The connection lines illustrate the relationship between the data and how to derive them in series. We would then demonstrate the extraction procedure based on the connection lines of the flow-chart.

## C-V Fitting

The measured C-V curve is compared with the calculated one by the quantum simulator with the gate oxide thickness $T_{OX}$, poly doping concentration $N_{poly}$ and channel doping concentration $N_{sub}$ as input.

$T_{OX}$, $N_{poly}$ and $N_{sub}$ each can be adjusted to affect the C-V curve, but only a distinct set of $T_{OX}$, $N_{poly}$ and $N_{sub}$ can be found with a perfect C-V

match. As shown in Fig. 3 $T_{OX}$ , $N_{poly}$ and $N_{sub}$ are simultaneously obtained by C-V fitting. Here, two different C-V comparisons were done: one from Schrodinger-Poisson solving [6] and the other from Berkeley's C-V simulation. They can both create desirable results, besides at high voltage where leakage current occurred in real experiment. C-V fitting eventually led to $T_{OX} = 1.4$ nm, $N_{poly} = 2.5\times10^{20}$ $cm^{-3}$, and $N_{sub} = 6\times10^{17}$ $cm^{-3}$ .

## Quasi-Equilibrium Device Parameter

With known $T_{OX}$ , $N_{poly}$ and $N_{sub}$ as input, the Schrodinger-Poisson solver was carried out to calculate the inversion layer $Q_{inv}$, the thermal injection velocity $v_{inj}$, and the effective gate capacitance $C_{eff}$. Fig. 4 shows the calculated inversion charges, $Q_{inv}$ , versus gate voltage. The thermal velocity, $v_{inj}$ , is displayed in Fig. 5 versus gate voltage. From these results, some properties can be drawn. First, at low gate voltage, or at the non-degenerate limit, the thermal velocity is regardless of gate voltage. Second, at the high gate voltage, or near degenerate limit, the thermal velocity increases with gate voltage. According to MOS electrostatics, $Q_{inv}$ can be expressed as

$$Q_{inv} = qn_s = C_{eff}(V_G - V_{tho}) \quad (6)$$

The effective oxide capacitive $C_{eff}$ is defined by [7]

$$C_{eff} = \frac{C_I C_Q}{C_I + C_Q} \quad (7)$$

where $C_I$ is the gate dielectric capacitance and $C_Q$ is the semiconductor (or quantum) capacitance related to the quantum mechanical confinement, polysilicon depletion, finite density-of-states, etc. From the slope of the $Q_{inv}$ versus $V_{GS}$, as shown in Fig. 6, we obtain $C_{eff}$ = 1.3926x10$^{-6}$ (F/cm$^2$).

## Drain Current against Gate Voltage

The drain current versus gate voltage, $I_D - V_G$, is measured under temperatures = 298K for different drain voltages of 0.01V, 0.1V, 0.5V, and 1.0V. The results are shown in Fig. 7 for W=1um, and L=0.1um.

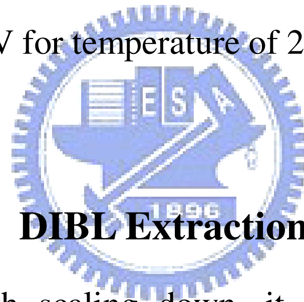
## Threshold Voltage

The threshold voltage is a key parameter in MOSFET design and modeling. There are many definitions and extraction methods for the threshold voltage. In this work, we employ a maximum trans-conductance method in the linear region to assess quasi-equilibrium threshold voltage and the constant subthreshold current method in the

saturation region to extract the DIBL [8].

## Quasi-Equilibrium Threshold Voltage Extraction

The maximum-$g_m$ method is used in the linear region with a low $V_{DS}$ of 10mV. In this method, a tangent line is established at the drain current with the maximum trans-conductance, as shown in Fig. 8. Through linear extrapolation to zero drain current, the quasi- equilibrium threshold voltage $V_{tho}$ was obtained. Fig. 9 shows the extracted $V_{tho}$ versus L. For L of 0.1um, $V_{tho}$ = 0.34688V for temperature of 298 °k.



## DIBL Extraction

With channel length scaling down, it is gradually important to consider short-channel effects such as $V_{th}$ roll-off and Drain Induced Barrier-Lowering (DIBL). We use constant subthreshold current method to determine threshold voltage operating in the saturation region (high $V_{DS}$). The critical constant current is defined as the drain current when the gate voltage is the threshold voltage from the maximum-gm method in the linear region [8], as shown in Fig. 10.

Drain-induced-barrier-lowering (DIBL) is defined as the gate voltage shift $(\Delta V_{GS})$ at the constant drain current due to a change in the drain voltage $(\Delta V_{DS})$. From Fig. 11, threshold voltage reduction due to

increasing $V_{DS}$ is mainly due to the DIBL effect. Fig. 12 shows threshold voltage versus L for drain voltage of 1 V. It can be seen that DIBL effect is insignificant for the long-channel device. With the channel shortening, DIBL effect imposes increasing influence on the threshold voltage.

## Results

According to the drain current formula (5), we can see that the parameters, $C_{eff}$ , $v_{inj}$ , DIBL, $V_{th}$ , and $r_C$ , have been extracted. Thus, the backscattering coefficient $r_C$ can be extracted by I-V fitting. The results are given in Fig. 13 (a) against gate voltage for $V_D$= 1V. Fig. 20 (b) and (c) are the case of $V_D$= 0.5V and 0.1V, respectively. From Fig. 13, it can be seen that (1) $r_C$ decreases with increasing gate voltage and then, critically, tends to saturate for $V_G \geq 0.8V$; and (2) at $V_D$=0.1V, $r_C$ is nearly constant.

# Chapter 3
# Mismatch Statistical Model

## Section 3.1 Mismatch in the above threshold region

We have extensively measured and analyzed the current mismatch of a small-size n-channel MOS transistor operated in the above threshold region with its p-well-to-$n^+$ source junction forward and reverse biased. The measured dependencies of the mismatch in the saturation region have been successfully reproduced by a new simple statistical model based on backscattering theory.

The transistors in the circuit usually operate in the saturation region, and one of the fundamental factors limiting the accuracy of MOS circuits operated in the saturation region is the current mismatch between identically designed devices. The poor control over the current match can cause a number of undesirable effects in the circuit level. Especially, in nanoscale devices, the effects are more and more serious.

## Section 3.2 Experiment

The measurement of current mismatch for identical devices was

achieved in terms of the dies on wafer as schematically shown in Fig. 14. All dies on wafer containing many n-channel MOS transistors have the same structure. They were fabricated using a 65 nm CMOS process. In our measurement of current mismatch, the p-well-to-$n^+$-source bias, $V_{BS}$, was fixed when sweeping $V_{GS}$ from 0 to 1.2 V in a step of 25 mV. The drain currents were measured and recorded for the subsequent analysis. The measurement setup contained the HP4156B and a Faraday box for shielding the test wafer, all performed in an air-conditioned room with the temperature fixed at 298°K. The total measurement time of one die's n-channel MOS for these full ranges was about 3 hours. A total of **25** n-channel MOS FETs were measured in one die. Fig. 15 depicts a typical measured I-V characteristic with $V_{GS}$ and $V_{DS}$ as parameters for the shown device size of W=0.24(um), and L=0.1(um).

## Section 3.3 Analysis and Modeling

The drain current mismatch $\sigma_{ID}$ is defined as the coefficient of variance of $I_D$: $\sigma_{ID} = I_{D\,(SD)}/I_{D\,(mean)}$ where $I_{D\,(mean)}$ and $I_{D\,(SD)}$ are the mean and SD ( standard deviation ) of drain current for all the same dimensions of n-channel MOS FETs. We analyze six device sizes from the data by

experiment, and calculate the mean and SD by a statistical tool. Fig. 16 shows the diagram of the calculated $\sigma_{ID}$ for different $V_{GS}$. From Fig. 16 we can observe that the drain current mismatch decreases with the increasing of $V_{GS}$ and becomes flat in above threshold region. From the backscattering theory, the drain current in the saturation region can be expressed as

$$I_{Dsat} = WC_{eff}[(V_G - (V_{tho} - DIBL \times V_D)]v_{inj}\frac{1-r_c}{1+r_c} \tag{3.1}$$

Now we propose a new simple statistical model to quantitatively account for the above observed dependencies of the mismatch in the above threshold region on the gate-to-source bias. As revealed by (3.1), our observed mismatch as a function of the $V_{GS}$ can be attributed to the coefficient of variation in the threshold voltage under the thermal equilibrium condition $V_{THO}$, the drain-induce-barrier-lowering DIBL, and the channel backscattering coefficient $r_C$. From (3.1) the mismatch of the current , $\sigma_{ID}$, can be derived as a function of the three coefficients of variance of the parameters : the coefficient of variance of the threshold voltage, $\sigma_{Vtho}$, the coefficient of variance of the drain-induce-barrier-lowering $\sigma_{DIBL}$, and the coefficient of variance of the

channel backscattering coefficient $\sigma_{rc}$ :

$$(\sigma_{ID})^2 = \frac{(DIBL \times V_D)^2}{[V_G - (V_{tho} - DIBL \times V_D)]^2}(\sigma_{DIBL})^2 + \frac{4r_c^2}{(1-r_c^2)^2}(\sigma_{rc})^2 + \frac{V_{tho}^2}{[V_G - (V_{tho} - DIBL \times V_D)]^2}(\sigma_{Vtho})^2 \quad \textbf{(3.2)}$$

This new formulation explicitly describes the dependence of $\sigma_{ID}$ on $V_{GS.}$ We can extract the $V_{THO}$ , DIBL, and $r_C$ from the drain currents of all dies on wafer that we measured, and calculate the coefficient of variance of the $\sigma_{Vtho}$, $\sigma_{DIBL}$, and $\sigma_{rc}$. We calculate the $\sigma_{rc}$ under $V_G$=1V and $V_B$=0V because the change of $\sigma_{rc}$ with gate voltage is very small. Fig. 17 shows that we use the backscattering mismatch model to reproduce the curve of the coefficient of variance of drain current versus $V_{GS}$ ($V_{GS}$ >0.5V) at $V_D$=1V, $V_B$=0V by calculating the appropriate $\sigma_{Vtho}$, $\sigma_{DIBL}$, and $\sigma_{rc}$ for the device size of width=0.24um, and length=0.1um. Thus we compare the parameters calculated with the parameters extracted by experiment: it can be observed that the differences between the calculated calculated parameters and experimentally extracted parameters are small.

**Mismatch model derivation based on backscattering theory**

The variance or standard deviation $\sigma_{g(x,y,z)}$ with three random variables of x, y and z can be expressed as

$$\sigma_{g(x,y,z)}{}^2 \cong (\frac{\partial g}{\partial x})^2 \sigma_x{}^2 + (\frac{\partial g}{\partial y})^2 \sigma_x{}^2 + (\frac{\partial g}{\partial z})^2 \sigma_z{}^2 + 2(\frac{\partial g}{\partial x})(\frac{\partial g}{\partial y}) C_{OV}(x,y)$$
$$+ 2(\frac{\partial g}{\partial x})(\frac{\partial g}{\partial z}) C_{OV}(x,z) + 2(\frac{\partial g}{\partial z})(\frac{\partial g}{\partial y}) C_{OV}(y,z) \tag{3.3}$$

where $\sigma_x$, $\sigma_y$ and $\sigma_z$ are the variances of x, y and z, respectively; and $C_{OV}(x,y)$, $C_{OV}(x,z)$ and $C_{OV}(y,z)$ is the correlation coefficient between (x, y), (x,z) and (y,z). To facilitate the analysis, we assume that $C_{OV}(x,y)$, $C_{OV}(x,z)$ and $C_{OV}(y,z)$ all are zero. Thus the coefficient of variance in the drain current $I_D$ can be written as

$$(\sigma_{ID})^2 = \frac{(DIBL \times V_D)^2}{[V_G - (V_{tho} - DIBL \times V_D)]^2} (\sigma_{DIBL})^2 +$$
$$\frac{4r_c{}^2}{(1 - r_c{}^2)^2} (\sigma_{rc})^2 + \frac{V_{tho}{}^2}{[V_G - (V_{tho} - DIBL \times V_D)]^2} (\sigma_{Vtho})^2 \tag{3.4}$$

The following backscattering current expression is considered for the mismatch model

$$I_{Dsat} = WC_{eff}[(V_G - (V_{tho} - DIBL \times V_D)]v_{inj} \frac{1 - r_c}{1 + r_c} \tag{3.5}$$

From (3.5) derivatives in (3.4) can easily be derived:

$$\frac{V_{tho}}{I_D} \frac{\partial I_D}{\partial V_{tho}} = \frac{-V_{tho}}{[V_{GS} - V_{tho} + DIBL \bullet V_D]} \quad ; \tag{3.6}$$

$$\frac{DIBL}{I_D} \frac{\partial I_D}{\partial DIBL} = \frac{DIBL \bullet V_D}{[V_{GS} - V_{tho} + DIBL \bullet V_D]} \quad ; \tag{3.7}$$

and

$$\frac{r_C}{I_D} \frac{\partial I_D}{\partial r_C} = \frac{-2r_C}{[1 - r_C{}^2]} \tag{3.8}$$

Thus we obtain a compact model :

$$\sigma_{ID} = \sqrt{\frac{(DIBL\times V_D)^2}{[V_G-(V_{tho}-DIBL\times V_D)]^2}(\sigma_{DIBL})^2+\frac{4r_c^2}{(1-r_c^2)^2}(\sigma_{rc})^2+\frac{V_{tho}^2}{[V_G-(V_{tho}-DIBL\times V_D)]^2}(\sigma_{Vtho})^2}$$

(3.9)

Apparently, (3.9) analytically expresses the current mismatch in strong inversion as function of the parameters of backscattering theory. We use (3.9) to reproduce the curve of current mismatch in other five device sizes by calculating $\sigma_{Vtho}$, $\sigma_{DIBL}$, $\sigma_{rc}$ in Fig. 18 and compare the calculated parameters with the experimentally extracted parameters. We can then observe that the differences between the two are small.

The corresponding calculated parameters and experimentally extracted parameters $\sigma_{Vtho}$, and $\sigma_{DIBL}$ versus the inverse square root of the device area are plotted in Fig. 19, and Fig. 20. The $\sigma_{rc}$ versus the channel length are plotted in Fig. 21. From these figures we can observe that the coefficients of variance of $V_{tho}$ and DIBL increase with decreasing device area, and the coefficient of variance of $r_C$ increases with decreasing channel length. From Fig. 22, Fig. 23, and Fig. 24, we have

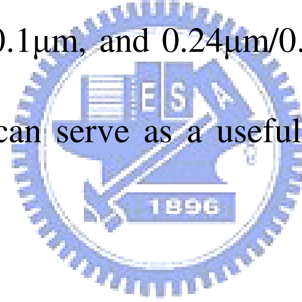
$$\sigma_{Vtho}=\frac{A_{Vtho}}{\sqrt{WL}},\ \sigma_{DIBL}=\frac{A_{DIBL}}{\sqrt{WL}},\ \text{and}\ \sigma_{rc}=\frac{A_{rc}}{L} \quad (3.10)$$

where $A_{Vtho}$, $A_{DIBL}$, and $A_{rc}$ are the size proportionality constants for $\sigma_{Vtho}$,

$\sigma_{DIBL}$, and $\sigma_{DIBL}$ respectively. The extracted values lead to $A_{Vtho}$ =0.01406μm, $A_{DIBL}$ =0.0296μm, and $A_{rc}$ =0.00702μm. Therefore, we use (3.10) to substitute (3.9)

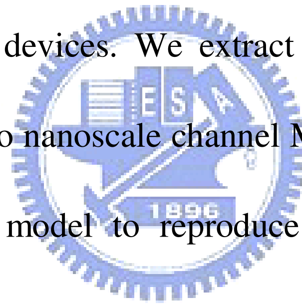
$$\sigma_{ID}=\sqrt{\frac{\left(DIBL\times V_D\right)^2}{[V_G-(V_{tho}-DIBL\times V_D)]^2}\left(\frac{\mathrm{A_{DIBL}}}{\sqrt{\mathrm{WL}}}\right)^2+\frac{4r_c^{\,2}}{\left(1-r_c^{\,2}\right)^2}\left(\frac{\mathrm{A_{rc}}}{\mathrm{L}}\right)^2+\frac{V_{tho}^{\;2}}{[V_G-(V_{tho}-DIBL\times V_D)]^2}\left(\frac{\mathrm{A_{Vtho}}}{\sqrt{\mathrm{WL}}}\right)^2} \tag{3.11}$$

We can calculate the drain current mismatch in the saturation region from (3.11) and compare with the curves of experimentally extracted $\sigma_{ID}$ versus gate voltage for W/L=1μm/0.5μm, 1μm/0.1μm, and 1μm/0.065μm; 0.24μm/0.5μm, 0.24μm/0.1μm, and 0.24μm/0.065μm in Fig. 25, and we can observe that (3.11) can serve as a useful analytic tool for properly calculating the mismatch.



# Chapter 4
# Conclusion

Mismatch is an important issue in today's VLSI technology. Lots of transistors in the circuit operate in the saturation region. We use the backscattering theory to derive the mismatch model in the saturation region. The drain current model in saturation based on backscattering theory is performed more accurately than the traditional drain current model in the nanoscale devices. We extract the parameters in a wide range of long channel to nanoscale channel MOSFETs and successfully use the new mismatch model to reproduce the experimental current mismatch.



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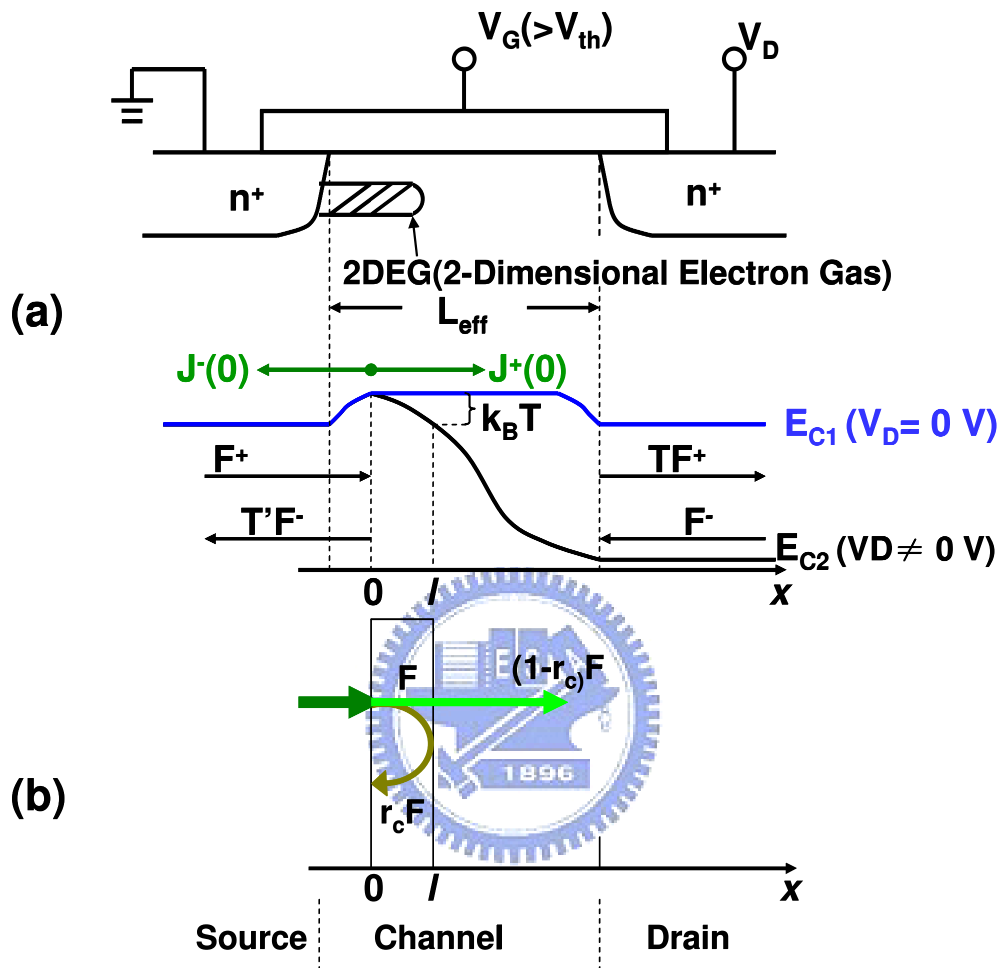
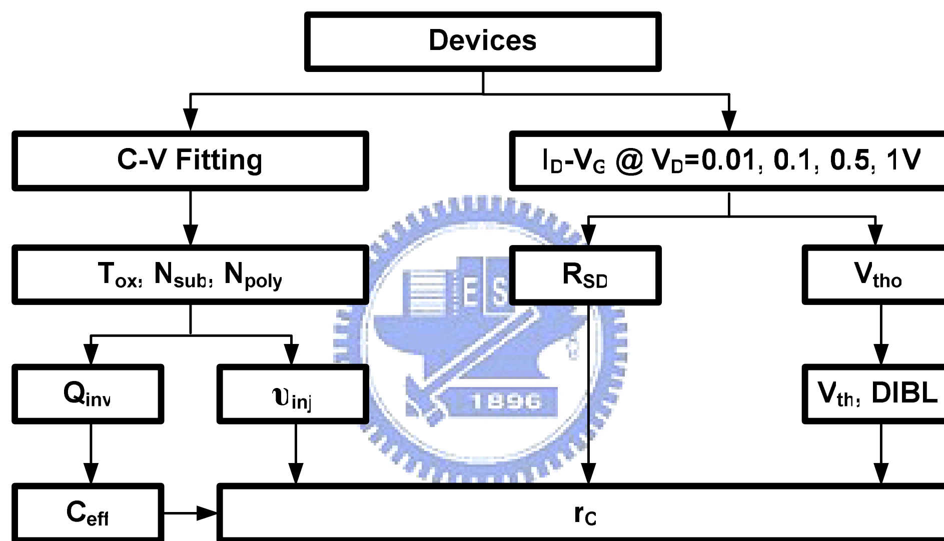



Fig. 1

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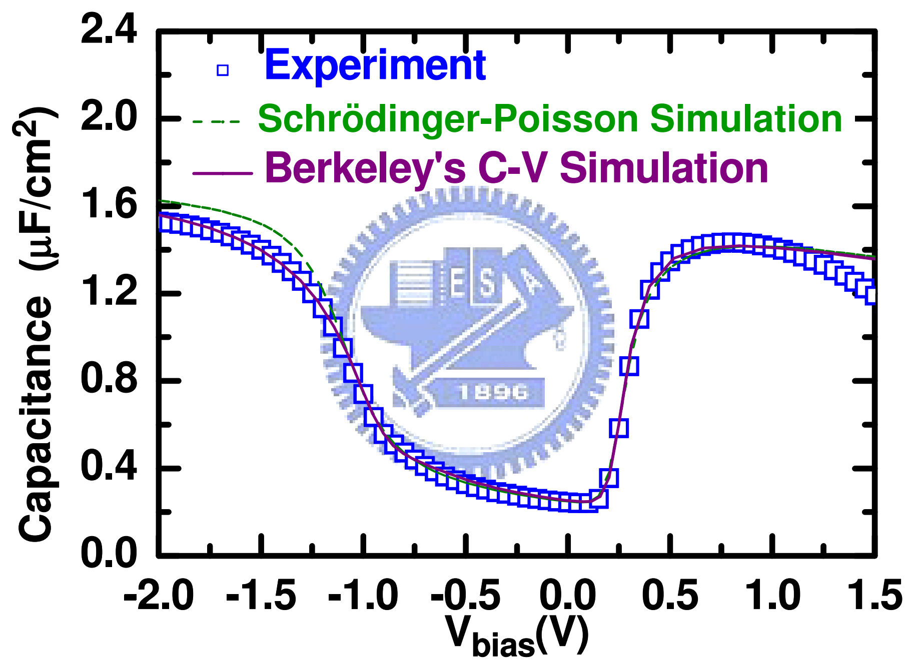


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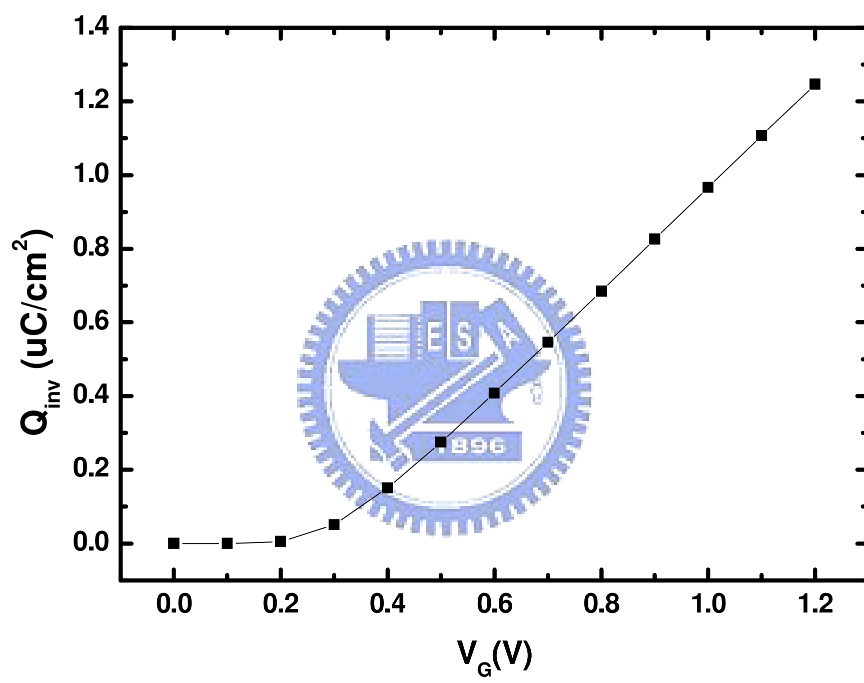


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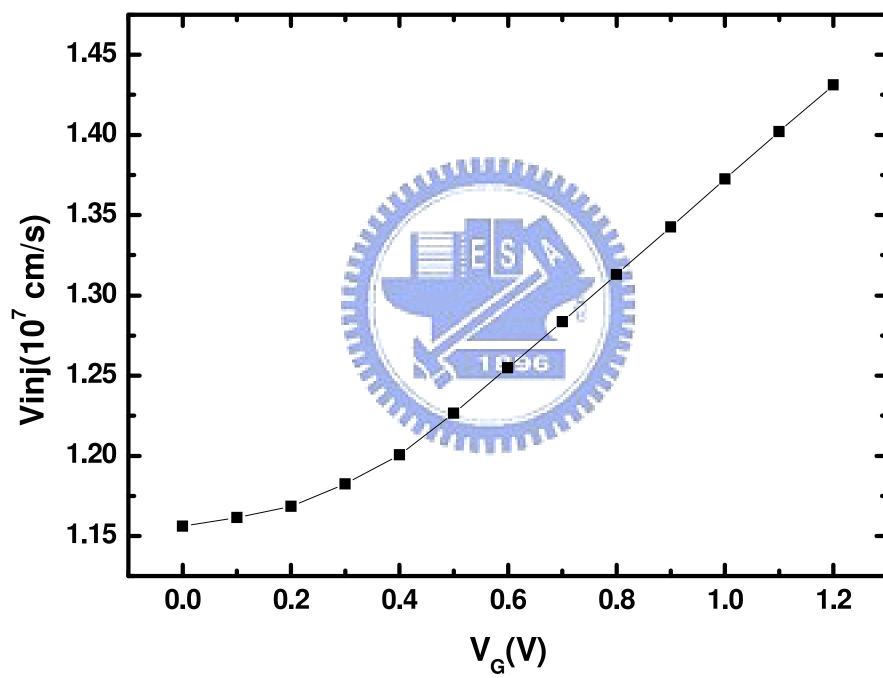


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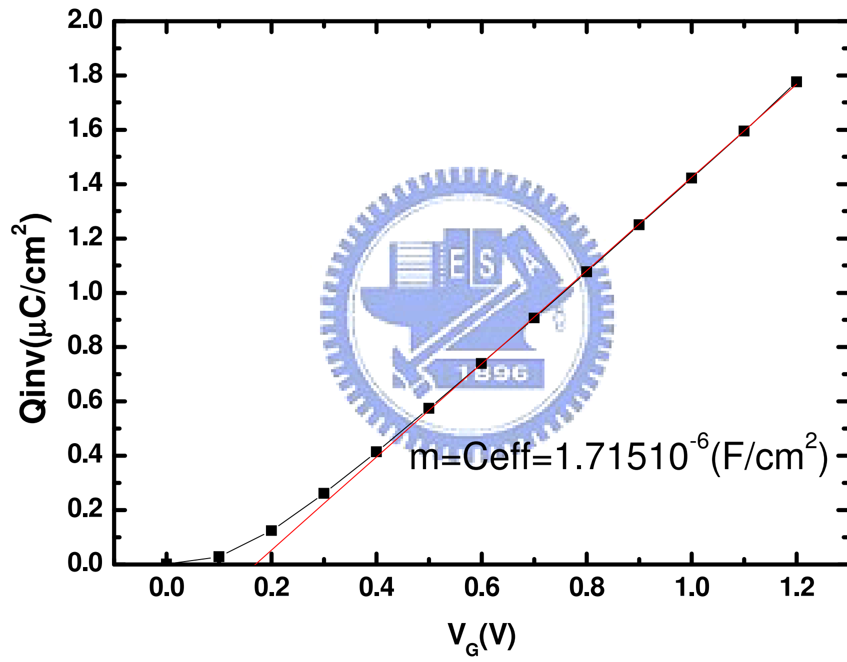
**Fig. 5**

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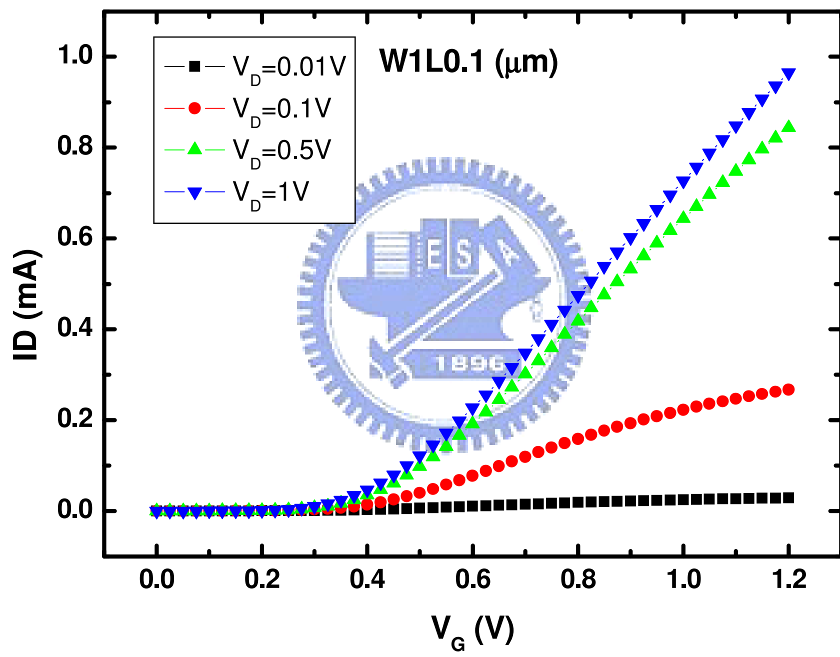


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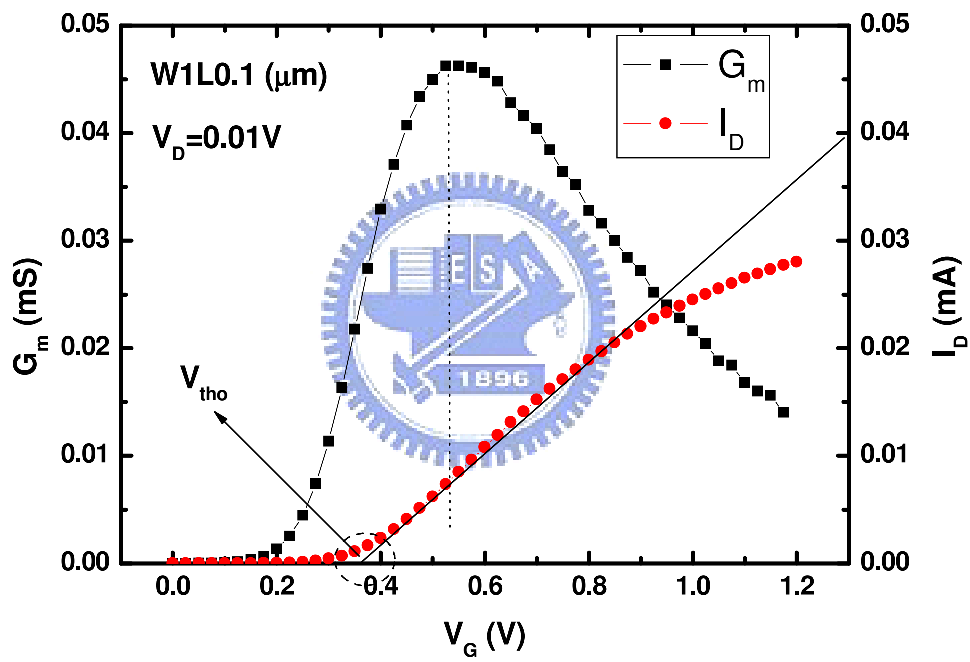


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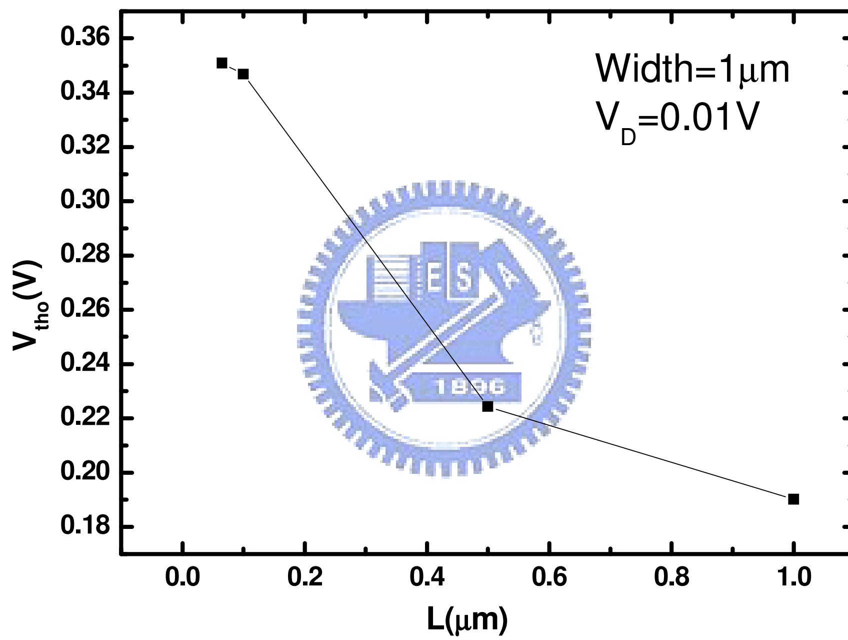


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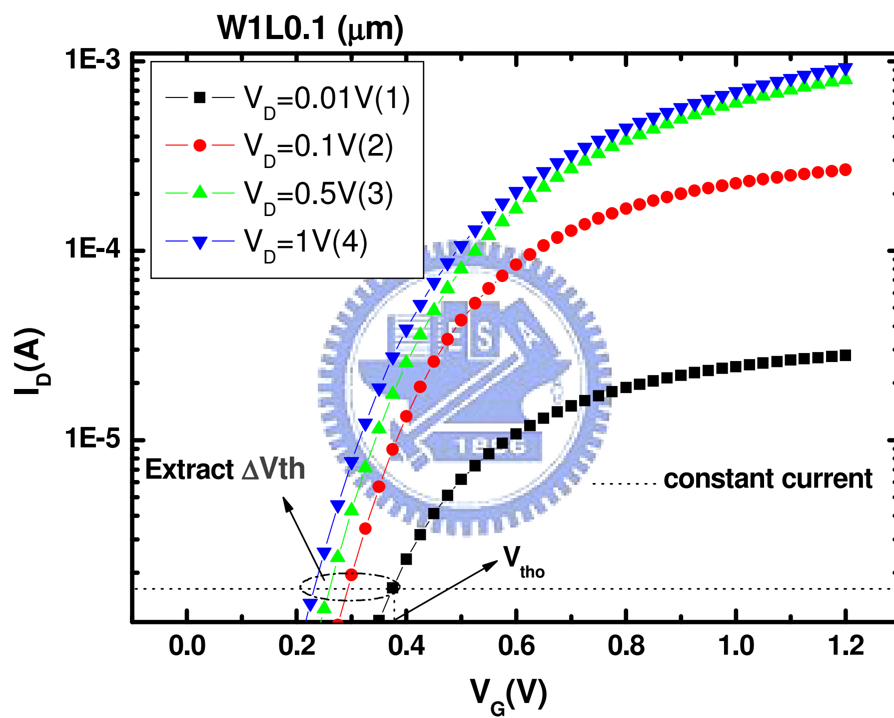


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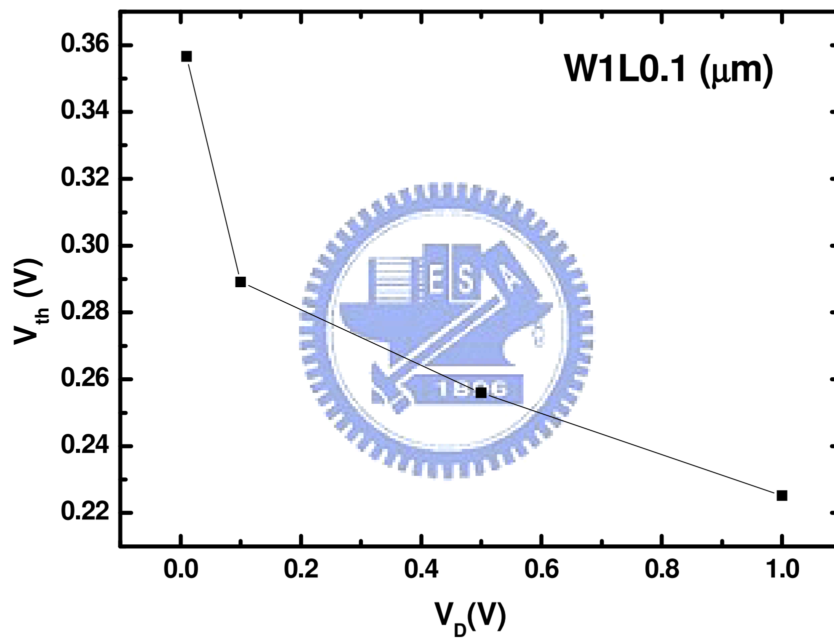


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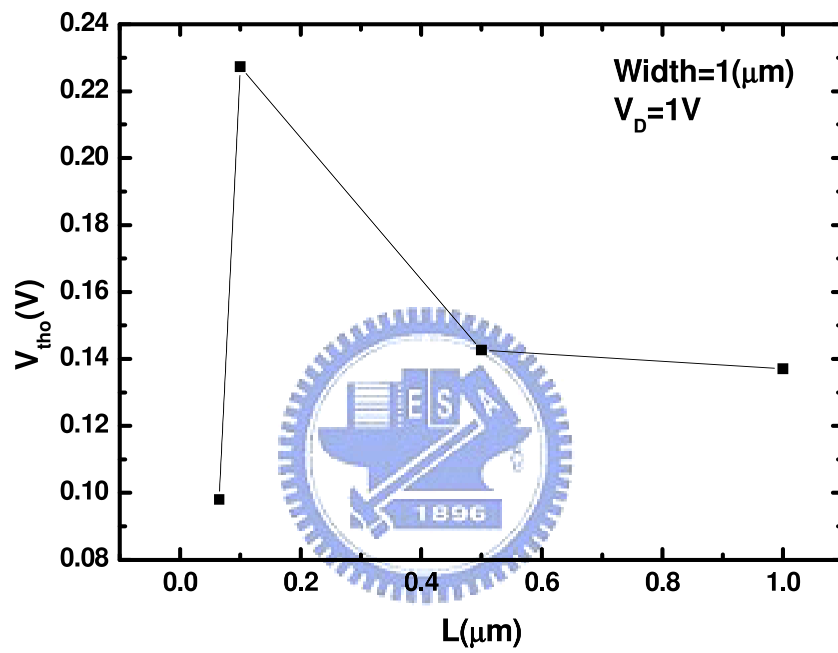


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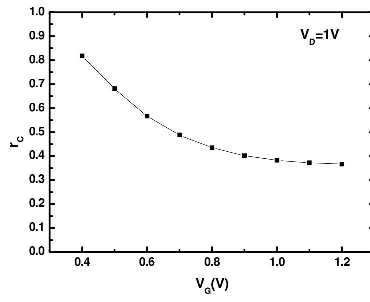
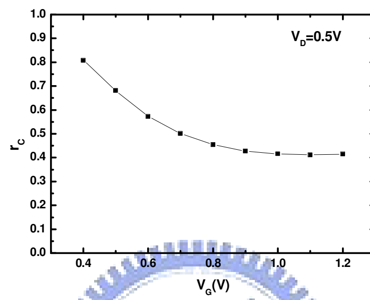
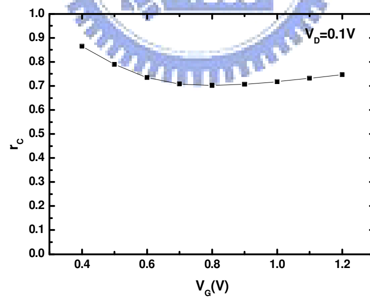



(a)




(b)




(c)

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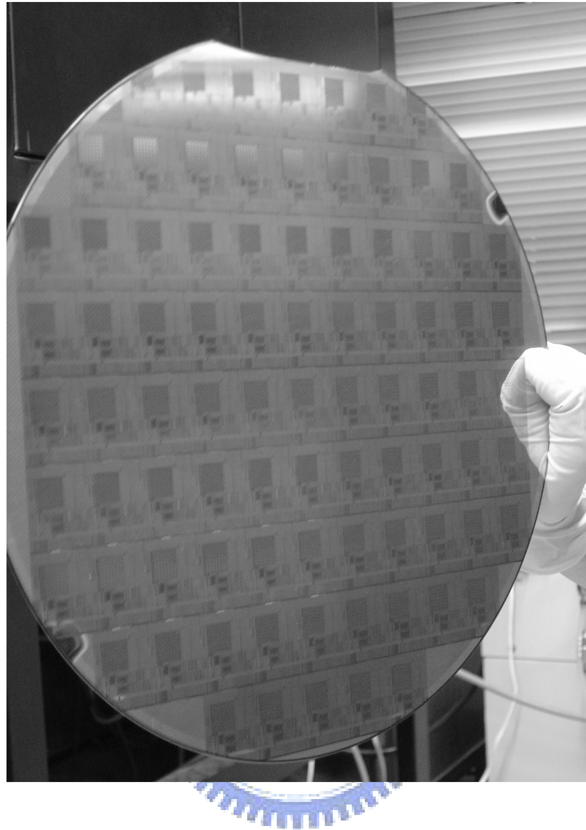

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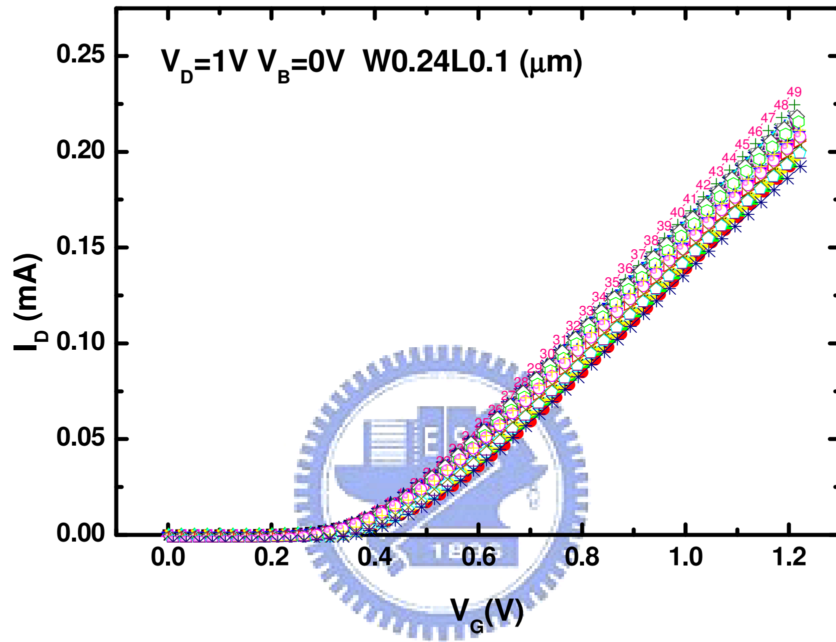


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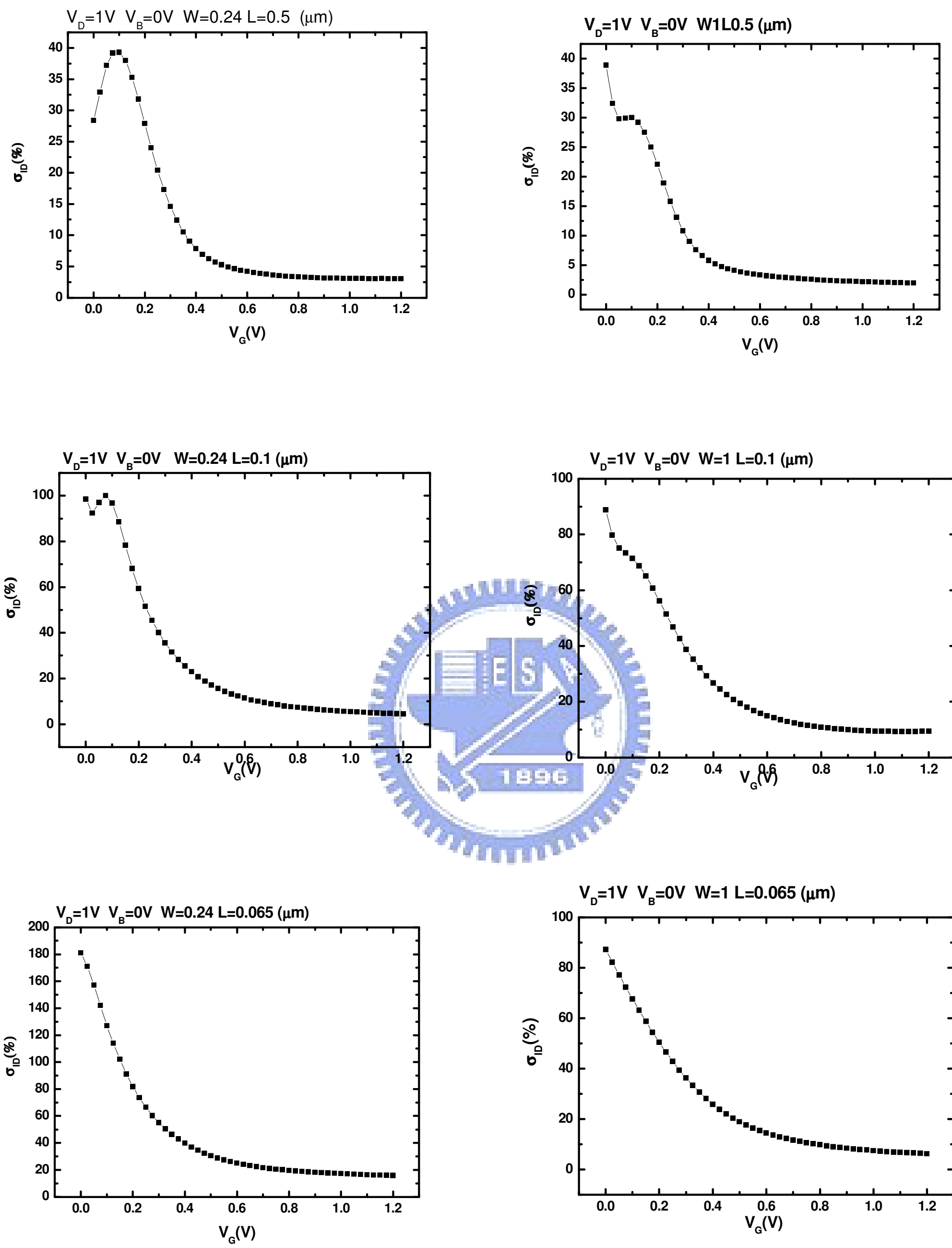



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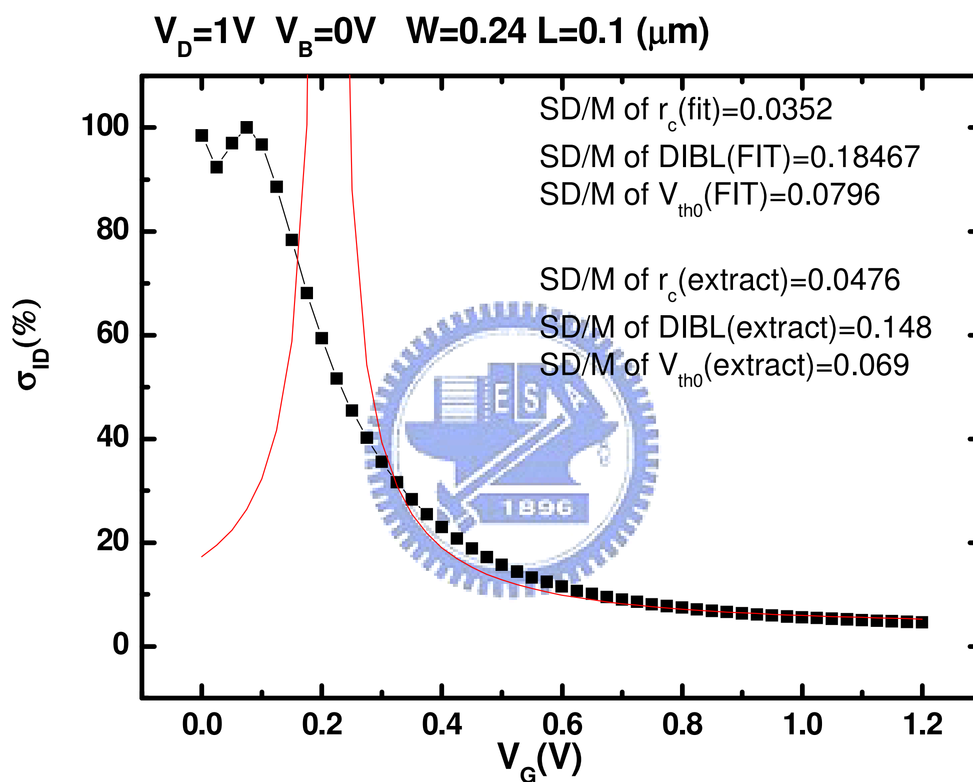
**Fig. 16**

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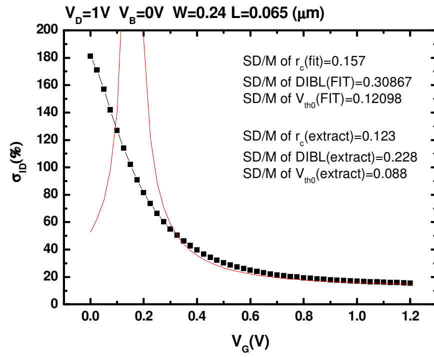


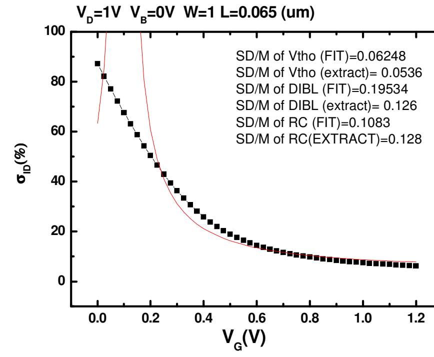


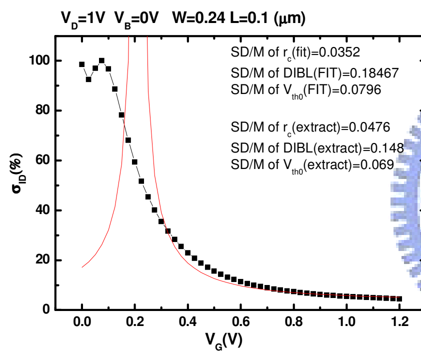


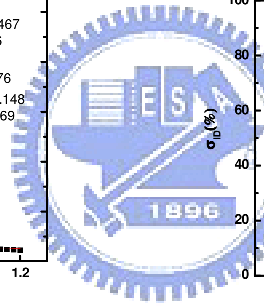

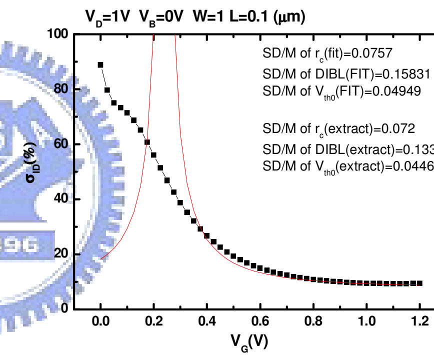


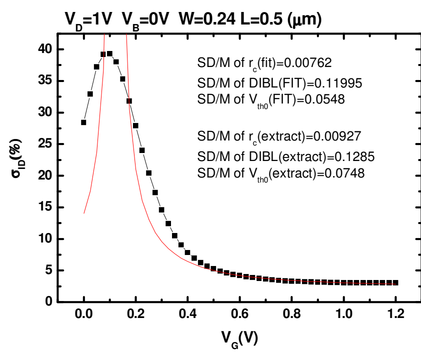


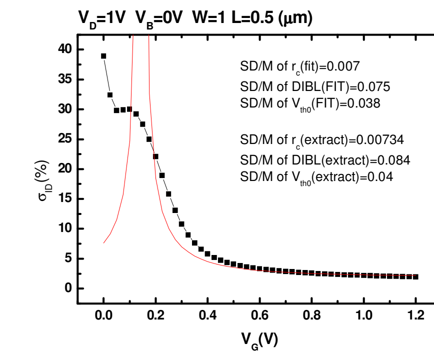


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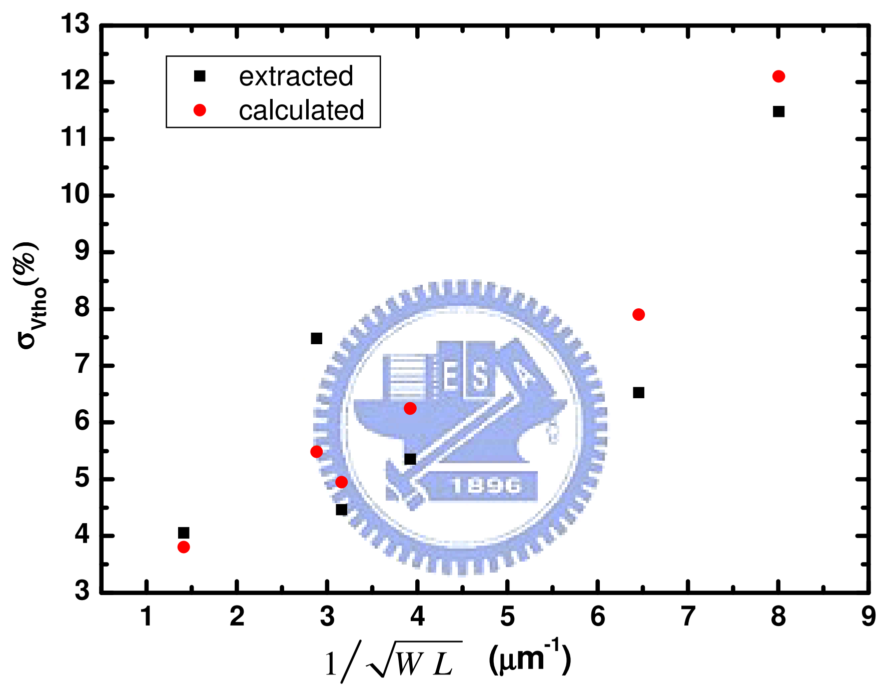


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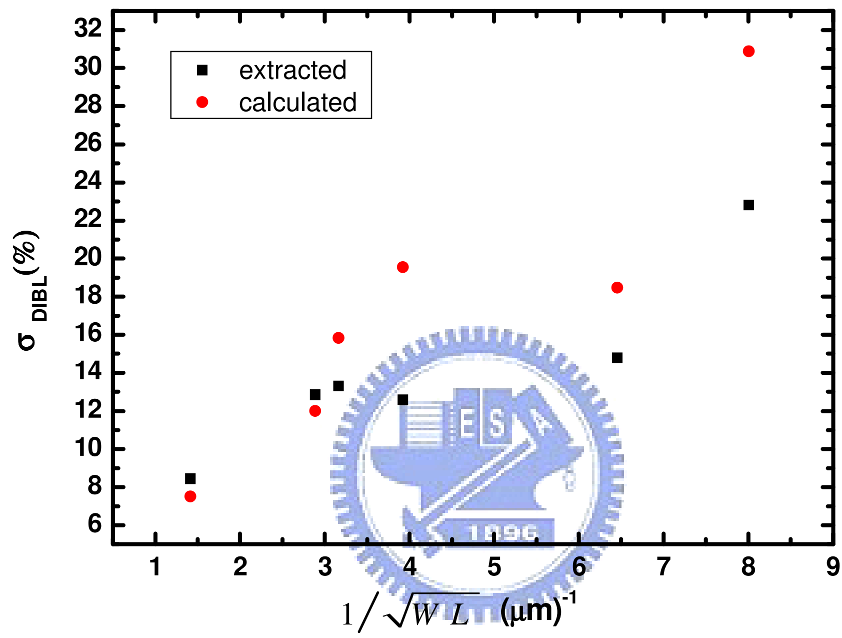


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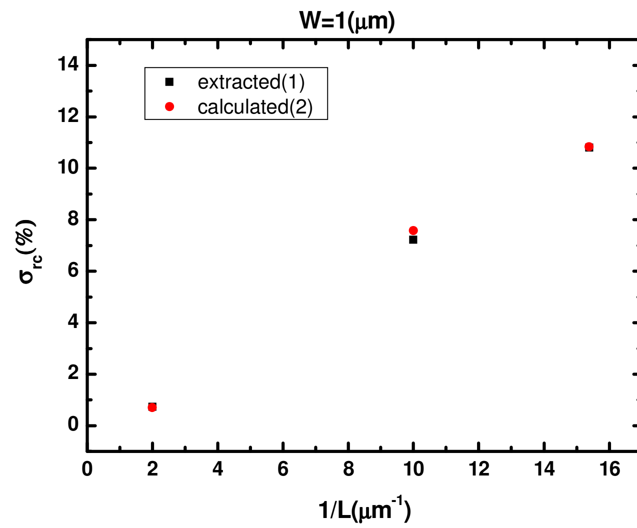


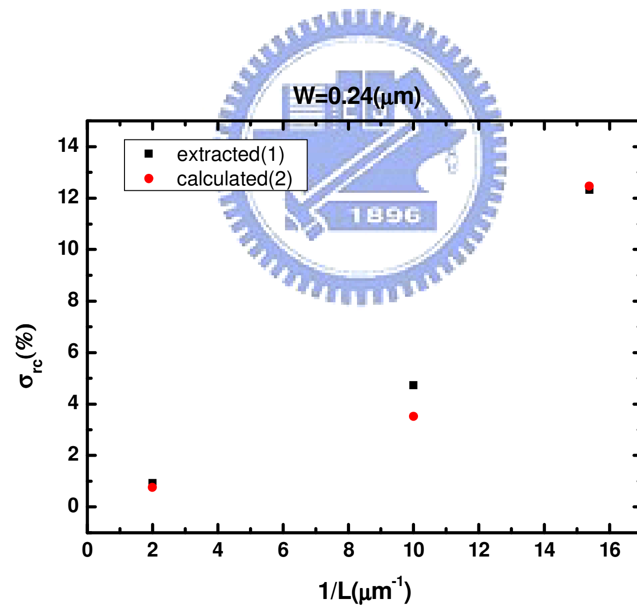


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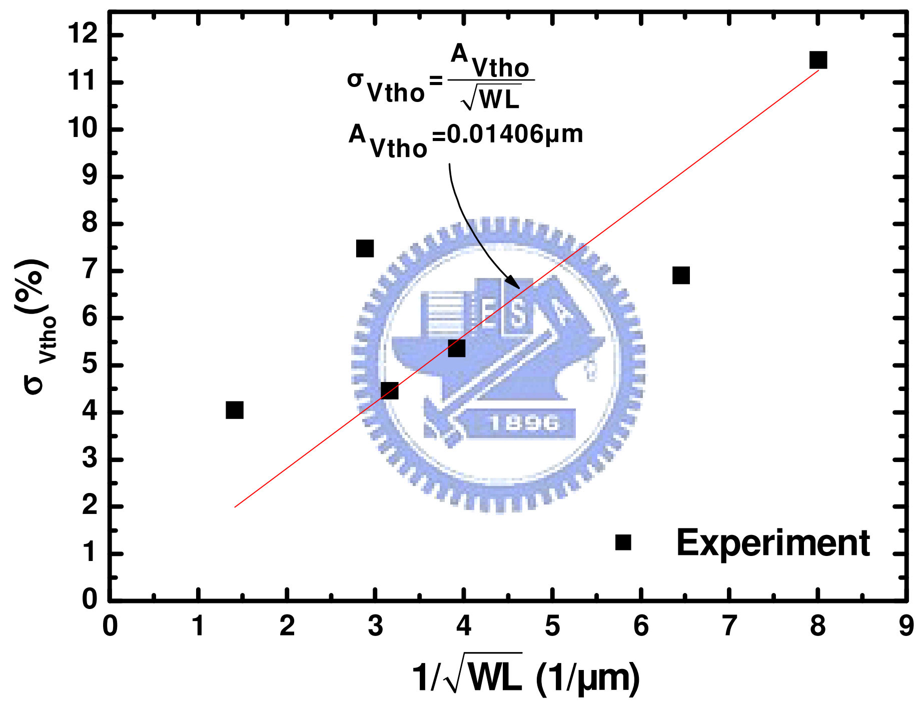


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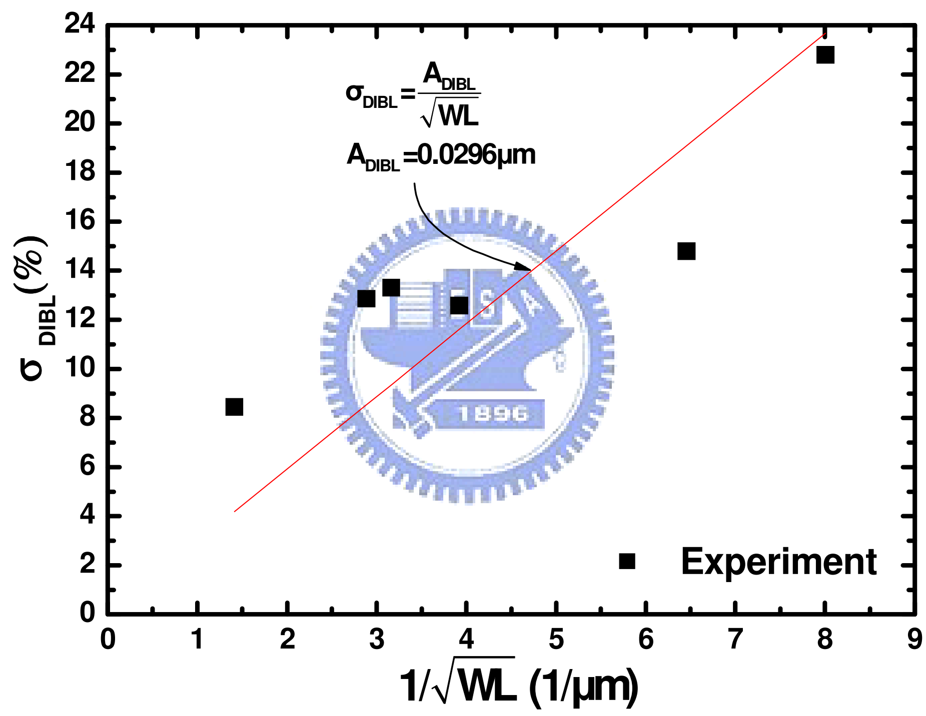
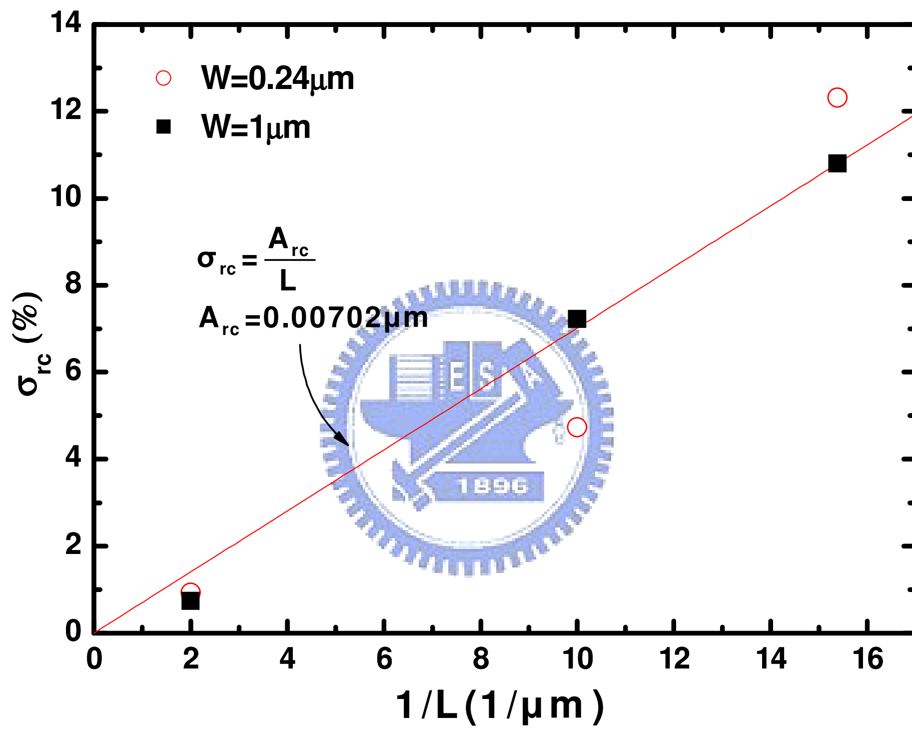



Fig. 23

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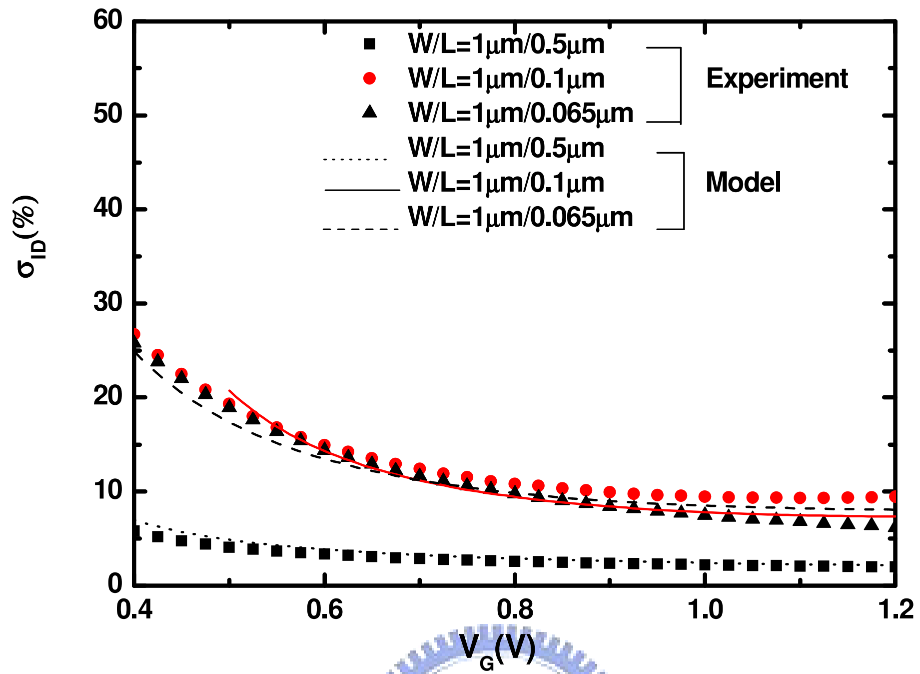


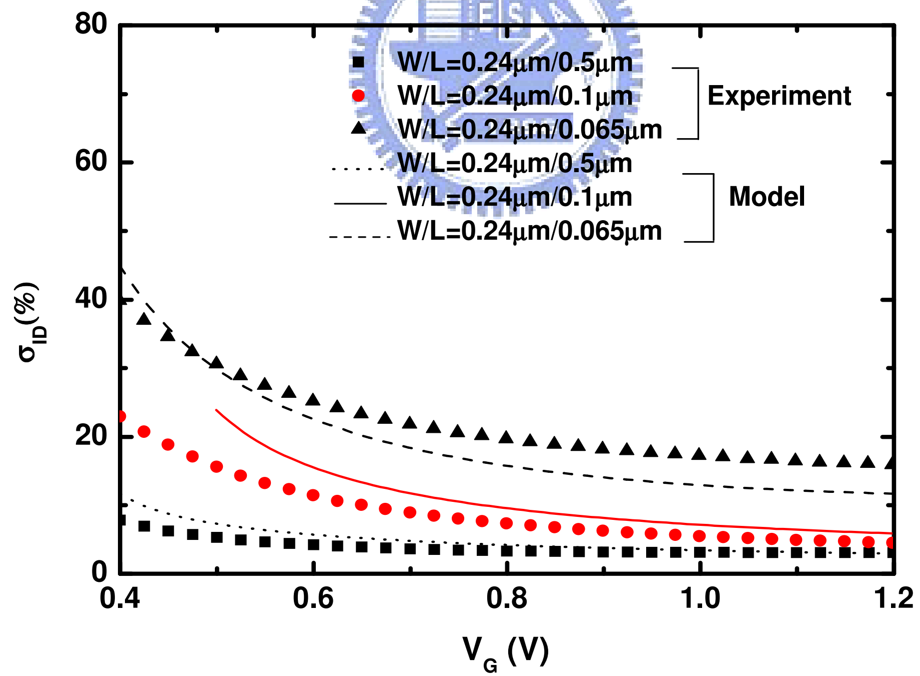


**Fig. 25**