


國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

形成矽化鎳時在矽化鎳與矽界面處離子活化相關研究



Research of Dopant Activation at the Interface
between Nickel Silicide and Silicon during Nickel
Silicide Formation

研究生：孫成業

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中華民國九十五年九月

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碩 士 論 文

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摘要

在先進互補式金氧半導體元件裡，當接觸尺寸縮小至奈米等級，源極及汲極的接觸電阻也會隨之增加。因此，金屬矽化物的技術應用在源極及汲極已經被開發用來同時降低接觸電阻及界面寄生電阻。在奈米金氧半場效電晶體的製造中，矽化製程是必須的，為了抑制源極及汲極的超淺界面形成所產生的短通道效應。所以，是否具有與矽基材完好界面特性的金屬矽化物，是在製造奈米尺寸的元件時重要的製程考量。在本論文中，我們主要探討離子佈植入矽化鎳再經由後續不同條件的退火製程後，所呈現出的活化量及電特性的研究。吾人實驗結果顯示矽化鎳經兩階段退火有助於界面狀態的改善，並且使活化的摻雜物朝界面堆積，界面呈現歐姆接觸(Ohmic Contact)。但是硼摻雜物當退火溫度超過 $550\text{ }^{\circ}\text{C}$ 30 sec 會發生短暫增強擴散(Transient Enhanced Diffusion)使硼向矽基材擴散，磷摻雜物則有不會發生此種現象。具有較強的溫度免疫力，可適用於高溫製程。硼則是具有較好的低溫活化能力。

Research of Low Temperature Activation Nickel Silicide and Interface properties


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Abstract

The logo of National Chiao Tung University is a circular emblem with a gear-like border. Inside the circle, there is a stylized building and the letters 'ES' and 'A'. Below the emblem, the year '1896' is written.

In advanced CMOS devices, as contact dimensions scale down to nanometer range, contact resistance of source and drain is increased correspondingly. As a result, the technique of metal silicides for poly gate and source/drain has been developed to reduce the contact resistance and the parasitic junction resistance as well. In nanometer MOSFET fabrication, this silicidation process requires considering to suppress short channel effect (SCE) when forming the ultra shallow source and drain junction. Therefore, metal silicides owning a perfect interfacial property with Si above an ultra-shallow junction is considered as a critical module toward the realization of nano-scale CMOS. In the thesis, we want know the amount of activation and electro-characteristics by different thermal process. The experiments show that nickel silicide interface state improved by two-step rapid thermal annealing (RTA) process. And the

activation dopant accumulates toward the interface. The junction presents ohmic contact. The implanted boron sample occur transient enhanced diffusion result in boron diffuse toward silicon substrate above 550 °C 30 sec. This phenomenon does not occur in the implanted phosphorous sample. Has the strong temperature immunity, suitably in high temperature process. However the boron has good activation ability at low temperature.



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南風又輕輕的吹起，絲絲的離情充滿了整個校園，艷麗的鳳凰花悄悄在枝頭綻放，昔日的讀書聲，窗外的嬉笑聲，也將成為美麗的回憶，想到這裡內心是多麼沉重，一股股的心酸不時的湧上心頭。

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Table Captions

Chapter 1

Table 1-1 Comparison the characteristics of Ti, Co and Ni silicides.

Chapter 2

Fig. 2-1 Process recipe of NiSi/p⁺p junction by ITS scheme.



Figure Captions

Chapter 1

Fig 1-1 With/without creep up phenomenon of metal silicides.

Chapter 2

Fig. 2-1 Process flow of NiSi/p⁺p junction by ITS scheme.

Chapter 3

Fig. 3-1 AFM image shows NiSi/Si interface morphology by 2nd RTP annealing (a) 400 °C (b) 500 °C (c) 600 °C (d) 700 °C for 30 sec.

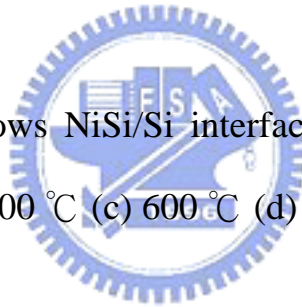


Fig. 3-2 RMS value of the interface roughness versus temperature with / without 2nd RTP annealing.

Fig. 3-3 SEM image shows NiSi formed by RTP annealing 400 °C for 30 sec.

Fig. 3-4 Four basic transport process under forward bias. [1]

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Fig. 3-6 The forward I_D - V_D characteristic curves of the NiSi/Si junction diode with 2nd RTA 30 sec by (a) BF_2^+ implantation and (b) P^+ implantation.

Fig. 3-7 The I_D - V_D characteristic curves of the NiSi/Si junction diode with 2nd RTA 30 sec by (a) BF_2^+ implantation and (b) P^+ implantation.

Fig. 3-8 The forward bias current density versus annealing temperature for the NiSi / Si junction diodes fabricated with (a) BF_2^+ and (b) P^+ implantation at various annealing time.

Fig. 3-9 The reverse bias current density versus annealing temperature for the NiSi / Si junction diodes fabricated with (a) BF_2^+ and (b) P^+ implantation at various annealing time.

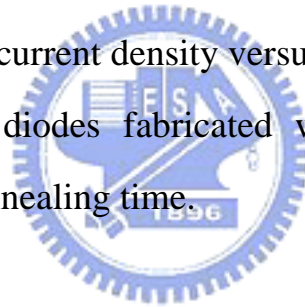


Fig. 3-10 The capacitance-voltage characteristics of Schottky junction diodes implanted (a) BF_2^+ and (b) P^+ without 2nd RTA.

Fig. 3-11 The doping concentration versus depth for the implanted (a) BF_2^+ and (b) P^+ by annealing at various temperature.

Fig. 3-12 The Active charge versus anneals temperature for (a) Boron and (b) Phosphorous implant.

Chapter 1

Introduction

1.1 General background

In order to improve the performance and packing density of metal-oxide-semiconductor (MOS) integrated circuit, the device dimension has been scaled down to nanometer region. In nanometer complementary metal- oxide- semiconductor (CMOS) circuit with gate length down to 0.1 μm , the parasitic resistance of gate, source and drain region will increase. Result in the increase of RC time delay and more power dissipation with integrated circuit.

In past years, many people effort to develop a new technology for reducing parasitic resistance to improve the device and circuit performance. Recently, the metal-silicide-related technology has become an integral part of nanometer devices for reducing the parasitic resistance in order to improve the devices and circuit performance. The major advantages of metal silicides can be grouped as follows:

(1) Their low resistivity for gate and interconnect applications, (2) easy

formation by self-aligned technology without any extra mask and compatible with conventional CMOS process.

Where the self-aligned silicide (salicide) process is widely used in MOS manufacturing to reduce the sheet resistance and contact resistance of the gate polysilicon. [1] In nanometer MOSFET fabrication, this silicidation process requires considering to suppress short channel effect (SCE) when forming the ultra shallow source and drain junction. Therefore, metal silicides owning a perfect interfacial property with Si above an ultra-shallow junction is considered as a critical module toward the realization of nano-scale CMOS. Besides, as the oxide thickness scaling down with the device dimensions, the gate oxide reliability will also be a concern for the silicided gate process.

Recently, numbers of silicide have been discussed to use to improve device performance, such as TiSi_2 , CoSi_2 , MoSi_2 and NiSi . Some of silicide, TiSi_2 , CoSi_2 and NiSi , has been used IC process. However, different silicide could observe different characteristics. Some properties have good merits for device fabrication, but some ones would affect the integrity circuit processes.

Titanium disilicide (TiSi_2) has been the most commonly used metal-silicide in ULSI process. Then, TiSi_2 must be phase transformation from the high resistivity phase C49 to low resistivity phase C54 [2-3]. As line keeps below $0.2 \mu\text{m}$, the width of C49- TiSi_2 is not enough to complete conversion to C54- TiSi_2 ($\geq 800 \text{ }^\circ\text{C}$) structure and the silicide agglomeration temperature limit ($\sim 950 \text{ }^\circ\text{C}$). Creep-up phenomenon is

also a problem of TiSi_2 process. During the silicidation of Ti/Si system, the Si atom is the dominant diffusing species. This facilitates the problem of creep-up in the MOSFET silicide structure, silicidation may occur on the side-walls, as shown in Fig 1.1. The possibility of Silicide Bridge forming between the gate and source or drain increases when creep-up is significant. As a consequence, there is an increasing need for new silicide material suitable for nanometer CMOS devices.

Cobalt disilicide (CoSi_2) is another alternative because CoSi_2 can be formed on narrow lines without the phase transformation problem and it has line width-independent sheet resistance. [4-5] However, CoSi_2 have major drawbacks. The formation of CoSi_2 consumes a relatively large amount of Si compared to the other silicides, as show in Table 1.1. Moreover, non-uniform CoSi_2/Si interface or Co spike will lead to the Increase of junction leakage. [6-7] This will be restricting the vertical scaling for CoSi_2 to achieve shallow junction.

Recently, nickel monosilicide (NiSi) has received more attention over the last years. Because of it has lower resistivity, lower Si consumption than TiSi_2 and CoSi_2 . Moreover, the film stress of NiSi is also much lower than that of TiSi_2 and CoSi_2 .

NiSi has another important advantage: reducing creep-up phenomenon. In the case of NiSi , silicidation proceeds by the diffusion of metal into the Si. So it can great amount reducing creep-up phenomenon. Recently, the work function of NiSi can be modulated by doping different dopants,

such as boron, arsenic. [8] These properties make NiSi suitable for nanometer CMOS technology.

NiSi has been widely used in industry. However, the problems encountered in the NiSi silicidation process are anomalously large junction leakage current and sheet degradation. Recently, using Ti or TaN cap [9] and nitrogen-doped [10] techniques have been reported to reduce junction leakage current. Ti or TaN cap structure on the Ni deposition can be an excellent oxygen scavenger and improve the large junction leakage during the thermal process.

1.2 Motivation

The rapid advance of integrated circuit technology has moved the minimum feature size into nanometer region. The vertical dimension also needs to be shrunk so as to improve the characteristics of device. Thus, reducing the junction depth becomes critical for advanced CMOS devices. Shallow junctions are hard to achieve because the ion implantation process will produce the implanted dopant profile to a given depth. Furthermore, the lateral spreading resistance and contact resistance of a shallow junction are often too large. [11]; as a result, the speed of device may be slowed down by the parasitic resistance. This problem can be alleviated by metallizing the source/drain junction with silicide. However, the quarter-micron device requires a junction depth of less than $0.1 \mu\text{m}$ and the silicidation of such a shallow source/drain junction will consume a good part of the high doping regions. The major obstacle for the silicidation of ultra shallow junctions comes from the nonuniform

silicide/silicon interface which may lead to local spiking of the junction. Consequently, the junction leakage may increase enormously after the silicidation process. To avoid this problem, the silicide film must be much thinner than the junction depth.

In this thesis, we want to investigate the activation of B and P implant through silicide (ITS). We clarified the thermal budget required for deactivation of B/P and also showed the impact of this phenomenon on achieving a shallow junction with a low sheet resistance.

1.3 Organization of the Thesis

In this thesis, we concentrate our efforts on the activation of B and P implant through silicide by RTA process. In chapter 1, brief introduction metal-silicide technology history evolution. In chapter 2, first overview of metal-silicide technology is given to describe the various applications and process technologies. Second the process flow of fabrication will be described.

In chapter 3, the detail discussion of characteristics includes physical properties, electrical properties, current transport mechanism, doping profile extraction and temperature effect. In chapter 4 is conclusions and chapter 5 is future works.

1.4 References

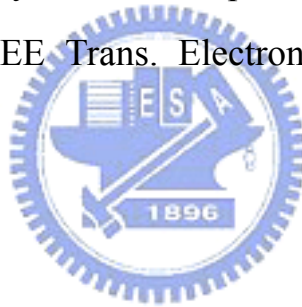
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Chapter 2

Formation and Characterization of Boron/Phosphorous Implanted Through Silicide by Subsequence Thermal Process

2.1 Introduction

As device dimension is scaled down to deep submicron, not only the size of gate electrode is shrunk, but also the vertical dimension of doped source/drain regions must be scaled to avoid device punch through and short channel effects. In the past, pn junctions were formed by dopant ion implantation into Si substrate followed by high temperature furnace annealing for dopant activation and implantation damage annihilation. However, channeling effect and high temperature dopant diffusion limit the formation of shallow junction. This is particularly important for the p^+n junction because boron is a light element and diffuses fast in silicon. In recent years, many advanced junction formation techniques have been studied using low energy ion implantation, low temperature annealing, and rapid thermal annealing process. These new methods are briefly reviewed as follows.

(1) Pre-amorphization of silicon substrate before dopant implantation

Pre-amorphization has been widely used to control the channeling

behavior of implanted dopant atoms. After the pre-amorphization of the silicon substrate surface layer, dopant implantation was performed followed by crystal regrowth and annealing process for the junction formation. Many heavy atoms have been used as pre-amorphization species, such as Si [1] and Ge. [2-3] Solid phase epitaxial (SPE) scheme can be used to regrow the crystal from the amorphous layer at a temperature as low as 550 °C [4]. The growth rate depends on the element used for pre-amorphization as well as the dopant implanted following the pre-amorphization. A careful annealing process is needed to annihilate the massive defects and dislocation induced by the pre-amorphization.

(2) Elevated source/drain structure

This method is to raise the source/drain regions by depositing a polysilicon (poly-Si) or amorphous silicon (α -Si) film or growing a selective epitaxial Si or SiGe layer. [5-6] Deposition of poly-Si/ α -Si film on the source/drain regions needs an additional lithographic step to define the elevated regions, while the selective epitaxial growth of silicon on the source/drain regions does not need such an additional lithographic step. The elevated source/drain regions made with selective epitaxial growth (SEG) provide a sacrificial layer for silicide formation and an alternative approach for the silicide process. However, the SEG scheme needs a high deposition temperature to obtain good crystallinity in the epitaxial layer. The fact that high temperature process deteriorates the device performance is the main disadvantage of this method. [7]

(3) Low energy ion implantation [8-10]

This is an extension of the conventional ion implantation technique. The implantation energy is lower than 1 keV and the implantation dose is typically from 1×10^{14} to 5×10^{14} cm^{-2} . The major disadvantage of this method is that no commercial implantation system of such a low energy beam line is available for high throughput mass production with reasonable cost.

(4) ITS/ITM technique

The implant through silicide (ITS) and implant through metal (ITM) processes have been investigated for shallow junction formation. The ITS/ITM process consists of implanting dopants into/through silicide or metal layer and the subsequent thermal annealing to form a silicide-contacted shallow junction [11-14]. The ITS scheme in particular is of much benefit to the formation of shallow junction. This is because metal silicides have a larger nuclear stopping power than silicon for the implanted dopant ions and thus can reduce the channeling effect; in addition, the junction formed by the ITS scheme can be almost free of implant damage, which is mostly confined in the silicide layer. Thus, the post-implant annealing temperature can be lowered while shallow junctions with superb characteristics can be obtained. Moreover, the silicided junction is conformal to the silicide/silicon interface, and thus the possibility of junction penetration by the silicide is reduced.

Boron is used for the extension and source/drain regions of pMOSFETs. Boron offers a high solid solubility, [15-17] which produces

a low resistance, but has a relatively high diffusion coefficient that results in deep junctions. Both the solid solubility and the diffusion coefficient increase with temperature. Therefore, it is difficult to realize a low resistance and shallow junction when using B. For these problems, we employ the ITS scheme which is used for silicide-contacted shallow junction formation.

2.2 Experiment

Samples were fabricated on p-type (100) oriented Si wafers. After a standard RCA clean process. Then, a 400 nm isolation oxide was grown on the wafer by wet oxidation at 1050°C for 30 min. The active regions were defined by the photolithography and etched by BOE (buffered oxide etchant) solution. Next, standard clean was used again to fully remove the contamination. Following, a 200 Å Ni deposited on the wafer in a dc sputtering system with a base pressure of less than 2.5×10^{-6} torr, using a Ni target in Ar ambient at a pressure of 2×10^{-3} torr with a deposition rate of about 0.1- 0.2 Å/sec. After the Ni film deposition, the samples were rapid thermal annealed (RTA) at 400°C for 30 sec in N₂ ambient to form NiSi. The unreacted Ni film was selectively etched using a solution of H₂SO₄ : H₂O₂ = 3 : 1 at 75~85 °C for 60 sec. The formed NiSi film thickness was determined by cross-sectional scanning electron microscopy (SEM). Then, the sample of NiSi were implanted with BF₂⁺ / P⁺ ions at an energy of 20 and 10 k eV to a dose of 1×10^{13} cm⁻². After ion implantation, followed by rapid thermal anneal (RTA) at 400 to 650 °C

for 30 / 60 / 90 sec in N₂ ambient for the activation dopant, as shown in Fig 2-1. Process recipe is listed in table 2-1.

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Chapter 3

Physical Properties and Electrical Characteristics of Boron/Phosphorous Implanted Through Silicide

3.1 Physical Properties boron/ Phosphorous implantation through silicide

3.1.1 Surface morphology by AFM inspection

In 1986, Binning et al. introduced another apparatus for surface characterization in atomic scale, the atomic force microscope (AFM). Since it can be applied to any types of material and environment, AFM has thus been used widely in surface characterization. Owing to its atomic scale resolution capability, AFM is also powerful equipment for nano-structure fabrication.

We want to inspect the surface morphology of NiSi/ Si interface by AFM. Because of the roughness between the NiSi/ Si interface related to the junction leakage. We want to know the impact on roughness of temperature.

Fig. 3-1 AFM image shows NiSi/Si interface morphology by 2nd RTP annealing (a) 400 °C (b) 500 °C (c) 600 °C (d) 700 °C for 30 sec. Fig. 3-2

RMS value of the interface roughness versus temperature with / without 2nd RTP annealing. For the 2nd annealing sample, the interface roughness is smoother than the without 2nd annealing sample. Therefore 2nd annealing may improve interface roughness.

3.1.2 SEM cross-sectional view inspection

In order to identify the real thickness of the as-deposited Ni film and the NiSi layer formed, scanning electron microscope (SEM) was used for cross sectional view inspection. Fig. 3-3 shows SEM image of NiSi layer formed by RTP annealing at 400 °C for 30sec.



3.2 Electrical measurements

The electrical properties of the silicide-contacted shallow junction diodes fabricated by the ITS scheme are dependent on a number of factors, including the dopant activation level, implantation damage recovery, silicide/silicon interface roughness, and the distance between the silicide/silicon interface to the junction position. All of these are closely related to the energy and dosage of the dopant ion implantation as well as the dopant activation ability and the drive-in diffusion during the subsequent annealing process; this is especially important for the case of low thermal budget and low energy implantation for the ITS scheme.

3.2.1 I-V measurement

The current transport in metal-semiconductor contacts is mainly due to majority carriers, in contrast to p-n junction, where the minority carriers are responsible. Fig. 3-4 shows four basic transport processes under forward bias.

The four processes are (1) transport of electrons from the semiconductor over the potential barrier into the metal [the dominate process for Schottky diodes with moderately doped semiconductors (e.g., Si with $N_D \leq 10^{17} \text{ cm}^{-3}$) operated at moderate temperatures (e.g., 300 °K)], (2) quantum-mechanical tunneling of electrons through the barrier (important for heavily doped semiconductors and responsible for most ohmic contacts), (3) recombination in the space-charge region [identical to recombination process in a p-n junction] and (4) hole injection from the metal to the semiconductor (equivalent to recombination in the neutral region). [1]

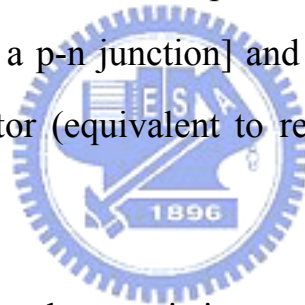


Fig. 3-5 shows the I_D - V_D characteristic curves of the NiSi/Si junction diode without 2nd RTA by (a) BF_2^+ implantation and (b) P^+ implantation. It is obvious that the NiSi/Si junction stills to appear the Schottky junction behavior both the BF_2^+ and P^+ implantation. The current transport leads by majority carriers from semiconductor over potential barrier into the metal.

Fig. 3-6 shows the forward I_D - V_D characteristic curves of the NiSi/Si junction diode with 2nd RTA 30 sec by (a) BF_2^+ implantation and (b) P^+ implantation. We after discovered the curve presents the ohmic contact the linear curve to pass through 2nd RTA 30 sec. The forward currents rise

along with the annealing temperature. After 550 °C maximize starts to reduce along with the temperature rise. According to the extrapolation: NiSi/Si interface damage is recovered and roughness repaired at 550 °C~650 °C. Fig. 3-7 shows I_D - V_D characteristic curves of the NiSi/Si junction diode with 2nd RTA 30 sec by (a) BF_2^+ implantation and (b) P^+ implantation. The I_D - V_D characteristic curves approximate linear. We knew schottky contact turns ohmic contact after the annealing process. Fig. 3-8 Forward bias current density versus annealing temperature for the NiSi/Si junction diodes fabricated with (a) BF_2^+ and (b) P^+ implantation at various annealing time. Forward bias current density drops along with the time and the temperature rise. High temperature and long time RTA process may promote interface state. Cause the tunneling current is reduction. [2-3]



3.2.2 Reverse leakage current density

Fig. 3-9 shows the reverse bias current density (J_R) versus annealing temperature for the NiSi / Si junction diodes with an area of 0.000625 cm² (250 × 250 μm) measured at a reverse bias of -5 V. The reverse bias current density (J_R) is determined by directly dividing the measured current by the diode's area. Roughness of the silicide/Si interface in a shallow junction may lead to the formation of localized Schottky contacts or the agglomeration-induced local silicide spiking, resulting in the increase of reverse bias current. After annealing at temperature above 600

°C 60 sec and above 500 °C 90 sec, the increased activation level, damage recovery level, and interface doping concentration should all have should all have contributed to better junction characteristics. [4]

3.2.3 C-V measurement and doping profile extraction

The capacitance-voltage (C-V) technique relies on the fact that the width of a reverse-biased space-charge region (scr) of a semiconductor junction device depends on applied voltage. This scr width dependence on voltage lies at the heart of the C-V technique. The C-V profiling method has been used with Schottky barrier diodes, p-n junction, MOS capacitance, and MOSFETs.

We consider the Schottky barrier diode. The semiconductor is p-type with doping density N_D . A dc bias V is applied to the metal contact. The reverse bias produces a space-charge region of width W . The differential or small signal capacitance is defined by

$$C = -\frac{dQ_s}{dV} \quad (3-1)$$

Where Q_s is the semiconductor charge. The negative sign accounts for more negative charge in the semiconductor scr (negatively charged ionized acceptors) for higher positive voltage on the metal. The capacitance is determined by superimposing a small-amplitude ac voltage v on the dc voltage V . The ac voltage typically varies at frequencies of

10 kHz to 1MHz with amplitude of 10 to 20 mV, but other frequencies and other voltages can be used.

Let us consider the diode to be biased to dc voltage V plus a sinusoidal ac voltage v . Imagine the ac voltage increase from zero to a small positive voltage adding a charge increasing dQ_m to the metal contact. The charge increment dQ_m must be balance by an equal semiconductor charge increment dQ_s for overall charge neutrality, where dQ_s is given by

$$dQ_s = -qAN_A(W)dW \quad (3-2)$$

The depletion approximation is employed in Eq. (3-2), i.e., the mobile carrier densities p and n are assumed to be zero in the depleted space-charges region. Furthermore, we assume $N_D = 0$ for this p -type substrate and we also assumed that all acceptors are fully ionized at measurement temperature. When that is not the case, as for acceptors and donors with energy levels deep within the band gap, true dopant density profile may not be measured.

The charge increment dQ_s , comes about through a slight increase in the scr width. From Eqs. (3-1) and (3-2) we find

$$C = -\frac{dQ_s}{dV} = qAN_A(W)\frac{dW}{dV} \quad (3-3)$$

In going from Eq. (3-2) to (3-3), we have neglected the term $dN_A(W)/dV$.

The assumes that N_A dose not vary over the distance dW , or variation of N_A over a distance dW cannot be obtained with the $C-V$ technique. The capacitance of in these equation is given in units of F not F/cm^2 .

The capacitance of a reverse-biased junction, when considered as a parallel plate capacitor, is

$$C = \frac{K_s \epsilon_0 A}{W} \quad (3-4)$$

Differentiating Eq. (3-4) with respect to voltage and substituting dW/dV into Eq. (3-3) gives

$$N_A(W) = \frac{C^3}{qK_s \epsilon_0 A^2 dC/dV} \quad (3-5a)$$

which can also be written as

$$N_A(W) = \frac{2}{qK_s \epsilon_0 A^2 d(1/C^2)/dV} \quad (3-5b)$$

Using the identity $d(1/C^2)/dV = -(2/C^3)dC/dV$. Note the area dependence in these expressions.

Since the area appears as A^2 , it is very important that the device area be width dependence on capacitance as

$$W = \frac{K_s \epsilon_0 A}{C} \quad (3-6)$$

Equations (3-5) and (3-6) are the key equations for doping profiling. The doping density is obtained from a $C-V$ curve by taking the slope dC/dV or from a $1/C^2-V$ curve by taking the slope $d(1/C^2)/dV$. The depth at which the doping density is evaluated is obtained from Eq. (3-6). For a Schottky barrier diode there is no ambiguity in the scr width since it can only spread into the substrate. Space-charge region spreading into the metal is totaling negligible. The doping profile equations are equally well applicable for asymmetrical pn junctions with one side of the heavily doped side is 100 or more times higher than that of the lowly doped side, then the scr spreading into the heavily doped region can be neglected, and Eqs. (3-5) and (3-6) hold. If that condition is not met, the equation must be modified or both doping density and depth will be in error. The correction, however, is fraught with difficulty. It has been proposed that no unique doping profile can be derived from $C-V$ measurements under those conditions. If the doping profile of one side of the junction is known, then the profile on the other side can be derived from the measurements. Fortunately, most pn junctions used for doping density profiling, are of the p^+n and n^+p type, and corrections due to doping asymmetries are not necessary.

Fig. 3-10 shows the capacitance-voltage characteristics of Schottky junction diodes implanted (a) BF_2^+ and (b) P^+ without 2nd RTA. We combine the Eq.3-5a and the Eq. 3-6. And extract the doping profile that

is shown in Fig. 3-11. We may observe the dopant to be able to approach NiSi/Si interface to pile up along with annealing temperature. That is called dopant segregation (DS). [5-6] Boron concentration near the NiSi/Si interface was about 10^{20} cm^{-3} after $550 \text{ }^\circ\text{C}$ annealing; it decreased slightly after $650 \text{ }^\circ\text{C}$. A low temperature annealing was able to accumulate the boron concentration near the NiSi/Si interface up to a very high value. At the $650 \text{ }^\circ\text{C}$ annealing, the boron concentration at NiSi/Si interface decreased to about 10^{18} cm^{-3} and significant boron diffusion was observed. Phosphorous concentration was about 10^{20} cm^{-3} near the NiSi/Si interface. After $650 \text{ }^\circ\text{C}$ annealing; it has not degradation phenomenon. Because of the implanted boron sample to occur transient enhanced diffusion in the early stage of the subsequent annealing process. [7-9] The Active charge versus annealing temperature for (a) Boron and (b) Phosphorous implant is shown Fig. 3-12. Obviously the active amount of boron is more than phosphorous about two times.

3.3 References

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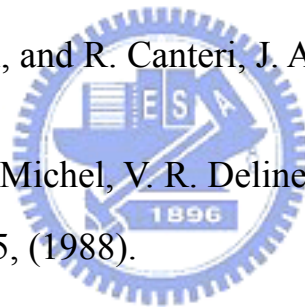
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Chapter 4

Conclusions

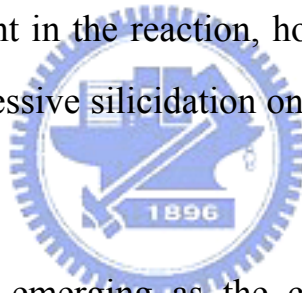
In this thesis, we have been investigated the activation of B and P implant through silicide (ITS) by RTA process. The schottky contact turns ohmic contact by 2 step RTA process. And the I_D-V_D characteristic curves present the linear curve to pass through 2nd RTA 30 sec. Also the NiSi/Si interface damage is recovered and roughness repaired by 2 steps RTA process. Short time annealing may cause interface to be smoother from AFM images knowing.

Obtain the doping profile using C-V measurement. We know the short-term annealing result in the dopant toward NiSi/Si interface accumulation. In implanted boron sample has the transition enhanced diffusion phenomenon. The boron atoms diffuse away into the silicon. Possibly cause sheet resistance rise at high temperature annealing. This phenomenon does not occur in the implanted phosphorous sample. Has the strong temperature immunity, suitably in high temperature process. However the boron has good activation ability at low temperature.

Chapter 5

Future Work

The overall integration of NiSi as the contact material in CMOS process flow is influenced by variables that include the substrate, metal deposition [1], ion implantation [2], and gate dielectric parameters. The two-step annealing sequence is common in the industry for Co and Ti silicide applications, and incorporates a wet removal of unreacted metal film after the silicide formation. In the case of Ni, the possibility of forming the mono-silicide phase in one step is under consideration. Since Ni is the diffusing element in the reaction, however, the one-step anneal process may result in excessive silicidation on the polysilicon layer of the gate stack [3].



Nickel silicide (NiSi) is emerging as the choice material for contact applications in semiconductor device processing for the 65nm technology node and beyond. The Ni/Si solid-state reaction has been widely studied in recent years [4-5], with several papers presented at recent IEDM conferences that highlight the merits of NiSi for shrinking device geometry, strained silicon in the channel [6], use in poly silicon-germanium, and use in dual metal-gate technology development [7].

Another challenge with the integration of NiSi is an increase in the junction leakage current due to the presence of a rough interface between NiSi and Si. Spike anneal offers the ability to limit diffusion, thereby

controlling the silicide-silicon interface morphology. It becomes increasingly critical to control silicon consumption as the junctions get shallower with technologies scaled at 45nm and beyond. As fully silicided gates are now being investigated as alternatives to metal gates, control of Ni diffusion in the (doped) polysilicon is critical to reap the benefits of work-function modifications while preventing Ni from diffusing into the gate oxide [8].

In addition to delineating the temperature effects of silicide formation, low-temperature processing capability will be useful for critical processes such as annealing high-k thin films and some backend anneal applications for future devices.



	Resistivity ($\mu\Omega\text{-cm}$)	Silicidation Temperature ($^{\circ}\text{C}$)	Silicon Consumption	Moving Species	Film Stress (dyn/cm^2)
TiSi_2	12-15	800-950	$0.9 \times T$	Si	1.5×10^{10}
CoSi	-	375-500	$0.91 \times T$	Si	-
CoSi_2	18	550-900	$1.04 \times T$	Co	1.2×10^{10}
NiSi	15-16	350-700	$0.82 \times T$	Ni	6×10^9
NiSi_2	35-50	700-850	-	Ni	-

T stands for thickness of silicide formed

Table 1-1 Comparison the characteristics of Ti, Co and Ni silicides.

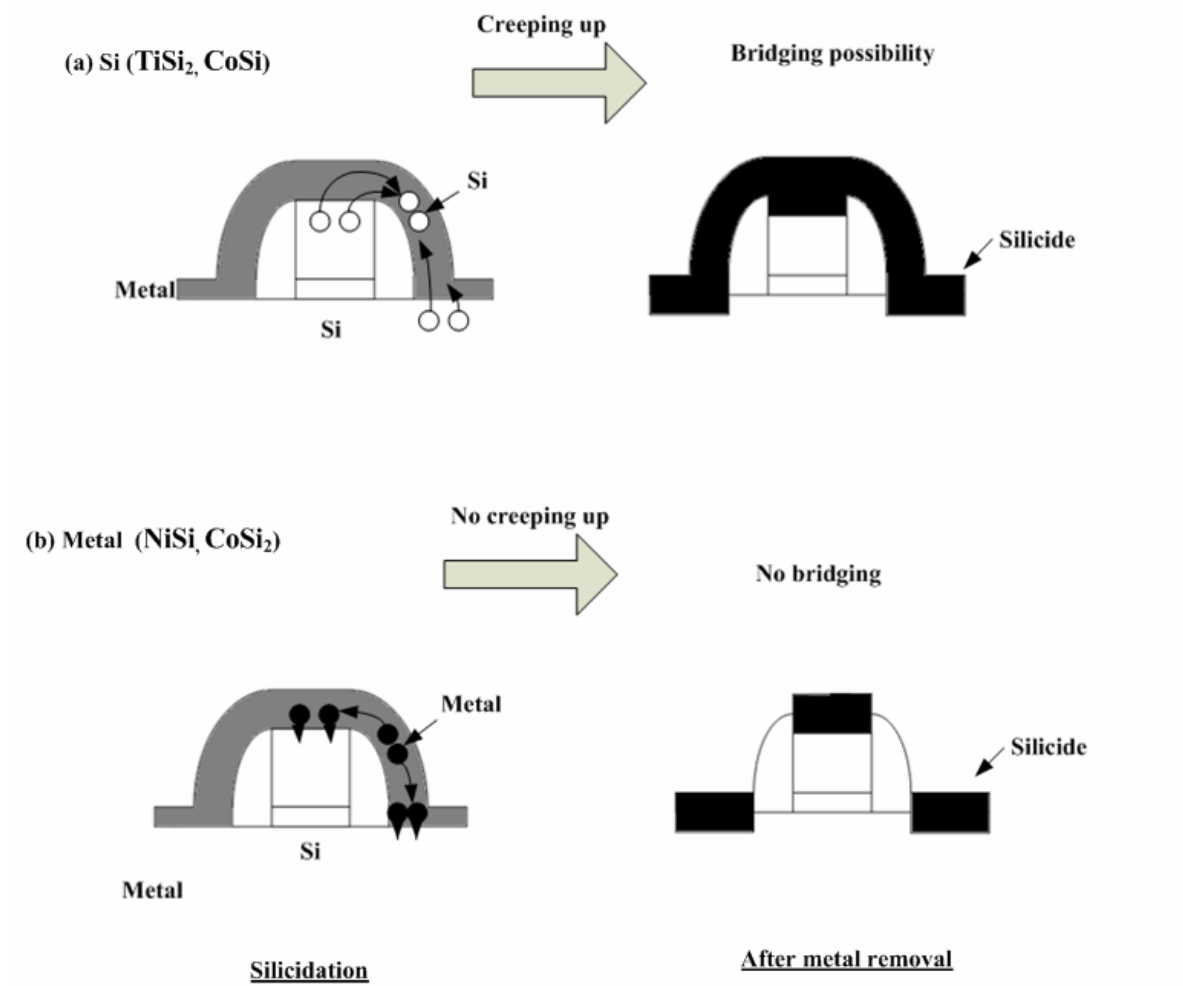
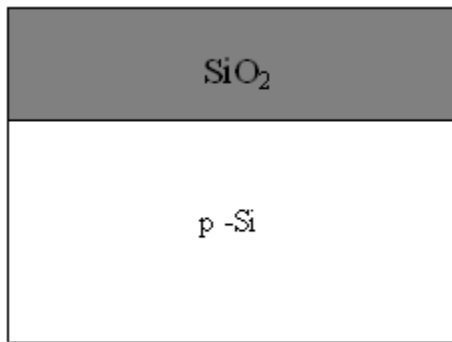
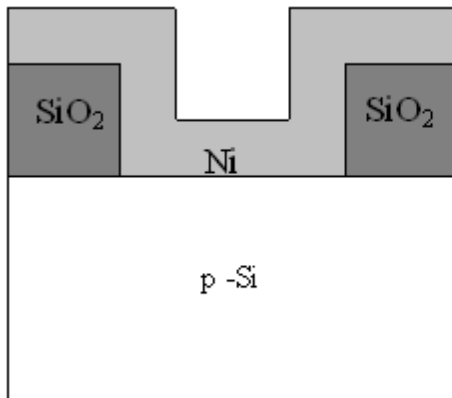


Fig 1-1 With/without creep up phenomenon of metal silicides.

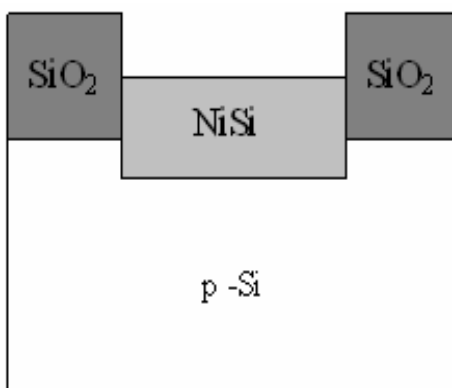


- **RCA Clean**

- **Field oxide growth**
Wet oxide 1050 /30 min

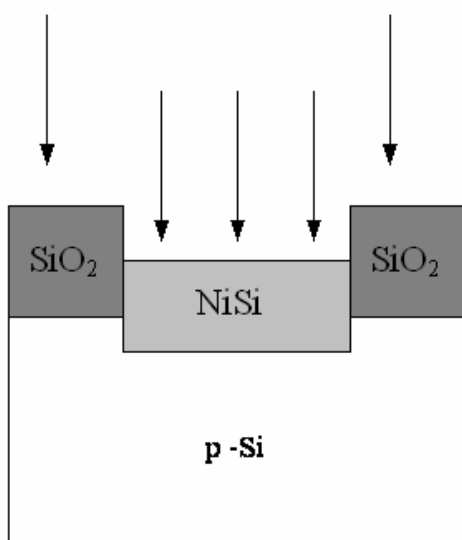


- **Ni film 200 Å deposition by sputtering**

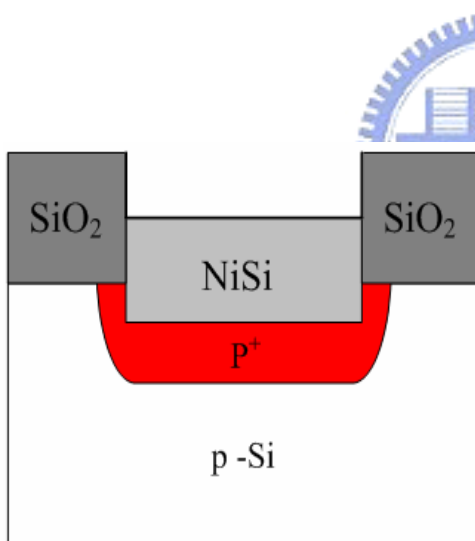


- **Silicidation by RTA 1(400 °C 30 sec)**

- **Selective etching (H₂SO₄ : H₂O₂ = 3 : 1) for unreacted Ni**



- Boron and phosphorous ion implantation



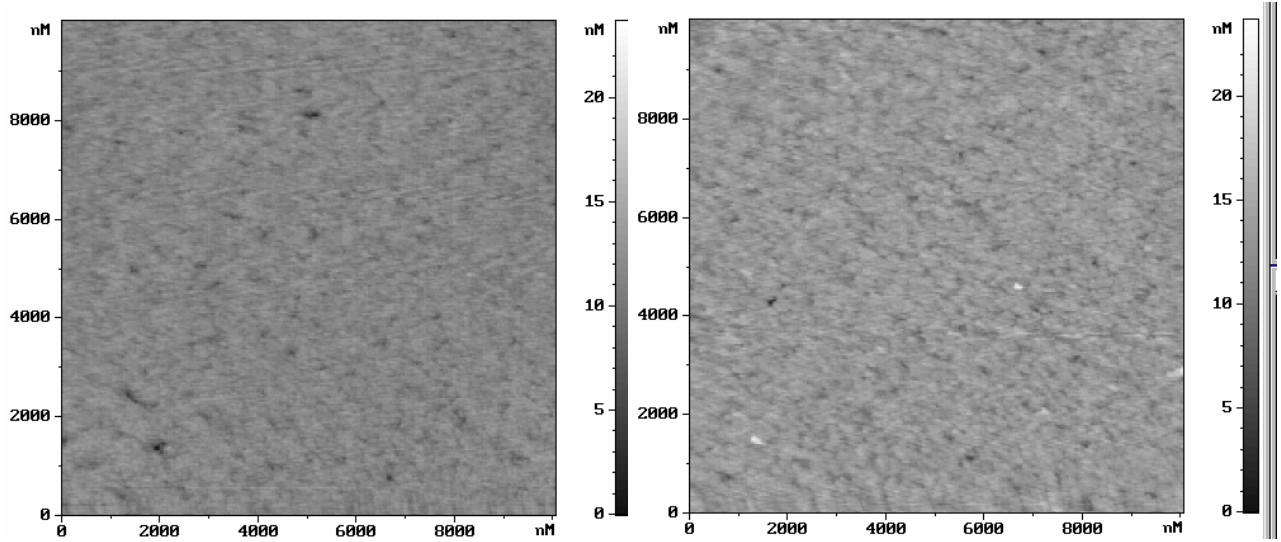
- Activation and junction formation
2nd RTA (400~650 °C)

Fig. 2-1 Process flow of NiSi/p⁺p junction by ITS scheme.

	Implanted ion	1st annealing	2nd annealing
p substrate	BF₂⁺/20 kev/1E13	400°C/30 sec	400 ~ 650°C 30 ~ 90 sec
n substrate	P⁺/10 kev/1E13	400°C/30 sec	400 ~ 650°C 30 ~ 90 sec

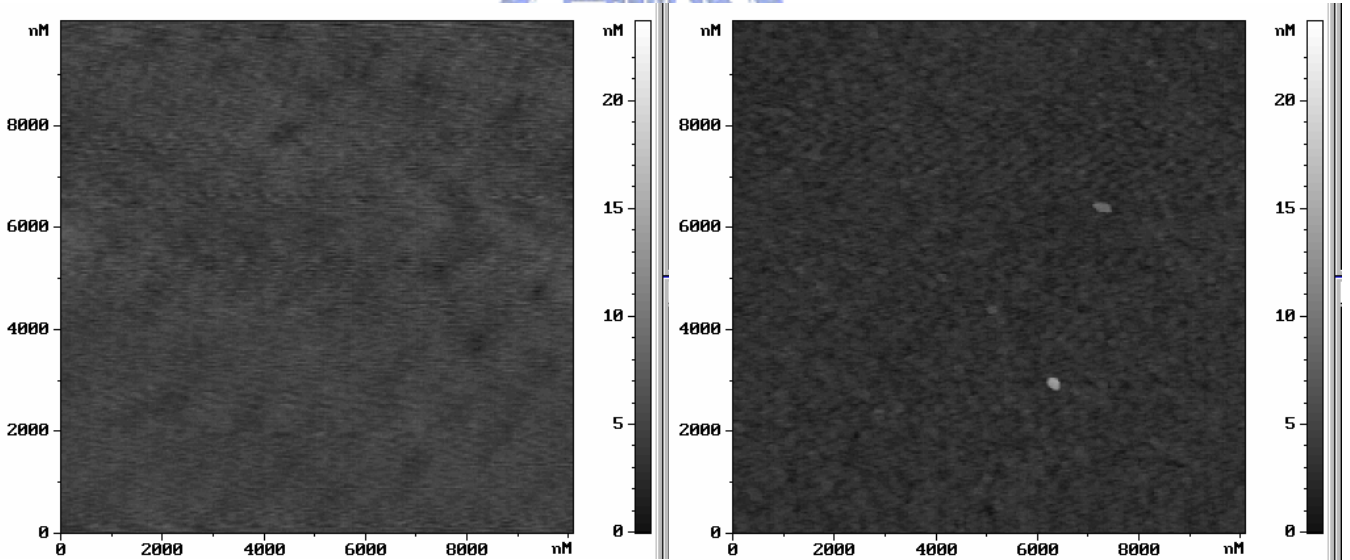
Fig. 2-1 Process recipe of NiSi/p⁺p junction by ITS scheme.





(a)

(b)



(c)

(d)

Fig. 3-1 AFM image shows NiSi/Si interface morphology by 2nd RTP annealing (a) 400 °C (b) 500 °C (c) 600 °C (d) 700 °C for 30 sec.

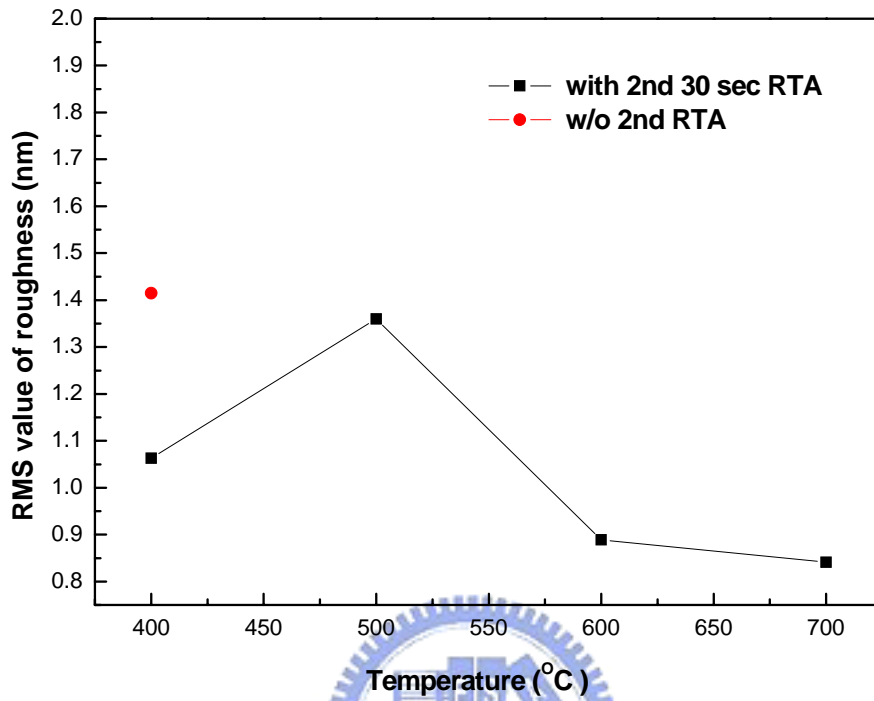


Fig. 3-2 RMS value of the interface roughness versus temperature with / without 2nd RTP annealing.

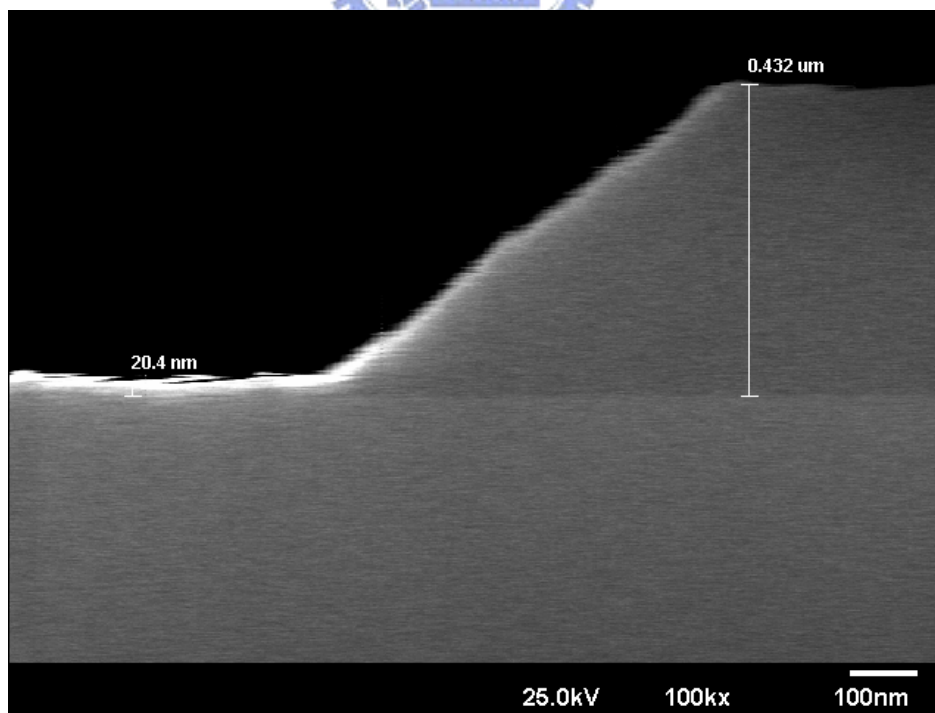
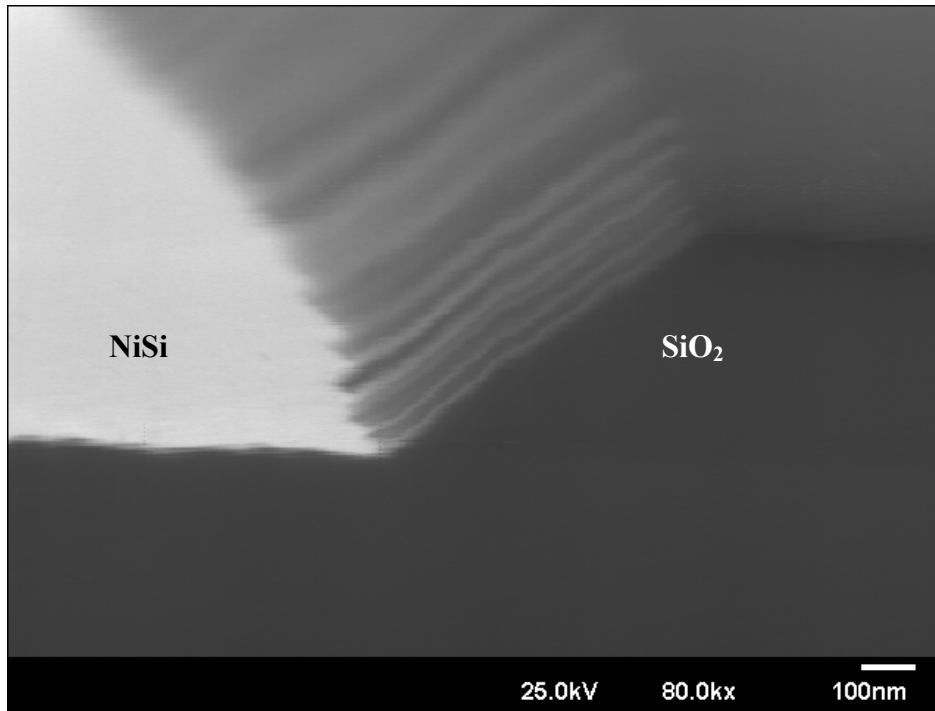


Fig. 3-3 SEM image shows NiSi formed by RTP annealing 400 °C for 30 sec.

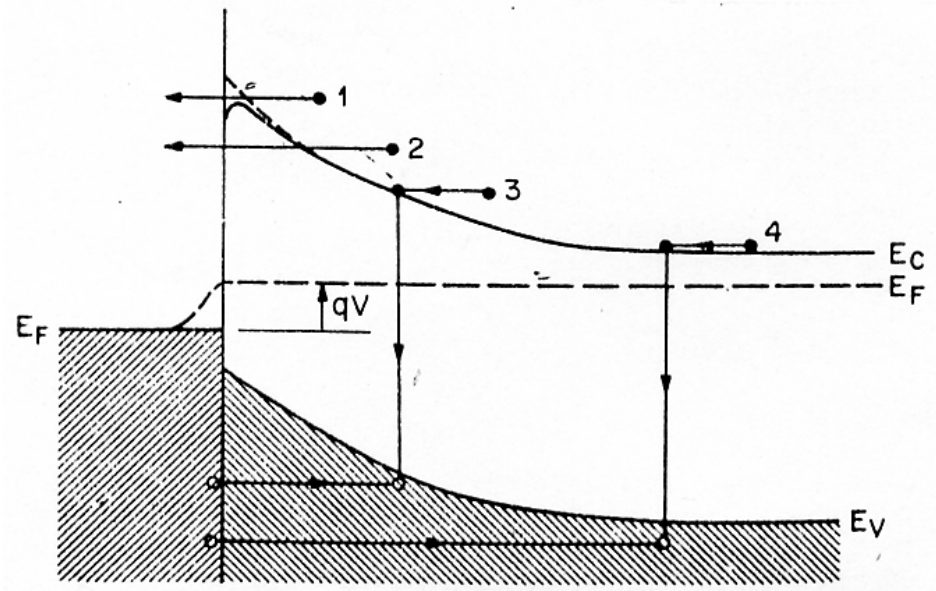
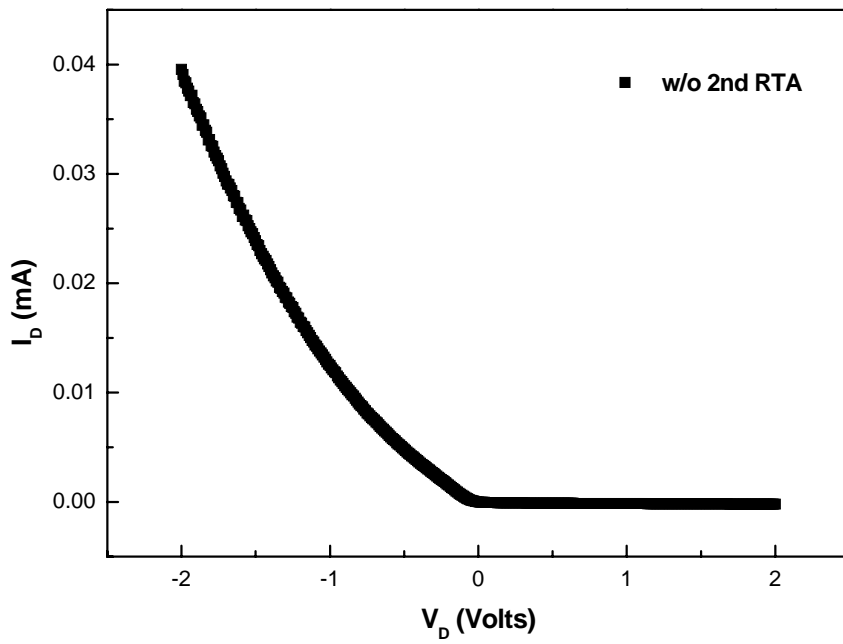
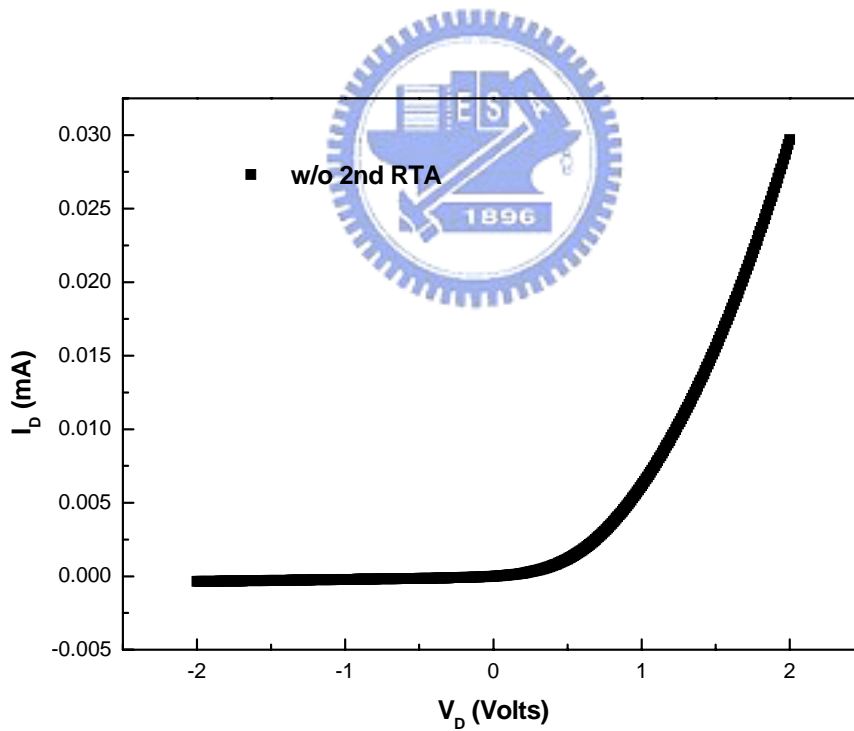


Fig. 3-4 Four basic transport process under forward bias. [1]



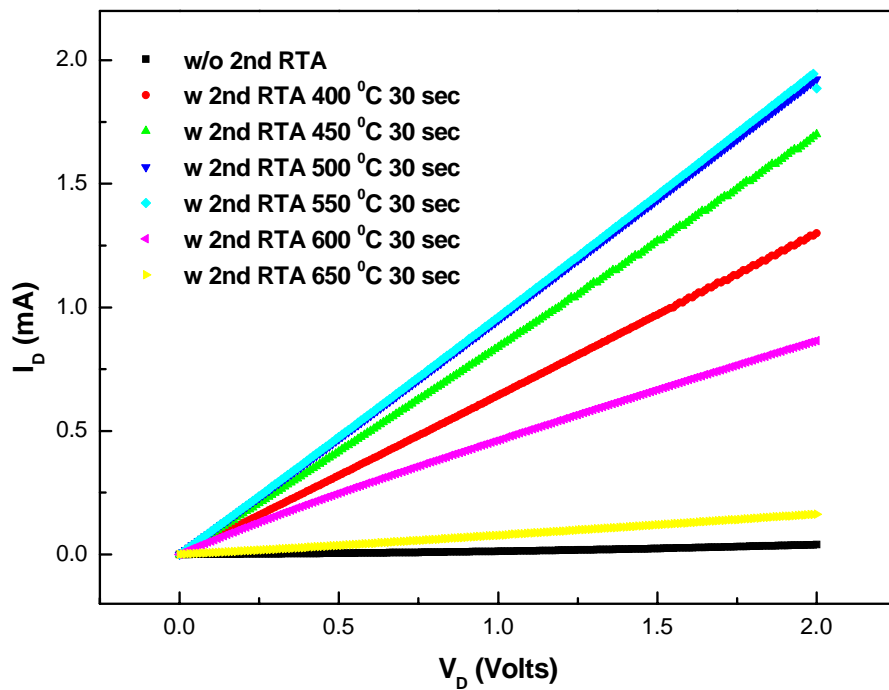


(a)

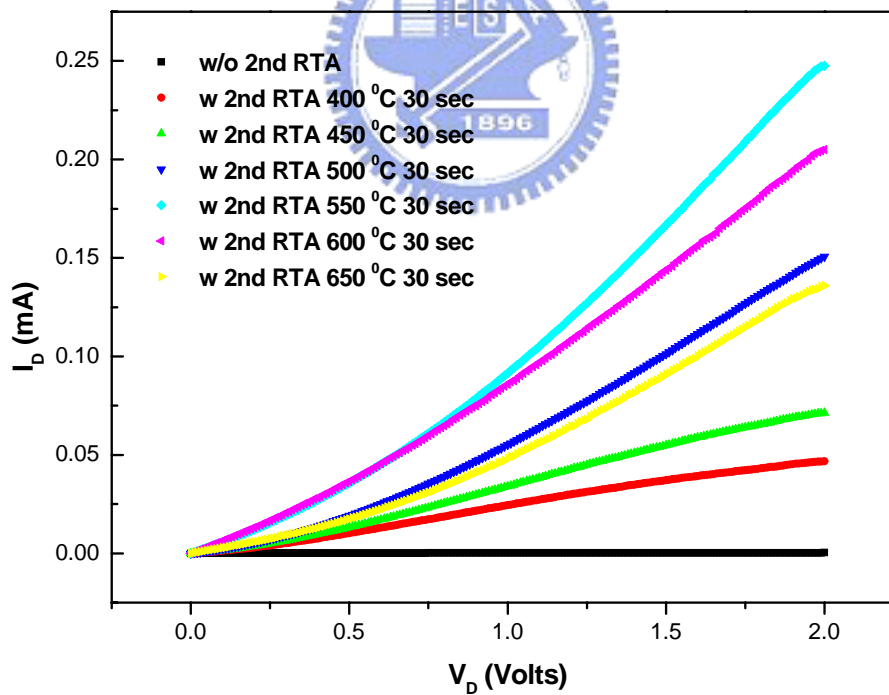


(b)

Fig. 3-5 The I_D - V_D characteristic curves of the NiSi/Si junction diode without 2nd RTA by (a) BF_2^+ implantation and (b) P^+ implantation.

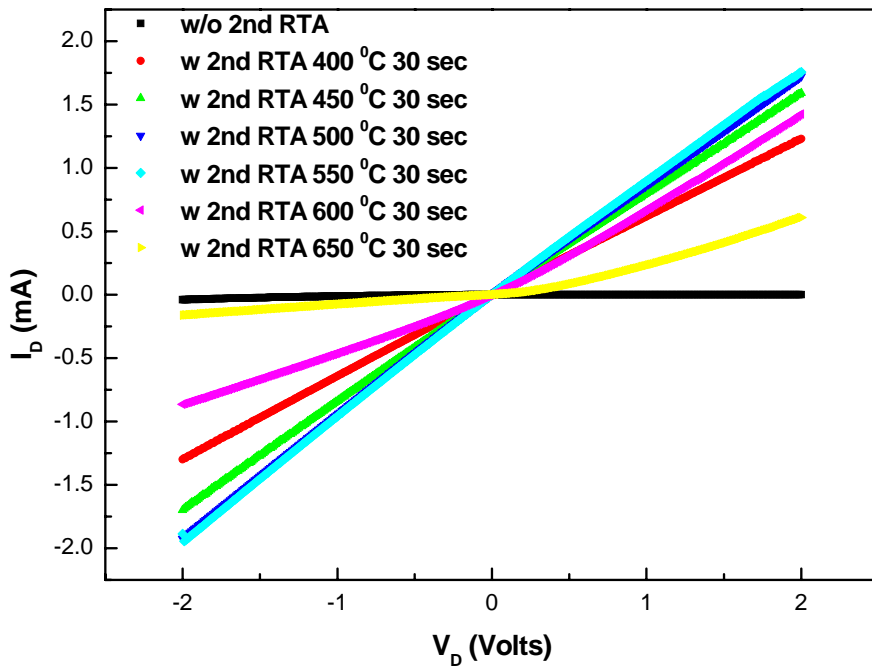


(a)

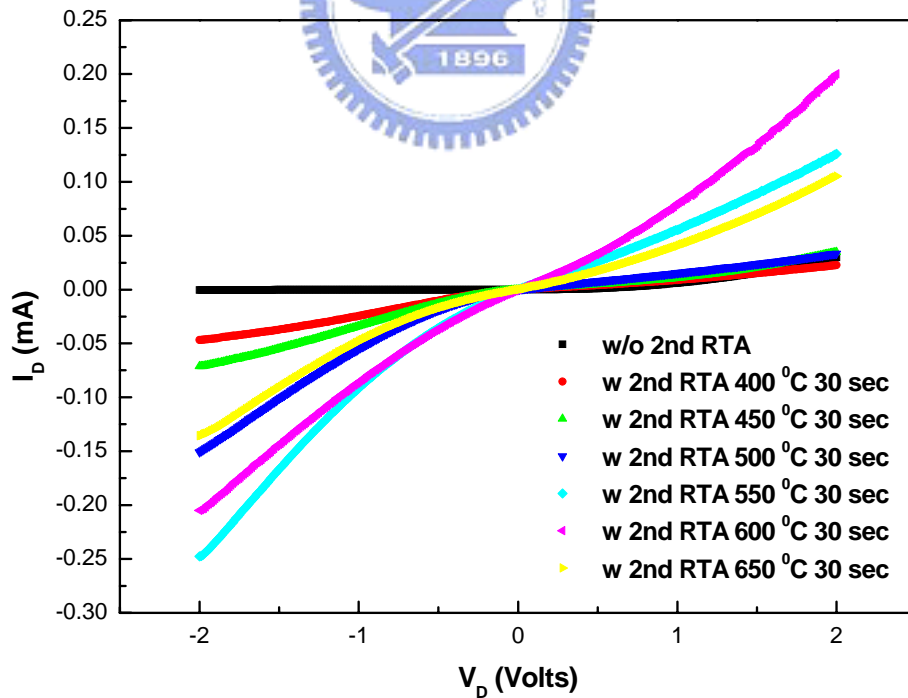


(b)

Fig. 3-6 The forward I_D - V_D characteristic curves of the NiSi/Si junction diode with 2nd RTA 30 sec by (a) BF_2^+ implantation and (b) P^+ implantation.

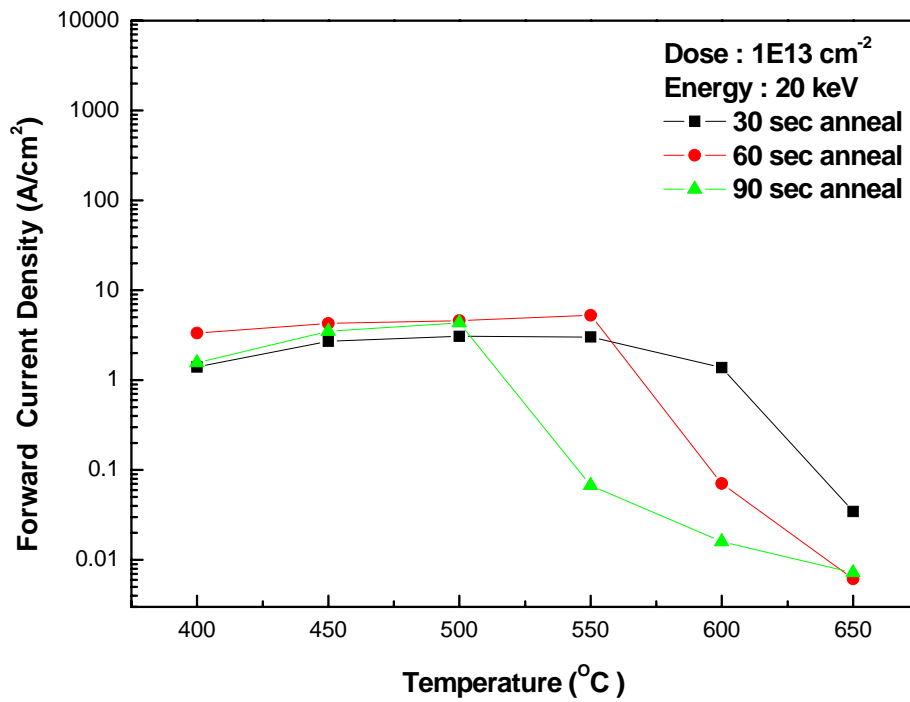


(a)

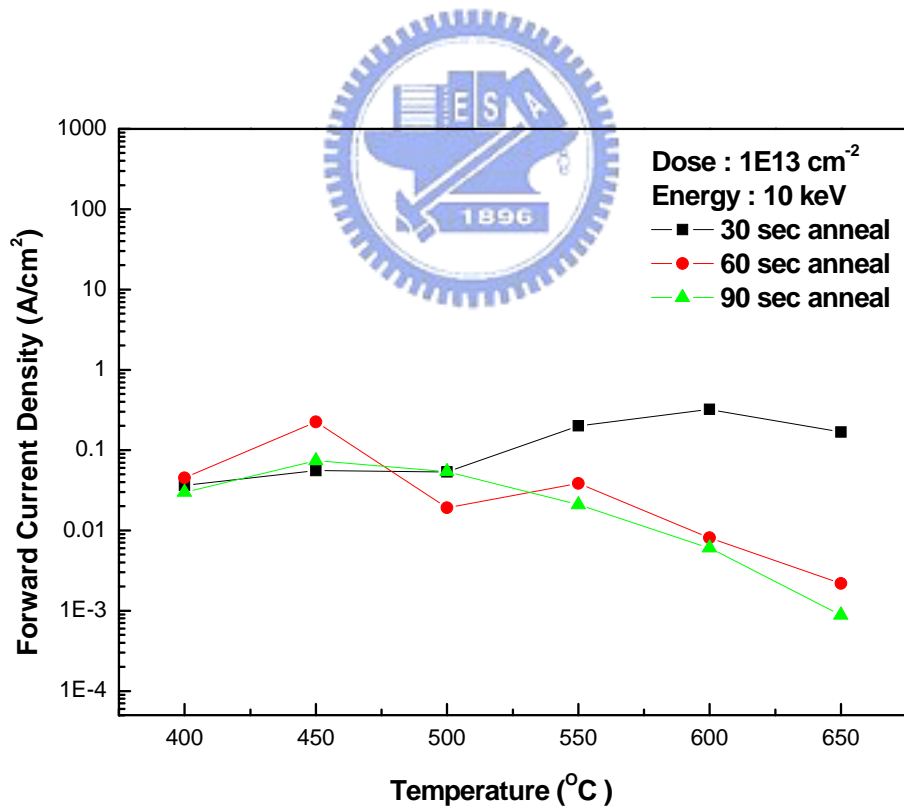


(b)

Fig. 3-7 The I_D - V_D characteristic curves of the NiSi/Si junction diode with 2nd RTA 30 sec by (a) BF_2^+ implantation and (b) P^+ implantation.

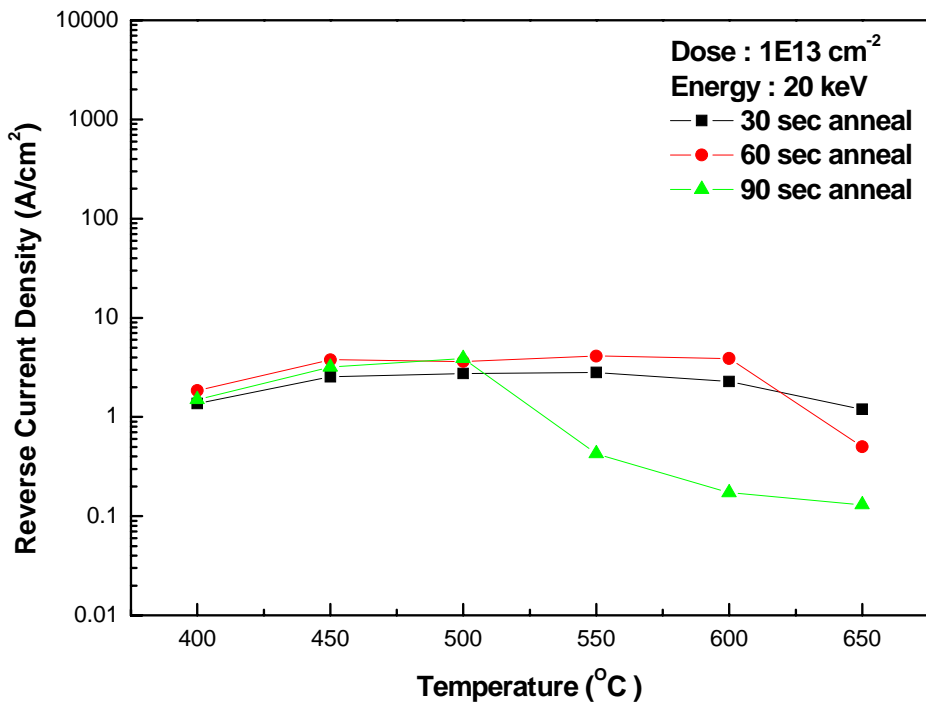


(a)

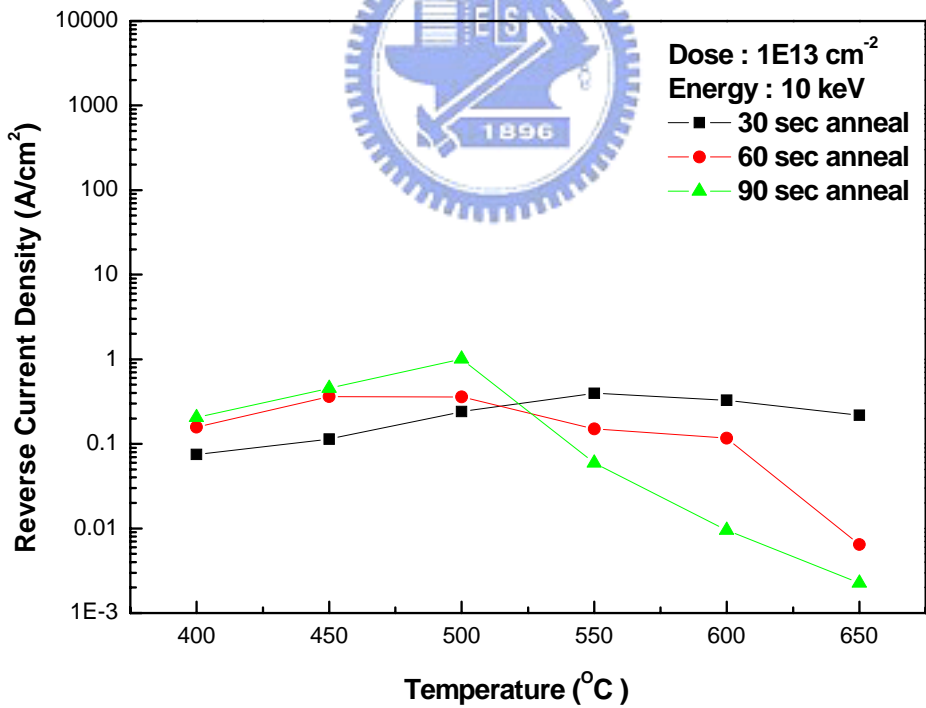


(b)

Fig. 3-8 The forward bias current density versus annealing temperature for the NiSi / Si junction diodes fabricated with (a) BF_2^+ and (b) P^+ implantation at various annealing time.



(a)



(b)

Fig. 3-9 The reverse bias current density versus annealing temperature for the NiSi / Si junction diodes fabricated with (a) BF_2^+ and (b) P^+ implantation at various annealing time.

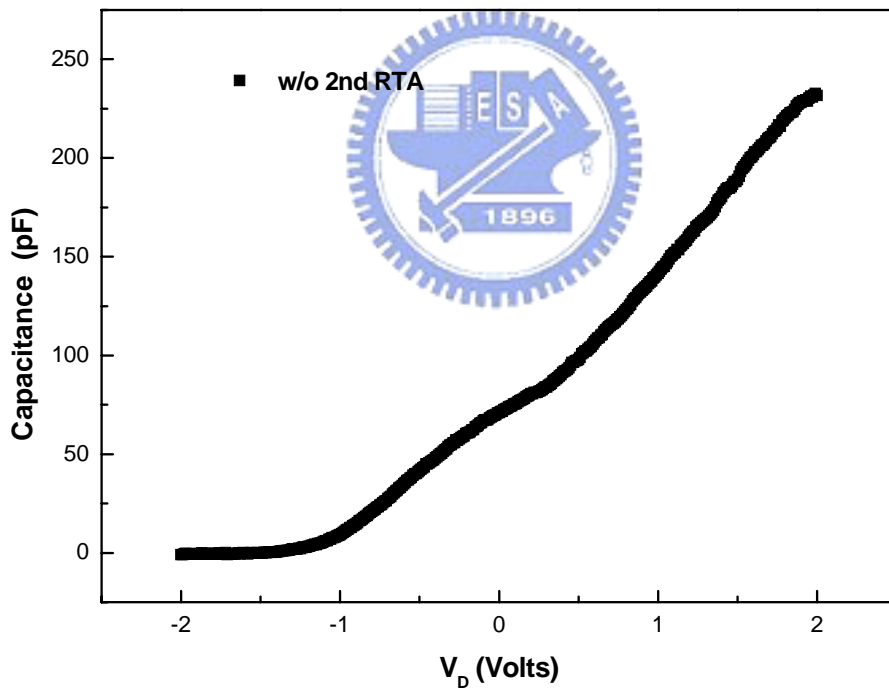
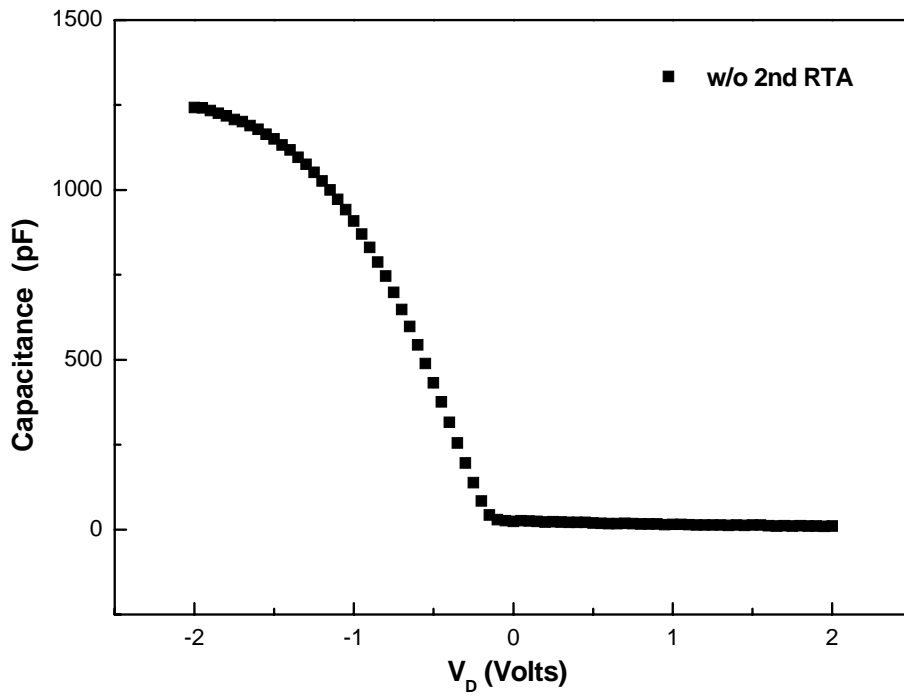
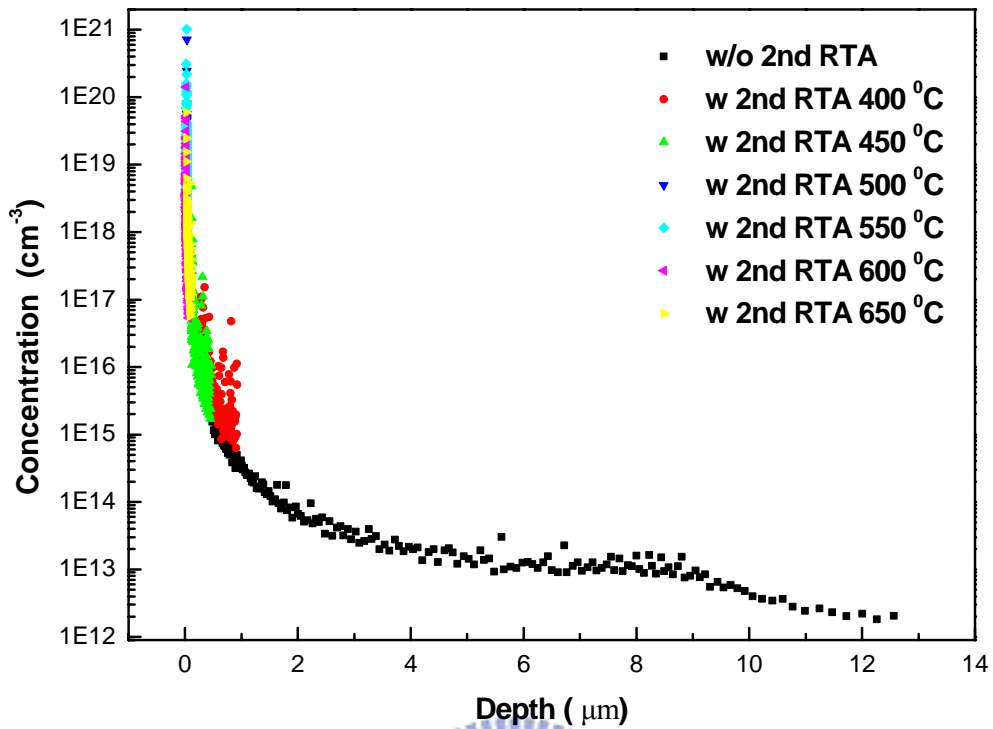
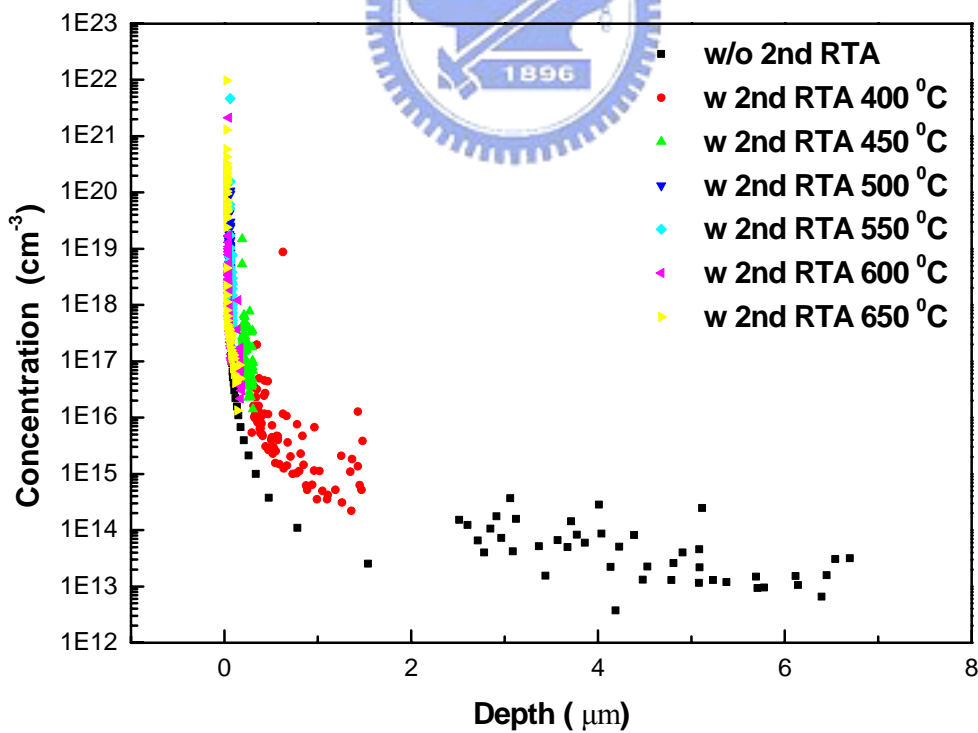


Fig. 3-10 The capacitance-voltage characteristics of Schottky junction diodes implanted (a) BF_2^+ and (b) P^+ without 2nd RTA.

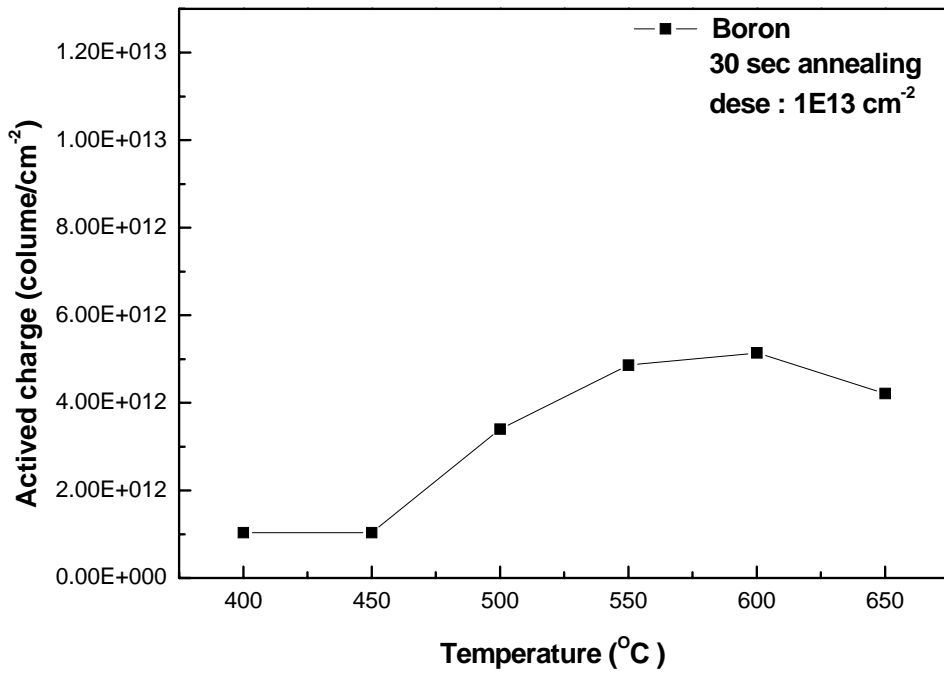


(a)

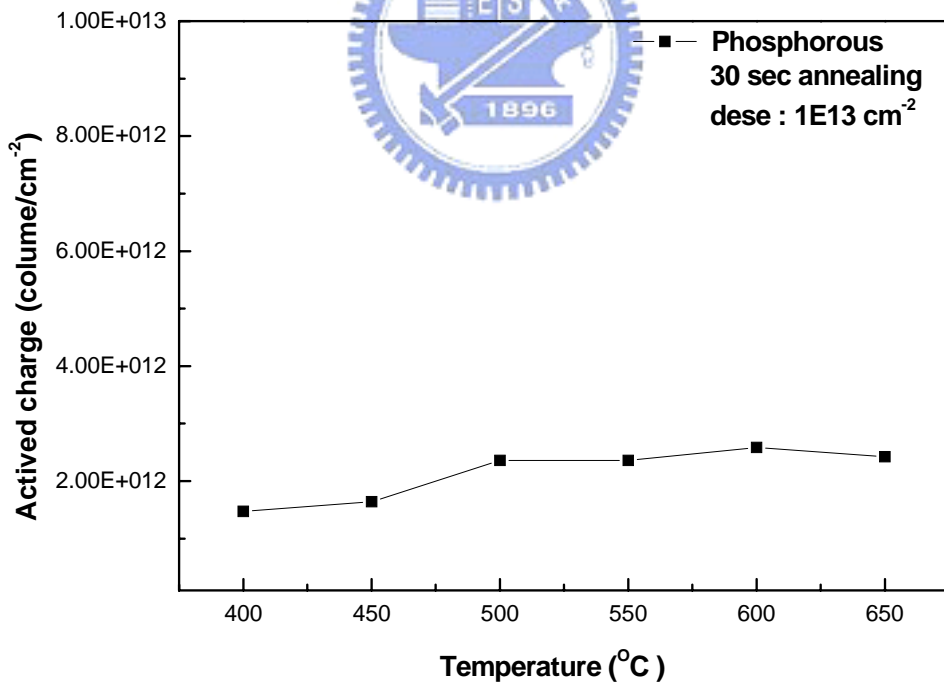


(b)

Fig. 3-11 The doping concentration versus depth for the implanted (a) BF_2^+ and (b) P^+ by annealing at various temperature.



(a)



(b)

Fig. 3-12 The Active charge versus anneals temperature for (a) Boron and (b) Phosphorous implant.

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(民國 93 年 9 月~民國 95 年 9 月)



碩士論文：形成矽化鎳時在矽化鎳與矽界面處離子活化相關研究

Research of Dopant Activation at the Interface between Nickel Silicide and Silicon
during Nickel Silicide Formation