國 立 交 通 大 學

電子工程學系　　電子研究所碩士班

碩 士 論 文

利用化學機械研磨技術製作新穎多晶矽薄膜電晶體結構及其電性模擬

The Fabrications and Simulations of a Novel Poly-Si TFT Structure Using CMP Technology

學生：楊國良　　Student: Guo-Liang Yang

指導教授：張國明 博士　　Advisor: Dr. Kow-Ming Chang

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中華民國九十五年七月

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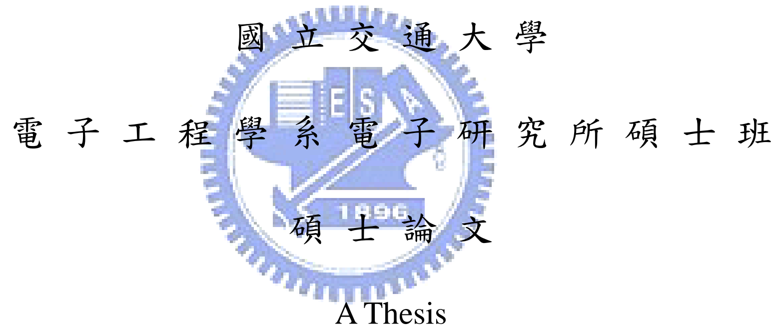

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摘要

本篇論文中，我們將探討和比較利用化學機械研磨技術所製作的新穎結構，此新穎結構具有加厚的汲/源極和一個薄通道。從模擬的結果來看，因爲較厚的源/汲極，在較厚的通道內的側向電場能被降低，所以漏電流可能會降低。而且成功的使漏電流下降了一個數量級。我們提供了一個使用化學機械研磨技術的新穎堆疊結構取代傳統的堆疊式結構，而且此製程能完全的與傳統四道製程相容。

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Abstract

In this thesis, the characteristics of the novel structure of poly-Si TFTs with thick S/D and thin channel by using CMP process have been investigated and compared. From the simulated results, the lateral electric field in the thicker channel near the drain region can be reduced with the thick S/D region, so the off-state current could be decreased. Moreover, we have succeeded to reduce the off-state current at least 1 orders. We proposed the novel staggered structure with CMP technology instead of conventional staggered structure, and the fabrication processes are fully compatible with the conventional four-mask ones. This structure may be an attractive device structure for future high-perform large-area device application.

誌謝

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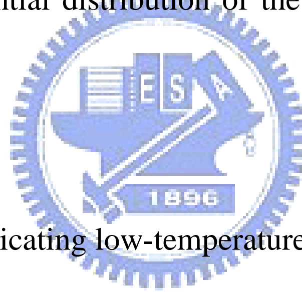

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Chapter 1
Introduction

1.1 Overview of Low Temperature Polycrystalline Silicon (LTPS) Thin-film Transistors (TFTs)

Polycrystalline Silicon (poly-Si) thin-film transistors (TFTs) fabricated at low temperature have attracted attention for high-density SRAMs [1][2], linear image sensors [3], photodetector amplifier [4], and nonvolatile memories [5] etc, especially peripheral driving circuits in AMLCDs [6]-[9].

Recrystallization technology is important for low temperature Poly-Si TFTs because of the grain size, grain boundary and intragranular defects [10], which influence the performance of Poly-Si TFTs. To achieve the bigger grain size, better performance and low temperature process, we have some useful recrystallization technologies: solid phase crystallization (SPC) [11], eximer laser annealing (ELA) [12]-[14], and metal-induced lateral crystallization (MILC) [15]-[17] etc. In this paper, we used SPC method to recrystallize the poly-Si TFTs.

In generally, poly-Si TFTs have two structures: top-gate coplanar structure and bottom-gate structure as shown in Figure 1-1. The top-gate TFTs are mainly used in AMLCD application because their self-aligned source/drain regions provide low parasitic capacitances and are suitable for device scaling down. On the other hand, Bottom-gate TFTs have better interface and higher plasma hydrogenation rate than top-gate TFTs, but they have lower current and need extra process steps for backside exposure and difficult fabrication.

The dominant leakage current mechanism in poly-Si TFTs is the field emission via the grain boundary traps by a high electric field near the drain [18]. Therefore, reducing the

lateral electric field near the drain junction is needed. For example, using a lightly doping drain (LDD) structure can reduced the lateral electric field [19][20]. The LDD structure certainly not only reduces the electric field but also enhances source/drain series resistance that limits the on-state current.

Besides LDD structure, many device structures are used to enhance poly-Si TFTs performance, such as offset gate [21][22], gate-overlapped LDD [23]-[25], multi-channel structure [26].

1.2 Issues in LTPS TFTs

Although we usually use the poly-Si TFTs instead of the amorphous TFTs for the high mobility, the poly-Si TFTs suffer from the high leakage current in the off-state operation and kink effect in the on-state operation. Besides, under the long-term operation, the stability of the poly-Si TFTs is a major issue. The hot carrier effect is also an important reliability in LTPS TFTs.

It is well known that there are three kinds of the leakage current mechanisms in poly-Si TFTs [27]. First, when the drain voltage is very low, the leakage current is governed by thermally generated carriers via trap states, which is denoted by G in Figure 1-2. Second, when the drain voltage is in the intermediate range, the leakage current is generated by the thermionic field emission of electrons indicated as T1 in Figure 1-2. In this case the electrons in the valence band are thermally excited to the trap states, and then tunnel to the conduction band quantum mechanically. The leakage current therefore increases with the gate voltage due to the narrowing of the barrier width. Third, when the gate voltage is high enough, the leakage current is governed by the field enhanced tunneling which is denoted by T2 and T1 in Figure 1-2. Obviously, decreasing the drain electric field is helpful to reducing the leakage current.

1.3 Motivations

The high off-state leakage current and the on-state kink effect are the influences on the properties of poly-Si TFTs, which even have higher on-state current than the amorphous Si TFTs. In this study, we used the Damascene process to form the thin channel with partially thicker region structure, which not only effectively reduces the drain electric field but also shows a low leakage current [28][29]. Besides, we also combine thick S/D and thin channel to achieve the purposes of low off-state current and drain electric field. In this process, an additional mask will not be required.

1.4 Thesis Organization

In chapter 1, a brief overview of LTPS TFT technology and related applications were introduced.

In chapter 2, the simulations of the novel LTPS TFTs, including the lateral electric field, the potential distribution, and the current flow, will be described.

In chapter 3, the fabrication process flow of the novel LTPS TFT device and experimental recipes will be presented.

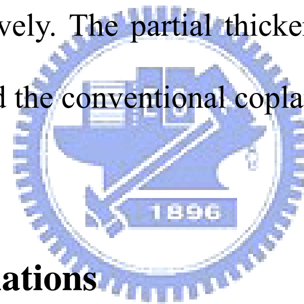
In chapter 4, we will show the electrical properties of the novel poly-Si TFT device, which contain transfer characterization and output characterization

Finally, conclusions and future work as well as suggestion for further research are given in chapter 5.

Chapter 2
Simulations of the Novel LTPS TFT's Structures

2.1 The Structures of Novel LTPS TFT's

In this thesis, we provide a new architecture, which combines thicker source/drain, thin channel and damascene-gate structure, and use MEDICI to simulate the structure. Figure 2-1 shows the structure of the proposed poly-Si TFTs. The thickness of the channel is 500 Å. Gate oxide thickness is also 500 Å. The thick source/drain has different thickness with 1000 Å, 2000 Å, and 3000 Å, respectively. The partial thicker channel thickness is the same as the source/darin. We also simulated the conventional coplanar structure with 500 Å channel layer.



2.2 The Results of Simulations

We primarily simulated the electric field in the on-state and off-state operation and the effects of electric fields to the current flow distribution. The sampling positions are shown in Figure 2-2. The line A is located below the thick source/drain surface 100 Å. The line B lies to the middle position between the surface of thick source/drain and the channel surface. The line C is under the channel surface 100 Å.

Figure 2-3 shows the simulated the lateral electric fields of a conventional TFT and the proposed TFTs in the off-state operation. Obviously, the electric field of the proposed TFT is lower than which of a conventional TFT. Figure 2-4 shows the potential distributions of the proposed TFTs and a conventional TFT to confirm the electric field. The results predict that

the leakage current can be reduced by lowering the lateral electric field near the drain region.

For example of the damascene-gated structure with 3000 Å Source/Drain, the reduction percent of the maximum lateral electric fields near the drain region are 17.84 %, 55.40 %, and 60.03 % at three sampling points, respectively, compared with the conventional ones. Moreover, the maximum lateral electric field near the drain region is reduced with increasing the source/drain thickness of the damascene-gated structure. The values and reduction percent of the maximum lateral electric fields near the drain region in off-state operation are shown in the Table I.

On the other hand, in the on-state operation, Figure 2-5 shows the simulated current flow. Obviously, the main current path is near the channel surface. It means that the primary influence on the on-state current is the surface lateral electric field near the drain region. The on-state electric field is shown in the Figure 2-6. Although the maximum lateral electric fields at the line B and C of proposed structure are higher than which of conventional structure, the on-state current is not affected remarkably. The lower lateral electric field at line A may result the on-state current reducing slightly, and it is expected to suppress the kink effect. Table II show the values and reduction percent of the maximum lateral electric fields near the drain region in on-state operation

In Figure 2-3 and 2-6, it is noted that larger the electric fields of proposed TFT from 11.5 nm to 12 nm along the channel direction result from the sampling line crossing the oxide layer.

2.3 Summary

It clearly shows that the lateral electric field near the drain region of the proposed TFT is lower than which of the conventional TFT. The simulated results show that the lateral electric

field near the drain region can be effectively reduced by the proposed structure, and it can be expected that the better performance of the proposed structures would be obtained.

Chapter 3

Experimental of the Novel Structure LTPS TFTs

3.1 The Fabrication Process Flow of Low Temperature Poly-Si TFTs

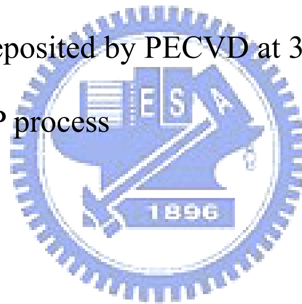
The poly-Si TFTs were fabricated on 6-inch-diameter p-type silicon wafer. Figure 3-1 shows the process flow of the proposed poly-Si TFTs. The undoped amorphous silicon (α-Si) film was initially deposited on 500 nm thermally oxide silicon (100) wafers by low temperature chemical vapor deposition (LPCVD) system with silane (SiH_4) gas at 620 ℃. The deposition pressure was 160 mtorr. Then the solid phase crystallization (SPC) process was carried out with 600 ℃, 24 hours. A 400 nm TEOS oxide film was deposited at 300 ℃ as passivation layer by PECVD. Then, the chemical-mechanical polishing (CMP) process was used to flat the surface of TEOS oxide. Gate regions were patterned by reactive ion etching and wet etching. The 50 nm-thick TEOS gate oxide was deposited by PECVD at 300 ℃, sequentially the 400 nm poly-Si film was formed by LPCVD at 620 ℃. Afterwards, CMP process polished the additional poly-Si to form the damascene gate. The passivation oxide layer was removed by the wet etching. Then the region of source, drain and gate were doped by a self-aligned phosphorus implantation. The dopants were activated at 600 ℃ in N_2 ambient for 24 hours. Next, a 300 nm TEOS oxide for a passivation layer was deposited by PECVD at 300 ℃, and the contact lithography was carried out. After opening the contact holes, a 500 nm Al was deposited by the thermal coater and the metal pad was patterned. Finally, the samples were sintered at 400 ℃ for 30 minutes in N_2 ambient. The main processes of fabrication are shown in Figure 3-1.

Figure 3-2 shows the conventional poly-Si TFTs to compare with the novel structure in the

same run.

The detail fabrication process flows are listed as follows.

1. (100) orientation Si wafer
2. Initial clean
3. Thermal wet oxidation at 980 ℃ to grow 500 nm thermal SiO_2 in furnace
4. α-Si (100 nm, 200 nm and 300 nm) film was deposited by LPCVD at 620 ℃ in SiH_4 gas
5. SPC was carried out with 600 ℃ for 24 hrs
6. Mask#1: define S/D
7. Poly-Si film was dry etched by poly-etcher system
8. 400 nm TEOS oxide was deposited by PECVD at 300 ℃
9. Flatting the surface by CMP process
10. Post clean
11. Mask#2: define gate
12. Oxide and poly-Si film were dry etched, poly-Si need to leave 50 nm as channel
13. Oxide was wet lateral etched
14. RCA clean
15. 50 nm TEOS gate dielectric deposition by PECVD at 300 ℃
16. 400 nm poly-Si gate was deposited by LPCVD at 620 ℃ in SiH_4 gas
17. CMP process to remove the additional poly-Si
18. Post clean
19. Passivation oxide layer were removed by wet etching
20. Ion implantation: P^{31}, 5×10^{15} cm^{-2}, 50 KeV (100 nm), 70 KeV (200 nm) ,100 KeV (300 nm)
21. Dopants activation in N_2 ambient at 600 ℃ for 24 hrs



22. Initial clean

23. 300 nm TEOS oxide film was deposited by PECVD at 300 ℃ for the passivation layer

24. Mask#3: open contact holes

25. Wet etching by B.O.E

26. 500 nm Al thermal evaporation

27. Mask#4: Al pads definition

28. Etching Al

29. Al sintering at 400 ℃ in N_2 ambient for 30 min

3.2 Methods of Device Parameter Extraction

Many methods have been proposed to extract the characteristic parameters of poly-Si TFT. In this section, the methods of parameter extraction used in this research are described.

3.2.1 Determination of Threshold Voltage (V_{th})

The threshold voltage V_{th} is an important MOSFET parameter required for the channel length-width and series resistance measurement. However, V_{th} is a voltage that is not uniquely defined. Various definitions exist and the reason for this can be found in the I_D - V_{GS} curve. One of the most common threshold voltage measurement techniques is the V_{GS} of drain current of (W/L) $\times$ 10^{-7} A at V_D = 5 V.

3.2.2 Determination of the On/off Current ratio

On/off current ratio is one of the most important parameters of poly-Si TFTs. The leakage current mechanism in poly-Si TFTs is different from MOSFET. In MOSFET, the channel is composed of single-crystalline silicon and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel layer region. However, in poly-Si TFTs, the channel is composed of polycrystalline silicon. A large amount of trap densities in grain boundary attribute a lot of defect states in energy band gap to enhance the tunneling effect. Therefore, the leakage current due to the tunneling effect is much larger in poly-Si TFTs than in single-crystalline devices. When the voltage drops increase, the band gap width decrease and the tunneling effect becomes worse. Normally, we can observe this effect in typical poly-Si TFT I_D-V_G characteristics where the magnitude of leakage current will reach a minimum and then increase as the gate voltage decrease/increase for n/p-channel TFTs.

There are a lot of ways to specify the on and off current. In this thesis, the on current is defined as the drain current when gate voltage equal to 30 V and drain voltage is 5 V. The off current is specified as the minimum leakage current in linear operation mode for usual cases.

$$\text{on / off current ratio} = \frac{I_{on}}{I_{min}} = \frac{\text{Maximum current of } I_{DS} - V_{GS} \text{ plot at } V_{DS} = 5V}{\text{Minimum current of } I_{DS} - V_{GS} \text{ plot at } V_{DS} = 5V} \qquad \text{(Eq. 3.1)}$$

Chapter 4
The Characteristics of the Novel Damascene-gated Low-temperature Poly-Si TFTs with Staggered Source/Drain Regions

In this chapter, we will discuss the device performances of our novel structure of the poly-Si TFTs, and also compare with the conventional TFTs. We measured the thickness of the films by n&k analyzer, and the I-V characteristics of poly-Si TFTs by HP4156 semiconductor parameter analyzer.

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4.1 The Characteristics of the Novel Damascene-gated Low-temperature Poly-Si TFTs with Staggered Source/Drain compared with the Conventional TFTs

Figure 4-1 ~ Figure 4-8 show the I_{DS} – V_{GS} transfer characteristics of the proposed structure compared with conventional structure. In the negative gate voltage, the leakage current of the proposed structures are lower than which of the conventional structure. In the chapter 2, we have simulated that the lateral electric field near the drain region of the proposed structure is lower than that of the conventional structure, which can suppress the leakage current. On the other hand, the proposed structures have a slightly lower on-state current because of the lower lateral electric field in on-state operation, but the on/off current ratio is affected lightly.

Figure 4-9 ~ Figure 4-12 show the measured $I_{DS} - V_{DS}$ output characteristics of the proposed TFTs and the conventional ones. In the theory, the lower lateral electric field near the drain region is considered that can suppress the kink effect. However, the kink effect is not suppressed obviously at high driving voltage. It is considered that there are too many grain boundary traps with the increase of the thickness of the S/D region, and the reduction of the lateral electric field near the drain region is limited.

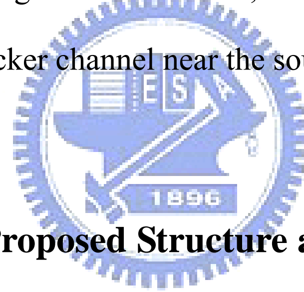
4.2 Comparisons of the Leakage Current in Off-State Operation and the On/Off Current Ratio

The leakage current in off-state (I_{leak}) is defined as the drain current (I_{DS}) at the negative voltage (V_{GS} = -15 V). For the proposed structure with W/L = 10 μm/5 μm in Figure 4-3, the leakage current (I_{leak}) of the proposed structures with 100-nm, 200-nm, 300-nm source/drain thickness decreased 0.71, 1.23 and 1.36 order of magnitude, respectively. In the other sizes, the leakage currents of the proposed structure with 300-nm source/drain thickness are all decreased over one order of magnitude at least.

On the other hand, the minimum leakage current (I_{min}) of the proposed structures are slightly increased than that of the conventional structure. This is because the proposed structure has more grain boundary traps in the channel near the thicker source/drain region. The on/off current ratio of the conventional structure, and the proposed structures of W/L = 10 μm/5 μm with 100-nm, 200-nm, 300-nm source/drain thickness are 1.58×10^7, 1.14×10^7, 1.38×10^7, and 1.24×10^7, respectively. Table III lists the on-state currents (I_{on}), the minimum leakage current (I_{min}), on/off current ratio (I_{on}/I_{min}), and off-state currents (I_{leak}) of the conventional and three kinds of proposed structures with different dimensions.

4.3 The Output Characteristics of the Proposed Structures Compared with the Conventional Structure

As shown in Figure 4-9 ~ Figure 4-12, the kink effect of the proposed structures is considered to be suppressed due to the lower electric field near the drain region. At the low driving voltage ($|V_{GS} - V_{th}| = 10$ V), the kink current of the proposed structure is much smaller than that of the conventional structure with W/L = 10 μm/5 μm and W/L = 5 μm/5 μm. As the driving voltage increasing, the kink effect becomes more significant. Although the lateral electric field near the drain region is decreased, it maybe due to large amount of grain boundary traps exists in the thicker channel near the source/drain region.



4.4 Comparison of the Proposed Structure and the Conventional Staggered Structure with Five Masks

Figure 4-13 shows the transfer characteristics of the proposed TFT and the conventional TFT with staggered source and drain region. It clearly presents that the curve of the proposed structure is almost the same with that of the conventional structure with staggered source and drain region (five masks). Therefore, we proposed a new fabrication with CMP process technology instead of an additional lithography step, and more simple than the conventional five-mask steps staggered source/drain structure.

Chapter 5
Conclusions and future work

5.1 Conclusions

In this thesis, a novel low-temperature poly-Si TFT with a thicker source/drain region and thin channel by using CMP process was proposed and investigated. Although, in our proposed structure, more grain boundary traps existed in the thicker channel region and lower lateral electric field would cause the on/off current ratio slightly decreasing, lower lateral electric field would substantially reduce the leakage current in off-state operation. Moreover, the fabrication processes of the proposed structure are simple and no additional mask step is needed. We proposed the novel staggered structure with CMP technology instead of conventional staggered structure, and the fabrication processes are fully compatible with the conventional four-mask ones. This structure may be an attractive device structure for future high-perform large-area device application.

5.2 Future work

We have proposed a damascene-gated low-temperature poly-Si TFTs with a thicker source/drain region and thin channel to improve the conventional low-temperature poly-Si TFTs performance. However, in order to further improve device electrical characteristics and apply to glass substrates, there will be still some works worth of being investigated.

In this experiment, the kink effect of the proposed structures was not significantly

suppressed due to large number of the grain boundary traps near the drain region existence. It is well known that NH_3 or H_2 plasma could significantly reduce the grain boundary traps due to the formation of S≡N and S-H bonds [30]. Moreover, recrystallization is also an important technology. SPC process obtains the small grain size. Using laser annealing can enlarge the grain size, and further decreasing the grain boundary traps.

In the simulation, there are only three kinds of the thickness of the source/drain region. We can simulate more different thickness of the source/drain region to optimize. Moreover, changing the location of the sampling line to study the variation of lateral electrical field which mainly affects the simulated spread current is need to be investigated. Besides, the change of the lateral electrical field by varying the thickness of the sidewall oxide is also an attractive topic.

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Table I

Off-state operation	Conventional structure	Damascene-gated 100 nm A	Damascene-gated 100 nm B	Damascene-gated 100 nm C
the maximum lateral electric field (MV/cm)	2.13	1.83	1.51	1.38
reduction percent	0	14.08 %	29.11 %	35.21 %

Off-state operation	Conventional structure	Damascene-gated 200 nm A	Damascene-gated 200 nm B	Damascene-gated 200 nm C
the maximum lateral electric field (MV/cm)	2.13	1.76	1.07	1.11
reduction percent	0	17.37 %	49.77 %	47.89 %

Off-state operation	Conventional structure	Damascene-gated 300 nm A	Damascene-gated 300 nm B	Damascene-gated 300 nm C
the maximum lateral electric field (MV/cm)	2.13	1.83	1.51	1.38
reduction percent	0	17.84 %	55.40 %	60.03 %

Table I. The simulated maximum lateral electric field near the drain region of the conventional and the damascene-gated TFTs at the three sampling points. The maximum was simulated at $V_{GS} = 0$ V and $V_{DS} = 20$ V

Table II

On-state operation	Conventional structure	Damascene-gated 100 nm A	Damascene-gated 100 nm B	Damascene-gated 100 nm C
the maximum lateral electric field (MV/cm)	0.110	0.083	0.120	0.261
reduction percent	0	25.45 %		

On-state operation	Conventional structure	Damascene-gated 200 nm A	Damascene-gated 200 nm B	Damascene-gated 200 nm C
the maximum lateral electric field (MV/cm)	0.110	0.082	0.094	0.272
reduction percent	0	25.45 %	15.45 %	

On-state operation	Conventional structure	Damascene-gated 300 nm A	Damascene-gated 300 nm B	Damascene-gated 300 nm C
the maximum lateral electric field (MV/cm)	0.110	0.082	0.093	0.258
reduction percent	0	25.45 %	15.45 %	

Table II. The simulated maximum lateral electric field near the drain region of the conventional and the damascene-gated TFTs at the three sampling points. The maximum was simulated at V_{GS} = 30 V and V_{DS} = 20 V

Table III

W/L = 5 μm/5 μm	Conventional structure	Damascene-gated 100 nm	Damascene-gated 200 nm	Damascene-gated 300 nm
I_{on} (A)	6.63×10^{-5}	5.35×10^{-5}	7.48×10^{-5}	6.5×10^{-5}
I_{min} (A)	4.29×10^{-12}	5.99×10^{-12}	5.63×10^{-12}	7.35×10^{-12}
on/off current ratio	1.55×10^{7}	8.93×10^{6}	1.13×10^{7}	8.84×10^{6}
I_{leak} (A)	4.28×10^{-8}	2.23×10^{-8}	1.62×10^{-8}	8.01×10^{-9}
I_{leak} Reduction magnitude		0.28	0.42	0.73

W/L = 10 μm/5 μm	Conventional structure	Damascene-gated 100 nm	Damascene-gated 200 nm	Damascene-gated 300 nm
I_{on} (A)	1.40×10^{-4}	1.18×10^{-4}	1.53×10^{-4}	1.34×10^{-4}
I_{min} (A)	8.87×10^{-12}	1.04×10^{-11}	1.11×10^{-11}	1.08×10^{-11}
on/off current ratio	1.58×10^{7}	1.14×10^{7}	1.38×10^{7}	1.24×10^{7}
I_{leak} (A)	1.90×10^{-7}	3.71×10^{-8}	1.11×10^{-8}	1.24×10^{-8}
I_{leak} Reduction magnitude		0.71	1.23	1.36

W/L = 5 μm/15 μm	Conventional structure	Damascene-gated 100 nm	Damascene-gated 200 nm	Damascene-gated 300 nm
I_{on} (A)	3.53×10^{-5}	2.37×10^{-5}	2.7×10^{-5}	2.54×10^{-5}
I_{min} (A)	2.4×10^{-12}	2.61×10^{-12}	2.59×10^{-12}	3.13×10^{-12}
on/off current ratio	1.47×10^{7}	9.08×10^{6}	1.04×10^{7}	8.12×10^{6}
I_{leak} (A)	7.42×10^{-8}	3.37×10^{-8}	6.16×10^{-9}	7.63×10^{-9}
I_{leak} Reduction magnitude		0.34	1.08	0.99

W/L = 10 μm/5 μm	Conventional structure	Damascene-gated 100 nm	Damascene-gated 200 nm	Damascene-gated 300 nm
I_{on} (A)	5.36×10^{-5}	3.97×10^{-5}	4.99×10^{-5}	4.83×10^{-5}
I_{min} (A)	3.96×10^{-12}	4.70×10^{-12}	4.92×10^{-12}	5.67×10^{-12}
on/off current ratio	1.35×10^{7}	8.45×10^{6}	1.01×10^{7}	8.52×10^{6}
I_{leak} (A)	8.81×10^{-8}	7.87×10^{-8}	4.69×10^{-8}	8.81×10^{-9}
I_{leak} Reduction magnitude		0.05	0.27	1

Table III. The characteristics of the drain current in $I_{DS} - V_{GS}$ plot of the conventional and proposed TFTs with different size at V_{DS}= 5 V

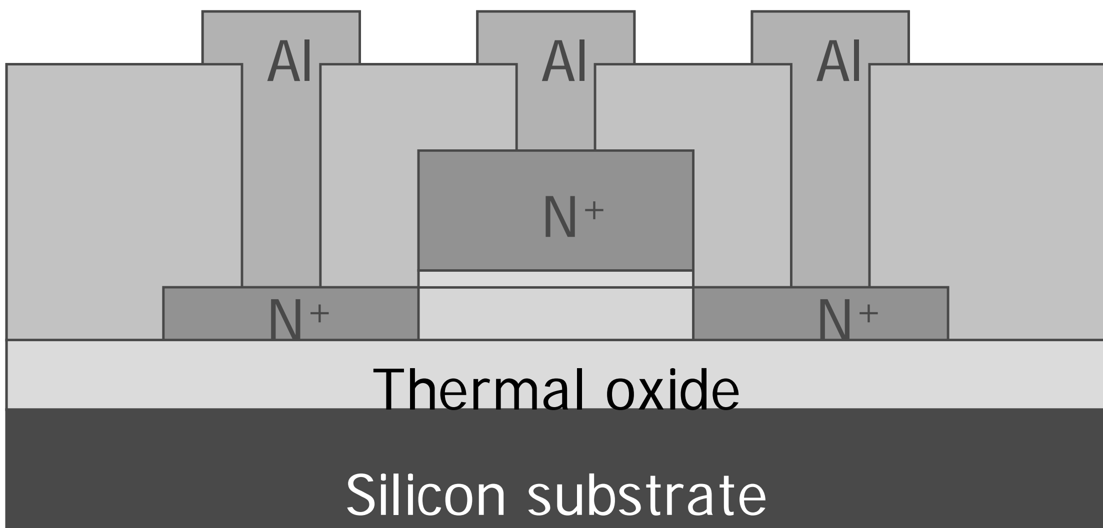

Fig. 1-1(a) The top-gate coplanar TFT

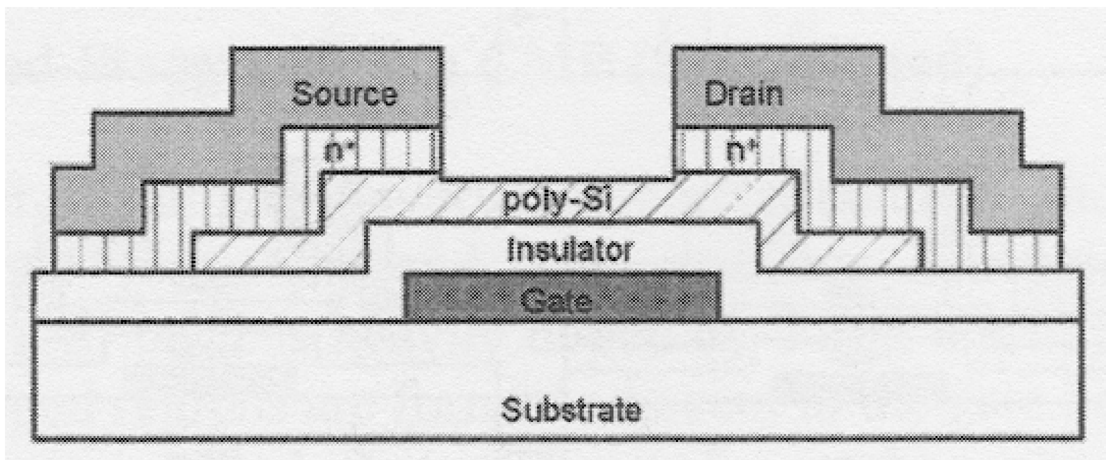

Fig. 1-1(b) The bottom-gate TFT

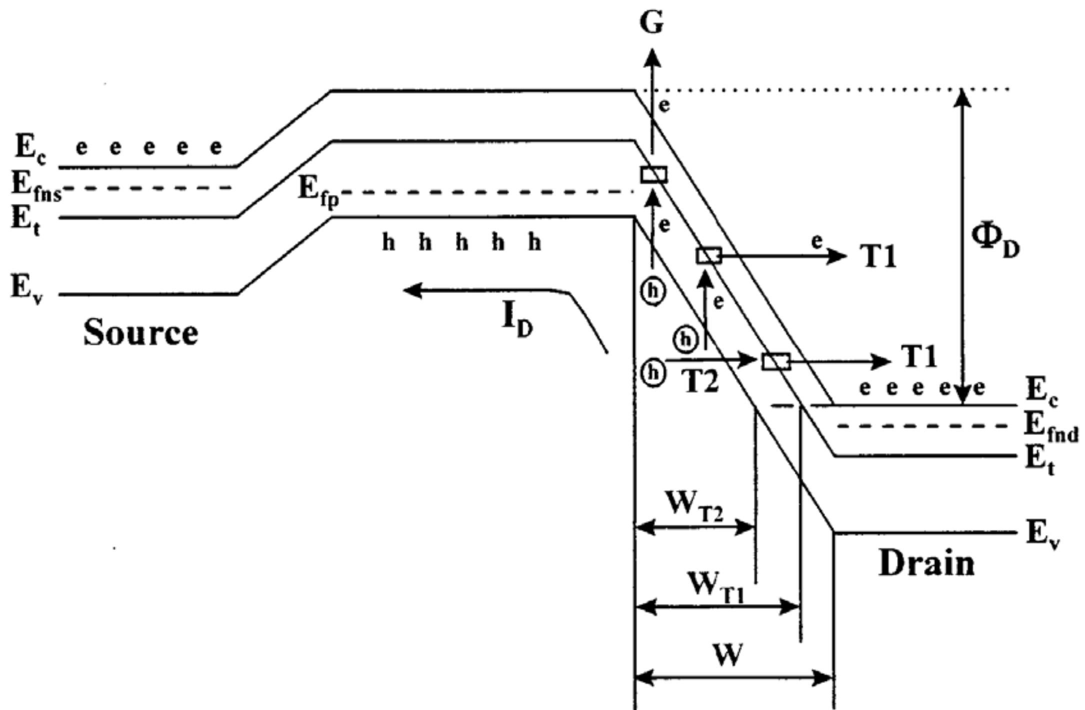

Fig. 1-2 The basic structure of an n-channel poly-Si TFT and its band diagram with the three kinds of leakage current mechanisms. G: The generation current, T1: the thermionic field emission current, T2: the field emission current, E_{fns}: quasi-Fermi level of electron at the source, E_{fp} : quasi-Fermi level of hole, E_{fnd} : quasi-Fermi level of electron at the drain.

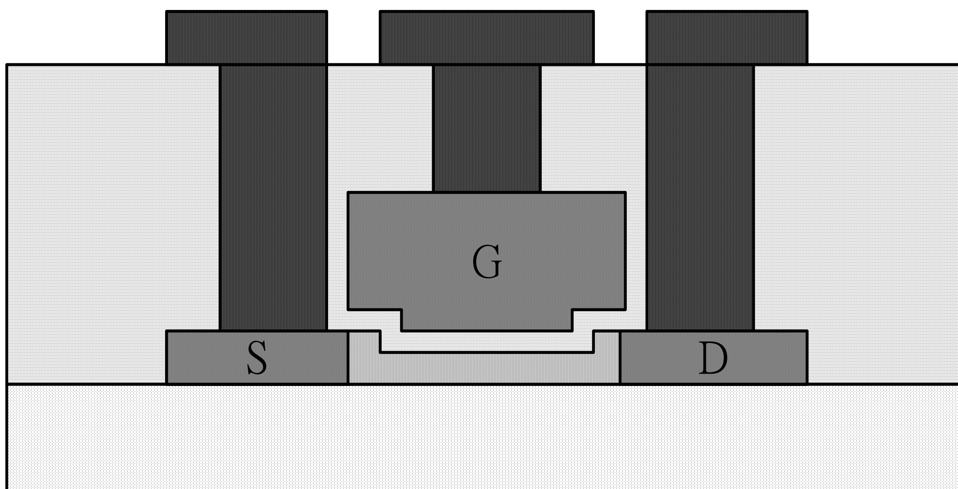

Fig. 2-1 The simulated proposed structure

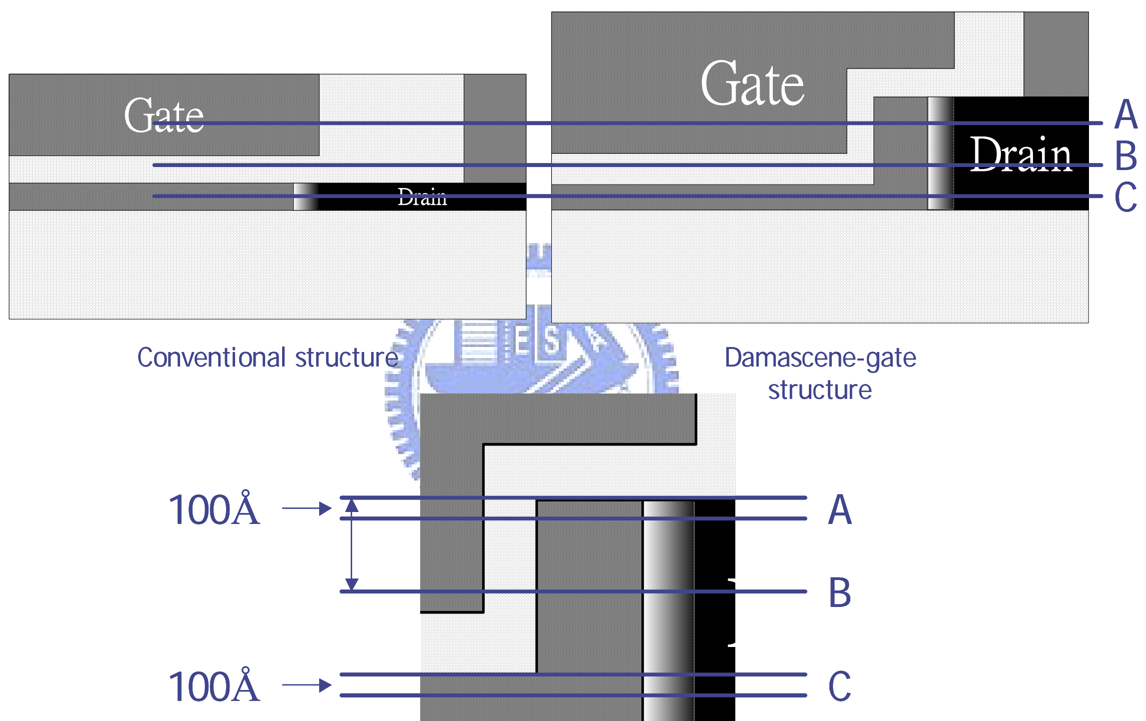

Fig. 2-2 The sampling positions of the damascene-gated and conventional structures

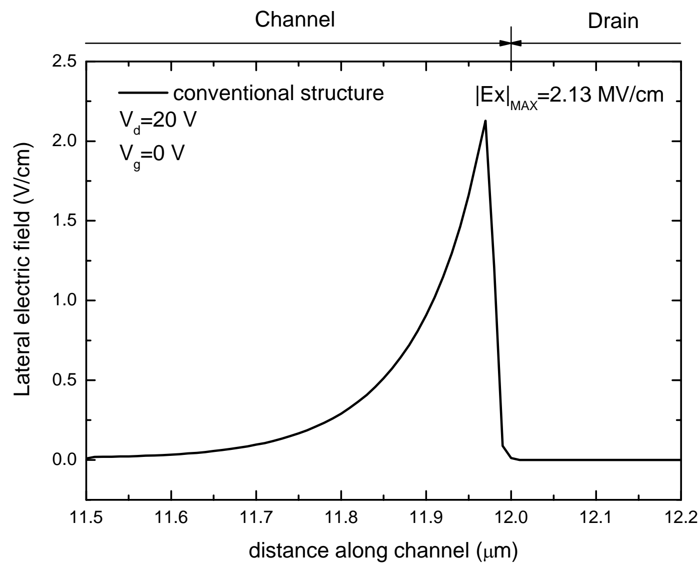

Fig. 2-3(a) The simulated lateral electric field of the conventional structure in off-sate operation

1896

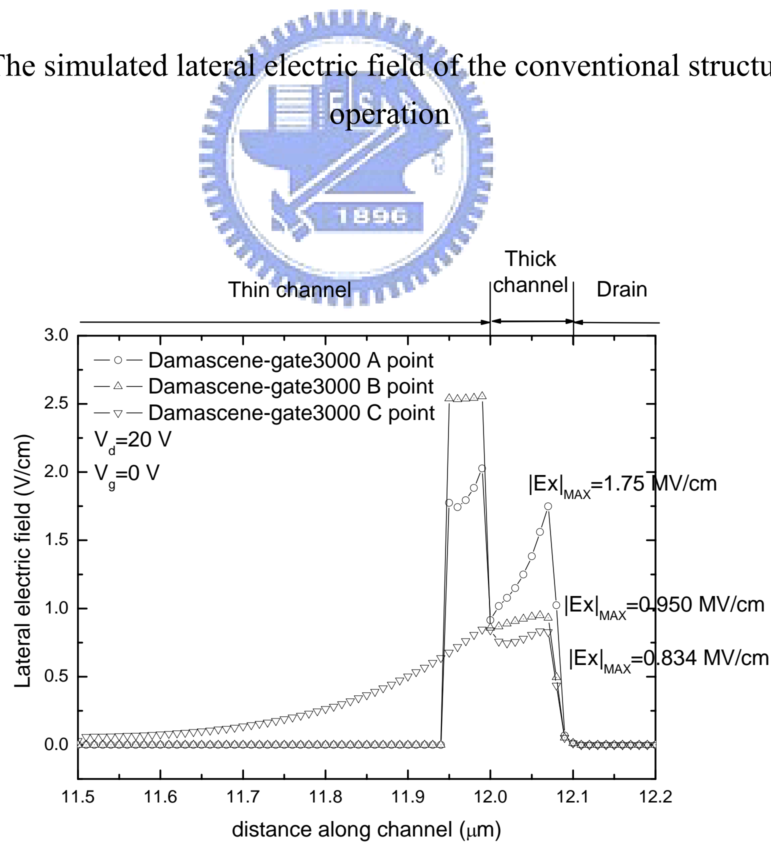

Fig. 2-3(b) The simulated lateral electric field of the 300 nm damascene-gated structure in off-sate operation

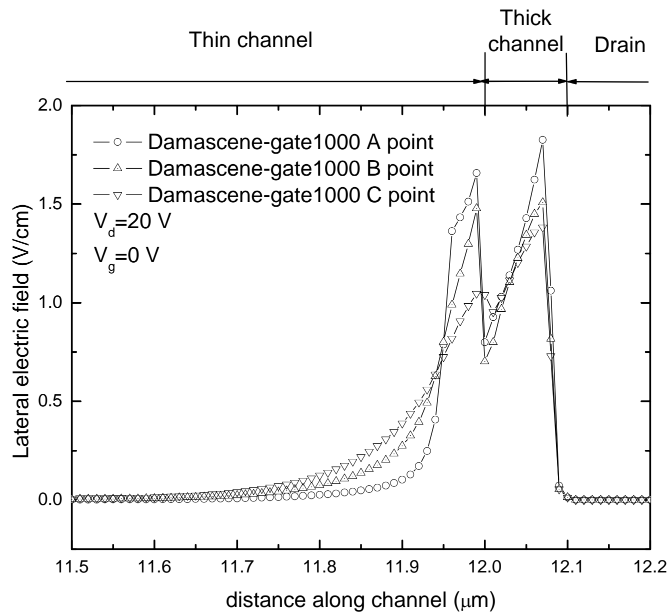

Fig. 2-3(c) The simulated lateral electric field of the 100 nm damascene-gated structure in off-sate operation

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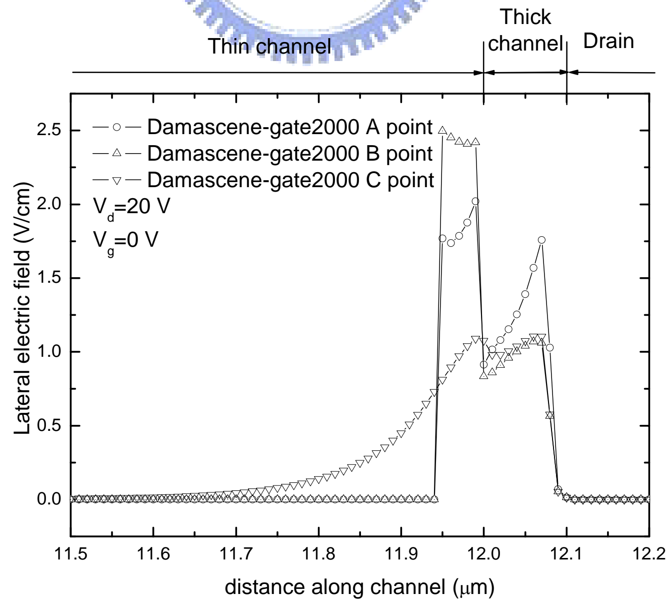


Fig. 2-3(d) The simulated lateral electric field of the 200 nm damascene-gated structure in off-sate operation

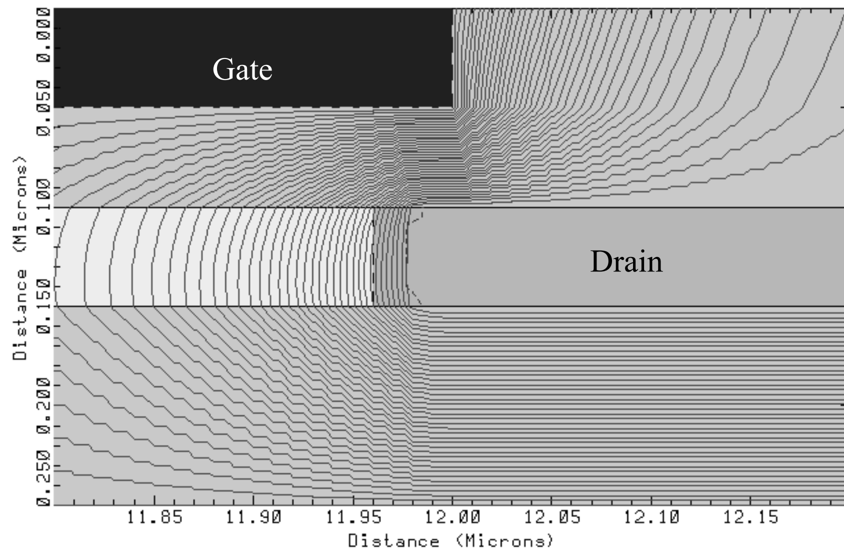
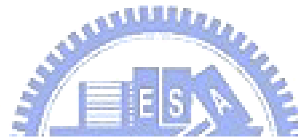


Fig. 2-4(a) The simulated potential distribution of the conventional structure in off-sate operation



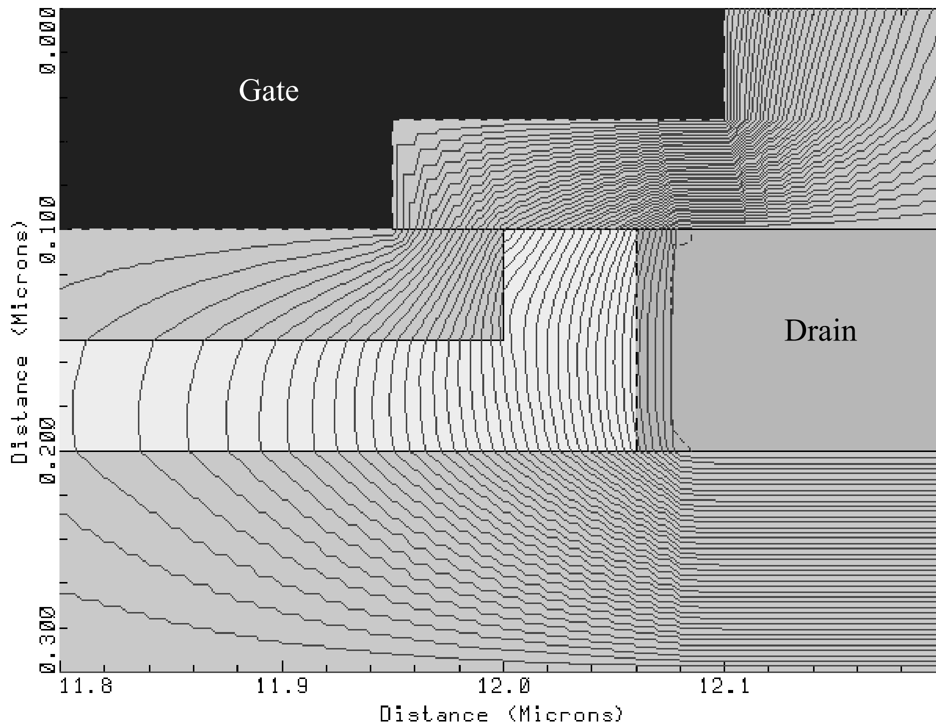


Fig. 2-4(b) The simulated potential distribution of the 100 nm damascene-gated structure in off-sate operation

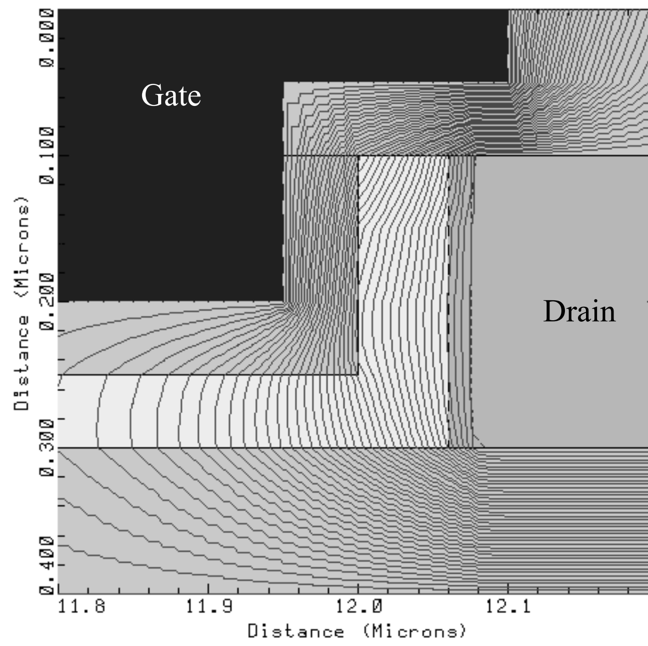


Fig. 2-4(c) The simulated potential distribution of the 200 nm damascene-gated structure in off-sate operation

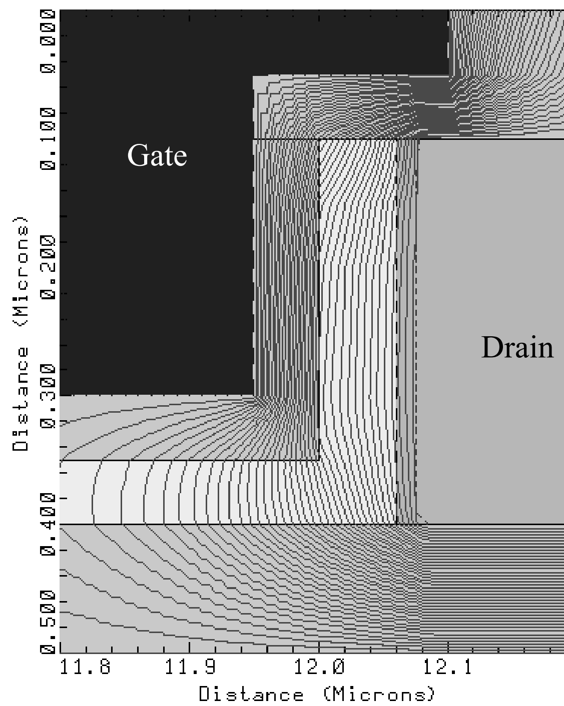


Fig. 2-4(d) The simulated potential distribution of the 300 nm damascene-gated structure in off-sate operation

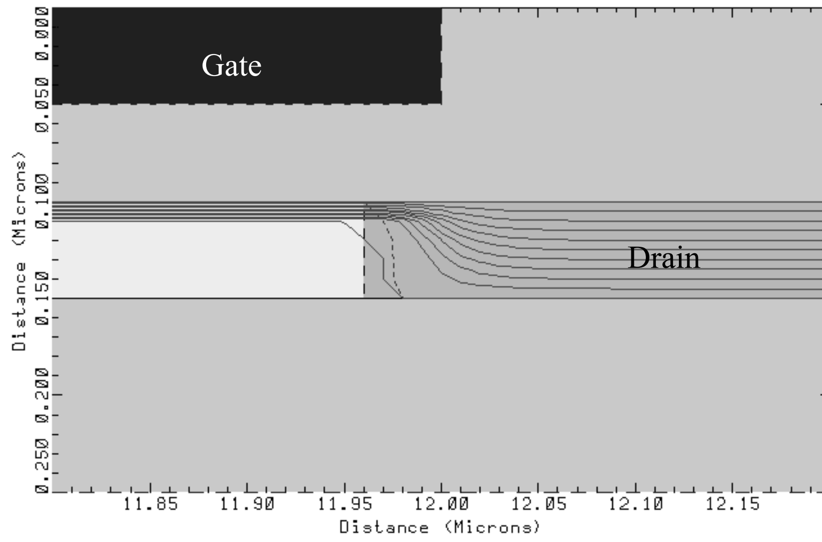


Fig. 2-5(a) The simulated current flow of the conventional structure in off-sate operation

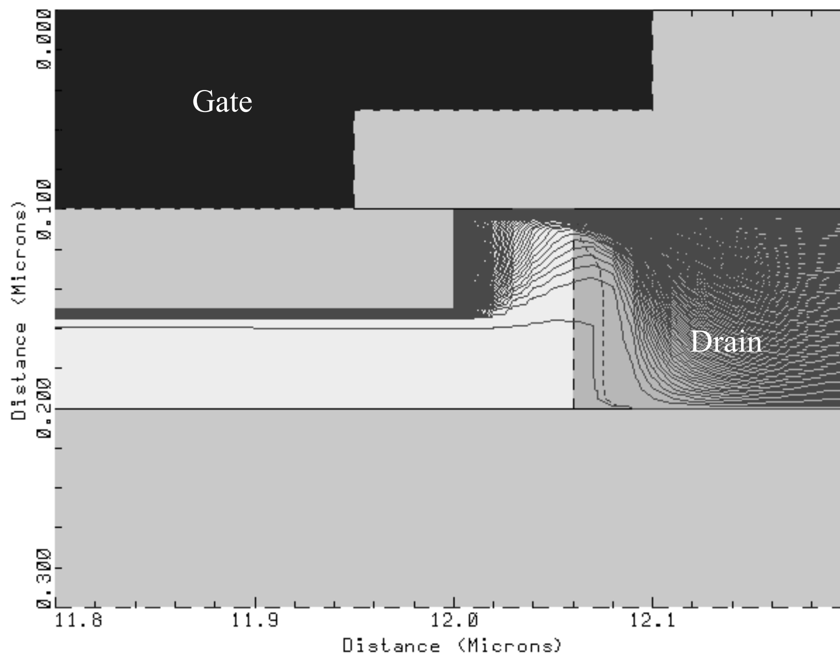


Fig. 2-5(b) The simulated current flow of the 100 nm damascene-gated structure in off-sate operation

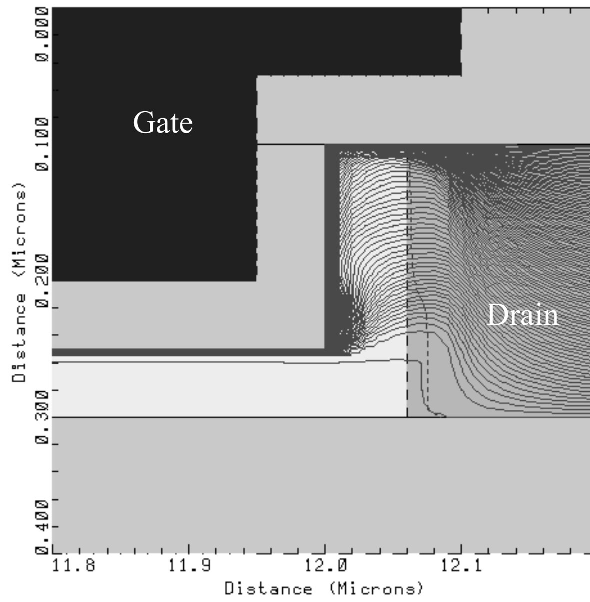


Fig. 2-5(c) The simulated current flow of the 200 nm damascene-gated structure in off-sate operation

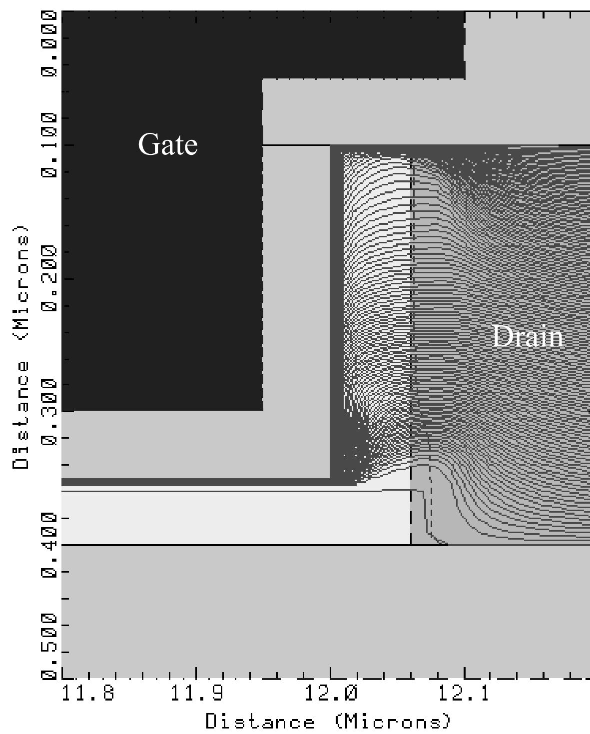


Fig. 2-5(d) The simulated current flow of the 300 nm damascene-gated structure in off-sate operation

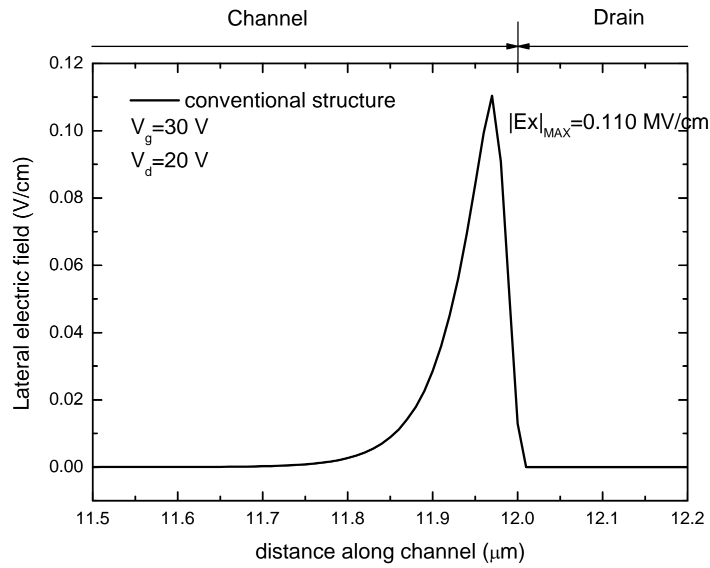


Fig. 2-6(a) The simulated lateral electric field of the conventional structure in on-sate operation

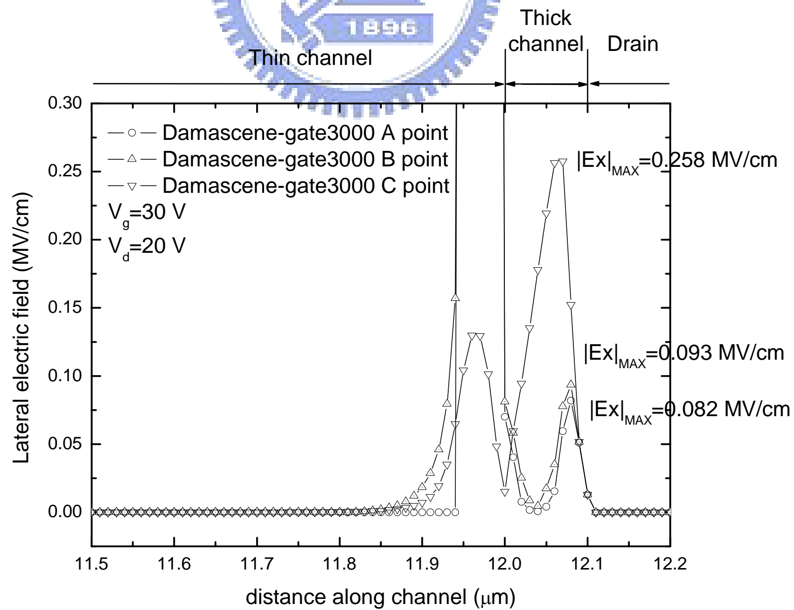


Fig. 2-6(b) The simulated lateral electric field of the 300 nm damascene-gated structure in on-sate operation

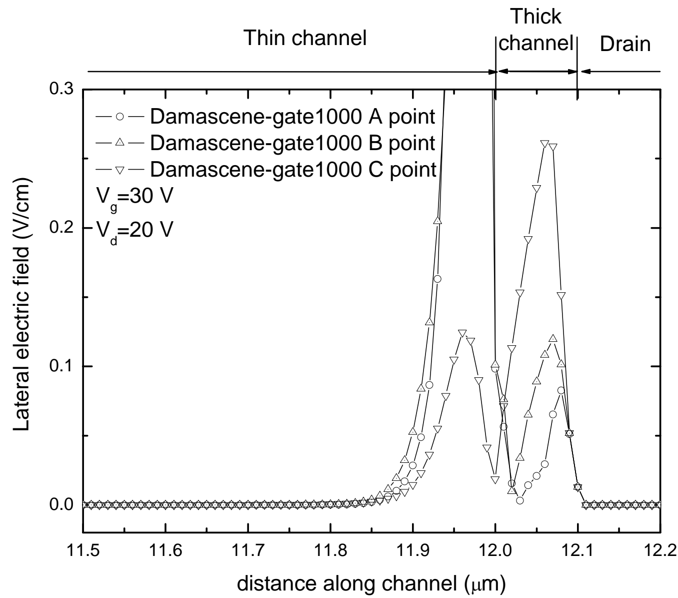


Fig. 2-6(c) The simulated lateral electric field of the 100 nm damascene-gated structure in on-sate operation

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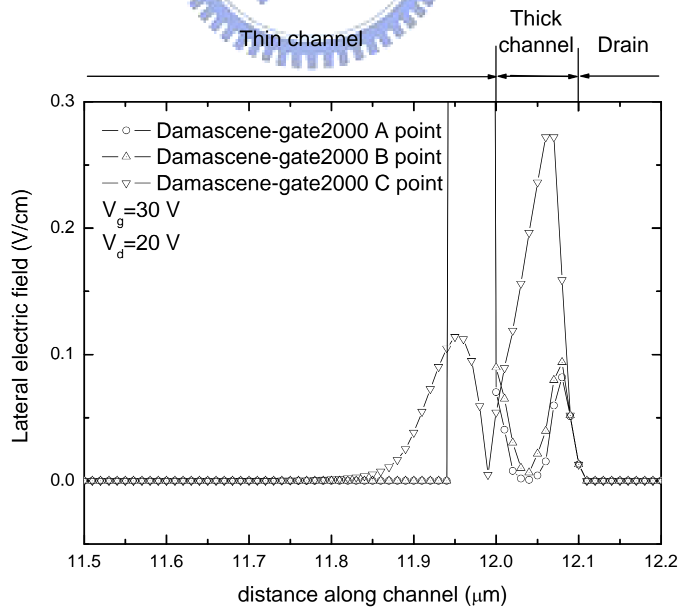


Fig. 2-6(d) The simulated lateral electric field of the 200 nm damascene-gated structure in on-sate operation

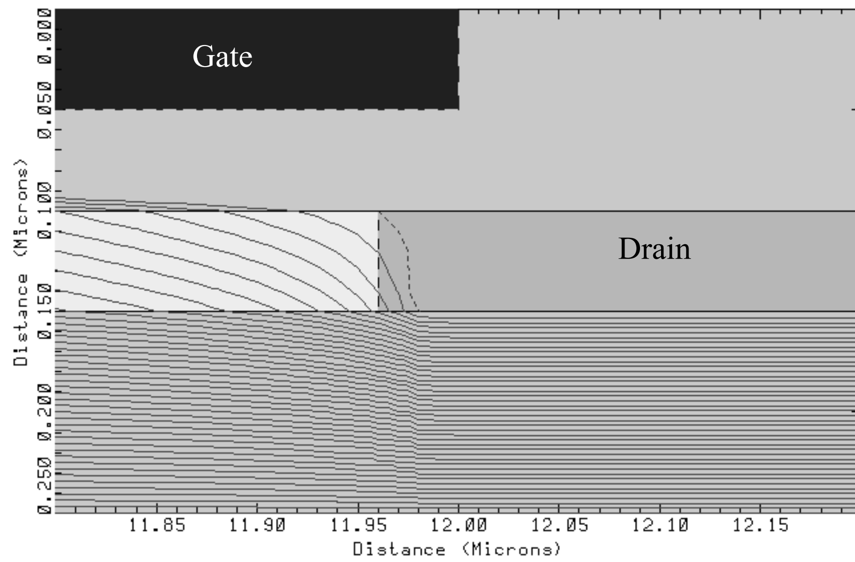


Fig. 2-7(a) The simulated potential distribution of the conventional structure in on-sate operation

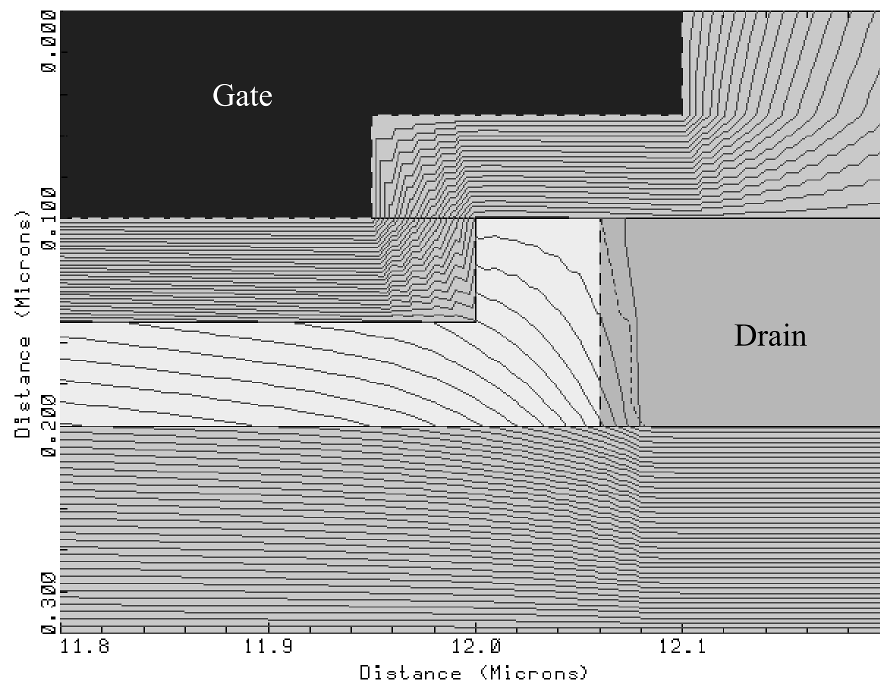


Fig. 2-7(b) The simulated potential distribution of the 100 nm damascene-gated structure in on-sate operation

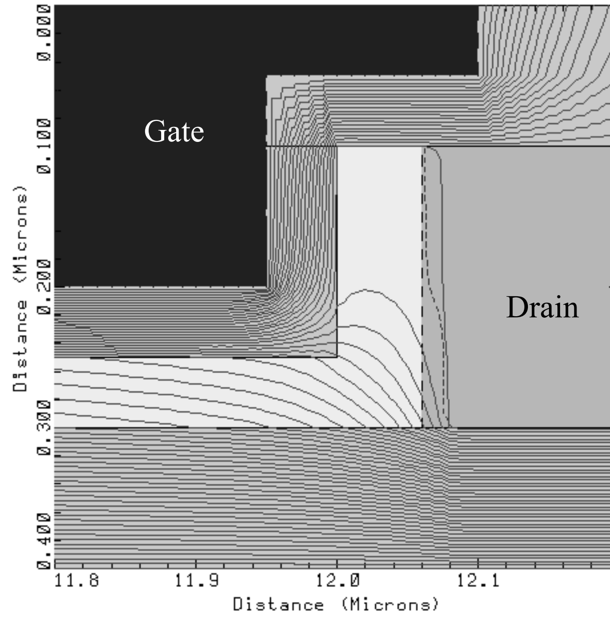


Fig. 2-7(c) The simulated potential distribution of the 200 nm damascene-gated structure in on-sate operation

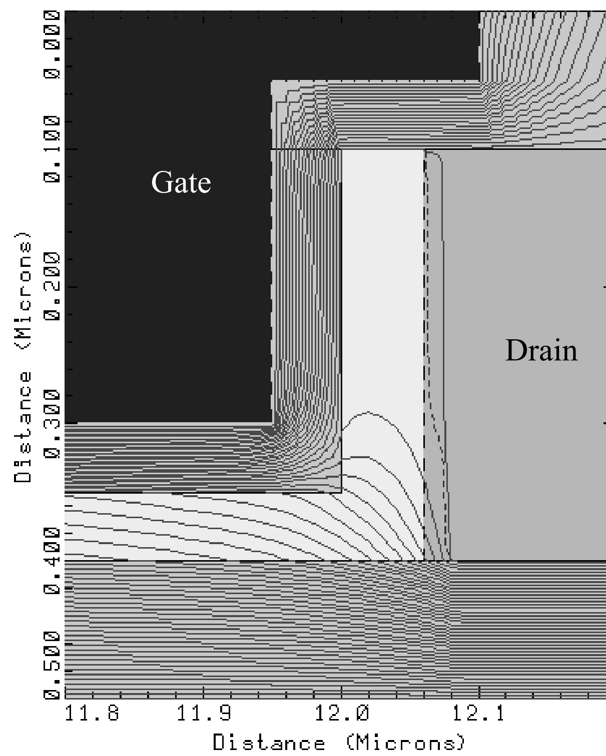
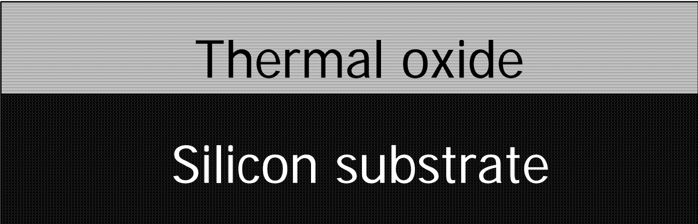
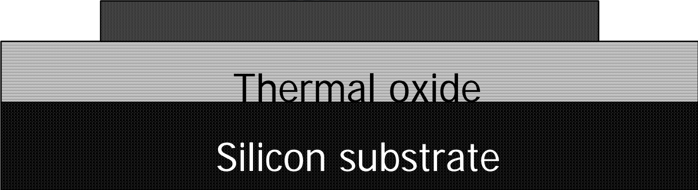


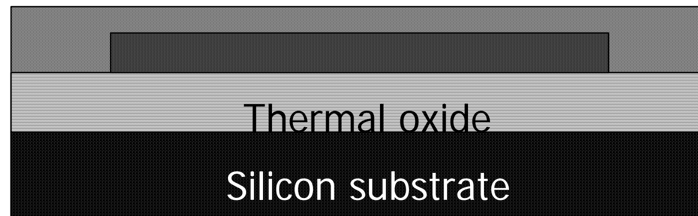
Fig. 2-7(d) The simulated potential distribution of the 300 nm damascene-gated structure in on-sate operation



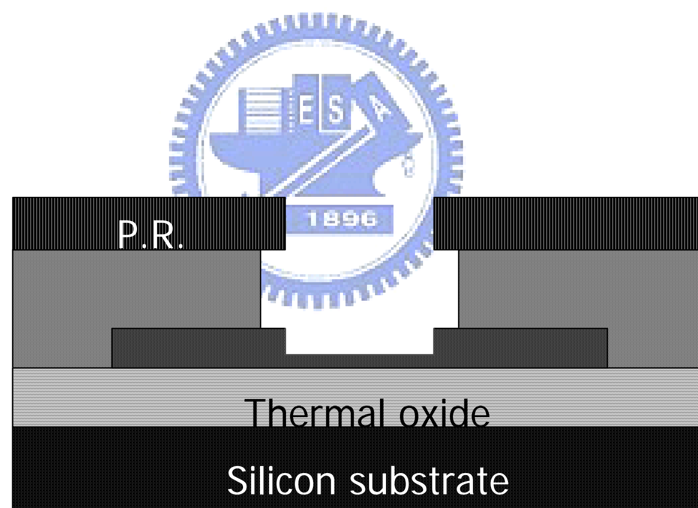
(a) Thermal oxidation



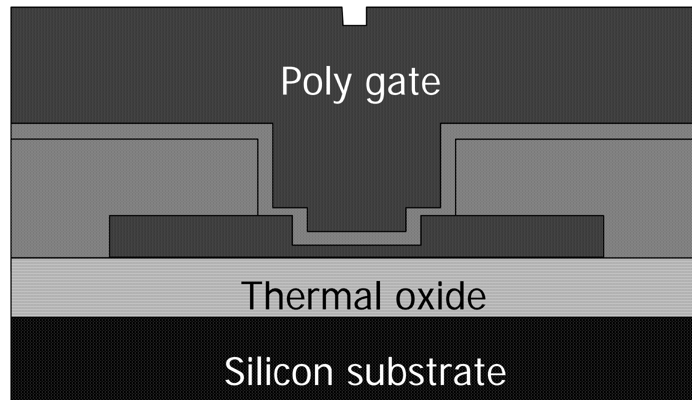
(b) LPCVD α-Si, Mask #1, RIE, SPC



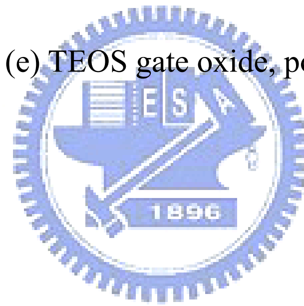
(c) TEOS oxide deposition, CMP

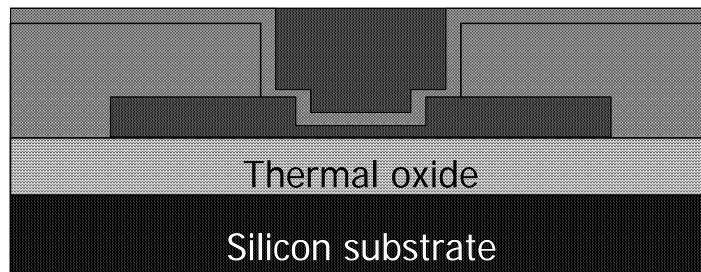


(d) Mask #2, RIE, wet etching

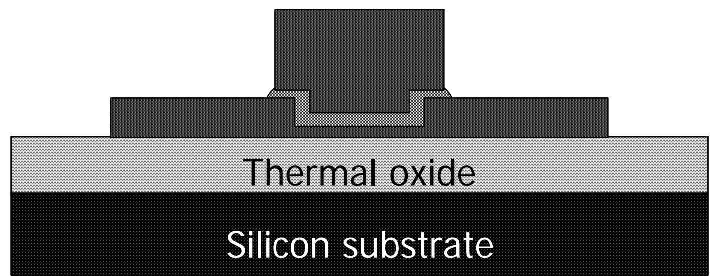


(e) TEOS gate oxide, poly gate

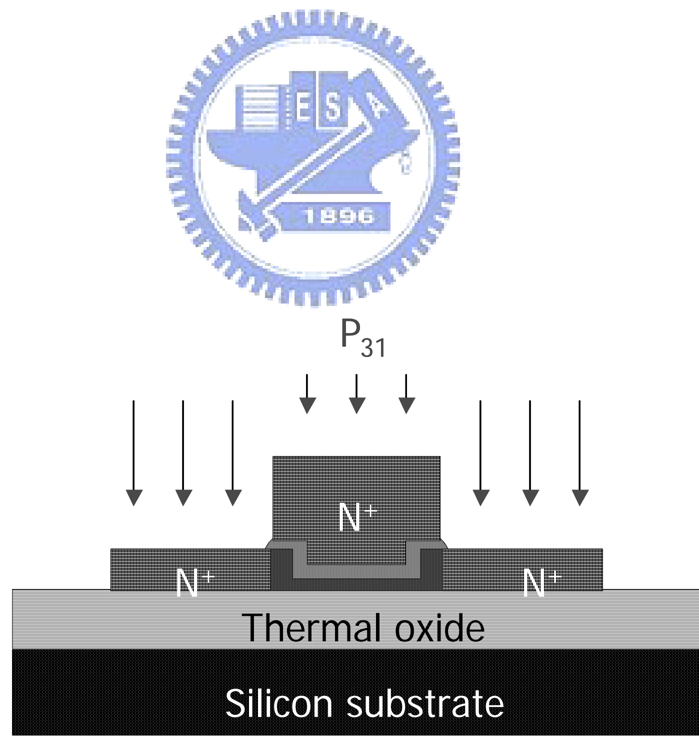




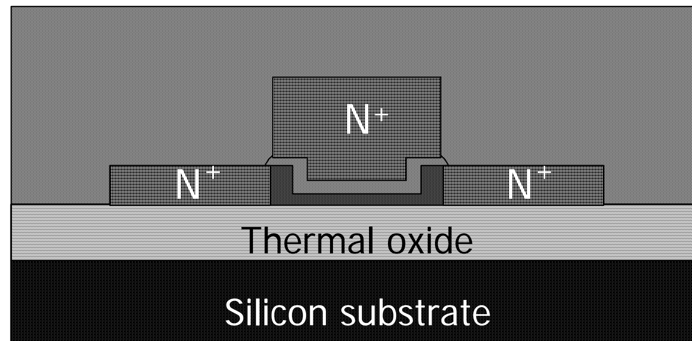
(f) CMP process



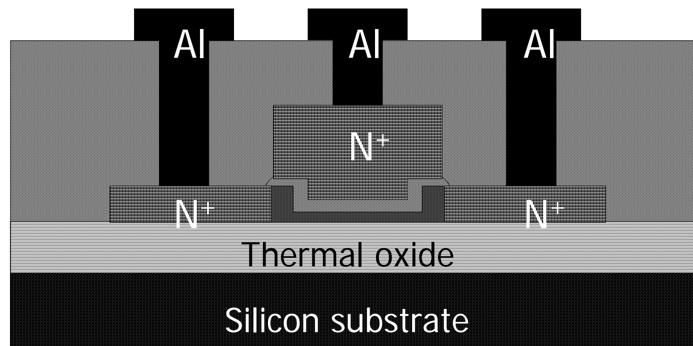
(g) B.O.E. etching



(h) Implantation and activation



(i) Passivation layer



(j) Al electrodes

Fig. 3-1 Process flow of fabricating low-temperature damascene-gated TFTs with thick S/D and thin channel

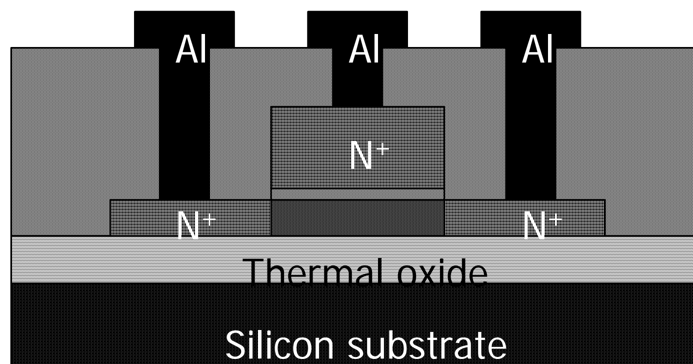
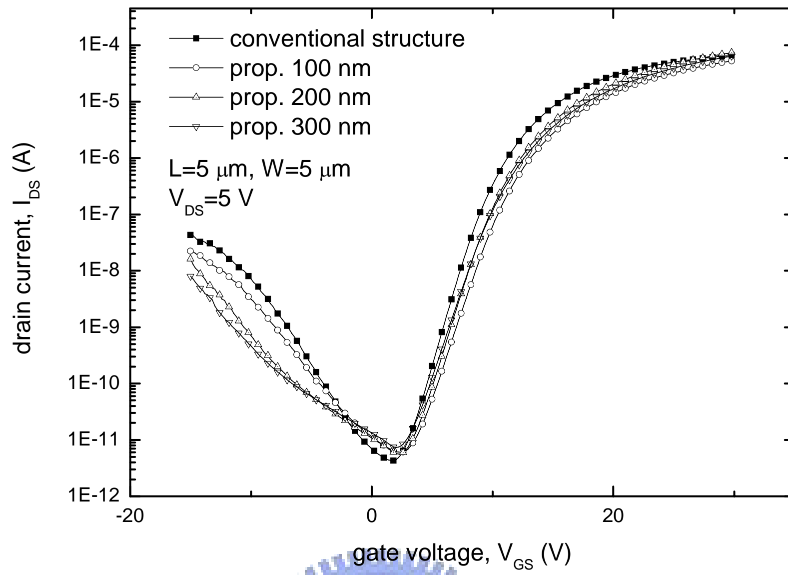


Fig. 3-2 The conventional TFT



E S A

Fig. 4-1 $I_{DS} - V_{GS}$ transfer characteristics of the proposed structure and conventional structure TFTs for V_{DS} = 5 V; W/L = 5 μm/5 μm

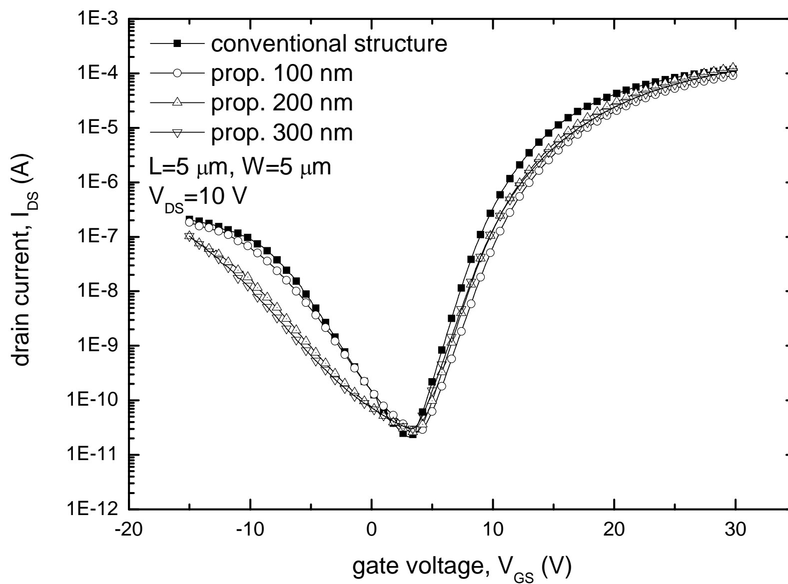


Fig. 4-2 $I_{DS} - V_{GS}$ transfer characteristics of the proposed structure and conventional structure

TFTs for V_{DS} = 10 V; W/L = 5 μm/5 μm

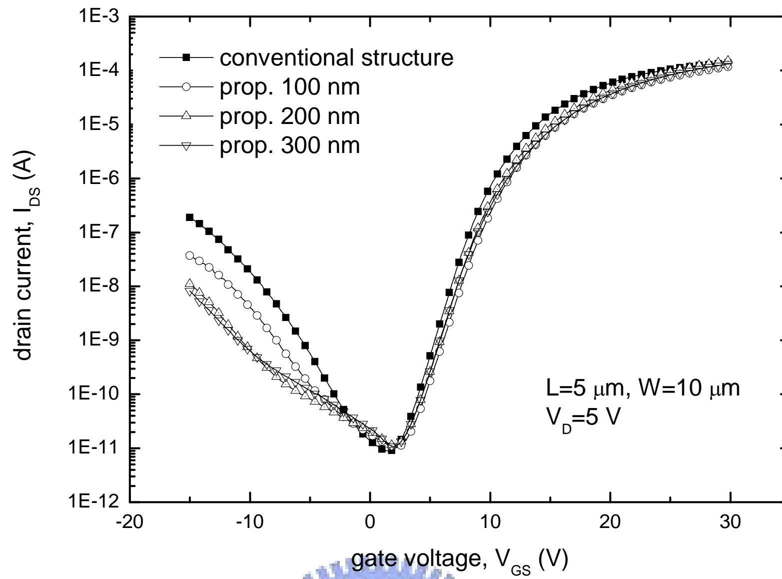


Fig. 4-3 $I_{DS} - V_{GS}$ transfer characteristics of the proposed structure and conventional structure TFTs for V_{DS} = 5 V; W/L = 10 μm/5 μm

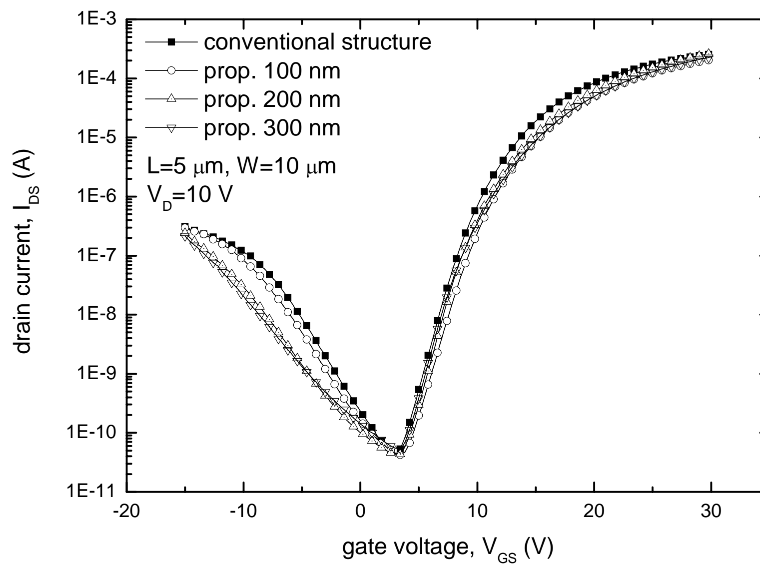


Fig. 4-4 $I_{DS} - V_{GS}$ transfer characteristics of the proposed structure and conventional structure

TFTs for V_{DS} = 10 V; W/L = 10 μm/5 μm

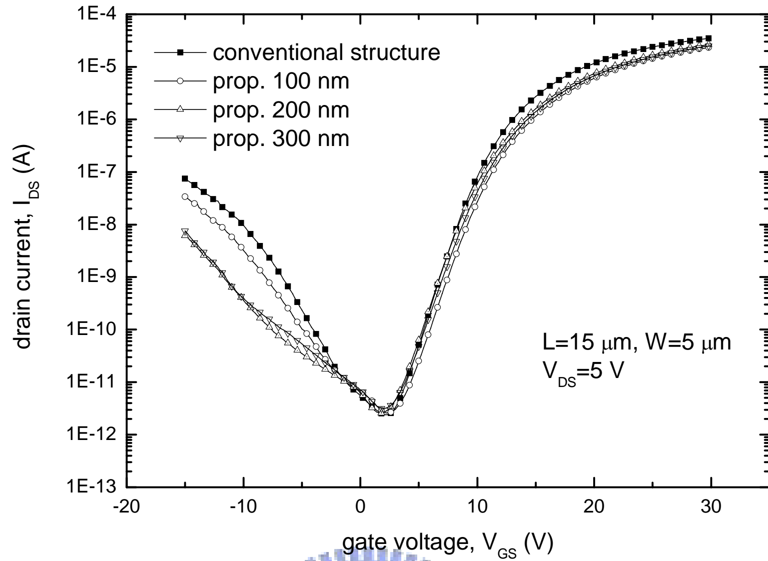


Fig. 4-5 $I_{DS} - V_{GS}$ transfer characteristics of the proposed structure and conventional structure TFTs for V_{DS} = 5 V; W/L = 5 μm/15 μm

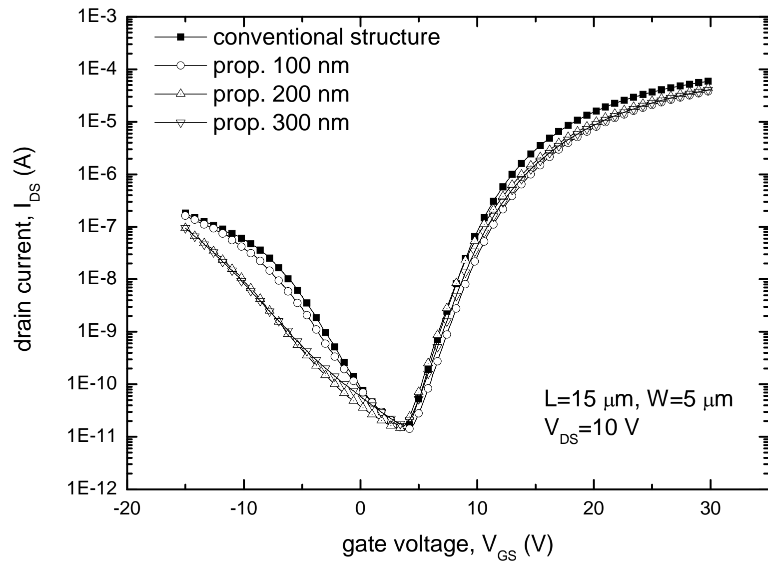


Fig. 4-6 $I_{DS} - V_{GS}$ transfer characteristics of the proposed structure and conventional structure

TFTs for V_{DS} = 10 V; W/L = 5 μm/15 μm

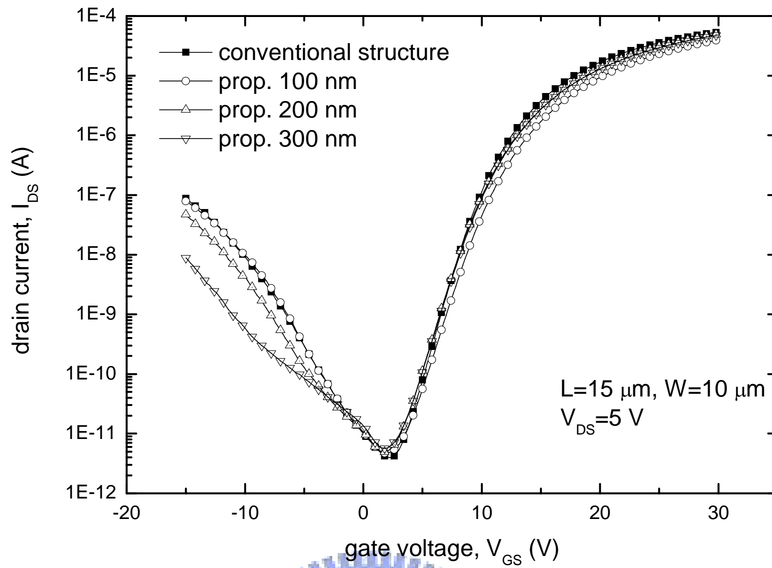


Fig. 4-7 $I_{DS} – V_{GS}$ transfer characteristics of the proposed structure and conventional structure TFTs for V_{DS} = 5 V; W/L = 10 μm/15 μm

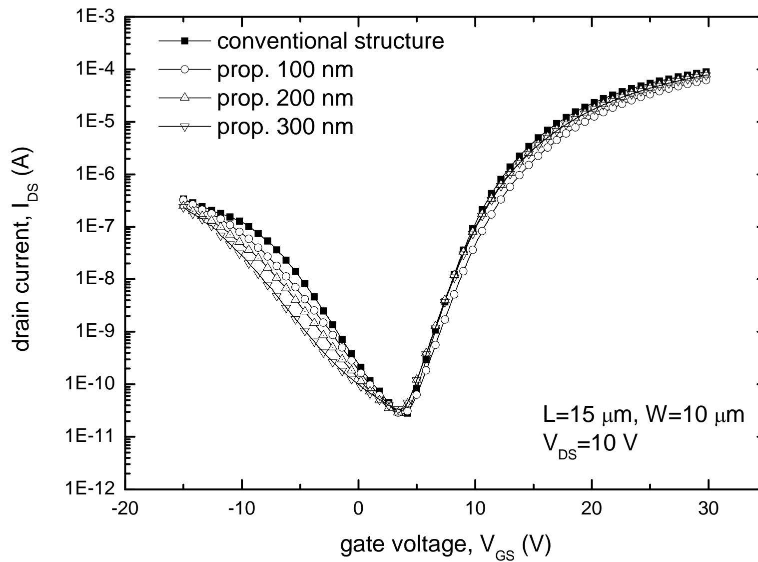


Fig. 4-8 $I_{DS} – V_{GS}$ transfer characteristics of the proposed structure and conventional structure

TFTs for V_{DS} = 10 V; W/L = 10 μm/15 μm

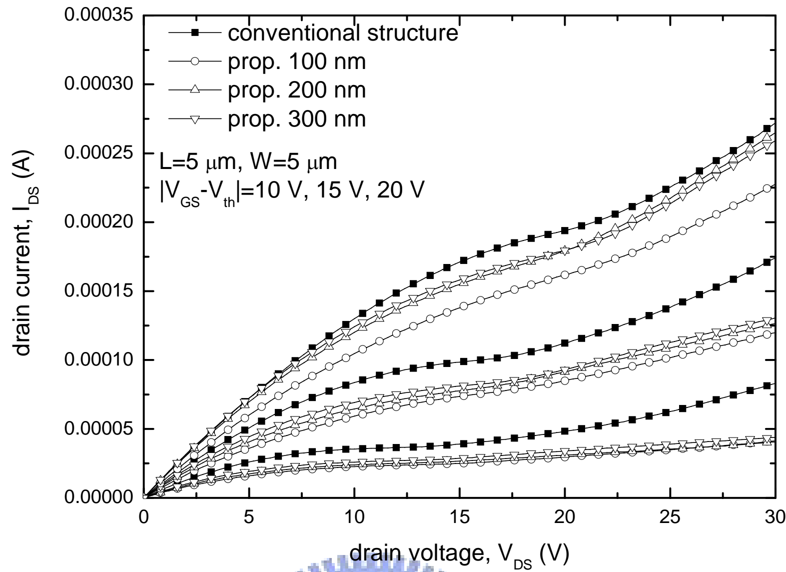


Fig. 4-9 I_{DS} – V_{DS} output characteristics of the proposed structure and conventional structure TFTs; W/L = 5 μm/5 μm

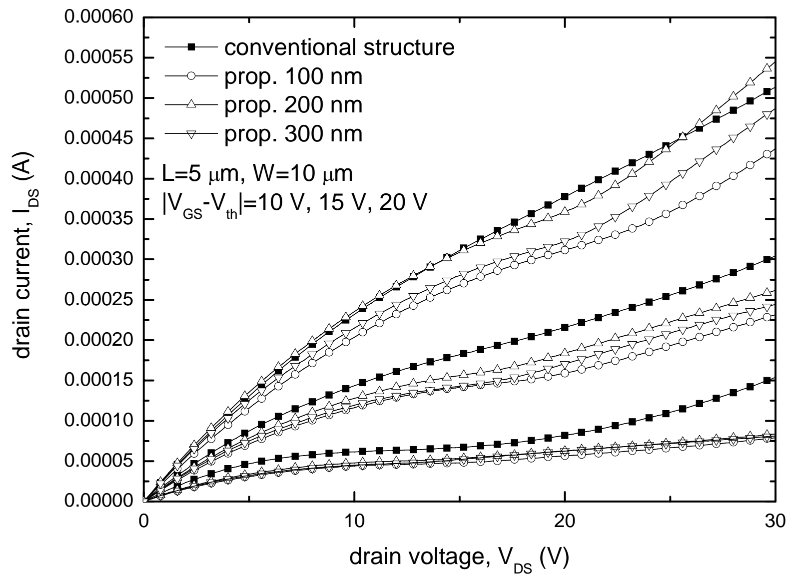


Fig. 4-10 I_{DS} – V_{DS} output characteristics of the proposed structure and conventional structure

TFTs; W/L = 10 μm/5 μm

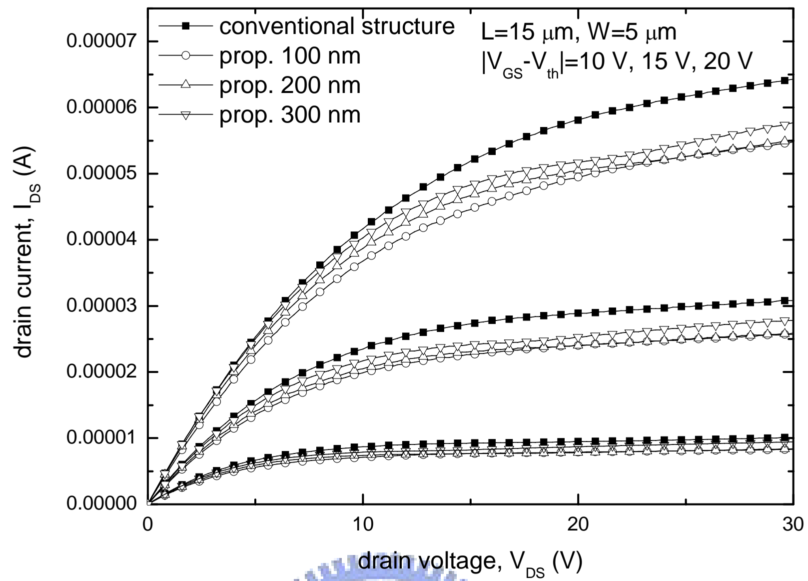


Fig. 4-11 $I_{DS} - V_{DS}$ output characteristics of the proposed structure and conventional structure TFTs; W/L = 5 μm/15 μm

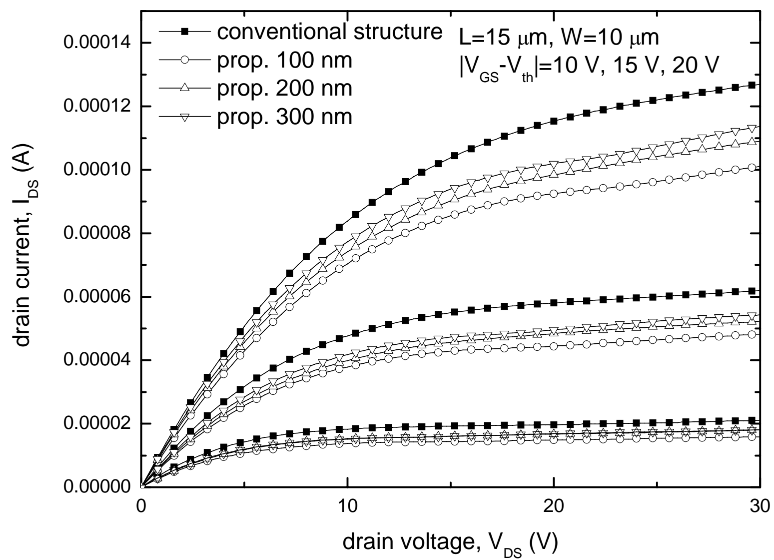


Fig. 4-12 $I_{DS} - V_{DS}$ output characteristics of the proposed structure and conventional structure

TFTs; W/L = 10 μm/15 μm

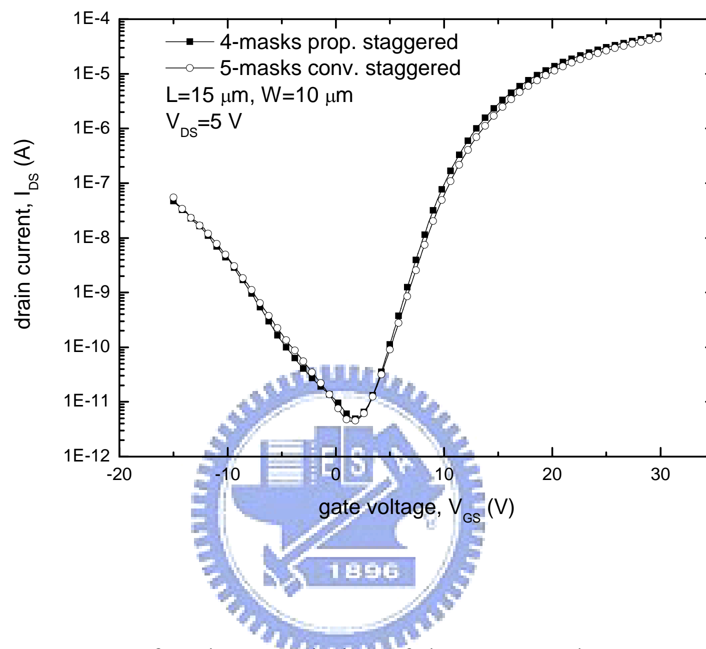


Fig. 4-13 $I_{DS} - V_{GS}$ transfer characteristics of the proposed structure and conventional structure with five masks