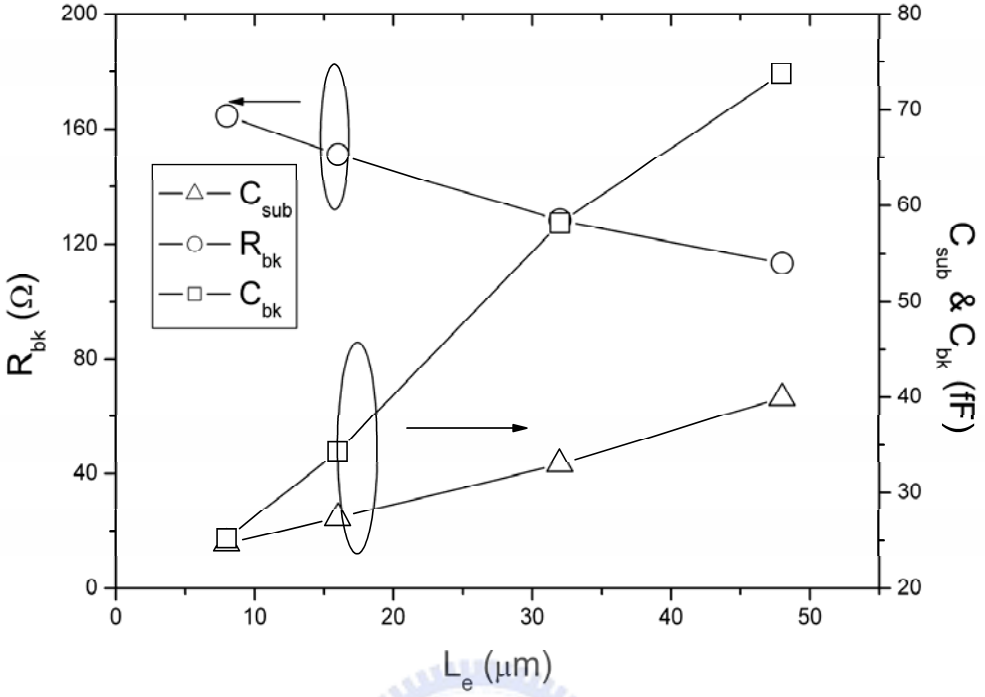


Fig. 4-1 Substrate parameters versus emitter length.

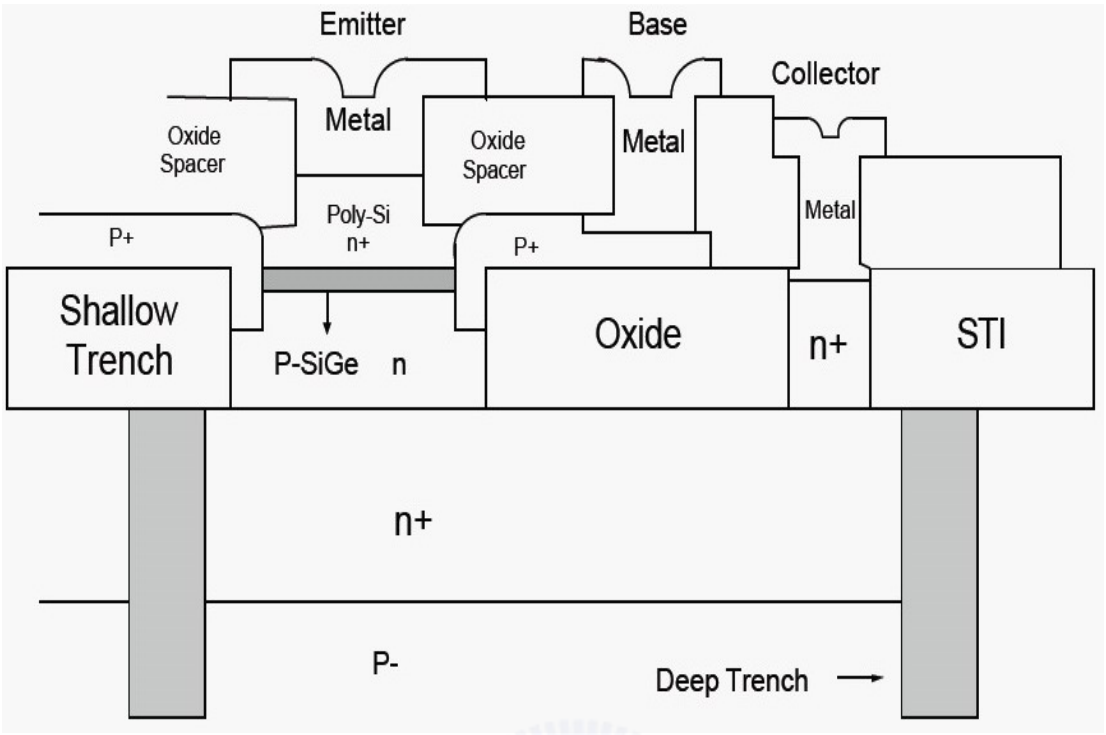


Fig.4-2 The schematic cross section of the SiGe HBT.

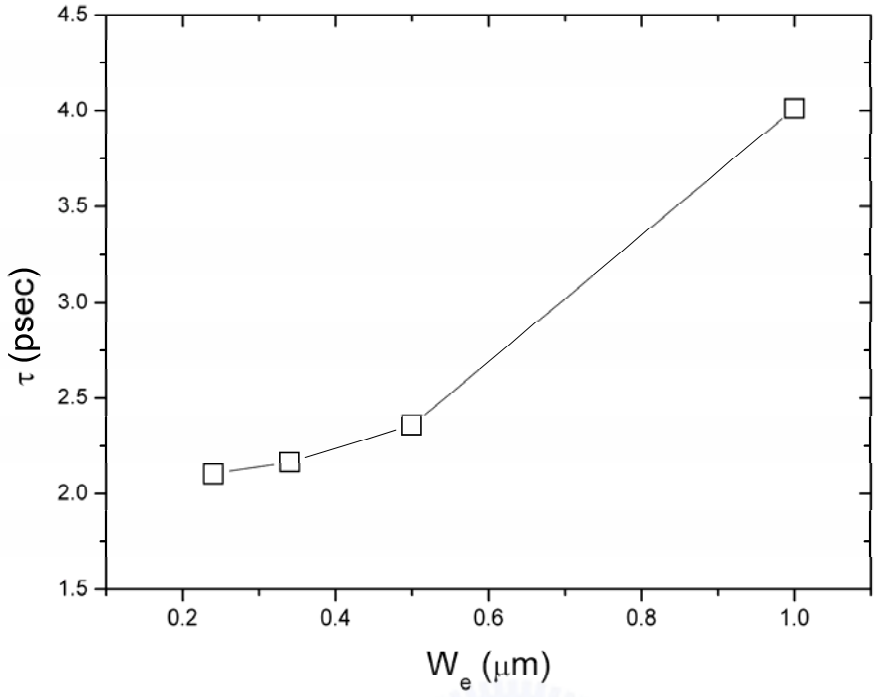


Fig.4-3 Excess phase delay versus emitter width.

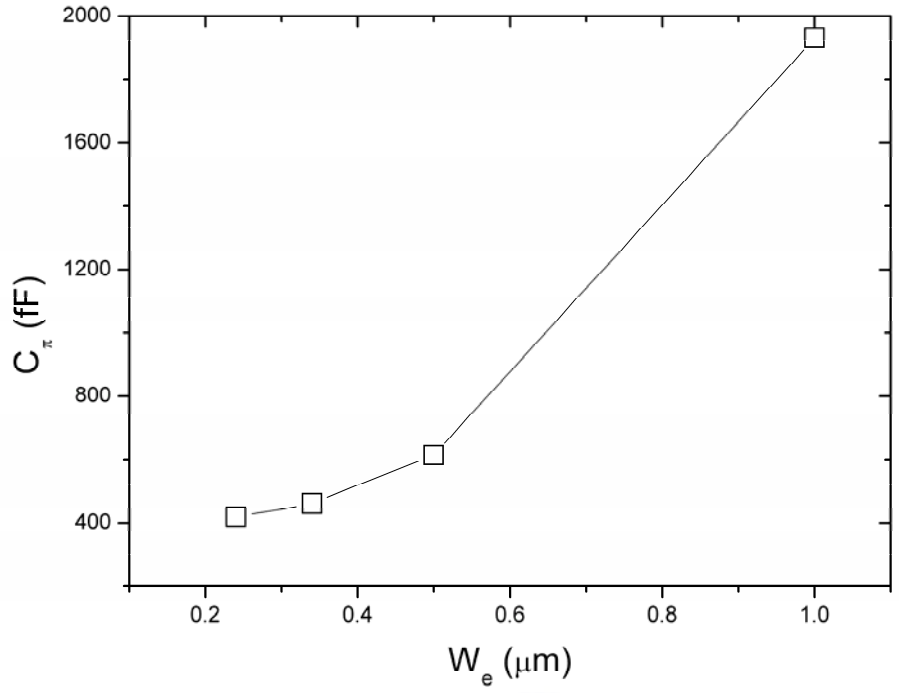


Fig. 4-4 Intrinsic base-emitter capacitance versus emitter width.

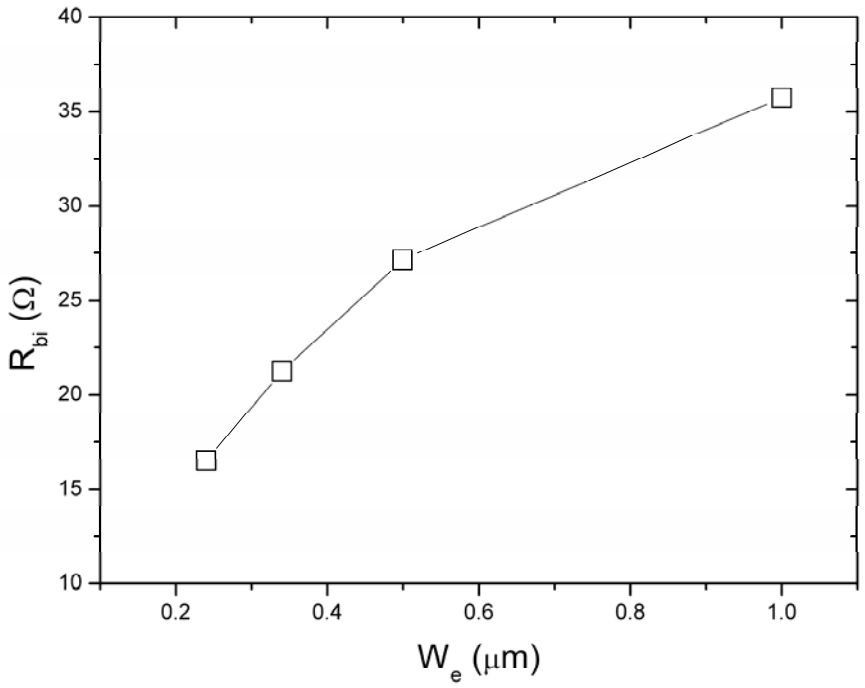


Fig.4-5 Intrinsic base resistance versus emitter width

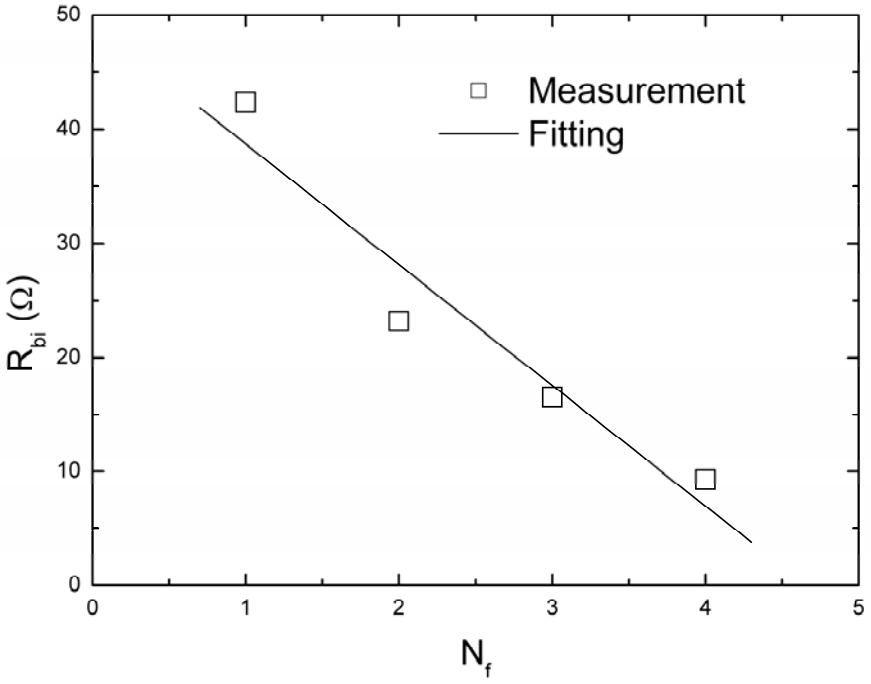


Fig. 4-6 Intrinsic base resistance versus finger number

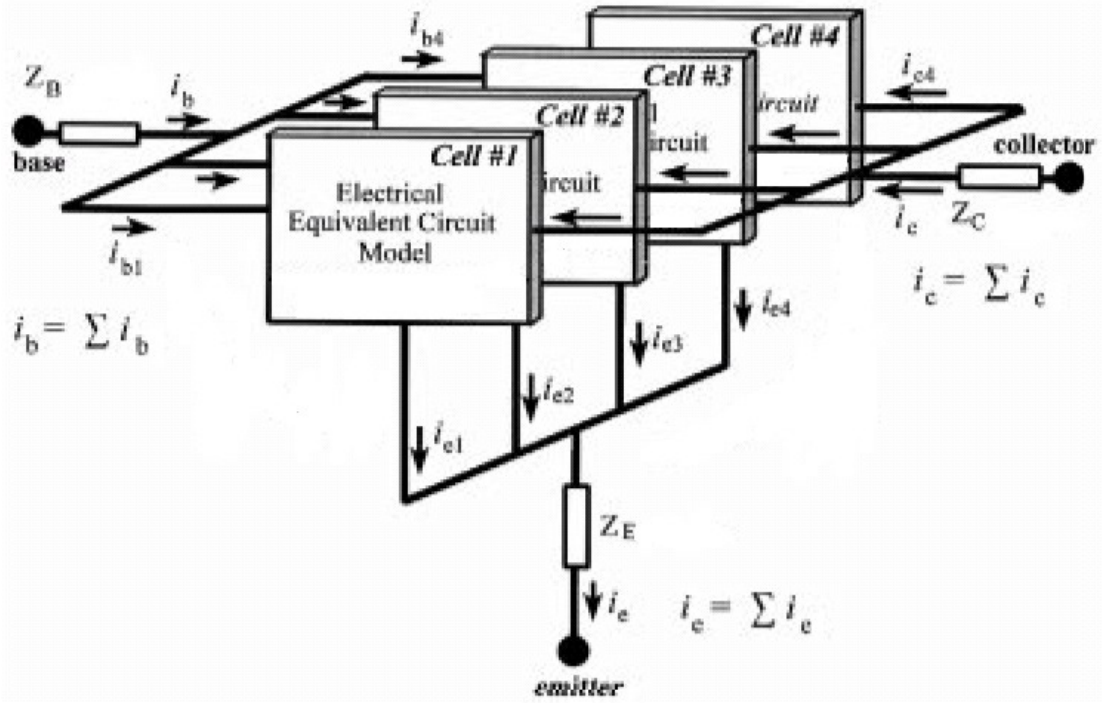
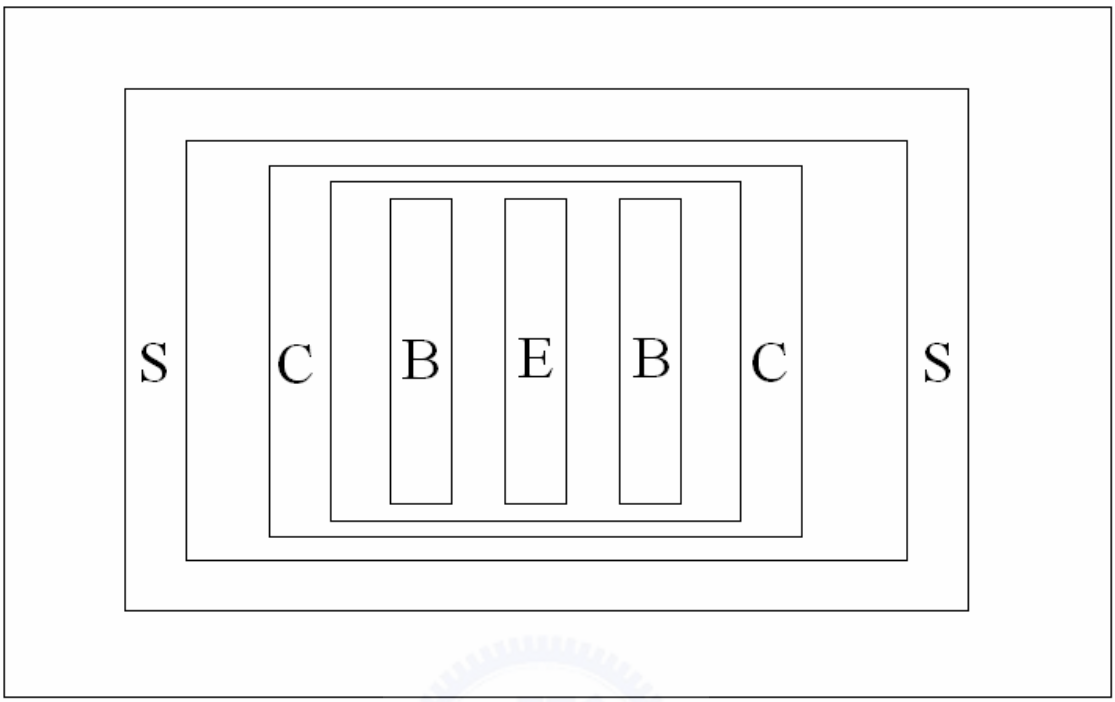
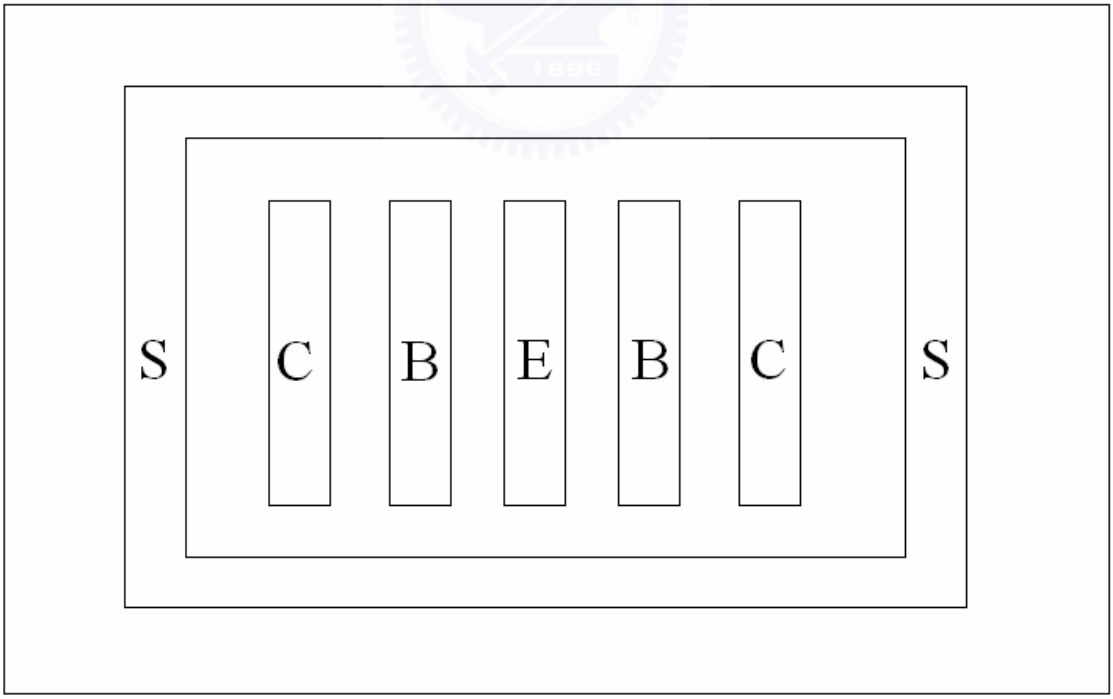


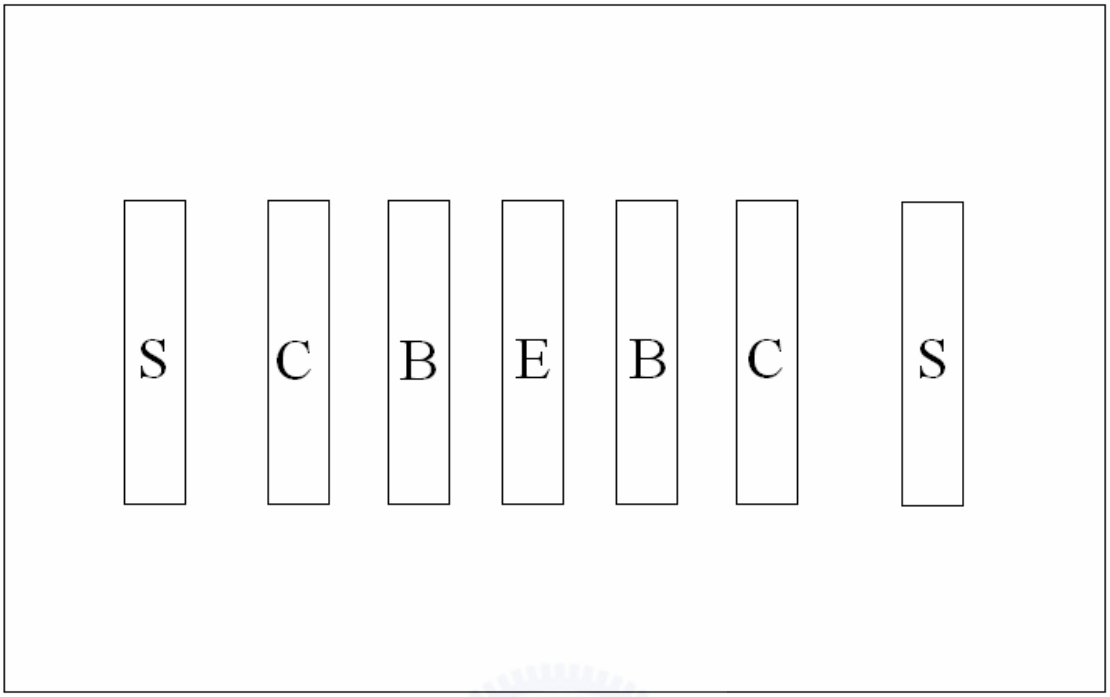
Fig. 4-7 The schematic of Multi-cell structure.



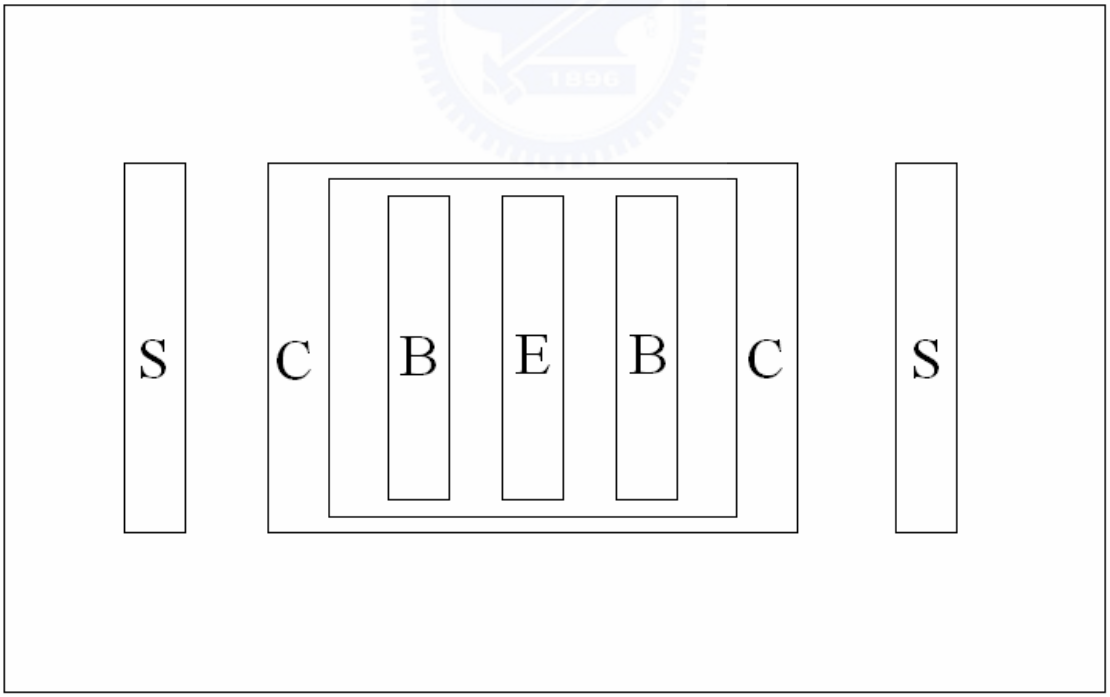
(a)



(b)



(c)



(d)

Fig. 4-8 Top View of (a) Ring Collector - Ring Substrate, (b) Strip Collector - Ring Substrate, (c) Strip Collector - Strip Substrate and (d) Ring Collector – Strip Collector

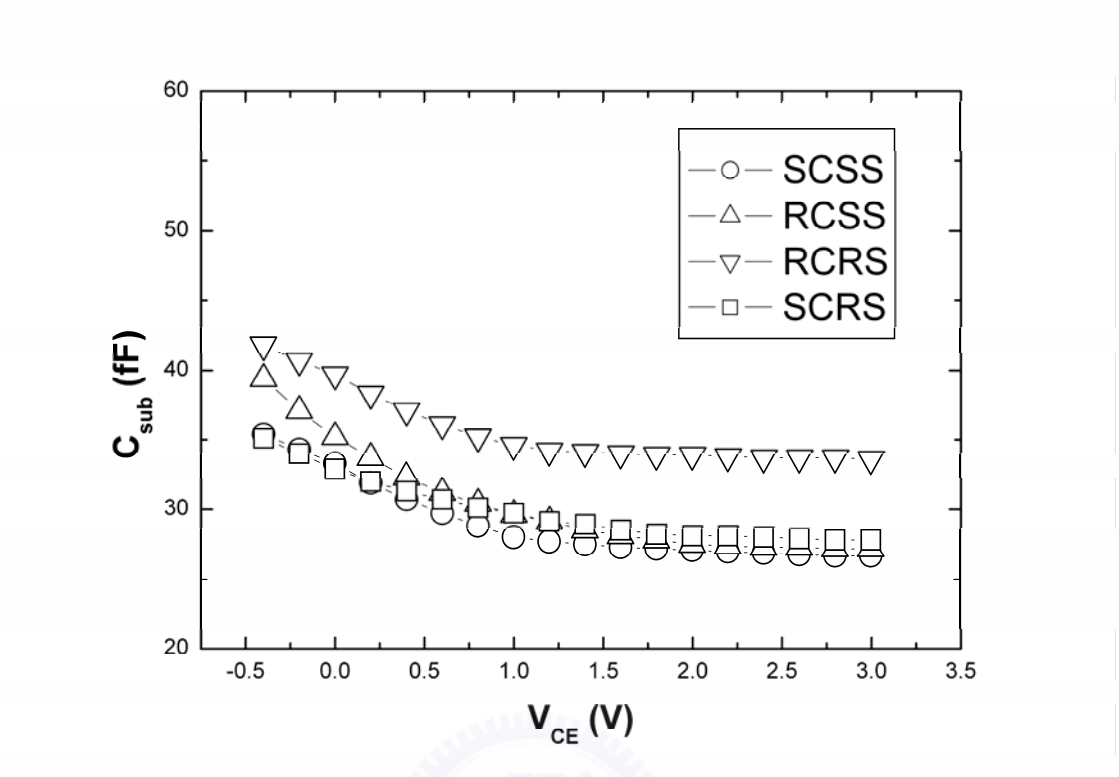


Fig. 4-9 Collector-voltage dependence of the extracted C_{sub} for SiGe HBTs biased at V_{BE}=0V and V_{CE} from -0.4V to 3V

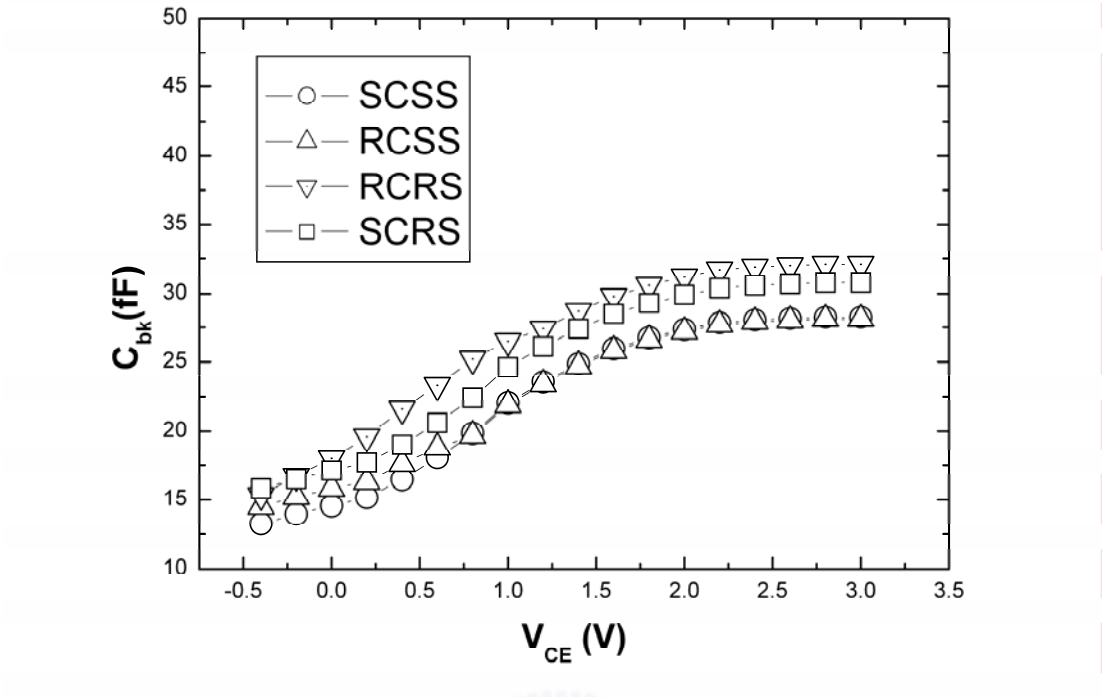


Fig. 4-10 Collector-voltage dependence of the extracted C_{bk} for SiGe HBTs biased at V_{BE}=0V and V_{CE} from -0.4V to 3V

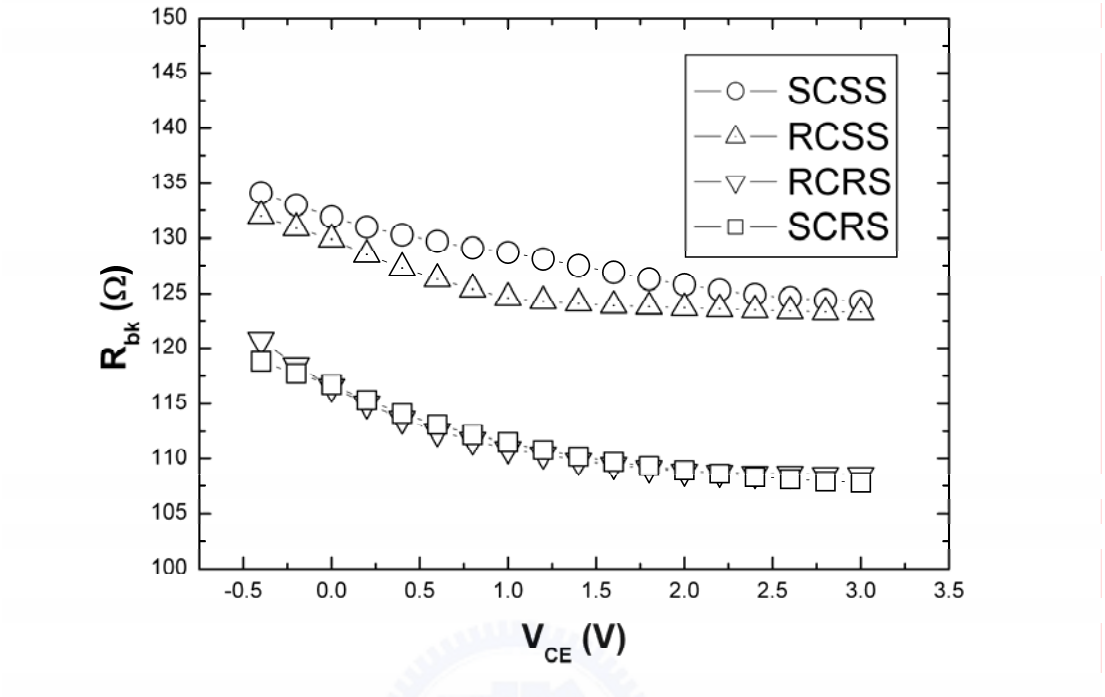
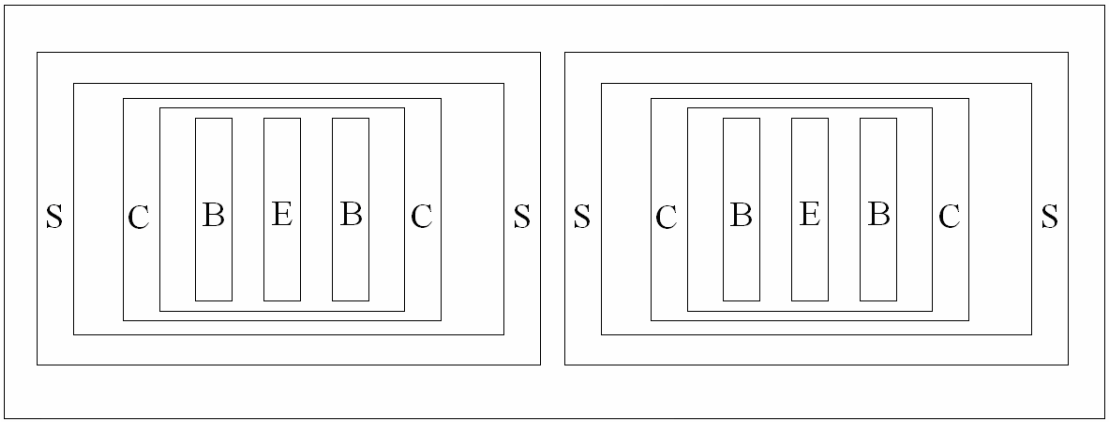
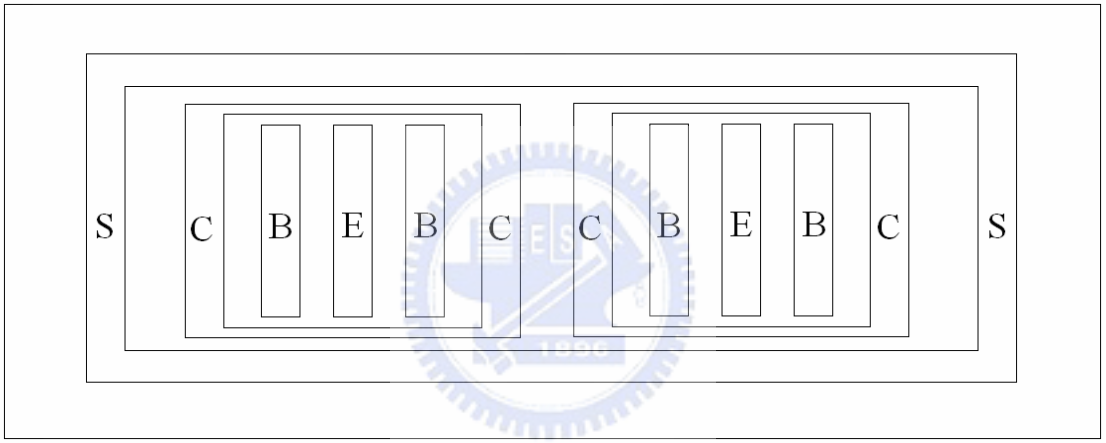


Fig. 4-11 Collector-voltage dependence of the extracted R_{bk} for SiGe HBTs biased at V_{BE}=0V and V_{CE} from -0.4V to 3V



(a)



(b)

Fig. 4-12 (a) Ring Collector – Parallel Ring Substrate, (b) Ring Collector – Outer Ring Substrate

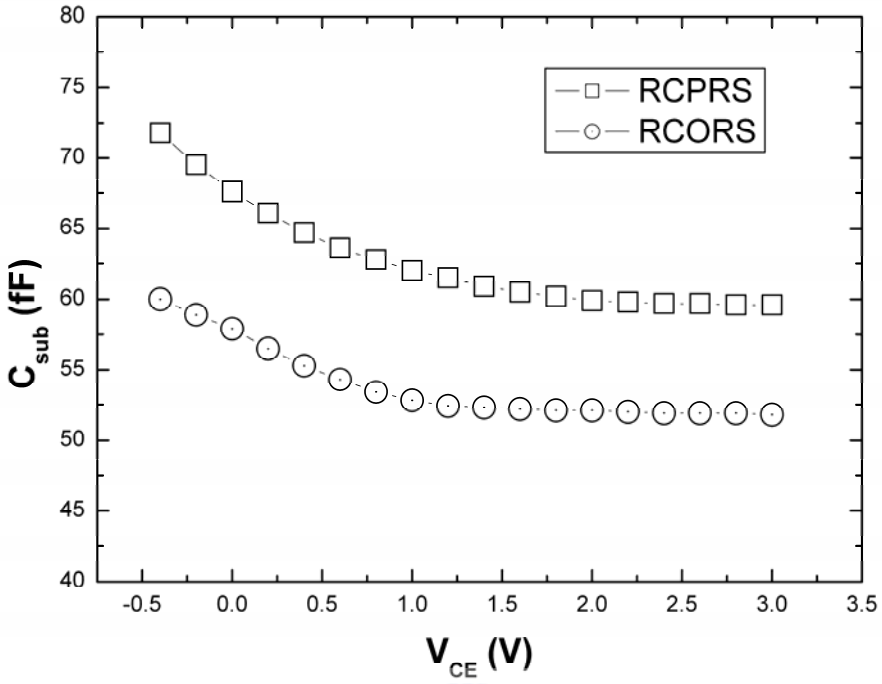


Fig. 4-13 Collector-voltage dependence of the extracted C_{sub} for SiGe HBTs biased at V_{BE}=0V and V_{CE} from -0.4V to 3V

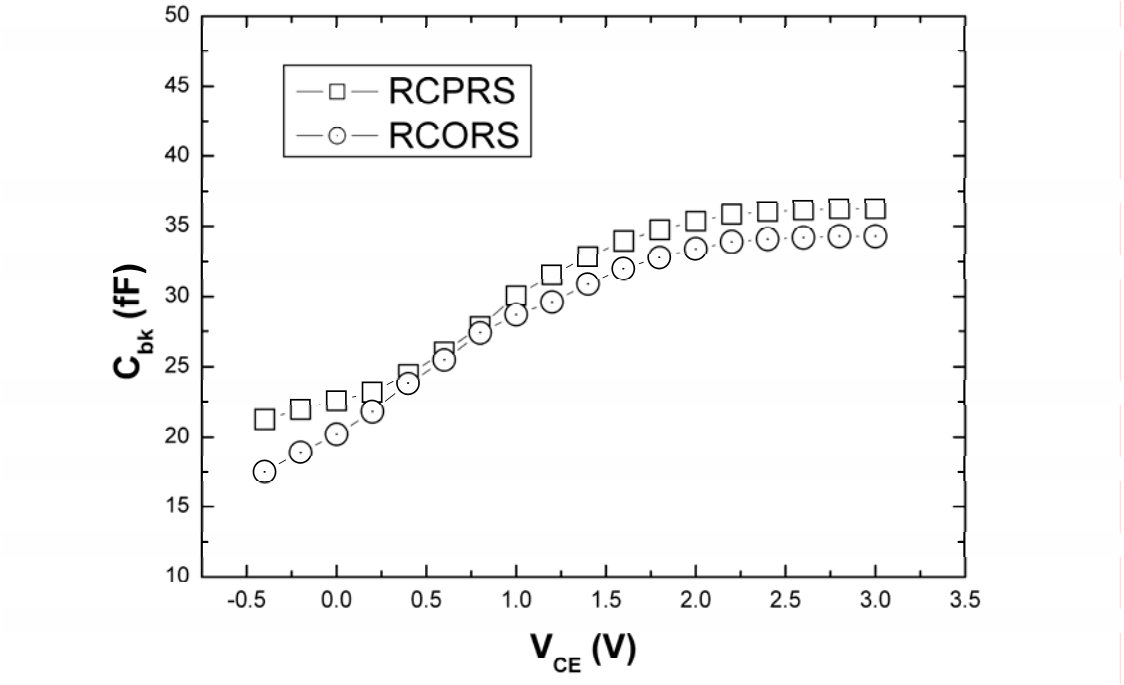


Fig. 4-14 Collector-voltage dependence of the extracted C_{bk} for SiGe HBTs biased at V_{BE}=0V and V_{CE} from -0.4V to 3V

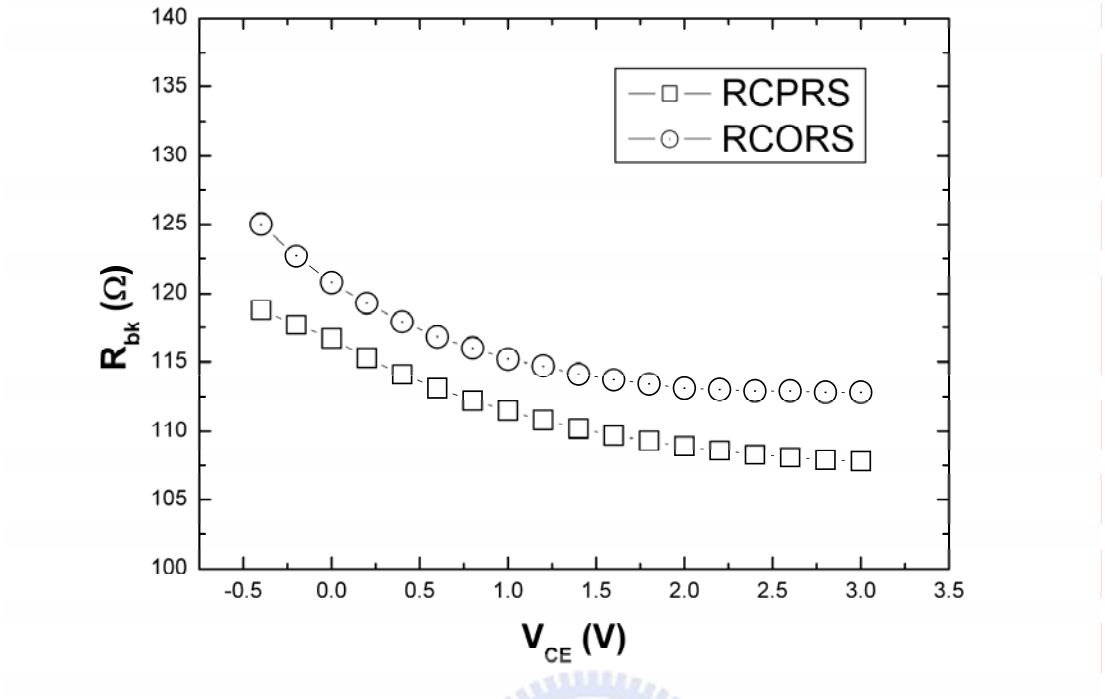


Fig. 4-15 Collector-voltage dependence of the extracted R_{bk} for SiGe HBTs biased at V_{BE}=0V and V_{CE} from -0.4V to 3V